Microelectronic Engineering 302 (2026) 112422

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Research paper

A statistical characterization of dielectric breakdown in FDSOI nanowire transistors

R. Goyal *, A. Crespo-Yepes, M. Porti, R. Rodriguez, M. Nafria

Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona (UAB), 08193, Bellaterra, Barcelona, Spain

ARTICLE INFO

Keywords:
Failure
Dielectric breakdown
FD-SOI
NW FETs
High-k
Reliability
Power consumption
Lifetime

ABSTRACT

In this work, dielectric breakdown (BD) and post-BD conduction in ultimate FDSOI nanowire (NW) transistors with Ω-gate and high-k dielectric have been investigated. The experiments show that BD in largely scaled NW transistors differ significantly from that in bulk planar transistors. Several types of post-BD behaviours have been observed, some of which not only hinder the device performance, but also jeopardize the integrity of the nanowire structure and materials. A comprehensive study of the phenomena has been performed on pMOS and nMOS with different widths and lengths, under different temperature conditions.

1. Introduction

Dielectric Breakdown (BD) of the gate oxide has been one of the most important reliability concerns in CMOS technologies due to its impact on gate stack dielectric conduction. As a result, it significantly modifies the device performance and eventually provokes its final failure [1–7] and loss of the circuit functionality [8–10]. In the last few decades, BD (i.e., Soft, Progressive and Hard BD [11–13]) has been extensively studied in planar bulk MOSFETs with SiO_2 and Hf-based high-k gate dielectrics [4–6,13]. The post BD conduction and the BD reversibility observed under certain electrical conditions [14–16] was also evaluated. The impact of BD on the circuit performances has also been widely analysed from the circuit functionality and system consumption perspectives [13,17–20]. In more advanced device architectures, such as FinFETs, or SOI technologies, dielectric BD remains a key factor for being one of the lifetime-limiting challenges for these technologies [21,22]. The ultimate Fully Depleted Silicon-On-Insulator (FDSOI) transistors with nanowire architecture (device channel confinement like in nano sheets) are also affected by the BD [23–25], but a complete description of the BD phenomenology and an evaluation of its impact on device performance are still lacking. In this work, BD in FDSOI NW high-k Ω-gate transistors [26] has been studied. The phenomenology has been described, the BD parameters have been statistically analysed, and the temperature effects have been evaluated. The pre- and post-BD behaviours have been investigated and their dependence on the device type, area and architecture has been addressed. A preliminary analysis of the BD impact on the device performance was also done. The results indicate that BD in FDSOI NW high-k transistors show some particular characteristics and much more post-BD variability compared to some previous technologies.

2. Device description and experimental procedure

The devices used in this work were nMOS and pMOS FDSOI Ω-gate nanowireFETs (NW-FET) fabricated at CEA-LETI [26]. The gate is a high-k stack (HfSiON/TiN) with EOT = 1.3 nm, H_{NW} = 11 nm and the buried oxide thickness of 145 nm. A 3D sketch and the cross-section of a single device are shown in Fig. 1. Devices with two different widths were studied: (1) W = 30 nm (1-channel) with lengths ranging from 20 nm to 1 μm, and (2) W_{eff} = 300 nm (split in 10 channels of W = 30 nm) with two lengths (20 and 40 nm). Ramped voltage stresses (RVS) were applied to the gate (from 0 to |10 V|, with V_D=V_S = 0 V) to induce oxide wear out and BD. No current limitation was applied during the RVS stress. The I_G-V_G and the I_D-V_G characteristics of the transistors were registered before and after the RVS test to study the performance of the fresh device and after inducing the BD. Unless stated, measurements were carried out at room temperature, though some tests at 85 °C and 125 °C were also performed on pMOS devices. A total of approximately 500 transistors has been measured, which allow the statistical analysis on the BD parameters.

* Corresponding author.
E-mail address: rishab.goyal@autonoma.cat (R. Goyal).

https://doi.org/10.1016/j.mee.2025.112422
Received 30 September 2025; Accepted 5 October 2025
Available online 6 October 2025

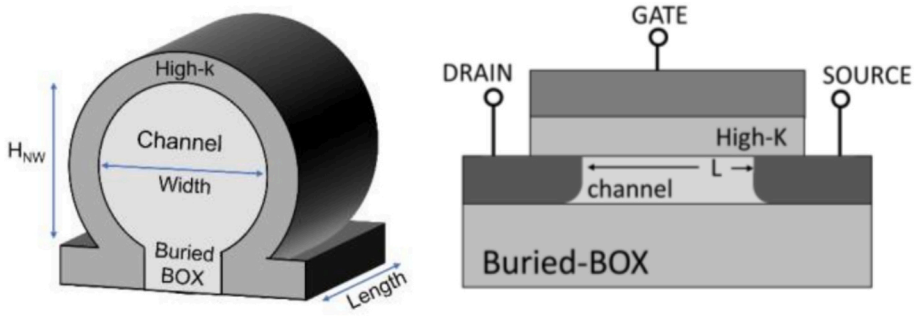

Fig. 1. (left) 3D sketch of the Ω-Gate NW FD-SOI transistors (high-k with EOT = 1.3 nm, H_{NW} = 11 nm and Buried Oxide Thickness = 145 nm). (right) Transistor cross-section [26].

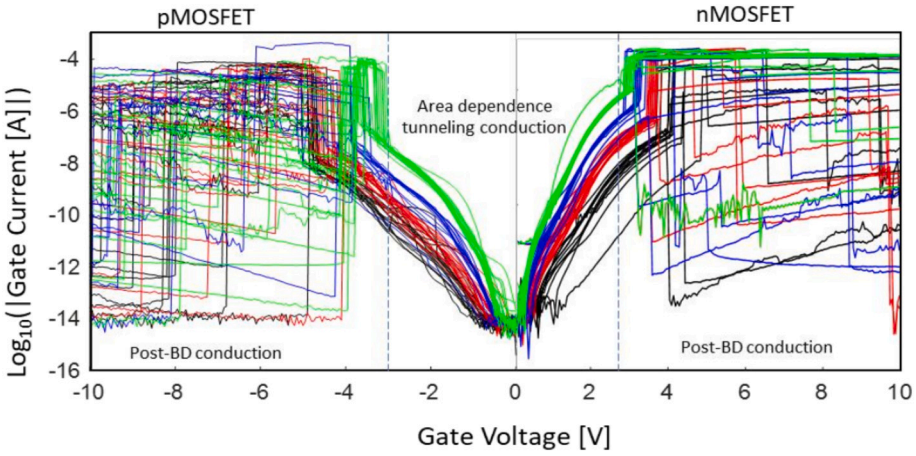

Fig. 2. I-V curves measured during the RVS test applied to provoke the BD in unichannel nMOS and pMOS transistors, with W = 30 nm and L = 20 nm (black), 40 nm (red), 120 nm (blue), and 1000 nm (green). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

3. BD phenomenology

First, the pre- and post-BD behaviours of the devices have been qualitatively investigated. Fig. 2 shows several examples of typical I_G-V_G curves measured during RVS, for nMOS and pMOS devices with W = 30 nm and different lengths: L = 20 nm (black lines), L = 40 nm (red lines), L = 120 nm (blue lines), and L = 1000 nm (green lines). In all cases, when voltages are lower than ~|4 V| (i.e., before BD), tunnelling through the device gate area controls the gate current [23], showing area dependence. Also, for devices with the same area, device-to-device variability is observed. As expected, there is a sudden jump in the gate current, identified as the BD event, which occurs at a voltage which is dependent on the gate area. Fig. 2 shows that, after BD, different behaviours of the gate current can be observed (as shown in detail in Fig. 3). The results also show that device-to-device variability is much larger than that measured before BD, with gate currents spanning over ten decades. In this sense, an important observation is that, after BD, the gate current suddenly decreases in many devices, appearing as an abrupt current drop (from now onwards named as Current Drop, CD). These observations are consistent with those reported in [23], though they were not analysed in detail. In this work, a detailed analysis of the observed phenomenology is presented.

Despite the extremely large variability in the gate dielectric conduction after BD, as shown in Fig. 2, the observed post-BD phenomenology can be classified into four different cases, according to how BD and CD are captured. Fig. 3 shows that these 4 cases appeared in both unichannel (red) and multichannel (black) nMOS devices. The same qualitative behaviour has also been observed for pMOS devices (not shown). Fig. 3a shows a typical BD event (case A), like those observed in planar bulk technologies. It appears as a sudden jump of the gate current that leads the gate dielectric to a high conductive state, where the gate current is driven by the BD path. However, in most of the measured devices, an abrupt Current Drop (CD) is also observed (as shown in Fig. 3b, c and d). In some devices, CD is observed at a higher voltage than BD voltage (case B, Fig. 3b); while in others, the BD event is immediately followed by the CD (case C, Fig. 3c). In other devices, only CD is registered (case D, Fig. 3d). The comparison of the four behaviours suggests that in cases C and D, BD does occur but the CD triggers so fast that makes the typical large post-BD conduction non-observable due to the measurement hardware sampling limitations (~5–10 milliseconds in the current range of interest). As a result, BD related currents increase is either partially observed (Fig. 3c) or not registered at all (Fig. 3d). Note that, in many cases, the gate current after CD is very low or almost negligible, close to the noise level of the system, which suggests that the BD path is no longer contributing to the gate conduction anymore.

Table 1 shows the percentage of devices displaying case A (only BD) and cases B, C and D (BD followed by CD), for each architecture (uni or multichannel devices), channel lengths and types (nMOS and pMOS). Clear differences are observed in the occurrence percentages. For nMOS, while most multichannel devices (>90 %) show a CD event, only around 50 % of the unichannel devices do regardless of L. However, for pMOS, CD is predominantly observed (>90 %) in both architectures and all L's. When focussing on CD occurrence, case C events are marginal, except in long unichannel pMOS, in which cases C and D seems to be exchanged. Therefore, we will mainly focus on cases B and D. For these cases, regarding the dependence on L for the unichannel devices, opposite trends have been observed, independently of the device type, i.e., whereas the probability of case B increases with L, the occurrence

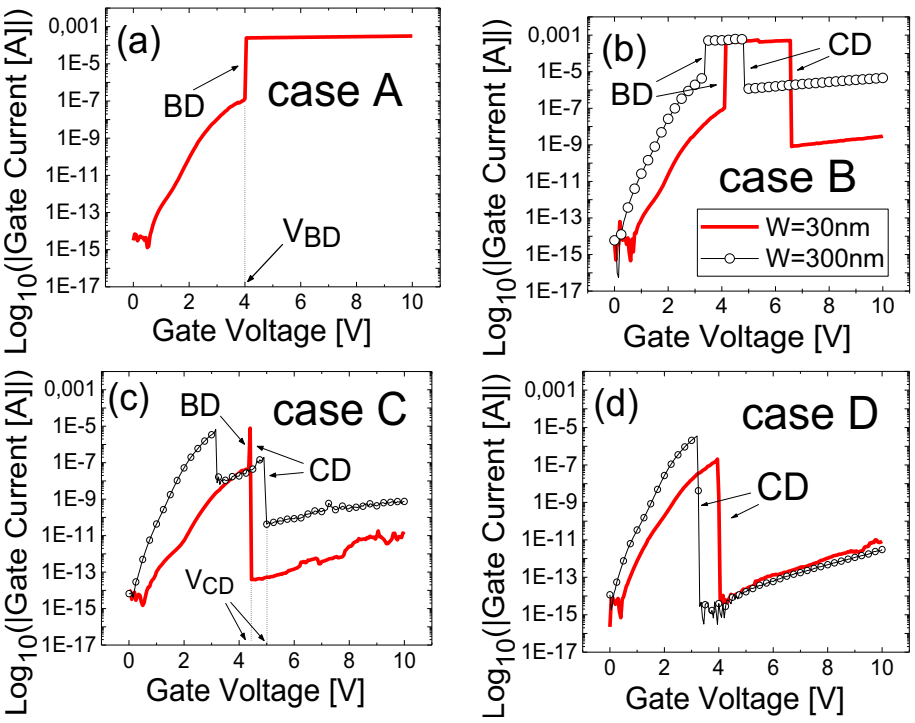

Fig. 3. Typical I_G-V_G curves measured during the RVS applied to the gate terminal to provoke the BD in nMOS transistors with W/L = 30 nm/20 nm (red line) and W/L = 300 nm/40 nm (black symbols). V_G is given in absolute value. From left to right and top to bottom: (i) a typical BD event (case A), (ii) BD-to-CD process (case B), (iii) fast BD-to-CD process (case C), and (iv) non-measurable BD-to-CD process (case D). Similar qualitative results are also obtained for pMOS devices. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 1
Probability of occurrence of case A (only BD) and cases B, C and D in which BD is followed by CD event, for the two architectures (uni or multichannel), device type (nMOS and pMOS) and channel lengths.

Device Length	nMOS cases				pMOS cases			
1-channel	A	B	C	D	A	B	C	D
20 nm	42 %	21 %	7 %	30 %	5 %	60 %	5 %	30 %
40 nm	47 %	30 %	0 %	23 %	6 %	42 %	0 %	42 %
120 nm	36 %	43 %	0 %	21 %	7 %	50 %	0 %	43 %
1000 nm	47 %	47 %	0 %	6 %	0 %	80 %	20 %	0 %
10-channels	A	B	C	D	A	B	C	D
20 nm	7 %	53 %	7 %	33 %	5 %	55 %	10 %	30 %
40 nm	0 %	39 %	0 %	61 %	5 %	90 %	0 %	5 %

probability of case D decreases. This observation indicates that the shorter the device, the larger the probability that CD is triggered very fast (case D). Note that this trend is also observed for multichannel pMOS devices, whereas the opposite trend is observed in nMOS. These results suggest that the device architecture (number of channels) and the substrate (p or n type) play a key role in the post-BD behaviour of the device. In the next sections, these dependencies will be analysed in detail.

4. Statistics of BD and current drop voltages

To gain more insight into the phenomenon, the statistical distributions of the BD and CD voltages (i.e., the voltages at which BD, V_{BD}, and CD, V_{CD}, occur) have been analysed, for different device lengths and widths (Figs. 4 and 5), in pMOS and nMOS transistors. Note that the V_{BD} distributions include case A and B events, whereas V_{CD} distributions gather cases B, C and D. Thus, case B is simultaneously considered in the V_{BD} and V_{CD} distributions, since BD and CD events are clearly

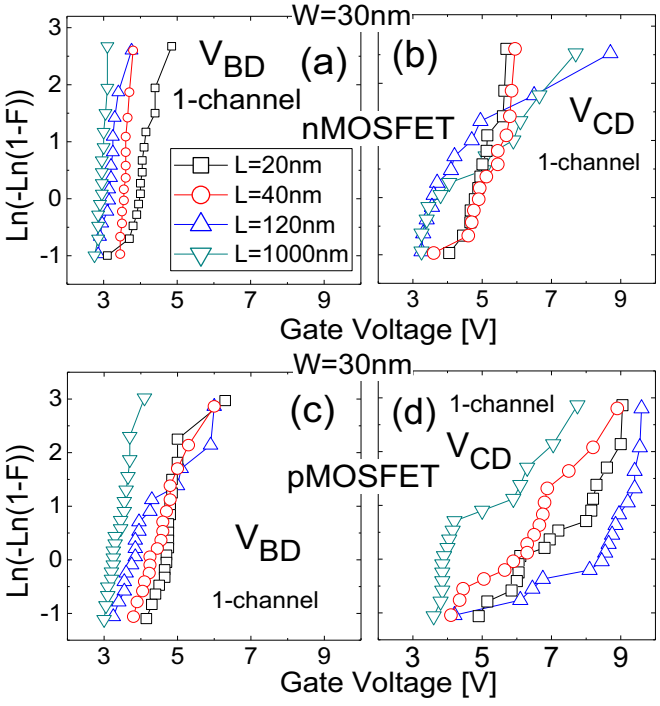

Fig. 4. Weibull distributions of V_{BD} (a and c), and V_{CD} (b and d), for nMOS and pMOS transistors, respectively, for unichannel architecture (W = 30 nm), and different lengths ranged from 20 nm to 1000 nm.

distinguished in this case. For unichannel devices (W = 30 nm), as observed in Fig. 4a and c for nMOS and pMOS, respectively, the BD voltages (V_{BD}) follow a Weibull distribution, clearly dependent on the device area (W = 30 nm and different L), as expected from the BD

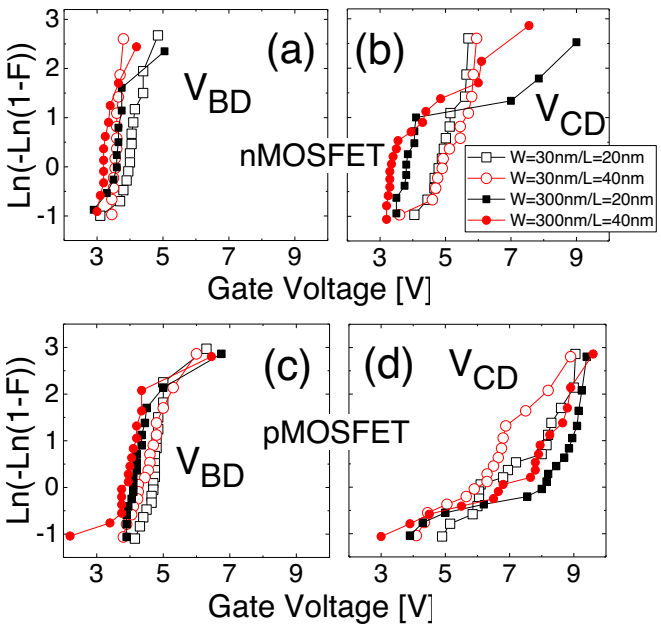

Fig. 5. Weibull distributions of V_{BD} (a and c), and V_{CD} (b and d), for nMOS and pMOS, respectively, for 10-channel architecture with 300 nm of width (Solid symbols) and two different lengths (20 nm and 40 nm). For easier comparison, data from unichannel devices in Fig. 4 (30 nm width) with the same length are also included (open symbols).

literature [27,28]. Note that V_{BD} for pMOS is larger than for nMOS. In the case of V_{CD} (Fig. 4b and d for nMOS and pMOS, respectively), the distributions are wider than V_{BD} and shifted towards higher voltages, and the area dependence is no longer observed. In some cases, bimodal distributions are obtained, particularly in pMOS devices. Similar trends are observed for the V_{BD} and V_{CD} distributions of the 10-channel devices (W_{eff} = 300 nm), as shown in Fig. 5. Several conclusions can be drawn from these results. (i) BD events in these FDSOI devices show no remarkable differences from those in bulk devices (i.e. Weibull distributions and area effect still hold). Then, in these devices, oxide wear out is responsible for BD, as widely accepted in the literature [5,9,22]. (ii) V_{BD} is larger for pMOS. (iii) CD events (if observed) take place after the BD event. (iv) CD events show larger variability than BD. (v) The observed bimodality suggests that two mechanisms control the post-BD device behaviour [29]. (vi) BD and CD take place at higher voltages for pMOS than for nMOS devices.

5. After-BD device performance

To analyse the impact of BD and CD on the device performance, the fresh (black lines) and post-BD (coloured lines) I_D-V_G and I_G-V_G characteristics of unichannel (top) and multichannel (bottom) devices have been analysed (see Fig. 6 right and left, respectively). In case A (i.e., CD not observed, red circles), for uni and multichannel devices, the large gate current is driven by the BD path (Fig. 6a and c) [23]. The channel current (Fig. 6b and d) is dominated by the large gate current. Interestingly, no gate voltage dependence is observed. In cases B, C and D (blue lines), for unichannel devices, CD drives the device into a non-conductive or low-conductive state. This occurs in both vertical (leakage current through the gate dielectric, Fig. 6a) and lateral directions (channel conduction, Fig. 6b), suggesting a fatal device failure. For multichannel devices, while the gate also shows a non-conductive state, the channel still remains conductive though without displaying gate voltage dependence. These results evidence that, after BD and CD, in the multichannel devices, there can be still some conduction through the channel, though dominated by the BD path. Therefore, though in this case BD effects do not appear to be so severe as in unichannel devices, the gate has lost the control of the drain current. Therefore, the device

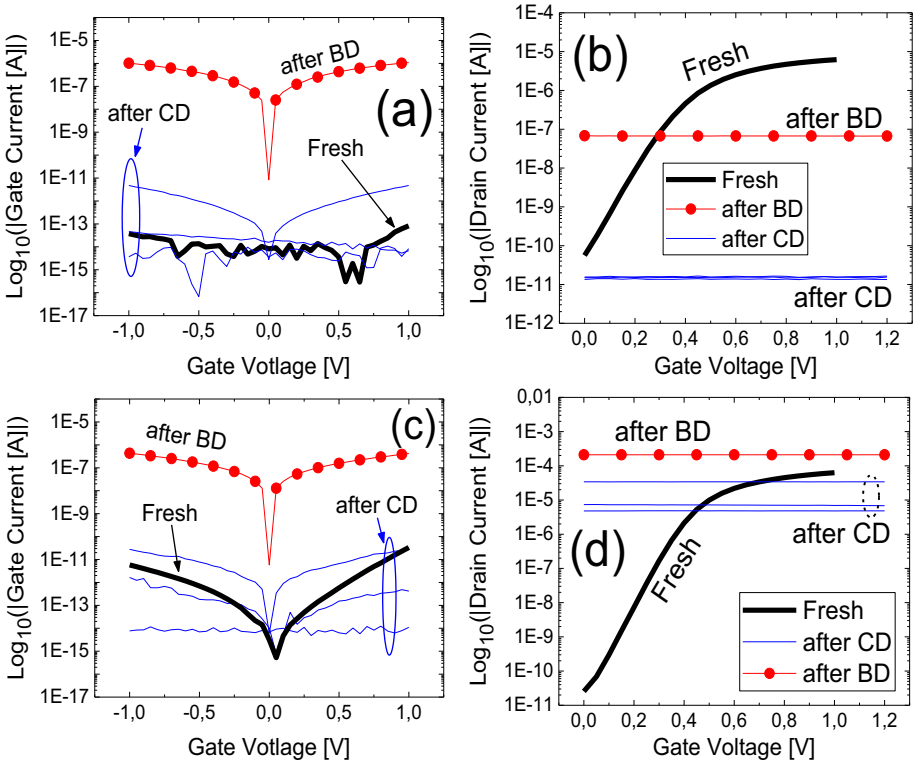

Fig. 6. Examples of typical fresh (black line), after a case A event (red circles), and after cases B, C and D (blue lines) I_G-V_G (left) and I_D-V_G (right) characteristics registered in uni channel (top) and multi-channel (bottom) nMOS devices with W = 30 nm/L = 20 nm and W = 300 nm/L = 20 nm, respectively. I_D was measured with V_D = 50 mV. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

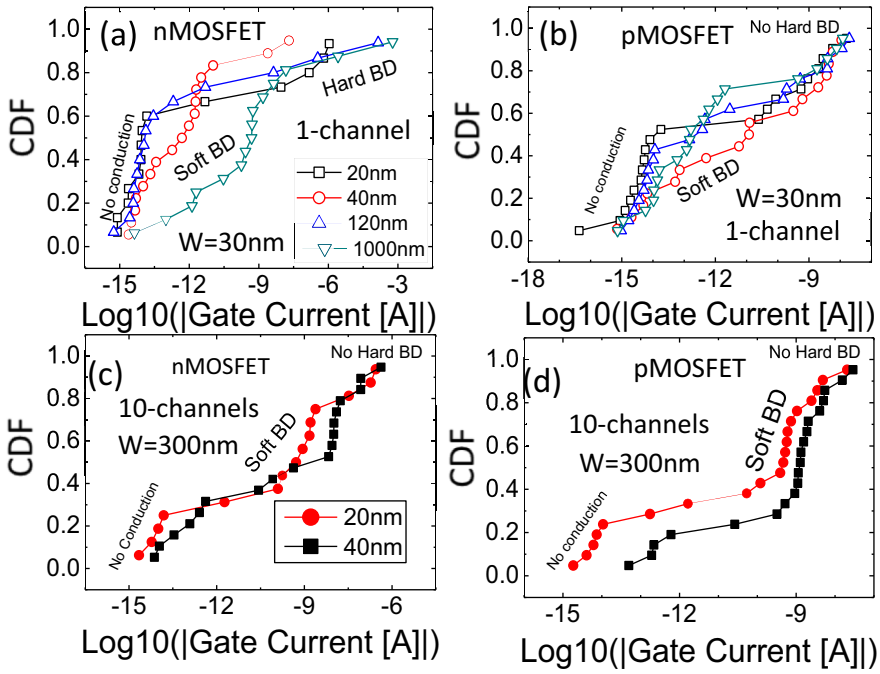

Fig. 7. Cumulative distribution functions (CDF) of post-stress I_G at $V_G = |1V|$, (a) 1-channel nMOS, (b) 1-channel pMOS, (c) 10-channel nMOS, and (d) 10-channel pMOS, with lengths ranging from 20 nm to 1000 nm.

cannot be operated any longer as a MOSFET [30].

A statistical study of the gate and drain currents measured from I-V curves like those in Fig. 6 has been carried out. Fig. 7 shows the Cumulative Distribution Functions (CDF) of I_G obtained from the I_G-V_G curves at $V_G = |1V|$ for the following cases: nMOS unichannel (Fig. 7a) and 10-channel (Fig. 7c) devices, and pMOS unichannel (Fig. 7b) and 10-channel (Fig. 7d) transistors. Note that these distributions contain information on the currents measured in all the devices, which may have suffered only a BD event (case A), or a BD followed by a CD event (cases B, C and D). Multimodal distributions are observed, which can be associated with different conductive modes: (i) the mode observed at very low currents ($<10^{-13}$ A) corresponds to CD events after which the device becomes non-conductive (i.e. currents close to the noise level), (ii) I_G values ranging from 10^{-12} to 10^{-6} A correspond to soft BD conduction (i.e. non-linear dependence of I_G on V_G), regardless BD and CD (cases B and C) or only CD (case D) are observed, and (iii) I_G values above $\sim 10^{-6}$ A correspond to hard BD (i.e. linear dependence of I_G on V_G) in those devices that only suffered an isolated BD event (case A). However, several differences have been observed, which depend on the substrate type (i.e. nMOS or pMOS) and device architecture (uni or multichannel). First, currents in pMOS transistors (unichannel and 10-channel devices) and multichannel nMOS devices range from noise-level to ~10 nA. However, for unichannel nMOS transistors currents increase up to ~100uA. Therefore, the Hard BD mode (case A) is rarely observed in the case of pMOS (Fig. 7b and d) and nMOS multichannel transistors (Fig. 7c). Second, for unichannel devices, the probability of having a non-conductive state is larger. Moreover, in these devices, the multimodality is blurred (specially for nMOS), with smoother changes between modes when compared to better-defined conduction modes in the multichannel devices. No remarkable differences with L have been observed for the range of channel lengths studied.

Therefore, these results, together with those in Table 1, suggest that the probability of occurrence of a BD/CD event and the post-BD/CD gate conduction depend on the device type and architecture. The probability of occurrence of case A event (i.e., only BD) is only significant in nMOS unichannel devices, and the channel length does not have relevant influence. As for the conduction after the CD event, no remarkable dependence on the channel length is observed when considering cases B, C and D together (see Table 1), although the probability of non-conductive state is lower in the multichannel devices (Fig. 7).

Regarding the channel conduction after BD and CD, Fig. 8 shows the I_D obtained from the I_D-V_G characteristic at $V_G = 0$ V (Fig. 8a and d), $V_G = |0.3|$V (Fig. 8b and e), and $V_G = |1|$V (Fig. 8c and f) in nMOS (left) and pMOS (right) transistors, respectively, for unichannel (open symbols) and multichannel (solid symbols) devices with different dimensions. Remarkably, Fig. 8 shows that, for all the studied devices, the channel conduction after BD/CD events is independent of the gate voltage (as already suggested by the curves in Fig. 6), corroborating that the gate can no longer control the current through the channel. However, depending on the current through the gate (i.e., after a CD, partial CD or BD) the values of the channel current depend on the device architecture. In the case of unichannel devices (open symbols in Fig. 8), in most of the devices, I_D is negligible (noise level, ~pA) for nMOS and pMOS, indicating that channel conduction has been completely lost and pointing out a severe failure of the device. Only some devices exhibit larger channel currents, that correspond to those cases where the BD path is driving the oxide conduction (case a). Conversely, larger I_D currents are measured in 10-channel devices. The spread of the I_D values is larger (~1 μA-1 mA) and independent of the channel length, suggesting that channel current is mainly linked to the current through the gate (which is local, and therefore area independent). Therefore, CD in multiple channel devices, as in unichannel ones, provokes the loss of the gate voltage control of the drain current (i.e., the current is independent of the gate voltage), but still some current flow is possible. Note however, that this case could be even more detrimental, from a power consumption point of view.

The results in Fig. 8 suggest that in these FDSOI NW devices, the BD of the gate oxide can be much more detrimental than in bulk planar devices. On the one hand, because, independently of the substrate type and the number of channels, the MOSFET functionality is completely lost (i.e., the gate voltage can no longer control the gate current). Moreover, in some cases, neither vertical nor horizontal conduction is possible anymore, which suggests a very severe device failure. On the other hand, in multichannel devices, although conduction is still possible, a large increase in power consumption has been observed, which is associated with a non-functional device. The differences

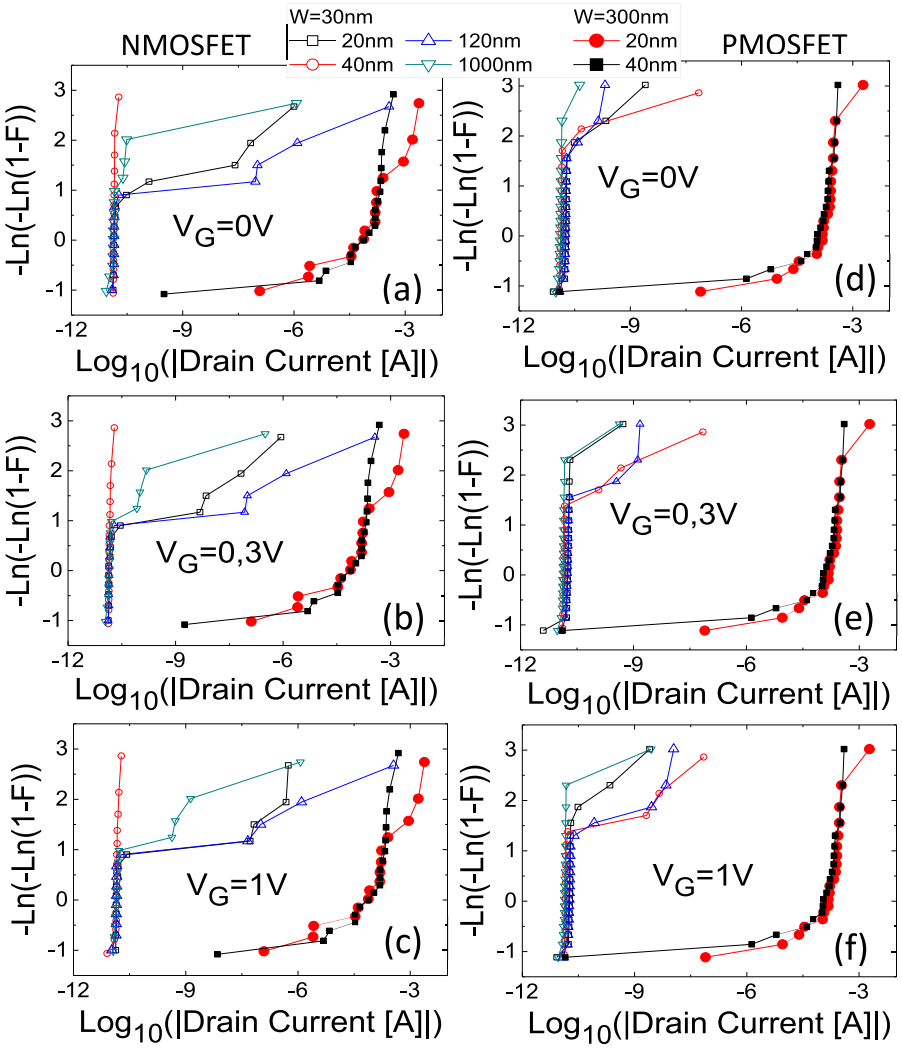

Fig. 8. CDFs of post-stress $|I_D|$ at $V_G = 0$ V (a and d), $V_G = 0.3$ V (b and e), and $V_G = 1$ V (d and f) in nMOS (left) and pMOS (right) transistors with W = 30 nm (unichannel) and different lengths ranging from 20 nm to 1000 nm (open symbols) and with $W_{eff} = 300$ nm (10-channel) and L = 20 and 40 nm (solid symbols).

observed in the post-BD and post-CD behaviours are strongly dependent on the substrate type and the number of channels. Though further work is needed to understand the physical origin of the observed phenomenology, it could be related to the device's capability of power dissipation after-BD. Recall that BD is an extremely local phenomenon and is stochastic in nature (i.e. V_{BD} and I_G are statistically distributed). The local power increase after the BD current runaway must be dissipated in the device substrate. However, in FDSOI technologies, the dissipation must occur in the thin substrate above the BOX, which has limited power dissipation capability [32]. Then, the initial local damage caused by the BD runaway may expand in the substrate beneath the BD spot, eventually 'disconnecting' that region of the channel under the location of the BD path, which would lead to CD observation. In this work, the term "disconnecting" is used to describe the situation where the localized BD event produces severe damage in the gate stack and/or in the underlying channel region, so that neither vertical current through the gate oxide nor lateral current along the channel can be sustained. In multi-channel devices, conduction could be still possible if only some fingers were affected by the BD event; in single-channel devices, BD could block any conduction path in the device, leading to the nearly insulating post-CD behaviour observed in our measurements. However, in some cases, predominantly in nMOS devices, 'softer' BD events may be triggered (that could be related to current limitation effects of the more resistive channel and/or smaller V_{BD}'s), resulting in a typical HBD event without CD. Note that, although before BD, longer channel devices show better performance from a power dissipation perspective (i.e., they conduct less drain current under the same bias conditions and have larger area), this does not mitigate the probability of CD occurrence since, after BD, the large and localized gate current is controlling the post-BD behaviour. In this situation, the CD occurrence will depend on the power dissipation capability at the BD spot region, which is confined in a very reduced area of the thin silicon film and the buried oxide. Therefore, the area of the device does not significantly influence the statistics of CD occurrence, consistent with the results shown in Table 1. In any case, after BD and after CD events, the conduction of the damaged channel will be no longer controlled by V_G, so that the device has lost its functionality. Reasonably, BD effects would depend on the device size. In our short 1-channel devices, BD would damage the whole gate area, fully destroying the device and leading to a non-conductive post-BD state (i.e., neither vertical nor lateral conduction is feasible, as suggested by the post-stress I_G-V_G and I_D-V_G curves). However, in those devices with more than one channel, only the channel where BD and CD has occurred (and eventually some other neighbour channels) would be disconnected, so that the lateral current could still be possible. This current could be controlled by the BD gate current and/or by changes in the electrostatics that may have been produced, indicating that the device functionality has also been lost.

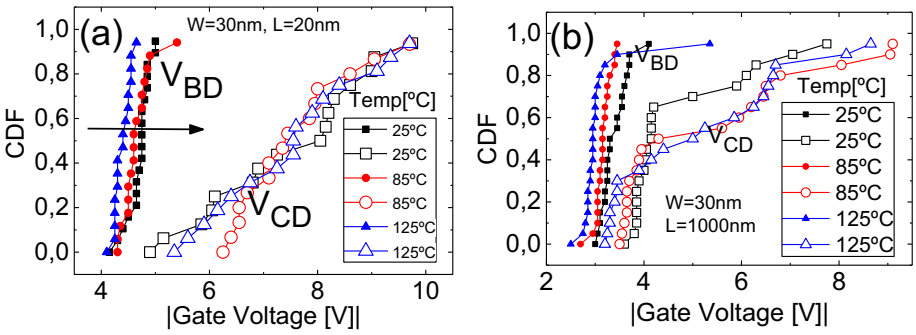

Fig. 9. CDFs of V_{BD} (solid symbols) and V_{CD} (open symbols) of pMOS devices with W = 30 nm (single channel) and 20 nm (a) and 1000 nm (b) lengths, at different temperatures.

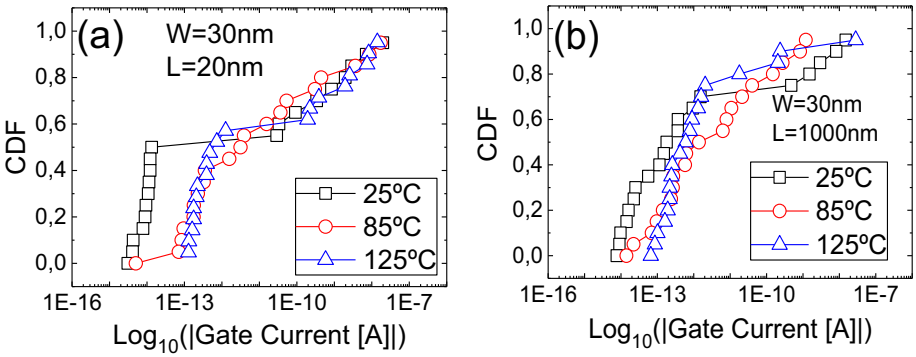

Fig. 10. CDFs of the I_G measured in second RVS test at different temperatures, 25 °C (black squares), 85 °C (red circles) and 125 °C (blue triangles), in pMOS devices with W = 30 nm and L = 20 nm (a) and L = 1000 nm (b). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

6. Temperature dependence analysis

Since BD and post-BD current in bulk devices are temperature dependent phenomenon [33] to gain more insights on the BD and post-CD phenomenology in these devices, the temperature dependences of the BD and CD voltages and of the gate currents have been analysed. Then, the experiments have been repeated at 85 °C and 125 °C on several pMOS transistors, for which BD appears to be more detrimental. Fig. 9 shows the V_{BD} and V_{CD} distributions obtained in unichannel (W = 30 nm) pMOS devices with L = 20 nm (Fig. 9a) and L = 1000 nm (Fig. 9b). The distributions reveal that, for both channel lengths, BD events are accelerated by temperature (solid symbols) [31], while for the CD no external temperature dependence is observed in the case of L = 20 nm. Recall that self-heating can be important in these devices [32], so that a dependence on the internal temperature cannot be ruled out). In large channel (1000 nm) pMOS, V_{CD} distributions exhibit large bimodality (open symbols in Fig. 9b), as already observed in Fig. 4d, indicating that two mechanisms may be driving the device failure after the CD. The CD mode observed at low gate voltages shows a clear temperature dependence, while the other one at higher voltages does not. The bimodal behaviour observed in the VCD distributions (Fig. 9b) suggests that two different failure mechanisms may coexist. Though further work is needed to determine their origin, the low-voltage CD mode, which shows a clear temperature dependence, could be tentatively attributed to thermally activated degradation processes of the gate oxide, such as further defect generation or structural modifications at the BD spot induced by the high power density. In contrast, the high-voltage CD mode, which appears to be temperature independent, could be more consistent with a more severe breakdown event, with irreversible structural damage.

The I_G obtained at V_G = |1V| from the I_G-V_G measured during a second RVS test has been also analysed. Fig. 10 shows the I_G distributions corresponding to the same devices as in Fig. 9. As observed, for all temperatures, the gate current after the BD and the CD are largely spread, ranging from the noise level (device destruction) to hundreds of nanoamperes. Some temperature dependence is observed when very low current values are measured (up to 0.1pA), probably dominated by thermal noise. However, above this level, when the BD-CD damage is driving the gate oxide conduction, current does not display any temperature dependence. These observations suggest that opposite to BD, which can be accelerated by increasing the operating temperature, the CD event appears to be temperature independent. Note, however, that dependence on the internal device temperature cannot be ruled out.

7. Conclusions

The BD phenomenology in high-K Ω-shaped NW FD-SOI transistors has been statistically analysed. Our results show that BD of the gate dielectric can be followed by a CD event. This event is observed as a large drop in the gate current, negatively impacting the drain conduction as well. Our results suggest that CD is especially damaging (from a structural point of view) in short unichannel devices, so that current conduction (neither vertical nor lateral) is not allowed anymore. In multi-channel architectures, some NW may not be affected by the BD, so that the device can still drive some current. However, the gate control has been lost, and the drain current is dominated by the gate current, so that the device not only is non-functional but also its power consumption has increased, especially in the case of nMOS devices. The results can be interpreted in terms of the power dissipation capability of these devices due to the confinement of the device channel, which is insufficient to withstand the large currents triggered by the BD event, ultimately resulting in a catastrophic failure of the device (probably related to a 'destruction' of the gate stack around the BD spot). Therefore, in these NW FDSOI devices, BD can be a more detrimental failure

mechanism than in bulk devices.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This work was supported by Grant PID2022-136949OB-C22 funded by MCIN/AEI/10.13039/501100011033/ FEDER, UE, and 2021-SGR-00199. EU ASCENT project is acknowledged for the samples.

Data availability

The authors do not have permission to share data.

References

[1] R. Degraeve, G. Groeseneken, R. Bellens, J.L. Ogier, M. Depas, P.J. Roussel, H. E. Maes, New insights in the relation between electron trap generation and the statistical properties of oxide breakdown, IEEE Trans. Electron Devices 45 (4) (Apr. 1998) 904–911, https://doi.org/10.1109/16.662800.

[2] B.P. Linder, S. Lombardo, J.H. Stathis, A. Vayshenker, D.J. Frank, Voltage dependence of hard breakdown growth and the reliability implication in thin dielectrics, IEEE Electron Device Lett. 23 (Nov 2002) 661–663, https://doi.org/10.1109/LED.2002.805010.

[3] A. Rodriguez, M.B. Gonzalez, F. Campabadal, J. Suñé, E. Miranda, Breakdown time statistics of successive failure events in constant voltage-stressed Al2O3/ HfO2 nanolaminates, Microelectron. Eng. 147 (Nov. 2015) 85–88, https://doi.org/10.1016/j.me e.201 5.04.048.

[4] A. Diab, X. Garros, M. Rafik, X. Federspiel, E. Vincent, G. Reimbold, Impact of gate impedance on dielectric breakdown evaluation for 28 nm FDSOI transistors, Microelectron. Eng. 178 (June 2017) 21–25, https://doi.org/10.1016/j.mee.2017.0 4.022.

[5] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, G. Ghibaudo, Review on high-k dielectrics reliability issues, IEEE Trans. Device Mater. Reliab. 5 (Mar. 2005) 5–19, https://doi.org/10.1109/TDMR.20 05.8 45236.

[6] M. Porti, M. Nafría, X. Aymerich, New insights on the post-BD conduction of MOS devices at the nanoscale, IEEE Electron Device Lett. 26 (Jan 2005) 109–111, https://doi.org/10.1109/LED.2004.841190.

[7] Y. Wang, S. Zheng, S. Zhang, J. Wang, G. Lu, G. Wen, Study on different failure mechanisms of MOSFET caused by different oxide defects in 14 nm FinFET IC, Microelectron. Eng. 299 (September 2025), https://doi.org/10.1016/j.mee.2025.112350.

[8] R. Rodriguez, J.H. Stathis, B.P. Linder, S. Kowalczyk, C.T. Chuang, R.V. Joshi, G. Northrop, K. Bernstein, A.J. Bhavnagarwala, S. Lombardo, The impact of gate-oxide breakdown on SRAM stability, IEEE Electron Device Lett. 23 (9) (Sep. 2002) 559–561, https://doi.org/10.1109/LED.2002.802600.

[9] B. Kaczer, R. Degraeve, Ph. Roussel, G. Groeseneken, Gate oxide breakdown in FET devices and circuits: from nanoscale physics to system-level reliability, Microelectron. Reliabil. 47 (Apr–May 2007) 559–566, https://doi.org/10.1016/j.microrel.2007.01.063.

[10] R. Fernandez, J. Martin-Martinez, R. Rodriguez, M. Nafria, X. Aymerich, Gate oxide wear-out and breakdown effects on the performance of analog and digital circuits, IEEE Trans. Electron Devices 55 (4) (May 2008) 997–1004, https://doi.org/10.1109/TED.2008.917334.

[11] M. Depas, T. Nigam, M. Heyns, Soft breakdown of ultra-thin gate oxide layers, IEEE Trans. Electron Devices 43 (9) (Sep 1996) 1499–1504, https://doi.org/10.1109/16.535341.

[12] K. Shubhakar, K.L. Pey, N. Raghavan, S.S. Kushvaha, M. Bosman, Z. Wang, S. J. O'Shea, Study of preferential localized degradation and breakdown of HfO_2/SiO_x dielectric stacks at grain boundary sites of polycrystalline HfO_2 dielectrics, Microelectron. Eng. 109 (September 2013) 364–369, https://doi.org/10.1016/j.mee.2013.03.021.

[13] A. Avella, W.H. Krautschneider, Impact of soft and hard breakdown on analog and digital circuits, IEEE Trans. Device Mater. Reliab. 4 (4) (Dec 2004) 676–680, https://doi.org/10.1109/TDMR.2004.836729.

[14] M. Nafría, J. Suñe, X. Aymerich, Exploratory observations of post-breakdown conduction in polycristaline-silicon and metal-gate thin-oxide metal-oxide-semiconductor capacitors, J. Appl. Phys. 73 (Jan 1993) 205–215.

[15] A. Crespo-Yepes, J. Martin-Martinez, R. Rodriguez, M. Nafria, X. Aymerich, Reversible dielectric breakdown in ultrathin Hf based high-k stacks under current-limited stresses, Microelectron. Reliab. 49 (9–11) (Sep-Nov 2009) 1024–1028.

[16] W.H. Liu, K.L. Pey, X. Li, M. Bosman, Observation of switching behaviours in post-breakdown conduction in NiSi-gated stacks, IEEE Int. Electron Devices Meet. (Mar 2010) 135–138, https://doi.org/10.1109/IEDM.2009.5424402.

[17] A. Crespo-Yepes, J. Martin-Martinez, A. Rothschild, R. Rodriguez, M. Nafria, X. Aymerich, Recovery of the MOSFET and circuit functionality after the dielectric breakdown of ultrathin high-k gate stacks, IEEE Electron Device Lett. 31 (6) (Apr 2010) 543–545, https://doi.org/10.1109/LED.2010.2045732.

[18] M. Silva, F. Cacho, V. Huard, D. Angot, X. Federspiel, M. Durand, M. Parra, A. Bravaix, L. Anghel, New insights about oxide breakdown occurrence at circuit level, in: IEEE International Reliability Physics Symposium, Jul 2014, pp. 2D 5.1–2D 5.6, https://doi.org/10.1109/IRPS.2014.6860597.

[19] L. Gerrer, G. Ghibaudo, M. Rafik, Unified compact model of Soft Breakdown oxide degradation and its impact on CMOS circuit's reliability, in: IEEE Transactions on Device and Materials Reliability 12(1), Dec 2011, pp. 171–176, https://doi.org/10.1109/TDMR.2011.21811.74.

[20] F. Cacho, A. Bravaix, T. Garba Seybou, H. Pitard, X. Federspiel, T. Kumar, F. Giner, A. Michard, D. Celeste, B. Miller, V. Dhanda, A. Varshney, V. Tripathi, J. Kumar, Device reliability to circuit qualification: insights and challenges, in: IEEE International Integrated Reliability Workshop, Mar. 2023, pp. 1–7, https://doi.org/10.1109/IIRW56459.2022.10077885.

[21] N. Singh, A. Agarwal, L.K. Bera, T.Y. Liow, R. Yang, S.C. Rustagi, C.H. Tung, R. Kumar, G.Q. Lo, N. Balasubramanian, D.L. Kwong, High-performance fully depleted silicon nanowire (diameter < 5nm) gate-all-around CMOS devices, IEEE Electron Device Lett. 27 (5) (May 2006) 383–386, https://doi.org/10.1109/LED.2006.873381.

[22] P.C. Feijoo, T. Kauerauf, M. Toledano-Luque, M. Togo, E. San Andres, G. Groeseneken, Time-dependent dielectric breakdown on subnanometer EOT nMOS FinFETs, IEEE Trans. Device Mater. Reliab. 12 (1) (2012) 166–170, https://doi.org/10.1109/TDMR.2011.2180387.

[23] A. Benoist, S. Denorme, X. Federspiel, B. Allard, P. Candelier, Extended TDDB power-law validation for high-voltage applications such as OTP memories in High-k CMOS 28nm FDSOI technology, in: IEEE International Reliability Physics Conference, Jun. 2015, pp. GD 3.1–GD 3.5, https://doi.org/10.1109/IRPS.2015.7112804.

[24] T. Garba-Seybou, X. Federspiel, F. Monsieur, M. Sicre, F. Cacho, J. Hai, A. Bravaix, Location of oxide breakdown events undere Off-state TDDB in 28nm N-MOSFETs dedicated to RF applications, in: 2023 IEEE International Reliability Physics Symposium, May 2023, https://doi.org/10.1109/IRPS48203.2023.10117725.

[25] M. Saliva, F. Cacho, C. Ndiaye, V. Huard, D. Angot, A. Bravaix, L. Anghel, Impact of gate oxide breakdown in logic gates from 28nm FDSOI CMOS technology, in: IEEE International Reliability Physics Symposium, Apr. 2015, pp. CA 4.1–CA 4.6, https://doi.org/10.1109/IRPS.2015.7112782.

[26] L.M. Almeida, P.G.D. Agopian, J.A. Martino, S. Barraud, M. Vinet, O. Faynot, Back gate bias influence on SOI Ω-gate nanowire down to 10nm width, in: IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), CEA-LETI, Jan 2017, https://doi.org/10.1109/S3S.2016.7804394.

[27] K.S. Yew, D.S. Ang, G. Bersuker, Bimodal Weibull distribution of metal/high-k gate stacks TDDB-insights by scanning tunneling microscopy, IEEE Electron Device Lett. 33 (2) (2011) 146–148, https://doi.org/10.1109/LED.2011.2174606.

[28] N. Raghavan, K.L. Pey, K. Shubhakar, X. Wu, W.H. Liu, M. Bosman, Role of grain boundary percolative defects and localized trap generation on the reliability statistics of high-k gate dielectric stacks, in: IEEE International Reliability Physics Symposium, Jul 2012, pp. 6A.1.1–6A.1.11, https://doi.org/10.1109/IRPS.2012.6241862.

[29] V. Iglesias, J. Martin-Martinez, M. Porti, R. Rodriguez, M. Nafria, X. Aymerich, T. Erlbacher, M. Rommel, K. Murakami, A. Bauer, L. Frey, G. Bersuker, Bimodal CAFM TDDB distributions in polycrystalline HfO2 gate stacks: the role of the interfacial layer and grain boundaries, Microelectron. Eng. 109 (2013) 129–132, https://doi.org/10.1016/j.mee.2013.03.022.

[30] R. Fernandez, R. Rodriguez, M. Nafria, X. Aymerich, MOSFET output characteristics after oxide breakdown, Microelectron. Eng. 84 (1) (Jan 2007) 31–36, https://doi.org/10.1109/SCED.2005.1504306.

[31] Y. Ernest, J. Suñé, On voltage acceleration mopdels of time to breakdown-PartII: experimental results and Votlage dependence of weibull slope in the FN regime, IEEE Trans. Electron Devices 56 (7) (June 2009) 1442–1450, https://doi.org/10.1109/TED.2009.2021725.

[32] Y. Zhao, Y. Qu, Impact of self-heating effect on transistor characterization and reliability issues in sub-10nm technology nodes, IEEE J. Electron Devices Soc. 7 (2019) 829–836, https://doi.org/10.1109/JEDS.2019.2911085.

[33] A. Crespo-Yepes, J. Martin-Martinez, A. Rothschild, R. Rodriguez, M. Nafria, X. Aymerich, Injected charge to recovery as a parameter to characterize the breakdown reversibility of ultrathin HfSiON gate dielectrics, IEEE Trans. Device Mater. Reliabil. 11 (1) (2010) 126–130, https://doi.org/10.1109/TDMR.2010.2098032.