Simulating the impact of Random Telegraph Noise on integrated circuits

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***Abstract*— This paper addresses the statistical simulation of integrated circuits affected by Random Telegraph Noise (RTN). For that, the statistical distributions of the parameters of a defect-centric model for RTN are experimentally determined from a purposely designed integrated circuit with CMOS transistor arrays. Then, these distribution functions are used in a statistical simulation methodology that, taking into account transistor sizes, biasing conditions and time, can assess the impact of RTN in the performance of an integrated circuit. Simulation results of a simple circuit are shown together with experimental measurements of a circuit with the same characteristics implemented in the same CMOS technology.**

Keywords—RTN, CMOS, Simulation, Transistor, Characterization

I. Introduction

Random Telegraph Noise (RTN) has become a subject of increasing concern in deeply-scaled CMOS technologies [1], due to its role as a source of device and circuit performance variability [2], [3]. At device level, RTN is observed as random and sudden discrete jumps of the drain current, which are caused by threshold voltage shifts associated to stochastic charge trapping/de-trapping events in/from device defects [4]. The impact of RTN has been reported for a wide variety of circuits, such as SRAMs or Ring Oscillators [3].

Fig. 1 shows an example of a current trace measured on a PMOS transistor with $|V_{gs}| = 1.0V$ and $|V_{ds}| = 0.1V$ clearly showing the RTN effect. The parameters that characterize the RTN phenomenon are the number of defects in the transistor, the amplitude of the current shifts (or, analogously, the amplitude of the threshold voltage shifts) associated to each of these defects, and their time constants, which may depend on the bias and temperature conditions. These time constants are the capture time (τ_c), i.e., the average time that an empty defect takes to capture a charge carrier, and the emission time (τ_e), i.e., the average time that an occupied defect takes to emit the charge carrier. All of these are stochastic parameters that can be modeled by distribution functions; hence, the impact of RTN on circuit performances must be studied statistically. To obtain the characteristic parameters of such distribution functions, an integrated circuit containing thousands of devices was designed on a 65-nm CMOS technology [5] and characterized with the experimental setup [6] shown in Fig. 2.

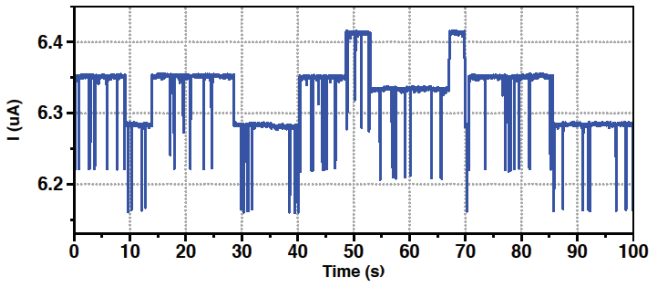

Fig. 1. Example of a current trace measured for a PMOS device displaying RTN-induced current shifts.

This paper presents the complete methodology for statistical simulation of RTN effects. To that end, Section II presents the distribution functions used. Section III presents the simulation methodology and Section IV shows the experimental results on a practical circuit.

II. RTN Characterization

The experimental setup allows to obtain thousands of current traces under different biasing and temperature conditions. From the current traces, the TiDeVa tool [7], [8], identifies the current levels by applying a maximum likelihood estimation (MLE)-based method. From the current levels, the number of defects, their associated current shifts, and the times at which captures and emissions take place can be identified [7].

These data must be modelled with a mathematical formulation that can be exploited for circuit simulation. The characteristic parameters of RTN are random variables, and, therefore, they are modeled with probability distribution functions.

A. Distribution of the number of defects

Frequently, the number of defects in a transistor has been modeled as a Poisson distribution [9], [10]. A discrete random

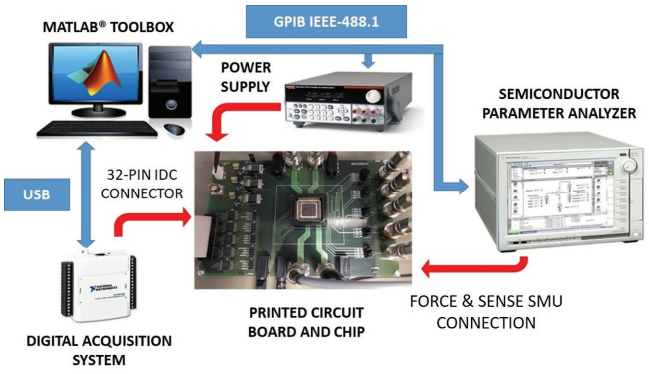

Fig. 2. Schematic representation of the experimental setup used in this work.

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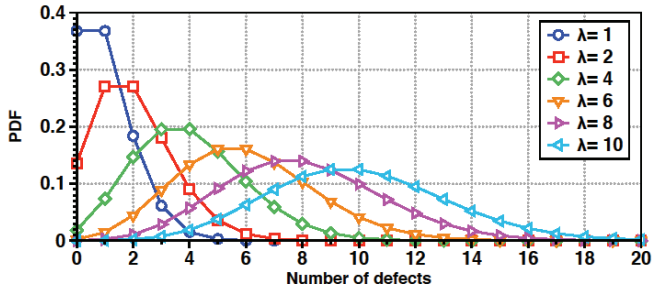

Fig. 3. Examples of Poisson distribution for several values of the mean number of defects λ.

variable X is said to have a Poisson distribution with parameter λ ($\lambda \in \mathbb{R},\ \lambda \geq 0$) if the probability mass function of X follows:

$$f(k;\lambda) = \Pr(X = k) = \frac{\lambda^k e^{-\lambda}}{k!} \tag{1}$$

For the RTN problem, this probability mass function represents the probability that, for transistors having an average number of defects λ, a given transistor contains exactly k defects. The equation can be easily adapted if instead of the average number of defects in the device, the average density of defects in the technology is considered:

$$\Pr(k \text{ defects in device}) = \frac{(\lambda A)^k e^{-\lambda A}}{k!} \tag{2}$$

where A is the device area and λ is now the average number of defects per unit area (defect density). Fig. 3 shows some examples of a Poisson distribution for several values of λ.

B. Distribution of the capture and emission times

The joint probability density function of the emission and capture times is formulated as a bivariate log-normal function [4],[11]:

$$P_{def}(\tau_e,\tau_c) = \frac{1}{\tau_e\tau_c 2\pi\sigma_{\tau_e}\sigma_{\tau_c}\sqrt{1-\rho^2}} \cdot e^{-\frac{1}{2\sqrt{1-\rho^2}}\left[\frac{(l\tau_e-\mu_{\tau_e})^2}{\sigma_{\tau_e}^2}+\frac{(l\tau_c-\mu_{\tau_c})^2}{\sigma_{\tau_c}^2}+\frac{2\rho(l\tau_e-\mu_{\tau_e})(l\tau_c-\mu_{\tau_c})}{\sigma_{\tau_e}\sigma_{\tau_c}}\right]} \tag{3}$$

where $l\tau_e = \log(\tau_e)$ and $l\tau_c = \log(\tau_c)$, μ_{τ_e} and μ_{τ_c} are the mean value of the emission and capture times, σ_{τ_e} and σ_{τ_c} are their standard deviations and ρ is the correlation coefficient. Distribution parameters are fitted to match the capture and emission events observed experimentally, resulting in the plot of Fig. 4.

It must be remarked that emission and capture times in (3) are in fact mean values of random variables corresponding to the real time at which particular emission or capture events occur. The emission and capture events are commonly modeled by a Markov process, yielding the probability that a defect with emission/capture time τ is emitted/captured at time instant t as:

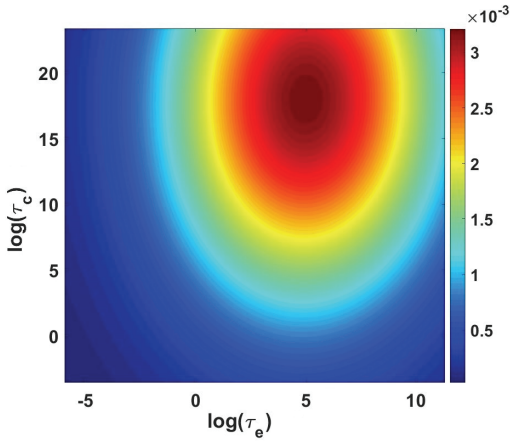

Fig. 4. Bivariate log-normal distribution of capture and emission times.

$$P(t) = \frac{1}{\tau} e^{-t/\tau} \tag{4}$$

C. Distribution of the threshold voltage and current shifts

The current shifts are extracted from the RTN current traces. Fig. 5 shows the histogram of the current shifts for 400 PMOS devices with $W/L = 80\text{nm}/60\text{nm}$ for $|V_{gs}| = 1.0\text{V}$ and $|V_{ds}| = 0.1\text{V}$. It can be concluded that a two-lognormal seems a good approximation for the current shifts δI:

$$f(\delta I) = \frac{R}{\delta I\sqrt{2\pi}\sigma_l} e^{-\frac{(\log(\delta I)-\mu_l)^2}{\sigma_l^2}} + \frac{(1-R)}{\delta I\sqrt{2\pi}\sigma_u} e^{-\frac{(\log(\delta I)-\mu_u)^2}{\sigma_u^2}} \tag{5}$$

where μ_l, μ_u, σ_l and σ_u, represent the mean and standard deviation of the lower and upper lognormal distribution and R represents the relative amplitude of both distributions.

Fitting the two-lognormal distribution in (5) to the experimental results in Fig. 5 yields the associated distribution function, displayed in red. Equivalently, a similar fitting process can be performed for the threshold voltage shift distribution.

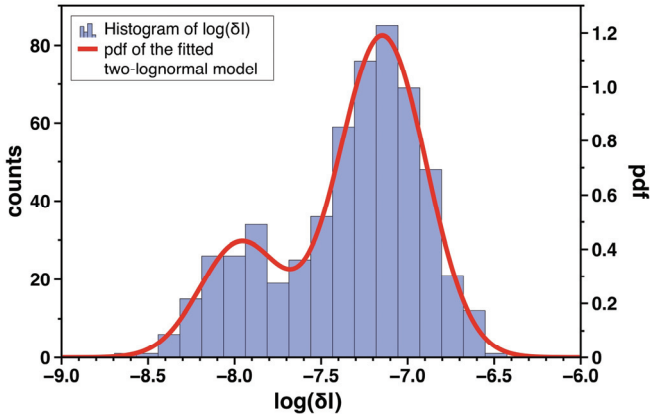

Fig. 5. Histogram of the experimentally extracted amplitudes for the RTN-induced current shifts (in blue), together with their associated pdf (in red).

III. Simulation Methodology

Once the probability density functions that govern RTN defects are established, a methodology to simulate circuits can be developed. Charge capture and emission in/from defects induce changes in the threshold voltages of the transistors and, hence, shifts of their drain current along time. As circuit simulators can obtain the drain current from a given threshold voltage (and operating conditions) modeling the shifts of the latter ones will enable obtaining the changes of the former ones.

Basically there are two possible approaches to incorporate this threshold voltage variation into circuit simulation [12]. The first one is to incorporate such variations into the transistor model, and the second one is to modify the circuit netlist to add a controlled voltage source to each transistor gate to model the threshold voltage shift, as illustrated in Fig. 6. Both approaches have benefits and downsides but the RTN mathematical framework shown before can be used with either approach. In the examples shown below, however, the circuit netlist modification approach has been used.

Being RTN a stochastic effect, circuit simulations should be also statistical (e.g., Monte-Carlo simulations). For that, hundreds or thousands of instances like that in Fig. 6(b) must be generated. The generation of instances in the form of a transient voltage along a certain simulation time T_{sim} proceeds through the following steps for each device:

Step 1: Generate the number of defects N_{def} for this device according to Poisson distribution. A simple algorithm to generate samples of this distribution can be found in [13]. If $N_{def} = 0$, the process is completed for this device.

Step 2: Generate emission τ_e and capture time τ_c of each defect according to the bivariate lognormal distribution in (3).

Step 3: Generate a sample of the associated threshold voltage shift ΔV_{th} for that defect. The governing probability density function, analogous to that for current shifts in eq. (5), can be efficiently sampled by: (1) deciding if the first or the second term in (5) becomes active by comparing the relative amplitude R with a sample of the commonly available uniform distribution; and (2) generating a sample of the selected log-normal distribution by applying the Box-Muller method using also two samples of uniform distributions [14].

Step 4: Generate the initial state ($t = 0$) of each defect according to the occupation probability: $P_{occ} = \frac{\tau_e}{\tau_e + \tau_c}$

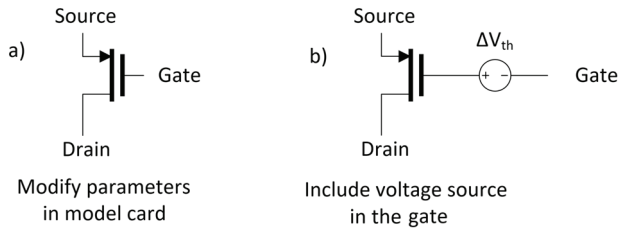

Fig. 6. Modeling RTN for circuit simulation: (a) modifying the parameters of the model card; (b) including a voltage source at the transistor gate.

Step 5: If the defect is occupied (empty), generate a sample of the time instant t_{ec} in which the charge will be emitted/captured. The probability, as given in (4), uses the time in the decimal scale. As the defects have been sampled from a bivariate log-normal distribution, it is necessary to transform (4) to logarithmic scale:

$$P(t) = \frac{t}{\tau} e^{-t/\tau} \tag{6}$$

The probability density function in (6) can be efficiently sampled by generating its cumulative density function and selecting a sample from a uniform distribution.

Step 6: Increase t by t_{ec}. Increase (decrease) threshold voltage shift at time t by ΔV_{th} if the defect has been captured (emitted).

Step 7: If $t < T_{sim}$ go to Step 5.

Step 8: Increase defect counter n. If $n \leq N_{def}$ go to Step 2.

Step 9: Sort the times t_{ec} corresponding to emission and capture events of all defects, and calculate the time evolution of their combined threshold voltage shift.

IV. Simulation and Experimental Results

The methodology in Section III was applied to the generation of hundreds of traces of threshold voltage shifts vs. time. For illustration's sake, four of these traces are shown in Fig. 7. By comparing these traces with the current trace in Fig. 1, it can be noticed that they show the same kind of random behavior, but Fig. 1 is a noisy one. This is because: (a) the voltage source in Fig. 6(b) must not contain noise as the noise is already included in the transistor model, and (b) the experimental trace in Fig. 1 contains noise intrinsic to the measurement setup that must not be included in a circuit simulation. The generated traces were used to simulate the impact of RTN on a basic integrated circuit: the simple current mirror in the inset of Fig. 8. An example of such a simulated output current for a constant input current is shown in Fig. 8(a), together with the associated copy factor in (b).

To experimentally validate the simulation methodology, the current mirror was integrated in the same 65-nm CMOS technology [15]. When biased in the same conditions, a typical behavior of the output current for a constant input current and the corresponding copy factor of the current mirror from one of the samples is shown in Fig. 9. It can be observed that the RTN directly impacts the copy factor of the current mirror, as expected from the simulation results displayed in Fig. 8.

V. Conclusions

In this paper, a complete methodology to simulate the impact of RTN on circuits has been presented. Since the parameters that characterize RTN are stochastic, a statistical

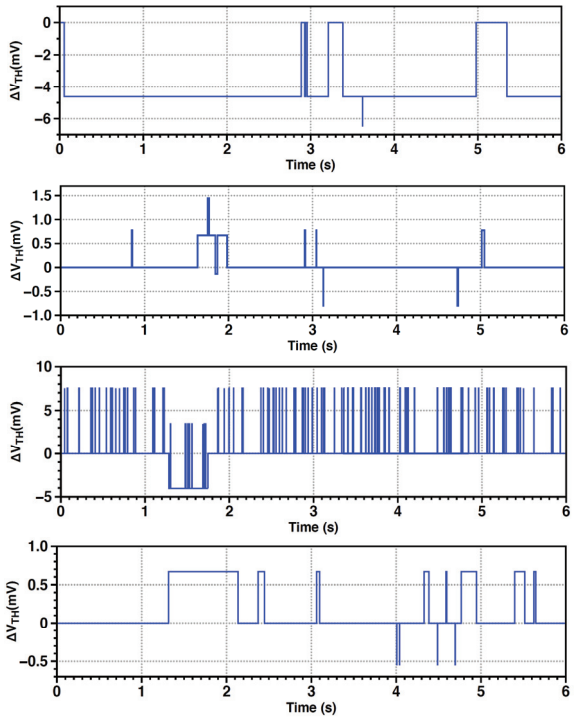

Fig. 7. Examples of ΔV_{th} traces generated for four different devices by using the simulation methodology presented in this work.

characterization of the phenomenon has been performed to extract the corresponding parameter distributions. Then, by sampling these distributions, the statistical simulation of integrated circuits affected by RTN can be performed. To do this, the effect of RTN on the devices V_{th} is included as a variation in the gate voltage of the device, which is incorporated through a voltage source on the transistor gate. Finally, this simulation methodology has been experimentally validated.

VI. References

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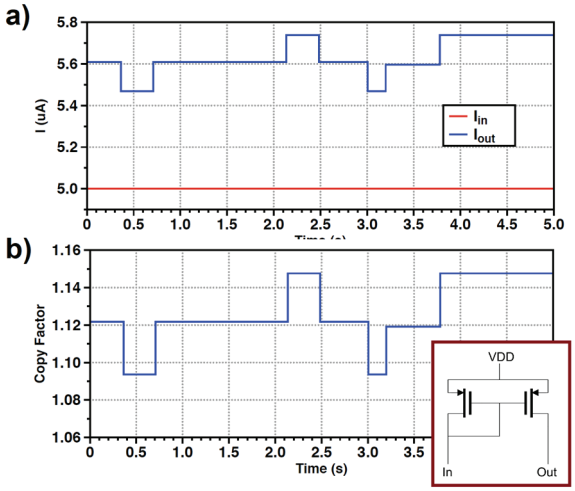

Fig. 8. a) Simulated I_{out} for a constant I_{in} displaying the impact of RTN, and b) the corresponding copy factor, for the current mirror in the inset.

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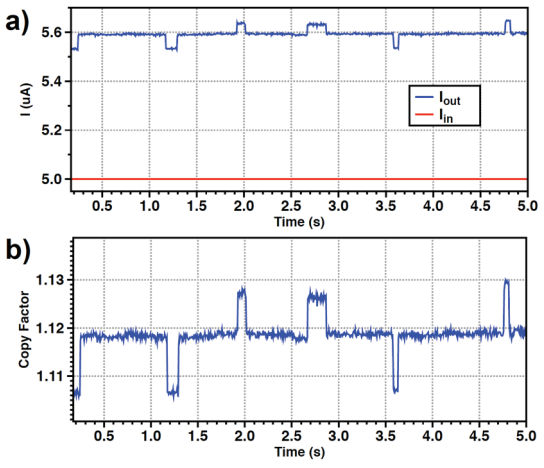

Fig. 9. a) Measured I_{out} for a constant I_{in} displaying the impact of RTN on the current mirror in the inset of Fig. 8 fabricated in the same 65nm CMOS technology [15], and b) the corresponding copy factor.