Stochastic resonance effect in binary STDP performed by RRAM devices

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***Abstract*—The beneficial role of noise in the binary spike time dependent plasticity (STDP) learning rule, when implemented with memristors, is experimentally analyzed. The two memristor conductance states, which emulate the neuron synapse in neuromorphic architectures, can be better distinguished if a gaussian noise is added to the bias. The addition of noise allows to reach memristor conductances which are proportional to the overlap between pre- and post-synaptic pulses.**

Keywords—Stochastic resonance, RRAM, memristor, resistive switching, STDP, neuromorphic systems.

I. INTRODUCTION

Memristors-based neuromorphic computing has acquired an increasing importance in the last years, being a potential candidate to implement efficient and low-power computing architectures [1]. In neural networks, which try to emulate the neurobiological behavior, memristor-based spike time dependent plasticity (STDP) learning approach is commonly accepted in the scientific community as a descriptor of the biological synapse [2]. STDP is characterized by the time difference between pre- and post-synaptic impulses [3], that determine the direction and magnitude (weight) of the change in synaptic plasticity [4]. In the binary STDP, only '1' or '0' values are valid for each synaptic weight [5]. Thus, binary STDP implemented with memristors involves switching the memristors resistance between two possible resistive states, i.e., HRS (High Resistive State) and LRS (Low Resistive State) (Figure1).

Although no noise or spike jitter are assumed in Artificial Neural Networks (ANN), in contrast, a significant amount of noise in biological systems is observed. There are controversial communications that discuss the role of that noise. In one side, it is considered that noise in biological systems is an undesired signal, caused by fluctuation in ions exchange mainly in synaptic units, that does not affect the network thanks to the fault tolerant capability of ANNs. However, other works postulate that, although noise is not associated with spiking codes, it affects the efficiency of signal firing when internal stimuli are under the voltage threshold required to start an action. Noise modules in some way the activation potential (threshold) of the neurons, beneficing the response of non-linear circuits, as mentioned by Anderson in [6], where he suggests that noise produced in the visual cortex facilitates the signal perception. In [7] Longtin confers to noisy neurons more sensitivity efficacy, based on the effect of Stochastic Resonance (SR), which is a phenomenon associated to no linear systems where noise has a beneficial role in the performance of the system.

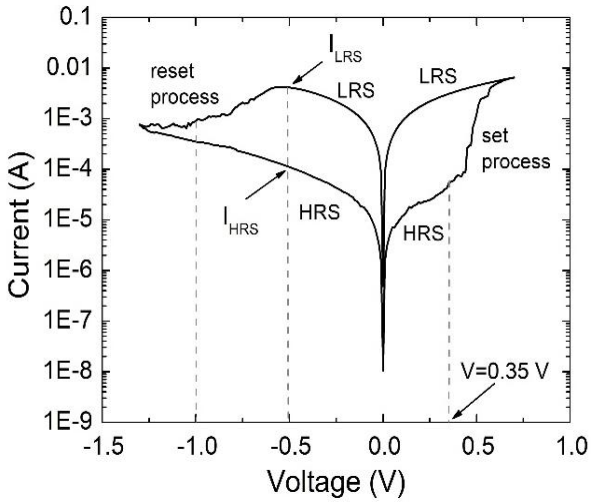

Figure 1: Current-voltage characteristic of the memristors used in this work.

Previous works have analyzed the constructive effect of noise in memristors [8-12]. In [13], the addition to the bias of gaussian noise increases the resistance difference between the memristor LRS and HRS and produces a lower dispersion of set and reset voltages and currents.

The aim of this work is to observe experimentally binary STDP induced by an external noise. The addition of noise is needed to initiate/achieve memristor state's switching, improving the STDP learning mechanism.

Figure 2: Schematic of the memristors used in this work

II. Devices and Measurement Procedure

The devices used in this work are HfO_2 based memristors with a metal-insulator-metal (MIM) structure: TiN-Ti-HfO_2-W-Ti in a vertical configuration, as presented in Figure 2. The 10nm-thick HfO_2 layer with a 5x5 μm^2 active area was deposited by atomic layer deposition (ALD) at 225°C using TDMAH and H_2O as precursors, and N_2 as carrier and purge gas. The bottom electrode consists in a 50 nm-thick W layer on top of a 20 nm-thick Ti layer and the top electrode is a 200 nm-thick TiN layer on top of a 10 nm-thick Ti layer acting as oxygen receiver material. The Al layer (bottom face of the wafer) acts as a contact for the bottom electrode. Find further information regarding the fabrication process in [14].

The electrical measurements were performed using the Semiconductor Parameter Analyzer (SPA) Agilent 4156C. The equipment was controlled via GPIB bus, and the measurement sequence programmed with Matlab software. Firstly, fresh (i.e. as-grown) memristors were subjected to a 1mA current-limited forming process that takes place at voltages ≅ 4V.

Figure 1 presents an example of the current-voltage (*I-V*) characteristic of the memristors used in this work, after forming. The applied voltage was swept from 0V to 0.7V, from 0.7V to -1.3V and from -1.3V to 0V and the current was registered during the application of voltage. The current was limited during the set process to 25mA to avoid the irreversible breakdown of the device.

The memristors used in this work present a bipolar behavior. The set process (the change from HRS to LRS) is produced for positive voltages and the reset process (the change from LRS to HRS) takes place at negative voltages (Figure 1). The variation in the memristor conductivity is related to the formation/destruction of a conductive filament through the dielectric, where oxygen-related species are responsible of this conductive variation [15].

To observe binary STDP, set and reset pulses have been applied to the memristor to achieve LRS and HRS resistance states, respectively. Actually, both set and reset pulses consist in the difference between a pulse applied to the top electrode (pre-synaptic pulse, V_{pre}) and a pulse applied to the bottom electrode (post-synaptic pulse, V_{post}) resulting in a memristor voltage drop of $V_{tot} = V_{pre} - V_{post}$ as shown in Figure 3.a. The pre- and post-synaptic pulses have a pulse width of 150ms. After each set and reset pulse, the memristor conductive state was registered, applying a reading voltage $V_{read} = -0.5$V during 150 ms to the top memristor terminal (Figure 3.b) with the bottom terminal grounded. This value of the reading voltage was selected as an optimum voltage to read the device state. The complete sequence is shown in Figure 3b. The set and reset pulses are configured differently. For the reset pulse, the difference between the pre- $(-0.5V)$ and post-synaptic $(0.5V)$ pulses results always in a 150ms pulse of $V_{reset} = V_{tot} = -1V$, to ensure the change to the HRS from the LRS (see Figure 1).

As our aim is to enhance binary STDP by adding an external noise to the set pulse, the pre- and post- synaptic pulse amplitudes are selected so as to ensure that the memristor does not change from HRS to LRS when no noise is applied. To do this, a set voltage, $V_{tot}=V_{set}$, lower than the one needed to trigger the set process is applied. In this case, we selected a maximum voltage of $V_{tot}=V_{set}=0.35$V (see Figure 1).

The generation of the set pulse (V_{set}) has some complexity since the post-synaptic pulse is shifted in time to produce different overlap situations between the pre- and the post-synaptic pulses, leading to different amplitudes and durations of V_{set}. Figure 3.c shows the initial situation of the pre- and post-synaptic pulses (without delay) and how the post-synaptic pulse is delayed (dashed lines) progressively. The measurement sequence of Figure 3.b is repeated 20 times for each of the considered post-synaptic pulse delays, allowing in this way a statistical analysis. That is, when the measurement sequence is started, the pre- and post-synaptic pulses have no overlap and set/reset currents were measured 20 times. Next, the post-synaptic pulse is delayed 15ms and the set and reset currents are measured 20 times again. In each of the subsequent shifts, the post-synaptic pulse is delayed $\Delta t = n*15$ms (with n=21 in the experiment described here). With this procedure, starting from the case of no overlap (for n=0), see Figure 4.a, the increment of n produces the progressive increase of the overlap between pre- and post-synaptic pulses until the maximum overlap is reached (for n=11, Figure 4.c) and then, as n continues increasing the overlap decreases, from the maximum value until the no

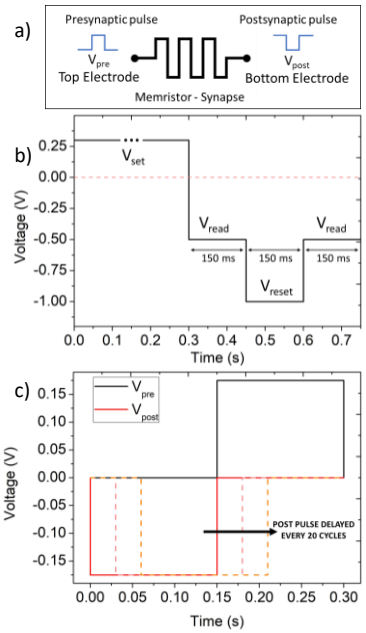

Figure 3: a) Pre- and post-synaptic pulses were applied to the top and bottom electrodes of the memristor, respectively b) schematics of the voltage waveform (cycle) applied to measure the set and reset currents (20 times) for a given Vset. The amplitude and duration of Vset has been changed by delaying the post-synaptic pulse, as shown in c). Initial configuration of the pre- and post-synaptic pulses, without overlapping. Dashed lines are two examples of delayed post-synaptic pulses.

overlap case again (for n=21). The dash blue line in Figure 5.c represents the overlap between the pre- and post-synaptic pulses as a function of Δt.

Due to the shift of the post-synaptic pulse, the duration of the set pulse at maximum voltage (0,35V) ranges from 0 up to 150ms and back to 0ms, in steps of 15ms. To better visualize this process, Figure 4 shows three different situations: the first one without overlapping between the pre and post-synaptic pulses (Figure 4.a), resulting in $V_{set} = V_{tot} = 0.175V$ and 300ms pulse duration; the second one, with a medium overlap, where a 3-level voltage pulse is obtained (Figure 4.b). In the represented example, the duration at maximum $V_{set} = V_{tot} = 0.35V$ was approx. 60ms; and the third one, with full overlapping, where $V_{set} = V_{tot} = 0.35V$ pulse with 150ms duration is applied to the memristor (Figure 4.c). This measurement procedure was implemented with and without noise addition, which was only included in the pre-synaptic pulse. Comparative measurements were performed in different devices (one device for measurements without noise and another one for the measurements with noise). The added noise was Gaussian with a standard deviation of $\sigma_{noise} = 150mV$. The resistance ratio is defined as $R_{Ratio} = (\frac{I_{Set}}{I_{Reset}})$ where I_{Set} and I_{Reset} are the currents at the reading voltage after the set and reset pulse respectively.

III. Results

Figures 5.a and 5.b show the currents measured (20 times), during all the iterations, as a function of the time shift between the pre- and post-synaptic pulses, for measurements without and with noise respectively. Red open dots correspond to currents after a set pulse and black open dots after a reset pulse. Both figures also show the mean set (red line) and mean reset (black line) currents. Comparing both figures, noise addition becomes essential for the identification of resistive states: when noise is not added, there is not state separation (Fig. 5.a), whereas, in the presence of noise (Fig. 5.b), an increase in the mean current after the set pulses is observed, which is proportional to the

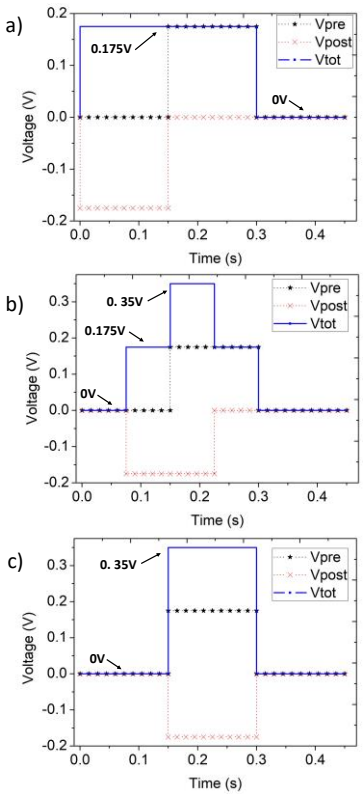

Figure 4: Total set voltage (V_{tot}) and pre- and post-synaptic pulses for 3 situations: a) no overlap, b) medium overlap, and c) full overlap.

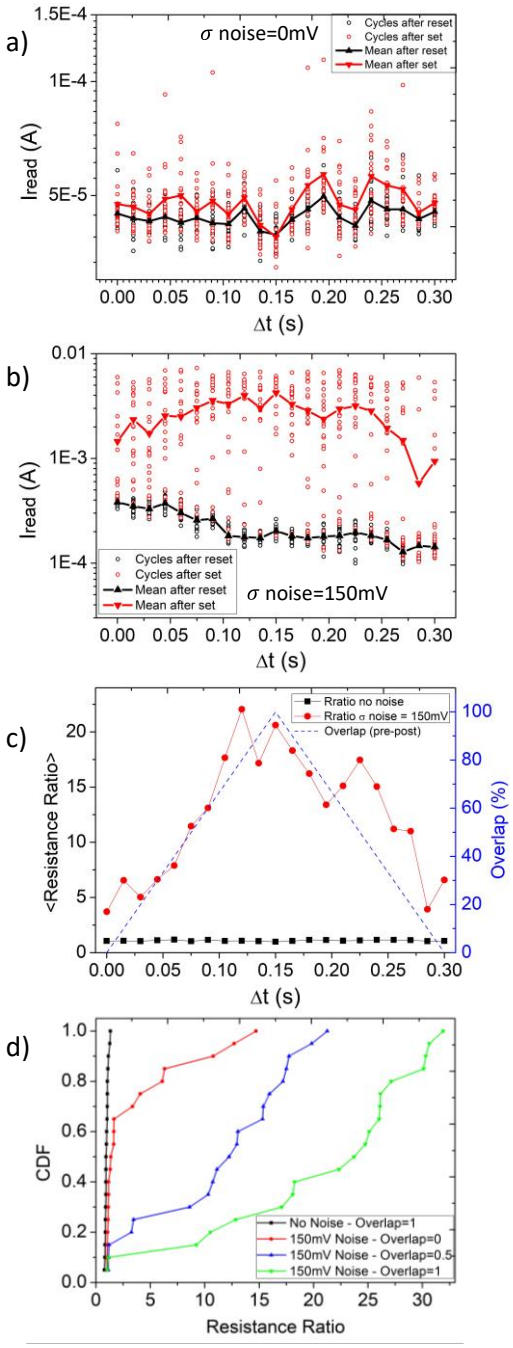

Figure 5: Current measured during the 20 cycles for each Δt shift and mean current evaluated after a set pulse (red) and after a reset pulse (blue) a) for the case w/o noise and b) adding a $\sigma = 150mV$ Gaussian noise. c) Mean resistance ratio versus the post-synaptic pulse delay for the experiments without noise (black) and with noise (red). d) CDF plots comparing the cases of maximum overlap without noise (black) and 3 different cases with additive noise: without overlap (red), medium overlap (blue) and full overlap (green).

overlap between the pre- and post-synaptic pulses (see maximum overlap at $\Delta t = 150ms$). For a better comparison, in Figure 5.c the mean resistance ratio parameter is shown as a function of Δt for the experiment without (black) and with (red) noise. Figure 5.c clarifies and corroborates the observations in Figures 5.a and 5.b: the proportionality between the pre- and post- synaptic pulses overlap (blue dash line in Figure 5) and resistance ratio. Lastly, the influence of the additive noise and the increase of the resistance ratio with Δt can be better seen in Figure 5.d. There, the cumulative density function (CDF) of the resistance ratio is represented for the maximum overlap situation without including noise (black line) and 3 different cases with added noise: without overlap (red line), medium overlap (blue line) and full overlap (green line). The figure shows that for the situation of no noise addition, as expected, the device is not able to switch to the LRS (black curve), with resistance ratio around 1. However, the simple addition of noise leads to an improvement of the resistance ratio. Moreover, by increasing the overlap between the pre- and post-synaptic pulses, the shift of the curves towards the right is larger, indicating a dependence of the R_{Ratio} improvement with this overlap.

IV. Conclusions

In this work, the beneficial role of additive noise in binary STDP implemented with HfO_2 based memristors is presented. This is a first experimental approach for the evaluation of stochastic resonance impact in memristors-based neuromorphic systems. The stochastic resonance phenomenon is studied in a situation where the memristor HRS and LRS states cannot be initially identified. However, our results demonstrate that the addition of a noise to the set pulse allows the switching between the two resistance states. The beneficial effect of noise has been evaluated through the dependence of the resistance ratio on the duration of the maximum value of set pulse (as determined by the pre- and post-synaptic pulses delay). The results show that the resistance ratio increases with the duration of the maximum value of the set pulse. These results are encouraging and open the path for further studies on the exploitation of the SR phenomemon in neuromorphic systems.

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