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Challenges and solutions to the defect-centric modeling and circuit simulation of time-dependent variability

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(Invited paper)

***Abstract*— Time-Dependent Variability (TDV) phenomena represent a serious concern for device and circuit reliability. To address the TDV impact at circuit level, Reliability-Aware Design (RAD) tools can be used by circuit designers to achieve more reliable circuits. However, this is not a straightforward task, since the development of RAD tools comprises several steps such as the characterization, modeling and simulation of TDV phenomena. Furthermore, in deeply-scaled CMOS technologies, TDV reveals a stochastic nature that can complicate those steps. In this invited paper, we review some of the main challenges that appear in each step of the flow towards the development of RAD tools, providing our solutions to them.**

***Index Terms*— Bias Temperature Instability (BTI), Random Telegraph Noise (RTN), Hot Carrier Injection (HCI), variability, aging, degradation, characterization, CMOS, reliability, array, Reliability-Aware Design (RAD).**

I. Introduction

Time-Dependent Variability (TDV) is an important concern for analog and digital circuit designers because of its growing impact on circuit reliability [1-5]. TDV manifests itself as shifts of the transistor parameters (e.g., threshold voltage) that, together with Time-Zero Variability (TZV), result in variations in the circuit performances. TDV comprises both transient phenomena, such as Random Telegraph Noise (RTN) [6-9], and aging phenomena, such as Bias Temperature Instability (BTI) [10-13] or Hot-Carrier Injection (HCI) [14-17], which cause the gradual degradation of circuits performance and may lead to their eventual failure.

The aforementioned TDV phenomena have been associated with the trapping/detrapping of charge carriers in/from defects present in the oxide or the silicon-oxide interface of MOSFETs [18,19]. The number of such defects per device, their time constants (i.e., the average time a defect takes to capture or emit a charge carrier) and the associated transistor-parameter shifts associated with these defects are stochastic. In older technology nodes, in the μm- or hundreds-of-nm range, each device contains a large number of defects. Therefore, the stochasticity of the defect parameters averages out, and TDV can be modeled in a deterministic way (i.e., two identical devices under the same operating conditions will present the same level of degradation). However, TDV in deeply-scaled MOSFETs has been linked to only a handful of defects in each device [11,18,19]. This introduces a stochastic component to the nature of TDV phenomena in these technology nodes, as two identical devices under the same operation conditions can present different levels of degradation. To deal with this stochasticity, defect-centric models have been presented in the literature [20-22]. Such models aim to predict the impact of TDV phenomena through the description of the trapping/detrapping behavior of defects. These models are necessary, but not sufficient, to address the impact of TDV on circuit reliability.

To mitigate the negative impact of TDV phenomena on circuits, they must be accounted for during the design process through a Reliability-Aware Design (RAD) approach. The road towards RAD comprises different steps, depicted in Fig. 1, such as the characterization of TDV, its modeling and its simulation. The stochastic nature of TDV in deeply-scaled technologies arises some challenges in each of these steps. For example, the characterization of TDV phenomena must be performed massively to retrieve statistically-significant information about the distributions of the defect parameters (number of defects, time constants and associated shifts).

In this invited paper, we review the challenges that are present in each step of the RAD flow and present the solutions

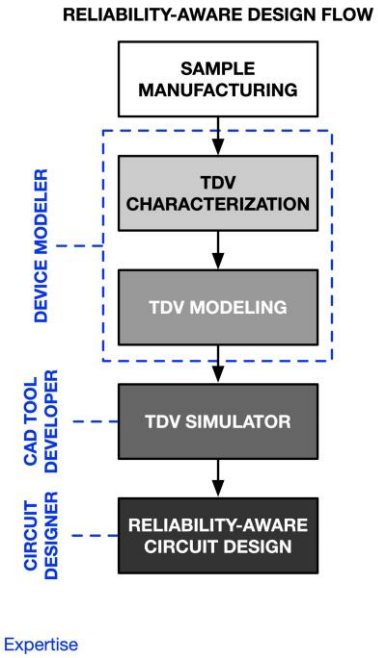

Fig. 1. Block diagram for the development of RAD solutions, indicating the different areas of expertise involved.

that we have given to them in our work. In Section II, we briefly describe the different TDV phenomena that our work has addressed and the kind of experimental tests used to study them. Then, in the following Sections, we review the challenges that appear during the characterization, modeling and simulation of TDV, and introduce our solutions to these challenges. Finally, we draw the main conclusions of the work.

II. TDV Phenomenology

Before diving into the existing challenges and our proposed solutions in the different steps involved in the study of TDV phenomena aimed at the development of RAD tools, we will briefly describe TDV. We will also discuss how we have measured these phenomena so that the challenges present in the characterization phase will become more understandable to the reader.

- **Random Telegraph Noise**: this is a transient phenomenon that has been linked to the trapping/detrapping of charge carriers into/from defects. In deeply-scaled technologies, where only a handful of defects are present in each transistor, RTN is observed as sudden and random discrete shifts in the threshold voltage of the device or, equivalently, in the drain current of the transistor, Fig. 2a. RTN is commonly measured by biasing a device at constant, nominal voltages and recording the drain current trace or the threshold voltage. In our case, we record the drain current of the devices, from which the threshold voltage can be inferred (Fig. 2.b). To obtain information relevant to construct a defect-centric model, it is necessary to extract the defect parameters from such current traces. These parameters are the number of defects, the time constants of these defects (τ_e, τ_c), which are defined as the average time that a defect takes to emit (τ_e) or capture (τ_c) a charge carrier when occupied/empty, and the current (δI) or threshold voltage (η) shift associated to the trapping/detrapping in/from each defect.

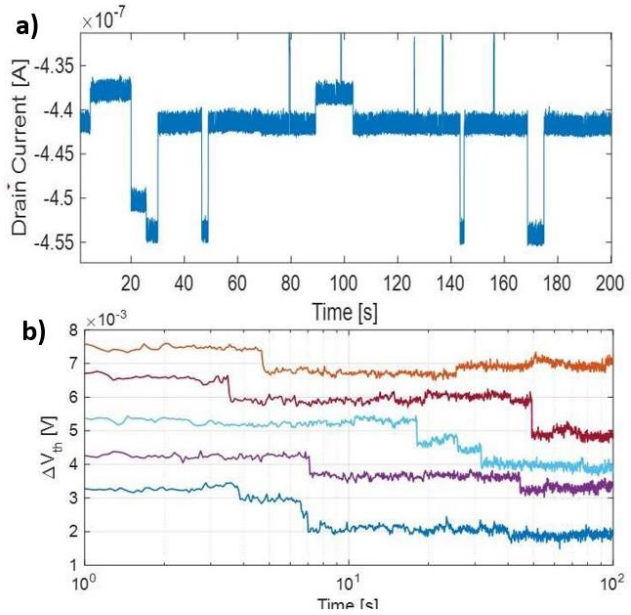

Fig. 2. Examples of RTN signals (a) and BTI recovery (b) threshold voltage traces recorded in our samples.

- **Bias Temperature Instability**: this is a gate-voltage- and temperature-activated aging phenomenon that leads to the gradual degradation of transistors. It is widely accepted that the same type of defects are responsible for RTN and BTI [12,18]. At nominal biasing conditions, the impact of BTI is only clearly visible in a time scale of weeks, months or even years. Thus, it is a common practice to apply high voltages and/or high temperatures (stress) to accelerate BTI degradation. In particular, measurement-stress-measurement (MSM) tests are conventionally employed to study this phenomenon. In these tests, samples are first measured to record a fresh reference, then stressed with a high gate voltage/temperature, and then measured again at nominal conditions to evaluate the impact of the stress. Several Stress Measurement (SM) cycles can follow the initial M cycle. In our case, we have usually employed a sequence of one fresh M phase, followed by 5 SM cycles of increasing stress times (1, 10, 100, 1,000 and 10,000 s) and constant measurement duration (100 s). During the measurement phases, the drain current of the devices is measured, and information about how the threshold voltage changes is recorded. Since BTI also has a recoverable component [11], this recovery is also studied during the measurement phases (some examples are shown in Fig. 2.b). This recovery is observed as sudden increases in drain current (decreases in threshold voltage) caused by the emission of trapped charge carriers. Analogously to the RTN case, in the framework of constructing a defect-centric model, it is necessary to obtain information about the defect parameters that control BTI aging, such as the number of defects, their time constants and associated shift amplitudes.
- **Hot Carriers Injection (HCI)**: this is a gate-voltage and drain-voltage activated phenomenon in which the defects are generated because of the collisions of high energetic carriers with the interface lattice. The main consequence of HCI is the permanent degradation of threshold voltage and device mobility. Similarly to the BTI case, HCI can be characterized by applying MSM tests.

III. TDV Characterization

Given the TDV properties described in section II, the characterization of TDV phenomena in deeply-scaled technologies entails a series of challenges:

- **Massive characterization**: the parameters associated with the defects that are responsible for TDV phenomena are stochastic and must be described with the suitable statistical distributions. Thus, the characterization should be performed massively to obtain statistically relevant information. Since TDV phenomena are voltage and temperature dependent,

this means that hundreds or thousands of devices should be measured under different voltage and/or temperature conditions.

- **Impractically long characterization times**: characterization of hundreds of thousands of devices under a given condition can lead to impractical or even unfeasible laboratory times.
- **Processing of large amounts of experimental data**: massive characterization of devices leads to large amounts of data, the analysis of which can become a challenge in itself.

During the last years, we have devoted large efforts to provide suitable solutions to these challenges, which are described in the next sub-sections.

A. *A device array to tackle the massive characterization of TDV*

Device arrays have gained interest for the characterization of TDV [23-27]. Shifting from wafer-level tests to array IC measurements implies a large reduction of area since the contact pads can be shared by a large number of devices in such arrays. Also, as it will be seen in the next point, device arrays allow stress parallelization, which can greatly reduce experimental times. We have presented a device array chip for the statistically significant and accurate characterization of individual FETs, named the Endurance chip [27]. A block diagram of the Endurance chip is shown in Fig. 3. This device array, fabricated in a commercial 65 nm, 1.2 V, planar technology, includes 3,136 FETs. These devices are nMOS and pMOS fabricated in 8 different geometries ranging from W×L = 80nm×60nm to W×L = 1,000nm×1,000nm. The architecture of the chip is such that individual access to the terminals of each device in the array is possible. Each device can be set in three different modes by means of digital signals: stress, measurement or standby. In each of these modes, the digital signals control the transmission gates that determine to which paths the terminals of each device are connected, so that MSM tests can be implemented. Then, it is possible to measure one specific device (device in measurement mode) while other device(s) are stressed in parallel (devices in stress mode) and others are left unstressed (devices in standby mode). This allows an accurate control of the timing of the biases applied to the devices throughout the tests. Thus, the Endurance chip allows the accurate measurement of TZV, RTN, BTI and HCI in individual devices.

Although device array ICs represent a much denser solution for TDV characterization than conventional wafer-level tests, it also gives rise to some issues. For instance, undesired voltage drops may appear along the lines. To avoid this, the Endurance chip incorporates a Force&Sense architecture in the drain lines to compensate for any such voltage drop. Also, the IC must be prepared to withstand the large currents that may appear when a large number of devices are stressed in parallel. This has been addressed by dimensioning the different lines and transmission gates accordingly to the expected current levels.

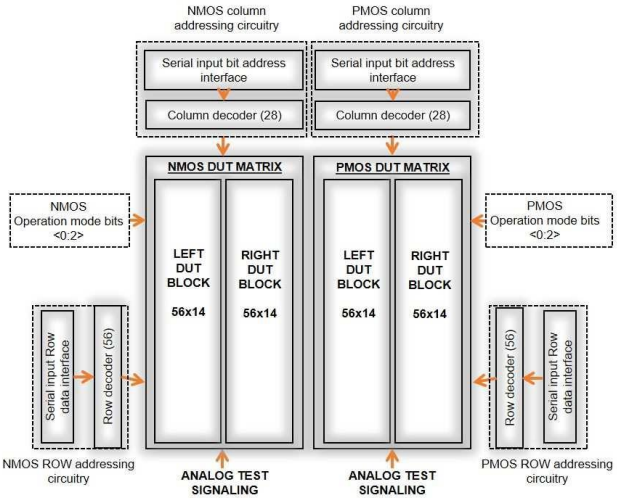

Fig. 3. Block diagram of the Endurance chip, which contains a total of 3,136 devices for TZV and TDV characterization [27].

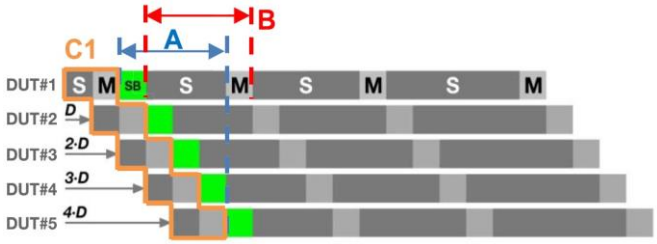

Fig. 4. Example of the improved PSPM scheme applied to five DUTs during a four-cycle SM test [29].

B. *A smart parallelization scheme to drastically reduce laboratory testing times*

In conventional accelerated aging tests, devices are stressed for hundreds or thousands of seconds. If a large number of devices undergo such tests serially, the experimental times can become unattainable [28]. This is the case for wafer-level tests performed with a probe station. Contrarily, , the architecture of the Endurance chip allows to bias multiple devices through the stress paths (devices on stress mode) while another device is biased and measured through the measurement paths (device on measurement mode). This can be exploited in a typical MSM test by setting a number of devices in stress mode simultaneously, i.e., by parallelizing the stress. However, when hundreds or thousands of devices must be measured, the task of minimizing the test time while keeping the same exact timing for all devices under test can become cumbersome. For this reason, we developed the software tool TARS [29]. This tool takes as input the user-defined test parameters such as the number of devices to test or the number and duration of the stress and scheme (Fig. 4). Additionally, the TARS tool automatically generates all the necessary GPIB commands to communicate with the instruments that conform the experimental setup. measurement cycles) and calculates the optimal timings for an improved parallel-stress/pipeline-measurement (PSPM). To illustrate the improvement that such a parallelization scheme brings, one can consider 4 BTI MSM

tests, each one performed on 200 devices with 5 stress-measurement cycles in which the duration of the stress cycles increase exponentially (1, 10, 100, 1,000 and 10,000 s) and the duration of the measurement cycles is kept at 100 s. Such tests would take ~107 days if performed serially, but only ~4.8 days with our improved PSPM scheme.

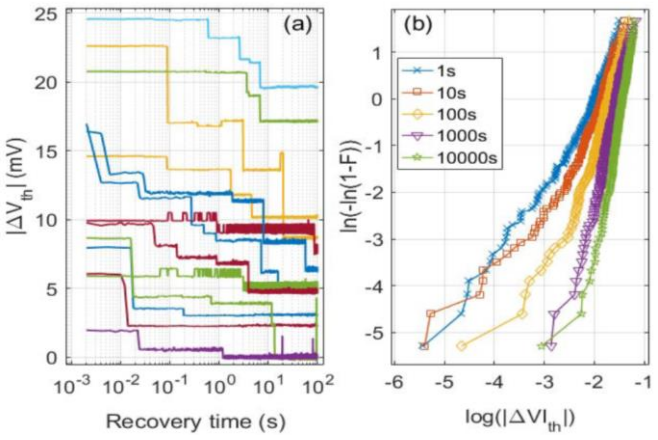

Fig. 5. a) ΔV_{th} evolution with time after the BTI degradation in some selected devices. b) Cumulative distribution functions of ΔV_{th} at different stress times measured in 200 pMOS transistors.

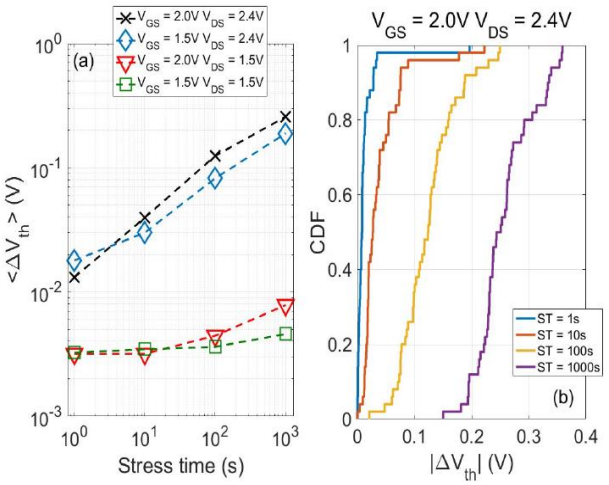

Fig. 6. a) Mean ΔV_{th} evolution with time after HCI stress at different gate voltage and drain voltage configurations. b) Cumulative distribution functions of ΔV_{th} at different times after de HCI stress measured in 200 pMOS transistors.

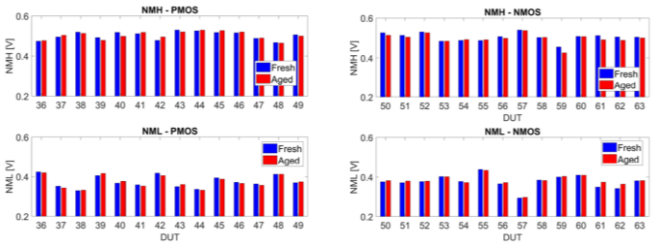

Fig. 7. Noise Margin High (NMH) and Low (NML) measured in CMOS inverters before and after the stress.

The Endurance chip, together with the developed smart parallelization scheme, allows an accurate TDV characterization. An example is presented in Fig. 5, where 200 pMOS transistors were subjected to BTI tests with stress phases with times ranging between 1 s and 10.000 s. Fig. 5a shows selected recovery threshold voltage shift traces and Fig. 5b shows the evolution of their cumulative distributions with the stress time. Fig. 6 shows another example in which 200 transistors were subjected to HCI stress. Fig. 6a shows the evolution with time of the ΔV_{th} mean value and Fig. 6b shows the ΔV_{th} cumulative distributions functions at different stress times. Examples of Fig. 5 and Fig. 6 proves that our proposal is valid to measure the TDV effects simultaneously in hundreds of devices.

Additionally, this approach can be easily extended to evaluate TDV in circuits. In [30] it is presented a new chip designed to measure TDV in basic circuits such as inverters, current mirrors or sense amplifiers using the same principles as in Endurance. As an example, Fig. 7 illustrates the change in the noise margins of inverters when aging is induced on their devices.

This section has presented a complete characterization procedure of TDV in hundreds of devices that can be extended to circuits and can be very useful to evaluate the reliability of a given technology. However, this could be not enough to correctly evaluate TDV effects, since the operating conditions of interest of our devices/circuits may be outside of the experimental window. Then, , it is necessary to use well-established models that can predict the TDV effects beyond the measurement conditions. The next section covers the main challenges and our proposed solutions to achieve accurate models that will allow evaluating TDV through simulations.

IV. TDV Analysis and Modelling

One of the most accepted frameworks for TDV phenomena is provided by defect-centric models, which account for the stochasticity in the threshold voltage shifts observed in deeply-scaled CMOS technologies. In our work, we have used the Probabilistic Defect Occupancy (PDO) model [22]. In such defect-centric models, ΔV_{th} depends on the number of defects in the transistor (N) and their major parameters, that is, the amplitude of the threshold voltage shift associated with each defect and their capture and emission time constants. These parameters do not take the same value for all transistors. Instead, they follow statistical distributions that must be unveiled to accurately describe the impact of TDV phenomena on CMOS transistors. This stochasticity entails some challenges that must be faced for the construction of a defect-centric model such as the PDO:

- **The current (or threshold voltage) shift associated with a defect can take very small values**: when a defect captures or emits a charge carrier, the threshold voltage of the transistor will undergo a discrete shift. In our measurements, this will translate into a drain current shift. These shifts can often be quite small, below the nA range. Depending on the background

noise level and the resolution of the measurement instrument, it can be challenging to accurately unveil the statistical distribution of these shifts.

- **The capture and emission time constants of defects can span across many orders of magnitudes**: it has been reported that the defect time constants can span from values below the µs-range to values well above the thousands of seconds [31]. Additionally, these time constants strongly depend on the biasing conditions. This can critically complicate the extraction of the time constant distribution, as, in a typical MSM test, only a small fraction of the total time constant distribution is inspected.

A. *Robust and automated methodology for the analysis of large amounts of TDV data*

In our massive characterization tests, where hundreds or thousands of devices are measured, large amounts of data are generated. In the case of our TDV tests, as explained in Section II, these data will correspond to current traces that may present discrete jumps linked to trapping/detrapping events. Then, the processing of these data should extract information such as the number of defects in each device, the threshold voltage shift associated with each defect, the time constants of each device or the threshold voltage shift after each stress cycle. The extraction of this information can sometimes be problematic, especially when a high background noise or a high number of defects present in a device complicates the current trace. Manually analyzing each trace would lead to a very long and cumbersome analysis process. For this reason, we developed the TiDeVa tool [32], which, using a Maximum Likelihood Estimation (MLE)-based method, allows to first "clean" the current traces from the undesired background noise, leaving only the discrete current levels caused by charge trapping/detrapping (Fig. 8). From there, it is possible to more easily extract the number of defects, time constants of those defects and associated current shifts. The current shifts are then transformed to threshold voltage shifts using a methodology that compares the experimental current traces to a set of 100,000 I_{DS}-V_{GS} curves generated by uniformly sampling the threshold voltage and the mobility of the transistor [33].

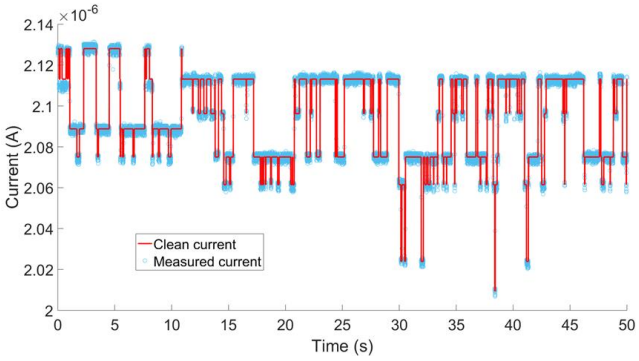

Fig. 8. Example of raw current trace (blue) together with the "clean" trace generated by TiDeVa (red), which allows the extraction of the defect parameters, such as time constants or current shift amplitudes associated to each defect.

Allowing the robust and automated analysis of TDV data, the TiDeVa tool relieves the user of an otherwise almost unfeasible task.

B. *Unveiling the time constant distribution of TDV defects*

Our general approach for the determination of the TDV defect time constants is based on, first, proposing a model for such distribution. Then, we proceed to simulate what we would observe in our MSM tests given such a model, and we vary the model parameters to match the experimental results. In particular, what we attempt to match are the Single Emission Events (SEE), which are defined as the emission of a charge (at

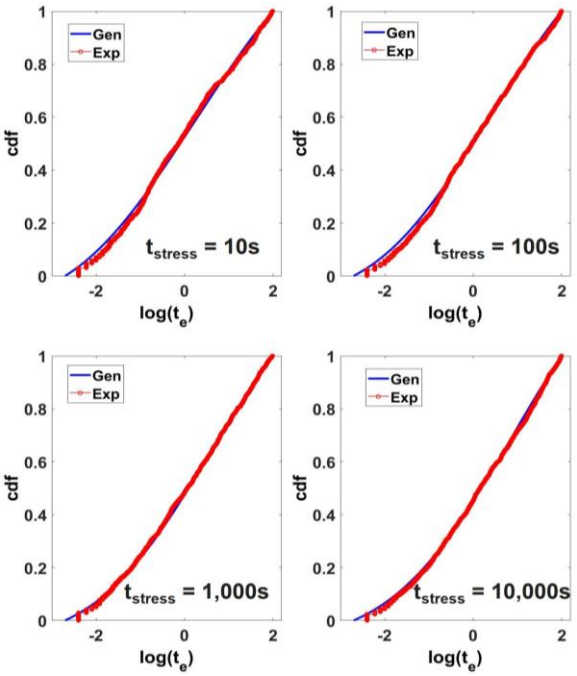

Fig. 9. Comparison of the experimental CDF of the SEEs observed at times t_e for 600 devices stressed at |VGS| = 2.5 V for 4 of the measurement phases in our MSM test (red) together with the SEE CDF generated using the best-fit parameters.

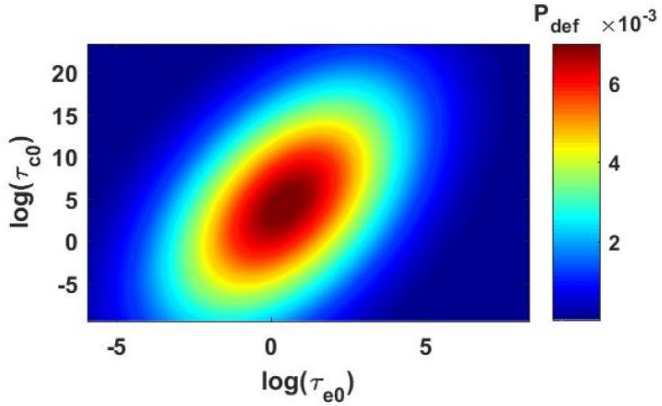

Fig. 10. Example of bivariate lognormal distribution of the defect time constants corresponding to the parameters found through the optimization process.

time t_e) from a defect that does not capture another charge during the remaining of the measurement phase. These are observed in the measurement phases of the MSM as discrete current increases that are not followed by a current decrease of the same amplitude during the remaining of the measurement phase. Other trapping/detrapping events (e.g., an emission followed by a capture) corresponding to RTN have not been considered, since, otherwise, the mathematical formulation of this problem might have become too complex. An example of the evolution of the cdfs of these SSE with the stress time for a given stress voltage is shown in Fig. 8 (red dots).

To mathematically tackle the task of emulating the experimental SEEs, we have considered three conditions (a more detailed mathematical formulation can be found in [34]). First, the defect must exist in order to undergo a SEE. The probability of a defect with a given pair of time constants (τ_e, τ_c) to exist is determined by the probability density function P_{def}. We have considered a bivariate lognormal distribution [21]. Fig. 9 shows an example of such distribution, corresponding to the model parameters found through the optimization process. The time constants depend on the applied voltages, and it has been taking mathematically taken into account in our approach. The second requirement for a defect to undergo a SEE during a measurement phase of the MSM test is that it should be occupied at the beginning of the measurement phase. By taking into account the time constants of a defect (and how they change across stress and measurement cycles when the bias conditions are different), it is possible to calculate its probability of occupation function (P_{occ}) at each instant throughout the test, including the beginning of each measurement phase. The third and final requirement for a charged defect to undergo a SEE during a measurement phase is that it emits a charge carrier during the measurement phase and it does not capture a charge carrier in the remaining of the measurement window. Since both the emission and the capture events can be modeled as Markov processes [35], it is possible to combine both probabilities into the mathematical formulation of a SEE (P_{SEE}). Then, the total probability of a defect to exist, be occupied at the beginning of each measurement phase and undergo a SEE in the experimental window can be calculated by combining P_{def}, P_{occ} and P_{SEE}. Finally, the fitting of the SEE cdf generated for each measurement phase to the experimental cdf of the SEE has been performed using a particle swarm optimization (PSO) [36], a global optimization algorithm that does not require any initial estimate of the initial parameters. The experimental cdfs, together with their best fit, are shown for 4 of the measurement phases (stress of 10 s, 100 s, 1,000 s and 10,000 s) in Fig. 9. The corresponding time constant distribution is shown in Fig.10.

In conclusion, we have exploited a conventional MSM test with increasing stress durations and different biasing conditions in the stress and the measurement phases to explore different regions of the time constant distributions and have mathematically formulated the probability of observing experimentally Single Emission Events to retrieve a time constant distribution that extends across several orders of magnitude in time.

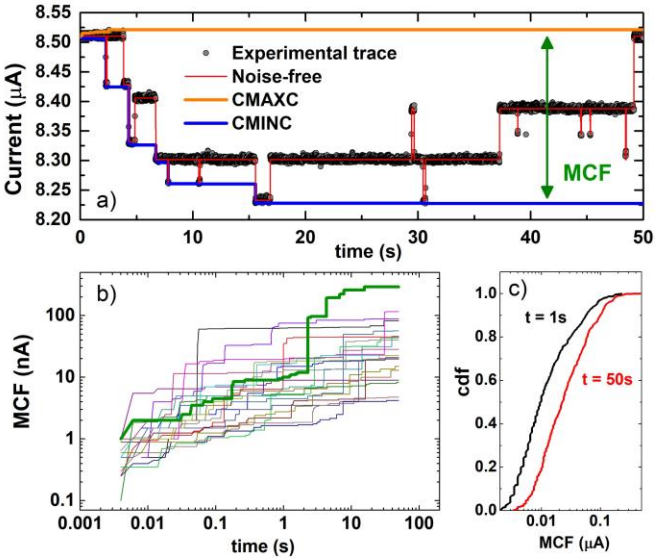

Fig. 11. a) Experimental current trace and current bounds from which the *MCF* is computed. The arrow indicates the *MCF* at around t=41s. b) *MCF*(t) obtained from 20 current traces (the one in Fig. 7a is highlighted in green. c) cdfs of the *MCF*s at t=1 s and t=5 0s for 500 measured devices.

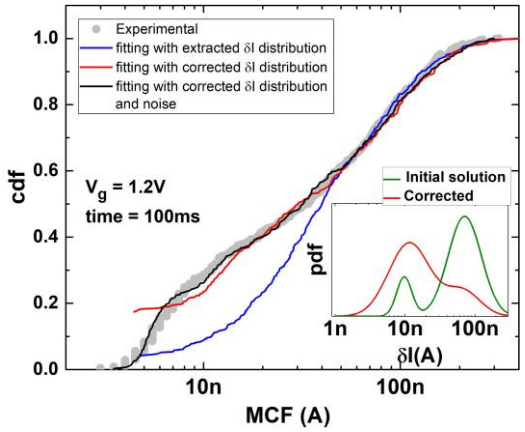

Fig. 12. MCF experimental distribution (grey symbols) and fitting (lines) considering the extracted and corrected δI distribution. The inset shows the initial guess of the δI distribution (green) and the corrected one (red).

C. A Maximum Current Fluctuation (MCF)-based method for the extraction of the distribution of current shifts

In Section III, we presented an MLE-based software tool that is capable of detecting the discrete current shifts within the measured current traces. These can be linked to the trapping/detrapping events and, thus, it is possible to extract the defect parameters from them, including the amplitude of their associated current shifts. The green line in the inset of Fig. 12 corresponds to a distribution extracted in such a manner. This experimental data can be fitted with a double lognormal distribution. However, the shifts with a lower amplitude are sometimes convoluted with the background noise. Thus, we developed a new technique based on the Maximum Current Fluctuation metric (MCF) [37]. The MCF of a measured device

can be defined as the difference between its cumulative current maximum (CMAXC) and its cumulative current minimum (CMINC), as can be seen in Fig. 11a. Thus, the MCF will be affected by discrete current jumps caused by defect trapping/detrapping, together with the background noise. Since the number of defects per device and the parameters of those devices are stochastic, different devices will display different MCF values, as can be seen in Fig.11b and c, which represent the evolution of *MCF(t)* for 20 measured devices and the cumulative distribution functions (cdf) of the *MCF*s at t=1s and t=50 s for 500 measured devices, respectively. The MCF cdf at a given time will be affected by the number of active defects up to that time (i.e., the number of defects that have trapped or detrapped a charge carrier), the amplitudes of their associated shifts and the background noise. Then, what we have done is to fit the experimental *MCF* cdf at given time instants utilizing as our optimization parameters the number of active defects (which follows a Poisson distribution [11]), the parameters of the double lognormal distribution for the current shift amplitudes, and the level of background noise. When only the defect parameters are considered, the red line in Fig. 12 is obtained. This represents already an improvement with respect to the blue line, which corresponds to the case in which the distribution extracted through the MLE-based method is used. When the background noise parameter is included in the optimization process, an even better adjustment is attained (black line in Fig. 12). The current shift amplitude distribution corresponding to this optimal adjustment is shown in the inset of Fig. 12 (red line). Notice that the main difference with respect to the MLE-extracted distribution is that more defects with a lower associated amplitude are found. This could be expected, as these defects may go undetected with a method that aims at detecting each individual discrete current transition if their amplitude is similar to the noise level. However, their associated current jumps will still affect the MCF metric, and thus they will be accounted for when using the MCF-based technique. This reinforces the adequacy of the MCF-based technique to get a deeper insight into the distribution of the current shift amplitude associated with defects.

V. CASE: A TDV Simulation in Circuits

Finally, the models that can take into account the effects of TDV, together with the extracted parameters, must be efficiently implemented in simulation tools that correctly transfer the TDV effects at device level to the circuit performance, accounting for all the particularities that may be relevant. As an example, CASE [38] is a tool for circuit reliability simulation that takes into account the stochastic nature of aging by using the PDO model, the joint inclusion of TZV and TDV and the updating of biasing conditions over time. CASE implements a fully automated simulation flow by linking TDV with a commercial circuit simulator directly implementing its effects in the transistors model card. With the help of CASE, designers can efficiently account for the impact of process variability and aging in the design process. To illustrate one of the CASE utilities, Fig. 13 shows the results obtained from simulating a Miller operational amplifier accounting for TZV and TZV together with TDV, in this particular case. These simulations have been carried out taking into account the particular operating conditions of each transistor within the circuit during its working life, which have been used to evaluate the TDV effects in each transistor within the circuit and included them in the devices model card.

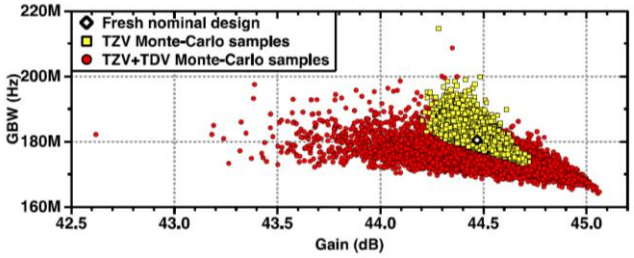

Fig. 13. Comparison Gain vs Gain-Bandwidth in 1000 Miller operational amplifier taking into account TZV and TZV together with TTDV.

VI. Conclusions

This work has presented a complete framework to characterize, model and evaluate Time-Dependent Variability (TDV) in devices and circuits, starting from the basic characterization of transistors and ending in the evaluation of the circuit's performance, going through the required modeling and simulation approaches.

To account for the TDV impact on transistors, massive device characterization in reasonable times must be performed. To face this challenge, we have designed and fabricated the Endurance chip together with a smart parallelization scheme that allows the characterization of hundreds of devices in reasonable measurement times. Moreover, the approach has been successfully extended to evaluate TDV in basic circuits. Accurate models are required to evaluate TDV impact beyond the limits imposed for the experimental procedures, such as the defect-centric PDO model. From the test results, the model parameter will have to be accurately extracted. With this aim, several analysis techniques and model approaches have been presented that allow obtaining the relevant parameters, and their statistical distributions. Finally, the CASE tool has been presented, which is a complete simulation tool that transfers the device TDV effects to the circuit performance, accounting for the actual operation condition of all the transistors within the circuit and accordingly modifying the devices' model card.

As a final conclusion, TDV requires solutions at three different levels: device characterization, modeling and simulation approaches. Here we have proposed solutions at these levels that all together constitute a powerful tool to optimize circuit reliability during its design phase.

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