A Multi-Self-Cascoded Voltage Reference with 2.73-ppm/V Line Sensitivity and 20.1-ppm/°C Temperature Coefficient at 0.45-V Supply

Francesco Gagliardi[1], Paolo Bruschi[1], Massimo Piotto[1], Soumaya Sakouhi[1] and Michele Dei[1]
[1]*Department of Information Engineering, University of Pisa, 56122 Pisa (PI), Italy*
Email: {francesco.gagliardi, paolo.bruschi, massimo.piotto, michele.dei}@unipi.it, soumaya.sakouhi@ing.unipi.it

***Abstract*—Recent advancements in low-power and low-voltage integrated circuits have spurred significant research interest, particularly for applications with demanding supply conditions. This work presents a single-branch voltage reference achieving exceptional immunity to supply voltage variations. Leveraging a ΔV_{GS}-based approach, the design utilizes transistors with different channel lengths to exploit geometry-dependent threshold voltage differences, enabling effective temperature compensation. Additionally, a multi-self-cascoded technique enhances immunity to supply voltage variations. Post-layout simulations of a 0.18-µm CMOS design, operating with supply voltage as low as 0.45 V, demonstrate a line sensitivity of 2.73 ppm/V and a temperature coefficient of 20.1 ppm/°C, with power consumption below 200 pW. The proposed architecture is shown to be a robust solution for implementing precise, low-voltage and low-power voltage references.**

***Index Terms*—Voltage reference, low power, low voltage, energy harvesting, temperature coefficient, line sensitivity, PSRR, self-cascoded, reverse short-channel effect.**

I. Introduction

Several of today's emerging applications, ecompassing wearable smart-sensing electronics [1]–[3], implantable medical devices [4] and environmental sensor nodes [5] require circuit solutions compliant with dramatically low supply voltage levels. Power consumption minimization is also of paramount importance, to cope with the highly-constrained power budgets offered by miniaturized batteries and energy harvesters. Integrated Circuits (ICs) designed for standalone-operation in the aforementioned contexts strongly require novel efficient implementations of reference circuits [6]–[12].

Recent works introduced effective Voltage Reference (VR) topologies featuring deep-subthreshold operation and minimal circuit complexity, often combined with leakage-based biasing strategies, to attain low-voltage and low-power capabilities. Among these innovative solutions, VRs based on Stacked Diode-connected MOSFET (SDMT) structures derive the output voltage from the difference between the V_{GS} voltages of stacked transistors [13]–[17]. Furthermore, based on a similar principle, leakage-based VRs [6], [18]–[33] leverage the subthreshold current of a transistor with zero or even negative V_{GS} to bias a properly scaled diode-connected MOSFET. Temperature compensation of these types of VRs can be achieved by combining different device types and selecting proper dimension ratios between them. However, besides temperature stability, ultralow Line Sensitivity (LS) is also required in various power-constrained applications (for instance, to minimize the effects of the possibly large supply voltage disturbances occurring upon variations of the harvester operating conditions in an energy-harvested system).

Herein, we present a novel single-branch NMOS-only VR, combining several circuit techniques into a highly accurate low-voltage and low-power design. To perform temperature compensation, a SDMT structure is included, supplied by a leakage current generator. The SDMT is implemented with transistors of the same type sized with different channel lengths. Thusly, the Reverse Short-Channel Effect (RSCE) [34], [35] is exploited to generate the Complementary-to-Absolute-Temperature (CTAT) term, consisting of a difference between unequal threshold voltages, needed for temperature compensation. Besides, an additional self-cascode arrangement is introduced, giving rise to a Multi-Self-Cascoded (MSC) architecture. The achieved LS and Power-Supply Rejection Ratio (PSRR) significantly improve the state of the art on low-voltage VRs. The remainder of this paper is organized as follows. Section II introduces the proposed VR. Section III reports on the results of accurate post-layout simulations. Finally, Section IV offers a state-of-the-art comparison.

II. Proposed Voltage Reference

In Fig. 1(a), a preliminary version of the proposed VR is shown, while the complete MSC architecture is shown in Fig. 1(b). A SDMT structure, composed by transistors M_1 and M_2, is employed to generate the output voltage, V_{ref}, while M_3, in deep-subthreshold conditions, generates the bias current in the form of subthreshold leakage. Recently, this approach has been widely used to push VR designs towards increasingly smaller supply voltages and power levels [6], [18]–[33]. To ensure saturation of M_3, the latter is implemented as a Low-V_{th} (LVT) device. In many CMOS processes, LVT devices are available as transistors with lightly-doped channel.

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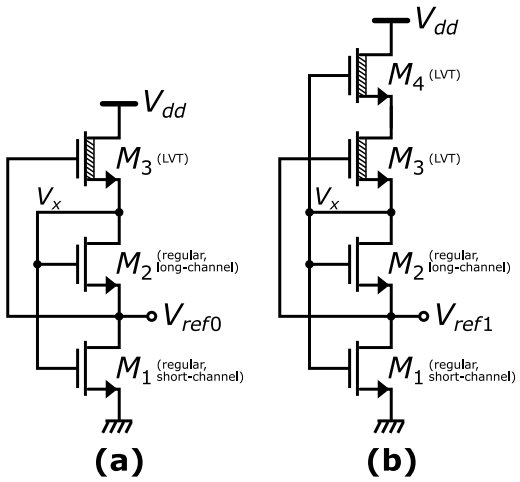

Fig. 1. Schematic view of the proposed circuit: (a) basic VR; (b) MSC-VR.

With the SDMT approach, V_{ref} is generated as $V_{ref} = \Delta V_{GS1,2} = \Delta V_{th1,2} + \Delta V_{od1,2}$ where $\Delta V_{GS1,2}$, $\Delta V_{th1,2}$ and $\Delta V_{od1,2}$ indicate the differences between the gate-source voltages, the threshold voltages and the overdrive voltages of M_1 and M_2. $\Delta V_{th1,2}$ is typically a CTAT term, usually obtained by implementing M_1 and M_2 with different transistor types (e.g., exploiting different gate oxide thicknesses or channel doping concentrations); conversely, through weak-inversion biasing of M_1 and M_2, $\Delta V_{od1,2}$ results to be a Proportional-To-Absolute-Temperature (PTAT) term. In this work, we derived the V_{th} difference exploiting geometry-dependent effects, taking inspiration from the approach recently proposed in [17]. Specifically, in the employed 0.18-µm CMOS process, the RSCE [34], [35] results to be the prevailing geometry-dependent effect, giving rise to V_{th} reduction as channel length is increased. Thereby, by designing M_1 and M_2 with short and long channels, respectively, the required $\Delta V_{th1,2}$ is obtained.

Regarding the temperature behavior of $\Delta V_{th1,2}$, it is important to note that the RSCE is primarily caused by highly doped halo regions introduced around the drain and source areas in many CMOS processes. Such halo regions, typically doped with impurities opposite to the drain-source wells, increase the average dopant concentration in the channel. This effect is more significant for short-channel devices, leading to a higher threshold voltage compared to long-channel ones. Furthermore, as implied by device physics models [36], higher doping of the channel may cause greater V_{th} sensitivity to temperature, leading to the Temperature Coefficient (TC) of V_{th1} to be more enhanced (more negative) than that of V_{th2}. Thereafter, with the adopted design choices, the overall temperature trend of $\Delta V_{th1,2}$ results to be CTAT.

V_{ref} is analytically derived in the following. To describe transistor behaviours, the Enz-Krummenacher-Vittoz (EKV) model [37], [38] is adopted. In weak-inversion and saturation conditions, the following equation is employed to express the drain current as a function of the gate voltage (V_G) and the source voltage (V_S), both referred to the grounded bulk:

$$I_D = I_S \exp\left(\frac{V_G - V_{th} - nV_S}{nU_T}\right), \tag{1}$$

where U_T, n and I_S indicate the thermal voltage, the sub-threshold slope factor and the specific current, respectively. I_S is defined as $I_S = 2n\mu C_{ox} U_T^2 W/L$, where μ, C_{ox}, W and L indicate the mobility, the gate capacitance per unit area and the channel width and length, respectively. Through direct calculations, the following expression is found to express V_{ref}:

$$V_{ref} = \frac{V_{th1} - V_{th2}}{n} + U_T \ln\left(\frac{\mu_2 W_2 L_1}{\mu_1 W_1 L_2}\right), \tag{2}$$

assuming that M_1 and M_2 have the same n factor. It is worth noting that, besides adopting $L_2 > L_1$ to create the V_{th} difference, the ratio between the aspect ratios of M_1 and M_2, $\frac{W_2/L_2}{W_1/L_1}$, also has to be optimized in order to cancel the temperature trend of the first CTAT term through proper scaling of the PTAT term, proportional to U_T.

Moving to discuss supply sensitivity, small-signal analysis of the circuit of Fig. 1(a) yields the following expression:

$$\mathrm{LS}_0 = \frac{v_{ref0}}{v_{dd}} = \frac{\alpha}{A_3\left(\frac{g_{m1}}{g_{m3}} + n_3 - \alpha\right) + \frac{r_{d3}}{r_{d1}}\alpha + 1}, \tag{3}$$

$$\text{with } \alpha = \frac{v_{ref0}}{v_x} = \frac{g_{m2} - g_{m1} + g_{d2}}{n_2 g_{m2} + g_{d1} + g_{d2}} \approx \frac{1}{n_2} - \frac{g_{m1}}{g_{m2}}. \tag{4}$$

In (3), A_3 is the intrinsic gain of M_3, equal to $g_{m3} r_{d3}$. Assuming saturation of M_3, it represents the largest term at the denominator of (3). The approximate equality in (4) is valid under the assumption $g_{m1,2} \gg 1/r_{d1,2}$, valid in saturation.

For further LS reduction, the additional cascode device M_4 is introduced in Fig. 1(b). By biasing M_4 with gate voltage equal to V_x, higher than V_{ref} by V_{GS2}, saturation biasing of all devices is made possible (also thanks to the use of LVT devices as M_3 and M_4). Concerning the LS of the complete MSC-VR [Fig. 1(b)], the following result is attained:

$$\mathrm{LS}_1 = \frac{v_{ref1}}{v_{dd}} = \frac{\mathrm{LS}_0}{A_4\left[n_4 + \left(\frac{g_{m1}}{g_{m4}} - 1\right)\frac{\mathrm{LS}_0}{\alpha}\right] + \frac{r_{d4}}{r_{d1}}\mathrm{LS}_0 + 1}. \tag{5}$$

From the expressions reported in (3)−(5), it is made evident how the proposed circuit offers two distinct strategies to minimize the LS: (*i*) minimizing the α factor through proper selection of the ratio g_{m1}/g_{m2}, and (*ii*) a double cascode action from M_3 and M_4, leading to $\mathrm{LS}_1 \propto \alpha/A_3A_4$.

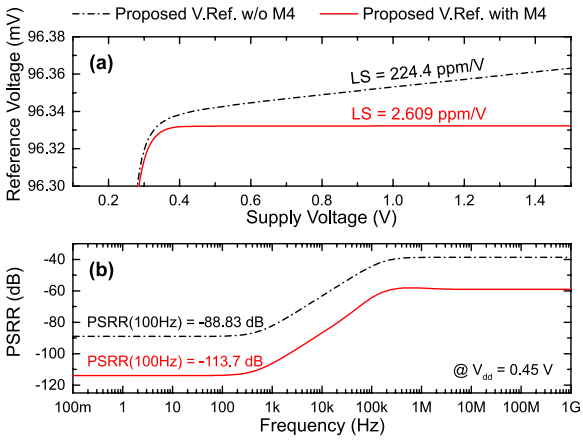

Fig. 2. Pre-layout comparison between the basic VR [Fig. 1(a)] and the MSC-VR [Fig. 1(b)]: (a) V_{ref} as function of V_{dd}; (b) PSRR.

In Fig. 2, a comparison between the two circuits of Fig. 1(a) and (b) is proposed in terms of LS and PSRR. These results were obtained from Spectre pre-layout simulations of 0.18-µm CMOS implementations of the VRs, optimized to yield V_{ref} equal to 96 mV with sub-200 pW power consumption. Thanks to the addition of M_4 (while the dimensions of the other devices were left unchanged), the LS decreases by 86 times, reaching 2.609 ppm/V (evaluated for V_{dd} between 0.45 V and 1.5 V). The PSRR improves by approximately 25 dB.

The employed device sizes are reported in Fig. 3(a), while Fig. 3(b) shows the layout view of the proposed MSC-VR. Its area occupation is equal to 13.5×8.2 µm^2.

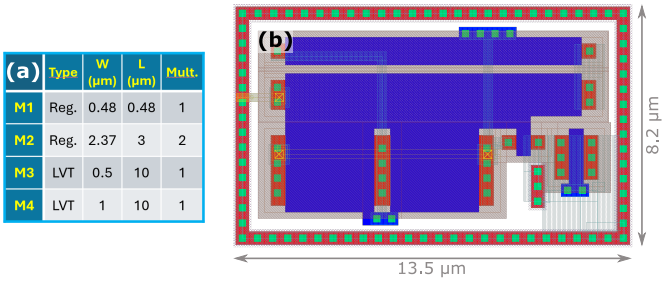

Fig. 3. Proposed MSC-VR design: (a) device sizes; (b) layout view.

III. Post-Layout Simulation Results

In this section, the results of accurate post-layout electrical simulations are reported. Extraction of the layout parasitic components was performed with the Calibre PEX tool, while Spectre was employed for circuit simulations.

In the first place, in Fig. 4, V_{ref} is shown as a function of the supply voltage in different process corners: slow (SS), typical (TT) and fast (FF). The worst-case LS remains as low as 3.07 ppm/V, estimated for $V_{dd} \in [0.45\text{ V},\ 1.5\text{ V}]$.

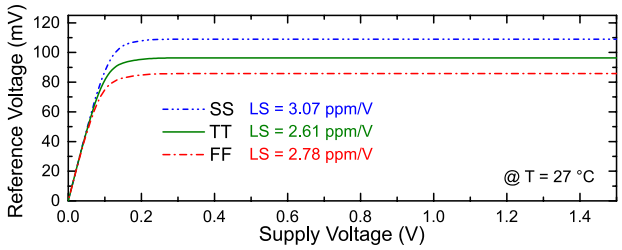

Fig. 4. Reference voltage as a function of the supply voltage.

In Fig. 5(a), the PSRR is shown as a function of frequency, both in pre-layout and post-layout conditions. Due to parasitic capacitances in the layout, the 3-dB bandwidth of the PSRR decreases from 448 Hz (pre-layout) to 83 Hz (post-layout). However, in the presence of a load capacitor of $C_L = 500$ fF connected between V_{ref} and ground (representing possible input capacitances of n-type-input circuits connected to the VR output node), the high-frequency PSRR results to be decreased, while the PSRR at low frequencies is left unchanged. Fig. 5(b) shows the post-layout PSRR in different process corners without any load capacitor.

The temperature behaviour of V_{ref} is shown in Fig. 6 across process corners. The typical TC is equal to 9.183 ppm/°C from −20 °C to 80 °C, while the worst-case TC (SS corner) remains below 30 ppm/°C. In Fig. 7, the current consumption is plotted as a function of temperature, showing the typical exponential trend encountered in leakage-based VRs [6], [18]–[33].

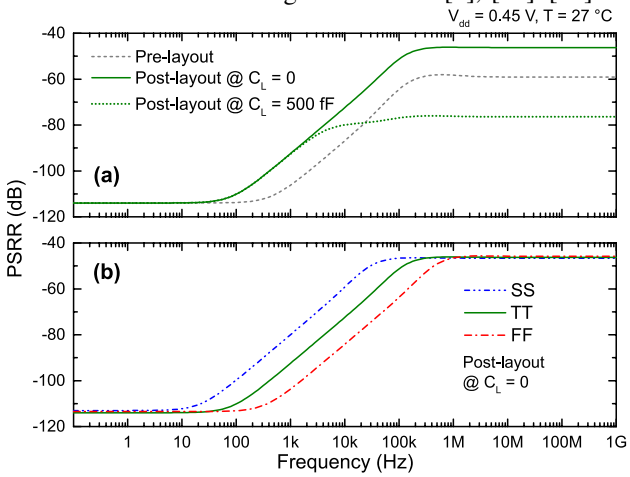

Fig. 5. PSRR as a function of frequency: (a) comparison between pre-layout and post-layout results; (b) PSRR in different process corners.

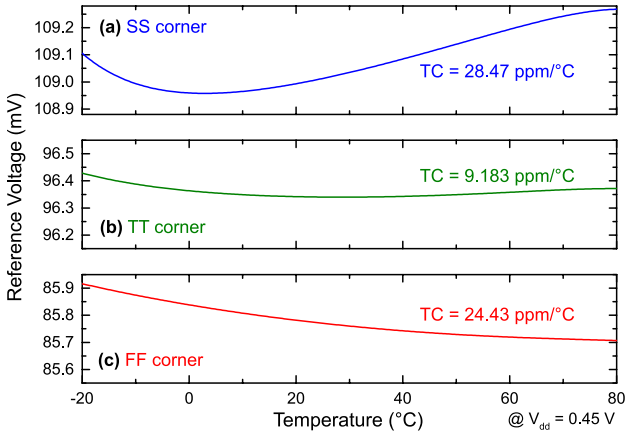

Fig. 6. Reference voltage as a function of temperature in different process corners: (a) slow; (b) typical; (c) fast.

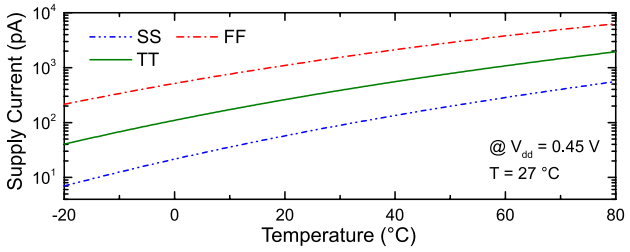

Fig. 7. Supply current as a function of temperature.

The start-up transient of V_{ref} is illustrated in Fig. 8, following a rising ramp of V_{dd}, from 0 to 0.45 V, occurring at $t = 2$ ms and completed in 1 µs. The results achieved in terms of settling time with $C_L = 500$ fF are annotated in Fig. 8.

Fig. 9 shows the output noise spectrum, both in pre-layout and post-layout conditions. The Root-Mean-Square (RMS) noise integrated from 0.1 Hz to 10 Hz is equal to 32.97 µV$_{\text{RMS}}$.

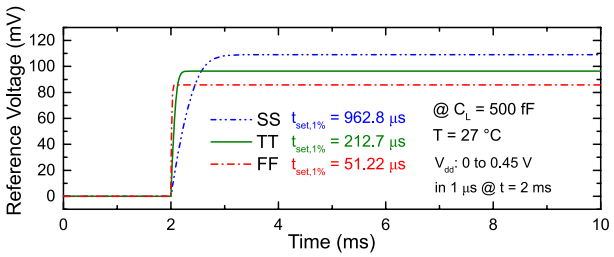

Fig. 8. Start-up transients.

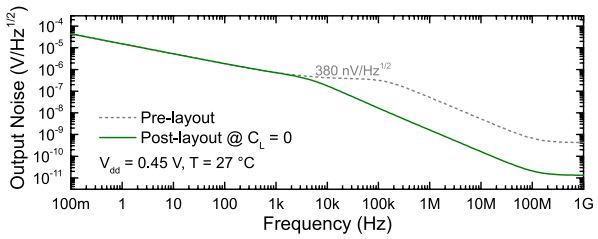

Fig. 9. Output noise spectrum.

Finally, in Fig. 10, the results of post-layout statistical simulations are illustrated concerning the main circuit performances. Sets of 1000 Monte Carlo runs were executed comprising both global and local (mismatch) random process variations. The room-temperature V_{ref} value has a relative standard deviation of 7.27%. The average and worst-case TC values are equal to 20.1 ppm/°C and 77.6 ppm/°C, respectively. The LS metric is equal to 2.73 ppm/V on average terms and has a standard deviation of only 0.341 ppm/V.

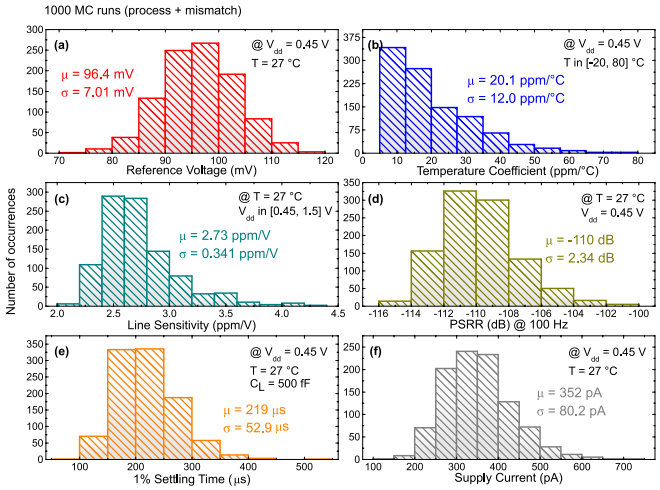

Fig. 10. Process spread of the main circuit performances: (a) V_{ref} value at room temperature; (b) TC; (c) LS; (d) PSRR at 100 Hz; (e) 1% settling time; (f) current consumption.

IV. Discussion

Table I compares the presented MSC-VR with selected works published in the last 5 years. Fig. 11 widens the comparison by means of scatter plots, summarizing the performances of a larger number of recent low-voltage VRs. For the proposed design, average performances across statistical Monte Carlo simulations are marked in red in Fig. 11.

TABLE I
PERFORMANCE COMPARISON OF LOW-VOLTAGE VOLTAGE REFERENCES.

	This work	[25] Electronics 2024	[15] TCAS-I 2020	[29] TCAS-II 2021	[24] Electronics 2025	[23] CICC 2020
Tech. (nm)	180	180	180	180	180	65
Results type	Sim.	Sim.	Meas.	Sim.	Sim.	Meas.
Device types	Reg.+ LVT	Thin+ thick ox.	Thin+ thick ox.	PMOS+ NMOS	Reg.+ ZVT*	Reg.
V_{ref} **(mV)**	96.4†	195.5	147.9	65.7	185†	258
V_{dd} **(mV)**	450	500	340	120	500	500
Power (pW)	158.4†	28.8	48	0.252	630	14.3
T **range (°C)**	−20∼80	0∼100	0∼100	−40∼120	−40∼150	0∼100
TC (ppm/°C)	20.1†	26.7†	14.8#	89.81†	14.4†	78.4
$(\sigma/\mu)_{vref}$ **(%)**	7.27†	6.96†	0.74†	3.95†	6.27†	0.36‡
LS (ppm/V)	2.73†	17.1†	190	2200	38†	200
PSRR (dB)	−110† (100 Hz)	−72 (10 Hz)	−62.7 (10 Hz)	−61 (100 Hz)	−100.5 (100 Hz)	N/A
Noise (μV_{RMS})	65.27◇,⋆	41.8⋆	55⋈,⋆	1740⋆	N/A	N/A
Area (mm^2)	0.00011	0.0024	0.0332	0.00007	0.00079	0.00084

⋆Native NMOS transistors, with nearly zero-V_{th} (ZVT). †From Monte Carlo simulations. ‡Standard deviation calculated on 6 chip samples from the same batch. #After trimming. ◇Integrated noise from 0.1 Hz to 100 MHz. ⋈Integrated noise from 0.1 Hz to 10 Hz. ⋆Without capacitor at the output node.

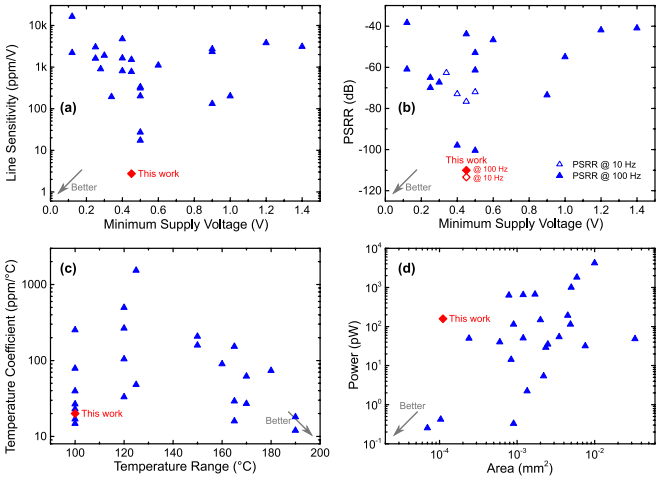

Fig. 11. Performance comparison of low-voltage VRs: (a) LS and V_{dd}; (b) PSRR and V_{dd}; (c) TC and temperature range; (d) power and area. References [6], [13]–[16], [18]–[33] are included in these plots.

Thanks to the proposed MSC architecture, the presented VR achieves best-in-class LS and PSRR metrics, while maintaining compliance with sub-0.5V supply voltages and power consumption in the hundred pW range. Compared to the second best LS result, reported in [25], this work demonstrates an improvement by 4.2 times. The achieved TC is at the low end of the state-of-the-art range, although other works reported wider temperature ranges. Area occupation of the presented design is also highly competitive, attaining the second smallest area among prior works on low-voltage and low-power VRs. These findings highlight the proposed MSC-VR as a solution with great potential for inclusion in ICs operating under very strict power and voltage constraints.

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