2018/2019

Integrated System Design for Digital Processing

Code: 42839
ECTS Credits: 6

Degree	Type	Year	Semester
4313797 Telecommunications Engineering	OB	1	2

Contact

Name: Jordi Carrabina Bordoll

Email: Jordi.Carrabina@uab.cat

Use of languages

Principal working language: english (eng)

Teachers

Lluís Antoni Teres Teres

Quang Vinh Ngo

David Castells Rufas

Prerequisites

Knowledge on the following subjects is recommented:

Electronic Systems Design
Digital Sistemes and Hardware Description Languages
Electronic Systems and Applications

Objectives and Contextualisation

The main objective of this course is to learn, understand and be able to design electronic systems with the focus on embedded systems. These Systems are composed of integrated circuits (or SoC from Systems on a chip) that manage their capacity of computation and communication through wired or wireless protocols. The study of these integrated systems will be oriented to the usual digital processing archtiectures in modern electronics: single-core (i.e. wireless sensor networks), multi-core (i.e. multimedia devices) and many core (high performance computing), and the different types of computation: data-flow and reactive. Digital systems are integrating also non digital components such as sensors, actuators, analog, RF and power components. We will review the different fabrication technologies available in the market, from silicon technologies to new processes for organic and flexible electronics, and we will use FPGA platforms to implement such systems in the labs.

Skills

- Be capable of using programmable logic as well as designing advanced electronic systems, both analogue and digital.
- Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
- Capacity for working in interdisciplinary teams

- Knowledge of the hardware description languages for highly complex circuits
- Maintain proactive and dynamic activity for continual improvement
- Students should be capable of integrating knowledge and facing the complexity of making judgements using information that may be incomplete or limited, including reflections on the social and ethical responsibilities linked to that knowledge and those judgements
- Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
- Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously

Learning outcomes

1. Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
2. Capacity for working in interdisciplinary teams
3. Design ASICs
4. Design integrated circuits using hardware description languages through ASICs and/or FPGAs
5. Knowledge of the hardware description languages for highly complex circuits
6. Maintain proactive and dynamic activity for continual improvement
7. Students should be capable of integrating knowledge and facing the complexity of making judgements using information that may be incomplete or limited, including reflections on the social and ethical responsibilities linked to that knowledge and those judgements
8. Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
9. Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously
10. Use programmable digital logic.

Content

1. Introduction to the Design of Integrated Systems for Digital Processing

Fundamental Concepts bàsics on Ciber-Phyísical Systems

Functional Specificacions

User Centered Design

Performmance Requirements

High Level System Design

2. Systems-on-a-Chip Design

Computational Models and Advanced Programming

SoC and MPSoC Architectures

Embedded Plataforms

Verification, Prototyping and Test

Industrialization; IPs and Patents

3. Integrated **Circuit Design** Methodologies

ASIC and FPGA Design Methodologies

VHDL Modelling, simulation and synthesis

4. Integrated Systems **Implementation** Technologies

Digital CMOS cell libraries

EDA Tools

Technologies for the Fabrication of Integrated Circuits

Printed Electronics and High Performance PCBs

Laboratory: Integrated Digital Processing on FPGA

Methodology

We propose a "top-down" model. Starting from a system level specification, for both functionality and performance requirements, to later refine that specification, towards its materialization through plaform and model based design methodologies, downto its implementation at structural level of HW and physical components.

The course will be mainly driven by the lectures, that will use adhoc material (presentations and documents) available in the virtual campus of the UAB.

Two seminars are schedulled and others can also be added, according to the parallel activity at UAB, in order to analyse in depth specific topics.

Laboratory work will let the students to apply and experiment the concepts acquired on FPGA platforms widelly used in industry.

According to the personal interests of every student, a scientific and/or technologic paper will be selected in order to get familiar and evaluate the knowledge that is available through specialized journals and publications.

Optionally, for students with previous knowledge in embedded systems and/or VHDL and/or FPGA we are proposing their participation in international challenges for embedded systems. That participation will replace the activities of laboratory and critical review.

Activities

Title	Hours	ECTS	Learning outcomes
Type: Directed			
Laboratory Sessions	15	0.6	1, 2, 5, 4, 6, 7, 8, 9, 10
Lectures	22	0.88	1, 5, 3, 4, 6, 7, 8, 10
Thematic Seminars	4	0.16	1, 3, 6, 7, 8, 9
Type: Supervised			
Selection and follow-up of a personalized scientific-technologic journal paper	14	0.56	1, 6, 7, 8, 9
Type: Autonomous			
Laboratory activities preparation and evaluation	20	0.8	1, 2, 5, 4, 7, 8, 10

Study	69	2.76	1, 5, 3, 4, 6, 7, 8, 10

Evaluation

Evaluation is based on:

• 2 parcial exams containign both theoretical concepts and exercices. M;inimum mark on those exams is 3 (over 10)

• Team work at lab scheduled in 5 sessions with the need to deliver the corresponding reports (delivered individually). This is mandatory to pass the course evaluation.

• Individual work on the critical review of a specific scientific and/or technological paper

• The participation in an international challenges from embedded systems companies will replace the activities of laboratory and critical review.

A method to recover failed parcial exams will be provided.

Any change on the above evaluation method will be communicated in advance

A student will be considered as NON PRESENTED if he/she did not participate in the following evaluation activities (defined in the guide): 2nd Parcial Test and Laboratory work reports.

Evaluation activities

Title	Weighting	Hours	ECTS	Learning outcomes
1st Parcial Test	25%	2	0.08	5, 3, 4, 7, 8, 10
2nd Parcial Test	25%	2	0.08	5, 3, 4, 7, 8, 10
Critical review of a personalized scientific-Technologic paper	15%	1	0.04	1, 6, 7, 8, 9
Laboratory work reports	35%	1	0.04	2, 5, 4, 6, 7, 8, 9, 10

Bibliography

F. Balarin et al.: "Hardware-Software Co-Design of Embedded Systems: The POLIS Approach"
Rajsuman, Rochit ."System-on-a-Chip: Design and Test"
P. Bricaud, M. Keating : "Reuse Methodology Manual for System-On-A-Chip Designs"
L. Terés, Y. Torroja, S. Olcoz, E. Villar: "VHDL: Lenguaje estándar de diseño electrónico"
I. Grout "Digital Systems Design with FPGAs and CPLDs"
H.J.M. Veendrick "Nanometer CMOS: from ASICS to BASICS", 2ª edición, Springer. 2017.

http://www.europractice.com/
Example of international challenge http://www.innovatefpga.com/portal/