

**Electrical Characterisation and Reliability**

Code: 43431  
ECTS Credits: 6

Degree	Type	Year	Semester
4314939 Advanced Nanoscience and Nanotechnology	OT	0	A

## Contact

Name: Montserrat Nafria Maqueda

Email: Montse.Nafria@uab.cat

## Use of languages

Principal working language: english (eng)

## Prerequisites

No prerequisites are required for students accepted to the program. It is advisable to have knowledge in electronic devices and their applications.

## Objectives and Contextualisation

This module aims to address the electrical characterization in nanoelectronic devices to assess their performance and reliability.

## Skills

- Communicate and justify conclusions clearly and unambiguously to both specialised and non-specialised audiences.
- Continue the learning process, to a large extent autonomously
- Identify the characterisation and analysis techniques typically adopted in nanotechnology and know the principles behind these, within one's specialisation.
- Show expertise in using scientific terminology and explaining research results in the context of scientific production, in order to understand and interact effectively with other professionals.
- Solve problems in new or little-known situations within broader (or multidisciplinary) contexts related to the field of study.

## Learning outcomes

1. Communicate and justify conclusions clearly and unambiguously to both specialised and non-specialised audiences.
2. Continue the learning process, to a large extent autonomously
3. Describe the principles and identify the possibilities of electric characterisation techniques at the nanoscale.
4. Design accelerated reliability tests in nanoelectronics.
5. Know the mechanisms of variability and malfunction in nanodevices.
6. Show expertise in using scientific terminology and explaining research results in the context of scientific production, in order to understand and interact effectively with other professionals.
7. Solve problems in new or little-known situations within broader (or multidisciplinary) contexts related to the field of study.
8. Use device-level instruments and characterisation methods in nanoelectronic devices.

## Content

The course is structured into 5 blocks:

- 1.- Devices at the nanoscale. Device characterization methods. Advanced Instrumentation.
- 2.- Failure mechanisms in nanodevices: Dielectric breakdown, Hot Carrier injection (HCI) and BTI. Resistive switching phenomenon in dielectrics and applications. Characterization of Random Telegraph Noise (RTN) in nanodevices.
- 3.- Effects of variability in nanoscale. Process variability. Degradation mechanisms and time dependent variability. Modeling and simulation of variability in nanodevices.
- 4.- Reliability in nanoelectronics. Reliability and performance. Reliability models. Reliability test design. Accelerated tests and test conditions.
- 5.- Advanced electrical characterization at the nanoscale. Operating principles and application to nanoelectronics probes for atomic force conductivity (C-AFM), capacitance (SCM) and contact potential (KPFM). Spreading resistance (SSRM). Other techniques.

## Methodology

Students must attend lectures, problem solving classes / cases / exercises and problem-based learning, with an active participation of students in the classroom. They must also make the presentation and defense of planned activities about specific topics and participate in the practical activities in the lab.

## Activities

Title	Hours	ECTS	Learning outcomes
<b>Type: Directed</b>			
Classes to solve problems / cases / exercises and problem-based learning	10	0.4	1, 3, 4, 5, 6, 7
Lectures	12	0.48	6
Oral presentation and discussion of works	6	0.24	1, 6
Practical activities	8	0.32	3, 4, 5, 6, 7, 8
<b>Type: Supervised</b>			
Tutorials	8	0.32	6
<b>Type: Autonomous</b>			
Personal study, reading articles and reports of interest	60	2.4	6
Preparation of works	46	1.84	1, 2, 6

## Evaluation

### Continuous evaluation

A separate evaluation will be made for each of the five blocks into which the course is divided.

For each of the blocks, the evaluation of the level of skills acquisition by the students is made taking into account the activities indicated in the table above, with their weights.

The final mark of the course will correspond to the average of the 5 blocks marks.

To pass the course, the student must have been evaluated of at least 60% of the proposed activities AND obtained an average mark higher than **5**.

### Final evaluation

In case the student fails during the continuous evaluation, but he/she has been evaluated of at least 60% of the proposed activities, specific tests will be planned for final evaluation, which can be theoretical and / or practical, to retake the failed block(s).

### Remarks

Any situation not specified in this document will be analyzed individually.

Assessment procedures may be adjusted, in case that the course development advices to do so.

For each of the blocks, a place, date and hour will be indicated, so that the student can review the evaluation of that block. In case of no-show at the indicated place/date, no other evaluation review will be allowed afterwards.

### Final remarks

Without prejudice to other disciplinary action deemed appropriate and in accordance with current academic regulations, any irregularities committed by the student that may lead to a change in the qualification of an act of assessment will be qualified with a zero. Therefore, copying or allowing copying any evaluation activity will involve failing it with a zero as mark. In case it was needed to be passed to pass the course, the entire course would be failed, without the opportunity to retake them in the same academic year.

The dates of assessment and delivery of works will be published in the campus virtual, and may be subject to changes, for reasons of better programming. Always the information about these changes will be announced in campus virtual, as it is understood that this is the common platform for information exchange between professors and students.

### Evaluation activities

Title	Weighting	Hours	ECTS	Learning outcomes
Attendance and active classroom participation	30%	0	0	1, 3, 4, 5, 6, 7, 8
Delivery of reports / works	40%	0	0	1, 2, 3, 4, 5, 6, 8
Oral defense of works	30%	0	0	1, 6

### Bibliography

- Eugene V. Dirote, "Focus on Nanotechnology Research", Nova Publishers, 2004
- Rainer Waser (Ed.), "Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices", Wiley 2006
- J. H. Stathis and S. Zafar, "The negative bias temperature instability in MOS devices: a review", Microelectronics Reliability, vol. 46, pp. 270-286, 2006.

- R. Degraeve, M. Aoulaiche, B. Kaczer, Ph. Roussel, T. Kauerauf, S. Sahhaf, G. Groeseneken, "Review of reliability issues in high-k/Metal gate stacks", International Symposium on the Physical and Failure analysis of Integrated Circuits, 2008. IPFA 2008.
- W. Wang et. al., "Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology" IEEE Transactions on Device and Material Reliability, 7 pp.509-517, 2007
- T. Grasser, "Bias Temperature Instability for Devices and Circuits", Springer, 2014
- R. Waser, R. Dittmann, G. Staoikoc and K. Szot, "Redox-based resistive switching memories-nanoionic mechanisms, prospects and challenges", Advanced materials, vol 21, issue 25-26, pp. 2632-2663, 2009.
- M. Toledano-Luque, B. Kaczer, J. Franco, P.J. Roussel, M. Bina, T. Grasser, M. Cho, P. Weckx, G. Groeseneken, "Degradation of time dependent variability due to interface state generation", Symposium on VLSI Technology (VLSIT), Page(s): T190 - T191, 2013.
- Groeseneken, G. ; Aoulaiche, M. ; Cho, M. ; Franco, J. ; Kaczer, B. ; Kauerauf, T. ; Mitard, J. ; Ragnarsson, L.-A. ; Roussel, P. ; Toledano-Luque, M., "Bias-temperature instability of Si and Si(Ge)-channel sub-1nm EOT p-MOS devices: Challenges and solutions ", 20th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Page(s): 41 - 50, 2013.
- Luo Weichun, Yang Hong, Wang Wenwu, Xu Hao, Ren Shangqing, Tang Bo, Tang Zhaoyun, Xu Jing, Yan Jiang, Zhao Chao, Chen Dapeng, Tianchun Ye, " Channel Hot-Carrier degradation characteristics and trap activities of high-k/metal gate nMOSFETs ", 20th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Page(s): 666 - 669, 2013.
- P. C. Feijoo, T. Kauerauf, M. Toledano-Luque, M. Togo, E. San Andres, G. Groeseneken, "Time-Dependent Dielectric Breakdown on Subnanometer EOT nMOS FinFETs" , IEEE Transactions on Device and Materials Reliability, Volume: 12 , Issue: 1 , Page(s): 166 - 170, 2012.
- Alvin W. Strong, Ernest Y. Wu, Rolf-Peter Vollertsen, Jordi Sune, Giuseppe La Rosa, Timothy D. Sullivan, Stewart E. Rauch, III, "Reliability Wearout Mechanisms in Advanced CMOS Technologies", 2009, Wiley-IEEE Press
- Yongho Seo and Wonho Jhe, "Atomic force microscopy and spectroscopy", Rep. Prog. Phys. 71, 016101, 2008.
- J. Loos, "The art of SPM: Scanning Probe Microscopy in materials Science", Advanced Materials, 17, 1821, 2005.
- Sergei Kalinin and Alexei Gruverman, "Scanning Probe Microscopy", Springer, 2007.
- International Electrotechnical Commission, standard IEC 61124, and AENOR UNE-EN 61124 , "Reliability testing , Compliance tests for constant failure rate and constant failure intensity", 2014
- International Technology Roadmap for Semiconductors. Semiconductor Industry association(www.itrs.net)
- www.agilent.com
- www.Keithley.com