Universitat Autònoma de Barcelona

2019/2020

Fundamentals of Computers

Code: 102765
ECTS Credits: 6

Degree	Type	Year	Semester
2502441 Computer Engineering	FB	1	2

Contact

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Use of Languages

Principal working language: catalan (cat)
Some groups entirely in English: No
Some groups entirely in Catalan: Yes
Some groups entirely in Spanish: No

Teachers

Jordi Aguiló Llobet
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Prerequisites

There are no prerequisites. However, it is recommended for students to have previously taken the courses "Fundamentals of Computing" and "Electricity and Electronics".

Objectives and Contextualisation

This is a basic training course, taught during the second semester of the first academic year. Computer Fundamentals is the bridge between the courses of Electricity and Electronics and Fundamentals of Computing, in the first year, and Computer Organization in the second year.

The objectives of this course are for students to understand the role of digital systems in the computer world, be capable of designing low-to-medium complexity digital systems using logic gates and reconfigurable devices, and understand that a computer is simply a digital system of a certain complexity. In the last part of the course, a simple computer is presented in order for the students to understand the concepts of process-unit, control-unit, instruction set, microinstructions, microorders and microprogramming.

Competences

- Acquire personal work habits.
- Acquire thinking habits.
- Know about the structure, organisation, operation and interconnection of computer systems, basic programming, and the application of the same to solve engineering problems.
- Know the basic materials and technologies to enable the learning and development of new methods and technologies, as well as those that that provide large-scale versatility to adapt to new situations.

Learning Outcomes

1. Demonstrate knowledge of machine operation algorithm and processor design based on this .
2. Develop a capacity for analysis, synthesis and prospection.
3. Know the basic principles of the structure and programming of computers.
4. Recognise and identify the methods, systems and technologies of computer engineering.
5. Show capacity for the design of basic components (logic ports, flip flops?) and for the design of combinational circuits and programmable logic devices.
6. Understand the basic principles of computer logic, Boolean functions and their minimisation.
7. Work independently.

Content

Block 1: Combinational Circuits (CC)

- Digital signals and digital systems. Description of digital systems.
- Electronic digital systems (EDS). MOS transistors. AND, OR and INV logical gates. Synthesis of EDS as a process of successive refinements.
- Combinational Circuits. Synthesis from a table I: ROM. Synthesis from a table II: logic gates.
- Boolean algebra. Truth tables.
- NAND, NOR, XOR, NXOR logical gates. 3-state buffers.
- Synthesis tools. Propagation time. Other logic blocks: multiplexers, decoders, AND-OR planes (PLAs).
- Synthesis from algorithms.

Block 2: Sequential Circuits (SC)

- The need for sequential circuits. Some examples. States and synchronization. Synchronous sequential circuits.
- Explicit functional description of SCs. State transition graphs and tables.
- Basic components: Bistables. Flip flops and latches.
- Synthesis of SC from tables. Moore and Mealy machines. States encoding.
- Registers, counters and memories. Structure, types and most common uses.
- Finite state machines (FSM). Formal definition. Implementation. Propagation times.
- Basic notions of VHDL. Some examples of FSM description using VHDL.
- Sequential implementation of algorithms.
- Physical implementation of digital circuits. Field Programmable Gate Arrays (FPGA) and other implementation strategies.

Block 3: Process Unit-Control Unit (PU-CU) architecture and processors

- PU-CU architecture.
- PU with multiplexers. PU with busses.
- ROM based Control Unit with sequencers.
- Basic structure of a microprocessor. Von Neumann architecture as an extended PU-CU architecture. Functional units and busses.
- A basic machine-level instruction set. An example of machine code programming.
- Fetch, decoding and execution cycles.
- Micro-orders and condition (status) signals. Microinstructions and microprograms.
- Microprogrammed implementation of the Control Unit.
- Relations between pure hardware, firmware, and high-level software languages.

Methodology

The course is organized in 3 blocks. In blocks 1 and 2, a "*flipped classroom*" learning approach is followed using the materials of a MOOC developed by the course lecturers ("*blended learning*"). These materials include videos that students must watch before attending classes and that explain the theoretical-practical knowledge necessary for the design of digital systems; and interactive exercises with automatic correction. In

small size (40-50 students) face-to-face classes, students' doubts and questions are addressed, and new design cases are worked on. The student must actively participate in these classes; they are not "conventional expository lectures".

In block 3, a more traditional methodology is followed: expository lectures in large groups (about 90-100 students), and problem-solving classes in small groups (40-50).

The course includes laboratory sessions where student physically implements on a FPGA the circuits that thus far they have only designed "on paper". Laboratory sessions are carried out in groups of 20-25 students, with two students per work-place, and last for two hours. Students must, however, demonstrate the skills acquired through an individual test.

The following transversal skills are addressed and assessed during the course:

T01.02 - Develop a capacity for analysis, synthesis and prospection: They are worked on in the face to face classes and assessed within the partial tests.

T02.01 - Work independently: Students must develop these skills by taking responsibility for viewing the videos before classes and doing the exercises autonomously. The viewing (and understanding) of the videos is assessed through Socrative questionnaires at the beginning of the classes. Both the questionnaires and the problems delivered are part of the final grade.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Exercise-based classes	12	0.48	6, 3, 5, 1, 2, 4
Face to face classes	18	0.72	6, 3, 5, 1, 2, 4
Laboratory practices	12	0.48	5
Type: Supervised			
Case study	12	0.48	6, 5, 2, 7
Laboratory practice assignments	10	0.4	5
Type: Autonomous			
Autonomous work	40	1.6	6, 3, 5, 1, 4, 7
Preparing and solving exercises	16	0.64	2, 7
Videos viewing	12	0.48	6, 3, 5, 1, 2, 4, 7

Assessment

a) Assessment activities

Subject assessment will be carried out as follows:

1. Three individual partial tests (one test per block) carried out face-to-face, in a controlled environment, and in written format. These partials tests assess the student's acquired knowledge and his/her skills designing efficient circuits and systems.

2. Exercises resolution: a set of on-line exercises, with automatic grading, must be delivered on previously scheduled dates.
3. The viewing of videos before attending the class and classroom attendance.
4. A face-to-face, on-computer, individual laboratory test, where students must design and simulate a circuit.
5. Lab-sessions preparation and the delivery of homework assignments.

b) Assessment procedure

The mark of the course by continued assessment ( ) is obtained from:

1. (activity 1) the mark obtained in the 3 partial tests (*PT1*, *PT2*, *PT3*),
2. (activities 2 and 3) the delivery of exercises, class attendance and video viewing (*Pb*),
3. (activity 4) the mark of the laboratory test (*LT*), and
4. (activity 5) the lab-preparation and homework assignments (*Lp*)

according to the formula: $CA = PT \cdot 0.5 + LT \cdot 0.3 + Pb \cdot 0.1 + Lp \cdot 0.1$

where: $PT = (PT1+PT2+PT3)/3$

To pass the course the following conditions must be met:

1. $CA \geq 5$,
2. *PT1*, *PT2*, and *PT3* must be ≥ 4, and *CA* must be ≥ 5; and
3. *LT* must be ≥ 5

At the end of the course:

- If the mark obtained in *PT1*, *PT2*, or *PT3* (only one of them) is **<** 4, the student is encouraged to raise this mark by repeating the test scored under 4. To pass the course, the new mark obtained must be $\geq$ 4,and the newaverage of the three marks must be ≥ 5. The mark *PT* will be this new average.
- If a student has obtained a mark **<** 4 in two or more partial tests, he is encouraged to take a final test of the whole course curriculum. The mark *PT* will be the grade obtained in this test, which must be ≥ 5 to pass the course.
- If $LT < 5$ and ($LT \geq 3$ or $(PT1+PT2)/2 \geq 4.5$), the student can retake the laboratory test. The new mark of *LT* will be the mark obtained in this new test and must be ≥ 5 to pass the course.

If $PT < 5$ or $LT < 5$ after retaking these new tests, the final score of the course will be the lowest number between *CA* and 4.5.

c) Scheduling of the assessment activities

The dates of the assessment tests and the submission of exercises are published in the Virtual Campus (VC) and may be subject to changes in programming due to unforeseen eventualities. Any modification will be reported through this platform.

It is important to bear in mind that no assessment activities will be permitted for any student at a different date or time to that established, unless for justified causes duly advised before the activity and with the lecturer's previous consent. In all other cases, if an activity has not been carried out, this cannot be re-assessed.

d) Grades review

The marks obtained by students in each of the tests are published in the VC. Along with the grades, the place, date and time of review will be indicated, allowing students to review the activity with the lecturer. In this context, students may discuss the activity grade awarded by the lecturers responsible for the subject.

If the student does not take part in this review, no further opportunity will be made available.

e) Irregularities committed by the student, copy andplagiarism

Notwithstanding other disciplinary measures deemed appropriate, and in accordance with the academic regulations in force, assessment activities will receive a zero whenever a student commits academic irregularities that may alter such assessment. Assessment activities graded in this way and by this procedure will not be re-assessable. If passing the assessment activity or activities in question is required to pass the subject, the awarding of a zero for disciplinary measures will also entail a direct fail for the subject, with no opportunity to re-assess this in the same academic year.

Irregularities contemplated in this procedure include, among others:

- the total or partial copying of a test, practical exercise, report, or any other evaluation activity;
- allowing others to copy;
- presenting group work that has not been done entirely by the members of the group;
- presenting any materials prepared by a third part as one's own work, even if these materials are translations or adaptations, including work that is not original or exclusively that of the student;
- having communication devices (such as mobile phones, smart watches, etc.) accessible during theoretical-practical assessment tests (individual exams).

f) Assessment of students who followed the subject last year but do not successfully passed it

Students who completed and passed the laboratory practices in the previous course but did not pass the subject may choose not to make them again in the current course. In that case, the laboratory practices mark (*LT*) will be 5, regardless of the grade reached the previous year.

The list of students who can choose this option will be published at the beginning of the course in the VC. If, anyway, the student wants to make the laboratory practices again, he/she must communicate it by mail to the professor responsiblefor the practices.

g) Special grades

- A "non-assessable" grade cannot be assigned to students who have participated in any of the individual partial tests or the final test.
- In order to pass the course with honours, the final grade must be $\geq$ 9.0. Because the number of students with this distinction cannot exceed 5% of the number of students enrolled in the course, this distinction will be awarded to whoever has the highest final grade.

To consult the academic regulations approved by the Governing Council of the UAB, please follow this link: https://www.uab.cat/doc/TR_Normativa_Academica_Plans_Nous

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Exercises delivering	10%	8	0.32	2, 7
Laboratory practices (sessions preparation, assignaments and individual test)	40%	2	0.08	5, 2, 4, 7
Three partial tests and/or final test	50%	8	0.32	6, 3, 5, 1, 2, 4, 7

Bibliography

- Coursera MOOC: https://www.coursera.org/learn/digital-systems
- Digital Systems: From Logic Gates to Processors. Deschamps JP, Valderrama E, Terés L. Springer 2017. ISBN 978-3-319-41198-9.

- Complex Digital Systems. Deschamps JP, Valderrama E, and Terés L. Springer 2019. ISBN 978-3-030-12652-0.
- Diseño de Sistemas Digitales. Deschamps JP, Ed. Paraninfo 1989. ISBN 84-283-1695-9.
- Digital Systems Fundamentals. T.L. Floyd. Ed. Prentice Hall. 9ª Edición ISBN: 8483220857.