Universitat Autònoma de Barcelona

2020/2021

Digital Systems and Hardware Description Languages

Code: 102684
ECTS Credits: 9

Degree	Type	Year	Semester
2500895 Electronic Engineering for Telecommunication	OB	2	1
2500898 Telecommunication Systems Engineering	OB	2	1

The proposed teaching and assessment methodology that appear in the guide may be subject to changes as a result of the restrictions to face-to-face class attendance imposed by the health authorities.

Contact

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Use of Languages

Principal working language: catalan (cat)
Some groups entirely in English: No
Some groups entirely in Catalan: Yes
Some groups entirely in Spanish: No

Teachers

Elena Valderrama Vallés
Josep Velasco González

Prerequisites

There are no prerequisites. However, it is recommended for students to have previously taken the courses "Fundamentals of Computing" and "Theory of Circuis and Electronics".

Objectives and Contextualisation

This is a basic training course, taught during the second academic year, first semester. Is the bridge between the courses "Theory of Circuits and Electronics" and "Fundamentals of Computing", in the first year, and "Computer Architecture and Peripherals", in the second year.

The objectives of this course are for students to understand the role of digital systems in the computer world, be capable of designing low-to-medium complexity digital systems using logic gates and reconfigurable devices, and understand that a computer is simply a digital system of a certain complexity. In the last part of the course, a simple computer is presented in order for the students to understand the concepts of process-unit, control-unit, instruction set, microinstructions, microorders and microprogramming.

Competences

Electronic Engineering for Telecommunication

- Develop personal work habits.
- Develop thinking habits.

- Learn new methods and technologies, building on basic technological knowledge, to be able to adapt to new situations.
- Work in a team.

Telecommunication Systems Engineering
- Develop personal work habits.
- Develop thinking habits.
- Learn new methods and technologies, building on basic technological knowledge, to be able to adapt to new situations.
- Work in a team.

Learning Outcomes

1. Analyse and design combinational and sequential, synchronous and asynchronous, microprocessor and integrated circuits.
2. Apply the basics of hardware device description languages.
3. Develop applications in real time.
4. Develop critical thinking and reasoning.
5. Develop independent learning strategies.
6. Develop systemic thinking.
7. Develop the capacity for analysis and synthesis.
8. Manage available time and resources.
9. Manage available time and resources. Work in an organised manner.
10. Use computer tools to research bibliographic resources or information on telecommunications and electronics.
11. Use the basics of software design, verification and validation in the description of hardware systems based on high level hardware description languages.
12. Work cooperatively.

Content

Block 1: Combinational Circuits (CC)

- Digital signals and digital systems. Description of digital systems.
- Electronic digital systems (EDS). MOS transistors. AND, OR and INV logical gates. Synthesis of EDS as a process of successive refinements.
- Combinational Circuits. Synthesis from a table I: ROM. Synthesis from a table II: logic gates.
- Boolean algebra. Truth tables.
- NAND, NOR, XOR, NXOR logical gates. 3-state buffers.
- Synthesis tools. Propagation time. Other logic blocks: multiplexers, decoders, AND-OR planes.
- Synthesis from algorithms.

Block 2: Sequential Circuits (SC)

- The need for sequential circuits. Some examples. States and synchronization. Synchronous sequential circuits.
- Explicit functional description of SCs. State transition graphs and tables.
- Basic components: Bistables. Flip flops and latches.
- Synthesis of SC from tables. Moore and Mealy machines. States encoding.
- Registers, counters and memories. Structure, types and most common uses.
- Finite state machines (FSM). Formal definition. Implementation. Propagation times.
- Hardware description languages: VHDL. Some examples of FSM description using VHDL.
- Sequential implementation of algorithms.
- Physical implementation of digital circuits. Field Programmable Gate Arrays (FPGA) and other implementation strategies.

Block 3: Process Unit-Control Unit (PU-CU) architecture and processors

- PU-CU architecture
- PU with multiplexers. PU with busses
- ROM based Control Unit with sequencers
- Basic structure of a microprocessor. Von Neumann architecture as an extended PU-CU architecture. Functional units and busses
- A basic machine-level instruction set. An example of machine code programming.
- Fetch, decoding and execution cycles
- Micro-orders and condition (status) signals. Microinstructions and microprograms
- Microprogrammed implementation of the Control Unit
- Relations between pure hardware, firmware, and high-level software languages

Methodology

Based in the guidelines set out by the Engineering School in the new context created by coronavirus, in-class teaching will be replaced by online teaching (TEAMS webinars) during the first semester of 2020-21 academic course. Webinar schedules will be those established for face-to face classes. On the first day of class (online), students will receive full details about how educational activities will be developed along the course.

This course is organized in 3 blocks. Blocks 1 and 2 are highly supported by a free-access Coursera MOOC developed by the own course lecturers. MOOC materials include videos presenting the theoretical and practical knowledges required to properly design digital systems, examples, self-assessment questionnaires, and a set of exercises having automatic correction of the answers. Students must watch the videos before attending online classes, since webinars will be devoted to address students' doubts and questions, and to the discussion of new cases proposed by the teachers. It is important to note that webinars will not be "conventional expository lectures", and that students will be asked to maintain a high level of interaction between them and with teachers.

There are no videos (by now) for block 3, but a complete set of written materials developed by the course teachers will be available. As in the previous case, students should read this material before attending classes.

Previous activities are complemented by laboratory practice where students design and simulate different parts of a simple processor which is finally implemented on a FPGA. To physically implement the circuits, a design environment for programmable logic devices (INTEL-ALTERA) is used. Students will become familiar with the concepts of schematic capture, functional simulation, temporal simulation, and the description of complex digital systems using hardware description languages (VHDL).

To ensure the compliance of the new health standards, it is foreseen that a part, or even the totally of laboratory sessions can be developed online.

Tutoring

There will be:

- Individual or in small group sessions, on request from students. They should contact the course staff, and a date will be set up at their and teacher' convenience.
- Open tutoring sessions proposed by the teaching staff. In this case, for the teachers can plan and carry out the tutoring properly, students should submit in advance, via a forum created for that purpose, those specific questions about concepts or exercises they want to be discussed during the tutoring session.

No tutorial will be carried out in the two days before the exam dates. During this period, the teaching staff will only answer queries via the corresponding forums.

The following transversal skills are addressed and assessed during the course:

T01.01 - Develop critical thinking and reasoning. T01.02 - Develop the capacity for analysis and synthesis. T01.04 - Develop systemic thinking. They are worked on in the face to face classes and assessed within the partial tests.

T02.02 - Develop independent learning strategies. T02.03 - Manage available time and resources. Work in an organised manner. Students must develop these skills by taking responsibility for viewing the videos before classes and doing the exercises autonomously. The viewing (and understanding) of the videosis assessed through Socrative questionnaires at the beginning of the classes. Both the questionnaires and the problems delivered are part of the final grade.

T03.01 - Work cooperatively. This skill is addressed and assessed in the laboratory practices, where students must work in groups of two.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Exercise-based classes	18	0.72	1, 6, 5, 7, 4, 9, 12
Face to face classes	26	1.04	1, 2, 7, 4, 10, 11
Laboratory practices	18	0.72	2, 5, 9, 12, 11
Type: Supervised			
Case study	18	0.72	5, 4, 9
Laboratory practice assignments	10	0.4	2, 6, 5, 7, 4, 8, 9, 12, 11
Type: Autonomous			
Autonomous work	39	1.56	5, 8, 9
Preparing and solving exercises	32	1.28	1, 2, 10, 11
Preparing laboratory sessions	30	1.2	9, 12
Videos viewing	18	0.72	5, 7, 4, 8, 9

Assessment

a) Assessment activities

Assessment will include:

1. Three individual partial tests (one test per block), carried out individually, face-to-face, in a controlled environment, and in written format. These partial tests assess the student's acquired knowledge and his/her capability to design efficient digital circuits and systems.
2. Exercises resolution: a set of on-line exercises, with automatic grading, must be delivered on previously scheduled dates.
3. Online webinars attendance, and the viewing of videos before attending the class will be assessed through eventual "5-minutes tests" that will be carried out within the webinar itself.
4. For each laboratory session, the attendance (in-class or online as determined), the lab-work preparation and the work carried out during the session will be assessed.
5. Let's note that, depending on the circumstances, and if deemed appropriate, it may be necessary to schedule a practical exam to complete the assessment.

b) Assessment procedure

The mark of the course by continued assessment (*CA*) is obtained from:

1. (activity 1) The mark obtained in the 3 partial tests (*PT1*, *PT2*, *PT3*),
2. (activities 2 and 3) the delivery of exercises, answer to questionnaires and class attendance (*Pb*),
3. (activity 4) the mark of the laboratory activities (*LT*), and

according to the formula: $CA = PT \cdot 0.5 + LT \cdot 0.3 + Pb \cdot 0.2$

where $PT = (PT1+PT2+PT3)/3$

To pass the course the following conditions must be met:

1. $CA \geq 5$
2. *PT1*, *PT2*, and *PT3* must be ≥ 4, and *PT* must be ≥ 5, and
3. *LT* must be ≥ 5

At the end of the course:

- If the mark obtained in *PT1*, *PT2*, or *PT3* (only one of them) is **<** 4, the student is encouraged to raise this mark by repeating the test scored under 4. To pass the course, the new mark obtained must be ≥ 4, and the new average of the three marks must be ≥ 5. The mark *PT* will be this new average.
- If a student has obtained a mark **<** 4 in two or more partial tests, he is encouraged to take a final test of the whole course curriculum. The mark *PT* will be the grade obtained in this test, which must be ≥ 5 to pass the course.

If *PT* **<** 5 or *LT* **<** 5 after retaking these new tests, the final score of the course will be the lowest number between *CA* and 4.5.

The following figure summarizes the possible situations for students having passed the laboratory practices (that is, $\boldsymbol{LT} \geq 5$)

c) Assessment activities: scheduling

Dates of the assessment tests and the submission of exercises are published in the Virtual Campus (VC) and may be subject to changes in programming due to unforeseen eventualities. Any modification will be reported through this platform.

It is important to bear in mind that no assessment activities will be permitted for any student at a different date or time to that established, unless for justified causes duly advised before the activity and with the lecturer's previous consent. In all other cases, if an activity has not been carried out, this cannot be re-assessed.

d) Grades review

Grades obtained by students in each test are published in the VC. Once the grades arepublished, students will be informed of the procedure to follow to review their exam. Students must request, through the VC, an exam review, and will receive a call with the day and time to do it through TEAMS.

Any student who does not follow this procedure, within the time frame established, may not request a new review.

e) Irregularities committed by the student, copy and plagiarism

Notwithstanding other disciplinary measures deemed appropriate, and in accordance with the academic regulations in force, assessment activities will receive a zero whenever a student commits academic irregularities that may alter such assessment. Assessment activities graded in this way and by this procedure will not be re-assessable. If passing the assessment activity or activities in question is required to pass the subject, the awarding of a zero for disciplinary measures will also entail a direct fail for the subject, with no opportunity to re-assess this in the same academic year.

Irregularities contemplated in this procedure include, among others:

- the total or partial copying of a test, practical exercise, report, or any other evaluation activity;
- allowing others to copy;
- presenting group work that has not been done entirely by the members of the group;
- presenting any materials prepared by a third part as one's own work, even if these materials are translations or adaptations, including work that is not original or exclusively that of the student;
- having communication devices such as mobile phones, smart watches, etc., accessible during theoretical-practical in-class assessment tests (individual exams).

f) Assessment of students who followed the subject last year but do not successfully passed it

Except for those who had committed some of the irregularities cited in the previous section, students who completed and passed the laboratory practices in the previous course but did not pass the course, may choose not to repeat them again during the current academic year. In that case, the laboratory practices grade (*LT*) will be 5, regardless of the grade reached the previous year.

The list of students who can choose this option will be published at the beginning of the course in the VC. If, anyway, the student wants to make the laboratory practices again, he/she must communicate it by mail to the course Coordinator.

If a student has committed irregularities (copies/plagiarism) in any evaluation activity in a previous call of the subject he will not have the right to have his practices validated (if he had approved them).

g) Special grades

- A "non-assessable" grade cannot be assigned to students who have participated in any of the individual partial tests or the final test.
- In order to reach the qualification "with Honours", the final grade must be $\geq$ 9.0. Because the number of students with this distinction cannot exceed 5% of the number of students enrolled in the course, this distinction will be awarded to whoever has the highest final grade.

To consult the academic regulations approved by the Governing Council of the UAB, please follow this link: *https://www.uab.cat/doc/TR_Normativa_Academica_Plans_Nous*

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
3 partial test and/or final test	50%	8	0.32	1, 2, 6, 5, 7, 4, 8, 9, 10, 11
Exercises delivering	20%	8	0.32	5, 7, 4, 8, 9
Laboratory practices	30%	0	0	1, 2, 3, 7, 4, 8, 9, 12, 11

Bibliography

- Coursera MOOC: https://www.coursera.org/learn/digital-systems
- Digital Systems: From Logic Gates to Processors. Deschamps JP, Valderrama E, Terés L. Springer 2017. ISBN 978-3-319-41198-9.
- Complex Digital Systems. Deschamps JP, Valderrama E, and Terés L. Springer 2019. ISBN 978-3-030-12652-0.
- Diseño de Sistemas Digitales. Deschamps JP, Ed. Paraninfo 1989. ISBN 84-283-1695-9 (in spanish).
- Digital Systems Fundamentals. T.L. Floyd. Ed. Prentice Hall. 9ª Edición ISBN: 8483220857.
- Desenvolupament del microprocessador LittleProc: des de la primera porta lògica fins a una plataforma reconfigurable. J. Saiz, A.Portero, R. Aragonès. Materials 234. Servei de Publicacions de la UAB; ISBN (paper format): 978-84-490-2700-0, ISBN (e-book): 978-84-490-2699-7 (in catalan. Book used for the preparation of the laboratory sessions).