Universitat Autònoma de Barcelona

2020/2021

Electronic Systems Design

Code: 102723
ECTS Credits: 6

Degree	Type	Year	Semester
2500895 Electronic Engineering for Telecommunication	OB	3	1

The proposed teaching and assessment methodology that appear in the guide may be subject to changes as a result of the restrictions to face-to-face class attendance imposed by the health authorities.

Contact

Name: Joan Oliver Malagelada
Email: Joan.Oliver@uab.cat

Use of Languages

Principal working language: catalan (cat)
Some groups entirely in English: No
Some groups entirely in Catalan: Yes
Some groups entirely in Spanish: No

Teachers

Joan Oliver Malagelada

External teachers

Vanessa Moreno

Prerequisites

It is recommended to have passed the subjects of the first year of programming and have taken Second Digital and VHDL Systems.

Objectives and Contextualisation

The main objective of the subject is to introduce the student in the design of mixed electronic systems:
- Learn the design and use of electronic systems on embedded system.
- Construction of mixed electronic systems with FPGA / PSoC
- Deepen the hardware description from high-level languages.

Competences

- Develop personal attitude.
- Develop personal work habits.
- Develop thinking habits.
- Learn new methods and technologies, building on basic technological knowledge, to be able to adapt to new situations.
- Resolve problems with initiative and creativity. Make decisions. Communicate and transmit knowledge, skills and abilities, in awareness of the ethical and professional responsibilities involved in a telecommunications engineers work.

- Work in a team.

Learning Outcomes

1. Adapt to multidisciplinary and international surroundings.
2. Assume and respect the role of the different members of a team, as well as the different levels of dependency in the team.
3. Build hardware / software interfaces based on complex platforms.
4. Construct, operate and manage systems for capture, transport, representation, processing, storage, management and presentation of multimedia information, in terms of electronic systems.
5. Develop curiosity and creativity.
6. Develop scientific thinking.
7. Develop the capacity for analysis and synthesis.
8. Exploit information and communication technology in observance of an engineers ethical and professional responsibilities.
9. Identify, manage and resolve conflicts.
10. Maintain a proactive and dynamic attitude with regard to ones own professional career, personal growth and continuing education. Have the will to overcome difficulties.
11. Manage available time and resources. Work in an organised manner.
12. Recognize hardware / software solutions for the implantation of electronic and telecommunication systems.
13. Work cooperatively.

Content

1. Introduction: embedded systems, programmable circuits, embedded systems.
2. FPGA's and PSoC. Cases of use.
3. Signal processing in FPGA / PSoC:
- Peripherals in SoCs (I): Signal acquisition techniques based on ADC and frequent level.
- Peripherals in SoCs (II): generic input / output ports, timers, LCDs and VGAs.
- Peripherals in SoCs (III): common communication protocols in SoC.
- Peripherals in SoCs (IV): digital filters.
6. Introduction to hardware description languages. VHDL.
7. Hardware / software decomposition. Considerations and techniques.

Methodology

Theory classes:

Blackboard presentations of the theoretical part of the syllabus of the subject. The basic knowledge of the subject and indications of how to complete and deepen in the contents are given.

Problem seminars:

The scientific and technical knowledge presented in the master classes is worked on. Problems are solved and case studies are discussed. Problems promote the ability to analyze and synthesize, critical reasoning, and train the student in problem solving.

The methodology followed in problems is as follows: complete exercises are delivered that must be solved. In class, a review is made of the doubts that have arisen.

Laboratory classes:

Laboratory classes are carried out during the course and serve to deepen the practical knowledge of the subject.

Although the internships will be individual, according to the lab it can be done in groups of 2 students.

In the lab classes the student will have to develop his own abilities thought of the matter and of work in group.

Notes due to Covid-19.

1. The current circumstances make it unpredictable to think about the normality with which teaching will take place during the first semester of the course.

Therefore, in almost total security, part of the teaching (perhaps all the subject) will have to be done in virtual mode.

2. On the other hand, the proposed teaching methodology and evaluation may be modified at any time depending on the attendance restrictions imposed by the teaching staff.

health authorities.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Master classes	26	1.04	3, 4, 7, 8, 12
Seminars	12	0.48	3, 4, 7, 12
Type: Supervised			
Laboratory classes	12	0.48	11, 10
Type: Autonomous			
Autonomous work	80	3.2	

Assessment

The evaluation of the subject is divided in:

Continuous evaluation:

1. 2 tests of continuous evaluation. Each test has a weight between 25% and 30% in the final grade of the subject. You must have a minimum grade of 3.5 to be able to do average in partial tests.

2. Laboratory activities. The weight in the total of the subject is 40%. It is indispensable to pass them to pass the subject. There is no established mechanism of recovery of practices.

3. The delivery of class problems (optional evaluation) can be up to 10% in the final grade.

Final examination:

There is a final evaluation test to retrieve the evaluation part (s) with continuous proof / s or to raise a note. In this last case, the final grade will be the one obtained in this last test.
In order to participate in the final test the student must have practices done and have participated at least in an evaluation test.

Considerations:

The dates of the partial exams are set at the beginning of the course, and there is no recovery date in case of non-attendance.
Any modification that must occur in this assessment forecast due to unforeseen circumstances will be communicated in an addictive way to the students using the communication medium established at the beginning of the course.

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Laboratori classes	40	12	0.48	1, 2, 5, 9, 10, 13
Theory	60	8	0.32	3, 4, 6, 7, 8, 11, 12

Bibliography

Main bibliography:
J.W. Valvano
Embedded Microcomputer Systems: Real Time Interfacing
Thomson
2011
S. Sjöholm, L. Lindh
VHDL for Designers
Prentice Hall
1997
Complementary bibliography:
D.G. Bailey.
Design for Embedded Image Processing on FPGAs.
John Wiley & Sons
2011
S.W. Smith.
The Scientist and Engineer Guide to Digital Signal Processing
California Technical Publishing, San Diego
1999