Universitat Autònoma de Barcelona

2020/2021

Hardaware/Software Integration

Code: 102794
ECTS Credits: 6

Degree	Type	Year	Semester
2502441 Computer Engineering	OB	3	2
2502441 Computer Engineering	OT	4	2

The proposed teaching and assessment methodology that appear in the guide may be subject to changes as a result of the restrictions to face-to-face class attendance imposed by the health authorities.

Contact

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Use of Languages

Principal working language: catalan (cat)
Some groups entirely in English: No
Some groups entirely in Catalan: Yes
Some groups entirely in Spanish: No

Teachers

Joaquín Saiz Alcaine
Raimon Casanova

Prerequisites

There is none, although it is recommended to have done the course of embedded systems of the first semester.

Objectives and Contextualisation

The objective of the course is to introduce the students in the design and synthesis of System-on-Chip (SoC). In particular, the specific objectives of the subject are:

- Learn the embedded system design methodology.
- Learn how to partition the design in the hardware part and the software part.
- Create interfaces and peripherals that are coupled to the system.
- Deepening in data process techniques on embedded systems.

Competences

Computer Engineering

- Acquire thinking habits.
- Capacity to design, develop, evaluate and ensure the accessibility, ergonomics, usability and security of computer systems, services and applications, as well as of the information that they manage.
- Have the capacity to design and build digital systems, including computers, microprocessor based systems and communication systems.

- Have the capacity to develop specific processors and embedded systems and to develop and optimise the software of said systems.
- Have the right personal attitude.
- Work in teams.

Learning Outcomes

1. Demonstrate a high capacity for abstraction.
2. Design and develop computer systems that fulfil the specifications of the system and the application, and in particular in reference to embedded and real time systems.
3. Design specific processors and embedded systems, meeting the specifications of the application.
4. Develop and optimise software on a system and application level to obtain the desired functionality.
5. Devise communication systems based on digital systems.
6. Manage information by critically incorporating the innovations of ones professional field, and analysing future trends.
7. Work cooperatively.

Content

1. Introduction to Hw-Sw integration.
2. FPGAs and programmable circuits.
3. Hardware programming languages: UML, VHDL / Verilog, SystemC.
4. Hw-Sw partitioning for embedded systems.
5. Modeling and hardware-software co-calculation.
6. Communication protocols in embedded systems.
7. Implications of partitioning Hw / Sw in consumption and energy.
8. Development of embedded software.
9. Multiprocessor embedded systems: MPSoC and NoC.
10. Verification of embedded systems.

Methodology

Theory classes:
Exhibitions on the board of the theoretical part of the syllabus of the course. They give the basic knowledge of the subject and indications of how to complete and deepen the contents.

Problem seminars:
The scientific and technical knowledge exposed in the master classes is worked on. Problems are solved and case studies are discussed. With the problems, the ability to analyze and synthesize, critical reasoning is promoted, and the student is trained in solving problems. The methodology followed to problems is the following: complete exercises are delivered that must be solved. In class a review of the doubts that have arisen and solved those that the students have had conflicts. In a problem session, a group is working to solve problems in the synthesis of the subject.

Laboratory practices:
The practices are carried out during the course and serve to deepen the practical knowledge of the subject. The students will work in groups of 2. In the practices, the student will have to develop their own habits of thought of the matter and work in a group.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			

Theory classes	26	1.04	5, 1, 4, 2, 3, 6
Type: Supervised			
Laboratory activities	12	0.48	1, 4, 2, 3, 6, 7
Seminars	12	0.48	4, 2, 3
Type: Autonomous			
Study	80	3.2	1, 6

Assessment

The evaluation of the course is broken down into the following items:

1. Evidence of continuous evaluation. The weight in the total of the course is 55%. It will be necessary to obtain a minimum mark of 4 to make a medium between continuous assessment tests and the notes of the rest of the activities.
2. Laboratory activities. The weight in the total of the subject is 35%. It is indispensable to approve them to pass the subject. There is no established mechanism of recovery of practices.
3. Evaluation of work. The weight in the total of the subject is 10%. It corresponds to work that the student will do during the course.

Evaluation considerations:

- It is considered non-evaluable for the course when there has been no continuous assessment test and no more than two practical sessions.
- In the case of not reaching the minimum required in any of the assessment activities, if the calculation of the final mark is equal to or greater than 4.5, a 4.5 note will be placed on the file.
- Granting a special honors qualification is a decision of the faculty responsible for the subject. The regulations of the UAB indicate that special honors qualification can only be awarded to students who have obtained a final mark of 9.00 or more. It can be granted up to 5% of special honors qualification of the total number of students enrolled.
- For repeaters, only the practices of the last course are validated if these were approved and the note will be 5.
- The continuous assessment tests will be carried out on the established dates and no exception will be made.
- There is a final evaluation test to recover the part of the suspended continuous assessment or to raise a note. In this last case, the final grade will be the one obtained in this last test.
- The dates of continuous evaluation and delivery of works will be published on the virtual campus and may be subject to changes of programming for reasons of adaptation to possible incidents.
- For each assessment activity, a place, date and time of the revision will be indicated in which the student will be able to review the activity with the teacher. In this context, claims can be made about the activity note, which will be evaluated by the teachers responsible for the subject. If the student does not submit to this review, this activity will not be reviewed later.
- Without prejudice to other disciplinary measures deemed appropriate, and in accordance with the current academic regulations, irregularities committed by a student that can lead to a variation of the qualification will be classified by zero (0). For example, plagiarizing, copying, copying, ..., an evaluation activity, will imply suspending this evaluation activity with zero (0). Assessment activities qualified in this way and by this procedure will not be recoverable. If it is necessary to pass any of these assessment activities to pass the subject, this subject will be suspended directly, without the opportunity to recover it in the same course.

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes

Exercises	10%	5	0.2	4, 2, 3
Laboratory activities	35%	10	0.4	4, 3, 7
Theory	55%	5	0.2	5, 1, 4, 2, 3, 6

Bibliography

- J.W.Valvano. Embedded Systems: Real-Time Operating Systems for Arm Cortex M Microcontrollers 2014.
- J.W.Valvano. Embedded Microcomputer Systems. Thomson edit, 2007
- M.Wolf. Computers as Components: Principles of Embedded Computing Systems Design. Third edition. Morgan Kaufmann Series. Elsevier, 2012
- S. Sjoholm, L. Lindh. VHDL for designers. Prentice Hall, 1997
- PSoC Designer User Guide. Cypress Semiconductor http://www.cypress.com
- P. Marwedel. Embedded System Design. Springer Verlag, 2006