Universitat Autònoma de Barcelona

2021/2022

Integrated System Design for Digital Processing

Code: 42839
ECTS Credits: 6

Degree	Type	Year	Semester
4313797 Telecommunications Engineering	OB	1	2

The proposed teaching and assessment methodology that appear in the guide may be subject to changes as a result of the restrictions to face-to-face class attendance imposed by the health authorities.

Contact

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Use of Languages

Principal working language: english (eng)

Teachers

Lluís Antoni Teres Teres

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Prerequisites

Knowledge on the following subjects is recommented:

Electronic Systems Design
Digital Sistemes and Hardware Description Languages
Electronic Systems and Applications
Computer Architecture

Objectives and Contextualisation

The main objective of this course is to learn, understand and be able to design electronic systems for digital processing with the focus on embedded systems. These Systems are composed of integrated circuits (or SoC from Systems on a chip) that manage their capacity of computation and communication through wired or wireless protocols. The study of these integrated systems will be oriented to the usual digital processing architectures in modern electronics: single-core (i.e. wireless sensor networks), multi-core (i.e. multimedia devices) and many core (high performance computing), and the different types of computation: data-flow and reactive. Different design methodologies will be used according the level of abstraction (physical, logic, architectural, system). Hardware Description Languages (HDL) and Virtual Components (IPs) will be introduced for SoC design. In order to implement such systems in the labs you will ues boards with FPGA reconfigurable devices.

Competences

- Be capable of using programmable logic as well as designing advanced electronic systems, both analogue and digital.
- Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
- Capacity for working in interdisciplinary teams
- Knowledge of the hardware description languages for highly complex circuits
- Maintain proactive and dynamic activity for continual improvement
- Students should be capable of integrating knowledge and facing the complexity of making judgements using information that may be incomplete or limited, including reflections on the social and ethical responsibilities linked to that knowledge and those judgements
- Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
- Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously

Learning Outcomes

1. Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
2. Capacity for working in interdisciplinary teams
3. Design ASICs
4. Design integrated circuits using hardware description languages through ASICs and/or FPGAs
5. Knowledge of the hardware description languages for highly complex circuits
6. Maintain proactive and dynamic activity for continual improvement
7. Students should be capable of integrating knowledge and facing the complexity of making judgements using information that may be incomplete or limited, including reflections on the social and ethical responsibilities linked to that knowledge and those judgements
8. Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
9. Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously
10. Use programmable digital logic.

Content

1. Introduction to the Design of Integrated Systems for Digital Processing
Fundamental Concepts on Ciber-Phyísical Systems
User Centered Design
Functional and Performmance Requirements
Global Microelectronics Ecosystem

2. Digital Integrated Systems Design: Concepts and Tools
Digital CMOS cell libraries and FPGA Components
Back-end EDA Tools, PCBs and Printed Electronics
Embedded Plataforms

3. Systems-on-a-Chip Design Methodologies
ASIC and FPGA Design Methodologies
HDL Modelling, simulation and synthesis
Virtual Components (IPs) and Patents

4. System Level Design
Models of Computation
Digital Processign Architectures
Example Cases

Methodology

The course will be mainly driven by the lectures, that will use adhoc material (presentations, documents, links and other resources) available in the virtual campus (VC) of the UAB.

Laboratory work will let the students to apply and experiment the concepts acquired on FPGA platforms widelly used in industry.

Students will deliver exercices on specific subjects (on the VC) and/or a scientific and/or technologic paper will be selected (according to the personal interests of every student) in order to get familiar and evaluate the knowledge that is available through specialized publications.

Two seminars are schedulled and others can also be added, according to the parallel activity at UAB, in order to analyse in depth specific topics.

Optionally, for students with previous knowledge in embedded systems and/or VHDL and/or FPGA we are proposing their participation in international challenges for embedded systems. That participation will replace the activities of laboratory and critical review.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Laboratory Sessions	15	0.6	1, 2, 5, 4, 6, 7, 8, 9, 10
Lectures	22	0.88	1, 5, 3, 4, 6, 7, 8, 10
Thematic Seminars	4	0.16	1, 3, 6, 7, 8, 9
Type: Supervised			
Thematic Homework (Individual)	14	0.56	1, 6, 7, 8, 9
Type: Autonomous			
Laboratory activities preparation and reporting	20	0.8	1, 2, 5, 4, 7, 8, 10
Study	69	2.76	1, 5, 3, 4, 6, 7, 8, 10

Assessment

The evaluation of the course will follow the rules of the continuous evaluation and the final grade for the course, is calculated with the proportions on the above table that contains:

• Parcial and Final exams containign both theoretical concepts and exercices. Minimum mark in the partial exam of 3,5 (over 10) is required to eliminate the evaluated content on the final exam.
• Individual work on the critical review of a specific scientific and/or technological paper.
• Team work at lab scheduled in 5 sessions with the need to deliver the corresponding reports (delivered

individually). This is mandatory to pass the course evaluation.
• The optionalparticipation in an international challenges from embedded systems companies will replace the activities of laboratory and critical review.

To obtain MH it will be necessary that the students have an overall qualification higher than 8.5 with the limitations of the UAB (1MH / 10students). As a reference criterion they will be assigned in descending order.

A final weighted average mark not lower than 50% is sufficient to pass the course, provided that a score over one third of the range is attained in everyone of the first 2 marks.

Plagiarism will not be tolerated. All students involved in a plagiarism activity will be failed automatically. A final mark no higher than 30% will be assigned.

An student not having achieved a sufficient final weighted average mark, may opt to apply for remedial activities the subject under the following conditions:
- the student must have participated in the problem-based learning laboratory activities, and
- the student must have a final weighted average higher than 30%, and
- the student must not have failed any activity due to plagiarism.

The student will receive a grade of "Not Evaluable" if:
- the student has not been able to be evaluated in the laboratory and learning-based activities due to not attendanceor notdeliver the corresponding reports without justified cause.
- the student has not carried out a minimum of 50% of the activities proposed in tutored sessions.
- the student has not taken the final exam.

Repeating students will be able to "save" their grade in lab and problem-based learning activities but not in the rest of the activities.

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Final Exam	20%	2	0.08	5, 3, 4, 7, 8, 10
Inidividual Exercises and/or review of a scientific paper	25%	1	0.04	1, 6, 7, 8, 9
Laboratory work reports	35%	1	0.04	2, 5, 4, 6, 7, 8, 9, 10
Parcial Exam	20%	2	0.08	5, 3, 4, 7, 8, 10

Bibliography

F. Balarin et al.: "Hardware-Software Co-Design of Embedded Systems: The POLIS Approach"
Rajsuman, Rochit ."System-on-a-Chip: Design and Test"
P. Bricaud, M. Keating : "Reuse Methodology Manual for System-On-A-Chip Designs"
L. Terés, Y. Torroja, S. Olcoz, E. Villar: "VHDL: Lenguaje estándar de diseño electrónico"
I. Grout "Digital Systems Design with FPGAs and CPLDs"
H.J.M. Veendrick "Nanometer CMOS: from ASICS to BASICS", 2ª edición, Springer. 2017.

http://www.europractice.com/
Example of international challenge http://www.innovatefpga.com/portal/

Software

The electronic design tools (EDA) associated with Intel-Altera FPGA boards used in laboratories that enable:
- Specification of digital systems in HDL languages
- Building SoC architectures for RISC processors (ARM, NIOS)

- Logical and physical synthesis of HDL
- Downloading HW and SW code from the PC to the FPGA

SoC-FPGA platforms will be used DE1_SoC for educational/industrial purposes.