Universitat Autònoma de Barcelona

2022/2023

Fundamentals of Computers

Code: 102765
ECTS Credits: 6

Degree	Type	Year	Semester
2502441 Computer Engineering	FB	1	2

Contact

Name: Mercedes Rullan Ayza
Email: mercedes.rullan@uab.cat

Use of Languages

Principal working language: catalan (cat)
Some groups entirely in English: No
Some groups entirely in Catalan: No
Some groups entirely in Spanish: No

Other comments on languages

The problems of group 411 are in spanish. The problems of group 412, 431,432,451,471 are in catalan.

Teachers

Jordi Carrabina Bordoll
Joaquín Saiz Alcaine
Lluís Antoni Teres Teres
Victor Montilla Gispert

Prerequisites

There are no prerequisites. However, it is recommended for students to have previously taken the courses "Fundamentals of Computing" and "Electricity and Electronics".

Objectives and Contextualisation

This is a basic training course, taught during the second semester of the first academic year. Computer Fundamentals is the bridge between the courses of Electricity and Electronics and Fundamentals of Computing, in the first year, and Computer Organization in the second year.

The objectives of this course are for students to understand the role of digital systems in the computer world, be capable of designing low-to-medium complexity digital systems using logic gates and reconfigurable devices, and understand that a computer is simply a digital system of a certain complexity.

In the last part of the course, methodologies based on "Process Unit - Control Unit (UP-UC)" architectures are addressed to solve digital systems of a certain complexity by introducing the basic concepts of these architectures both in their "wired" version (UC made with gates and logic blocks) and "microprogrammed" (UC based on ROM + sequencer). Finally a simple computer open source (RISC-V) is presented in order for the students to understand the concepts of process-unit, control-unit, instruction set, microinstructions, microorders and microprogramming and applying the previous UP-UC architectures.

Competences

- Acquire personal work habits.
- Acquire thinking habits.
- Know about the structure, organisation, operation and interconnection of computer systems, basic programming, and the application of the same to solve engineering problems.
- Know the basic materials and technologies to enable the learning and development of new methods and technologies, as well as those that that provide large-scale versatility to adapt to new situations.

Learning Outcomes

1. Demonstrate knowledge of machine operation algorithm and processor design based on this .
2. Develop a capacity for analysis, synthesis and prospection.
3. Know the basic principles of the structure and programming of computers.
4. Recognise and identify the methods, systems and technologies of computer engineering.
5. Show capacity for the design of basic components (logic ports, flip flops?) and for the design of combinational circuits and programmable logic devices.
6. Understand the basic principles of computer logic, Boolean functions and their minimisation.
7. Work independently.

Content

Block 1: Combinational Circuits (CC)

- Digital signals and digital systems. Description of digital systems. Electronic digital systems (EDS). MOS transistors. AND, OR and INV logical gates. Synthesis of EDS as a process of successive refinements.
- Combinational Circuits. Synthesis from a table I: ROM. Synthesis from a table II: logic gates.
- Boolean algebra. Truth tables.
- NAND, NOR, XOR, NXOR logical gates. 3-state buffers.
- Features: Propagation time. Hardware cost
- Other combinational blocks: multiplexers, decoders, AND-OR planes (PLAs).
- Synthesis tools: Synthesis from algorithms.

Block 2: Sequential Circuits (SC)

- The need for sequential circuits. Some examples. States and synchronization. Synchronous sequential circuits. Clock, reset and set.
- Explicit functional description of SCs. State transition graphs and tables.
- Basic components: Flip flops and latches.
- Synthesis of SC from tables. Moore and Mealy machines. States encoding.
- Registers, counters and memories. Structures, types and most common uses.
- Finite state machines (FSM). Formal definition. Implementation. Propagation times.
- Basic notions of VHDL. Some examples of FSM description using VHDL.
- Sequential implementation of algorithms.
- Physical implementation of digital circuits. Field Programmable Gate Arrays (FPGA) and other implementation strategies.

Block 3: Process Unit-Control Unit (PU-CU) architecture and processors

- PU-CU architecture.
- PU with multiplexers. PU with busses.
- ROM based Control Unit with sequencers.
- Basic structure of a microprocessor. Von Neumann architecture vs Harvard. Functional units and busses.
- Processor instruction set. Programming with machine language. Micro-orders and status signals.
- Example of open source processor: RISC-V

- Harvard architecture. Fetch, decoding and execution cycles.
- Microinstructions and microprograms.
- Microprogrammed implementation of the Control Unit.
- Relations between pure hardware, firmware, and software.

Methodology

The subject is organized in three blocks. Blocks 1 and 2 use a Coursera free access MOOC developed by the teachers of the subject. The materials offered through the MOOC include a series of videos that students must view before attending class and that contain the theoretical-practical knowledge needed for the design of digital systems, interactive self-correction exercises and a simulation environment of digital systems. Block 3 materials include a series of videos that are available through the UAB virtual campus. Block 3 uses the same work methodology indicated in the previous paragraph, without the Coursera environment.

The subject is taught in "classroom problems" mode. All face-to-face classes are treated as problem-based sessions. The classes are dedicated to solving questions and doubts in the videos, and cases proposed by the teacher. Students must actively participate in these classes; these are not conventional "theory" classes. They take place in small groups (of the order of 40-50 students), an indispensable condition to reach the necessary degree of interactivity in a subject of eminently practical character.

The course is completed with laboratory practices where students physically implement the circuits, which until then had been limited to design "on paper". Each session accommodates 20-25 students working in groups of 2 and lasts 2 hours.

Tutoring sessions may be individual or in small groups and will be done on demand and in coordination between each teacher and the related students. There may also be open tutoring sessions for all interested students that may be proposed by the teaching staff; but these will require prior submission to the corresponding forum of the Virtual Campus (CV) those specific questions about concepts or exercises that must be addressed in order for the teachers to plan and carry out that tutoring properly.

The following transversal skills are addressed and assessed during the course:

- T01.02 - Develop a capacity for analysis, synthesis and prospection: They are worked on in the face to face classes and assessed within the partial tests.
- T02.01 - Work independently: Students must develop these skills by taking responsibility for viewing the videos before classes and doing the exercises autonomously. The viewing (and understanding) of the videos is assessed through Moodle questionnaires at the beginning of the classes. Both the questionnaires and the problems delivered are part of the final grade.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Exercise-based classes	30	1.2	6, 3, 5, 1, 2, 4
Laboratory practices	12	0.48	5
Type: Supervised			
Case study	12	0.48	6, 5, 2, 7
Laboratory practice assignments	10	0.4	5

Type: Autonomous			
Autonomous work	40	1.6	6, 3, 5, 1, 4, 7
Preparing and solving exercises	16	0.64	2, 7
Videos viewing	12	0.48	6, 3, 5, 1, 2, 4, 7

Assessment

a) Assessment activities

Student assessment includes the following activities:

1. Three individual partial tests (one test per block) carried out face-to-face, in a controlled environment, and in written format. These partials tests assess the student's acquired knowledge and his/her skills designing efficient circuits and systems.
2. Exercises resolution: a set of on-line exercises, with automatic grading, must be delivered on previously scheduled dates.
3. The viewing of videos before attending the class and classroom attendance.
4. Activities in which students must demonstrate the skills acquired during the development of the practices.

The mark of the course by continued assessment (CA) is obtained from:

1. (activity 1) the mark obtained in the 3 partial tests (*PT1*, *PT2*, *PT3*),
2. (activities 2 and 3) the delivery of exercises, class attendance and video viewing (*Pb*),
3. (activity 4) the note of the evaluable activities of practices (*LT*)

according to the formula: $AC = PT \cdot 0{,}5 + Pb \cdot 0{,}2 + LT \cdot 0{,}3$

where: $PT = (PT1+PT2+PT3)/3$

To pass the course the following conditions must be met:

1. $\boldsymbol{CA} \geq 5$,
2. ***PT1***, ***PT2***, and ***PT3*** must be ≥ 4, and ***CA*** must be ≥ 5; and
3. ***LT*** must be ≥ 5

At the end of the course:

- If the mark obtained in *PT1*, *PT2*, or *PT3* (only one of them) is **<** 4, the student is encouraged to raise this mark by repeating the test scored under 4. To pass the course, the new mark obtained must be $\geq$ 4,and the new average of the three marks must be ≥ 5. The mark *PT* will be this new average.
- If a student has obtained a mark **<** 4 in two or more partial tests, he is encouraged to take a final test of the whole course curriculum. The mark *PT* will be the grade obtained in this test, which must be ≥ 5 to pass the course.
- If *LT* **<** 5 the student will be able to do a recovery activity related to the internship. The grade obtained in this recovery activity will be the new grade LT, which must be ≥ 5 to pass the subject.

If *PT* **<** 5 or *LT* **<** 5 after retaking these new tests, the final score of the course will be the lowest number between *CA* and 4.5.

The following figure summarizes the possible situations for students having passed the laboratory practices (that is, LT ≥ 5)

b) Assessment activities: scheduling

Dates of the assessment tests and the submission of exercises are published in the Virtual Campus (VC) and may be subject to changes in programming due to unforeseen eventualities. Any modification will be reported through this platform.

It is important to bear in mind that no assessment activities will be permitted for any student at a different date or time to that established, unless for justified causes duly advised before the activity and with the lecturer's previous consent. In all other cases, if an activity has not been carried out, this cannot be re-assessed.

c) Recovery process

The evaluation activity 1 corresponding to the theory can be recovered in the final test, following the conditions explained in section a. The student can present himself to the recovery as long as he has presented himself to 2 of the 3 partials of theory.

1) If the grade obtained in one (and only one) of the partial tests PP1, PP2 or PP3 is $<$ 4, this qualification must be passed by taking a recovery exam of the corresponding block. To pass the course the grade obtained in this exam must be $\geq$ 4, and the new average PP of the three partials must be $\geq$ 5.

2) If the grade obtained in two or more partials is $<$ 4, the student must take a new exam that will include the entire course. The grade obtained will be the new PP, which must be $\geq$ 5 to pass the course.

Activities 2 and 3 (delivery of exercises, class attendance and tests) which corresponds to 20% of the final grade cannot be recovered.

Activity 4 can be recovered, as indicated in section a, by carrying out a specific recovery activity related to the practices.

d) Grades review

Grades obtained by students in each test are published in the VC. Once the grades are published, students will be informed of the procedure to follow to review their exam. Students must request, through the VC, an exam review, and will receive a call with the day and time to do it through TEAMS.

Any student who does not follow this procedure, within the time frame established, may not request a new review.

e) Special grades

- A "non-assessable" grade cannot be assigned to students who have participated in any of the individual partial tests or practices.
- In order to reach the qualification "with Honours", the final grade must be $\geq$ 9.0. Because the number of students with this distinction cannot exceed 5% of the number of students enrolled in the course, this distinction will be awarded to whoever has the highest final grade.

f)Irregularities committed by the student, copy and plagiarism

Notwithstanding other disciplinary measures deemed appropriate, and in accordance with the academic regulations in force, assessment activities will receive a zero whenever a student commits academic irregularities that may alter such assessment. Assessment activities graded in this way and by this procedure will not be re-assessable. If passing the assessment activity or activities in question is required to pass the subject, the awarding of a zero for disciplinary measures will also entail a direct fail for the subject, with no opportunity to re-assess this in the same academic year.

Irregularities contemplated in this procedure include, among others:

- the total or partial copying of a test, practical exercise, report, or any other evaluation activity;
- allowing others to copy;
- presenting group work that has not been done entirely by the members of the group;
- presenting any materials prepared by a third part as one's own work, even if these materials are translations or adaptations, including work that is not original or exclusively that of the student;

- having communication devices such as mobile phones, smart watches, etc., accessible during theoretical-practical in-class assessment tests (individual exams).
- talk to peers during individual theoretical-practical assessment tests (exams);
- copy or attempt to copy from other students during theoretical-practical assessment tests (exams); - use or attempt to use writings related to the subject during the performance of the theoretical-practical evaluation tests (exams), when these have not been explicitly allowed.

g) Assessment of students who followed the subject last year but do not successfully passed it

Students who completed and passed the laboratory practices in in one of the previous two years but did not pass the course, may choose not to repeat them again during the current academic year. In that case, the laboratory practices grade (*LT*) will be 5, regardless of the grade reached the previous year.

The list of students who can choose this option will be published at the beginning of the course in the VC. If, anyway, the student wants to make the laboratory practices again, he/she must communicate it by mail to the practice Coordinator.

If a student has committed irregularities (copies/plagiarism) in any evaluation activity in a previous call of the subject he will not have the right to have his practices validated (if he had approved them).

From the second matriculation and if the student has the approved practices and chooses to validate them, you can choose that the evaluation system is:

1. make the normal evaluation (continues + final recovery) established in the section "a) Process and programmed evaluation activities" where a 5 would be maintained to the practices (if you have passed them) but the grade of the exercises would not be maintained.
2. replace the continuous evaluation with a final exam (on the date of the third part) and take into account your grade of practices and exercises of the previous course (5 maximum in each case):

final grade = 0.5 * final test + 0.3 * grade of the practices of the previous course (a 5) + 0.2 * note previous course exercises (maximum a 5)

If the student fails he has a second chance in this alternative 2) which would be to do again a final exam of the whole subject on the dates of the final recovery, maintaining the same conditions for the practices and the exercices (maximum a 5)

To be eligible for this differentiated evaluation (2),repeating students must request it from the person responsible for the subject by email no later than 15 days after the start of classes.

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Assessable practice activities	30%	2	0.08	5, 2, 4, 7
Exercises delivering	20%	8	0.32	2, 7
Three partial tests and/or final test	50%	8	0.32	6, 3, 5, 1, 2, 4, 7

Bibliography

- Coursera MOOC: https://www.coursera.org/learn/digital-systems
- Digital Systems: From Logic Gates to Processors. Deschamps JP, Valderrama E, Terés L. Springer 2017. ISBN 978-3-319-41198-9.
- Complex Digital Systems. Deschamps JP, Valderrama E, and Terés L. Springer 2019. ISBN 978-3-030-12652-0.
- Diseño de Sistemas Digitales. Deschamps JP, Ed. Paraninfo 1989. ISBN 84-283-1695-9.

- Digital Systems Fundamentals. T.L. Floyd. Ed. Prentice Hall. 9ª Edición ISBN: 8483220857.
- Arquitecturas UP-UC: de los sistemas digitales a medida al processador de propósito general RISC-V. Valderrama E., Deschamps J-P., Rullàn M. y Terés, L. Notes of block-3 of the course.

Software

- Oracle VM VirtualBox
- Quartus II Web Edition