UAB
Universitat Autònoma de Barcelona

2022/2023

Integrated Heterogenous Systems Design

Code: 42838
ECTS Credits: 6

Degree	Type	Year	Semester
4313797 Telecommunication Engineering	OB	1	2

Contact

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Use of Languages

Principal working language: english (eng)

Other comments on languages

English language will be employed for teaching this course.

Prerequisites

In order to achieve the best understanding of syllabus contents, the following background is needed:

• Signal processing
• Circuit theory
• Electronic devices
• Analog CMOS circuits

Objectives and Contextualisation

The aim of this syllabus can be split into two goals:

• Introduction to the design of A/D and D/A data converters in CMOS technologies
• Hands-on experience on the design methodology and EDA tools for mixed-signal and full-custom integrated circuits.

Competences

- Be capable of using programmable logic as well as designing advanced electronic systems, both analogue and digital.
- Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
- Capacity for designing and manufacturing integrated circuits.
- Capacity for working in interdisciplinary teams
- Knowledge of the hardware description languages for highly complex circuits
- Maintain proactive and dynamic activity for continual improvement
- Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
- Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously

Learning Outcomes

1. Be capable of designing heterogeneous electronic systems
2. Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
3. Capacity for working in interdisciplinary teams
4. Design advanced electronic systems, both digital and analogue
5. Design analogue and mixed integrated circuits
6. Maintain proactive and dynamic activity for continual improvement
7. Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
8. Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously

Content

Chapter 1. Introduction to integrated heterogeneous systems
1.1. Evolution of CMOS technologies
1.2. Trends in analog and mixed IC design
1.3. A/D and D/A conversion principles
1.4. ADC and DAC figures of merit
1.5. Lab proposal: My Delta-Sigma ADC in 2.5um CMOS technology (CNM25)

Chapter 2. ADC architectures and CMOS circuits
2.1. ADC classification
2.2. Flash techniques
2.3. Sub-ranging, time-interleaving and pipelining techniques
2.4. Successive-approximation techniques
2.5. Integrating techniques
2.6. Delta-Sigma modulation techniques
2.7. Time-domain techniques

Chapter 3. DAC architectures and CMOS circuits
3.1. DAC classification
3.2. Flash techniques
3.3. Pulse-width modulation techniques
3.4. Delta-Sigma modulation techniques

Chapter 4. Full-Custom IC Design Methodology
4.1. Mixed-Signal Design Flow
4.2. AMS Hardware Description Languages
4.3. Device Sizing
4.4. Process and Mismatching Simulation
4.5. The Art of Analog Layout
4.6. Physical Verification
4.7. Parasitics Extraction
4.8. DFM Techniques

(Seminar about CNM25 design kit)

Chapter 5. CMOS OpAmps
5.1. OpAmp Figures of Merit
5.2. The Mono-Transistor Amplifier
5.3. Differential Circuits with CMFB
5.4. Folded Amplifiers

5.5. Cascode Topologies
5.6. Gain Enhancement Techniques
5.7. Multi-Stage OpAmps

Chapter 6. Delta-Sigma Modulators for ADC
6.1. Oversampling and noise shaping principles
6.2. Architecture selection based on quantization error
6.3. Switched-capacitor CMOS implementations
6.4. Modeling circuit second order effects
6.5. Digitally assisted techniques
6.6. Low-power circuit topologies

Chapter 7. Application to Low-Power Read-Out ICs for Smart Sensors
7.1. High-resolution SC Delta-Sigma ADC for space applications
7.2. Compact pixel integrating ADC for infrared and X-ray imagers
7.3. Potentiostatic CT Delta-Sigma ADC for electrochemical integrated sensors

Methodology

• Directed activities: lectures, case studies and exercises, lab sessions and seminars
• Supervised activities: tutorials
• Non-supervised activities: study, lab pre-work

Also, a 15-minute slot will be allocated in a lecture session to allow students filling the corresponding surveys for the evaluation of teaching quality.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Case studies and exercises	10	0.4	2, 1, 6, 7
Lab sessions	12	0.48	2, 3, 1, 6, 7
Lectures	23	0.92	1, 5, 4, 7
Type: Supervised			
Tutorials	15	0.6	2, 5, 4, 6
Type: Autonomous			
Lab pre-work	10	0.4	2, 3, 5, 4, 6, 7
Study	68	2.72	2, 1, 5, 4, 6, 7

Assessment

Progressive evaluation of the overall mark is based on the following weights:

• Two partial exams (25%+25%)

• Lab report (40%)
• Solved exercises (10%)

The above evaluation scheme is only applicable when marks for first and second items are greater or equal to 5/10.

If the combined mark for partial exams is less than 5/10, students can re-take a single exam (remedial exam) to recover that 50% of the overall mark.

Lab work (including sessions and report) is mandatory to pass evaluation and it can not be recovered.

Finally, students will be considered as absent (i.e. "No Presentat") if they do not attend lab sessions OR they are not present at the required exams.

Any change on the above evaluation method will be communicated in advance.

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Lab report	40%	4	0.16	2, 3, 1, 5, 4, 6, 7
Partial exam 1	25%	2	0.08	2, 1, 5, 4, 7, 8
Partial exam 2	25%	2	0.08	2, 1, 5, 4, 7, 8
Remedial exam (only when required)	50%	2	0.08	2, 1, 5, 4, 7
Solved exercises	10%	2	0.08	1, 5, 4, 7

Bibliography

Materials supplied during class sessions are almost self-explanatori. For a deeper understanding of both theoretical and practical contents, the following readings are recommended:

• R. van de Plassche, CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters, Kluwer Academic Publishers
• R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters, John Wiley & Sons
• V. Peluso, M. Steyaert and W. Sansen, Design of Low-Voltage and Low-Power CMOS Delta-Sigma A/D Converters, Kluwer Academic Publishers
• F. Medeiro, A. Pérez-Verdú and A. Rodríguez-Vázquez, Top-Down Design of High-Performance Sigma-Delta Modulators, Kluwer Academic Publishers
• T. Tuma and A. Burmen, Circuit Simulation with SPICE OPUS: Theory and Practice, Modeling and Simulation Science, Engineering and Technology, Birkhäuser Boston
• A. Hastings, The Art of Analog Layout, Pearson Prentice Hall

Software

Academic Process Design Kit: CNM25 Edition
http://www.cnm.es/users/pserra/apdk
Developed by the own teachers.