Universitat Autònoma de Barcelona

2023/2024

Digital Systems and Hardware Description Languages

Code: 102684
ECTS Credits: 9

Degree	Type	Year	Semester
2500895 Electronic Engineering for Telecommunication	OB	2	1
2500898 Telecommunication Systems Engineering	OB	2	1

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Teaching groups languages

You can check it through this link. To consult the language you will need to enter the CODE of the subject. Please note that this information is provisional until 30 November 2023.

Teachers

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Prerequisites

There are no prerequisites. However, it is recommended for students to have previously taken the courses "Fundamentals of Computing" and "Theory of Circuis and Electronics".

Objectives and Contextualisation

This is a basic training course, taught during the second academic year, first semester. Is the bridge between the courses "Theory of Circuits and Electronics" and "Fundamentals of Computing", in the first year, and "Computer Architecture and Peripherals", in the second year.

The objectives of this course are for students to understand the role of digital systems in the computer world, be capable of designing low-to-medium complexity digital systems using logic gates and reconfigurable devices, and understand that a computer is simply a digital system of a certain complexity.

In the last part of the course, methodologies based on "Process Unit - Control Unit (UP-UC)" architectures are addressed to solve digital systems of a certain complexity by introducing the basic concepts of these architectures both in their "wired" version (UC made with gates and logic blocks) and "microprogrammed" (UC

based on ROM + sequencer). Finally a simple computer open source (RISC-V) is presented in order for the students to understand the concepts of process-unit, control-unit, instruction set, microinstructions, microorders and microprogramming and applying the previous UP-UC architectures.

Competences

Electronic Engineering for Telecommunication

- Develop personal work habits.
- Develop thinking habits.
- Learn new methods and technologies, building on basic technological knowledge, to be able to adapt to new situations.
- Work in a team.

Telecommunication Systems Engineering

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- Develop thinking habits.
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Learning Outcomes

1. Analyse and design combinational and sequential, synchronous and asynchronous, microprocessor and integrated circuits.
2. Apply the basics of hardware device description languages.
3. Develop applications in real time.
4. Develop critical thinking and reasoning.
5. Develop independent learning strategies.
6. Develop systemic thinking.
7. Develop the capacity for analysis and synthesis.
8. Manage available time and resources.
9. Manage available time and resources. Work in an organised manner.
10. Use computer tools to research bibliographic resources or information on telecommunications and electronics.
11. Use the basics of software design, verification and validation in the description of hardware systems based on high level hardware description languages.
12. Work cooperatively.

Content

Block 1: Combinational Circuits (CC)

- Digital signals and digital systems. Description of digital systems. Electronic digital systems (EDS). MOS transistors. AND, OR and INV logical gates. Synthesis of EDS as a process of successive refinements.
- Combinational Circuits. Synthesis from a table I: ROM. Synthesis from a table II: logic gates.
- Boolean algebra. Truth tables.
- NAND, NOR, XOR, NXOR logical gates. 3-state buffers.
- Features: Propagation time. Hardware cost
- Other combinational blocks: multiplexers, decoders, AND-OR planes (PLAs).
- Synthesis tools: Synthesis from algorithms.

Block 2: Sequential Circuits (SC)

- The need for sequential circuits. Some examples. States and synchronization. Synchronous sequential circuits. Clock, reset and set.
- Explicit functional description of SCs. State transition graphs and tables.
- Basic components: Flip flops and latches.
- Synthesis of SC from tables. Moore and Mealy machines. States encoding.
- Registers, counters and memories. Structures, types and most common uses.
- Finite state machines (FSM). Formal definition. Implementation. Propagation times.
- Hardware description language: VHDL. Some examples of FSM description using VHDL.
- Sequential implementation of algorithms.
- Physical implementation of digital circuits. Field Programmable Gate Arrays (FPGA) and other implementation strategies.

Block 3: Process Unit-Control Unit (PU-CU) architecture and processors

- PU-CU architecture.
- PU with multiplexers. PU with busses.
- ROM based Control Unit with sequencers.
- Basic structure of a microprocessor. Von Neumann architecture vs Harvard. Functional units and busses.
- Processor instruction set. Programming with machine language. Micro-orders and status signals.
- Example of open source processor: RISC-V
- Harvard architecture. Fetch, decoding and execution cycles.
- Microinstructions and microprograms.
- Microprogrammed implementation of the Control Unit.
- Relations between hardware, firmware and software.

Methodology

The subject is organized in three blocks. Blocks 1 and 2 use a Coursera free access MOOC developed by the teachers of the subject. The materials offered through the MOOC include a series of videos that students must view before attending class and that contain the theoretical-practical knowledge needed for the design of digital systems, interactive self-correction exercises and a simulation environment. of digital systems. Block 3 materials include a series of videos that are available through the UAB virtual campus. Block 3 uses the same work methodology indicated in the previous paragraph, without the Coursera environment.

The subject is taught in "classroom problems" mode. All face-to-face classes are treated as problem-based sessions. The classes are dedicated to solving questions and doubts in the videos, and cases proposed by the teacher. Students must actively participate in these classes; these are not conventional "theory" classes. They take place in small groups (of the order of 40-50 students), an indispensable condition to reach the necessary degree of interactivity in a subject of eminently practical character.

Previous activities are complemented by laboratory practice where students design and simulate different parts of a simple processor which is finally implemented on a FPGA. To physically implement the circuits, a design environment for programmable logic devices (INTEL-ALTERA) is used. Students will become familiar with the concepts of schematic capture, functional simulation, temporal simulation, and the description of complex digital systems using hardware description languages (VHDL).

Depending on the evolution of the health situation that are established, the practices could be carried out partially or completely in a non-contact mode.

Tutoring sessions may be individual or in small groups and will be done on demand and in coordination between each teacher and the related students. There may also be open tutoring sessions for all interested students that may be proposed by the teaching staff; but these will require prior submission to the corresponding forum of the Virtual Campus (CV) those specific questions about concepts or exercises that must be addressed in order for the teachers to plan and carry out that tutoring properly.

The following transversal skills are addressed and assessed during the course:

- T01.01 - Develop critical thinking and reasoning. T01.02 - Develop the capacity for analysis and synthesis. T01.04 - Develop systemic thinking. They are worked on in the face to face classes and assessed within the partial tests.
- T02.02 - Develop independent learning strategies. T02.03 - Manage available time and resources. Work in an organized manner. Students must develop these skills by taking responsibility for viewing the videos before classes and doing the exercises autonomously. The viewing (and understanding) of the videos is assessed through questionnaires Moodle at the beginning of the classes. Both the questionnaires and the problems delivered are part of the final grade.
- T03.01 - Work cooperatively. This skill is addressed and assessed in the laboratory practices, where students must work in groups of two.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Exercise-based classes	18	0.72	1, 6, 5, 7, 4, 9, 12
Face to face classes	26	1.04	1, 2, 7, 4, 10, 11
Laboratory practices	18	0.72	2, 5, 9, 12, 11
Type: Supervised			
Case study	18	0.72	5, 4, 9
Laboratory practice assignments	10	0.4	2, 6, 5, 7, 4, 8, 9, 12, 11
Type: Autonomous			
Autonomous work	39	1.56	5, 8, 9
Preparing and solving exercises	32	1.28	1, 2, 10, 11
Preparing laboratory sessions	30	1.2	9, 12
Videos viewing	18	0.72	5, 7, 4, 8, 9

Assessment

This course does not include single assessment.

a) Assessment activities

Student assessment includes the following activities:

1. Three individual partial tests (one test per block) carried out face-to-face, in a controlled environment, and in written format. These partials tests assess the student's acquired knowledge and his/her skills designing efficient circuits and systems.

2. Exercises resolution: a set of on-line exercises, with automatic grading, must be delivered on previously scheduled dates.
3. The viewing of videos before attending the class and classroom attendance.
4. Activities in which students must demonstrate the skills acquired during the development of the practices.

The mark of the course by continued assessment (*CA*) is obtained from:

1. (activity 1) The mark obtained in the 3 partial tests (*PT1*, *PT2*, *PT3*),
2. (activities 2 and 3) the delivery of exercises, answer to questionnaires and class attendance (*Pb*),
3. (activity 4) the mark of the laboratory activities (*LT*), and

according to the formula: $CA = PT \cdot 0.5 + LT \cdot 0.3 + Pb \cdot 0.2$

where $PT = (PT1+PT2+PT3)/3$

To pass the course by continued assessment (*CA*) the following conditions must be met:

1. ***CA*** ≥ 5
2. ***PT1***, ***PT2***, and ***PT3*** must be ≥ 4, and ***PT*** must be ≥ 5, and
3. ***LT*** must be ≥ 5

b) Assessment activities: scheduling

Dates of the assessment tests and the submission of exercises are publishedin the Virtual Campus (VC) and may be subject to changes in programming due to unforeseen eventualities. Any modification will be reported through this platform.

It is important to bear in mind that no assessment activities will be permitted for any student at a different date or time to that established, unless for justified causes duly advised before the activity and with the lecturer's previous consent. In all other cases, if an activity has not been carried out, this cannot be re-assessed.

c) Recovery process

The evaluation activity 1 corresponding to the theory can be recovered in the final test. The student can present himself to the recovery as long as he has presented himself to 1 of the 3 partials of theory.

1. If the mark obtained in one or two of *PT1*, *PT2*, or *PT3* is **<** 4, the student is encouraged to raise this mark/s by repeating the test/s scored under 4. To pass the course, the new mark obtained must be ≥ 5 (it will be a global note of the two partials to recover), and the new average of the marks must be ≥ 5. The mark *PT* will be this new average.
2. If a student has obtained a mark **<** 4 in three partial tests, he is encouraged to take a final test of the whole course curriculum. The mark *PT* will be the grade obtained in this test, which must be ≥ 5 to pass the course.

If *PT* **<** 5 or *LT* **<** 5 after retaking these new tests, the final score of the course will be the lowest number between *CA* and 4.5.

Activities 2 and 3 (delivery of exercises, class attendance and tests) which corresponds to 20% of the final grade and activity 4 (laboratory practices) which corresponds to 30% of the final grade cannot be recovered.

d) Grades review

Grades obtained by students in each test are published in the VC. Once the grades are published, students will be informed of the procedure to follow to review their exam. Students must request, through the VC, an exam review, and will receive a call with the day and time to do it through TEAMS.

Any student who does not follow this procedure, within the time frame established, may not request a new review.

e) Special grades

- A "non-assessable" grade cannot be assigned to students who have participated in any of the individual partial tests or the final test.
- In order to reach the qualification "with Honors", the final grade must be $\geq$ 9.0. Because the number of students with this distinction cannot exceed 5% of the number of students enrolled in the course, this distinction will be awarded to whoever has the highest final grade.

f) Irregularities committed by the student, copy and plagiarism

Notwithstanding other disciplinary measures deemed appropriate, and in accordance with the academic regulations in force, assessment activities will receive a zero whenever a student commits academic irregularities that may alter such assessment. Assessment activities graded in this way and by this procedure will not be re-assessable. If passing the assessment activity or activities in question is required to pass the subject, the awarding of a zero for disciplinary measures will also entail a direct fail for the subject, with no opportunity to re-assess this in the same academic year.

Irregularities contemplated in this procedure include, among others:

- the total or partial copying of a test, practical exercise, report, or any other evaluation activity;
- allowing others to copy;
- presenting group work that has not been done entirely by the members of the group;
- unauthorized use of AI (eg Copilot, ChatGPT or equivalent) to solve exercises,practices and/or any other evaluable activity;
- presenting any materials prepared by a third part as one's own work, even ifthese materials are translations or adaptations, including work that is not original or exclusively that of the student;
- having communication devices such as mobile phones, smart watches, etc., accessible during theoretical-practical in-class assessment tests (individual exams).
- talk to peers during individual theoretical-practical assessment tests (exams);
- copy or attempt to copy from other students during theoretical-practical assessment tests (exams); - use or attempt to use writings related to the subject during the performance of the theoretical-practical evaluation tests (exams), when these have not been explicitly allowed.

g) Assessment of students who followed the subject last year but do not successfully passed it

Students who completed and passed the laboratory practices in the previous course but did not pass the course, may choose not to repeat them again during the current academic year. In that case, the laboratory practices grade (*LT*) will be 5, regardless of the grade reached the previous year.

The list of students who can choose this option will be published at the beginning of the course in the VC. If, anyway, the student wants to make the laboratory practices again, he/she must communicate it by mail to the practice Coordinator.

If a student has committed irregularities (copies/plagiarism) in any evaluation activity in a previous call of the subject he will not have the right to have his practices validated (if he had approved them).

From the second matriculation and if the student has the approved practices and choose to validate them, the student can choose that the evaluation system is:

1. make the normal evaluation (continues + final recovery) established in the section "a) Process and programmed evaluation activities" where a 5would be maintained to the practices but thegradeofthe exercises would not be maintained.
2. replace the continuous evaluationwith a final exam (on the date of the third part)and take into account your grade of practices and exercises of the previous course (5 maximum in each case):

final grade = 0.5 * final test + 0.3 * grade of the practices of the previous course (a 5) + 0.2 * note previous course exercises (maximum a 5)

If the student fails he has a second chance in this alternative 2) which would be to do again a final exam of the whole subject on the dates of the final recovery, maintaining the same conditions for practices and exercises (maximum a 5).

To be eligible for this differentiated evaluation (2),repeating students must request it from the person responsible for the subject by email no later than 15 days after the start of classes.

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
3 partial test and/or final test	50%	8	0.32	1, 2, 6, 5, 7, 4, 8, 9, 10, 11
Exercises delivering	20%	8	0.32	5, 7, 4, 8, 9
Laboratory practices	30%	0	0	1, 2, 3, 7, 4, 8, 9, 12, 11

Bibliography

- Coursera MOOC: https://www.coursera.org/learn/digital-systems
- Digital Systems: From Logic Gates to Processors. Deschamps JP, Valderrama E, Terés L. Springer 2017. ISBN 978-3-319-41198-9.
- Complex Digital Systems. Deschamps JP, Valderrama E, and Terés L. Springer 2019. ISBN 978-3-030-12652-0.
- Diseño de Sistemas Digitales. Deschamps JP, Ed. Paraninfo 1989. ISBN 84-283-1695-9 (in spanish).
- Digital Systems Fundamentals. T.L. Floyd. Ed. Prentice Hall. 9ª Edición ISBN: 8483220857.
- Arquitecturas UP-UC: de los sistemas digitales a medida al processador de propósito general RISC-V. Valderrama E., Deschamps J-P., Rullàn M. y Terés, L. Notes of block-3 of the course.
- Desenvolupament del microprocessador LittleProc: des de la primera porta lògica fins a una plataforma reconfigurable. J. Saiz, A.Portero, R. Aragonès. Materials 234. Servei de Publicacions de la UAB; ISBN (paper format): 978-84-490-2700-0, ISBN (e-book): 978-84-490-2699-7 (in catalan. Book used for the preparation of the laboratory sessions).

Software

In the laboratory session we will use the software Altera Quartus II 9.0 WebEdition. Students will be required to install this software, which does not require any license.