Universitat Autònoma de Barcelona

2023/2024

Electronic Devices

Code: 102721
ECTS Credits: 6

Degree	Type	Year	Semester
2500895 Electronic Engineering for Telecommunication	OT	4	0

Contact

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Teaching groups languages

You can check it through this link. To consult the language you will need to enter the CODE of the subject. Please note that this information is provisional until 30 November 2023.

Prerequisites

To know at a basic level:

a) Circuits theory.

b) Basics of electrostatics.

c) Mathematics.

d) Diodes and transistors fundamentals.

e) Fundamentals of the physics principles of semiconductors.

f) Fundamentals of circuit simulators.

Objectives and Contextualisation

The main objectives of this subject are:

a) To know the fundamentals of the basic microelectronics processes and their integration in CMOS technology.

b) To know the characteristics as an electronic device of the MOS transistor and their most important SPICE models.

c) To be able to relate the electric characteristics of the MOS transistor with their technological parameters of the corresponding CMOS technology.

d) To know roughly the current problems associated to the state of the microelectronics technology and the main trends of its evolution.

Competences

- Communication
- Design components and electronic circuits in accordance with specifications
- Develop personal attitude.
- Develop personal work habits.
- Develop thinking habits.

Learning Outcomes

1. Apply simulation techniques for performance analysis.
2. Design basic electronic devices, establishing the relationship with manufacturing technology.
3. Develop independent learning strategies.
4. Develop the capacity for analysis and synthesis.
5. Make one's own decisions.
6. Manage information by critically incorporating the innovations of one's professional field, and analysing future trends.
7. Use English as a language of communication and as the reference in professional relations.
8. Use circuit models of the electrical behaviour of electronic devices, including parasites and noise sources, and considering their limitations.

Content

PART I. Technological processes

Introduction: CMOS technology. Cleanrooms. Lithography

Silicon growth

Impurity diffusion

Ion implantation

Thermal oxidation. LOCOS process

Layer deposition. Epitaxial growth

Metallization

Etching

Back-End processes. Damascene

PART II. MOS transistor

Introduction to the physics of semiconductors and band theory

The MOS capacitance. Structure and polarization states

The MOS transistor. Structure and conduction states

SPICE model LEVEL 1

SPICE model LEVEL 2

SPICE model LEVEL 3

LABORATORY

Definition of a technological process

TMOS electrical characterization

Methodology

The learning process will be based on master classes and practical sessions in the laboratory and classroom.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Classroom problems	12	0.48	1, 4, 2, 5, 8
Laboratory sessions	12	0.48	1, 4, 2, 5, 8
Master classes	24	0.96	1, 4, 2, 6, 8
Type: Supervised			
Tutorship	5	0.2	3, 4, 6
Type: Autonomous			
Laboratory sessions preparation	8	0.32	1, 4, 2, 5, 7, 8
Problems resolution	25	1	1, 3, 4, 2, 5, 8
Study	40	1.6	3, 4, 6

Assessment

a) Process and programmed evaluation activities

The subject will be evaluated through the following activities:

- EP1: Partial Exam 1. Exam of part 1: Technological processes. It consists of a theory section and a problems section. 37.5% of FINAL MARK.

- EP2: Partial Exam 2. Exam of part 2: MOS transistor. It consists of a theory section and a problems section. 37.5% of FINAL MARK.

- LABINF: Laboratory sessions report. 25% of FINAL MARK.

The accomplishment of ALL these activities enables the continuous evaluation, as long as the mean mark over 10 obtained from the two exams is equal or higher than 4.5.

The activities with a second opportunity are:

EP1 and EP2, as indicated in section c).

The activities with NO second opportunity are:

LABINF.

To enable the evaluation of the LABINF activity it is necessary:

1) To attend ALL laboratory sessions (an absence proof will be required).

2) To submit the report before deadline.

SUMMARY:

EXAM MARK = EP1_MARK*0.5 + EP2_MARK*0.5

If EXAM MARK > 4.5 then:

FINAL MARK= EXAM MARK*0.75 + LABINF MARK*0.25

If EXAM MARK < 4.5 then:

FINAL MARK= EXAM MARK

ALL marks in the previous expression are considered over 10.

b) Evaluation activities programming

The calendar of the evaluation activities* will be published through the Moodle's classroom (CAMPUS VIRTUAL) during the firsts semester's weeks. In any case, it is foreknown that:

-EP1 will take place at mid semester: last week dedicated to Part 1 (just before or after Easter).

-EP2 will take place at the end of semester: last week dedicated to Part 2 (just before resit exams period).

-The laboratory report, LABINF, will be submitted not later the resit exam*, following the procedure indicated in the Moodle's classroom.

*The resit exams will be published in the Engineering School's webpage (exams part).

c) Retrieval process

According to UAB regulations, the student can only participate in the retrieval process as long as he has fulfilled a set of activities representing at least 2/3 of the final mark of the subject. In the case of the present subject, this condition is only fulfilled if the student attends both partial exams.

The only retrievable activities are the partial exams EP1 and EP2, by means of a FINAL RESIT EXAM.

This FINAL RESIT EXAM consists of 2 independent parts corresponding to Part 1 (Technological processes) and Part 2 (MOS transistor), each one of them with their own theory and problems sections (identical structure

as partial exams), so that it is possible to retrieve the mark of one single part or the mark of both parts. Thus, the mark of each part, FINAL_MARK1 and FINAL_MARK2, substitutes the mark of the corresponding partial exam, EP1_ MARK and EP2 MARK, as long as the first one overcomes the second one.

Therefore, the FINAL RESIT EXAM will NEVER lead to a mark lower than the obtained through the partial exams.

SUMMARY:

EXAM MARK = MAX(EP1_ MARK ; FINAL_MARK1)*0.5 + MAX(EP2_ MARK ; FINAL_MARK2)*0.5

If EXAM MARK > 4.5 then:

FINAL MARK= EXAM MARK*0.75 + LABINF MARK*0.25

If EXAM MARK < 4.5 then:

FINAL MARK= EXAM MARK

ALL marks in the previous expressionare considered over 10.

d) Marks review procedure

For each evaluation activity, it will be indicated (through Campus Virtual) place, date and time for the review with the teacher of the evaluation activity results. In this context, the student will be able to exhibit possible claims about the obtained mark, that will be analyzed by the teacher. In case the student does not attend the review, any other review activity will be scheduled later.

e) Marks

A student will be considered NOT EVALUABLE (NA) if one of the two following conditions is satisfied:

a) He/she does not attend at least one of the two partial exams EP1 or EP2.

b) He/she does not submit the laboratory report LABINF.

On the other hand, according to UAB regulations, among those students with a final mark over 9.0, a maximum number of Matrícules d'Honor (MH) corresponding to 5% (rounded by excess) of the total number of students can be granted. In case the number of students is below 20, 1 MH can be granted.

f) Student's irregularities, copy and plagiarism

Without detriment of other disciplinary measures, it will be graded with a zero all the irregularities committed by the student that could lead to a modification in the mark of an evaluation activity. Therefore, copying, plagiarizing, misleading, letting copy, etc. in any of the evaluation activities will imply to fail the activity with a zero.

g) Evaluation of repeating students

As from the second enrollment, the student may ask to validate the laboratory mark (LABINF MARK) obtained in a previous course. In this case, it is not necessary that the student to notifies this fact to the teacher in charge of the subject.

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Exam	75%	6	0.24	1, 3, 2, 6, 5, 7, 8

Laboratory sessions and corresponding report	25%	18	0.72	1, 4, 2, 5, 8

Bibliography

Bibliography PART 1. Technological processes

"Circuits i dispositius electrònics, fonaments d'electrònica". Lluís Prat et al. Edicions UPC

"Fundamentals of semiconductor fabrication", Gary S. May, Simon M. Sze . New York : Wiley, cop. 2004. ISBN: 0471232793.

"Semiconductor devices : physics and Technology", S. M. Sze. 2nd ed. New York : Wiley, cop. 2002. ISBN: 0471333727.

Bibliography PART 2. MOS transistor

"CMOS, circuit design, layout and simulation". R. Jacob Baker. Ed Wiley, 2010

"CMOS analog circuit design". Phillip E. Allen. Ed Oxford, 2002

"Principles of CMOS VLSI design". Neil H.E. Weste. Ed Adison, 1994

"Semiconductor fundamentals", Robert F. Pierret. Addison-Wesley 2nd ed. 1988. ISBN: 0201122952.

"Field effect devices", Robert F. Pierret. Addison-Wesley 2nd ed. 1990. ISBN: 0201122987.

"Semiconductor device modeling with SPICE", Giuseppe Massobrio and Paolo Antognetti, McGraw-Hill 2nd ed. 1993. ISBN: 0070024693.

Software

PSpice

ICECREM