Universitat Autònoma de Barcelona

2023/2024

Integrated System Design for Digital Processing

Code: 42839
ECTS Credits: 6

Degree	Type	Year	Semester
4313797 Telecommunication Engineering	OB	1	2

Contact

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Teaching groups languages

You can check it through this link. To consult the language you will need to enter the CODE of the subject.
Please note that this information is provisional until 30 November 2023.

Teachers

Raimon Casanova Mohr

David Castells Rufas

Marc Codina Barbera

Prerequisites

Knowledge on the following subjects is recommented:

Electronic Systems Design
Digital Sistemes and Hardware Description Languages
Electronic Systems and Applications
Computer Architecture

Objectives and Contextualisation

The main objective of this course is to learn, understand and be able to design electronic systems for digital processing with the focus on embedded systems. These Systems are composed of integrated circuits (or SoC from Systems on a chip) that manage their computation and communication. The study of these integrated systems will be oriented to the usual digital processing architectures in modern electronics: single-core (i.e. IoT wireless sensor networks), multi-core (i.e. multimedia devices) and many core (high performance computing), and the different types of computation: data-flow and reactive. Different design methodologies will be used according the level of abstraction (physical, logic, architectural, system). Hardware Description Languages (HDL) and Virtual Components (IPs) will be introduced for SoC design. In order to implement such systems in the labs you will ues boards with FPGA reconfigurable devices.

Competences

- Be capable of using programmable logic as well as designing advanced electronic systems, both analogue and digital.
- Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
- Capacity for working in interdisciplinary teams
- Knowledge of the hardware description languages for highly complex circuits
- Maintain proactive and dynamic activity for continual improvement
- Students should be capable of integrating knowledge and facing the complexity of making judgements using information that may be incomplete or limited, including reflections on the social and ethical responsibilities linked to that knowledge and those judgements
- Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
- Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously

Learning Outcomes

1. Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
2. Capacity for working in interdisciplinary teams
3. Design ASICs
4. Design integrated circuits using hardware description languages through ASICs and/or FPGAs
5. Knowledge of the hardware description languages for highly complex circuits
6. Maintain proactive and dynamic activity for continual improvement
7. Students should be capable of integrating knowledge and facing the complexity of making judgements using information that may be incomplete or limited, including reflections on the social and ethical responsibilities linked to that knowledge and those judgements
8. Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
9. Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously
10. Use programmable digital logic.

Content

1. Introduction to the Design of Integrated Systems for Digital Processing
Fundamental Concepts of the Internet of Things (IoT)
Clasification of Chips according to their Energy Efficiency
Functional and Performmance Requirements
Global Microelectronics Ecosystem

2. System Level Design
Components of the Ciber-Phyísical Systems
Real World Modelling
Simulation frameworks: Ptolemy
Models of Computation and digital implementations
Examples

3. Systems-on-a-Chip Design Methodologies
Microelectronic Design Methodologies for ASIC and FPGA
HDL Modelling, simulation and synthesis
Virtual Components (IPs) and Patents

4. Physical Chip Design
ASIC Process Design Kit (PDK): Digital CMOS cell libraries and FPGA Components
Back-end Electronic Design Automation (EDA) Tools
PCBs and Printed Electronics for Embedded Plataforms

Laboratory: Integrated Digital Processing on FPGA

Methodology

The course will be mainly driven by the lectures, that will use adhoc material (presentations, documents, links, tools and other resources) available in the virtual campus (VC) of the UAB.

Students will deliver exercices on specific subjects (on the VC) and a scientific and/or technologic paper will be selected (according to the personal interests of every student) in order to get familiar and evaluate the knowledge that is available through specialized publications.

Laboratory work will let the students to apply and experiment the concepts acquired on FPGA platforms widelly used in industry.

Two seminars are schedulled and others can also be added or skipped according to the activity at the classroom, in order to analyse in depth specific topics.

Optionally, for students with previous knowledge in embedded systems and/or VHDL and/or FPGA we are proposing their participation in international challenges for embedded systems. That participation will replace the laboratory activities.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Activities

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Laboratory Sessions	15	0.6	1, 2, 5, 4, 6, 7, 8, 9, 10
Lectures	22	0.88	1, 5, 3, 4, 6, 7, 8, 10
Thematic Seminars	4	0.16	1, 3, 6, 7, 8, 9
Type: Supervised			
Thematic Homework (Individual)	14	0.56	1, 6, 7, 8, 9
Type: Autonomous			
Laboratory activities preparation and reporting	20	0.8	1, 2, 5, 4, 7, 8, 10
Study	69	2.76	1, 5, 3, 4, 6, 7, 8, 10

Assessment

The course is structured in 2 parts assessed using different procedures: The first part corresponds to subjects 1, 2 and 3 and the second part to subject 4.

Student assessment uses continuous evaluation made up of two partial assessments:

• A partial exam for the first part of the course, corresponding to 2/3 parts tought in the classroom, which gives 33% of the final grade
• Individual work in thematic exercises (delivered on the virtual campus) for the second part of the subject, which accounts for 17% of the final grade

The final exam allows students to assess the achievement of skills in a single exam or to recover any partial assessments that had a mark lower than 3.5. Thak is also the minimum mark requered for any of the parts to pass the course if the average mark of the exam is not below 5.

Additionally, the final grade has two additional contributions:
• Team work in the laboratory, scheduled in 5 sessions, with the obligation to deliver the corresponding individual reports. An evaluation above 5 is mandatory to pass the course. This activity contributes 33% to the final grade of the course.
• Individual work in thematic exercises of the first part of the course and the critical review of a scientific-technological article in the second one. This activity contributes 17% to the final grade of the course. Participation in an international competition of embedded systems companies will replace laboratory activities.

A weighted final grade of not lower than 5 is required to pass the course.

In order to obtain MH, students will need to have an overall qualification higher than 8.5 with the limitations of the UAB (1 MH/10 students). As a reference criterion, they will be assigned in descending order.

Plagiarism will not be tolerated either in exams or in individual activities on the Virtual Campus. In this case, the available tools will be used to verify it. All students involved in plagiarism will be automatically suspended. A final grade of no more than 30% will be assigned.

The student will receive a grade of "Not Evaluable" if:
- the student has not been able to be evaluated in the laboratory due to not attendance or not deliver the corresponding reports without justified cause.
- the student has not carried out a minimum of 50% of the activities proposed.
- the student has not taken the final exam.

Repeating students will be able to "save" their grade in lab and problem-based learning activities but not in the rest of the activities.

Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Inidividual Exercises (part 1) and review of a scientific paper (part 2)	15%	1	0.04	1, 6, 7, 8, 9
Laboratory work reports	35%	1	0.04	1, 2, 5, 4, 6, 7, 8, 9, 10
Partial Evaluación (Part 1): Exam	33%	2	0.08	5, 3, 4, 7, 8, 9, 10
Partial Evaluación (Part 2): individual Exercises	17%	2	0.08	1, 3, 6, 9

Bibliography

Main references:

Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, MIT Press, ISBN 978-0-262-53381-2, 2017.
Available at https://ptolemy.berkeley.edu/books/leeseshia/releases/LeeSeshia_DigitalV1_08.pdf

Maribel Fernandez, Models of Computation: An Introduction to Computability Theory, Springer, ISBN 978-1-84882-433-1, 2009.

Vaibbhav Taraate , Digital logic design using Verilog : coding and RTL synthesis, Springer, ISBN 978-981-16-3198-6, 2022
Available at on-line thrrough your UAB account https://bibcercador.uab.cat/

H.J.M. Veendrick "Nanometer CMOS: from ASICS to BASICS", 2ª edición, Springer. 2017.
Available at on-line thrrough your UAB account https://bibcercador.uab.cat/

Additional References:

F. Balarin et al.: "Hardware-Software Co-Design of Embedded Systems: The POLIS Approach"

Rajsuman, Rochit ."System-on-a-Chip: Design and Test"

P. Bricaud, M. Keating : "Reuse Methodology Manual for System-On-A-Chip Designs"

I. Grout "Digital Systems Design with FPGAs and CPLDs"

Access to technologies and microlectronic design tools in Europa:
http://www.europractice.com/

Example of international challenge
http://www.innovatefpga.com/portal/
https://www.openhw.eu/

Software

The electronic design tools (EDA) associated with Intel-Altera FPGA boards used in laboratories that enable:
- Specification of digital systems in HDL languages
- Building SoC architectures for RISC processors (ARM, NIOS)
- Logical and physical synthesis of HDL
- Downloading HW and SW code from the PC to the FPGA
- Execution of the algorithm in the FPGA

Intel Altera's DE1_SoC board will be used as the SoC-FPGA platform.

Students will have free access, upon request, to courses on industrial EDA tools (CADENCE) useful for their curriculum and training, mainly for subjects 3 and 4.
https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/training/learning-maps.pdf