Microelectronics Design

Code: 102720
ECTS Credits: 6

2024/2025

Degree	Type	Year
2500895 Electronic Engineering for Telecommunication	OT	4

Contact

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Teachers

Maria Aranzazu Uranga del Monte

Teaching groups languages

You can view this information at the end of this document.

Prerequisites

To face up this subject in the best conditions it is convenient to have a previous knowledge of circuit resolution, equivalent models of large and small signal and general knowledge of electronic, both analog and digital.

Objectives and Contextualisation

To have a general view of the microelectronic design problem.

To know the stages of the design of an integrated circuit, distinguishing those that correspond specifically to the designer and those that correspond to the technologist.

To know the strategies and design stages, together with the CAD tools used, as well as the different alternatives or design styles.

To understand the operation of general-purpose analog and digital circuits.

Competences

- Communication
- Design components and electronic circuits in accordance with specifications
- Develop personal attitude.
- Develop personal work habits.

- Develop thinking habits.

Learning Outcomes

1. Apply simulation techniques for performance analysis.
2. Apply the basic techniques of integrated systems and circuit testing.
3. Design basic analogue and digital integrated circuits based on specifications of cost, size, power consumption and reliability and applying specific programming techniques.
4. Develop independent learning strategies.
5. Develop the capacity for analysis and synthesis.
6. Make one's own decisions.
7. Manage information by critically incorporating the innovations of one's professional field, and analysing future trends.
8. Use English as a language of communication and as the reference in professional relations.

Content

UNIT 1. Introduction to microelectronic design

1.1 Evolution of microelectronics

1.2 Basic concepts of microelectronic design

1.3 Design flow

UNIT 2. Fundamentals of the MOS transistor in microelectronic design

2.1 MOSFET Physical structure

2.2 MOSFET Model

2.3 CMOS design parameters

2.4 CMOS technological scaling

2.5 Design of passive elements: resistors, capacitors

UNIT 3: Analog microelectronic design

3.1 Active resistors

3.2 Current sources. Current mirrors.

3.3 Basic inverting amplifiers. Cascode configuration.

3.4 Differential stage.

3.5 The operational amplifier

UNIT 4. Digital microelectronic design

4.1 MOSFET model for digital design

4.2 The inverter: DC characteristic, commutation characteristic and layout

4.3 Full custom design of CMOS gates

Activities and Methodology

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
problem solving sessions	12	0.48	5, 6
theory classes	24	0.96	1, 2, 3, 5
Type: Supervised			
lab sessions	12	0.48	3, 5
Type: Autonomous			
Individual study	52	2.08	1, 2, 3, 4
Report on practical work (lab work)	12	0.48	5, 6
Search of information	12	0.48	5, 6, 7, 8
problem resolution	20	0.8	3, 4, 5, 6

During the semester, theory lessons and exercises will be held in the classroom. Theory lessons will present the scientific-technical knowledge of the subject in a structured, clear and ordered manner. The students will learn the basics with instructions on how to complete and deepen these contents. During the exercises, in small groups, students will have to solve problems related to the subject exposed in the master classes, with the teacher's support. The objective is to complete and deepen the understanding of the contents of the subject.

A total of 4 sessions of laboratory sessions, of compulsory attendance will be planned. The objective of the lab sessions is to promote active student learning by working on the implementation and design of basic circuits, as well as developing critical reasoning and teamwork competencies.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Assessment

Continous Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Report on practical work (lab work)	30%	2	0.08	1, 2, 4
Specific written and/or oral presentation of a digital design	20%	1	0.04	1, 2, 3, 4, 5, 6, 7, 8
Specific written and/or oral presentation of an analog design	50%	3	0.12	1, 2, 3, 4, 5, 6, 7, 8

Continuous evaluation process:

The evaluation of the subject will be carried out continuously through two types of clearly differentiated activities: lab sessions and homework

1. Lab sessions:

The attendance to the lab sessions and the delivery of the corresponding reports are indispensable condition to pass the subject.

The mark corresponding to the laboratory sessions has a weight of 30% of the final grade, and a minimum score of 5 is required so that they can be considered for the evaluation of the subject.

A mark smaller than 5 in the lab sessions implies the student wlll fail the complete subject.

2. Works proposed by the teacher:

Two written reports and / or oral presentation will be proposed by the teacher, corresponding to an analog and digital design respectivaly. The work must be done individually.

Students who have failed some of the works must submit to a final synthesis exam and take the exam of all the material not approved. A minimum final mark of 5 points will be required to average with the rest of the marks obtained by the student.

Recovery process: final exam

The final synthesis exam will consist of two parts, corresponding to each half of the subject. In order to be evaluated, the student must have a lab mark equal to or greater than 5, must have previously delivered the corresponding analog design activity and must have been evaluated with a grade higher than 2.5 out of 10.

Students can also attend to the final exam, even if they have passed, to improve the final qualification. In these cases the students renounce to the previous mark. A final minimum mark of 4 points will be required in the synthesis test to be computed with the rest of the marks.

In accordance with the current academic regulations, irregularities committed by a student that can lead to a variation of the qualification will be evaluated with a zero (0). For example, plagiarizing or copying an evaluation activity, will imply a zeromark in the activity. Assessment activities qualified in this way will not be recoverable. If it is necessary to pass any of these assessment activities, the student will fail this subject, without opportunity to recover it in the same course

Special qualifications

Only if the student does not present the lab report ofor homework, the note will be Non-Valuable. Otherwise, the final qualification will be calculated based on the weight of each evaluation activity.

For each subject , the number of Honors qualifications results from calculating the five percent or fraction of the students enrolled inall the teaching groups. Students will only be awarded if they have obtained a final mark equal to or greater than 9.00, and whenever the teacher considers it appropriate(depending on the student's excellence).

Bibliography

- R.J.Baker, H.W. Li, D.E. Boyce. *CMOS: circuit design, layout, and simulation*. IEEE Press Series on Microelectronic Systems. 2019
- P.E. Allen, D.R. Holberg. *CMOS analog circuit design*. HRW Series in Electrical and Computer Engineering.
- B. Razavi. *Design of analog CMOS integrated circuits*. McGraw-Hill. 2006
- F. Maloberti,*Analog Design for CMOS VLSI Systems,* Kluwer Academic Publishers

Software

Cadence (IC package)

Language list

Name	Group	Language	Semester	Turn
(PAUL) Classroom practices	321	Catalan	first semester	morning-mixed
(PLAB) Practical laboratories	321	Catalan	first semester	morning-mixed
(PLAB) Practical laboratories	322	Catalan	first semester	morning-mixed
(TE) Theory	320	Spanish	first semester	morning-mixed