UAB
Universitat Autònoma de Barcelona

Electronic Systems Design

Code: 102723
ECTS Credits: 6

2024/2025

Degree	Type	Year
2500895 Electronic Engineering for Telecommunication	OB	3

Contact

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Teachers

(External) Vanessa Moreno Font

Teaching groups languages

You can view this information at the end of this document.

Prerequisites

It is recommended to have passed the subjects of the first year of programming and have taken Second Digital and VHDL Systems.

Objectives and Contextualisation

The main objective of the subject is to introduce the student in the design of mixed electronic systems:
- Learn the design and use of electronic systems on embedded system.
- Construction of mixed electronic systems with FPGA / PSoC
- Introduction to the hardware description from high-level languages.

Competences

- Develop personal attitude.
- Develop personal work habits.
- Develop thinking habits.
- Learn new methods and technologies, building on basic technological knowledge, to be able to adapt to new situations.
- Resolve problems with initiative and creativity. Make decisions. Communicate and transmit knowledge, skills and abilities, in awareness of the ethical and professional responsibilities involved in a telecommunications engineer's work.
- Work in a team.

Learning Outcomes

1. Adapt to multidisciplinary and international surroundings.
2. Assume and respect the role of the different members of a team, as well as the different levels of dependency in the team.
3. Build hardware / software interfaces based on complex platforms.
4. Construct, operate and manage systems for capture, transport, representation, processing, storage, management and presentation of multimedia information, in terms of electronic systems.
5. Develop curiosity and creativity.
6. Develop scientific thinking.
7. Develop the capacity for analysis and synthesis.
8. Exploit information and communication technology in observance of an engineer's ethical and professional responsibilities.
9. Identify, manage and resolve conflicts.
10. Maintain a proactive and dynamic attitude with regard to one's own professional career, personal growth and continuing education. Have the will to overcome difficulties.
11. Manage available time and resources. Work in an organised manner.
12. Recognize hardware / software solutions for the implantation of electronic and telecommunication systems.
13. Work cooperatively.

Content

1. Introduction: embedded systems, programmable circuits, embedded systems.

2. FPGA's and PSoC. Architectures and applications.

3. Interface with the real world. Sensors and actuators

4. Peripherals in SoCs:

- ADC-based signal acquisition architectures.

- Input / output ports.

- Usual communication protocols in SoC.

- Digital filters.

5. Hardware description languages for creating components.

- Verilog

6. Hardware / software decomposition. Considerations and techniques.

7. SoC operating system

Activities and Methodology

Title	Hours	ECTS	Learning Outcomes
Type: Directed			

Master classes	26	1.04	3, 4, 7, 8, 12
Seminars	12	0.48	3, 4, 7, 12
Type: Supervised			
Laboratory classes	12	0.48	10, 11
Type: Autonomous			
Autonomous work	80	3.2	

Theory classes:

Blackboard presentations of the theoretical part of the syllabus of the subject. The basic knowledge of the subject and indications of how to complete and deepen in the contents are given.

Problem seminars:

The scientific and technical knowledge presented in the master classes is worked on. Problems are solved and case studies are discussed. Problems promote the ability to analyze and synthesize, critical reasoning, and train the student in problem solving.

The methodology followed in problems is as follows: complete exercises are delivered that must be solved. In class, a review is made of the doubts that have arisen.

Laboratory classes:

Laboratory classes are carried out during the course and serve to deepen the practical knowledge of the subject.

Although the internships will be individual, according to the lab it can be done in groups of 2 students.

In the lab classes the student will have to develop his own abilities thought of the matter and of work in group.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Assessment

Continous Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Laboratori classes	40	12	0.48	1, 2, 5, 9, 10, 13
Theory	60	8	0.32	3, 4, 6, 7, 8, 11, 12

The evaluation of the subject is divided in:

Continuous evaluation:

1. Continuous assessment tests. Continuous assessment tests weigh between 55% and 60% in the final grade of the subject. The tests, among them, have the same weight. You must have a minimum grade of 3.5 to be able to average in partial tests.

2. Laboratory activities. The weight in the total of the subject is between 35% and 40%. It is mandatory to pass the laboratory practices to pass the subject. There is no established mechanism of recovery of practices.

3. Carrying out exercises and other activities in class (optional assessment) can account for 10% of the final grade.

Final examination:

There is a final evaluation test to retrieve the evaluation part (s) with continuous proof / s or to raise a note. In this last case, the final grade will be the one obtained in this last test.

Considerations:

The dates of the partial exams are set at the beginning of the course, and there is no recovery date in case of non-attendance.
Any modification that must occur in this evaluation schedule due to unforeseen circumstances will be communicated in an appropriate manner using the communication mean established at the beginning of the course.

Bibliography

Main bibliography:
J.W. Valvano
Embedded Microcomputer Systems: Real Time Interfacing
Thomson
2011
S. Brown, Z. Vranezic
Fundamentals of Digital Logic with Verilog Design
McGraw-Hill
2014
Complementary bibliography:
D.G. Bailey.
Design for Embedded Image Processing on FPGAs.
John Wiley & Sons
2011
S.W. Smith.
The Scientist and Engineer Guide to Digital Signal Processing
California Technical Publishing, San Diego
1999
V. Taraate
Digital Logic Design Using Verilog
Springer India
2016

Software

The PSoC Creator development environment (Cypress) is used for internships.

Modelsim (Intel) is used for modeling and simulation with Verilog

Language list

Name	Group	Language	Semester	Turn
(PAUL) Classroom practices	321	Catalan	first semester	morning-mixed
(PLAB) Practical laboratories	321	Catalan	first semester	morning-mixed
(PLAB) Practical laboratories	322	Catalan	first semester	morning-mixed
(TE) Theory	320	Catalan	first semester	morning-mixed