Electronic Systems Design

Code: 102723
ECTS Credits: 6

2025/2026

Degree	Type	Year
Electronic Engineering for Telecommunication	OB	3

Contact

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Teachers

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Teaching groups languages

You can view this information at the end of this document.

Prerequisites

It is recommended to have passed the subjects of the first year of programming and have taken Second Digital and VHDL Systems.

Objectives and Contextualisation

The main objective of the subject is to introduce the student in the design of mixed electronic systems:
- Learn the design and use of electronic systems on embedded system.
- Construction of mixed electronic systems with FPGA / PSoC
- Introduction to the hardware description from high-level languages.

Competences

- Develop personal attitude.
- Develop personal work habits.
- Develop thinking habits.
- Learn new methods and technologies, building on basic technological knowledge, to be able to adapt to new situations.
- Resolve problems with initiative and creativity. Make decisions. Communicate and transmit knowledge, skills and abilities, in awareness of the ethical and professional responsibilities involved in a telecommunications engineer's work.
- Work in a team.

Learning Outcomes

1. Adapt to multidisciplinary and international surroundings.
2. Assume and respect the role of the different members of a team, as well as the different levels of dependency in the team.
3. Build hardware / software interfaces based on complex platforms.
4. Construct, operate and manage systems for capture, transport, representation, processing, storage, management and presentation of multimedia information, in terms of electronic systems.
5. Develop curiosity and creativity.
6. Develop scientific thinking.
7. Develop the capacity for analysis and synthesis.
8. Exploit information and communication technology in observance of an engineer's ethical and professional responsibilities.
9. Identify, manage and resolve conflicts.
10. Maintain a proactive and dynamic attitude with regard to one's own professional career, personal growth and continuing education. Have the will to overcome difficulties.
11. Manage available time and resources. Work in an organised manner.
12. Recognize hardware / software solutions for the implantation of electronic and telecommunication systems.
13. Work cooperatively.

Content

1. Introduction: embedded systems, programmable circuits, embedded systems.

2. FPGA's and PSoC. Architectures and applications.

3. Interface with the real world. Sensors and actuators

4. Peripherals in SoCs:

- ADC-based signal acquisition architectures.

- Input / output ports.

- Usual communication protocols in SoC.

- Digital filters.

5. Hardware description languages for creating components.

- Verilog

6. Hardware / software decomposition. Considerations and techniques.

7. SoC operating system

Activities and Methodology

Title	Hours	ECTS	Learning Outcomes
Type: Directed			

Master classes	26	1.04	4, 3, 7, 8, 12
Seminars	12	0.48	4, 3, 7, 12
Type: Supervised			
Laboratory classes	12	0.48	11, 10
Type: Autonomous			
Autonomous work	80	3.2	

Theory classes:

Blackboard presentations of the theoretical part of the syllabus of the subject. The basic knowledge of the subject and indications of how to complete and deepen in the contents are given.

Problem seminars:

The scientific and technical knowledge presented in the master classes is worked on. Problems are solved and case studies are discussed. Problems promote the ability to analyze and synthesize, critical reasoning, and train the student in problem solving.

The methodology followed in problems is as follows: complete exercises are delivered that must be solved. In class, a review is made of the doubts that have arisen.

Laboratory classes:
The practices are carried out during the course and serve to deepen the practical knowledge of the subject.

The practices, whenever the capacity of the laboratory allows, will be carried out in groups of 2.

In the practices, the thinking habits specific to the subject and group work will be developed.

About the use of AI tools.

The use of AI tools helps learning. However, it is not allowed in any of the theoretical-practical activities that have an evaluation activity at the end.

Virtual tool
The Virtual Campus is used as a communication tool for the subject.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Assessment

Continous Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Laboratori classes	40	12	0.48	1, 2, 5, 9, 10, 13
Theory	60	8	0.32	4, 3, 6, 7, 8, 11, 12

This subject/module does not provide for a single assessment system

The assessment of the subject is broken down into the following items:

Continuous assessment:

1. Continuous assessment tests. Continuous assessment tests have a weight between 55% and 60% in the final grade of the subject. The tests, among themselves, have the same weight. A minimum grade of 3.5 is required to be able to make an average in partial tests. Those who do not obtain this grade will be able to recover it in the final exam.

2. Laboratory activities. The weight in the total of the subject is between 35% and 40%. It is essential to pass the practices to pass the subject. There is no established mechanism for recovering practices. Attendance at practices is mandatory.

3. Carrying out exercises and other activities in class (if they are done, it is an optional assessment) can account for 10% of the final grade.

Final exam

There is a final assessment exam to recover the part(s) of the continuous assessment tests that have been failed.

Grade review procedure

For each assessment activity, a place, date and time of review will be indicated in which students can review the activity with the teacher. In this context, complaints may be made about the grade of the activity, which will be evaluated by the teacher responsible for the subject.

If the student does not attend this review, this activity will not be reviewed later.

Considerations

The grade of MH is given whenever the grade is greater than or equal to 90% of the total maximum grade for the subject and excellence is obtained in each of the assessment activities carried out.

Not evaluated indicates that no assessment activity has been carried out.

When one of the minimum grades specified for each assessment activity is not reached, a failure is obtained. The failure grade is calculated by applying a minimum of{4.5, average grade for the subject according to the weighting of activities}.

Irregularities committed

Without prejudice to other disciplinary measures that may be deemed appropriate, and in accordance with current academic regulations, irregularities committed by a student that may lead to a variation in the grade will be graded with a zero (0). For example, plagiarism, copying, allowing copying, unauthorized use of AI (e.g., Copilot, ChatGPT or equivalent) etc. in any of the assessment activities will imply failing it with a zero (0). Assessment activities graded in this way and by this procedure will not be recoverable. If it is necessary to pass any of these assessment activities to pass the subject, this subject will be directly failed, with no opportunity to recover it in the same course.

Repeating students

To receive differentiated treatment, the repeating student must send an email to the subject teacher at the beginning of the course. Each case will be studied in particular.

Any modification that may occur in this assessment forecast due to unforeseen circumstances will be communicated appropriately using the means of communication established at the beginning of the course.

Bibliography

Main bibliography:
J.W. Valvano
Embedded Microcomputer Systems: Real Time Interfacing
Thomson
2011
Saad Motahhir
Smart Embedded Systems and Applications
River Publishers, Gisrupt (Dinamarca)
2023
Verilog:

Stephen Brown and Zvonko Vranesic.
Fundamentals of Digital Logic with Verilog Design
McGrawHill
3a edició
2014

Complementary bibliography:
D.G. Bailey.
Design for Embedded Image Processing on FPGAs.
John Wiley & Sons
2011
S.W. Smith.
The Scientist and Engineer Guide to Digital Signal Processing
California Technical Publishing, San Diego
1999
V. Taraate
Digital Logic Design Using Verilog
Springer India
2016

Software

The PSoC Creator development environment (Cypress) is used for internships.

Modelsim (Intel) is used for modeling and simulation with Verilog

Groups and Languages

Please note that this information is provisional until 30 November 2025. You can check it through this link. To consult the language you will need to enter the CODE of the subject.

Name	Group	Language	Semester	Turn
(PAUL) Classroom practices	321	Catalan	first semester	morning-mixed
(PAUL) Classroom practices	322	Catalan	first semester	morning-mixed
(PLAB) Practical laboratories	321	Catalan	first semester	morning-mixed

(PLAB) Practical laboratories	322	Catalan	first semester	morning-mixed
(PLAB) Practical laboratories	323	Catalan	first semester	morning-mixed
(TE) Theory	320	Catalan	first semester	morning-mixed