UAB
Universitat Autònoma de Barcelona

Hardware/Software Systems

Code: 102794
ECTS Credits: 6

2025/2026

Degree	Type	Year
Computer Engineering	OB	3
Computer Engineering	OT	4

Contact

Name: David Castells Rufas

Email: david.castells@uab.cat

Teachers

Joaquin Saiz Alcaine

Raimon Casanova Mohr

Vanessa Moreno Font

Teaching groups languages

You can view this information at the end of this
document.

Prerequisites

There are none, although it is recommended to have passed the following subjects:

From 2nd year:

- Structure of Computers
- Operating Systems
- Computer Architecture

From 3rd year:

- Embedded Systems

Objectives and Contextualisation

The aim of the subject is to train students to design hardware devices that can be integrated into existing
platforms and develop the necessary software so that these can be controlled from computer applications.

- Learn how to design and verify Hardware
- Learn to communicate Hardware and Software

- Learn to co-simulate Hardware and Software
- Create interfaces and peripherals that connect to a complex system.
- Create systems that reuse existing functionality (Hardware intellectual property blocks, Software libraries, Operating System distributions, etc.)

Competences

Computer Engineering
- Acquire thinking habits.
- Capacity to design, develop, evaluate and ensure the accessibility, ergonomics, usability and security of computer systems, services and applications, as well as of the information that they manage.
- Have the capacity to design and build digital systems, including computers, microprocessor based systems and communication systems.
- Have the capacity to develop specific processors and embedded systems and to develop and optimise the software of said systems.
- Have the right personal attitude.
- Work in teams.

Learning Outcomes

1. Demonstrate a high capacity for abstraction.
2. Design and develop computer systems that fulfil the specifications of the system and the application, and in particular in reference to embedded and real time systems.
3. Design specific processors and embedded systems, meeting the specifications of the application.
4. Develop and optimise software on a system and application level to obtain the desired functionality.
5. Devise communication systems based on digital systems.
6. Manage information by critically incorporating the innovations of one's professional field, and analysing future trends.
7. Work cooperatively.

Content

1. Introduction to Hardware-Software integration
2. FPGAs and programmable circuits
3. Hardware Description Languages (HDL)
4. Hardware simulation techniques
5. Hardware verification
6. Systems on a Chip (SoC)
7. Software development techniques for SoCs
8. Virtual Platforms
9. Hardware/Software Co-Simulation
10. Operating Systems for SoCs

Activities and Methodology

Title	Hours	ECTS	Learning Outcomes
Type: Directed			
Theory classes	26	1.04	5, 1, 4, 2, 3, 6

Type: Supervised			
Laboratory activities	12	0.48	1, 4, 2, 3, 6, 7
Seminars	12	0.48	4, 2, 3
Type: Autonomous			
Study	80	3.2	1, 6

Theory classes:
Exhibitions on the board of the theoretical part of the syllabus of the course. They give the basic knowledge of the subject and indications of how to complete and deepen the contents.

Problem seminars:
The scientific and technical knowledge presented in the master classes is worked on. Problems are solved, practical cases are discussed and problems are raised that the student will have to deliver through the virtual campus. With the problems, the ability to analyze and synthesize, critical reasoning is promoted, and the student is trained in problem solving.

Laboratory practices:
The practices are carried out during the course and serve to deepen the practical knowledge of the subject. The students will work in groups of 2. In the practices, the student will have to develop their own habits of thought of the matter and work in a group.

All the communications will be made through the Campus Virtual.

In this subject, the use of Artificial Intelligence (AI) technologies is not allowed in any of its phases. Any work that includes fragments generated with AI will be considered a lack of academic honesty and may lead to a partial or total penalty in the grade of the activity, or greater sanctions in serious cases.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Assessment

Continous Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Exercises	20%	5	0.2	4, 2, 3
Laboratory activities	30%	10	0.4	4, 3, 7
Theory	50%	5	0.2	5, 1, 4, 2, 3, 6

This subject does not provide for the single assessment system

The evaluation of the course is broken down into the following items:

1. Partial Exams. The weight in the total of the course is 50%. It is necessary to get a minimum mark of 4 in each partial exam. It is necessary to get a minimum mark of 5 in the mean of the theory exams.

2. Laboratory activities. The weight in the total of the subject is 30%. It is necessary to get a minimum mark of 5. There is no established mechanism of recovery of labs. Attendance is mandatory. Repeating students will be able to validate laboratory practices with a grade of 5.

3. Exercises. The weight in the total of the subject is 20%. It is necessary to get a minimum mark of 3. It corresponds to work that will be introduced in the exercises class and the student will deliver through the Virtual Campus.

Evaluation considerations:

- It is considered non-evaluable for the course when there has been no continuous assessment test and no more than two practical sessions.
- In the case of not reaching the minimum required in any of the assessment activities, if the calculation of the final mark is equal to or greater than 4.5, a 4.5 note will be placed on the file.
- Granting a special honors qualification is a decision of the faculty responsible for the subject. The regulations of the UAB indicate that special honors qualification can only be awarded to students who have obtained a final mark of 9.00 or more. It can be granted up to 5% of special honors qualification of the total number of students enrolled.
- The partial exams will be carried out on the established dates and no exception will be made.
- There is a final evaluation test to recover or improve the grade from partial exams. In this last case, the final grade will be the one obtained in this last test.
- The dates of partial examsand delivery of labs and exercises will be published on the virtual campus and may be subject to changes of programming for reasons of adaptation to possible incidents.
- For each assessment activity, a place, date and time of the revision will be indicated in which the student will be able to review the activity with the teacher. In this context, claims can be made about the activity note, which will be evaluated by the teachers responsible for the subject. If the student does not submit to this review, this activity will not be reviewed later.
- Without prejudice to other disciplinary measures deemed appropriate, and in accordance with the current academic regulations, irregularities committed by a student that can lead to a variation of the qualification will be classified by zero (0). For example, plagiarizing, copying, copying, ..., an evaluation activity, will imply suspending this evaluation activity with zero (0). Assessment activities qualified in this way and by this procedure will not be recoverable. If it is necessary to pass any of these assessment activities to pass the subject, this subject will be suspended directly, without the opportunity to recover it in the same course.

Bibliography

- Martin, Grant, Brian Bailey, and Andrew Piziali. ESL design and verification: a prescription for electronic system level methodology. Elsevier, 2010..
- Gajski, Daniel D., Samar Abdi, Andreas Gerstlauer, and GunarSchirner. Embedded system design: modeling, synthesis and verification. Springer Science & Business Media, 2009.
- M.Wolf. Computers as Components: Principles of Embedded Computing Systems Design. Third edition. Morgan Kaufmann Series. Elsevier, 2012
- Patterson, D. A., and J. L. Hennessy. "Computer organization and design RISC-V edition: The Hardware/Software interface.Morgan Kaufmann, 2021.

Software

Intel Quartus Prime Lite Edition (Free).

Python 3 + Jupyter Notebook (Free).

Groups and Languages

Please note that this information is provisional until 30 November 2025. You can check it through this link. To consult the language you will need to enter the CODE of the subject.

Name	Group	Language	Semester	Turn
(PAUL) Classroom practices	431	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	431	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	432	Catalan/Spanish	second semester	morning-mixed
(TE) Theory	430	Catalan/Spanish	second semester	morning-mixed