

Degree	Type	Year
Computer Engineering	FB	1

Contact

Name: Mercedes Rullan Ayza

Email: mercedes.rullan@uab.cat

Teachers

Joaquin Saiz Alcaine

Lluís Antoni Terés Terés

Gabriel Ramirez Gonzalez

David Castells Rufas

Isaac Martinez Sabate

Jordi Sacristan Riquelme

Teaching groups languages

You can view this information at the [end](#) of this document.

Prerequisites

There are no formal prerequisites, but it is recommended to have taken and passed the first-year Computer Fundamentals course, first semester.

Objectives and Contextualisation

The objective of the course is for students to understand the role that digital systems play in the world of Information and Communication Technologies (ICT) in general, and to be capable of designing and implementing medium- to low-complexity digital circuits using logic gates and reconfigurable devices. They should also understand that a computer is nothing more than a digital system of a certain complexity.

The course introduces methodologies based on "Processing Unit - Control Unit (PU-CU)" architectures to solve digital systems of moderate complexity, presenting the basic concepts of these architectures in both their "hardwired" version (PU-CU built with gates and logic blocks) and their "microprogrammed" version (CU based on ROM + sequencer). In the third part of the course, the design of an open-source processor (RISC-V) is presented, starting from its basic instruction set and applying the design strategies and methodologies of the previously introduced PU-CU architectures. Both the microprogrammed version (RVuabM) and the hardwired

version (RVuabC) of this processor are implemented, and the main cost/performance differences between the two approaches are analyzed. The course concludes with a brief introduction to the concept of pipelining as an optimal and widely used solution in modern processors.

Learning Outcomes

1. KM08 (Knowledge) Recognise the different parts of computers, as well as their internal functioning.
2. SM08 (Skill) Determine the basic architecture and functional units of a computer and its theoretical foundations of programming.

Content

Block 1. Sequential Circuits (SC)

- Moore and Mealy machines.
- Finite State Machines (FSM). Formal definition, implementation, and response time.
- Basic concepts of System Verilog (SV). Examples of FSM descriptions in SV.
- Synthesis of sequential circuits from an algorithm.

Block 2. Processing Unit - Control Unit (PU-CU) Architecture

- Processing Unit (PU) - Control Unit (CU) architecture.
- PU with multiplexers and with buses.
- Control Unit with a sequencer based on a ROM.

Block 3. RISC-V Processor Design

- Basic structure of a simple processor. Von Neumann vs Harvard architecture. Functional units and buses.
- Processor instruction set. Programming in machine language. Microinstructions and microprograms, micro-operations, and status signals.
- Example of an open-source processor: RISC-V
- Harvard architecture. Fetch, decode, and execute cycles.
- RVuabM: Microprogrammed implementation of the Control Unit.
- RVuabC: Hardwired single-cycle implementation of the Control Unit.
- RVuabPL: Introduction to RISC-V Pipeline.

Activities and Methodology

Title	Hours	ECTS	Learning Outcomes
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Type: Directed			
Exercise-based classes	30	1.2	KM08, SM08, KM08
Laboratory practices	12	0.48	KM08, SM08, KM08
Type: Supervised			
Case study	12	0.48	KM08, SM08, KM08
Laboratory practice assignments	10	0.4	KM08, SM08, KM08
Type: Autonomous			
Autonomous work	40	1.6	KM08, SM08, KM08
Preparing and solving exercises	16	0.64	KM08, SM08, KM08
Videos viewing	12	0.48	KM08, SM08, KM08

The course is organized into three blocks. The materials provided through the Virtual Campus include a series of videos that students are required to watch before attending class. These videos contain the theoretical and practical knowledge necessary for digital systems design. Additionally, students have access to automatically graded interactive exercises and a digital systems simulation environment.

The course is taught using a "problem-based classroom" approach. All face-to-face sessions are problem-oriented and focus on addressing questions and doubts arising from the videos, as well as on solving cases proposed by the teaching staff or the students themselves. Active student participation in these sessions is essential; these are not conventional "lecture-based" classes. Sessions are conducted in small groups (around 30-40 students), a necessary condition to ensure the required level of interactivity in a course with a highly practical and applied nature.

The course also includes laboratory sessions in which students physically implement the circuits they have previously only designed on paper or in a simulation environment. Each lab session hosts 20-25 students working in pairs and lasts 2 hours.

Tutorials may be individual or in small groups and are scheduled on demand in coordination between each instructor and their students. Group tutorials may also be proposed by the teaching team, but in such cases, students must submit specific questions in advance through the corresponding Virtual Campus (VC) forum. This allows instructors to properly plan and conduct the tutorial session.

Annotation: Within the schedule set by the centre or degree programme, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

Assessment

Continuous Assessment Activities

Title	Weighting	Hours	ECTS	Learning Outcomes
Exercises delivering (periodic)	20%	10	0.4	KM08, SM08
Laboratory practices	30%	0	0	KM08, SM08

This course does not include the single assessment option.

a) Evaluation process and scheduled activities

1. Two midterm exams, to be taken individually and in person, under controlled conditions and in written format. These exams assess the students' acquired knowledge and their ability to solve problems by designing appropriate and efficient digital circuits.
2. Exercise resolution: consists of a set of online exercises with automatic grading, which students must submit by specified deadlines. Individual activity
3. Video viewing prior to attending class.
4. Activities in which students must demonstrate the competencies acquired during the lab sessions (attendance required). Group activity of 2 students.

The final grade for the course obtained through continuous assessment (CA) is calculated as follows:

- (Activity 1) The average of the two midterm exams (MT1 and MT2)
- (Activities 2 and 3) Completion of exercises and video viewing (Ex)
- (Activity 4) Grade from the evaluated lab activities (LB)

Formula: $CA = MT \cdot 0.5 + Ex \cdot 0.2 + LB \cdot 0.3$,
where $MT = (MT1 + MT2) / 2$

To pass the course through continuous assessment, the following conditions must be met:

- $CA \geq 5$
- $MT1$ and $MT2 \geq 4$ (each), and $MT \geq 5$
- $LB \geq 5$

b) Schedule of evaluation activities

The dates for exams and assignment submissions are published at the beginning of the course on the Virtual Campus (VC) and on the School's website (exam section). These dates may be subject to change due to unforeseen circumstances. Any changes will be communicated through the CV.

It is important to note that no exams will be administered outside the scheduled dates, unless there is a justified reason, communicated in advance and with the instructor's approval and the approval of the teaching team.

c) Resit process

Activity 1 (theory exams) can be retaken during the final exam.

- If the grade obtained in one of the partial tests PP1 or PP2 is < 4 , this grade must be exceeded by taking a retake exam in the corresponding partial. In order to apply the formula (which takes into account the partial tests, the assessables and the practices), the grade obtained in this retake must be ≥ 5
- If the grade obtained in the 2 partial tests respectively is < 4 , the student must take a new exam that will include the entire subject. The grade obtained will be the new PP grade, which must be ≥ 5 in order to apply the formula (which takes into account the partial tests, the assessables and the practices).

A student who has passed a partial exam or even passed through continuous assessment can retake the exam. The final grade will be the one obtained in this retake, whether better or worse than the previous one.

Activities 2 and 3 (exercises and video viewing, worth 20% of the final grade) cannot be retaken.

Activity 4 (labs) also cannot be retaken.

If $MT < 5$ or $LB < 5$, the final course grade will be the lower of the continuous assessment grade (CA) or 4.5.

d) Grade review procedure

Grades for evaluation activities will be published on the Virtual Campus. Once published, information on the grade review process will be provided. Normally, a deadline will be set for students to request a review. Based on the requests, students will be informed of the specific date and time for the review session.

If a student does not follow the established procedure or does not attend the review, the activity will not be reviewed later. The review of any test can mean either an improvement or a worsening of the corresponding grade, depending on the revised interpretation made of the test.

e) Special grades

- A student who has not participated in any assessment activity or lab session will receive a grade of "Not Assessable".
- To be eligible for an "Honors Distinction (MH)", a final grade of ≥ 9.0 is required. However, since the number of MHs awarded cannot exceed 5% of enrolled students, this condition alone is not sufficient. MHs will be granted to the students with the highest grades.

f) Consequences of academic misconduct: copying, plagiarism, etc.

Without prejudice to other disciplinary measures, and in accordance with current academic regulations, any academic misconduct by a student that may affect the grading of an assessment activity will result in a zero (0) grade for that activity. Such activities cannot be retaken.

If the activity in question is required to pass the course, the course will be automatically failed with no opportunity for retake during the same academic year.

These irregularities include, but are not limited to:

- Full or partial copying of a lab report, assignment, or any other evaluable activity
- Allowing others to copy
- Submitting group work not entirely completed by all group members (this applies to all members)
- Unauthorized use of AI tools (e.g., Copilot, ChatGPT, or equivalents) to solve exercises, labs, or any evaluable activity
- Presenting third-party work as one's own, including translations or adaptations
- Possession of communication devices (e.g., phones, smartwatches, pens with cameras, etc.) during individual or group assessment activities (exams)
- Talking to classmates during individual assessments (exams)
- Copying or attempting to copy from others during exams
- Using or attempting to use unauthorized materials during exams

Restricted use of AI: for this subject, the use of Artificial Intelligence (AI) technologies is allowed exclusively in support tasks, such as bibliographic or information searches. The student must clearly identify which parts have been generated with this technology, specify the tools used and include a critical reflection on how these have influenced the process and the final result of the activity. The lack of transparency in the use of AI in this assessable activity will be considered a lack of academic honesty and may lead to a partial or total penalty in the grade of the activity, or greater sanctions in serious cases.

In summary: copying, allowing others to copy, or plagiarism (or the attempt) in any assessment activity results in an automatic fail, not compensable and with no validation of previous work in future editions of the course.

g)Evaluation of repeating students

In the evaluation process described, there will be no differentiated treatment for repeating students.

Bibliography

- Coursera MOOC: <https://www.coursera.org/learn/digital-systems>
- Digital Systems: From Logic Gates to Processors. Deschamps JP, Valderrama E, Terés L. Springer 2017. ISBN 978-3-319-41198-9.
- Complex Digital Systems. Deschamps JP, Valderrama E, and Terés L. Springer 2019. ISBN 978-3-030-12652-0.
- Diseño de Sistemas Digitales. Deschamps JP, Ed. Paraninfo 1989. ISBN 84-283-1695-9.
- Digital Systems Fundamentals. T.L. Floyd. Ed. Prentice Hall. 9ª Edición ISBN: 8483220857.
- Arquitecturas UP-UC: de los sistemas digitales a medida al procesador de propósito general RISC-V. Valderrama E., Deschamps J-P., Rullan M. y Terés, L. Apuntes del bloque-3 del curso.

Software

- Quartus II Web Edition

Groups and Languages

Please note that this information is provisional until 30 November 2025. You can check it through this [link](#). To consult the language you will need to enter the CODE of the subject.

Name	Group	Language	Semester	Turn
(PAUL) Classroom practices	411	Catalan/Spanish	second semester	morning-mixed
(PAUL) Classroom practices	412	Catalan/Spanish	second semester	morning-mixed
(PAUL) Classroom practices	431	Catalan/Spanish	second semester	morning-mixed
(PAUL) Classroom practices	432	Catalan/Spanish	second semester	morning-mixed
(PAUL) Classroom practices	451	Catalan/Spanish	second semester	afternoon
(PAUL) Classroom practices	452	Catalan/Spanish	second semester	afternoon
(PLAB) Practical laboratories	411	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	412	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	413	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	414	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	415	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	416	Catalan/Spanish	second semester	morning-mixed

(PLAB) Practical laboratories	417	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	418	Catalan/Spanish	second semester	morning-mixed
(PLAB) Practical laboratories	419	Catalan/Spanish	second semester	afternoon
(PLAB) Practical laboratories	420	Catalan/Spanish	second semester	afternoon
(PLAB) Practical laboratories	421	Catalan/Spanish	second semester	afternoon
(PLAB) Practical laboratories	422	Catalan/Spanish	second semester	afternoon