

| Degree                        | Type | Year |
|-------------------------------|------|------|
| Telecommunication Engineering | OB   | 1    |

## Contact

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## Teachers

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## Teaching groups languages

You can view this information at the [end](#) of this document.

## Prerequisites

Previous elementary knowledge on SystemVerilog (evolution from Verilog) Hardware Description Languages is required. For those students that don't have these minimal skills, we will offer complementary sessions prior to the starting of the course either face-2-face (to be scheduled) or on-line (e.g. part of [https://www.cadence.com/en\\_US/home/training/all-courses/82143.html](https://www.cadence.com/en_US/home/training/all-courses/82143.html)).

Knowledge on the following subjects is recommended:

Digital Signal Processing

Electronic Systems Design

Electronic Systems and Applications

## Objectives and Contextualisation

(This course has been updated for the year 2025-26)

The main objective of this course is to learn, understand and be able to design electronic systems for digital signal processing with the focus on integrated systems. These systems are composed of integrated circuits that manage their computation and communication. The study of these integrated systems will be oriented to the usual digital signal processing architectures with the focus on applications of acoustics, audio and speech processing.

Different design methodologies will be used according to the level of abstraction (system, architecture, implementation).

Hardware Description Languages (HDL) will be used to prototype such systems in the labs on electronic boards with FPGA reconfigurable devices.

## Competences

- Be capable of using programmable logic as well as designing advanced electronic systems, both analogue and digital.
- Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
- Capacity for working in interdisciplinary teams
- Knowledge of the hardware description languages for highly complex circuits
- Maintain proactive and dynamic activity for continual improvement
- Students should be capable of integrating knowledge and facing the complexity of making judgements using information that may be incomplete or limited, including reflections on the social and ethical responsibilities linked to that knowledge and those judgements
- Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
- Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously

## Learning Outcomes

1. Capacity for critical reasoning and thought as means for originality in the generation, development and/or application of ideas in a research or professional context.
2. Capacity for working in interdisciplinary teams
3. Design ASICs
4. Design integrated circuits using hardware description languages through ASICs and/or FPGAs
5. Knowledge of the hardware description languages for highly complex circuits
6. Maintain proactive and dynamic activity for continual improvement
7. Students should be capable of integrating knowledge and facing the complexity of making judgements using information that may be incomplete or limited, including reflections on the social and ethical responsibilities linked to that knowledge and those judgements
8. Students should know how to apply the knowledge they have acquired and their capacity for problem solving in new or little known fields within wider (or multidisciplinary) contexts related to the area of study
9. Students should know how to communicate their conclusions, knowledge and final reasoning that they hold in front of specialist and non-specialist audiences clearly and unambiguously
10. Use programmable digital logic.

## Content

1. Introduction to Integrated System Design for Digital Processing  
Fundamentals of Digital Signal Processing (Quantization, Sampling, Z-transform, Filter design, Digital Fourier Transform)  
Microelectronic Design Methodologies for ASIC and FPGA

2. High-level Digital Signal Processing  
Introduction to Acoustics, Spatial Audio, Speech Sounds and Speech Processing  
Source Filter Models & Speech Coding  
Perceptual Models and Hearing Devices (Hearing Aids and Cochlear Implants)

3. Adaptation for Implementation of Signal Processing Algorithms  
 Asynchronous sample rate conversion (ASRC) and Real time low latency processing (circular buffers)  
 Optimization of algorithms (Fast Fourier Transform - Radix algorithms)  
 Floating point to Fixed Point conversion Algorithms

4. Systems-on-a-Chip Design Methodologies

Virtual Components (IPs) and its connectivity  
 SystemVerilog for HDL Modelling and synthesis  
 Verification techniques: HDL simulation, Hardware-in-the-loop (HIL)

5. Deployment on Integrated Systems

Chip structure: ASICs & FPGAs  
 Power Performance Analysis (PPA): area, speed & Energy  
 Clock and Power Management  
 Prototyping and industrialization

Laboratories: Real-time Audio and Speech Digital Signal Processing on FPGA

**Activities and Methodology**

| Title   | Hours | ECTS | Learning Outcomes          |
|---|-------|------|----------------------------|
| Type: Directed                                  |       |      |                            |
| Laboratory Sessions                             | 15    | 0.6  | 1, 2, 5, 4, 6, 8, 9, 7, 10 |
| Lectures  | 30    | 1.2  | 1, 5, 3, 4, 6, 8, 7, 10    |
| Type: Supervised                                |       |      |                            |
| Thematic Homework (Individual)                  | 10    | 0.4  | 1, 6, 8, 9, 7              |
| Type: Autonomous                                |       |      |                            |
| Laboratory activities preparation and reporting | 20    | 0.8  | 1, 2, 5, 4, 8, 7, 10       |
| Study   | 69    | 2.76 | 1, 5, 3, 4, 6, 8, 7, 10    |

The course will be mainly driven by the lectures, that will use ad hoc material (presentations, documents, links, tools and other resources) available in the virtual campus (VC) of the UAB (<https://cv.uab.cat>). Students will deliver exercises on specific subjects (on the Virtual Campus).

Laboratory work will let the students to apply and experiment the concepts acquired on FPGA platforms, widely used in industry. Inici del formulari

Attendance will be mandatory for all sessions. Any lack of attendance must be communicated in advance to the teacher in charge, attaching the corresponding reasonable justified reasons.

The use of AI is allowed in this course and it is recommended to validate its result before submitting any report since it can make serious errors that may imply negative evaluations.

Annotation: Within the schedule set by the center or master program, 15 minutes of one class will be reserved for students to evaluate their lecturers and their courses or modules through questionnaires.

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## Assessment

### Continous Assessment Activities

| Title                             | Weighting | Hours | ECTS | Learning Outcomes          |
|-----------------------------------|-----------|-------|------|----------------------------|
| Individual Exercises              | 15%       | 1     | 0.04 | 1, 6, 8, 9, 7              |
| Laboratory work reports           | 35%       | 1     | 0.04 | 1, 2, 5, 4, 6, 8, 9, 7, 10 |
| Partial Evaluación (Part 1): Exam | 25%       | 2     | 0.08 | 5, 3, 4, 8, 9, 7, 10       |
| Partial Evaluación (Part 2): Exam | 25%       | 2     | 0.08 | 1, 3, 6, 9                 |

This course does not provide for the single assessment system (No exam).

Student assessment uses continuous evaluation made up of the following assessments:

- Two partial exams for the each part of the course, which gives 25% of the final grade.
- Individual work in thematic exercises (delivered on the virtual campus), which accounts for 15% of the final grade
- Team work in the laboratory, scheduled in 5 sessions, with the obligation to deliver the corresponding individual reports. An evaluation above 5 is mandatory to pass the course. This activity contributes 35% to the final grade of the course.

The final exam allows students to assess the achievement of skills in a single exam or to recover any partial assessments that had a mark lower than 3.5. That is also the minimum mark required for any of the parts to pass the course and the average mark of both exams is not below 5.

A weighted final grade of not lower than 5 is required to pass the course.

In order to obtain MH, students will need to have an overall qualification higher than 8.5 with the limitations of the UAB (1 MH/10 students). As a reference criterion, they will be assigned in descending order.

Plagiarism will not be tolerated either in exams or in individual activities on the Virtual Campus. In this case, the available tools will be used to verify it. All students involved in plagiarism will be automatically suspended. A final grade of no more than 30% will be assigned.

Open source code or available libraries can be used but they must be referred in the corresponding reports.

The student will receive a grade of "Not Evaluable" if:

- the student has not been able to be evaluated in the laboratory due to not attendance or not deliver the corresponding reports without justified cause.
- the student has not carried out a minimum of 50% of the activities proposed.
- the student has not taken the final exam.

Repeating students will be able to "save" their grade in lab but not in the rest of the activities.

## Bibliography

## Digital Speech Processing

- Peter Vary, Rainer Martin, Digital Speech Transmission: Enhancement, Coding and Error Concealment, John Wiley & Sons Inc, 2006. (New issue to appear during 2024).
- L.R. Rabiner and W. Schafer. 2007. Introduction to digital speech processing.  
[http://cronos.rutgers.edu/~lrr/dsp%20design%20course/final\\_speech\\_paper\\_1\\_2008.pdf](http://cronos.rutgers.edu/~lrr/dsp%20design%20course/final_speech_paper_1_2008.pdf)
- Xuedong Huang, Alex Acero, Hsiao-Wuen Hon, Spoken Language Processing: A Guide to Theory, Algorithm, and System Development, ISBN: 0130226165, Prentice Hall, 2001.

## Hearing Aids and Cochlear Implants

- Harvey Dillon, Hearing Aids, ISBN 3131289414, Thieme, 2010
- Graeme Clark, Cochlear Implants: Fundamentals and Applications (Modern Acoustics and Signal Processing), ISBN 0387955836, Springer, 2013.

## SoC Design & HDL

- Chakravarthi, V.S. A practical approach to VLSI system on chip (SoC) design: a comprehensive guide [on line]. Cham: SpringerCham,2020. Available at:  
<https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-030-23049-4>. ISBN 9783030230494.
- P. Bricaud, M. Keating : "Reuse Methodology Manual for System-On-A-Chip Designs"
- Spear, C.; Tumbush, G. SystemVerilog for verification: a guide to learning the testbench language features [on line]. 3rd ed. New York,NY: Springer, 2012. Available at:  
<https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-1-4614-0715-7>. ISBN 9781461407157.
- Vaibbhav Taraate, Digital logic design using Verilog : coding and RTL synthesis, Springer, ISBN 978-981-16-3198-6, 2022. Available at on-line through your UAB account <https://bibcercador.uab.cat/>
- Mehta, A.B. ASIC/SoC functional design verification [on line]. Springer, 2017 [Consultation: 11/06/2024]. Available on:  
<https://link-springer-com.recursos.biblioteca.upc.edu/book/10.1007/978-3-319-59418-7>. ISBN 9783319594187.
- Wile, B.; Goss, J.C.; Roesner, W. Comprehensive functional verification: the complete industry cycle [on line]. Elsevier/MorganKaufmann, 2005.Avaliable at:  
<https://ebookcentral-proquest-com.recursos.biblioteca.upc.edu/lib/upcatalunya-ebooks/detail.action?pqrq> ISBN 9780080476643.

## Integrated and Embedded Systems:

- Edward A. Lee and Sanjit A. Seshia, Introduction to Embedded Systems, A Cyber-Physical Systems Approach, Second Edition, MIT Press, ISBN 978-0-262-53381-2, 2017.Avaliable at  
[https://ptolemy.berkeley.edu/books/leeseshia/releases/LeeSeshia\\_DigitalV1\\_08.pdf](https://ptolemy.berkeley.edu/books/leeseshia/releases/LeeSeshia_DigitalV1_08.pdf)
- I. Grout "Digital Systems Design with FPGAs and CPLDs"
- H.J.M. Veendrick "Nanometer CMOS: from ASICS to BASICS", 2ª edición, Springer. 2017. Available at on-line through your UAB account <https://bibcercador.uab.cat/>

## Software

Students will use two main high level signal processing tools:

- Application Specific tools for recording (smartphone or PC with microphone), plus Audacity SW to edit the sounds (<http://audacity.sourceforge.net/>) and PRAAT (<http://www.fon.hum.uva.nl/praat/>) as speech processing tool including a great variety of integrated function
- Matlab/Simulink as a general purpose platform for model building, transformation and generation of the hardware descriptions of the systems to implement.

The electronic design tools (EDA) associated with Intel-Altera FPGA boards used in laboratories that enable:

- Specification of digital systems in HDL languages
- Building SoC architectures for RISC processors (ARM, NIOS)
- Logical and physical synthesis of HDL
- Downloading HW and SW code from the PC to the FPGA
- Execution of the algorithm in the FPGA

Intel Altera's DE1\_SoC board will be used as the SoC-FPGA platform.

Students will have free access, upon request, to courses on industrial EDA tools (CADENCE) useful for their curriculum and training, mainly for subjects 4 and 5.

[https://www.cadence.com/content/dam/cadence-www/global/en\\_US/documents/training/learning-maps.pdf](https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/training/learning-maps.pdf)

## Groups and Languages

Please note that this information is provisional until 30 November 2025. You can check it through this [link](#). To consult the language you will need to enter the CODE of the subject.

| Name                       | Group | Language | Semester        | Turn      |
|----------------------------|-------|----------|-----------------|-----------|
| (TEmRD) Teoria (màster RD) | 1     | English  | second semester | afternoon |