Instead of methacrilate, the device was manufactured in Teflon, which provided smaller deformability during heat periods. Operation with the device was relatively straightforward. First, the chip was positioned face down onto the rectangular site ground of the inferior device slab. Then, the superior slab was put into place and the chip was clamped using Allen screws until an effective airtight sealing of the chip ends was accomplished by means of the underlying toric joints. Thereafter, Ø1 mm, 2.5 mm-long copper bars with soldered signal wires were introduced into the electrical access holes and effectively clamped with electrically-insulated (Kapton adhesive tape covered) clamps mounted on Ø4 mm screw pedestals. Finally, a 1.1W-12 V electric fan (SUNON) was mounted on the chip opening to provide fast dissipation cooling. After assembly (see Figure 166), electrical contacts were checked (typically by measuring sensor and actuator resistors with a multi-meter) and the device was ready for operation.
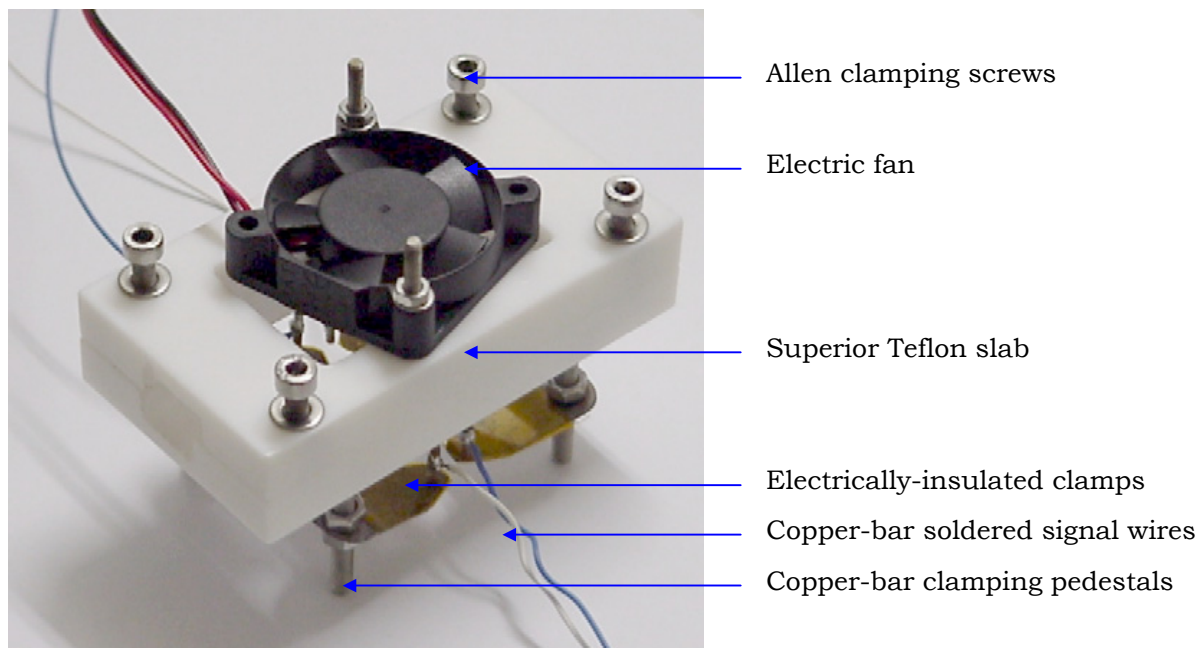

Figure 166 - Assembled, ready-for-operation Teflon device.

Methacrilate and Teflon devices were manufactured by Jose A. Rus, Julian Felipo and Jose L. Fernández, to whom I would like to convey my gratitude for their patience and readiness at work.

8.2.4. CHIP WIRING AND BONDING

To electrically and thermally characterize the behavior of polysilicon resistors both as actuators (see p.228) and sensors (see p. 231) special printed circuit boards were designed for chip placement and wiring.

Custom PCBs

Custom PCBs were designed with CorelDraw7 design software (*Corel*) and printed on a slide film with a 300 dpi laser printer. The pattern was then transferred to a 1.6 mm-thick blank photo-resist coated copper clad board (*Bungard*) by insulation for 2.5 min in a DP130/UV30.40 vacuum-fix insulator (*CIF*). Development was done by immersion in PDN developer (*Electrolube*) for 1.5 min and then the exposed copper layer was etched away with a H_2O_2:salfuman:H_2O (1:1:2) solution [Salfuman: HCl-20%, NO-HSO$_4$-5%, *Tequima*). The remaining photo-resist was then removed with FLUX-SK10 spray (Kontakt Chemie). After completing the PCB process, Ø1 mm holes were drilled onto the contact pad zones of the PCB circuit with a 395 Multipro PCB precision drill (*Dremel*) and terminal blocks mounted and soldered into them.

Initial PCB designs (see Figure 167a) did not have a central ventilation opening under the chip and, thus, forced-convection cooling times were larger for these devices (see p.230). Later designs (see Figure 167b) included a central ventilation hole and provided pedestal support for a KDE1206PTS3 1.1W-12 V axial fan that provided powerful forced-convection to the chip for fast cooling.
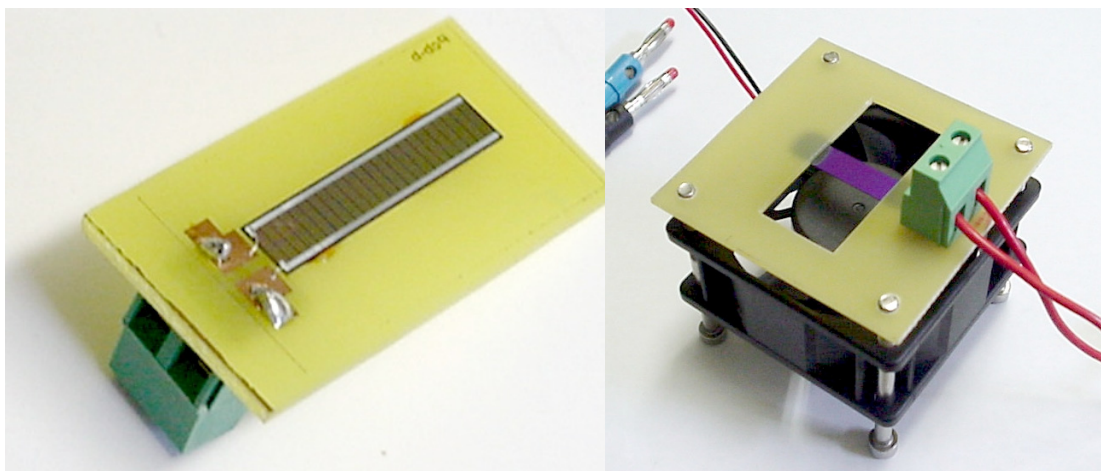

Figure 167 - Initial PCB design (a) and final setup for the later systems (b).

Wiring and bonding

After completion of the PCBs, chips were bonded to these with a 120 ºC thermo-curable epoxy layer and wired to the pad zones of the PCB with a Ø381 μm platinum wire (see Figure 168), capable of delivering currents far larger than the 2 A here required.
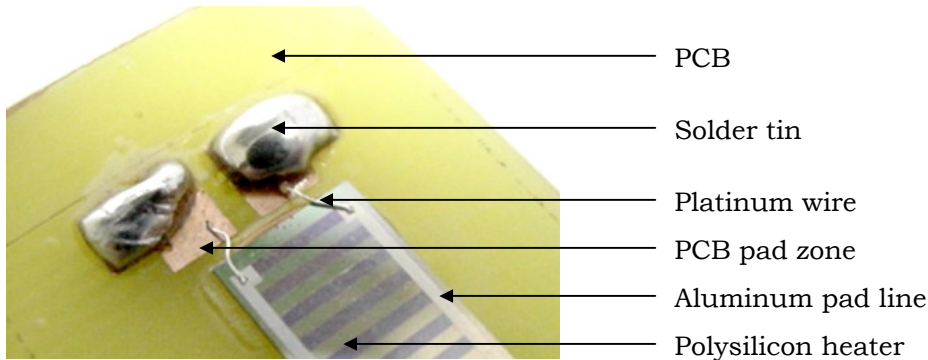

PCB

Solder tin

Platinum wire

PCB pad zone

Aluminum pad line

Polysilicon heater

Figure 168 - Detail of the wiring for a polysilicon chip in one of the initial PCB designs.

8.3. ELECTRONICS, SENSORS AND ACTUATORS

8.3.1. CIRCUIT BOARDS DESIGN AND FABRICATION

Circuit design

Many different circuits (power drivers, Pt100 and thermocouple conditioning circuitry, otpo-isolation boards, etc.) have been designed and produced within the work here reported. Typically, initial design ideas were first implemented and checked on aluminum based breadboards (*Wisher*). Occasionally, as in the case of analog opto-coupler isolation circuitry, simplified designs were electrically simulated using PC design software OrCAD-9 (*Cadence*) built-in pSPICE module. Thereafter, schematics were invariably designed with OrCAD-9 CaptureCIs module, using available or custom developed footprint libraries. Net-listing and initial placing & routing were carried out with OrCAD-9 LayoutPlus module, and finished manually with the same software (see Figure 169).

Circuit production

Circuit layouts obtained with OrCAD-9 LayoutPlus module were printed on a slide film using a 300 dpi LaserJet 4100DTN laser-printer (*Hewlett-*

Packard). As in the case of chip-bonding PCBs (see p.302), the ensuing pattern was then transferred to a 1.6 mm-thick blank photo-resist coated copper clad board (*Bungard*) by insulation for 2.5 min in a DP130/UV30.40 vacuum-fix insulator (*CIF*). For some PCBs, this process was repeated for both sides of the copper clad board, with manual alignment of double-side motifs. After insulation, resist development was carried out by immersion in PDN developer (*Electrolube*) for 1.5 min and then the exposed copper layer was etched away with a H_2O_2:salfuman:H_2O (1:1:2) solution. The remaining photo-resist was then removed with FLUX-SK10 spray (*Kontakt Chemie*). After completing the PCB process, Ø0.75 mm holes were drilled into pad zones of the PCB circuit with a 395 Multipro PCB precision drill (*Dremel*) and terminal blocks mounted and soldered into them.
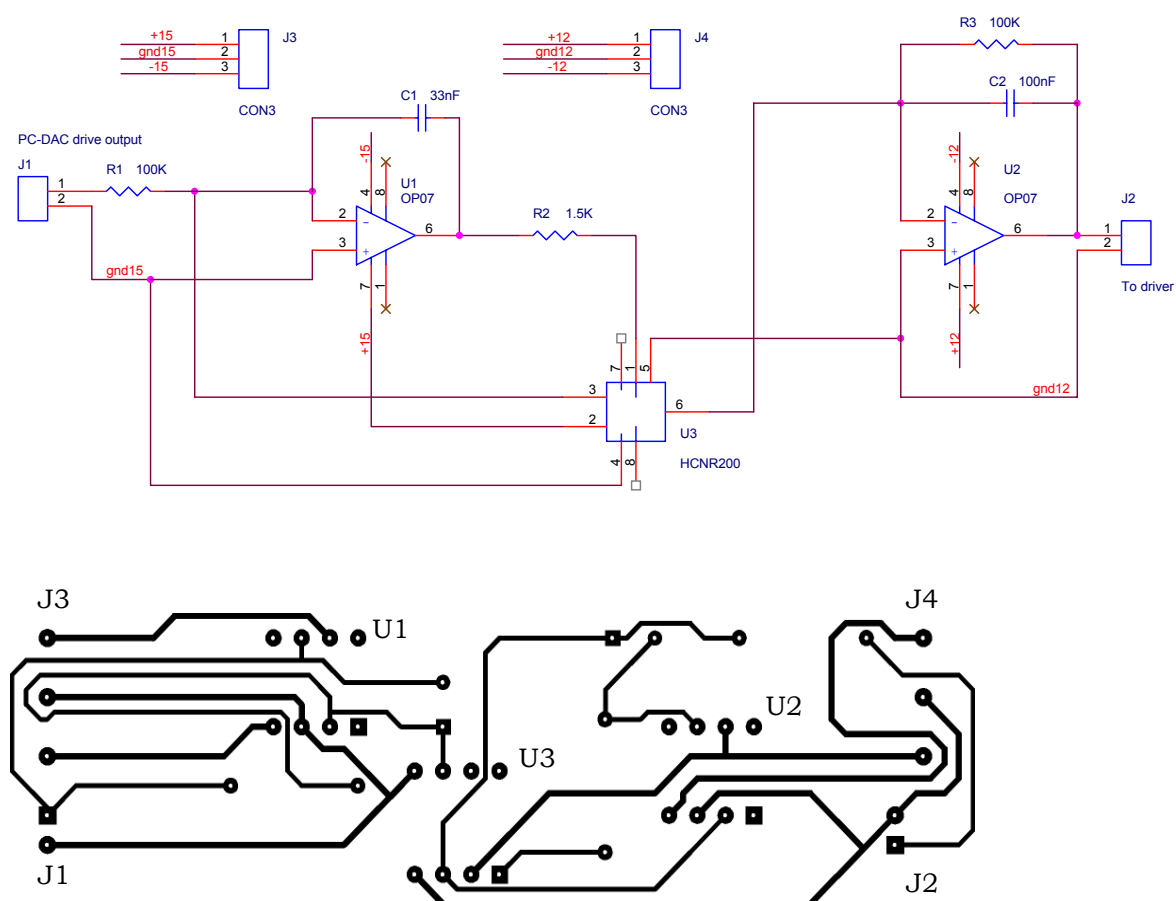

Figure 169 - Example of a typical OrCAD-9 CaptureCIs schematic and the ensuing LayoutPlus layout (in this case, the drive opto-isolation circuit, see p.253).

8.3.2. DATA ACQUISITION BOARD

To accomplish fast and accurate temperature control, a PCI-1200 DAQ device was acquired from *National Instruments*. The PCI-1200 data acquisition board features 12bit A/D-D/A ±5 V analog input (eigth) and output (two) channels, together with three 8-bit digital ports. Scan rates are determined by the settling time for input multiplexers and are dependent on the desired gain. In this work, the typical multi-channel scan rate was of 12,000 samples per second, with an internal gain of 2, and 1000 samples were software averaged to filter-out noise, yielding a real scan rate of 12 samples per second. Finally, the PCI-1200 board can be configured in three different input modes: differential (DIFF), referenced single-ended (RSE) and non-referenced single-ended (NRSE). Differential mode halves the number DAC analog inputs, since it requires to wires for each input (signal and reference ground). Initial measures were conducted in DIFF mode, to ensure precision readings, but, after the repeated occurrence of ground-loop problems, the board was reconfigured into NRSE mode, where all signals are referenced to an external ground, eliminating ground-loop and common-mode voltage problems.

8.3.3. SENSORS AND ACTUATORS

Actuators

Since polysilicon resistors have already been extensively documented previously (see p.219-240), the following section covers the fundamentals of the remaining kind of actuators: Peltier cells.

Peltier cells

Thermoelectricity basics

Peltier cells are thermoelectric elements based on the Peltier effect (as opposed to the Seebeck effect governing thermocouples), discovered by *Jean Peltier* while investigating the latter and further formulated by *Lord Kelvin* in 1854. The basic intuitive notion of both Seebeck and Peltier reversible thermodynamic effects is that heat and charge carriers in a solid conductor/semiconductor are basically the same elements: electrons. In essence, when a heat gradient is applied over a solid conductor, the electron cloud will undergo a kinetic redistribution and the electrons will

loose or gain energy levels according to whether they move to lower or upper heat regions. This electronic imbalance will induce an electric field that is called the Thomson effect after *Lord Kelvin's* discovery.
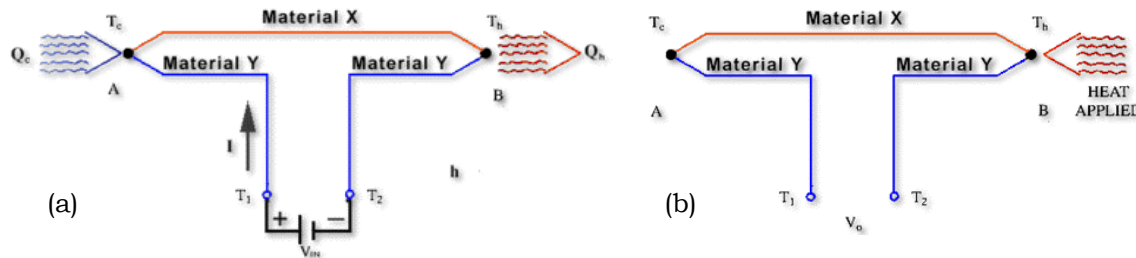

Figure 170 - Schematic diagram for Peltier (a) and Seebeck (b) effects. Source: *Ferrotec, Inc.*

Therefore, when two dissimilar conductor or semiconductor materials are coupled as in Figure 170a and a voltage is applied across the circuit, a temperature flow will be also induced across the conductors. According to thermodynamics law of energy preservation, the difference in temperature flows provoked by the electric field at each of the conductors must be absorbed or lost as radiation at the junctions between both materials. This net effect is called the Peltier effect. Conversely, if voltage is measured instead of imposed and a temperature gradient between the junctions is induced, the Seebeck effect will induce an electromotive force in the circuit (see Figure 170b). The basic equations that govern these principles are shown in Equation 13 and the Seebeck and Peltier effects can be used for heat-pumping (Peltier cells), temperature measurement (Seebeck thermocouples) or even electricity generation.

$$V_{Seebeck} = \alpha_{xy}\left[T_h - T_c\right] \qquad Q_{Peltier} = \rho_{xy} \cdot I$$

Equation 13 - Equations for Seebeck voltage (V) and Peltier heat power (W). α_{xy} (V/°C) and ρ_{xy} (V) are the differential Seebeck and Peltier coefficients for materials x and y, while T_h and T_c are hot and cold junction temperatures (°C) and I is the intensity (A) flowing across the Peltier junction.

In practice, even the best semiconductor Peltier junctions (Bi_2Te_3) do not offer large mass heat-pumping by themselves and, thus, they are arranged in parallel arrays of junctions and capped with (typically) ceramic substrates in what has become to be known as Peltier cells (see Figure 171).
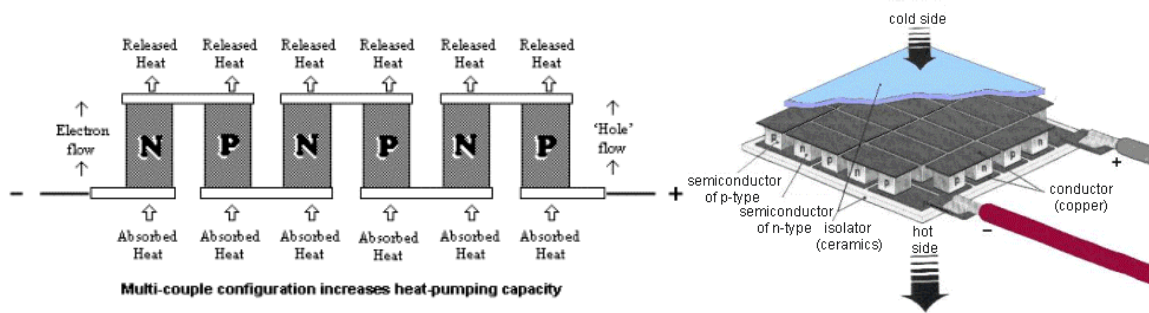
Figure 171 - Parallel (electrically serial) array of Peltier junctions in a standard Peltier cell configuration. Source: *Ferrotec, Inc.*

Peltier cells can be made more powerful (have higher heat-transfer rates) by increasing the density of PN junctions, but their differential temperature limit is at last determined by the ultimate differential capabilities of its individual components (around 68 ºC for Bi_2Te_3 junctions under a null load thermal mass). Therefore, to obtain larger temperature differentials and increase heat-pumping power, Peltier cells can be arranged in vertical cascade (or multistage) configurations, where each member of the serial cascade sees its reference (cold) temperature as the pumped heat from the previous stage. In this case, and contrary to the single Peltier cell configuration of junctions, the arrangement is spatially serial, but electrically parallel. To maximize heat-transfer rates, cascade Peltier assemblies are usually arranged in a pyramidal shape (see Figure 172), with the most powerful Peltier cell placed at the bottom.
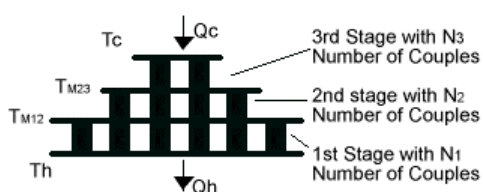

Figure 172 - Standard multistage Peltier cell pyramidal configuration.

Selected Peltier cells

As previously discussed (see p.149), the pyramidal shape of standard cascade modules provided unfeasible dimensions for the chips here used and, although custom cascade setups with varying dimensions can be ordered, they are highly expensive. Therefore, it was decided to acquire single-stage Peltier cells of two different dimensions (roughly, chip and

reservoir dimensions) and to evaluate their performance prior to acquiring a multistage module. Since, with the use of an underlying Series 1000 hotplate/stirrer (*Jenway*) to provide forced ambient temperature to the Peltier cell cold-side (see p.172), reasonable temperature cycling could be achieved, it was decided not to buy a multistage module.

The chosen Peltier cells were a CP 1.0-127-05L and a CP 1.4-127-045L (*Melcor*). The CP 1.0-127-05L provided a useful 30x30 mm^2 area to heat the main reservoir area with 33.4W heat transfer rate and a maximum temperature differential of 67 °C, while the CP 1.4-127-045L offered a 40x40 mm^2 area to hold the whole chip and heat/cool it with 72W heat transfer rate and also 67 °C of maximum temperature differential. The properties of both types of cells are listed below:

Cell type	I_{max} (A)	at T_H= 25 °C			N	Dimensions (mm)		
		Q_{max} (W)	V_{max} (V)	dT_{max} (°C)		X	Y	Z
CP 1.0-127-05L	3.9	33.4	15.40	67	127	30	30	3.2
CP 1.4-127-045L	8.5	72	15.4	67	127	40	40	3.3

Table 24 - Peltier cell datasheet. Source: *Melcor, Inc.*

Characterization

Prior to use, Peltier cells were characterized using a FAC-304 ±15 V 1 A dual power supply (*Promax*) and a custom made heat dissipater. Figure 173 shows characterization for a previously bought CP-1.4-71-06L Peltier cell (*Melcor*).
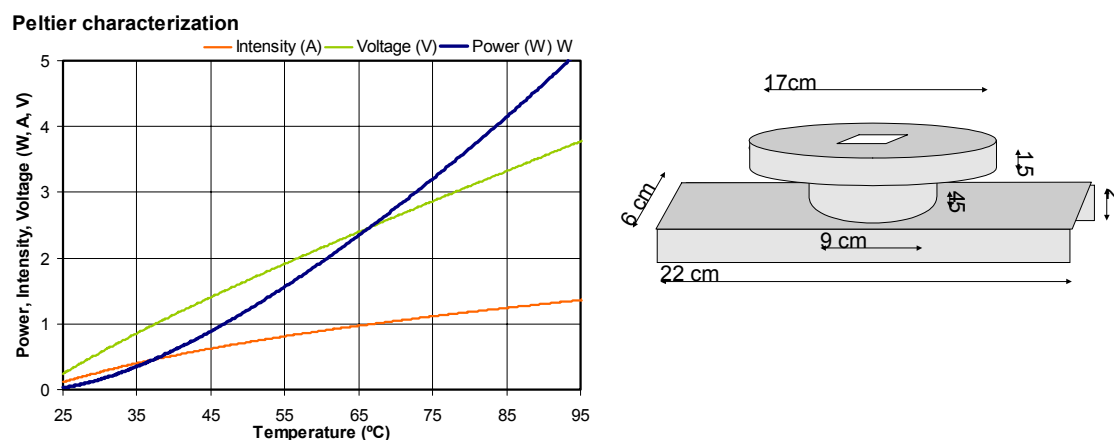

Figure 173 - Peltier cell characterization graph (for a CP-1.4-71-06L cell) and the custom steel dissipater setup.