III. Two approaches of flexural mode resonators: Out-of-plane and in-plane vibrating resonators

The performance and, more generally, the response of a nano/micromechanical resonator embedded in a capacitive readout system depends much on how the configuration of Figure 9 is realized in practice. Considering only resonators operated in their fundamental flexural mode, we identify two cases of study with very distinct electrical responses: out-of-plane and in-plane vibration devices.

It must be clearly stated that in terms of mechanical behavior, there is absolutely no difference in the theoretical treatment between both categories. The single but very significant difference concerns the electrical response because those two types of devices are affected in a very different way by parasitic capacitances.

III.1. Out-of-plane flexion mode resonators

With the aim of selecting a type of resonating device to undertake its fabrication and its electrical test to subsequently implement it as mass sensor, three types of silicon resonators operated in the fundamental out-of-plane flexural mode are compared in terms of electrical response and mass sensitivity [36].

Cantilevers (Figure 3), bridges (Figure 4) (common structures used for mass sensing [37, 38]) and quad-beam resonators (Figure 5) are studied hereafter.

III.1.a. Comparison in terms of electrical response of three discrete devices with simplified RLC model

The goal is to compare the electrical response of those three devices in a capacitive readout scheme. For this purpose, the electrical figure of merit *FM* defined in section II.2.c (page 59) is used. *FM* must be adapted to the specific case of out-of-plane flexion resonators:

$$\boldsymbol{FM} = 100\frac{\boldsymbol{i}_{M}}{\boldsymbol{i}_{P}+\boldsymbol{i}_{W}} = 100\frac{\boldsymbol{Q}\,\varepsilon_0^{\,2}\,\boldsymbol{A}^2\,\boldsymbol{V}_{IN\,DC}^{\;\;2}}{\boldsymbol{d}^4\left(\boldsymbol{C}_P+\boldsymbol{C}_W\right)}\frac{1}{\boldsymbol{k}}$$

- actuation is performed by applying a voltage (AC+DC) between resonator and substrate, that acts as driving electrode
- C_P is the capacitance related to the physical capacitor Si/SiO_2/Si formed between resonators anchors, lines and pads, and substrate. Its gap is d (i.e. SiO_2 thickness)
- C_W is the static capacitance related to the physical capacitor formed between the resonator area, the air and the substrate (modeled as parallel finite plates with a constant gap d equal to the sacrificial SiO_2 layer thickness).

For device specific *FM* calculation (k depends upon the type of structure), useful expressions are reported in Table II - 6:

	Cantilever	Bridge	Quad beam (*)
f_0 resonance frequency of the first out-of-plane flexion mode	$\frac{1.015}{2\pi}\sqrt{\frac{E}{\rho}}\frac{h}{l^2}$	$\frac{6.5}{2\pi}\sqrt{\frac{E}{\rho}}\frac{h}{l^2}$	$\frac{\sqrt{\lambda_{QB}}}{2\pi}\sqrt{\frac{E}{\rho}}\frac{h\,b^{0.5}}{l^{1.5}L_1}$
FM with $\left\{\gamma=\frac{Q\,\varepsilon o^2 V_{IN\,DC}^2}{(C_P+C_W)d^4 E h^3}\right\}$	$\frac{3}{2}\gamma l^5 b$	$\frac{1}{32}\gamma l^5 b$	$\frac{1}{\lambda_{QB}}\gamma\frac{L_1^4 l^3}{b}$
Punctual: $\alpha_{1_P}=m_{EFF}/m_{RESONATOR}$	0.24	0.379	1
k_{EFF_P} spring constant for punctual mass loading at the free end	$\frac{1}{4}\frac{E h^3 b}{l^3}$	$16\frac{E h^3 b}{l^3}$	$\lambda_{QB}\frac{E h^3 b}{l^3}$
S (g.Hz^{-1})	$\left(\frac{4\pi\alpha_{1_P}}{1.015}\frac{\rho^{3/2}}{E^{1/2}}\right)l^3 b$	$\left(\frac{4\pi\alpha_{1_P}}{6.5}\frac{\rho^{3/2}}{E^{1/2}}\right)l^3 b$	$\left(\frac{4\pi\alpha_{1_P}}{\sqrt{\lambda_{QB}}}\frac{\rho^{3/2}}{E^{1/2}}\right)\frac{L_1^3 l^{1.5}}{b^{0.5}}$
Distributed: $\alpha_{1_A}=m_{EFF}/m_{RESONATOR}$	0.65	0.757	1
k_{EFF_A} spring constant for uniform force distribution	$\frac{2}{3}\frac{E h^3 b}{l^3}$	$32\frac{E h^3 b}{l^3}$	$\alpha_{QB}\frac{E h^3 b}{l^3}$
S_D (g·cm^{-2}·Hz^{-1})	$\left(\frac{4\pi}{1.015}\frac{\rho^{3/2}}{E^{1/2}}\right)l^2$	$\left(\frac{4\pi}{6.5}\frac{\rho^{3/2}}{E^{1/2}}\right)l^2$	$\left(\frac{4\pi}{\sqrt{\alpha_{QB}}}\frac{\rho^{3/2}}{E^{1/2}}\right)\frac{L_1 l^{1.5}}{b^{0.5}}$

Table II - 6. Basic equations used to compare quantitatively three kinds of electrostatically actuated and detected resonators implemented as mass sensors, where b is the beam width, h the beam thickness, l the beam length, L_1 the QB plate width, E the Young modulus and ρ the density of the structural material.

In Figure 16, *FM* has been plotted as a function of the characteristic length of the device (defined as the most varying parameter, see Table II - 6): for bridges and cantilevers this is their length l; for QB this the plate width L_1. The rest of parameters is: constant thickness (h = 600 nm), beam width (b = 0.5 µm) and gap (d = 0.8µm). A Q-factor equal to 20 for all devices is considered (corresponding to ambient conditions in air). QB are DC biased with 50 V, bridges and cantilevers with 20 V: these voltages are below the pull-in voltage threshold. The spring-softening effect lowering the resonance frequency is neglected. To calculate the spring constant inside the *FM* formula, we have considered a uniform electrostatic force (see Table II - 6).

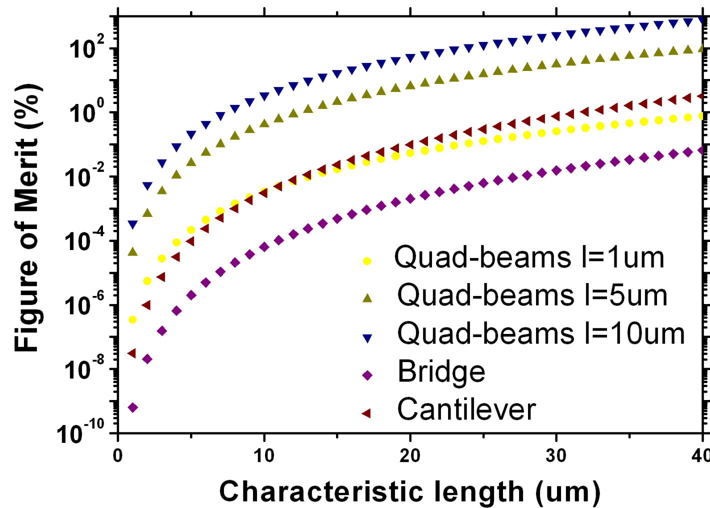

Figure 16. Electrical figure of merit (FM) in air for three kinds of resonators for b=0.5 µm, h=600 nm as a function of the characteristic dimension.

It is seen that the QB resonator exhibits increasing *FM* according as its arms increase in length. Among those three out-of-plane vibrating devices, this is probably the most appropriate one in terms of electrical response for an operation in air (i.e. low Q and high R_M).

III.1.b. Comparison in terms of mass sensitivity (punctual and distributed)

In this section, we compare the mass sensing attributes of the three devices for punctual and distributed mass accretions.

III.1.b.i) Punctual mass sensitivity

We study the case of masses deposited at the point of highest deflection (mid-point for bridges, free end for cantilevers and central plate for QB). The punctual mass sensitivity S is calculated from eq.(II.46) and plotted in Figure 17 as a function of l and L_1 (characteristic length of each device) for the same conditions of Figure 16. k_{EFF_P} and m_{EFF_P} get specific coefficients reported in Table II - 6, in the grey zone.

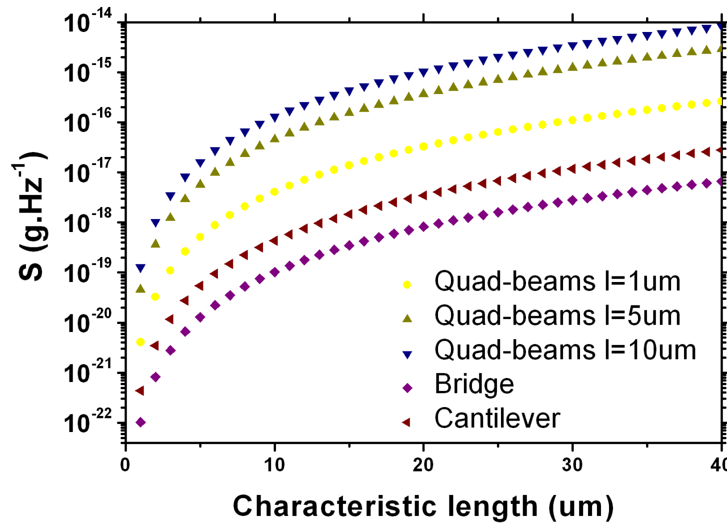

Figure 17. Punctual mass sensitivity for three kinds of resonators for b=0.5 µm, h=600 nm as a function of the characteristic dimension.

This graph shows that the bridge is the most sensitive, about one order of magnitude better than the cantilever. Concerning QB, they are about three orders of magnitude less sensitive than cantilevers, however they have a bigger active area what can be convenient for the deposition of the target adsorbate.

III.1.b.ii) Distributed mass sensitivity

Distributed (or areal) mass sensing is another application of a mass sensor. This is the field of quartz-crystal microbalances, generally implemented as mass rate sensors to monitor the thickness of thin layers deposited inside commercial evaporation chambers: they represent a reliable tool for this purpose but have a very poor punctual mass sensitivity.

Applying equation (II.50) to those three structures, we calculate the distributed mass sensitivity S_A. Additionally, we find that for any kind of flexural out-of-plane vibrating structure, the following quantity is constant:

$$\frac{f\,S_A}{h} = 2\rho \tag{II.83}$$

where ρ is the resonator structural layer density and h its thickness. Therefore, for a given thickness, the higher the resonance frequency, the better is the sensitivity.

Based on formulas of Table II - 6, we have plotted S_A (distributed mass sensitivity) in Figure 18 as a function of l and L_l (characteristic length of each device) for the same conditions of Figure 16:

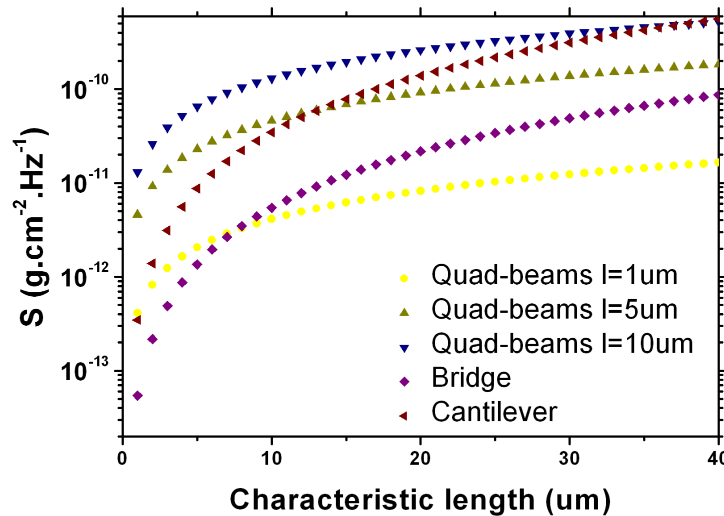

Figure 18. Distributed mass sensitivity for three kinds of resonators for b=0.5 µm, h=600 nm as a function of the characteristic dimension.

Globally, only the bridge differentiates notably from the other devices: it is between one and two orders of magnitude better in terms of distributed mass sensitivity.

However, the bridge has the poorest electrical response. A trade-off between reasonably high electrical response and sensitivity must be found in function of the targeted sensitivity of the mass measurement.

III.1.c. Analysis of the quad-beams device

Among the three devices that have just been presented, the QB resonator exhibits the highest electrical response and is therefore the most convenient device regarding the detection aspect. This is why our study of out-of-plane flexion devices will now be exclusively focused on it. For mass sensing purposes, this is also an interesting device as its large active area (i.e. the central plate) makes more convenient the punctual deposition of a target specie.

Hereafter, a simplified electromechanical model is developed for qualitative estimation of the resonance signal as a function of geometrical dimensions, materials and device polarization.

III.1.c.i) Electromechanical modeling

Neglecting air damping and any other type of loss, the resonance frequency of the first out-of-plane flexural mode is approximately given (see Table II - 6) by:

$$f_1 = \frac{\sqrt{\lambda_{QB}}}{2\pi}\sqrt{\frac{E}{\rho}\frac{hb^{0.5}}{l^{1.5}L_1}} \tag{II.84}$$

where E and ρ are the Young modulus and the density of the material. b and h are the beam width and the thickness of the device (see next figure). λ_{QB} stands as a corrective empiric factor to maintain the resonance frequency under such a form that makes its manipulation easier for simple electromechanical calculations.

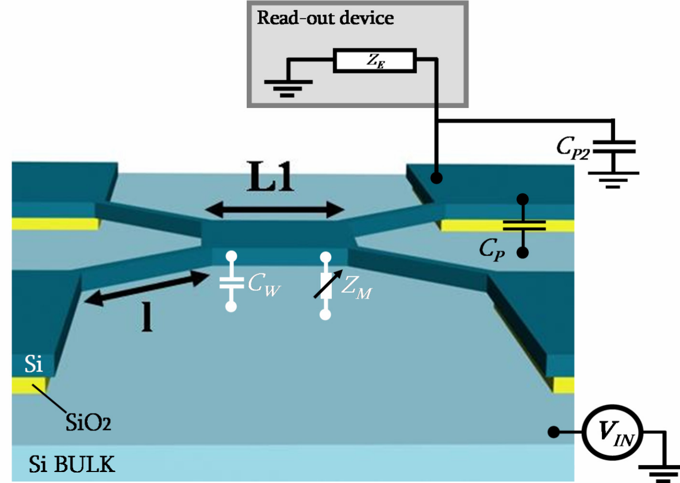

Figure 19. QB geometrical dimensions and characteristic impedances in a capacitive readout scheme

Figure 19 is a specific implementation of out-of-plane vibrating QB in a capacitive detection system. Let us discuss the meaning and the typical value of each parameter:

- C_P (parallel parasitic capacitance) and C_W (parallel static capacitance) have been defined already (section III.1.a)
- At resonance, the motional impedance Z_M can be assimilated to R_M, a simple resistance whose general value is given by eq.(II.69). In this specific case, the detail of R_M is:

$$R_m = \frac{\sqrt{\lambda_{QB}}\, d^4 \rho^{0.5} E^{0.5}}{\varepsilon_0^2 Q V_{IN\,DC}^2}\frac{b^{0.5}h^2}{L_1^3 l^{1.5}} \tag{II.85}$$

- C_{P2} is associated to the measurement instrumentation (coaxial cables, etc…), therefore it does not depend on the resonator shape and dimensions. It contributes to attenuate the available output level of resonance signal.
- Z_E is the input impedance of the readout device. For the measurement of discrete devices, a network analyzer (see next section III.1.c.iii)) is implemented (input impedance adjustable to 50 or 1MΩ).

Considering eq.(II.85) of motional impedance, it appears that the most decisive parameters for increasing the level of resonance motional current are L_1 (that should be increased) and h (that should be decreased). In parallel, considering the electrical FM (eq.(II.73)), basically C_P should be lowered. Regarding this objective, one should notice that it does not depend on the resonator

shape but is only related to the anchor and contact pads area. Consequently, special efforts in terms of device design should focus on reducing this area.

The most significant features of this system are:

- for dimensions in the micron and submicron range (b in the submicron range, 10 μm range for L_1 and l), R_M is high [1-100MΩ range] and always between one and two orders of magnitude larger than the impedance associated to C_P.

  Consequently, the resonance motional current ($i_M = V_{IN\,AC} / R_M$) never dominates over the two other parallel branches ($R_M // C_W // C_P$).
- based on these statements and on results of section II.2.b.i), we can therefore expect from QB a poor phase peak around resonance and a resonance current magnitude systematically 'sunk' in a high background signal (mostly related to C_P, while C_W plays a minor role).
- however, QB may achieve lower R_M than other devices like cantilevers or bridges, between other reasons because they can endure much higher polarization voltages since the pull-in voltage threshold is higher.
- CMOS integration would not improve the *FM* (defined between the three branches contributions), however more signal would be collected because of the decrease of C_{P2} and an improvement of SNR (signal to noise ratio) would be achieved.

As a conclusion, out-of-plane vibrating flexural quad-beams embedded in a capacitive detection scheme offer contrasted features: (i) high levels of resonance current are obtained owing to potentially low R_M but (ii) this resonance signal is poorly differentiated with respect to a high intrinsic background signal (low *FM*), that is related to stray parasitic capacitances originated by QB anchors.

III.1.c.ii) Fabrication of discrete devices: e-beam lithography on SOI

As a preparatory step before the CMOS integration, discrete (i.e. on bare wafers without CMOS circuitry) quad-beams devices have been fabricated using a technological process based on standard silicon surface micromachining using silicon-on-insulator (SOI) wafers. The thickness of the SOI layer is 1.5 μm, the thickness of the SiO_2 is 1 μm. Pads and anchors areas have been minimized in order to decrease physical parasitic capacitances (see previous section): device routing and contact pads are solely realized with silicon.

Therefore, for the whole process, a single lithography step is required. We have used electron beam lithography: first to be able to define submicron patterns, second because of its flexibility for prototyping new devices. The lithography is followed by a lift-off process of aluminum optimized for nanometer scale features. Al is used as mask for the subsequent reactive ion etching (RIE) of Si because of its excellent selectivity with respect to Si even for very thin layers (24 nm) what makes the lift-off process easier. Then, QB plates and beams are released by selective wet under-etching of SiO_2 in HF.

Hereafter, all process steps are detailed. Figure 20 shows scanning electron micrographs of mechanical resonators at the end of the process. The right image reveals that the mechanical structure is successfully released from the substrate:

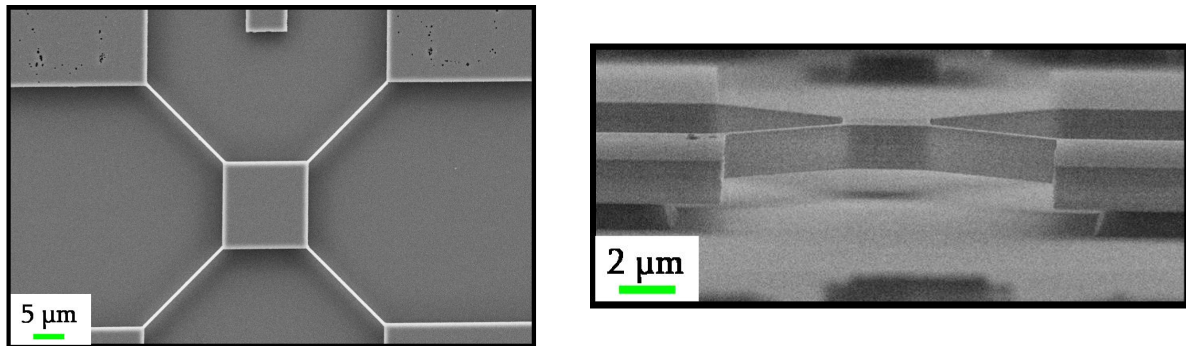

Figure 20. Scanning electron micrographs (left: top view; right: tilted view) of a mono crystalline Si quad-beam resonator fabricated by surface micromachining of a SOI wafer

WAFER DOPING

First, the monocrystalline Si upper layer n doped ($N_d \approx 10^{18}$ at·cm^{-3}) at wafer level.

- **Step 1.** n-type doping per diffusion of $POCl_3$
  Recipe: OPOC4800 (T3), 18 min at 950°C in order to dope superficially 480 nm of Si
- **Step 2.** Wet etching of PSG (Phospho-Silicate-Glass) (this particular type of Si oxide forms at the Si surface because of doping impurities during diffusion).
  Recipe: QDPSGC25 (AC 5/2)
- **Step 3.** Activation of P doping atoms.
  First, Si surface oxidation at 1100°C to impede posterior exodiffusion of impurities
  Second, annealing at 1000°C under N_2.
  Recipe: O&R-ESP (T1 or T8)
- **Step 4.** Removal of thermal Si oxide formed during previous step.
  Wet etching to remove a 70 nm thick Si oxide. Overetching to make the process surer
  Recipe: QDOXTXXX (AC 2/1)

At this step, the wafer is diced and we start working at chip level.

PMMA DEPOSITION

- **Step 1.** Cleaning in acetone, water, IPA and water. Drying with nitrogen spray
- **Step 2.** Dehydration. 30 min at 200°C
- **Step 3.** Spinner. v=1500 rpm; a=4500 rpm/s; 30 s with PMMA 950 KmW. (resulting in ~115 nm thick layer)
- **Step 4.** Post-bake. 30 min at 180°C in oven or 1 min at 180°C with a hot plate

E-BEAM LITHOGRAPHY STEP

System: Raith controller interfaced to a LEO SEM column

- **Step 1.** Exposure with an extraction voltage of 10 kV, aperture: 20 μm.
- **Step 2.** Development: MIBK (metilisobutilketona) : IPA [1:3], 30 s.
- **Step 3.** Rinsing in IPA, 30 s. Drying with nitrogen spray

METALLIZATION

System: Leybold-Heraeus Z-550 sputtering (Magnetron circular cathode type)
Recipe MZ550ING
Type of Al: Al/Cu 0.5% (Cu decreases Al electromigration in CMOS processes)

LIFT-OFF

- **Step 1.** 5 min immersion in heated acetone (40°C): heating makes PMMA lift off more easily
- **Step 2.** 5 min immersion in room temperature (RT) acetone with ultrasounds
- **Step 3.** 5 min immersion in IPA (RT) for cleaning
- **Step 4.** 5 min immersion in water with ultrasounds
- **Step 5.** Rinsing and drying

RIE (REACTIVE ION ETCHING) OF THE UPPER SI LAYER

- **Step 1.** Chamber conditioning.
  The chip is placed onto a bare Si carrier wafer. First, the system must be adequately conditioned: a bare Si wafer is etched with the etching recipe until it overpasses 10 minutes without having any reflected power pulse above 6 W.
  Once this step is completed, the sample is etched by proceeding with discrete steps of 14 s (equivalent to 4 cycles, one cycle representing the injection of the passivating gas C_4F_8 followed by the injection of the etching gas SF_6).The lateral overetching is around 50 nm for an etched depth of 1.3 µm.
- **Step 2.** Etching.
  System: Alcatel A601-E (recipe *Nano1*)
  t: 4 discontinued steps of 14 s (14 s are equivalent to 4 cycles of 3.5 s)
  C_4F_8: 100 sccm (1 s)
  SF_6: 150 sccm (2.5 s)
  Pressure: 1.4 – $2.8.10^{-2}$ mbar
  ICP Power: 1500 W
  Plate power: 15 W
  Nominal etching speed: 1300 nm/min at 20ºC

RELEASE ETCHING

Objective: wet etch in a controllable way the sacrificial buried SiO_2 layer in order to release the mechanical structures

Etchant: HF 49%
Etching velocity: ~ 1.6 µm/min. This value tends to decrease with old bottles.
Rinsing in water, drying with a critical point drying (CPD) system

III.1.c.iii) Measurement of discrete devices

Prototypes of discrete quad-beams resonators were measured in air. First, to enhance substrate polarization and to facilitate the electrical contact with a probe, we used a paintbrush to manually coat the surface around the resonators with a conductive Au-based resist. Through a manually controllable contact probe, an AC voltage (<10 V, provided by a network analyzer, AGILENT E5100A) summed to a DC voltage (50-100 V) by means of a bias tee (MINI-CIRCUITS ZFBT-4R2GW) are applied to the substrate.

The resonator layer is accessed via a contact pad using another probe connected to the network analyzer wherein the capacitive current produced by the resonator is converted into a voltage according to the adjustable input impedance (50 or 1 MΩ). Due to the MΩ range values of the resonator impedance around the resonance frequency, the allowed parasitic capacitance C_{P2} (Figure 9) at the output port is limited far below the pF range. In practice, C_{P2} is around 50 pF, equivalent to about 2 kΩ in the MHz range. Consequently an input impedance of 1 MΩ is

preferably employed so that 2 kΩ dominate at output (otherwise, 50 Ω would dominate resulting in a still worse transimpedance amplification of the current).

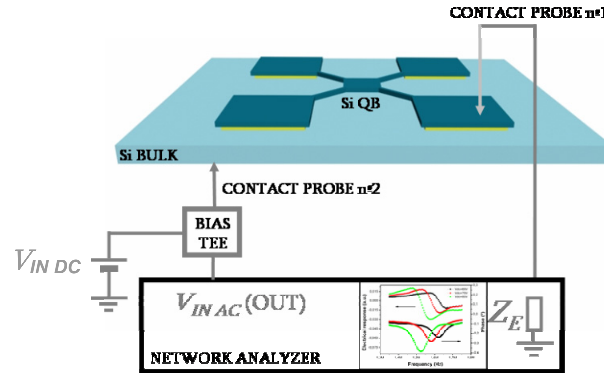

Figure 21. Measurement set-up of discrete QB resonators

The response in air of a QB (whose dimensions are: L_1=14 µm, l=18 µm, b=0.55 µm, h=1.5 µm) is depicted in Figure 22 for several values of $V_{IN\ DC}$:

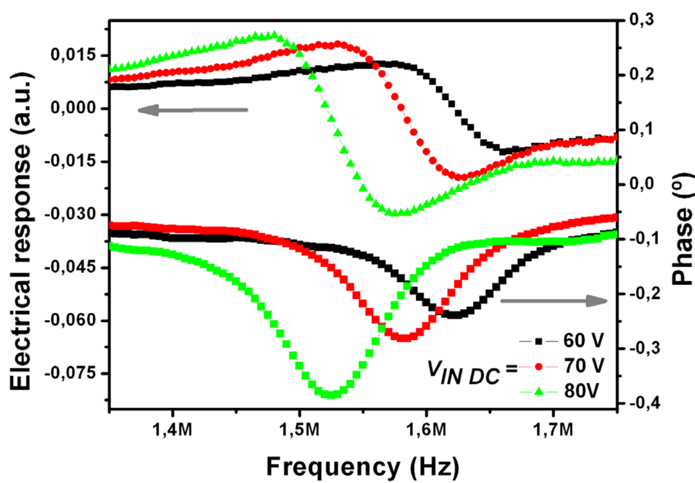

Figure 22. Resonance curves of a measurement in air for several applied dc voltages. They are obtained after calibration of the background signal with the network analyzer

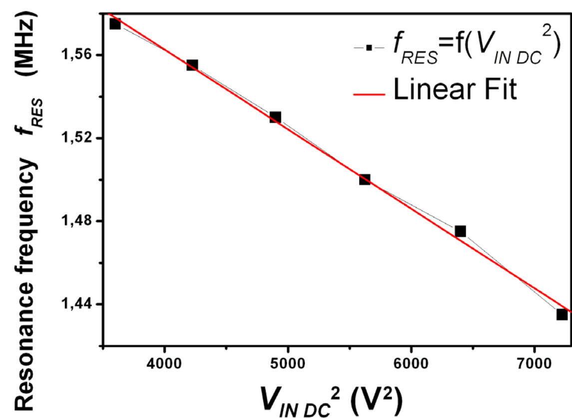

Figure 23. Experimental curve and linear fit of the voltage dependant resonance frequency as a function of the squared applied voltage ($V_{IN\ DC}^2$)

The amplitude spectrum exhibits one maximum and one minimum corresponding to resonance and anti-resonance respectively (see II.2.b.i)). The anti-resonance is related to parallel parasitic capacitances. In Figure 23, the evolving resonance frequency (i.e. amplitude maxima) is plotted as a function of $V_{IN\ DC}^2$ [eq.(II.82)], the natural resonance frequency f_0 is obtained by linear extrapolation (very conformal linear fit as expected from eq.(II.82)): its natural value (at $V_{IN\ DC}$=0) is found to be around 1.72 MHz. This is in good agreement with analytical mechanical calculations, based on Rayleigh-Ritz quotient (see Table II - 4, first row).

Yet, the resulting level of signal is very low because of the output low-pass filter created by the high parasitic output capacitance C_{P2} (around 50 pF). CMOS integration is expected to overcome this effect by decreasing the output parasitic capacitance down to around 10 – 50 fF.

III.2. In-plane flexion mode resonators. Cantilevers

With respect to out-of-plane vibrating resonators, in-plane vibrating flexural devices present a completely distinct electrical response, as it is going to be illustrated hereafter. We focus here exclusively on the cantilever design for two reasons: according to the previous comparative study (i) bridge resonators generate much less capacitive signal than cantilevers because of their superior stiffness and (ii) QB resonators cannot be easily integrated in-plane as 3D (or tricky 2D) lithography would be required to form non-planar beams.

Neglecting air damping and any other type of loss, the resonance frequency of the first in-plane flexural mode is given (see section I.2.b.i)) by:

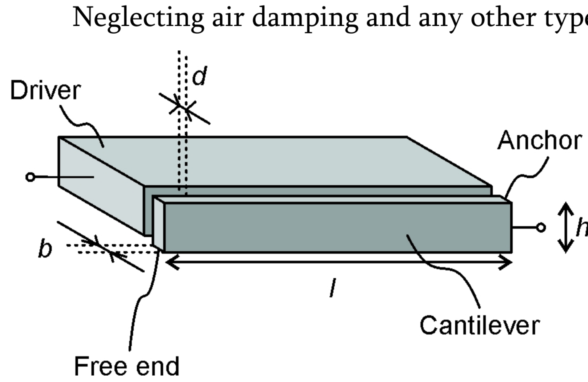

Figure 24. Cantilever geometrical dimensions

$$f_0 = \frac{1.015}{2\pi}\sqrt{\frac{E}{\rho}}\frac{b}{l^2} \tag{II.86}$$

where E and ρ stand for the Young modulus and the density of the structural material. b and l are the width and the length (see Figure 24).

Figure 25 is a specific implementation of in-plane vibrating cantilevers in a capacitive detection system. Let us discuss the meaning and the typical value of each parameter:

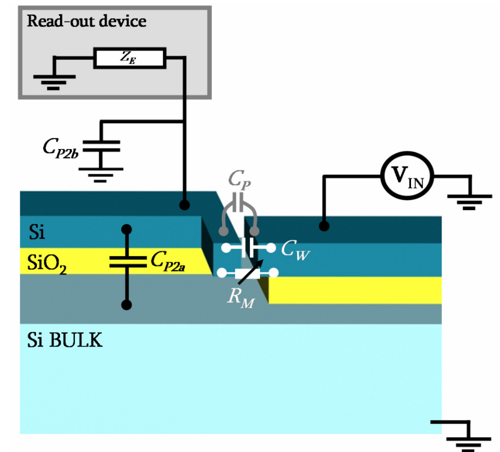

Figure 25. 3D view of an in-plane vibrating cantilever system. All main impedances are represented.

- C_P is called fringing field capacitance. It is associated to the three dimensional electric field between cantilever and front electrode. Its value is in the same order as C_W (it is calculated in chapter 5)
- C_W is the static capacitance related to the cantilever/air/electrode capacitor. A bias dependent corrective factor K [21], also named electromechanical coupling factor, is applied to take into account the bending of the cantilever (i.e. to correct the non-parallelism of the capacitor) when a DC voltage is applied:

$$C_W = (1 + K V_{IN\,DC}^2) C_0 \tag{II.87}$$

where $K = \frac{3\varepsilon_0 l^4}{4 E b^3 d^3}$ [see eq.(II.81)] assuming $V_{IN\,DC} >> V_{IN\,AC}$ and C_0 represents the static parallel capacitor: $C_0 = \frac{\varepsilon_0 h l}{d}$.

- At resonance, the motional impedance can be assimilated to a simple resistance R_M whose general value is given by eq.(II.69). In this specific case, a more accurate approach that takes into account the DC voltage-related static bending is followed [21]. This method starts by evaluating C_M (the motional capacitance), then L_M is deduced from the resonance frequency and C_M, and finally R_M is estimated from C_M and L_M (see eq.(II.69):

$$C_M = 1.798\, K\, V_{IN\,DC}^2\, C_0\,,\ L_M = \frac{1}{4\pi^2 f_{RES}^2 C_M}\text{, and } R_M = \frac{1}{Q}\sqrt{\frac{L_M}{C_M}} \qquad \text{(II.88)}$$

- C_{P2} is a sum of two contributions (see Figure 25) C_{P2a} and C_{P2b}. C_{P2a} corresponds to the physical capacitor between anchor and substrate. However, C_{P2b} associated to wiring (coaxial cables, etc…) dominates here. C_{P2} tends to attenuate the available output level of resonance signal.
- Z_E is the input impedance of the readout device.

The most significant features of this system are:

- for dimensions in the micron and submicron range (down to 100 nm), R_M is very high [10M-100MΩ range] but is of the same order of magnitude (and even smaller) than the impedance associated to C_W and/or C_P. Consequently, the motional current ($i_M = V_{IN\,AC} / R_M$) is the highest contribution of the three parallel branches ($R_M // C_W // C_P$) and is not sunk in a high background signal unlike QB.
- based on these statements and on results of section II.2.b.i), we can therefore expect from the cantilever much higher phase changes than the QB. This feature is very interesting regarding the possibility of a future insertion of the cantilever in a closed loop as self-oscillator.
- however, in-plane vibrating cantilever beams produce very low resonance signals, owing to their high R_M, which consequently are closer to the noise floor. The additional strong attenuation at resonator output (related to C_{P2}) makes even more difficult resonance measurements of discrete devices.
- in this sense, in-plane vibrating cantilever configuration would benefit much from a monolithic integration as C_{P2} would drastically be reduced.

As a conclusion, in-plane vibrating cantilevers embedded in a capacitive detection scheme also offer contrasted features: (i) low resonance signal levels are obtained, (ii) however, these resonance signals are not sunk in the background signal caused by parallel parasitic capacitances. Therefore, relatively high phase changes can be expected.

Conclusion of chapter 2

In this chapter, the mechanical and electrical behaviors of electrostatically actuated nano/microresonators (cantilevers, bridges and quad-beams) embedded in a capacitive detection scheme have been analytically analyzed. In parallel, methods to calculate the mass sensitivity of a nano/micromechanical resonator have been described.

A comparative study of in-plane and out-of-plane vibrating flexural resonators has been carried out. Although they have identical mechanical features except the direction of vibration, their electrical response differ much. This arises from the fact that in a capacitive detection scheme, parasitic parallel capacitances can drastically degrade the performance of the transduction.

In this sense, in-plane vibrating devices are much less affected than the out-of-plane ones since the driving and the readout electrodes are sufficiently decoupled: much higher amplitude and phase relative changes can be obtained with respect to the background signal. However, in practice in-plane vibrating resonators present reduced capacitive coupling areas what results in low absolute signal levels. Additionally, output parasitic capacitances related to the measurement instrumentation (wirings, etc...) can further reduce the available signal levels.

For this reason, the opportunity to integrate monolithically nano/micromechanical resonators on CMOS in order to detect the signal through a specific CMOS circuitry is studied in next chapter (nº3). Such integration should provide two relevant advantages: (i) reducing all the parasitic loads at the resonator output, and (ii) amplifying and conditioning ‘on-chip’ the resonance signal.

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CHAPTER 3

DEVICE MODELING AND IC DESIGN OF NANO/MICROMECHANICAL RESONATORS ON CMOS CIRCUITRY

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As a continuation of chapter 2, chapter 3 is focused on the monolithic integration of nano/micromechanical resonators on CMOS circuitry. The motivation and advantages are detailed in terms of device operation. Later, chapter 4 will be related to the fabrication process of M-NEMS/CMOS integrated systems.

As demonstrated in chapters 1 and 2, nano/micromechanical resonators have a strong interest mainly in two areas: as high sensitivity sensors [1, 2] and as building blocks for high frequency telecommunication systems [3-5]. Many practical applications of mechanical resonators require all electric actuation and detection methods whose smartest and most efficient implementation is monolithic integration with a CMOS circuit: this solution is optimum for 'on-chip' signal processing since parasitic capacitances are drastically reduced. The integrated circuit (IC), interfaced with the M/NEMS, efficiently collects the resonance signal and can subsequently amplify and condition it

Concerning sensing applications, several recent publications confirm that nanotechnology is becoming a promising approach to integrate both sensors [6-10] and actuators [11] in CMOS technologies.

On another hand, the semiconductor market exhibits an increasing demand on products for mobile applications, requiring in general very low-power and compact IC. In this sense, nanotechnologies also seem a suitable partner for CMOS circuits, since mechanical implementations of RF components may achieve larger power consumption savings and size reductions than their electronic counterparts. In particular, the possibility of using NEMS to replace the quartz crystal devices (as reference clock oscillator) is of high interest for the implementation of integrated oscillators [12, 13]. With respect to quartz devices, NEMS consume much less energy, offers outstanding perspectives of integration and are compatible with batch fabrication processes.

In this context, this chapter will start by the comparison in terms of electrical performance between discrete and integrated devices, and then a state-of-the-art of reported CMOS circuits for N-MEMS interfacing will be presented.

Specific CMOS circuits either for testing NEMS or for their interfacing within the final mixed electromechanical system-on-chip (SoC) need to be developed. Here, an approach is followed whereby electrostatic actuation and capacitive readout by an IC are used to detect the oscillations of the nanomechanical resonators. The RLC model presented in chapter 2 is implemented to predict the electrical response of nano/micromechanical resonators: the expected low signal levels in the range of nA and the required bandwidth in the MHz range imposed a series of challenging circuit specifications.

Thereby, a specific built-in low-power CMOS readout circuit [14] has been developed in the framework of this thesis and is presented hereafter. Its function is to interface NEMS resonators by collecting the motional current and to provide the frequency response in order to be able to detect the mechanical resonance frequency; more specifically the behavior of cantilevers and QB operated in in-plane and out-of-plane flexion respectively is studied. The IC architecture is inspired from second generation current conveyors (CCII). Circuit topology, layout and simulated response are detailed in this chapter.

I. Interest of monolithic integration with CMOS

Major enhancements in terms of device performance can be achieved by integrating nanomechanical structures with CMOS circuitry to form NEMS/CMOS systems. Following an all electric actuation and detection scheme (capacitive transduction), a monolithic integration provides a better readout of the output signal through a decrease of parasitic capacitances at NEMS output. This signal can subsequently be amplified and conditioned 'on chip'. This opens perspectives of closed loop operation as stand alone electromechanical oscillator. NEMS/CMOS devices also offer unique advantages in terms of compactness and packaging for portable applications like sensors or electronic devices (mobile phones, etc…).

I.1. Comparison integrated/discrete structures

Following the electrical modeling presented in chapter 2, the behavior of discrete and integrated cantilevers and QB is compared. Figure 1 sketches the equivalent electrical modeling of a nanomechanical resonator (cf. chapter 2, fig. 9), whereby the key elements are:

- Z_P, the parasitic impedance (related to parasitic capacitances C_P) and Z_W the 'static' impedance (related to the resonator static capacitance C_W)
- Z_M, the motional impedance, equivalent around the resonance frequency to a simple resistance R_M
- Z_{P2}, the NEMS output impedance (related to parasitic output capacitances C_{P2}).

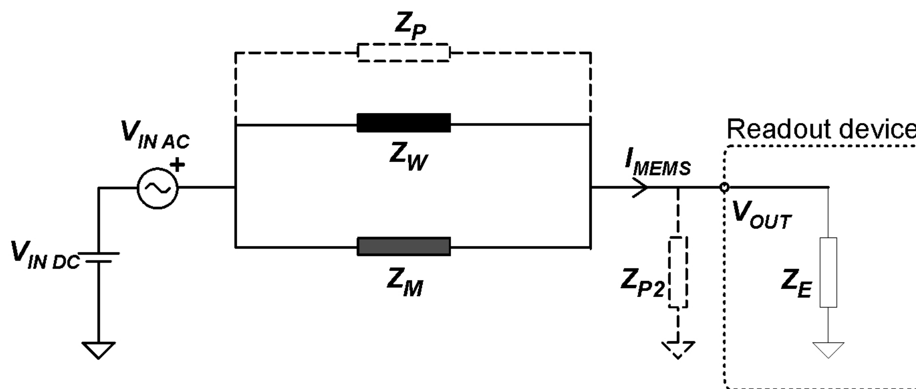

Figure 1. Equivalent electrical modeling of a nanomechanical resonator

Three criteria determine both the magnitude of the collected NEMS current (I_{MEMS}) and the relative contribution of the resonance current I_{RES} within I_{MEMS}:

- CRITERIA 1 the lower is R_M, the higher is the generated resonance signal (I_{RES})
- CRITERIA 2 the smaller is the ratio $\frac{R_M}{Z_P + Z_W}$ (= 1/*FM*), the larger is the ratio $\frac{I_{RES}}{I_{MEMS}}$ and better is the 'quality' of the resonance signal. Concretely, it means that higher amplitude peaks are obtained with respect to the background signal created by Z_P and Z_W. The same happens concerning the phase: more significant phase peaks (phase changes) are generated (c.f. chapter 2).

- CRITERIA 3 the higher is Z_{P2} (e.g. the smaller are the output capacitances), the higher is the available resonance signal for the readout device, in other words the lower are the losses.

Criteria 1 and 2 are intrinsic to a NEMS structure and do not depend on whether it is discrete or integrated.

From previous studies, it states that in-plane vibrating cantilevers are limited by criteria 1 (high R_M) and produce very low signals. However, the motional signal (the interesting one) is equal or bigger than the parallel parasitic ones, what makes that criteria 2 is fully satisfied.

Concerning quad-beams, the situation is reversed: criteria 1 is correctly satisfied while their response to criteria 2 is very poor, possibly complicating irreversibly an implementation of QB in closed loop operation, on the contrary to cantilevers.

Monolithic integration provides a drastic enhancement facing criteria 3, independently of the NEMS structure. The insertion of a built-in interface IC at the output electrode reduces C_{P2} $\left(= \frac{1}{\boldsymbol{Z}_{P2}\,\omega}\right)$ to a low capacitance physical capacitor formed by the routing between NEMS output electrode and IC input.

For discrete devices, C_{P2} is related to the measurement set-up (wire bonding, probe station, coaxial cables, etc…) and is in the order of tens of pF. For integrated, C_{P2} is in the order of tens of fF, what represents an improvement by three or four orders of magnitude. Therefore signal losses at NEMS output are almost nulled and the entire resonator current $\left(\boldsymbol{I}_{MEMS} = \boldsymbol{I}_{RES} + \boldsymbol{I}_{W} + \boldsymbol{I}_{P}\right)$ is collected for the readout through the IC.

As a conclusion, CMOS integrated NEMS ensures better transduction efficiency as more resonance signal is collected for subsequent readout due to the reduction of losses at NEMS output, and provided CMOS circuitry does not generate any additional noise, better SNR (signal to noise ratio) are consequently obtained.

I.2. State-of-the-art of circuit topologies

Monolithic integration of nano/micromechanical resonators with CMOS readout circuitry is more efficient in terms of transduction; however the global performance of the mixed NEMS-CMOS system depends on the type of readout IC. Different approaches have been reported in the literature to get to the result of electrically measuring the resonance frequency of nano/micromechanical resonators.

Circuit topologies depend on the type of transduction, mainly either capacitive or piezoresistive. The frequency of operation is also a relevant factor: very high frequency N-MEMS require more complex circuits, and signal transmission issues also perturb the readout process. Hereafter, a short survey of existing CMOS circuits for the readout of mechanical oscillations is presented.

Concerning piezoresistively sensed mechanical resonators, the integrated detection electronics is generally based on specific implementations of Wheatstone bridge. A solution relying on an off-chip high impedance buffer amplifier wire bonded to the sensor die has been proposed to measure the variation of resistance of an implanted piezoresistor in a half bridge scheme [15]. Regarding monolithic solutions, a chopper amplifier placed after a half bridge configuration has been used for low frequency devices [16-19] to circumvent the effect of 1/f noise as the signal is moved from low to the chopping frequency and amplified there.

An original approach consists in employing stressed transistors as deflection sensors [20]. Four diode-connected PMOS-transistors (acting as active loads) are used to sense the mechanical stress created by cantilever vibrations: orientating adequately four well-matched transistors, an 'on-resonator' Wheatstone bridge is formed where strained MOS channels play the role of resistors.

However, most examples of CMOS integrated resonators use capacitive transduction.

In [21], an integrated floating-electrode electric microgenerator is proposed. The mechanical motion of a metallic resonator creates charges in an in-front (permanently charged) insulated electrically floating fixed electrode working like a conventional non-volatile memory. This floating electrode is connected to the gate of a transistor acting as sensor for charge monitoring.

In [12, 22, 23] and [10], the current/voltage conversion is realized at resonator output, not inside the CMOS circuit. Indeed, the capacitive motional current is integrated through the parasitic capacitance formed by the parallel routing and intrinsic CMOS input capacitances. The resulting voltage passes through an unity gain differential pair, the output stage is a source follower. The DC input node voltage is controlled with a bias resistance in [12], with a PMOS transistor operated in the subthreshold region (high impedance is ensured so that no current flows in) in [10].

In [4, 13, 24-28], the motional current is converted to a voltage in the first stage of the circuit. In [4, 13, 24, 25], this operation is realized through the use of a low input impedance shunt-shunt feedback amplifier: the transimpedance gain is achieved by a nearly linear cross-coupled configuration [24] or using a MOS resistor [4, 13, 25].

In [24], an interesting solution is proposed to diminish the cross-talk of feed-through capacitances: differential signaling is put in practice through the simple analog subtraction of the currents arising both from the readout electrode and from an auxiliary electrode, non-movable and with the same feed-through capacitance.

In many cases, these CMOS circuits that amplify the motional current in a way or another actually make part of a closed loop MEMS/CMOS oscillator [4, 13, 26-28].

In this thesis, an original and new CMOS topology [14] is proposed based on a low input impedance second generation current conveyor (CCII)-based circuit that collects and amplifies the motional current. The current/voltage conversion is realized externally at circuit output by means of a load resistor.

II. Integration of NEMS on CMOS

In this section, a detailed description of our approach for the monolithic integration of NEMS resonators on CMOS is given. The guidelines for the choice of adequate geometrical dimensions for integrated cantilevers and QB are explained. Then, a new topology of interfacing CMOS readout circuit is presented: its schematic and layout are exposed. Its intrinsic behavior and its behavior when coupling it to the NEMS are discussed based on electrical simulations.

II.1. Design of CMOS integrated NEMS resonators

The maximum cut-off frequency permitted by CNM CMOS technology is limited to 5-10 MHz. As we will explain it in more details in chapter 4, this CMOS technology was selected for its flexibility in terms of fabrication (all process steps are well-known and may be slightly modified). The process strategy of integration is based on using existing layers of the CMOS as structural (polysilicon) and sacrificial (field SiO_2) layers.

Focusing this work on cantilevers and QB integration, their geometrical dimensions must be optimally chosen so that (i) their resonance frequency (that depends only on resonator dimensions and material) does not exceed a limit of 5 MHz (limitation caused by the technology), (ii) the electrical figure of merit (*FM*) is maximized and (iii) an areal mass sensitivity around 10^{-10} g.cm^{-2}.Hz^{-1} is provided for further mass sensing experiments. To get free of unavoidable deviations due to process fluctuations, the resonance frequency was limited to 1-2 MHz.

II.1.a. In-plane vibrating cantilevers

The vibration mode to be transduced is the first in-plane flexural mode. Considering a limitation in the resonance frequency of 2 MHz, cantilever length and width (l and b respectively) are the two parameters to be adjusted since polysilicon thickness has a fixed value determined by the technology ($h \approx 600$ nm) (see chapter 2, fig. 24).

Improving the electrical figure of merit (*FM*) can be achieved reducing b or increasing l. At the same time, l should be as short as possible (i) in order to increase the value of the pull-in voltage, (ii) shorter cantilevers are stiffer what makes them less sensitive to 'sticking' effect which may collapse them against their in-front electrode or against the underneath substrate during their release.

Concerning fabrication aspects, a demonstration of high nanopatterning resolution has been pursued (NaPa project, see chapter 4) therefore b has been chosen around 200 nm. In this context, length around 13 -14 µm enter the specifications in terms of resonance frequency.

II.1.b. Out-of-plane vibrating QB

The vibration mode to be transduced is the first out-of-plane flexural mode. According to table II.6, L_1, the plate width, is the key parameter governing the electrical *FM* while l, the beam length, is the key parameter governing the resonance frequency and the distributed mass sensitivity S_D.

l and L_1 have contrary effects, increasing L_1 will result in a better *FM*, however it will deteriorate S_D, and vice versa for l. Considering a limitation in the resonance frequency of 2 MHz,

the choice of l and L_1 is a trade-off between FM and S_D : the final values must be selected in function of the desired target, either a better electrical response or better sensing attributes. Regarding the beam width b, it does not influence much nor FM neither S_D, however it is kept in the submicron range due to the technology (test parameter of patterning resolution).

In this context, l and L_1 being both in the 10 μm range and b around 500 nm, the three aforementioned requirements are satisfied.

II.2. CCII CMOS circuit characteristics

A specific integrated capacitive readout system [14] is proposed for the electrical detection of the mechanical resonance. The proposed monolithic CMOS new implementation is based on a second generation current conveyor (CCII) circuit coupled to a NEMS resonator:

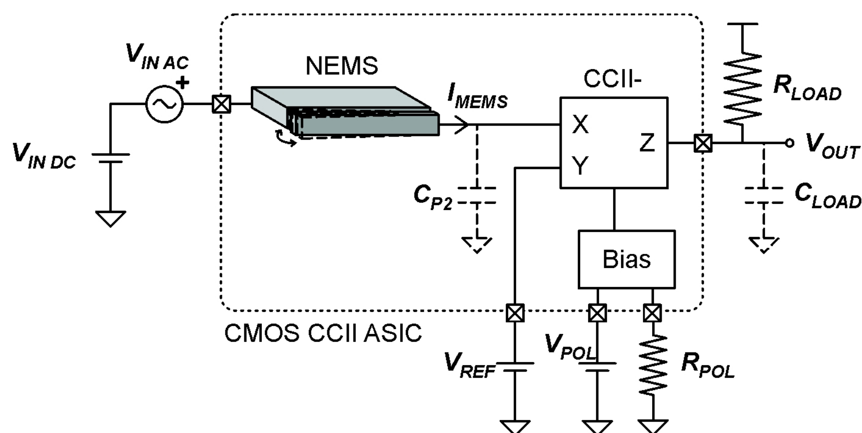

Figure 2. Proposed monolithic CMOS-NEMS system. Example of an in-plane vibrating cantilever

The nano/micromechanical resonator is electrostatically actuated by a DC+AC voltage. The readout electrode (i.e. the resonator anchor), electrically connected to the IC input, collects a capacitive current whose one part is specifically generated (see chapter 2) by the variation of electrode-resonator capacitance due to mechanical motion.

With the aim of reading out the output current of the resonator, a CMOS CCII is inserted at the output electrode. The circuit keeps a constant voltage at the NEMS output electrode (node X) according to the control electrode (node Y) and the monolithic integration ensures values of C_{P2} (parasitic capacitance determined by the routing) in the far sub-pF range. Furthermore, the CCII supplies flat spectral amplification of I_{MEMS} at the circuit output (node Z) for either external measurement at V_{OUT} or internal feedback for future implementations as stand-alone oscillator.

II.2.a. CCII Circuit topology

The CMOS interfacing circuit of Figure 2 must ensure a constant bias at the output of the NEMS so that the circuit input (node X) behaves like a low impedance node in order to readout its current like an ammeter. Its complementary function is to amplify it and convert it externally into a voltage according to a load resistor.

For this purpose, the compact CMOS circuit shown in Figure 3 is proposed (the complete schematic is given in annex A.6). Basically, it is a transimpedance amplifier (input in current, output in voltage) whose architecture is divided into two main blocks that consist of an input low-impedance stage (M1-M4) and an output current scaler (M5-12).

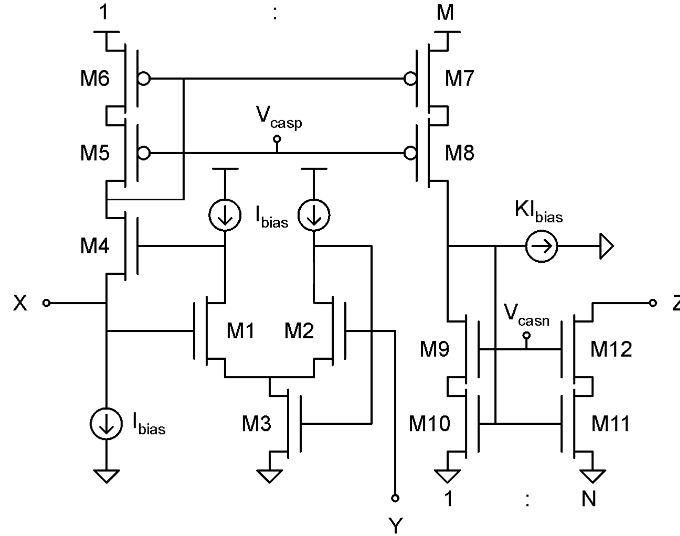

Figure 3. Simplified schematic of the CMOS CCII circuit

On one hand, the low-input impedance is achieved by the cascode transistor M4. Its gate is continuously regulated by the telescopic differential amplifier M1-M3, whose negative feedback tends to compensate any difference between V_X and V_Y. As a result, this input stage behaves like a voltage source V_X controlled by V_Y, sinking or sourcing the I_{MEMS} current demanded by the NEMS resonator. In this sense, the I_{MEMS} full scale that can drive the CCII-circuit from X is defined by its Class-A bias level I_{BIAS}. Class-A is optimum to maintain a good linearity and by reducing the complexity of the circuit, a smaller circuit area is obtained. The associated higher static consumption is not an issue here. According to the advanced EKV MOSFET model [29], the small-signal input resistance of this controlled voltage source is found to be:

$$r_{in} = \left(\frac{1}{n + \frac{gm_{g1}}{gm_{d1}}} \right) \frac{1}{gm_{g4}} \tag{III.1}$$

where n stands for the subthreshold slope factor, gm_{g1} for the gate transconductance of transistor M1, gm_{d1} for the drain transconductance of transistor M1, and gm_{g4} for the gate transconductance of transistor M4. Hence the error amplifier scales down r_{IN} by its gain factor $\frac{gm_{g1}}{gm_{d1}}$ compared to the impedance of the single M4 transistor $\frac{1}{gm_{g4}}$.

On the other hand, the NEMS current sensed by M4 is amplified by the geometrical scaling factors M and N of the two-stage cascode current mirrors M5-M8 and M9-12 biased at V_{CASP} and V_{CASN}, respectively. In order to reduce the overall power consumption, a K/M fraction of the biasing is subtracted before the second amplification stage.

In conclusion, the proposed circuit qualitatively behaves like a classic CCII- [30], but with an extra gain from the I_X to I_Z signals:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -MN & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{III.2}$$

In fact, the new CCII-topology introduced in Figure 3 is an improvement of the input stage of [31] in order to allow a wider voltage range for both V_X and V_Y thanks to the symmetry of the M1 and M2 drain connections. Also, compared to other CCII- evolutions like [32], the proposed circuit saves power consumption by minimizing the transistor count of the input stage.

Applying the circuit model (matrix (III.2)) to the general readout scheme of Figure 1, the following characteristics are obtained:

$$V_{OUT\,AC} = R_{LOAD}\, M\, N\, I_{MEMS} \tag{III.3}$$

$$V_X = V_{NEMS\,OUT} = V_{REF} \tag{III.4}$$

where $I_{MEMS} = I_{RES} + I_W + I_{PA}$ is the total MEMS current with the three contributions previously mentioned while $V_{NEMS\ OUT}$ stands for the DC voltage at resonator output.

Additionally, the DC output voltage is given by:

$$V_{OUT\,DC} = V_{DD} - R_{LOAD}\left[\left(M - K\right) N\, I_{BIAS}\right] \tag{III.5}$$

where I_{BIAS} is given in first approximation by:

$$I_{BIAS} \approx V_{POL} / R_{POL} \tag{III.6}$$

V_{POL} and R_{POL} are externally controllable through contact pads and are a DC voltage and a variable resistance respectively. In the next section, the calculation of I_{BIAS} is detailed.

The external output stage consisting of R_{LOAD} and C_{LOAD} represents a low-pass filter whose cut-off frequency is given by:

$$f_{MAX\,-3dB} = \frac{1}{2\pi\, R_{LOAD}\, C_{LOAD}} \tag{III.7}$$

From initial tests, an approximate value of 50 pF for the output parasitic capacitance C_{LOAD} (related to the probe station, PCB and coaxial cables) had been estimated and implemented in initial circuit simulations. Final experimental tests with fully fabricated samples yielded 30 pF. The corresponding maximum value for R_{LOAD} is 2.65 kΩ for a cut-off frequency of 2 MHz. This corresponds to a global transimpedance amplification of 2.65 10^5 (108.5 dB). For instance, an I_{MEMS} (NEMS AC current) of 10 nA would result in an AC output voltage of about 2.65 mV.

MOS transistors dimensions of this circuit implementation are listed in Table III - 1:

Transistor	α*W/L (µm/µm)
M1-2	4 * 30/5
M3	2 * 15/10
M4	30/3
M5-6	10/5
M7-8	M * 10/5
M9-10	50/5
M11-12	N * 50/5

Table III - 1. Transistor dimensions for the CCII circuit of Figure 3, where α, W and L stand for the device multiplicity, channel width and length, respectively

The resulting specifications for a CCII circuit fabricated with CNM CMOS technology are summarized in Table III - 2 for a typical set of values: I_{BIAS} = 10 μA, M = N = 10, K = 5, R_{LOAD} = 2.65 kΩ and C_{LOAD} = 30 pF.

	Specifications	Simulation results from layout extraction (including parasitic capacitors)
Technology	CNM25, 1 metal	-
Supply	0 - 5V	-
CMIR (Common Mode Input Range) for V_{REF}	[1.5 V – 2.5 V]	[1.3 V – 3 V]
Transimpedance	100 dB	108.5 dB
Bandwidth	≥ 1 MHz	2 MHz for R_{LOAD} =2.65 kΩ
In-band input impedance	as low as possible	< 3 kΩ
In-band input current noise	≤1 pA rms / √Hz	0.5 pA rms / √Hz
Current consumption	-	230 μA

Table III - 2. Initial circuit specifications and results of layout SPICE simulations

Concerning the range of AC input current, the inferior limit is set by the noise floor depending on the measurement bandwidth. The upper limit is reached when the output AC voltage saturates and loses symmetry. This can be avoided by decreasing adequately R_{LOAD}, actually an extreme case would be if R_{LOAD} =10 Ω, then the upper limit for I_{MEMS} would be in the order of a few mV (what represents between four and six orders of magnitude more than the expected signal levels).

ADDITIONAL FEATURE

A start-up p-type transistor has been placed within the transistor network that generates I_{BIAS}. This network consists of two crossed current mirrors that force the R_{POL} voltage node to the voltage of (externally controllable) V_{POL} node.

In this way, I_{BIAS} is generated according to eq.(III.6), flows in both branches and can thereby be replicated in any other parallel stages with a mirror.

Yet, a very hypothetic scenario (and alternative steady solution) is that no current flows in both branches. In this case, the source of the start-up transistor would be at V_{DD} =5 V and its gate at 0 V. In these conditions of polarization, the transistor would generate a current pulse that would switch on the circuit anyway.

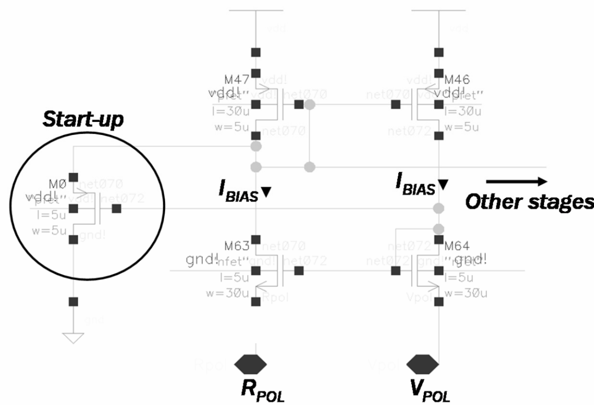

Figure 4. Transistors network generating I_{BIAS}. A start-up transistor is inserted to ensure a correct initialization

In normal steady state operation, this transistor is operated in its deep sub-threshold regime and no current flows into it.

II.2.b. CCII circuit performance

Simulations of the intrinsic frequency response of this new built-in CCII IC were performed with HSPICE under ICFB of CADENCE 4.46. The simulation cell is represented in Figure 5: at CCII input, an ideal current source is placed to substitute the NEMS output signal. A series of

parameters (R_{LOAD}, C_{LOAD}, R_{POL}, V_{POL} and V_{REF}) is adjustable so that the circuit can be fully characterized.

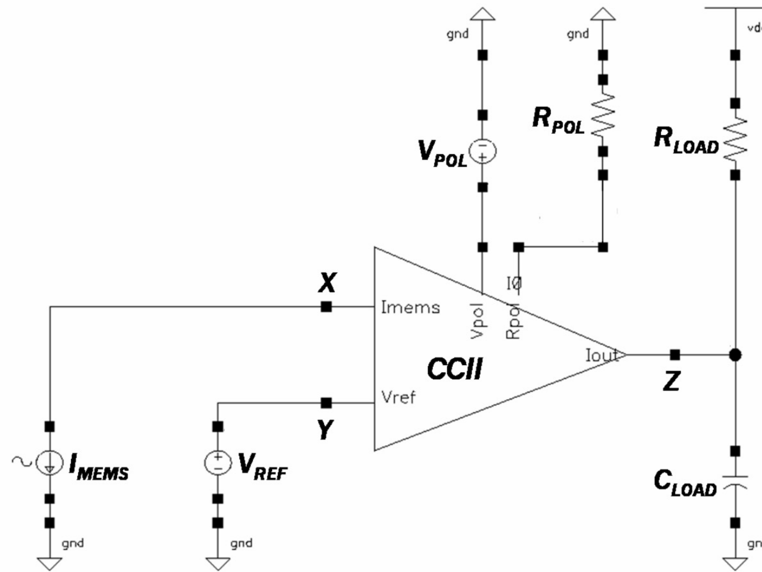

Figure 5. SPICE simulation cell for the characterization of the CCII response

Hereafter, an exhaustive analysis of the behavior of the CCII circuit is undertaken. DC simulations are made to determine the operating point and I_{BIAS} is calculated. AC simulations of the extracted layout (including physical parasitic capacitances) are made in order to study the influence on the frequency response of every externally adjustable parameter. Transient simulations are performed to check the functionality of the starter switch, and then the conditions of saturation and of linearity are determined. Finally, a brief noise analysis is proposed.

II.2.b.i) Determination of operation points (DC)

The DC behavior is investigated when V_{POL} and V_{REF} are set to the same value (what is realized in practice in experimental measurements), in particular the calculation of I_{BIAS} is addressed. According to Figure 4, the feedback loop (optimized for V_{POL} =1 V) forces the R_{POL} node to V_{POL} resulting in $I_{BIAS} = V_{POL}/R_{POL} = 1/R_{POL}$. However, if V_{POL} takes another value than 1 V, R_{POL} node is not completely forced to 1 V. The rigorous V_{POL} expression for I_{BIAS} is:

$$I_{BIAS} = \frac{V_{R_{POL}\,node}}{R_{POL}} \tag{III.8}$$

In the next table, the results of DC simulation for two values of R_{POL} are listed as a function of $V_{POL} = V_{REF}$. The resulting CCII input voltage (node X), the voltage at R_{POL} node and the resulting I_{BIAS} are given while the resultding DC output voltage is calculated according to eq.(III.5):

R_{POL} =200 kΩ

V_{REF}/ V_{POL} (V)	node X (V)	node R_{POL} (V)	I_{BIAS} (μA)	$V_{OUT\,DC}$ (V)
1	1.29	1	5	4.75
2	2	1.59	8	4.60
3	2.93	1.6	8	4.60

R_{POL} =1 MΩ

V_{REF}/ V_{POL} (V)	node X (V)	node R_{POL} (V)	I_{BIAS} (μA)	$V_{OUT\,DC}$ (V)
1	1	1	1	4.95
2	2	2	2	4.90
3	2.95	2.6	2.6	4.87

Table III - 3. Results of DC simulations for several V_{REF}-V_{POL} for a typical set of values for R_{LOAD} =1000 Ω

II.2.b.ii) AC response

In this section, the factors affecting the transimpedance gain $\left(G_{dB} = 20\log\frac{V_{OUT\,AC}}{I_{MEMS}} \right)$, the bandwidth and the circuit input impedance are studied. Simulations are performed with the following standard conditions:

Parameter	Value
R_{LOAD}	1 kΩ
C_{LOAD}	30 pF
R_{POL}	200 kΩ
V_{POL}	1 V
V_{REF}	2 V

Table III - 4. Standard simulations parameters

- Study of R_{LOAD} influence

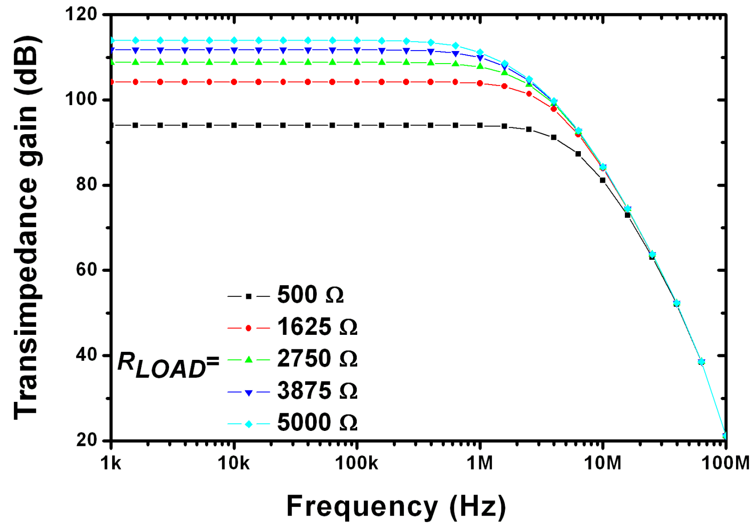

Figure 6. Bode diagram as a function of R_{LOAD}

The Bode diagram for several values of R_{LOAD} is depicted in Figure 6. As expected according to eq. (III.3) and (III.7), when R_{LOAD} increases the gain increases while the bandwidth decreases. In next table, the simulated cut-off frequencies and the calculated cut-off frequencies corresponding to the output low-pass $R_{LOAD}\,//\,C_{LOAD}$ filter are listed for a typical set of values:

R_{LOAD} (Ω)	$f_{MAX\,-3dB}$ (simul.) CCII (MHz)	$f_{MAX\,-3dB}$ of the filter R_{LOAD} // C_{LOAD} (MHz)
500	4.99	10.6
1625	2.88	3.26
2033	2.42	2.61
2750	1.88	1.93
3875	1.40	1.37
5000	1.07	1.06

Table III - 5. Simulation and calculated results of frequency response

Table III - 5 demonstrates that for C_{LOAD} = 30 pF, the low-pass filter is the limiting factor of the CCII bandwidth while R_{LOAD} > 2 kΩ, but at lower R_{LOAD} values, the limitation arises from an internal high impedance pole of the circuit itself, that is the drain of M1 (see Figure 3).

- Study of C_{LOAD} influence

The previous section revealed that the bandwidth is limited by an internal pole and above a critical value of R_{LOAD}, the bandwidth becomes limited by the $R_{LOAD}//C_{LOAD}$ output low-pass filter. Studying now the influence of C_{LOAD}, the analysis is consequently carried out for a low and a high value of R_{LOAD}: the incidence of C_{LOAD} is overviewed for realistic orders of magnitude from 1 to 100 pF. In Figure 7, the Bode diagram of the CCII circuit is depicted for R_{LOAD} = 700 Ω:

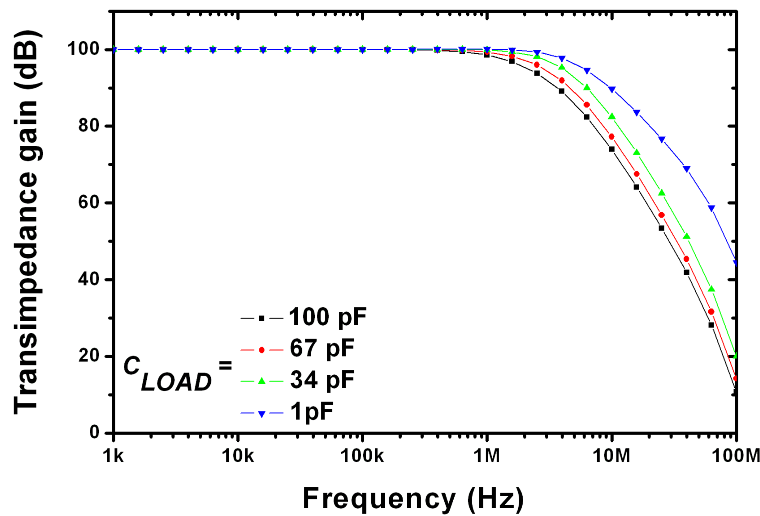

Figure 7. Bode diagram as a function of C_{LOAD}

From Figure 7, it is clear that C_{LOAD} has no influence on the transimpedance gain. This statement remains true independently of R_{LOAD}. Nevertheless, it logically acts as a parameter limiting the bandwidth (according to eq.(III.7)).

R_{LOAD} =700 Ω			R_{LOAD} =4000 Ω		
C_{LOAD} (F)	$f_{MAX\text{-}3dB}$ (simul.) CCII (MHz)	$f_{MAX\text{-}3dB}$ of filter $R_{LOAD}//C_{LOAD}$ (MHz)	C_{LOAD} (F)	$f_{MAX\text{-}3dB}$ (simul.) CCII (MHz)	$f_{MAX\text{-}3dB}$ of filter $R_{LOAD}//C_{LOAD}$ (MHz)
1p	5.896	227	1p	5.508	40
34p	4.281	6.69	34p	1.196	1.17
67p	2.959	3.39	67p	0.609	0.594
100p	2.176	2.27	100p	0.409	0.398

Table III - 6. Simulation and calculated results of CCII response

In Table III - 6, the simulated cut-off frequencies and the calculated cut-off frequencies corresponding to the output low-pass R_{LOAD}/C_{LOAD} filter are listed for two values of R_{LOAD}: 700 and 4000 Ω.

The results at low C_{LOAD} confirm the existence of an internal pole, which makes that the limiting factor of the cut-off frequency is not systematically the output RC filter.

- Study of R_{POL} (i.e. I_{BIAS}) influence

In next curve, the Bode diagram for several values of R_{POL} is plotted. Since R_{POL} governs I_{BIAS} through eq.(III.8), it is interesting to study its incidence on the speed of the circuit. More biasing current should likely decrease the commutation time of the transistors and enlarge the bandwidth.

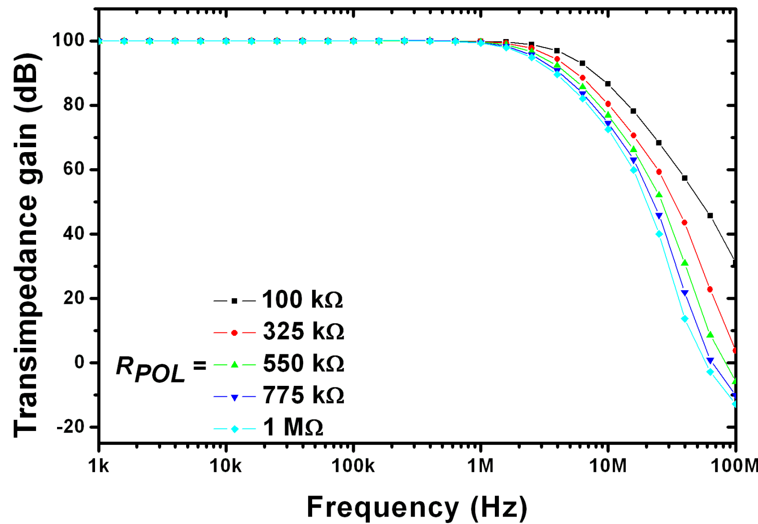

Figure 8. Bode diagram as a function of R_{POL}

Figure 8 confirms this assumption: by decreasing R_{POL} (i.e. increasing I_{BIAS}) the bandwidth can be increased. Physically, this corresponds to a faster charging of capacitance (analogy with the slew rate $SR=I\ /C$) when more current flows. As a conclusion, I_{BIAS} magnitude and circuit bandwidth follow the same trend.

- Input Impedance analysis

One of the required features of the CCII circuit is a low input impedance for an accurate current sensing (like an ammeter) as well as to decrease the influence of NEMS output capacitances.

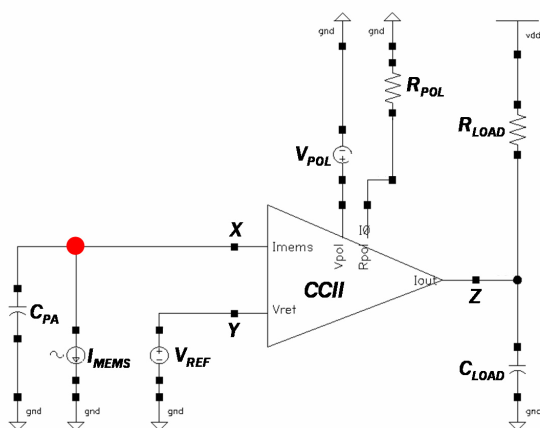

Figure 9. Input impedance test module

To estimate the input impedance, a parallel capacitance 'C_{PA}' is added at CCII input to simulate the presence of parasitic capacitances at NEMS output. Its influence on the circuit input impedance (Z_E) is analyzed.

For this purpose, simulations are performed with the test module of Figure 9 where C_{PA} is swept from 1 fF to 1 pF. I_{MEMS} AC amplitude is set to 1, hence $Z_E = V_X/I_{MEMS} = V_X$. Measuring V_X directly provides the value of Z_E.

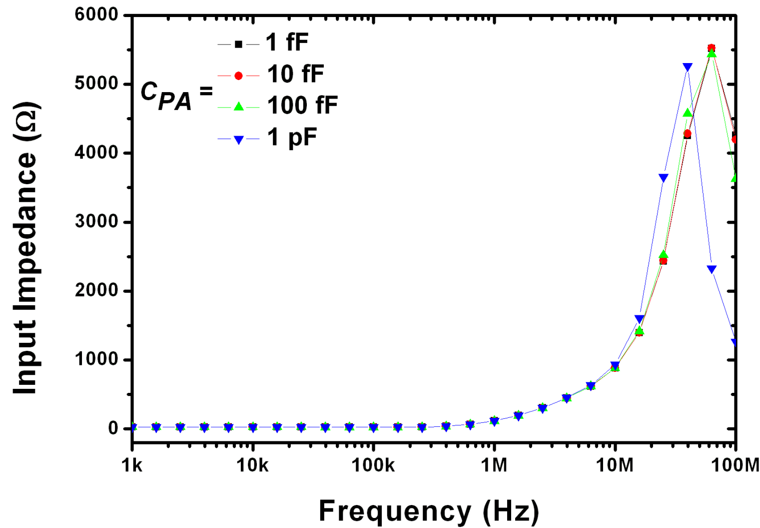

Figure 10. Input impedance (Z_E) (measured through V_X) versus frequency in function of C_{PA}

From this simulation, it is clear that in the 1-2 MHz range, the parallel parasitic capacitance has no influence on Z_E. In this frequency range, Z_E is in the order of 100-500 Ω. This range of value is satisfactory as it is sufficiently low:

- compared to the equivalent impedance of C_{PA2} which is in the range of the MΩ
- not to perturb the stability of the X node forced to V_{REF}. If I_{MEMS} was as high as 10 µA (extreme case), this would generate a fluctuation of about [10.10^{-6} * 500] = 5 mV what is still negligible compared to 2 V (typical value of V_{REF}).

II.2.b.iii) Transient simulations

In this section, the circuit initialization and its conditions of stability are investigated realizing transient simulations.

- **Transient analysis of circuit initialization**

It is necessary to check if the functionality of start-up mechanism, i.e. if the circuit will adequately switch on when polarizing V_{DD} and V_{SS}.

For this purpose, I_{MEMS} is set to 0. At t=0, V_{DD} =0. Then V_{DD} is progressively polarized with a ramp from 0 to 5V in 100 ns, and then a constant 5 V voltage is applied.

The initialization is measured through R_{POL} node voltage (red node), e.g. where I_{BIAS} is produced: as previously explained, two crossed current mirrors, depicted in Figure 4, are supposed to force this node to V_{POL} value (1 V here). If everything works correctly, this node must reach 1 V within some micro-seconds.

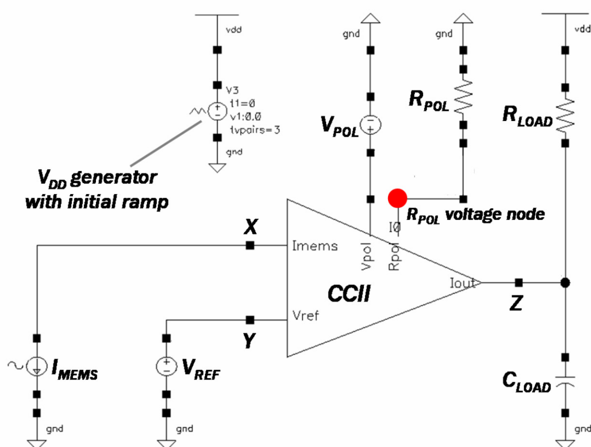

Figure 11. Initialization test module

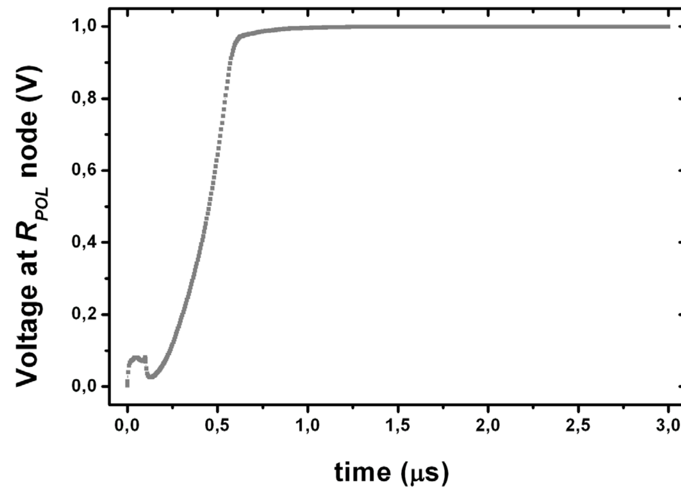

Figure 12. Transient analysis of circuit initialization. Voltage measurement at R_{POL} node versus time

According to this graph, the circuit initiates properly since R_{POL} node voltage reaches 1 V (= V_{POL}) after 0.8 μs. From this instant on, I_{BIAS} is constantly produced and the circuit is properly switched on.

- Analysis of circuit stability

The influence of the NEMS output parasitic capacitance (modeled here as an input capacitance C_{PA}) on the CCII stability is investigated for several C_{PA} values. Actually, the negative feedback loop constituted of M1 and M4 transistors (Figure 3) contains a high impedance pole at the drain of M1 (≡ gate of M4 and drain of another transistor generating I_{BIAS}). It represents in fact the second main pole of the CCII after the one consisting of the output low-pass RC filter. If C_{PA} increases, the frequency of the internal pole shifts down to lower frequencies and gets closer the main pole. The potentially insufficient phase margin can generate some instability materialized by unwanted oscillations. Actually this parasitic input capacitance is equivalent to C_{P2} in Figure 2: it is estimated around 50-100 fF, as a maximum, taking into account the anchor area and the routing area between resonator and CCII input.

To test this, a simulation module sketched in Figure 13 is built up. A parallel capacitance 'C_{PA}' is added at CCII input to simulate the NEMS output parasitic capacitances. A single step current is applied at I_{MEMS} source and the response at the output Z node is measured.

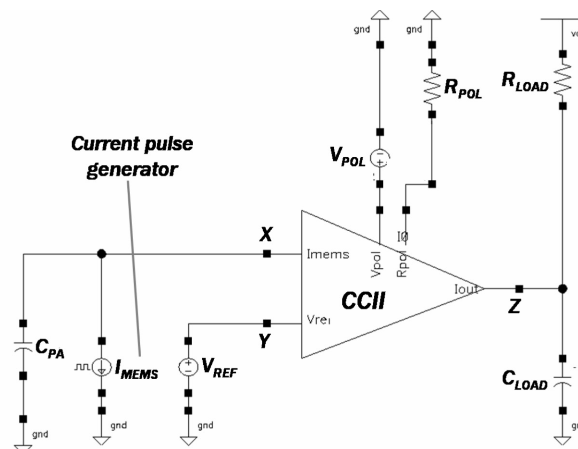

Figure 13. Stability test module

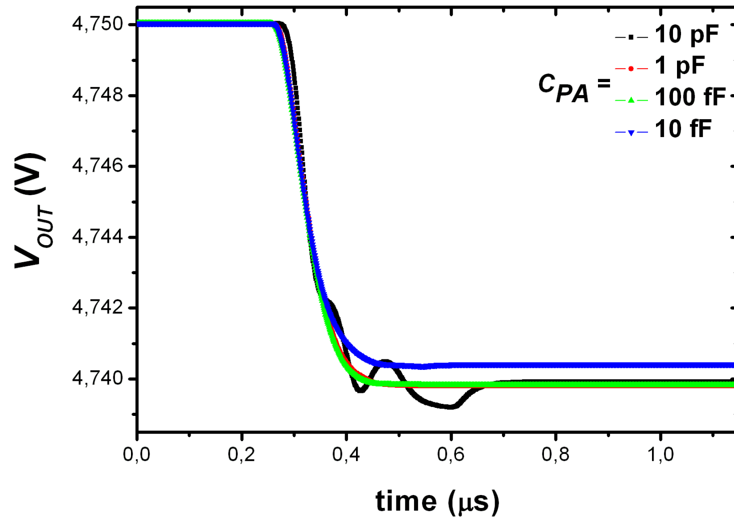

Figure 14. Transient analysis in function of C_{PA}. Output voltage versus time.

This graph indicates that for values of 10 fF and 100 fF, the system should be perfectly stable. However, for 1 pF, slight oscillations start to appear and from 10 pF on, the system is no more stable. If both poles get nearer, an overshoot peak should appear in the Bode diagram.

II.2.b.iv) Conditions of saturation

The conditions for circuit saturation can be derived mathematically. The results of this analytical approach have actually been confirmed by simulations.

The maximum value of the output AC peak-peak voltage ($V_{OUT\,AC\,pp})_{MAX}$ is limited by the DC output voltage offset $\Delta V_{OUT\,DC}$ generated by the amplification I_{BIAS} $\left(\Delta V_{OUT\,DC} = V_{DD} - V_{OUT\,DC}\right)$ (see eq.(III.5)). This can be described numerically as:

$$\left(V_{OUT\,AC\,pp}\right)_{MAX} / 2 = \Delta V_{OUT\,DC} \tag{III.9}$$

Expressing the left and the right term according to eq.(III.3) and (III.5), one can write:

$$\frac{\left(V_{OUT\,AC\,pp}\right)_{MAX}}{2} = 100\,R_{LOAD}\left[\frac{\left(I_{MEMS\,pp}\right)_{MAX}}{2}\right] \quad \text{and} \quad \Delta V_{OUT\,DC} = 50\,R_{LOAD}\,I_{BIAS} = 50\,R_{LOAD}\,\frac{V_{R_{POL}}}{R_{POL}} \tag{III.10}$$

what results in:

$$\left(I_{MEMS\,pp}\right)_{MAX} = I_{BIAS} = \frac{V_{R_{POL}}}{R_{POL}} \tag{III.11}$$

This means that the peak-peak magnitude of I_{MEMS} must be inferior or equal to I_{BIAS} to avoid any saturation of the output voltage.

II.2.b.v) Linearity of the circuit response

In order to further analyze the linearity of the response of the nano/micromechanical resonator, it is necessary to be able to decorrelate it from the linearity of the electrical response of

the circuit. In practice, if the circuit response is linear, any deviation in the electrical response of the resonator from a linear behavior can be attributed to its own mechanical behavior only and not to any electrical artifact. In this section, the linearity of the circuit is checked in the range of I_{MEMS} = 1 μV AC. Actually, a DC analysis is performed and the resulting output voltage is plotted in next figure for several values of R_{POL}. The output voltage is normalized to remove the DC offset that depends on the R_{POL} value (see eq.(III.5) and (III.8)).

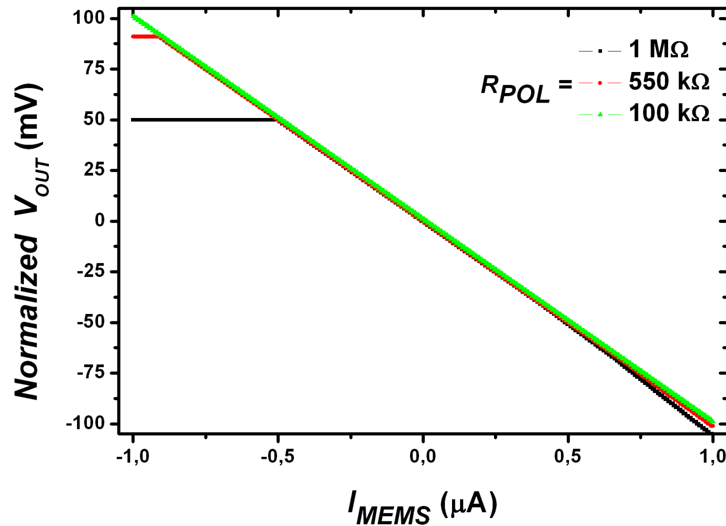

Figure 15. Output AC voltage versus I_{MEMS} for several R_{POL} values

This graph indicates that the response is very linear, particularly for values of R_{POL} inferior to 1 MΩ. The curves for R_{POL} = 550 kΩ and 1 MΩ exhibit plateaus in the output voltage for negative values of I_{MEMS}. This phenomenon is not related to any loss of linearity but to saturation effects according to eq.(III.11) (the observed saturation threshold is in perfect agreement with that equation). In fact, these two curves are normalized but if the DC offset had not been removed, a saturation at 5 V (V_{DD}) could be observed.

II.2.b.vi) Noise analysis

Based on simulations, a noise analysis is undertaken to evaluate the noise of the output voltage which is a combination of the global noise generated internally by the circuit itself and by the external load resistor (thermoelectrical noise called 'Nyquist and Johnson' noise). It comes that the spectral density of the output voltage noise is constant until 5 MHz, e.g. in all the bandwidth of the CCII circuit.

In Table III - 7 and Table III - 8, the spectral density is provided for different conditions of operation. Then, the resulting output voltage noise is given as function of the bandwidth of a 2 MHz mechanical resonator for two values of Q: 10 (like for a measurement in air) and 10000 (like for a measurement in vacuum). The resonator bandwidth is approximated as:

$$BW = \frac{f_0}{Q} \tag{III.12}$$

Let us define the voltage gain G_V as:

$$G_V = 20\log\left(\frac{V_{OUT\,AC}}{V_{IN\,AC}}\right) \tag{III.13}$$

these two tables also provide the resulting voltage gain G_V of the output voltage noise floor:

R_{POL} (Ω)	Density of output voltage noise D_{OVN} (nV / Hz$^{1/2}$)	BW(Hz) for f_0= 2 MHz	Output noise $V_{OUT\,AC}$ (µV)	G_V(dB) for $V_{IN\,AC}$ =1V
100 k	100	200 k (for Q=10)	45	-79
		200 (for Q=10000)	1.41	-109
1 M	55	200 k (for Q=10)	25	-84
		200 (for Q=10000)	0.8	-114

Table III - 7. Noise study for R_{LOAD} =1 kΩ

R_{LOAD} (Ω)	Density of output voltage noise D_{OVN} (nV / Hz$^{1/2}$)	BW(Hz) for f_0= 2 MHz	Output noise $V_{OUT\,AC}$ (µV)	G_V(dB) for $V_{IN\,AC}$ =1V
500	36	200 k (for Q=10)	16	-88
		200 (for Q=10000)	0.5	-118
1000	69	200 k (for Q=10)	31	-82
		200 (for Q=10000)	1.0	-112

Table III - 8. Noise study for R_{POL} = 200 kΩ

To reduce the noise, R_{POL} should be as high as possible: low values of R_{POL} result in more bias current what naturally generates more noise current. Depending on the measurement bandwidth, the total output noise varies from hundreds of nV to tens of µV.

On the opposite, the results of Table III - 8 reveal that the CCII circuit dominates over R_{LOAD} . In fact, the signal to noise ratio (SNR) is fixed within the circuit and the output noise current is converted by R_{LOAD} into an output voltage noise but it is not increased by the load resistor. Indeed, according to Table III - 8 the density of output voltage noise is proportional to R_{LOAD} . If R_{LOAD} was the dominant factor, it would create a 'Nyquist-Johnson' voltage noise which is in principle proportional to the square root of R_{LOAD} : this is not the case here. This means that the equivalent input noise is independent of R_{LOAD} .

II.2.c. CCII circuit performance with NEMS model at input

In chapter 2, it has been demonstrated that a mechanical resonator can be electrically modeled as an equivalent RLC component. The calculation of these electrical parameters opens up the possibility of performing electrical simulations of the cluster RESONATOR-CCII CIRCUIT. Simulations cells are built up where the NEMS device modeled by three parallel branches (c.f. chapter 2) replaces the ideal current source utilized in previous simulations.

Provided the RLC model is accurate, the experimental frequency response should be well predicted. In addition, it is necessary to check that the CCII circuit carries on working with a more realistic input device than an ideal current source.

II.2.c.i) Electrical simulations of cantilevers-CCII mixed circuit

Figure 16 is a scheme of the simulation cell of the mixed electromechanical system CANTILEVER-CCII CIRCUIT. Cantilevers are placed at CCII input and modeled by three branches (c.f. chapter 2). The first one contains the RLC components (called R_M, L_M and C_M in this schematic), the second the static capacitance C_{DC} (called C_W in chapter 2) and the third one the parallel parasitic capacitance C_{PA} (called C_P in chapter 2). The NEMS output parasitic capacitance is named C_{PA2} (called C_{P2} in chapter 2).

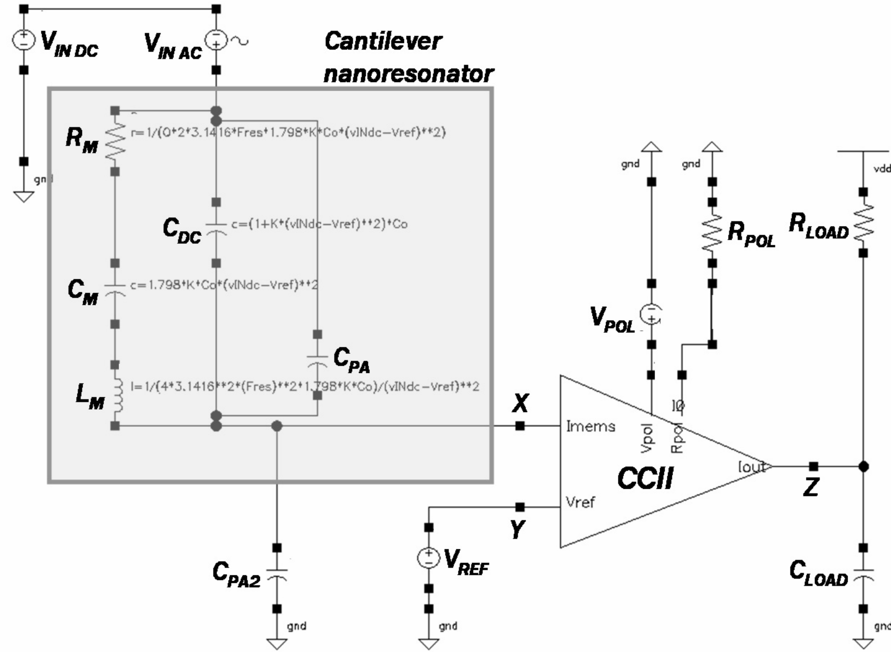

Figure 16. Simulation module based on a RLC model that represents the cantilever at CCII input

In this model, the spring-softening effect that shifts the resonance frequency down to lower values when the excitation voltage is increased is neglected. The resonator parameters are calculated in the following way (c.f. section III.2 chapter 2):

$$C_{DC} = (1 + K V_{DC\,IN}^2) C_0 \text{ where } C_0 = \frac{\varepsilon_0 h l}{d} \text{ and } K = \frac{3 \varepsilon_0 l^4}{4 E b^3 d^3} \quad \text{(III.14)}$$

$$C_M = 1.798 K V_{DC\,IN}^2 C_0 \qquad L_M = \frac{1}{4\pi^2 f_{RES}^2 C_M} \quad R_M = \frac{1}{Q}\sqrt{\frac{L_M}{C_M}} \quad \text{(III.15)}$$

C_{PA} is related to the fringing field and is in the order of magnitude of C_{DC} or slightly higher. C_{PA2} is estimated between 10 and 100 fF from direct measurements of dimensions in the layout:

$$C_{PA2} = C_{ANCHOR} + C_{CONTACTS} + C_{ROUTING} \quad \text{(III.16)}$$

Regarding the NEMS part, adjustable variables in the simulation cell are: f_{RES}, K, C_0, C_{PA}, and C_{PA2}, accurately calculated as a function of geometrical dimensions of the cantilever. $V_{IN\,AC}$ and $V_{IN\,DC}$, the AC and DC excitation voltages, are also tunable. The Q-factor is the last variable: initially it was estimated based on previous experimental measurements of discrete devices. HSPICE subsequently calculates C_M, L_M, R_M and C_{DC} following equations (III.14) and (III.15).

Regarding the CCII part, adjustable variables in the simulation cell are the same as in the previous simulations: R_{POL}, R_{LOAD}, C_{LOAD}, V_{POL} and V_{REF} (set to the same value).

Complementarily with the study of the intrinsic behavior of the CCII circuit, the influence of characteristic parameters, like R_{LOAD} or R_{POL}, on the frequency response of the mixed NEMS/CMOS system is investigated.

Realistic values for all parameters, evaluated from experimental data, are implemented into the model and reported into Table III - 9, Table III - 10 and Table III - 11. These data are

calculated as a function of the geometrical dimensions of the cantilever: *l* (length), *b* (width), *h* (thickness) and *d* (gap with driver), and for E=130 GPa. Subsequent simulations are performed based on these conditions.

Parameter	Value
l; b; h; d	14.5 ; 0.29; 0.56 ; 0.75 (μm)
f_{RES}	1.66 MHz
Q	13
K	2.2 10^{-4}
C_0	96 aF
C_{PA}	1 fF (≈ 10·C_0)
C_{PA2}	50 fF
$V_{IN\,AC}$	0.9 V pp (0 dBm)
[1] $V_{IN\ DC}$	20 V (22 applied)

Table III - 9. NEMS parameters

Parameter	Value
R_M	490 MΩ
L_M	605 H
C_M	15 aF

Table III - 10. Equivalent motional parameters

Parameter	Value
R_{LOAD}	1 kΩ
C_{LOAD}	30 pF
R_{POL}	200 kΩ
V_{POL} / V_{REF}	2 V

Table III - 11. CCII parameters

The resulting C_{DC} is 104 aF according to eq.(III.14). The influence of C_{PA2} is analyzed in the 1fF - 1pF range, and seems to be negligible; therefore it is not depicted later. In all the following simulations, the frequency response is given in terms of voltage gain (see eq.(III.13))

- Comparison with discrete cantilevers

The electrical frequency responses of two identical cantilevers, one integrated with the CCII, the other discrete, are plotted in Figure 17 in order to measure the incidence of the CMOS integration. For the discrete one, C_{PA2} is actually equal to C_{LOAD} =30 pF, while for the integrated one C_{PA2} = 50 fF, e.g. three orders of magnitude less.

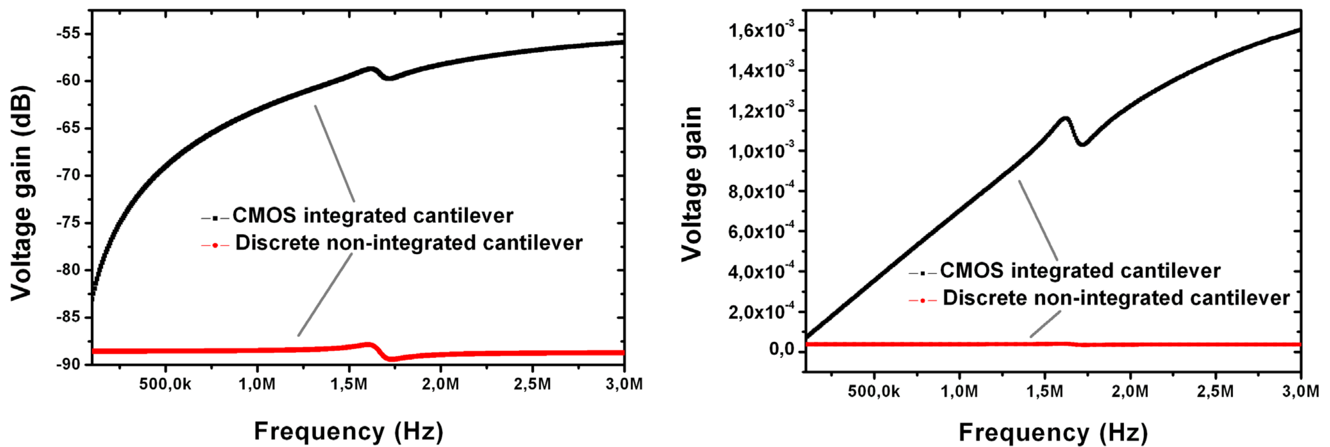

Figure 17. Comparison integrated/discrete cantilever. Left: gain in dB; right: normal gain.

In this specific context, where R_{LOAD} is relatively low, the circuit already provides a 30 dB (equivalent to a factor 30) enhancement in terms of signal level. Elevating R_{LOAD} is a straightforward way to increase even more this difference. As future prospect, the same CCII topology with one or more additional internal amplification stages (through cascode mirrors) would provide even higher output signals.

[1] since the resonator is biased at V_{REF}, in order to apply X V to the resonator, $V_{IN\,DC}$ value must be X + V_{REF}. For simplification purposes, $V_{IN\,DC}$ will be cited as X only.

- Study of R_{LOAD} influence

In Figure 18, the output frequency spectrum is plotted for several values of R_{LOAD} from 0.5 to 5 kΩ.

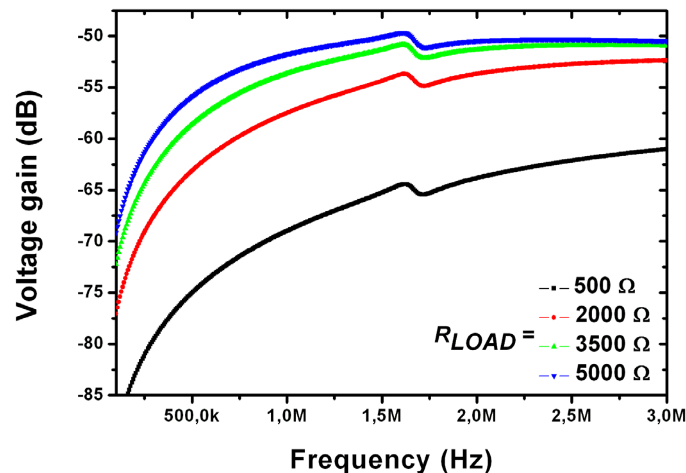

Figure 18. CMOS cantilever frequency response as a function of R_{LOAD}

R_{LOAD} increases the level of both the resonance peak and the background signal (arising mainly from C_{PA}) even if the relative amplitude of one with respect to the other remains constant (same offset in dB). It can be observed that above 3500 Ω, the response curve is attenuated (flatter) before f_{RES} since for these values of R_{LOAD} the cutting frequency becomes inferior to f_{RES}. This graph reveals that for C_{LOAD} around 30 pF, there is no sense adjusting R_{LOAD} to more than 3 kΩ (in all subsequent simulations, R_{LOAD} is set to 1 kΩ).

- Study of C_{LOAD} influence

In Figure 19, the output frequency spectrum is plotted for three values of C_{LOAD}: 1, 10 and 100 pF.

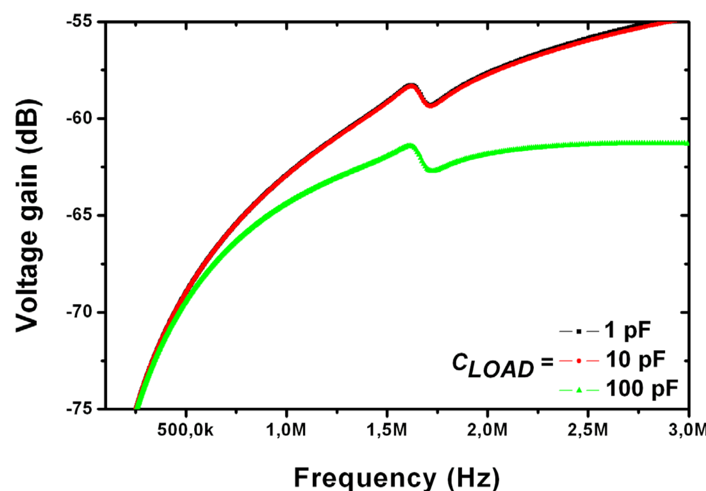

Figure 19. CMOS cantilever frequency response as a function of C_{LOAD}

For values of C_{LOAD} resulting in cut-off frequencies larger than the resonance frequency of the resonator, the spectrum pattern remains unaffected by C_{LOAD}. However, for C_{LOAD} =100 pF, cut-off frequency and resonance frequency take the same value and the signal level starts decreasing. Since C_{LOAD} is intrinsic to the measurement set-up, R_{LOAD} must be adequately chosen to avoid signal attenuation.

- Study of R_{POL} influence

In Figure 20, the output frequency spectrum is plotted for R_{POL} = 0.01, 0.1 and 1MΩ.

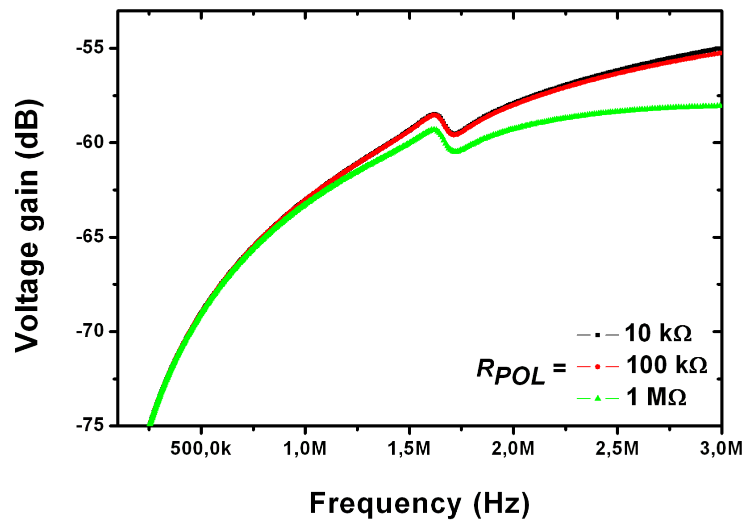

Figure 20. CMOS cantilever frequency response as a function of R_{POL}

In agreement with Figure 8, this graph shows that R_{POL} does not influence the resonance peak level but the lower it is the higher is the bandwidth what avoids signal attenuations.

- Study of C_{PA} influence

In Figure 21, the output frequency spectrum is plotted for several values of C_{PA} from 1 aF to 10 fF.

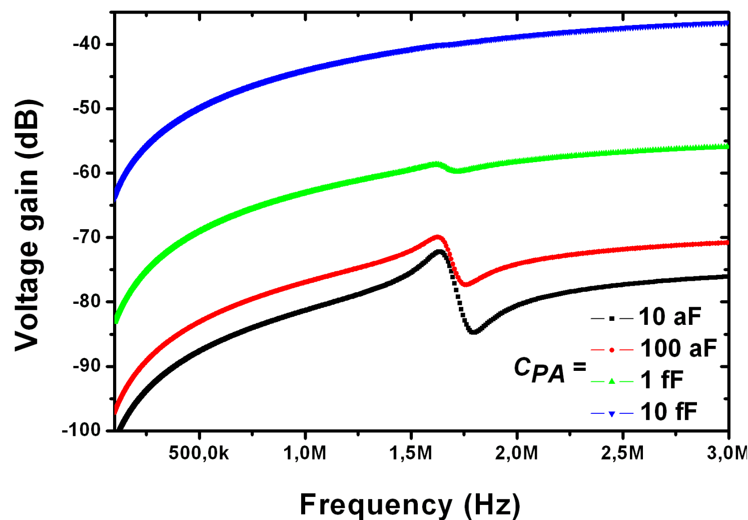

Figure 21. CMOS cantilever frequency response as a function of C_{PA}

This graph reveals that C_{PA} is one of the most critical parameters in the resonance spectrum pattern. As the background signal level is mainly related to C_{PA}, when C_{PA} is low the background level is low and the resonance peak emerges much: see for C_{PA}= 10 and 100 aF. Then, there is a critical domain for 100 aF<C_{PA}<1 fF where the background signal becomes really dominant over the resonance peak. The cantilever resonators of this work are situated in this domain.

- Study of $V_{IN\ DC}$ influence

In Figure 22, the output frequency spectrum is plotted for several values of $V_{IN\ DC}$ from 15 to 25 V.

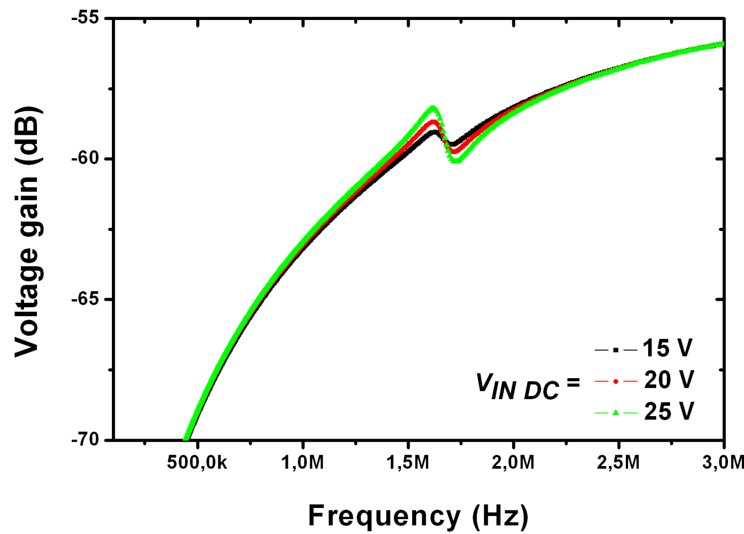

Figure 22. CMOS cantilever frequency response as a function of $V_{IN\ DC}$

This graph shows the major role played by $V_{IN\ DC}$ on the peak amplitude (neglecting the frequency translation owing to spring-softening effect).

CONCLUSION

According to these simulations, the parameters that most affect the resonance peak amplitude are C_{PA} and $V_{IN\ DC}$, as well as the Q-factor, not analyzed here. Q and C_{PA} are intrinsic parameters that cannot be varied (unless measurements are performed in vacuum what would drastically improve the Q-factor). Regarding $V_{IN\ DC}$, its upper limit is the value of the pull-in voltage which provokes irreversible lateral sticking of the cantilever on its in-front electrode.

The parameters that most affect the background level of the resonance peak are C_{PA} and the adjustable R_{LOAD}. C_{LOAD} and R_{POL} are less determining than other parameters but they must be adequately chosen to avoid signal attenuations. Reducing C_{LOAD} would allow increasing R_{LOAD} but in the present conditions C_{LOAD} is not modifiable as it is determined by the measurement set-up.

II.2.c.ii) Electrical simulations of QB-CCII mixed circuit

Figure 23 is a scheme of the simulation cell of the mixed electromechanical system QB-CCII CIRCUIT. QB are placed at CCII input and modeled by three branches (c.f. chapter 2). With respect to Figure 16, their meaning is identical except for C_{PA}. The C_{PA} branch is related to anchors capacitors.

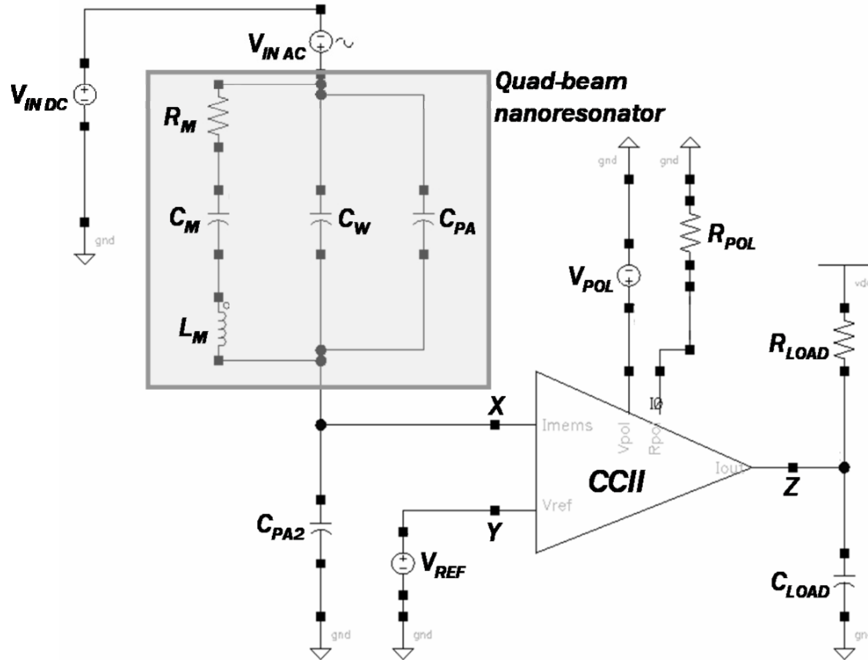

Figure 23. HSPICE simulation cell of a QB coupled to the CCII

In this model, the spring-softening effect (that shifts the resonance frequency down to lower values with increasing driving voltage) is also neglected. The resonator parameters are calculated according to a RLC model (c.f. chapter 2):

$$C_W = \frac{\varepsilon_0 L_1^2}{d} \tag{III.17}$$

$$R_M = \frac{D}{\eta^2} = \frac{\sqrt{km}}{Q\eta^2} \qquad C_M = \frac{\eta^2}{k} \qquad L_M = \frac{m}{\eta^2} \tag{III.18}$$

where

$$\eta \approx \frac{\varepsilon_0 L_1^2}{d^2} V_{IN\,DC} \qquad k = \alpha_{QB} \frac{E\,h^3\,b}{l^3} \qquad m = \rho\, L_1^2\, h \tag{III.19}$$

C_{PA} is related to the physical capacitor constituted of polysilicon anchor // SiO_2 pillar // Si bulk. It is approximated as:

$$C_{PA} = 4\frac{\varepsilon_{SiO_2} A_{ANCHOR}}{h_{SiO_2}} \tag{III.20}$$

C_{PA2} is estimated between 10 and 100 fF from direct measurements of dimensions in the layout:

$$C_{PA2} = C_{CONTACTS} + C_{ROUTING} \tag{III.21}$$

Regarding the NEMS part, adjustable variables in the simulation cell are: k, m, η, C_W, C_{PA}, C_{PA2}, accurately calculated as a function of geometrical dimensions of the QB. $V_{IN\ AC}$ and $V_{IN\ DC}$, AC and DC excitation voltages, and Q-factor are also tunable. HSPICE subsequently calculates C_M, L_M, R_M following equations (III.18).

Regarding the CCII part. adjustable variables in the simulation cell are: R_{POL}, R_{LOAD}, C_{LOAD}, V_{POL} and V_{REF}.

Taking into account previous results, the study of the influence of characteristic parameters on the frequency response of the mixed QB/CMOS system is restricted to C_{PA}, the parallel parasitic capacitance, since the phenomenological incidence of the other parameters is already known. In the case of QB, C_{PA} is so high that it constitutes de facto the most critical parameter determining the level of background signal and the resonance peak amplitude (to what extent it emerges from this background signal).

Realistic values for all parameters, evaluated from experimental data, are implemented into the model and reported into Table III - 12, Table III - 13 and Table III - 14. These data are calculated as a function of the geometrical dimensions of the QB: L_1 (square paddle width), l (beam length), b (beam width), h (thickness) and d (gap with substrate), and for E=130 GPa.

Parameter	Value
L_1 ; l	5.9 ; 13.2 (µm)
b; h ; d	0.42; 0.45; 1.1 (µm)
k	3.7 N/m
m	36 pg
η	5 10^{-9}
Q	35
C_W	280 aF
C_{PA}	80 fF
C_{PA2}	25 fF
$V_{IN\ AC}$	0.9 V pp (0dBm)
$V_{IN\ DC}$	20 V (22 applied)

Table III - 12. QB NEMS parameters

Parameter	Value
R_M	380 MΩ
L_M	1400 H
C_M	8 aF

Table III - 13. Equivalent motional parameters

Parameter	Value
R_{LOAD}	0.92 kΩ
C_{LOAD}	30 pF
R_{POL}	200 kΩ
V_{POL}- V_{REF}	2 V

Table III - 14. CCII parameters

- **Study of C_{PA} influence**

In Figure 24, the output frequency spectrum is plotted for three values of C_{PA} from 10 fF to 1 pF.

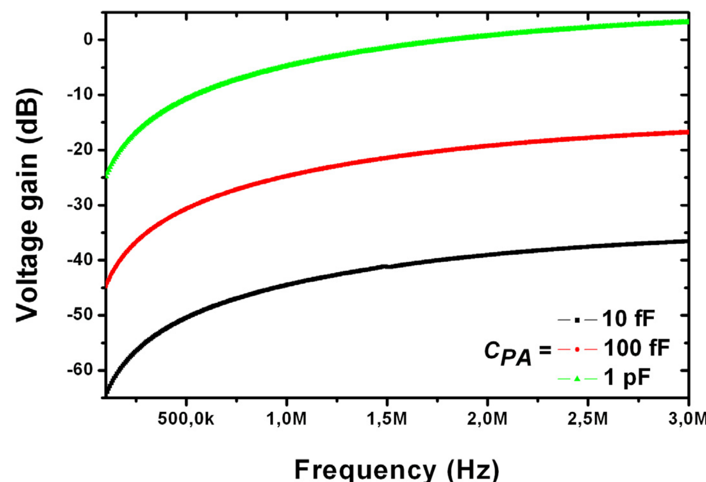

Figure 24. CMOS QB frequency response as a function of C_{PA}

From Figure 24, it is clear that for C_{PA} values in the 10 fF-1 pF range, the induced background signal is so high that the resonance peak is totally masked. This is consistent with the predictions of chapter 2. To circumvent this issue, a 'calibration' of the background signal is made: it can be performed with a network analyzer during experimental measurements (for detailed explanations, refer to chapter 5).

A simulation cell is built up according to this calibration approach. Like in Figure 24, the output frequency spectrum is plotted in Figure 25 for three values of C_{PA} from 10 fF to 1 pF, but with a calibrated signal.

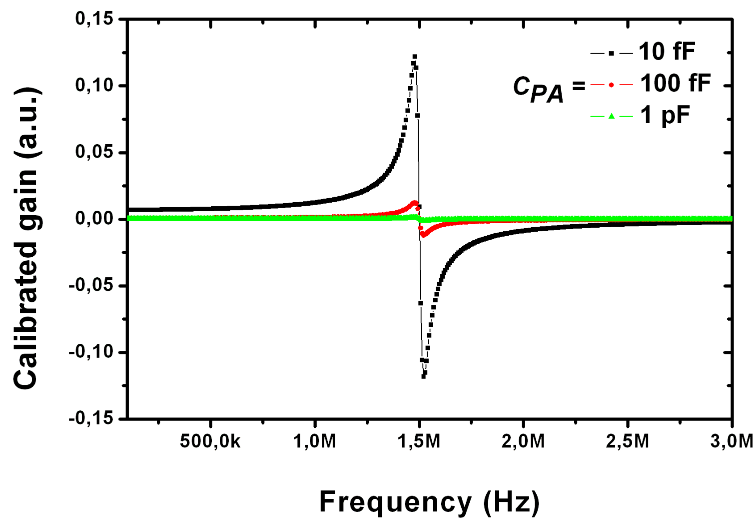

Figure 25. CMOS QB frequency response (calibrated) as a function of C_{PA}

This graph confirms the major role played by C_{PA} regarding the amplitude of the peak.

CONCLUSION

Apart from the Q-factor, the parameter that most affect both the resonance peak amplitude and the level of background signal is C_{PA}. Unfortunately, Q and C_{PA} are intrinsic parameters that cannot be varied. At least, special efforts should be dedicated to the resonator design in order to decrease as much as possible the area of the four anchors.

With respect to discrete devices, CMOS integration does not provide any improvements regarding the role of C_{PA}, nevertheless signal attenuation due to C_{PA2} is drastically reduced.

II.3. NEMS/CMOS circuit layout

The CCII layout was made using CADENCE ICFB with CNM process library. Hereafter, the guide lines followed during the design of the layout of the CCII and its integration areas are explained. An exhaustive description of the entire chip layout is provided

II.3.a. CCII Circuit layout, integration areas layout

The layout of the CMOS CCII circuit has been done according to several requirements. Concerning the circuit itself, transistor matching and routing optimization have been the two critical points. Indeed, CNM CMOS technology contains one single metal layer and the routing has to associate two materials: so-called *poly1* (polysilicon) and *metal* (Al).

The resulting size of the CCII circuit without pads is about 500 * 400 μm² (0.2 mm²). Since CNM CMOS technology is a 2.5 μm lithography process, a considerably smaller implementation can be obtained using modern submicron CMOS technologies.

Regarding the objective of integrating NEMS on CMOS, a fabrication strategy (detailed in chapter 4) is chosen whereby nanomechanical resonators are defined by post-processing pre-fabricated CMOS substrates. In other words, the nanopatterning step for NEMS definition and the subsequent process steps are carried out after complete fabrication of the CMOS circuit. This approach requires the use of specific areas, subsequently called '**integration areas**' (*IA*), in which NEMS devices will be defined.

As explained later in chapter 4, the layout of the entire chip (7.5 * 7.5 mm²) is not trivial: all the clusters CCII circuits + integration areas had to be placed adequately in order to be able to align a full-wafer nanostencil membrane a posteriori. Since the design of the stencil responds to specific rules owing to the mechanical behavior of the membrane, the position of the integration areas had to respect the position of the membranes apertures.

Each resonating nano/micromechanical device is connected to its own readout circuit. Indeed, the CCII circuit has not been designed for operating arrays of resonators. This means that every ensemble CIRCUIT+RESONATOR is electrically isolated and independent one from each other. Each ensemble has its own contact Al pads for electrical test.

At the end of the fabrication process, the whole surface of the chip is covered with a passivation bi-layer (800 nm thick) constituted of silicon nitride (SiN) and silicon oxide (SiO_2). Local apertures into the passivation layers are only defined on top of:

- all Al contact Al pads
- all **integration areas**. These are the special areas where nano/micromechanical devices are fabricated in a post-processing module after CMOS fabrication. One resonator per area is fabricated. They are electrically connected on one side to Al contact pads and on the other to CCII input. Their layout is detailed hereafter.

INTEGRATION AREA (*IA*) LAYOUT

They are located on an n-well to isolate them from the surrounding p-bulk and for independent polarization. Their fabrication is realized along the CMOS process whose steps are

described in detail in chapter 4 and in annex A7.1. The final result after CMOS process completion is:

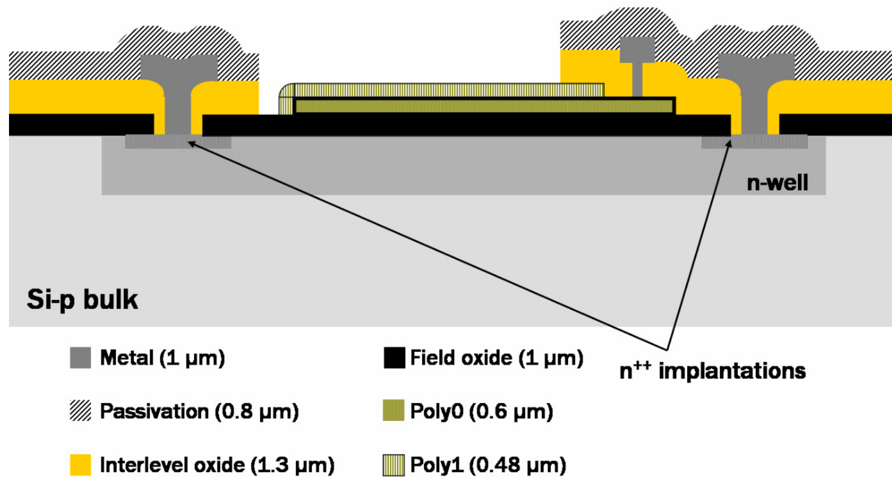

Figure 26. Cross-sectional view of an integration area

The main novelty regarding the layout with respect to the previous experience in NANOMASS project is the presence of INTERLEVEL OXIDE above the integration area. This technological improvement leading to higher yield is detailed in chapter 4. Figure 27 depicts the top view of the integration area:

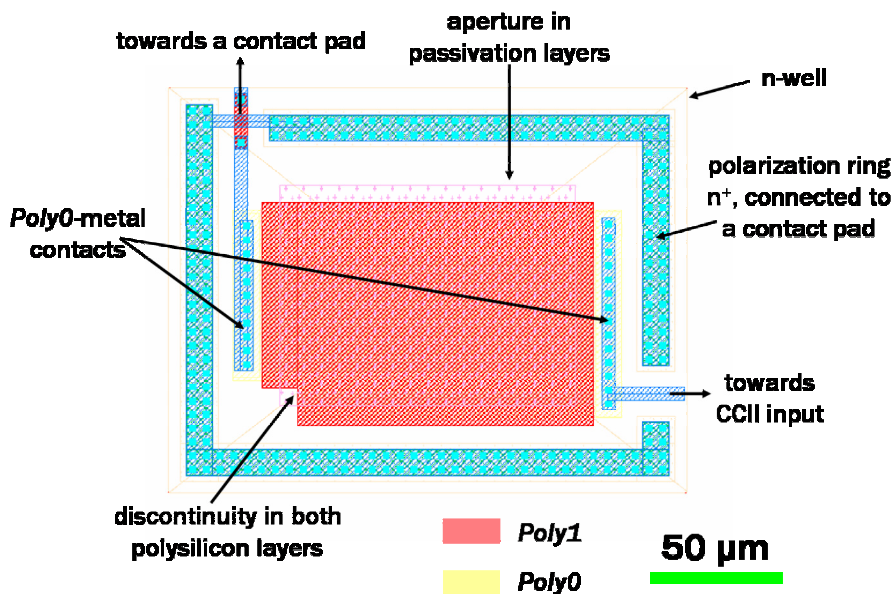

Figure 27. Integration area layout. Specific design for in-plane cantilever integration

At one of the four edges of the passivation aperture, a discontinuity is included in both *poly0* and *poly1* patterns so that left and right electrodes are isolated one from each other after nanodevice pattern transfer by Reactive Ion Etching (RIE) of polysilicon. A margin of 7 μm between passivation aperture and polysilicon patterns is provided. The discontinuity area has been minimized in order to maximize the 'usable' *poly0* area with the aim of making easier the alignment of nanodevices inside integration areas.

CCII CIRCUIT LAYOUT WITH INTEGRATION AREA

Three kinds of devices are integrated with CMOS: cantilevers, quad-beams and torsional paddles. We have focused specifically on in-plane vibrating cantilevers and out-of-plane vibrating quad-beams. Figure 28 represents the ensemble READOUT CIRCUIT + INTEGRATION AREA + NANODEVICE PATTERN + CONTACT PAD for cantilevers integration; Figure 29 represents integrated quad-beams. The green pattern corresponds to the Al pattern deposited by metal evaporation and structured either by nSL or by eBL and lift-off. This gives an idea of how nanodevices have to be aligned within an integration area. In the case of cantilevers, the left anchor is electrically connected to the V_{EXC} pad (for excitation voltage), the right one is connected to CCII input. This kind of layout contains 8 pads depicted in Figure 28:

- Pads V_{REF}, V_{DD}, V_{POL}, R_{POL} and V_{SS} for circuit polarization
- Pad I_{OUT} collecting the amplified AC (I_{MEMS}) + DC (I_{BIAS}) current that subsequently flows externally into R_{LOAD}.
- Pads V_{EXC} for polarizing the resonator through its driving electrode ($V_{IN\,DC}$ + $V_{IN\,AC}$)
- Pads $V_{GND\text{-}NANOAREA}$ for polarizing the underlying n-well like V_{REF} in order to diminish parasitic capacitances and to be at the same voltage as the resonator (connected to CCII input, i.e. V_{REF}) so that it is not attracted and does not collapse downwards

In the case of quad-beams, all pads have the same meaning except that the device (resonating 'vertically', i.e. out-of-plane) is polarized through the underlying n-well connected to the V_{EXC} pad (see Figure 29).

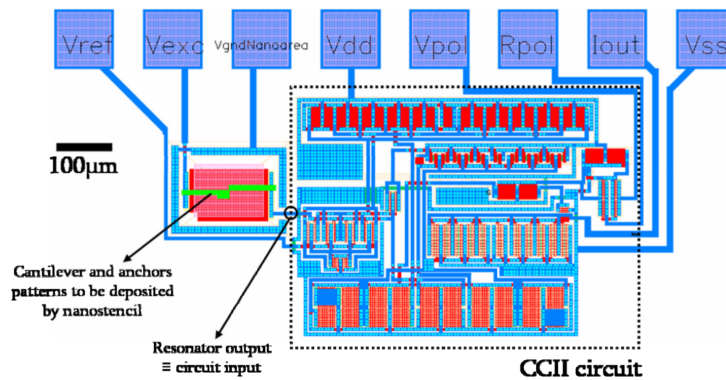

Figure 28. CCII layout with cantilevers-specific integration area

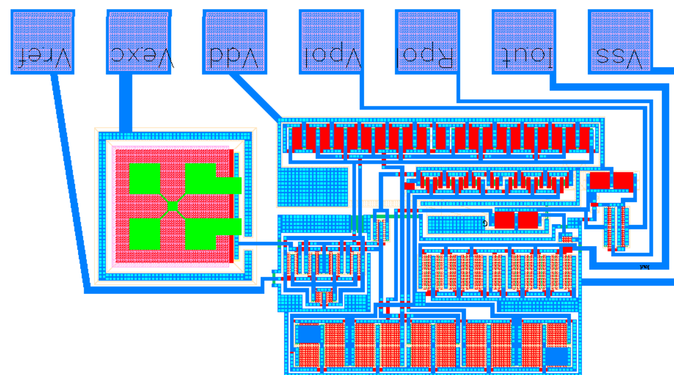

Figure 29. CCII layout with quad-beams-specific integration area

By a simple calculation of a p-n junction, the necessary distance between integration area and circuit can be estimated to prevent excessive extension of the depletion zone formed at the n-well/p-bulk interface. If this depletion zone reaches the p-substrate of the n-transistors of the CCII-, their operation can be perturbed. A 5 µm distance between the n-well of the integration area and the CCII CMOS circuit has been foreseen what limits the polarization voltage of the n-well to 6 V. A posteriori, it is clear that it has not been sufficient for QB which require higher voltages.

II.3.b. Chip layout

The layout of the whole chip contains 37 CCII CIRCUIT + RESONATOR ensembles together with 41 integration areas for discrete devices. The chip has a 7.32 * 7.32 mm^2 area. Integration areas for discrete devices have an identical architecture but they have no associated circuitry, their output electrode is connected to a contact pad for external detection.

Figure 30 illustrates the devices distribution within the chip:

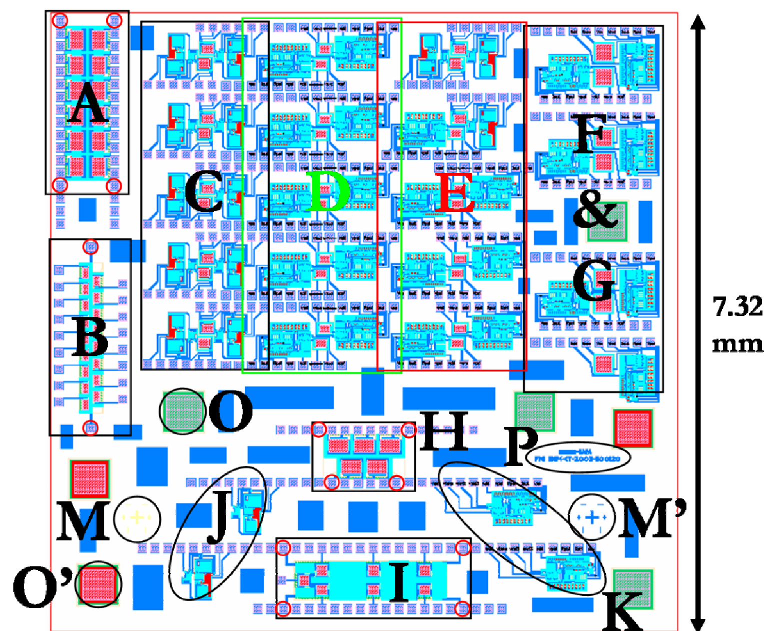

Figure 30. NaPa chip layout

Zones A, B, H and I contain *IA* for different types of discrete devices and are all located on a n-well. In-between each *IA*, electrical contacts metal (connected to the pads) / n^+ substrate have been inserted to polarize the well more efficiently (possible until 100 V).

Big metal rectangles (in blue) were included in order to homogenize the metal spatial distribution and therefore to improve the metal etching homogeneity.

zone A 12 *IA* for discrete devices (longitudinal mode dual beams, not described in this thesis) controllable with 2 pads. The n-well can be accessed by 4 pads visible on Figure 30 (red circles at extremities).

zone B 17 *IA* for discrete paddle resonators (not described in this thesis) controllable with 1 pad. The n-well can be accessed by 2 pads visible on Figure 30 (red circles at extremities).

zone C	10 BSNN circuits (not described in this thesis) for integration of in-plane vibrating cantilevers.
zone D	10 CCII circuits for integration of in-plane vibrating cantilevers.
zone E	from left to right and up to down: 3 BSNN circuits for integration of double cantilevers 2 CCII circuits for integration of double cantilevers 5 CCII circuits for integration of paddle resonators
zone F & G	7 CCII circuits for integration of quad-beams
zone H	5 *IA* for discrete devices (longitudinal mode dual beams) controllable with 2 pads. The n-well can be accessed by 4 pads visible on Figure 30 (red circles at extremities).
zone I	7 *IA* for discrete QB resonators, controllable with 1 pad. The n-well can be accessed by 4 pads visible on Figure 30 (red circles at extremities).
zone J	2 BSNN test circuits (not described). J1 above, J2 below.
zone K	2 CCII test circuits. K1 above, K2 below.
zone M	*poly0* patterns serving as nanostencil-CMOS alignments marks (see chapter 4)
zone M'	*metal* patterns serving as nanostencil-CMOS alignments marks see chapter 4)
zone O	cell for testing [passivation+interlevel oxide] RIE (see chapter 4)
zone O'	cell for testing *poly1* RIE (see chapter 4)
zone P	CNM logo and NaPa project references

Conclusion of chapter 3

In this chapter, a specific low-power CMOS readout circuit designed in the framework of this thesis has been described in detail: its function is to read out the capacitive current generated by resonating nano/micromechanical devices.

Complementarily, a whole CMOS chip has been designed, responding both to the requirements of the design rules of the CMOS technology and of the posterior integration of NEMS.

The topology and the corresponding layout of the second-generation current conveyor (CCII) circuit have been presented. The circuit behavior (intrinsic and coupled to resonating N-MEMS) has also been fully simulated. Electrical simulations show that CMOS integration greatly enhances the capacitive detection of the resonance of mechanical resonators by (i) drastically reducing parasitic loads at the resonator output and (ii) amplifying 'on-chip' the resonance signal.

These two statements remain true for any type of resonator. However, for out-of-plane vibrating resonators CMOS integration does not solve the issue of 'vertical' (out-of-plane) stray capacitances. In fact, this issue can mainly be solved through an optimization of the design of the resonator anchors.

In terms of processing, combining the technology for the fabrication of nanomechanical resonators with a standard CMOS technology is challenging. However, this issue has been addressed through a novel technology that is going to be detailed in chapter 4. In chapter 5, the experimental electrical characterization of successfully fabricated NEMS/CMOS together with an analysis of their frequency response will be carried out.

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CHAPTER 4

FABRICATION OF NANO/MICROMECHANICAL RESONATORS ON CMOS CIRCUITRY

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As a continuation to chapter 3, chapter 4 is focused on the technological aspect of the monolithic integration of nano/micromechanical resonators with CMOS circuitry.

Chapter 3 detailed to what extent such a monolithic integration implies a drastic enhancement in terms of device operation through the low-loss coupling with a CMOS circuit for on-chip signal conditioning and amplification. In chapter 4, we address the technological realization of this objective.

Regarding processing, the key issue of the fabrication of devices with submicron scale dimensions arises from lithography. In this connection, the technological process flow is mostly determined by the choice of nanopatterning technique.

We follow an approach [1, 2] based on post-processing pre-fabricated standard CMOS wafers. The fabrication strategy consists in using existing CMOS layers as structural layer (capacitor polysilicon) and sacrificial layer (field oxide) of the resonators. This method facilitates the interconnection between the nanomechanical device and the CMOS circuit, avoiding the need to use any additional layer and/or material.

The post-processing approach also allows using a different lithography technique for CMOS circuit fabrication and NEMS definition: in this way, potentially cheaper, not ultra-advanced CMOS technologies can be utilized for circuitry fabrication while a higher resolution nanolithography technique is implemented for subsequent (single step) NEMS patterning.

To define the nanodevices dimensions, we have chosen two different nanolithography techniques: nanostencil (nSL) and electron beam lithography (eBL). Actually, most of the work exposed in this thesis has been devoted to nSL, an emerging technique, still in development, in particular to demonstrate that it represents an outstanding tool to define nanometer scale devices on CMOS wafer at full wafer level. In parallel, we have developed another post-processing technology based on eBL for rapid, but serial, prototyping of new devices.

The development of nSL technique for this purpose has been realized in the framework of the NaPa[1] project, whose goals are the development of emerging nanopatterning techniques like nanoimprint, soft-lithography or self-assembly. The fabrication of nanomechanical devices monolithically integrated into CMOS circuit has represented an ideal platform to demonstrate the full-wafer patterning of nanodevices on CMOS wafers by nSL, what was one of the initial objectives of NaPa. This task has given occasion to a close collaboration with the Microsystems laboratory LMIS1 from EPFL, in particular with Dr Marc.A.F. van den Boogaart and Prof. Jürgen Brugger. Initially, this work partially relied on the previous experience of CNM in FP5 EU project NANOMASS[2] in which a similar approach was followed but using alternative nanolithography methods: in that project, the functionality of few prototypes was demonstrated but not the patterning of a whole CMOS wafer.

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[1] "Emerging Nanopatterning methods" project funded by the European Commission within FP6 (6th Framework Program), 31 (academic and industrial) partners from 14 countries (contract NMP4-CT-2003-500120)

[2] Project funded by the European Commission within the FP5 (5th Framework Program), contract nº IST-1999-14053

Pursuing a monolithic integration of NEMS on CMOS, several nanolithography techniques may be adequate but only a few simultaneously ensure parallel patterning for rapid processing at wafer scale and nanometer-sized features definition. Moreover, CMOS circuits require compatibility of the patterning technique for proper circuitry operation, in other words, to avoid any damage during the post-processing related to NEMS definition.

Nanostencil lithography (nSL) is a suitable technique to fulfill those requirements. It is a flexible (easy to apply), parallel and resistless patterning method based on a high-resolution wafer-scaled shadow mask.

It allows a wide choice of materials and surfaces to be selectively deposited (i.e. only where needed). On the contrary to deep-ultraviolet (DUV), X-ray, electron beam, or ion beam exposure, mechanically fragile and chemically functionalized surfaces can be structured, due to the absence of cyclic (resist-based) process steps and to the absence of etching processes (unlike nanoimprint lithography). Additionally, nSL potentially has a sub-100 nm (maybe sub-50 nm) resolution what is better than DUV, for example.

Its parallelism and its associated potentially high throughput make it a serious candidate for industrialization. Nevertheless, as it will be explained in this chapter, some limitations still exist for its industrial implementation but some of them have been solved during the development of this thesis.

This chapter will review the main aspects of the fabrication and applications of nanostencils. Then the fabrication of a full-wafer stencil will be explained. The challenges and the related necessary optimization of nSL-based process on CMOS will be exposed. All process steps will be detailed before concluding on the obtained results. At the end, the CMOS compatibility of the nSL-based process in terms of circuit operation will be commented.

Much more briefly, the interest and limitations of e-beam lithography for integration of NEMS on CMOS as well as the details upon the corresponding process flow we have been defining will be exposed.

I. Lithography techniques for integration of NEMS on CMOS

I.1. Nanostencil lithography, a full-wafer high-resolution technique

Nanostencil lithography (nSL) is a shadow-mask based lithography technique (see Figure 1). Potentially, patterning techniques implementing shadow-masks are not limited in resolution and towards the confirmation of this assumption, some authors have applied single-walled carbon nanotubes as shadow masks for the fabrication of 1-2 nm wide gaps [3, 4].

In this work, the shadow-masks are under the form of stencils that are micromachined Si wafers containing hundreds of nanostencils in the form of thin (200 nm thick) free-standing silicon nitride (SiN) membranes with micro- and nano-scale apertures (see Figure 2). As it will be demonstrated along this chapter, this type of stencil allows local nanopatterning of a whole CMOS wafer in one deposition step.

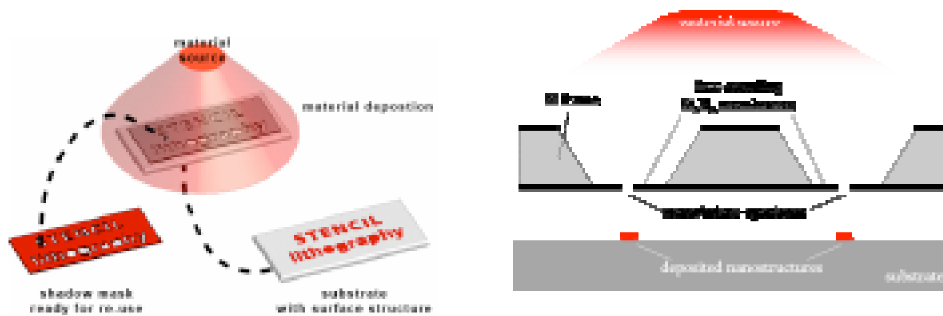


Figure 1 [5]. Principle of nanostencil lithography

Figure 2. Specific implementation of nanostencil lithography in this thesis. Nanostencils free-standing membranes (framed by a Si wafer) with local nano/microapertures

First, the applications and various fabrication processes of nanostencil membranes reported in the literature will be discussed. After this introduction, the fabrication of a full-wafer (100 mm) nanostencil based on advanced bulk and surface nano-micromachining [6] will be described.

I.1.a. State of the art, features and advantages of the technique

ADVANTAGES OF THE TECHNIQUE

Stencil lithography (SL) is a versatile method that can be used in a variety of applications. There has been recently a strong interest regarding the use of shadow masks, mostly related to combinatorial materials science [7, 8], organic based device fabrication [9, 10], as well as rapid prototyping of nanoscale structures using dynamic [11-13] or quasi-dynamic [14] stencil deposition. These papers are mainly focused on process related topics [6, 15-18]; few ones are more focused on the application itself [1, 19, 20].

From the study of almost all reported variants of SL, a series of intrinsic generic advantages emerges. Its main features are its 'cleanliness', its flexibility, its parallelism and its high resolution.

Moreover, it is a non-contact and resistless (i.e. clean) technique. This exclusive characteristic makes that ultra-clean surfaces with high purity deposits can be obtained. From that, mechanically fragile [16] and chemically functionalized surfaces [21] can be structured, due to the absence of cyclic (resist-based) process steps.

More generally, SL allows a wide choice of materials (the limitation comes from the deposition technique and not from SL itself) and surfaces to be selectively deposited (i.e. only where needed). In particular, several examples of deposition of complex oxides by Pulsed Laser Deposition (PLD) through nanostencils have recently been reported [22, 23].

Its parallelism makes it much faster than presently existing charged particle techniques (FIB or eBL) and in this context one objective of NaPa project, relying on a collaboration between EPFL and CNM, has been the demonstration of its implementation at full-wafer scale while providing 150 nm resolution.

TYPES OF SHADOW-MASK

There are basically two types of shadow masks: in-situ and membrane-based. In-situ shadow masks were used, for example, to fabricate the first single electron transistor [24]; this is also a well-known technique in MBE (Molecular Beam Epitaxy) experiments with II-VI and III-V semiconductor compounds [25, 26]. In practice, such a shadow mask consists of a two-layer stack onto the substrate to be patterned: the top layer is the proper shadow mask and the bottom one, generally a sacrificial layer, acts as spacer. A clear disadvantage of in-situ SL is the need to remove this mask after evaporation what involves a chemical treatment contaminating the substrate.

The other approach is based on the implementation of a locally perforated membrane. Its material may be a metal, Si, Si_3N_4 or even polymers. To release the membrane from the backside, several distinct techniques were already reported. Membrane thickness and area are two key features.

It is important to obtain a final thin membrane mainly for two reasons: it makes its perforation easier (shorter etching) and it increases the uniformity of the structures whose replication patterns are located at the extremities of the stencil: otherwise the apertures sidewalls may shadow the incoming flux and deform the obtained pattern shape.

Nanoapertures are generally defined from the membrane front-side either by eBL (and subsequent pattern transfer by RIE) [27] or FIB [11, 18, 28] but these two techniques are serial and impede large area fabrication of apertures and consequently the available throughput.

Concerning the area of thin membranes, it generally does not exceed 1 mm^2 [5, 28, 29] because of its fragility. Mechanical in-situ reinforcements could permit to increase the membrane area but in general this tends to decrease the density of apertures [29].

LIMITATIONS

The resolution of the deposited structures is both determined by the stencil aperture resolution and the geometrical configuration of the deposition chamber (source size, source-substrate distance and gap between stencil and substrate). In practice, a deposited structure is composed of a main structure, a penumbra, whose dimensions are calculable in a simple way through geometrical laws [28, 30], and surface interaction effects such as surface migration and re-deposition (scattering). The penumbra formation depends exclusively on the geometrical conditions and together with those surface-related effects, they cause a distortion of the pattern

resulting in blurred edges and pattern widening. This so-called 'blurring effect' has been observed by numerous authors [10, 16, 25, 28, 30, 31]. The gap between stencil and surface appears to be the key parameter of this issue. In contrast, the deposition of a material through the apertures of a stencil directly put in contact with the substrate yields a perfect 1:1 replication of the aperture pattern [16]. 'Blurring effect' is the topic of section II.2.b.

Another source of pattern distortion, associated to 'blurring effect', is the stress-related increasing deflection of membranes around specific apertures (for example U-shape) during material deposition. As the gap is constantly varying, the resulting pattern is not well defined and its edges are smooth and blurred. To circumvent that, reinforced membranes have been demonstrated by EPFL [32, 33]. Their full-wafer fabrication process is actually detailed in next section.

A third relevant effect causing pattern distortion is clogging. It always occurs but can be more or less significant: when evaporating a material, a certain amount is deposited on the membrane itself and inside its apertures (on the sidewalls). Kölbel et al. [15] proposes a solution to remedy to this problem by coating stencils with an anti-adhesive self-assembled monolayer (SAM): this reduces the adhesion of the evaporated material inside the apertures and thereby the clogging of nano/micro apertures.

OBJECTIVE AND CONTEXT OF THIS WORK

It has been shown that the fabrication of apertures as small as 15-20 nm [27] is possible with the use of thin suspended SiN membranes. However in this paper the membranes have a limited area (max. 100 x100 μm^2).

In this context, EPFL has demonstrated the possibility of fabricating full-wafer scale (100 mm) stencils with local free-standing membranes, whose apertures result in arbitrary shaped patterns between 200 nm up to 300 µm [6, 18] (this large range of pattern size, simultaneously obtainable, is clearly a key feature of the technique).

To compete or complement with other standard micro and nanofabrication technologies, nSL needs to fulfill the following requirements: high resolution, high pattern density, large area and further integration into existing processes, like for example CMOS. This was the purpose of the collaboration undertaken within NaPa project between EPFL and CNM.

I.1.b. Fundamental aspects of the fabrication of a full-wafer stencil by DUV

FABRICATION PROCESS OF STABILIZED MEMBRANES [5, 6]

Limited stencil size is mainly due to the lack of a suitable high-resolution and high-throughput lithography and of MEMS fabrication methods for creating nanoscale structures on large areas combined with well-controlled wafer-through etching of thin solid-state membranes. Serial fabrication technologies like FIB or eBL have been used to obtain apertures at nanoscale, however with limited throughput. Laser interference lithography (LIL) can achieve 100 nm scale patterning on large areas, but is exclusively limited to periodic structures. In order to overcome these limitations for the fabrication of large-area nanostencils with arbitrary apertures, a 100 mm wafer scale combined DUV (Deep Ultra Violet)/MEMS fabrication process was developed at EPFL. Using this method, aperture patterns covering multiple length scales, from 200 nm up to 300 µm,

can be defined in a thin silicon nitride layer by a wafer stepper DUV exposure followed by dry etching. Additional local FIB milling can introduce sub-200 nm features in these stencils.

In order to overcome or limit the effects of membrane deformation, two distinct fabrication processes have been developed in which the membranes were mechanically stabilized. This is done in such a way that the local membrane stabilization does not interfere with the normal stencil deposition process, e.g. the line of sight is not affected by the stabilization. These fabrication processes have resulted in silicon supported SiN membranes and corrugated SiN membranes. The improved micro/nanostencils incorporate in-situ, local stabilization structures increasing their moment of inertia, *I*, which is the structural property directly related to stiffness or deformability [33]. Since the corrugated stabilized stencil membranes add only one process step to the standard stencil fabrication process, it has been tried to combine this stabilization fabrication process with a wafer stepper DUV exposure.

Figure 3 shows a schematic overview of the fabrication process of a full-wafer stencil with corrugated membrane stabilization. The process begins with the definition of stabilization structures or rims by UV lithography and anisotropic dry etching into a double-side polished, 380 μm thick Si wafer (Figure 3a). Then the deposition of 100, 200, or 500 nm thick low-stressed silicon nitride (LS-SiN) by low pressure chemical vapor deposition (LPCVD) follows as illustrated in Figure 3b. Mesoscopic patterns which will form the membrane apertures were defined in a DUV resist via a 4 times reduced projection in a DUV wafer stepper. Transfer of the resist pattern into the low-stress SiN layer was done by means of anisotropic etching (RIE) (Figure 3c).

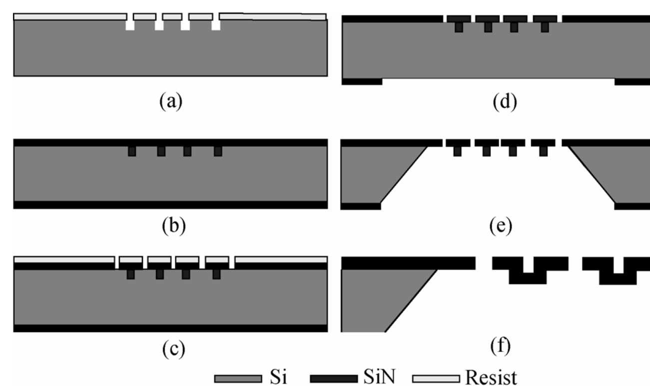


Figure 3 [5]: Simplified schematic illustration of the fabrication process for a corrugated stencil fabrication. (a) definition of stabilization structures/rims; (b) LPCVD low-stress SiN deposition; (c) transfer by RIE of the DUV resist patterns into SiN; (d) membrane etch window definition by backside lithography and pattern transfer (e) KOH etching of bulk Si to release membranes; (f) schematic detail of the corrugated membrane.

The key process parameters for the transfer of the patterned DUV resist into the low-stress SiN layer is the selectivity of the etching agent between the DUV resist mask layer and the SiN structural layer. In order to optimize the pattern transfer conditions, a C_2F_6 gas flow of 20 sccm is used with additional 20 sccm of CH_4. The backside patterns are defined in photoresist by means of conventional photolithography. The SiN layer on the backside is opened using ICP (Inductive Coupled Plasma) anisotropic etching. This backside patterned SiN (Figure 3d) forms the etch mask for the subsequent membrane release (Figure 3e). A schematic detail of the corrugated membrane can be seen in Figure 3f.

DUV RETICLE

The 4 times reduced projection in a DUV wafer stepper of the mesoscopic patterns into a DUV resist required the design and fabrication of a suitable reticule (mask). The general layout of the reticule was designed at EPFL containing several specific designs provided by and for NaPa partners. In our case, the chip design for full-wafer replication of NEMS devices on CMOS was done by us respecting design rules defined by EPFL. Because of the 4 times reduced projection used in the DUV exposure, 200 nm features in a stencil design become 800 nm features in the reticule.

This reticle contains standard structures and markers related to the used exposure equipment (ASML, PAS 5500/700 system). In the middle of the reticule lies an exposure field in which all the designs are placed. The DUV stepper allows exposing one single structure of the reticule on a wafer in contrast to a 1:1 exposure, in which an entire wafer is directly exposed in a single exposure. The step and repeat exposure has been utilized to expose NaPa partner specific wafer stencils and chip-based stencils.

Figure 4 shows a schematic overview of the reticule containing the markers and the individual designs together with two examples of wafers, exposed according to NaPa partner specifications. At CNM, we have made our chip design (presented in the next section) and sent it to EPFL to incorporate it in the exposure field of the reticle: CNM patterns are the so-called “stencil 1” in Figure 4.

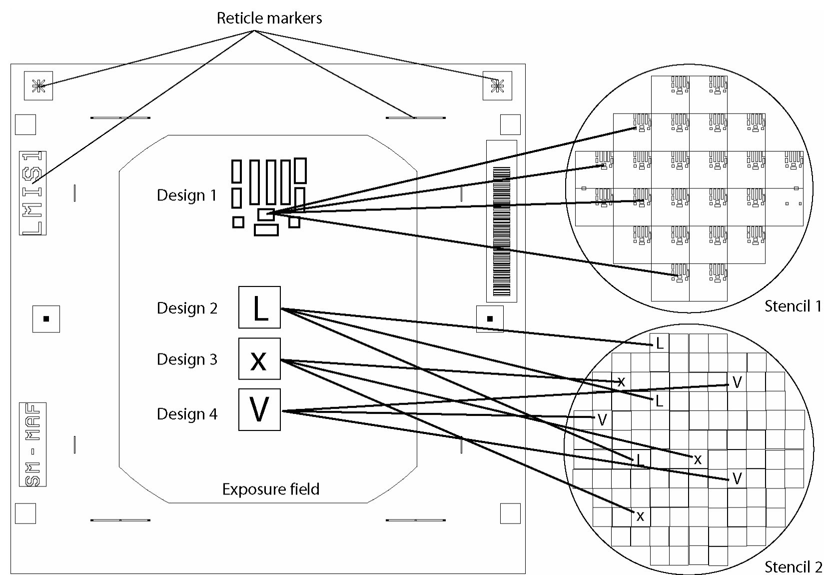


Figure 4. Schematic representation of NaPa reticle and 2 examples of stencils. This reticle contains several designs which can be selectively exposed on custom wafers enabling large freedom in reticle designs.

DUV EXPOSURE [5, 6]

The DUV exposure was done in cooperation with ASML directly at their labs in Veldhoven, The Netherlands. It was realized on a modified PAS 5500/700 system. In order to obtain a higher process window bottom- and top anti-reflective coatings were applied. Four different wafers were exposed of which two wafer designs had a stabilized option integrated. The stabilized series of stencils were exposed with the same setting as the normal stencils.

I.1.c. Specific nanostencil layout for CNM CMOS wafer

The fabricated full-wafer nanostencil contains 24 identical chips (7.5 * 7.5 mm^2) per wafer. The corresponding layout of the chip to replicate had to combine two independent requirements:

- adaptation to nanostencil fabrication and robustness-related design rules:

  SiN membranes are released from the back side of the Si wafer (380 µm thick). This wet etching is made by KOH through photolithographic apertures: consequently the etch profile is not vertical but inclined of 54°. For this reason, two membranes must be separated of at least 0.6 mm. For enhanced stability of non stabilized membranes, their area should not exceed 1 mm^2.

- adaptation to CMOS chip design (and vice versa) for alignment of the resonators patterns (nanostencil apertures) with the integration areas of the CMOS substrate. Actually, both CMOS and nanostencil chip layouts were made interactively to respond to all respective spatial limits: membrane separation and area, CCII circuit size, etc…

Figure 5 depicts a schematic view of the nanostencil layout (chip level) with all the membranes (grey rectangles) and their in-between separation. Table IV - 1 reports the characteristics of each membrane depending on the type of patterned device and whether they contain integrated (connected to a CCII CMOS readout circuit) and discrete (without integrated readout circuitry) devices. We will focus on the study of integrated cantilevers and QB (membranes C, D, E, F and G).

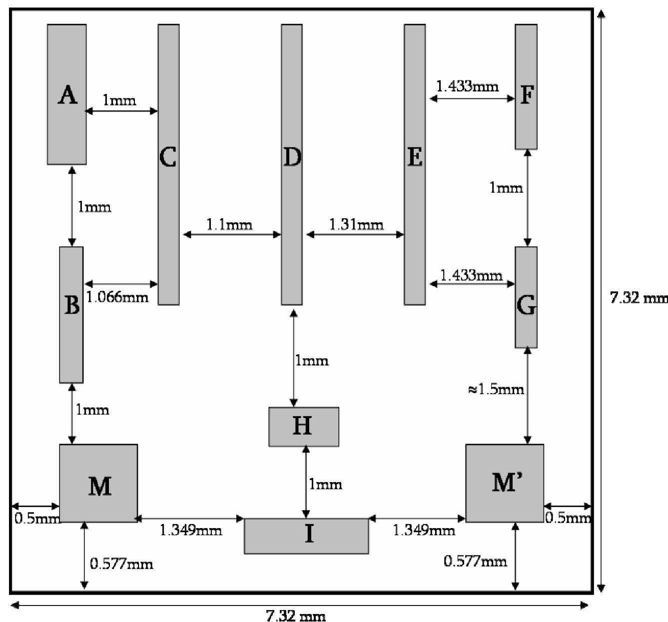


Figure 5. Nanostencil layout at chip level.

Membrane	number and type of devices (apertures)	Area (mm^2)
A	12; discrete paddles	0.9
B	17; discrete paddles	0.51
C	10; int. cantilevers	0.98
D	10; int. cantilevers	0.98
E	10; int. cantilevers and paddles	0.98
F	4; int. QB	0.44
G	3; int. QB	0.36
H	5; discrete paddles	0.45
I	7; discrete QB	0.72
M	set of alignment	1
M'	marks	1

Table IV - 1. Membrane characteristics

In total, there are **78** patterns of nano/micromechanical structures per nanostencil chip, distributed over 9 membranes, 37 of them are integrated with CMOS, the others are discrete. This

number of 37 is not a limitation; the entire chip could have exclusively contained integrated devices. The limiting factor here was the CMOS technology whose big transistors size (gate length 2.5 μm) resulted in big circuit areas.

COMMENT ON ALIGNMENT

Initially, the accuracy of the full-wafer alignment to perform between nanostencil and CMOS wafers was difficult to predict although we targeted it in the sub-10 μm. Therefore, a minimum 15 μm margin between stencil pattern and passivation window was foreseen to make nanostencil alignment easier within the integration area.

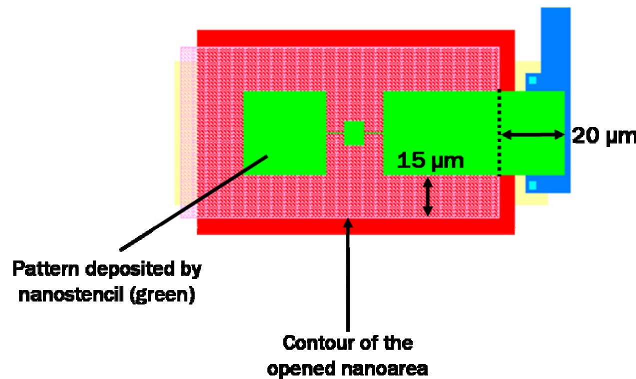
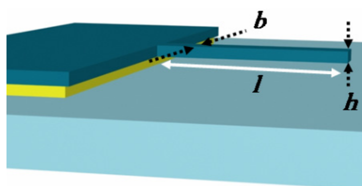


Figure 6: Integration area (in CMOS) + corresponding nanostencil pattern to be defined (in green). The aperture in the passivation layers is depicted in pink. Examples of margin foreseen for the correct insertion of the pattern within the integration area is depicted.

LIST OF DEVICES

Hereafter, we provide the list of nominal dimensions of the devices according to the nomenclature used in the GDS Cadence file. Note that the nominal thickness is 600 nm for all, determined by the CMOS technology.

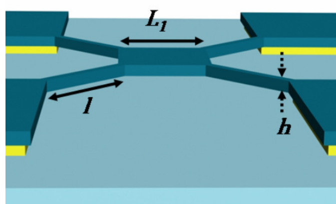
Cantilevers



Name	Characteristics	*l* (μm)	*b* (nm)	*g* (nm)
C1	Simple	14	250	900
CN_2 CI_2	double	14	250	900

l is the cantilever length (μm), *b* its width (μm) and *g* the gap separating from the electrode (μm)

Quad-beams



Name	L_1 (μm)	*l* (nm)	*b* (nm)
A1	14.1	18	600
A2	14.1	18	400
A3	14.1	18	800
A4	14.1	15	600
A5	14.1	21	600
A6	11.1	18	600
A7	17.1	18	600

L_1 is the plate width (μm), *l* the beam length (μm) and *b* the beam width (μm).

I.2. Electron beam lithography

Electron beam lithography (eBL) started its development in early 70s and since then, it has represented an alternative to conventional optical lithography (OL) for the definition of submicron patterns. Actually, eBL consists in irradiating by means of a focused electron beam a surface coated with an electron sensitive resist. eBL is a direct writing technique utilizing electrons as irradiation support, on the contrary to optical techniques that require an opaque mask and light respectively. Physically, enhanced resolution is obtained basically since electronic radiation is not limited by diffraction effects that affect the resolution of OL.

With such an eBL system, a layout is directly written through the spatial monitoring of a high energy electron beam applied upon a surface whose top material (a coated resist) properties are physically or chemically modified by the incident beam. The subsequent step is the development of the sample in order to remove the irradiated part of the resist (if it is positive).

The key parameters determining the efficiency of an eBL step [34] are the beam shape and its characteristics, its electronic energy, electron-matter interactions, resist thickness and molecular structure, the development solution and time, but also the design of the structure to be drawn. In recent years, every element of the system has known a big progress; more stable filaments are now available, beam diameter has been reduced down to few nm, and globally the whole eBL process (electron generation and focus, sample displacement, etc…) is fully automated.

At CNM, our eBL consists of a Scanning Electron Microscope (SEM) completed by a set of electronic devices that control beam deflection and blanking. The SEM system provides the electron source, focusing elements and a movable substrate holder for nano/micropositioning. PMMA (PolyMethilMethaCrylate) is used as a resist.

In industry and research areas, eBL is mainly applied to the fabrication of masks, for device prototyping and fabrication in low amounts. More generally, it is useful in research for very specific applications (nano/microelectrodes patterning, etc…). For us at CNM, the use of eBL is of interest for its high resolution and versatility. Indeed, it allows rapid fabrication of new prototypes, since it is a direct writing method that does not require purchasing a mask each time that first prototypes of a new device have to be produced. In this sense, it is cost and time effective. eBL is also capable of realizing patterns in a large range of dimensions (50 nm - 100 μm).

Nevertheless, intrinsically and comparatively with nSL, eBL suffers a series of limitations. First, the cost of the system is relatively high. Second, its slowness and low throughput must be pointed out. Compared to nSL, OL or NIL which are parallel, eBL is serial what considerably slows the patterning of a full wafer. In comparison with nSL, eBL requires more related process steps: resist coating, exposure, development, metallization and lift-off, in other words five steps, while nSL only requires one evaporation, i.e. one single step (two if counting alignment and clamping).

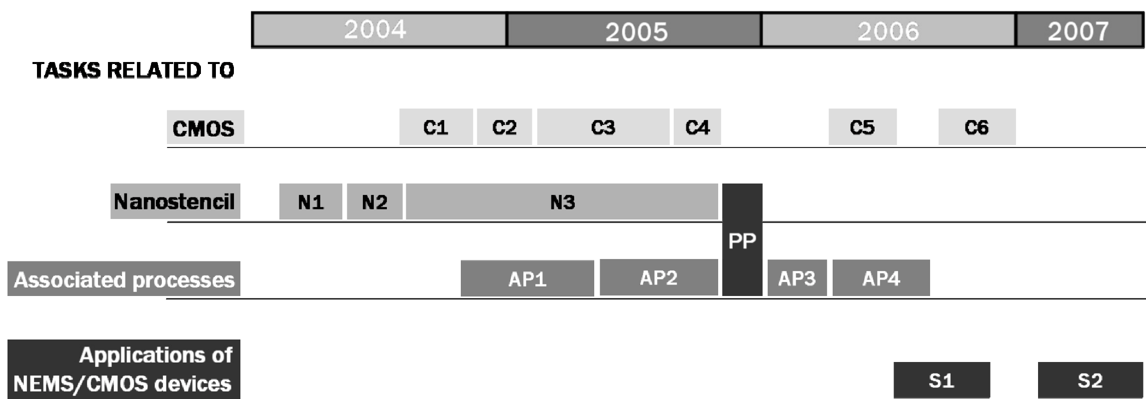
Third, the large quantity of parameters and the complexity of operation imply a low reproducibility of eBL systems. Constant technical support is required and only big foundries can afford having an entire team devoted to the optimization of the system.

Last but not least, some authors have pointed out the fact that eBL degrades the performance of the CMOS circuitry [35] when it is implemented as nanolithography technique for the fabrication of nanodevices on pre-fabricated CMOS substrates. In contrast, in section II.3.f, CMOS compatibility of nSL is discussed: in our samples, no relevant change between before and after post-processing has been observed.

II. Fabrication of micro/nanomechanical resonators on CMOS by nanostencil lithography (nSL)

This work is the result of an intensive collaboration realized with LMIS1 (Microsystems Laboratory 1) from EPFL (Lausanne, Switzerland) in the frame of the NaPa European project, in particular with Dr. Marc .A.F. van den Boogaart, who was pursuing his PhD at this time on Stencil Lithography, and Professor Jürgen Brugger. To less extent, SÜSS MICROTEC also participated in the development of tools for stencil/CMOS alignment, in particular a specific chuck was designed for adapting to a standard SÜSS MICROTEC bond aligner.

Figure 7 shows the time evolution of different tasks related to NaPa project and my thesis. Between the beginning of the project (in 2004) and the first demonstration of device functionality, about 20-22 months passed. It has been a success and further advancements are still in course.



TASKS CORRESPONDANCE

CMOS	Nanostencil (nSL)	Associated processes	Applications of NEMS/CMOS devices
C1: CCII circuit design and simulations **C2:** circuit layout **C3:** circuit fabrication **C4:** circuit pre-test **C5:** tests of CMOS integrated cantilevers **C6:** tests of CMOS integrated quad-beams (QB)	**N1:** design (CNM) and fabrication (EPFL) of 1ST generation of chip-sized stencils **N2:** first tests with non-custom CMOS chips **N3:** design (CNM) and fabrication (EPFL) of full-wafer nanostencils	**AP1:** characterization of 'blurring effect' **AP2:** fabrication of dummy wafers for process tests **PP:** post-processing of CMOS wafers by nSL **AP3 and AP4:** development of release etchings of integrated cantilevers (AP3) and QB (AP4)	**S1:** implementation of NEMS/CMOS as highly sensitive mass sensors to monitor the deposition of ultra-thin gold layers **S2:** implementation of NEMS/CMOS as positioning sensors in quasi-dynamic stencil lithography system

Figure 7. Time evolution of my thesis work for NaPa project

Up to our knowledge, this work represents the first time that patterning of full CMOS wafers with nanostencil lithography is achieved and probably even the first time that a relatively low cost full wafer monolithic integration of nanodevices on CMOS has been demonstrated. Actually, advanced optical lithography can be used to define devices on CMOS at nanometer scale, but it requires the use of expensive equipment and materials, as well as complex processing only available for large microelectronics companies specialized in the fabrication of large series of semiconductor memories and microprocessors. Other emerging lithography techniques have

already been used to pattern devices on CMOS, like e-beam lithography [36], laser lithography [37] or nanoimprint lithography, but none of them had simultaneously demonstrated a reliable and CMOS compatible full wafer patterning.

By combining the technology for the fabrication of nanomechanical resonators with a standard CMOS technology, we present a novel wafer-scale (100 mm) technological process based on post-processing pre-fabricated CMOS circuits using nSL. This approach separates CMOS circuit fabrication and nanodevice fabrication, so that two different lithography techniques for each phase are used. Thus, a rather low-cost nanolithography technique may be implemented on CMOS substrates whose processing does not require an ultra-advanced patterning technique. In this context, nSL is adequate since it is clean (resistless), direct and parallel.

As it will be shown, we have succeeded in the parallel definition and fabrication of multiple (~2000) silicon nanomechanical resonators at the 200 nm scale that are monolithically integrated into CMOS circuits. Further decreasing the resolution should be soon possible.

II.1. CNM CMOS technology

The CMOS circuit fabrication is based on CNM 'in house' process (www.cnm.es) (described in detail in annex A7.1). This technology includes two polysilicon layers and a single metal level. The minimum feature size of the channel length is limited to 2.5 μm. Two different polysilicon layers are employed for specific functions:

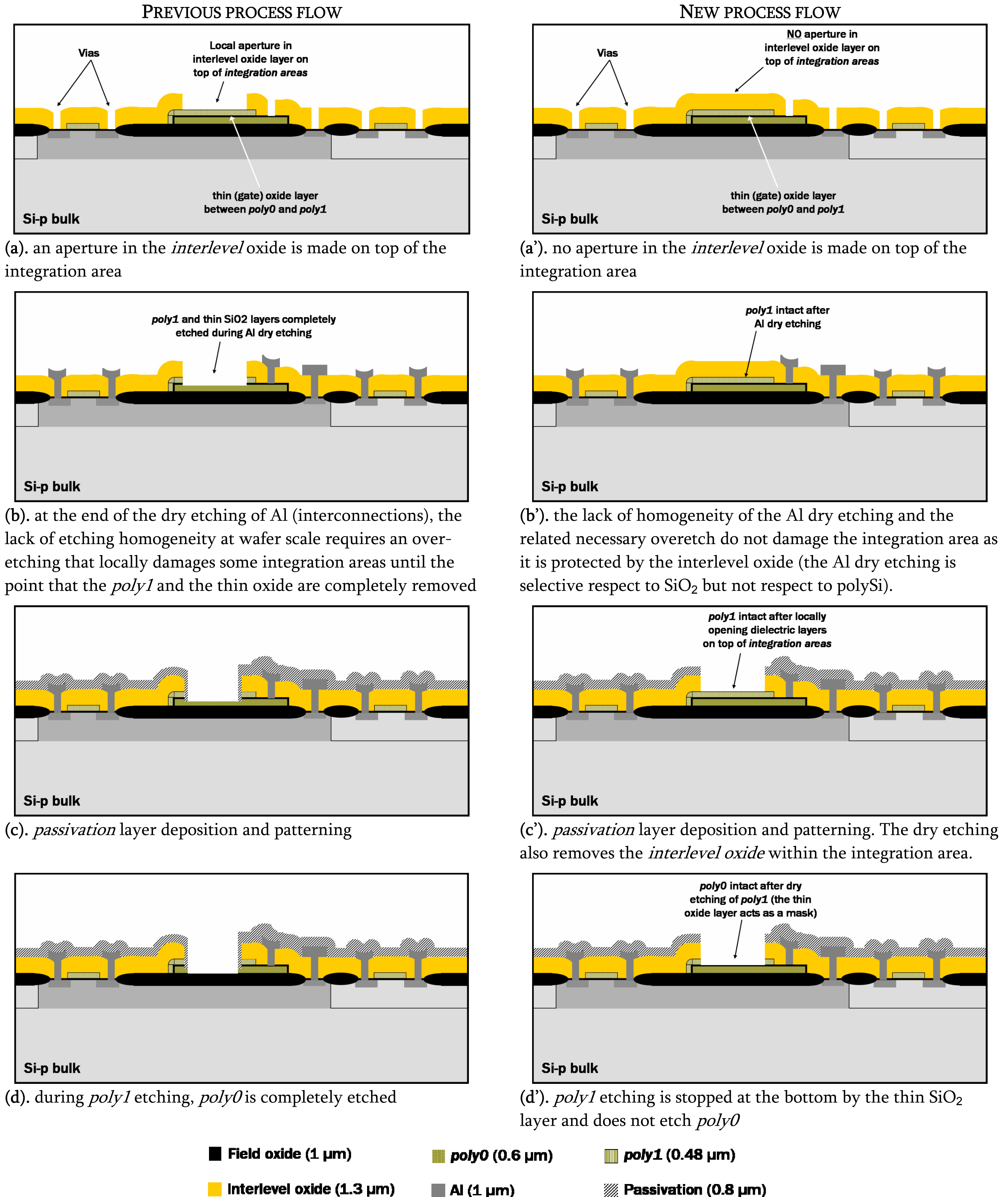
- the so-called *poly0* layer is implemented as a capacitor electrode material
- the so-called *poly1* layer is implemented as transistor gate material

This is not a leading CMOS technology, but it allows a certain degree of flexibility on the process flow; in other words some parameters can be modified. In particular, it has been possible to change the initial deposition parameters of *poly0* in order to improve its crystalline quality so that it may be used as structural layer of the resonator. It has been possible as well to choose its thickness for optimizing the resonator dimensions.

Taking into account the know-how acquired during previous projects, different aspects of the technology regarding the combination with NEMS fabrication have been optimized for reaching a much higher final fabrication yield.

The main modification, that is schemed in Figure 8, has consisted not in changing the process but in modifying the layout of given photolithography masks in order to obtain with high yield viable **integration areas** for posterior integration of nano/micromechanical resonators inside them. Basically, in the new CMOS circuit layout no aperture in the *interlevel oxide* is made on top of the integration areas so that this dielectric layer protects the underlying polysilicon layers during the subsequent metal etching. Indeed, the dry etching of metal is not uniform and from one point of the wafer to another the removal of metal is not realized at the same speed: while in some integration areas some metal still has to be etched, in others the process has already started overetching and damaging the two underlying layers: *poly1* and thin SiO_2.

Now, the structuring by dry etching of *interlevel oxide* within all integration areas is made immediately after the etching of the *passivation* layer with the same masking resist (photolithography reticule nº8 named *passivation*): a single mask level allows opening both layers with a prolonged reactive ion etching (RIE). In this way, the *interlevel oxide* protects the integration area during the whole process.



(a). an aperture in the *interlevel* oxide is made on top of the integration area

(a'). no aperture in the *interlevel* oxide is made on top of the integration area

(b). at the end of the dry etching of Al (interconnections), the lack of etching homogeneity at wafer scale requires an over-etching that locally damages some integration areas until the point that the *poly1* and the thin oxide are completely removed

(b'). the lack of homogeneity of the Al dry etching and the related necessary overetch do not damage the integration area as it is protected by the interlevel oxide (the Al dry etching is selective respect to SiO_2 but not respect to polySi).

(c). *passivation* layer deposition and patterning

(c'). *passivation* layer deposition and patterning. The dry etching also removes the *interlevel oxide* within the integration area.

(d). during *poly1* etching, *poly0* is completely etched

(d'). *poly1* etching is stopped at the bottom by the thin SiO_2 layer and does not etch *poly0*

Figure 8. Previously and newly implemented CMOS process (partial) flows for posterior NEMS integration