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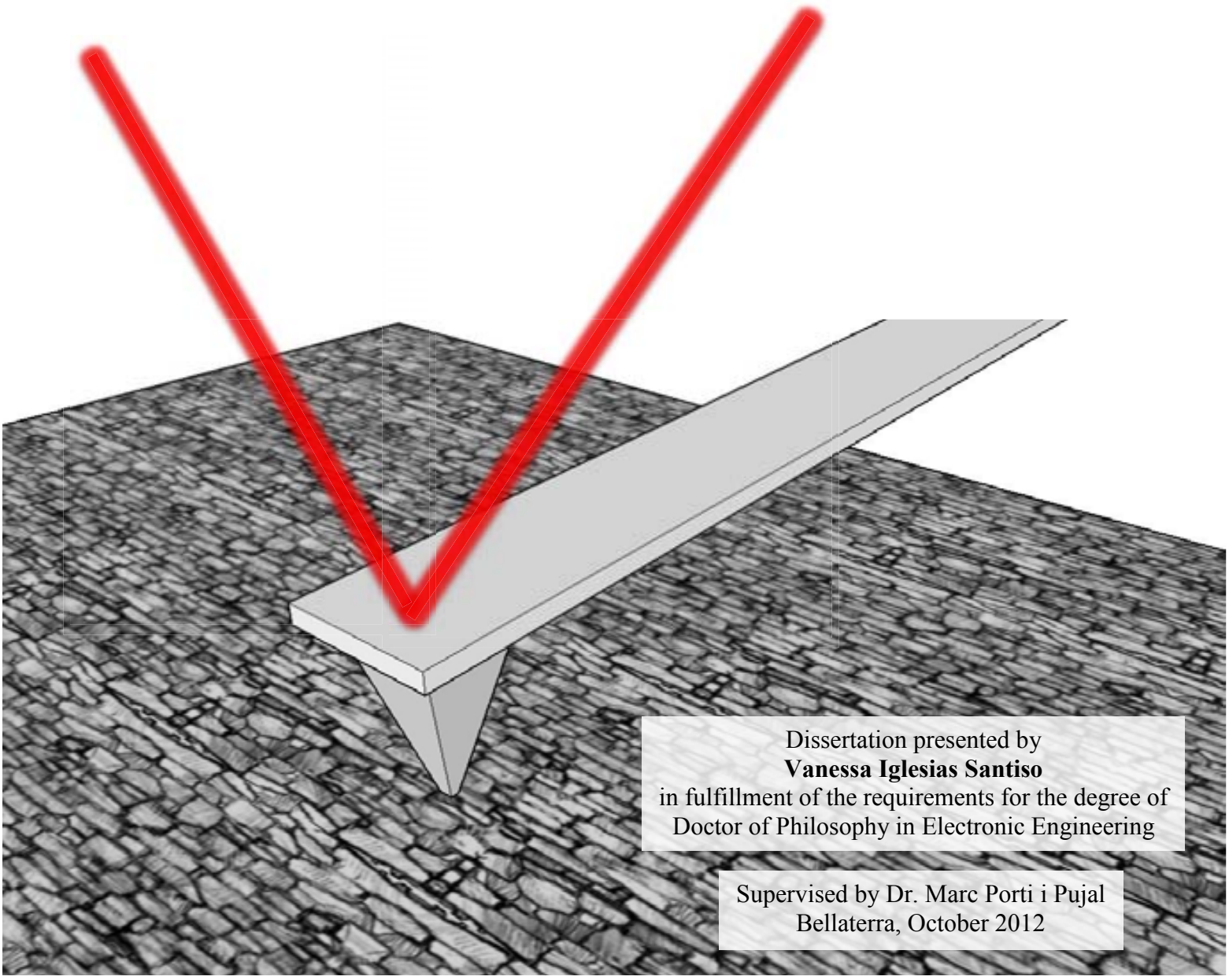
CAFM Nanoscale electrical properties and reliability of HfO_2 based gate dielectrics in electron devices: Impact of the polycrystallization and Resistive Switching



Dissertation presented by
Vanessa Iglesias Santiso
in fulfillment of the requirements for the degree of
Doctor of Philosophy in Electronic Engineering

Supervised by Dr. Marc Porti i Pujal
Bellaterra, October 2012

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Dr. Marc Porti, titular professor of the Electronic Engineering department of the Universidad Autónoma de Barcelona,

Certifies

That the dissertation "**CAFM Nanoscale electrical properties and reliability of HfO_2 based gate dielectrics in electron devices : Impact of the polycrystallization and resistive switching**" submitted by Vanessa Iglesias Santiso to the School of Engineering in fulfillment of the requirements for the degree of Doctor of Philosophy in Electronic Engineering has been performed under his supervision.

Dr. Marc Porti

Bellaterra, October of 2012

Adicado a vós,
ós que sempre estivestes ó
meu carón e confiastes en min

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Index

Publications related to this thesis

COMPENDIUM OF PUBLICATIONS INCLUDED IN THIS THESIS

A) V. Iglesias, M. Porti, M. nafría, X. Aymerich, P. Dudek, G. Bersuker, "Dielectric BD in polycristalline HfO_2 gate dielectrics investigated by CAFM", Journal of Vacuum Science & Technology B Journal Vacuum Science Technology B 29, 01AB02 (2011)

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- V. Iglesias, M. Martin-Martinez, M. Porti, R. Rodriguez, M. Nafria, X.Aymerich, T. Erlbacher, M. Rommel, K. Murakami, A. J. Bauer, L. Frey, G. Bersuker "Temperature dependence of CAFM TDDB distributions in polycrystalline HfO_2 gate stacks: The role of the interfacial layer and grain boundaires", submitted to Electron Device Letters.

1

PRESENTATION

Nowadays it is difficult to imagine a life without electronic devices anywhere. They are so present in our routines that they seem to be there from always. However, electronics beginning is not so far away. In 1883, Thomas Alva Edison discovered that electrons flew from one metal conductor to another through vacuum when a voltage is applied between them. This effect, known as *Edison effect*, was applied in 1904 by John Fleming to invent the *diode*, opening the way to the current electronics. After this, the electronic field evolution was continuous. Different devices appeared (triode, tretode, etc.), but the bipolar transistor development in 1947 by John Bardeen, Walter Houser Brattain and William Bradford Shockley supposed a turning point in the electronics era. The introduction of the transistor allowed, among other things, to reduce the electronic device dimensions as well as to increase its speed. Shortly afterwards, a different type of transistor was developed, the FET (Fiel Effect Transistor), although the theory had been patented previously to the bipolar transistor development. For many years, transistors were made as individual electronic components and were connected to other electronic devices (resistors, capacitors, inductors, diodes, etc.) on boards to fabricate an electronic circuit. They were much smaller than vacuum tubes, faster and consumed much less power. However, circuits based on individual transistors became too large and too difficult to be assembled. To improve them it would be necessary to pack the transistors closer and closer together. To solve that, in 1959, Jack Kilby and Robert Noyce developed the integrated circuit. Silicon-based integrated circuits (ICs) have become the backbone of today's semiconductor world, being the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) his main, more common and important device.

For more than 45 years, since the 1960's, the number of transistors per unit area has been doubling every 1.5 years, leading to an important shrinking in the transistor size. However, this continuous miniaturization has found its physical limits. For example, the thickness reduction of SiO_2 dielectric layer, with current sizes at nanometric scale, has become a crucial issue in the scientific comunity since it is being affected by quantum phenomena, as for example, tunneling current. Thickness scaling down leads to larger leakage currents (implying a higher power consumption) and, consequently, to an impoverishment of the reliability of the transistor. At this point, it seems inevitable the introduction of some variations in the present technology as well as the research of different alternatives. From the different proposed solutions, the SiO_2 replacement by other materials, as high-*k* dielectrics, could be an alternative. However, although it sounds simple it is really a complicate issue. The introduction of new materials has associated new challenges and difficulties that must be solved as soon as possible to

achieve the semiconductor company's request. The main problems related to the use of high-*k* dielectrics based stacks are: i) high density of intrinsic defects, ii) no good interaction with the gate electrode, iii) unavoidable formation of a SiO_2 layer at the interface with the Silicon substrate, iv) poor carrier's mobility at the conductive channel due to scattering phonons, and v) polycristallization of the high-k dielectric when it is subjected to high temperatures during the manufacturing process, which can alter the electrical properties of the device, among others.

Since many of the problems associated to these materials (like, for example, their polycrystallization) and the failure mechanisms that affect the gate oxide are phenomena that have been found to have a nanometric origin, it seems logical to study them at the same scale to obtain an accurate knowledge. Different tools as the Scanning Probe Microscopy based techniques have recently been used to perform such nanoscale analyses. Among them, especially when studying the electrical properties and reliability of gate dielectrics, the Conductive Atomic Force Microscope (CAFM) has been the most used until now. This technique is capable to obtain simultaneously and independently topographical and electrical information at the nanoscale, achieving lateral resolutions of the order of 10nm.

Following this line, this thesis is focused to evaluate, mainly with CAFM, the influence of the polycrystallization on the electrical properties and reliability of a high-*k* based gate stack. In chapter I, the MOSFET, basic component of present microelectronics, is introduced. Among other things, its evolution and different problems related to its scaling down are described. High-*k* dielectrics are also introduced in this chapter as well as different characterization techniques to achieve a nanoscale resolution.

Chapter II is devoted to describe in detail the main characterization tool used in this work, the Atomic Force Microscope (AFM), and two related techniques, which are important to study the electrical properties and reliability of gate dielectrics: CAFM and Kelvin Probe Microscope (KPFM).

Chapter III is focused on the description of the sample characteristics used in this work and the search of optimal experimental conditions to perform the CAFM measurements with the highest resolution.

Chapter IV presents the main aim of this work. It is known that some high-k materials, as for example HfO_2, could change its morphology as a consequence of high temperature manufacturing processes. In this chapter, a deep study about the impact of the high-k layer polycristallization of HfO_2 based gate stacks, after an annealing process, on the gate stack electrical characteristics and reliability is shown. The study has been carried out at the nanoscale using, mainly, a CAFM.

Finally, chapter V introduces the analysis at the nanoscale of high-k materials in the field of non-volatile data memories (NVMs). Specifically, in the Resistive Random Access Memory (RRAM) technology, based on a reversible and repeatable change of the resistance (Resistive Switching, RS) of a metal-insulator-metal (MIM) memory cell. The RS phenomenon is analysed at device level and at the nanoscale with CAFM.

CHAPTER I

Introduction

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the main, more common and important device in the silicon-based integrated circuits. It is present in almost every electronic set, having, therefore, a relevant position in the microelectronics field. In this chapter, firstly, the basic concepts of a MOSFET transistor are introduced as well as the consequences of the continuous shrinking of MOS devices and the possible alternatives to avoid these consequences. High-*k* dielectrics and associated failure mechanism, as dielectric breakdown (BD), are also introduced. Resistive switching, which will be also treated in chapter V, based on the creation of reversible conductive filaments (probably related to reversible BD events) is presented too. In the second part, the attention will be centred in the different characterization techniques normally used to study the electrical properties and reliability of MOS devices: standard characterization techniques and tools with nanometric resolution, as Conductive Atomic Force Microscope (CAFM).

1.1 The MOSFET transistor

1.1.1 Basic principles

The MOSFET is based in the Metal Oxide Semiconductor (MOS) structure, illustrated by Figure 1.1. A traditional MOS structure consists of a semiconductor substrate, which can be p or n-type, with a thin silicon oxide layer and a polysilicon contact, referred to as the gate [Pierret 96]. Before 1970, the gate was typically made of metal. After 1970, heavily doped polycrystalline silicon was used as the standard gate material because of its ability to withstand high temperature without reacting with SiO_2. After 2007, the trend has been to reintroduce metal gate and replace SiO_2 with more advanced dielectrics (see section 1.2). As the oxide is a dielectric material, its structure is equivalent to a planar capacitor with one of the electrodes replaced by a semiconductor.

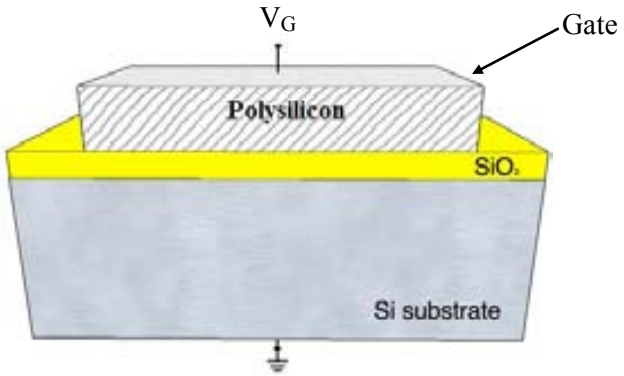

Figure 1.1: Traditional MOS structure consisting of a semiconductor substrate, which can be p or n-type, a silicon oxide layer as dielectric and a polysilicon contact as gate

The energy band diagram of an ideal MOS structure is drawn in figure 1.2. The oxide is situated in the middle meanwhile the gate and the substrate are on the left- and right-hand sides. In an ideal situation there is no charge in the oxide or at SiO_2/Si interface and no band bending that usually occurs as a consequence of the different values of metal and semiconductor work functions (Φ, defined as the energy needed to move an electron from the Fermi level into the vacuum).

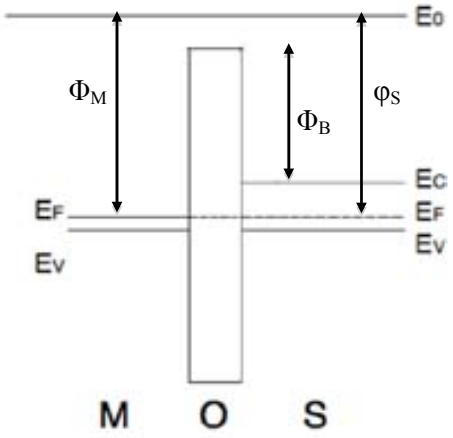

Figure 1.2: Energy band diagram for an ideal MOS capacitor. Φ_M and Φ_S are the metal and semiconductor work functions respectively. Φ_B is the electron energy barrier

Assuming a p-type Si substrate three modes can be distinguished in a MOS capacitor depending on the applied bias between the gate (V_G) and the substrate (V_S): accumulation, depletion and inversion.

If the applied voltage is $V_{GS}<0V$, a large number of holes are attracted to the surface (figure 1.3(a-top)). Looking at the band diagram (figure 1.3(a-bottom)), it can be observed that the band edge on the gate side shifts upwards. Consequently, E_v (valence energy) is closer to E_F (Fermi energy) at the oxide/semiconductor interface than in the bulk and therefore, the surface hole concentration, *p*, is larger than the bulk hole concentration, forming an accumulation layer at or near the interface. This regime is known as *accumulation*.

If a positive V_{GS} is applied, the positive charge in the oxide/semiconductor interface is pushed away into the substrate. Therefore, the semiconductor is depleted of mobile carriers at the interface and a negative charge, due to the ionized acceptor ions, remains in the space charge region figure 1.3(b-top). Looking at the band diagram it can be observed that the band edge on the gate side shifts downwards figure 1.3(b-bottom). In this case, a depletion region is formed since E_F is far from both E_c (conduction energy) and E_v. This regime is known as *depletion*

If V_{GS} is high enough, free electrons (minority carriers in a P-type substrate) are attracted to the insulator/semiconductor interface increasing the density of the negative charge (figure 1.3 c-top). From the band diagram is observed that the band edge on the gate side shifts downwards further (figure 1.3(b-bottom). At some values of V_G, E_F will be close enough to E_c at the Si/SiO_2 interface, becoming this, rich in electrons figure 1.5(b) (minority carriers) and, therefore inverting the interface from P type to N type. This regime is known as *inversion*. The minimum voltage required to generate this situation is known as threshold voltage, $V_{TH.}$

An analogue behaviour can be described for a MOS structure with a n-type silicon substrate. However, in this case, the different operation modes are reached by applying inverted polarities. It is important to remember that the behavior described until now corresponds to the ideal situation, which occurs when no charge is trapped in the oxide and the work function difference between metal and semiconductor metal (Φ_{ms}) is zero (the work function is defined as the energy needed to move an electron from the Fermi level into vacuum). However, this is not normally true and, moreover, the presence of charge in the oxide cannot be ruled out. Therefore, it is necessary to add a voltage to achieve the flat band conditions, defined as the situation in which there is no internal potential difference across a metal-oxide-semiconductor structure.

The MOS capacitor is not a widely used device in itself, but it is the basic part of the MOS transistor (MOSFET), by far the most used semiconductor device. The MOSFET is a four-terminal device with a source (S), gate (G), drain (D), and bulk (B) (or substrate) as electrodes (figure 1.4). Its working principle is based on the modulation of free carriers' concentration at the channel (oxide-semiconductor interface) by the polarization of the MOS capacitance. Depending on the type of carriers through the conduction channel (i.e. the inversion layer), the MOSFET can be classified as N-MOSFET (electron through the channel) or P-MOSFET (holes through the channel). Combination of both, P-MOSFET and N-MOSFET are used to construct integrated circuits (ICs). This technology is known as Complementary Metal Oxide

Semiconductor (CMOS).

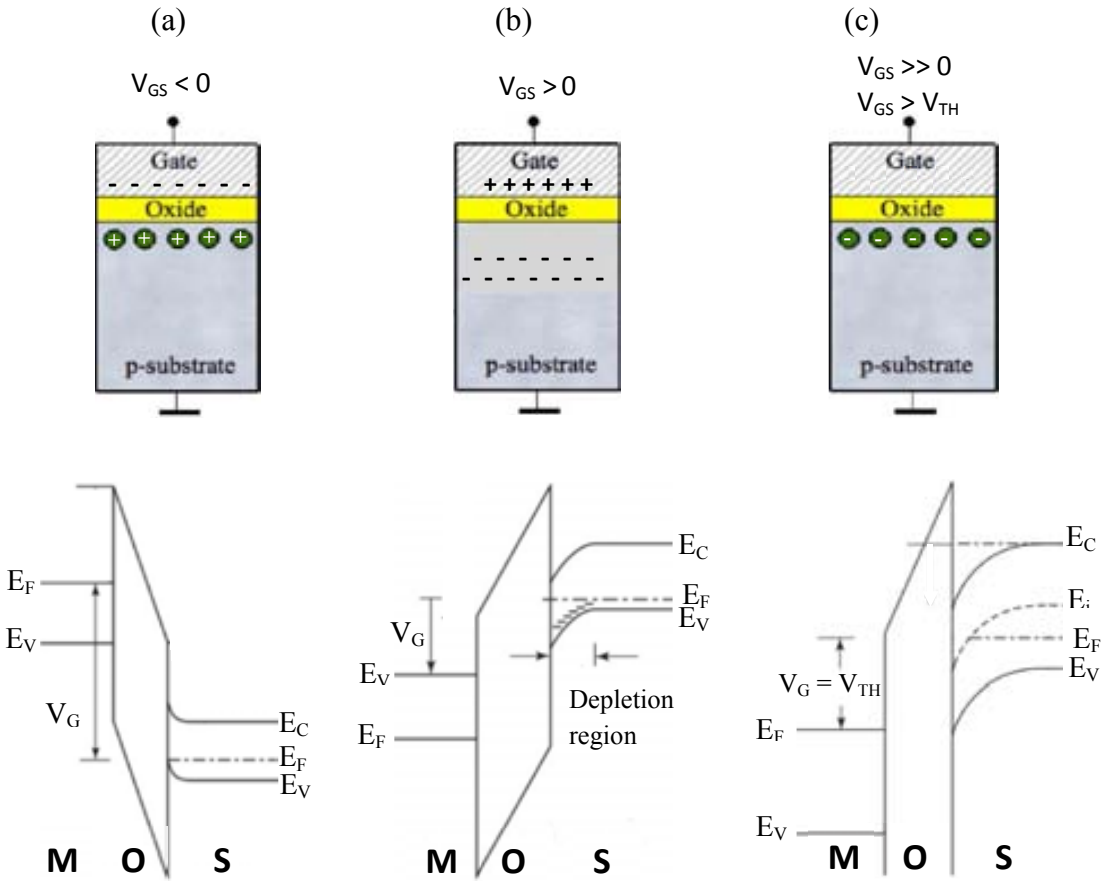

Figure 1.3: Different modes of an ideal MOS capacitor: (a) accumulation (b) depletion (c) inversion. On top, the types of charges present on the insulator/semiconductor interface are represented. On bottom, the energy band diagrams are shown.

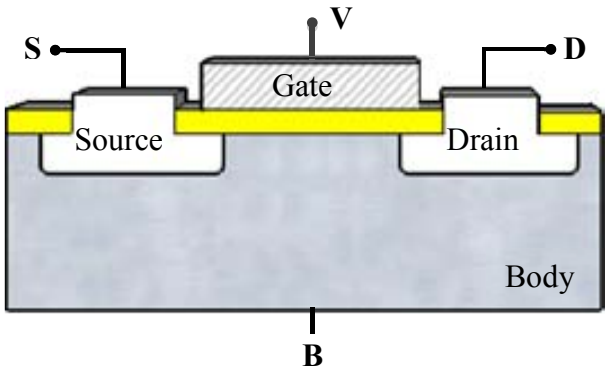

Figure 1.4: Cross-section of an Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET).

Depending on the applied voltage at the terminals, three different modes can be defined: a) cutoff or weak-inversion mode, b) ohmic mode or linear region, and c) saturation or active mode [Pierret 96 [I]].

If $V_{GS} < V_{TH}$ the inversion channel is not created at the interface and the transistor is turned off, that is, there is not conduction between source and drain (I_{DS}) even when a V_{DS} is applied. This is known as *cutoff* or *weak inversion mode*.

If $V_{GS} > V_{TH}$ and $V_{DS} < (V_{GS} - V_{TH})$, the transistor is turned on and a channel, which allows current to flow between the drain and the source, is created. The current flowing through the channel is defined as (1.2):

$$I_{DS} \approx \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2\right) \qquad (1.2)$$

were μ_n is the carrier mobility, C_{ox} the oxide capacitance, W the channel width, L the channel length and V_{GS}, V_{TH} and V_{DS} are the gate-source, threshold and drain-source voltage, respectively. In this region, the MOS transistor acts as a variable resistor controlled by the gate voltage relative to the source voltage. This is known as *ohmic* or *linear mode*.

If $V_{GS} > V_{TH}$ and $V_{DS} \geq (V_{GS} - V_{TH})$, the channel is "pinched off" at the drain end, and I_{DS} saturates. That is, I_{DS} becomes, in first approximation, independent of the drain voltage. This is known as saturation mode. Figure 1.5 shows the typical I-V characteristics for the different modes for a N-MOSFET. Note that the behaviour above described corresponds to the ideal situation.

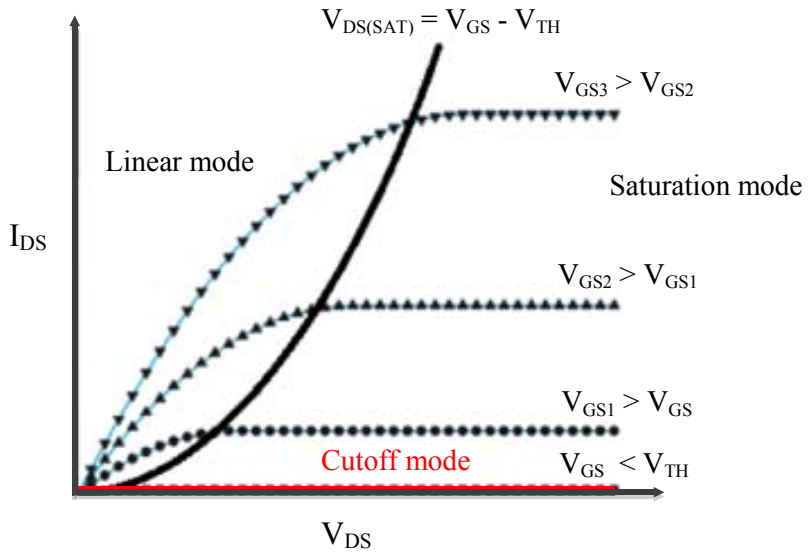

Figure 1.5: I_{DS}-V_{DS} characteristics of an n-channel MOSFET for different V_{GS} voltages. Depending on the V_{GS} and V_{DS} values, different operation modes can be described.

1.1.2 MOSFET scaling

Over time, the reduction of the MOSFET dimensions has been continuous [Dennard 74, Baccarani 84, Critchlow 99, Frank 01]. Starting from a channel length of 10 mm in the 1960s, channel lengths of approximately the mean free path of charge carriers have been reached nowadays. This is known as scaling. There are several reasons for this continued size reduction. The main reason is to pack more and more devices in a given chip area. From an economical point of view, since fabrication costs for a semiconductor wafer are relatively fixed, the introduction of more chips per wafer reduces the price per chip. Moreover, smaller transistors switch faster and the power consumption decreases significantly with the down-scaling [Wilk 01]. In 1965, Gordon Moore, Intel co-founder, predicted that the number of transistors on a chip would double every year [Moore 65] although later, he actualized it to approximately every two years. Nowadays this prediction is known popularly as Moore´s law.

During long time, the scaling rules were governed by two scaling methods: constant field scaling and constant voltage scaling [Dennard 74, Critchlow 99]. On one hand, constant voltage scaling proposed to maintain the applied voltage constant, while the dimensions of the MOSFET were scaled down. The associated disadvantage was the increase of the electric field as the minimum feature length was reduced, leading to: velocity saturation, mobility degradation, increasing leakage currents and lower breakdown voltages [Critchlow 99]. On the other hand, constant field scaling rules proposed to shrink MOSFET dimensions by a factor α to get a smaller FET with similar behaviour. To do that, all voltages and dimensions have to be reduced by the scaling factor α, meanwhile the doping and charge densities have to be increased by the same factor, maintaining constant the electric field inside the FET. This scaling methodology leads to an increase in the velocity of the circuit proportional to α . In addition, circuit density increases proportionally to α^2. However, residual current increases due to the threshold voltage reduction [Frank 01, Ghani 00]. Since the 'further scaling' of threshold voltage lead to large off state drain leakage currents, more generalized scaling rules were redefined during the 80´s. The *generalized scaling* approach, were the voltage is not scaled as fast as the dimensions, allows to increase the electric field by a factor ε [Baccarani 84], being ε the scaling parameter, which usually describes the size-reduction. Although the scaling trend during the last decades of the past XX century was more aggressive than during the last 10 years, leading to a general believe that the end of Moore´s law was close, on February of 2012, Intel announced a new device which assures that Moore´s law will continue, at least for some more generations [Intel].

However, despite the advantages of the scaling, the MOSFET dimensions reduction has also some drawbacks that must be considered in detail. One of the consequences of such scaling process of the MOSFET is the reduction of the gate oxide thickness which leads to the appearance of what is known as tunnelling current through the gate oxide. Tunnelling current through the gate oxide is a quantum phenomenon by which the gate current (current between the gate and the substrate, I_{GS}) is different of zero when a V_{GS} is applied (ideally it should be zero due to the presence of insulators). It was noticed as a significant source of leakage and greatly increased power dissipation in the 90s decade for the first time [Momose 94].

According to the tunnelling theory [Sanchez del Río 99], an important parameter that determines the magnitude of the tunnelling probability is the width of the potential

barrier. In MOSFETs, the element that plays the role of a potential barrier is the gate dielectric. Therefore, when the oxide thickness decreases, the width of the energy barrier is reduced, facilitating electrons tunneling through the insulator layer [Lee 01, Clerc 02, Gehring 04] as figure 1.6a shows.

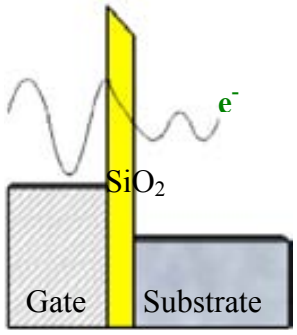

Figure 1.6: Tunneling current in a MOSFET.

Different conduction modes can be described for the gate tunneling current, which are easily understood by analyzing the energy band diagram of the MOS structure [Lee 01]. Taking into account the shape of the energy barrier, Direct Tunneling (DT) and Fowler-Nordheim (FN) tunnelling are considered. If the oxide tunnel barrier is trapezoidal, DT occurs while FN takes place through a triangular barrier (figure 1.7). The transition from FN to DT occurs when the difference in potential energy over the oxide layer qV_{ox} becomes smaller than the tunnel barrier height Φ_B, at the injecting interface [Depas 95]. In addition to the applied electrical field, the dominant conduction mechanism through the oxide (DT or FN) also depends on the oxide thickness. For small voltages and thin oxides the dominat tunneling mechanism is the DT, while for thick oxides and high electrical fields the dominant tunneling mechanism is the FN [Degraeve 99]. A more strict analysis of the conduction modes can be found in [Gehring 04, Yang 04].

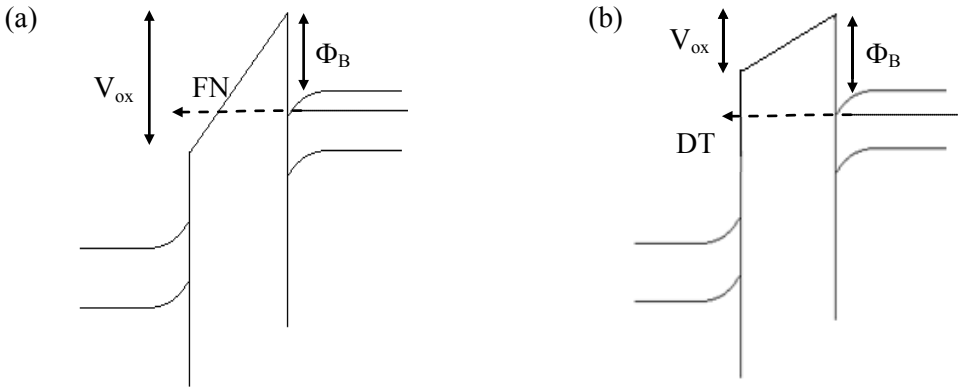

Figure 1.7: Schematic energy band diagram in the case of (a) Fowler-Nordheim tunneling (FN) and (b) direct tunneling (DT) current

Due to the continuous SiO_2 layer thickness shrinking in a MOS transistor, tunnelling current increased more and more becoming the dominant source of device leakage. The main consequences of this leakage current enlargement are, on one hand, the consumption increase in standby power [Lo 97] and, on the other hand, the impoverishment of the reliability of the device. This impoverishment can be understood as an increment of the probability that the device failure happens for shorter times than usually.

At this point, the scientific community was forced to look for different alternatives since the perfect SiO_2 layer had reached his physical limit. In 2007, materials with higher dielectric constant were chosen as alternative to the SiO_2 layer to reduce the tunnelling current and also to avoid reliability issues [Yuan 97, Momose 94]. However, even with these materials, further scaling will be also required for future conventional CMOS generations. For example, the International Technology Roadmap for Semiconductors (ITRS) predicts an EOT of 0.55 nm for high-performance logic transistor on bulk Si in the year 2017 [ITRS], substantially lower than the currently 0,84-0,79 nm. The first idea that comes to mind is to reduce the physical thickness of the high-k layer, however, this is not a solution because this would increase gate leakage current again. The different options that are being taken into account are: (i) To introduce a new high-k material with k-value greater than the actual Hf-based oxides; (ii) To increase the k-value of IL; (iii) To reduce the physical thickness of IL [Frank 09, Frank 11, Ando 12]. Nowadays, devices with alternative architectures are also being investigated as possible replacements for the classical CMOS structure. Silicon on Insulator (SOI) MOS transistors and, especially multigate field-effect transistor (multigate FET) are acquiring an outstanding position to be the next generation of transistors [Colinge 04]. In fact, Intel has recently presented a new technology at 22nm based in 3D FinFET [sale en junio]. Anyway, high-k materials are also used in these new technologies so a better knowledge about them is mandatory. For this reason, high-k are the main topic of this thesis.

1.2 High-*k* dielectrics

The substitution of the SiO_2 layer by high-k dielectrics allows to reduce the prohibitive leakage current through SiO_2 based gate stacks as gate oxide thickness is scaled down. This replacement makes necessary the introduction of a new parameter to describe the electrical behavior of the transistor: the Equivalent Oxide Thickness (EOT). EOT, described in (1.3), is defined as the equivalent thickness of a SiO_2 layer needed to obtain the same capacitance than the one obtained by the high-*k* dielectrics:

$$EOT = \frac{K_{SiO_2} \cdot t_{high-k}}{K_{high-k}} \tag{1.3}$$

where K and t are the dielectric constant and physical thickness, respectively, of the materials indicated in subscript (high-k and SiO_2).

With the substitution of the SiO_2 by high-k dielectrics, equivalent performance can be obtained for the capacitance with a larger physical thickness (figure 1.8) and, therefore, reducing the leakage current. In addition, with the introduction of high-*k* gate insulators at the 45nm technology [Mistry 07], the poly-crystalline silicon gate electrode was replaced by metals [Chau 04, Gusev 06, Chudzick 07, Guha 09] in order to avoid the

channel mobility degradation because of poly-Si/high-*k* interface [Gusev 01, Lee 03].

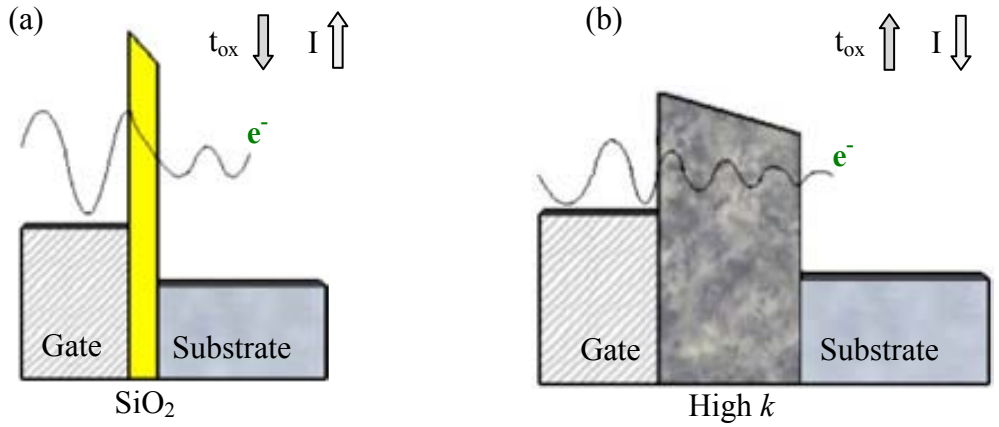

Figure 1.8: Schematics representation of the leakage current reduction (meanwhile the capacitance remains unalterable) in a MOS structure when a SiO_2 dielectric (a) is replaced by a high-*k* dilectric (b)

However, the substitution of the SiO_2 by high-k dielectrics has not been an easy task. Mainly because the only inconvenient of SiO_2 is its lower dielectric constant while high-k dielectrics are materials with, in principle, only one advantage (a higher dielectric constant) and a lot of drawbacks. Despite the rapid increase in the understanding of high-k dielectrics, a lot of unresolved problems on their electrical performance and reliability still lie ahead. It was recognized that high-*k* materials knowledge is not enough mature to replace the traditional poly-Si/SiO_2 gate stack while simultaneously ensuring sufficiently low EOT, leakage current, appropriate threshold voltages and good reliability. It is unnecessary therefore, to say that a better knowledge about these materials is mandatory. Some of these problems are associated to the material itself as well as on the processing technology. For this reason, during the last years, the physical and electrical properties of several metal oxides as ZrO_2, Al_2O_3, Y_2O_3 and La_2O_3 (among others) were studied as candidate materials [Wilk 01, Qi 99, Chin 00, Ragnarsson 01, Wu 00]. Among them, the semiconductor industry converged on Hf-based oxides, such as HfO_2 (k ~20-25) or $HfSi_xO_y$, for the first CMOS generation (45 nm technology) products featuring high-*k* gate dielectrics and metal gate electrodes (HKMG) [Mistry 07, Jan 09]. However, although two distinct integration schemes are being pursued currently for metal gate/high-k transistor fabrication, "gate-first" and "gate-last" integration [Kesapragada 10], the contact between HfO_2 and Si-substrate is not totally under control [Miyata 12]. The fabrication process of devices based on HfO_2 dielectrics can lead to an interfacial SiO_2 layer (IL) between both, high-*k* and Si-substrate, which can increase the EOT of the structure (figure 1.9). The IL layer, in addition to the high-*k* layer, results in a system that is equivalent to two capacitors connected in series. For that reason, the total EOT of the HKMG stack can be expressed as it is indicated in (1.4).

$$EOT = EOT_{IL} + EOT_{HK} \tag{1.4}$$

Where EOT_{IL} and EOT_{HK} are contributions from the IL and high-*k* layer, respectively.

In figure 1.9, a typical HKMG stack structure is compared with a stack based in SiO_2 gate.

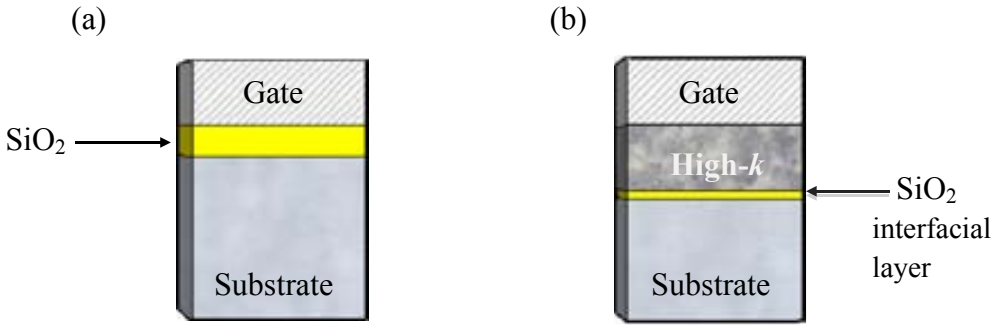

Figure 1.9: SiO_2 gate stack (a) compared with typical high-k metal gate stack (b). In (b), a SiO_2 interfacial layer appears increasing the EOT of the stack.

The morphology of the high-k material and its impact on the electrical properties of the stack is another important factor to be considered. High-k dielectrics can show polycrystalline, epitaxial crystalline or amorphous structure. The epitaxial crystalline layers show a good interfacial behavior with Si. However, this option requires great efforts since its manufacturing process is more difficult and expensive, increasing the cost of the device. For this reason, amorphous layers are generally the preferential option for several reasons such as low cost because of high compatibility with the existing fabrication process, lower density of interfacial defects and isotropic behavior which minimizes the carrier's dispersion and degradation of the mobility [Robertson 04]. However, most of the amorphous high-k dielectrics tend to polycrystallize either during deposition or after heat treatment in a traditional CMOS process. This involves drawbacks, such as, inhomogeneity in their electrical behaviour and fluctuations of the dielectric constant along the stack due to the different orientations of the poly-crystals and the presence of grain boundaries (GB) [Chowdhury 10]. The impact of polycrystallization is an interesting issue to be analysed since its influence in the electrical behaviour is not well understood. Some works state that GBs act as conductive paths [Yanev 08, Bayerl 11] while others suggest that GBs do not have influence in the conduction through the dielectric [Kim 04]. The GBs influence in the electrical behaviour of a polycrystalline high-k layer, specifically HfO_2, is treated in more detail in chapter IV as one of the main topics of this thesis.

It must also be considered that the introduction of new materials is generally associated with new reliability challenges that must be deeply studied. High-*k* materials introduce novel reliability phenomena, related to the asymmetric gate band structure and the presence of fixed charge, as well as degradation mechanisms already known for SiO_2 based technologies [Oates 03, Degraeve 08, Stathis 10, Ribes 05]. Although on the whole, most of the models and concepts that had been developed for SiO_2 reliability could be maintained on high-k stacks [Degraeve 08], the transfer of knowledge about SiO_2 properties and degradation mechanisms to the high-k dielectrics should be done very carefully due to the significant physical differences between both. For that, a better understanding is required for both, new and already known mechanism, since the behavior of well-known failure mechanisms could change [ITRS].

The most important high-k dielectric degradation and failure mechanisms are:

- *Charge Trapping*. High-*k* dielectrics have been known to be "trap-rich" materials. Significant amount of charge trapping centers that affect to device parameters, such as threshold voltage stability and drive current, are enclosed at high-*k* dielectrics films [Ribes 05, Shajan 04, Kerber 02, Minseok 07]. Nevertheless, the existence of these traps is not always a disadvantage. Since charge trapping could be a reversible phenomenon, some companies as Samsung, have developed flash memories based in charge trapping effects [Lee 05].

- *Negative/Positive Bias Temperature Instability* (NBTI/PBTI) is defined as the shift of the threshold voltage in a PMOS/NMOS transistor when a negative/positive voltage is applied to the gate at elevated temperature. NBTI is associated with positive charge trapping [Degraeve 08, Neugroschel 08]. PBTI is associated with negative charge trapping. Meanwhile PBTI was insignificant in NMOS transistors with SiO_2, in SiO_2/high-*k* it becomes an important reliability issue [Degraeve 08, Shimokawa 09].

- *Channel Hot Carriers* (CHC). Charge carries are accelerated by the large electric field across the channel of a MOSFET acquiring kinetic energy. Those carries that gain a very high kinetic energy are called hot carriers (HC). Hot carriers can generate electron-hole pairs near the drain due to impact ionization from atomic-level collisions. Moreover, HC can be injected into the gate channel interface, damaging the dielectric and causing threshold-voltage shift. [Amat 09, Amat 11, Amat 10]

- *Stress Induced Leakage Current* (SILC) is defined as an increase in the gate leakage current of a MOSFET, due to defects created in the gate oxide during electrical stressing.

- *Dielectric breakdown* (BD) is related to the loss of the dielectric properties of the gate oxide when the stack is subjected to an elevated electrical field. The changes of the electrical properties of the oxide after breakdown, can lead to the device or even circuit failure [Martin-Martinez 12].

Since, among the different failure mechanisms described above, the analysis of the BD of HfO_2/SiO_2 based gate stacks will be part of this thesis, next section will be devoted to briefly introduce the main concepts and models related to this failure mechanism.

1.3 Dielectric Breakdown

1.3.1 SILC and percolative model

As noted above, BD is related to the loss of the dielectric properties of the gate oxide. As consequence of the changes on its dielectric properties, the failure of the device or even of the circuit [Martin-Martinez 12, Degraeve 01] could occur. For this reason, gate-oxide breakdown is one of the key reliability issues in MOSFETs. BD is characterized by a strong increase of the current through the oxide, which can be several

orders of magnitude greater than the current measured on a fresh (before BD) structure. Although BD has been intensively studied for more than two decades, there is not general consensus about its physical origin. Nevertheless, the percolation model, which describes the BD process, is widely accepted [Degraeve 98, Stathis 99, Nigam 09, Suñe 10, Raghavan 12]. According to this model, BD is the consequence of a degradation stage of the oxide microstructure [Lombardo 05], which has been related to the generation of defects during an electrical stress. The oxide degradation induced during an electrical stress can be understood as a continuous creation of traps, which lead to local energy levels in the bandgap of the oxide, facilitating trapping of charges in these defects tunnelling carriers from cathode to anode depending on the oxide thickness. In the last case, it is important to note that the measurement of the progressive increase of the gate leakage current during the degradation stage (SILC) could also give information about the degradation mechanism.

SILC is principally observed in oxides from 3 to 7nm thick [Jahan 99]. In thicker oxides, trapping charge at the generated defects becomes dominant while in thinner oxides, SILC is masked by Direct Tunnelling current. Even in 3-7nm thick oxides, SILC is basically measured at low fields, since at high fields is masked by Fowler-Nordheim tunnelling current [DiMaria 95]. SILC is caused by trap-assisted tunnelling through single traps. However, in some cases, a localized configuration of two traps can appear making easy the carriers tunnelling from cathode to anode. If it happens, a larger current density, compared to normal SILC, is observed. This phenomenon is known as "anomalous" SILC and it is, among others, a critical reliability issue in flash memories [Kumagai 08]. Actually, in thin oxides layers, breakdown can be understood as an extreme case of anomalous SILC [Degraeve 02]. Figure 1.10 illustrates a scheme where it is possible to compare: a) direct tunnelling from cathode to anode without traps in the oxide; b) trap-assisted tunnelling through single traps created during an electrical stress, responsible for SILC; and finally c) two-trap percolation path, responsible for "anomalous" leakage current.

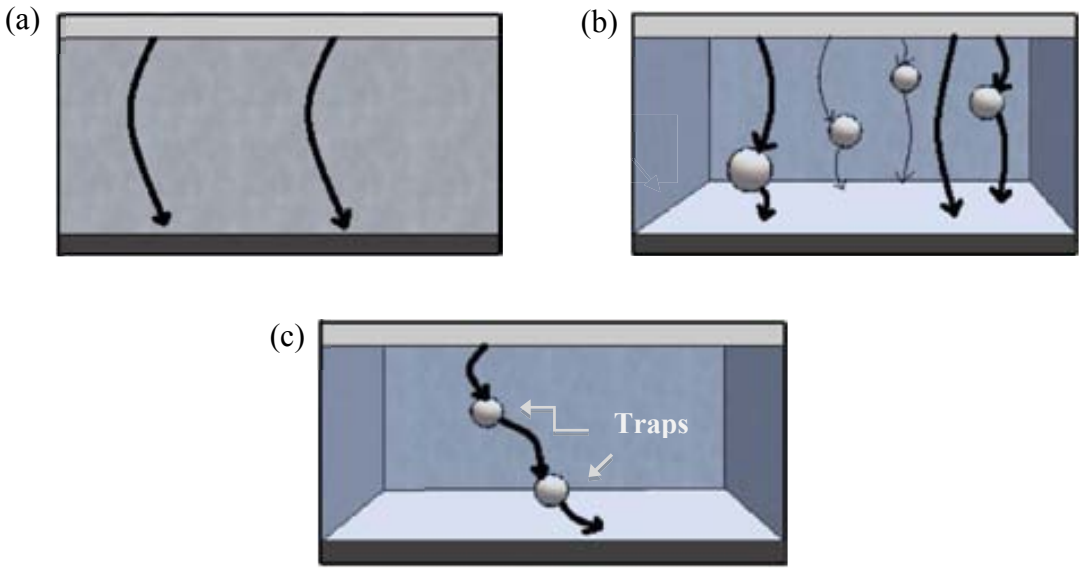

Figure 1.10: Schematic showing (a) direct tunneling from cathode to anode without traps in the oxide, (b) trap assisted tunneling through single traps created during an electrical stress, responsible for SILC, (c) two-trap percolation path, responsible for "anomalous" leakage current.

According to the percolative model, when the density of created defects reaches a critical value, a conductive path is formed between anode and cathode leading to a sudden increase of the gate current and, consequently, to BD [Suñe 90, Degraeve 96, Degraeve 98]. Furthermore, this model takes into account the extremely local nature (10-100nm^2) of dielectric breakdown since the post-BD current mainly flows through the percolative path instead of the whole dielectric. In figure 1.11, a schematic that shows the formation of the percolation path associated to dielectric BD is illustrated to facilitate its understanding. Figure 1.11(a) represents the random generation of traps during an electrical stress while figure 1.11(b) shows the formation of the percolative path, leading to BD.

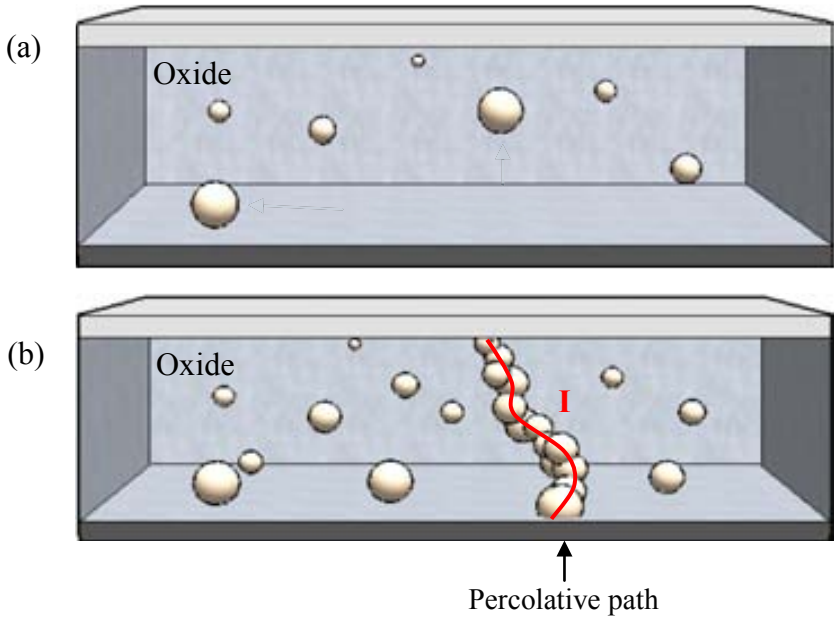

Figure 1.11: Formation of the percolative path, described from the percolation model, associated to dielectric BD. (a) Random generation of traps during an electrical stress. (b) Formation of the percolative path leading to a sudden and large increase of the gate current. When that happens, stack BD has been triggered.

Traditionally, for thick SiO_2 oxides (>10 nm), BD was observed as a sudden increase of the tunnelling current and it was associated to a complete loss of the dielectric properties (hard breakdown, HBD). However, with the oxide thickness reduction (< 5nm), besides HBD, two new breakdown modes less severe than HBD were identified: soft breakdown (SBD) [Miranda 00] and progressive breakdown (PBD) [Monsieur 02]. The analysis of these new failure modes and its impact on the device and circuit performance is specially important since it has been demonstrated that, depending on the breakdown hardness and the circuit functionality, the failure of a given device can or cannot lead to the failure of the corresponding circuit, especially on digital circuits [Avellan 04, Kaczer 00, Rodriguez 03, Kerber 06, A4 Ribes 08]. The main difference between the different modes is the time scale of the BD triggering and the post-BD current level. Post-breakdown current is the main difference between SBD and HBD. For the first case, the post-breakdown current is some orders of magnitude smaller than

for HBD. In the same way, the damage area observed is lower for the SBD than for the HBD as it was reported in [Alam 00, Miranda 01]. PBD is generally observed in oxides with a thickness lower than 2,5 nm. In this case, a progressive increase of current is observed before the BD is achieved [Monsieur 01]. PBD corresponds to the same phenomenon than SBD and HBD, in fact is considered their precursor, but at different time scales.

Figure 1.12a illustrates typical I-t curves measured when the different BD modes are observed during the application of a constant voltage stress. On the other hand, figure 1.12b illustrates typical post-BD I-V curves of the different failure modes (SILC, SBD and HBD) observed after applying ramped voltage stresses in a 2,5nm thick SiO_2 based stack. The I-V curve measured before any stress (labelled as FN, fresh) is also included as reference.

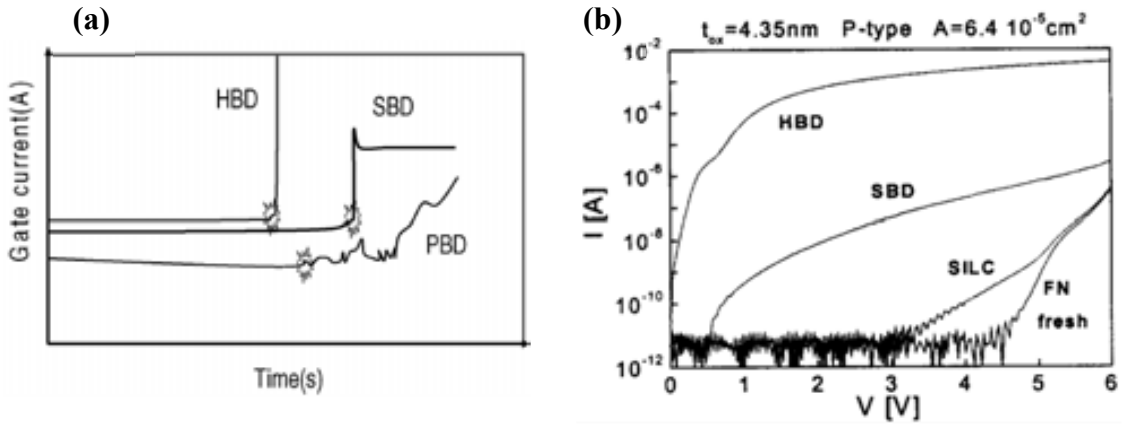

Figure 1.12: a) Different modes of breakdown: HBD, a sudden increase of the current is observed; SBD, an increase of the current, lower than HBD mode, is observed; PBD, a progressive increase of current is observed [Ribes 05]; b) Typical stages in the I-V characteristic of an ultrathin gate oxide as the degradation proceeds. FN refers to Fowler-Nordheim behavior of a fresh oxide; SILC to Stress Induced Leakage Current, SBD to Soft Breakdown and HBD to Hard Breakdown [Miranda 01]

With the advent of high-k dielectric films as a replacement of the SiO_2/SiON dielectric, new questions come up due to the presence of a dual dielectric layer that includes an high-k and interfacial SiO_2 layer. Among them, at which layer breakdown is initially triggered, if any?, has still not found an unified answer. Some authors claim that BD is initially triggered at the interfacial layer [Aguilera 06, Bersuker 08, Suñe 10, Ribes 10, Raghavan 12]. However, others authors point to the high-k layer [Okada 08, Nigam 09]. This concern is one of the topics analyzed in this thesis and will be studied in more detail in chapter IV.

1.3.2 Statistical distribution of BD

It is also important to remark that BD is a random event. Therefore, it should be described from a statistical point of view. In this sense, gate oxide breakdown is recognized as a statistical process which is normally characterized by Weibull distribution (1.5).

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right] \tag{1.5}$$

Where *F(t)* is the cumulative failure function, *t* is the random variable, β is the shape parameter (usually called Weibull slope) that indicates the data dispersion, and η is the scale factor (time for a 63% probability of BD occurrence). Equation (1.6), known as Gumbel plot, is easily deduced from equation (1.5):

$$\ln\left[-\ln\left(1 - F(t)\right)\right] = \beta \ln(t) - \beta \ln(\eta) \tag{1.6}$$

Equation (6) is usually used to represent the t_{BD} cumulative distribution for the dielectric breakdown analysis. Plotting ln[-ln(1-F(t))] vs. ln(t), a linear behavior is observed and β and η can be easily extracted since β is the slope of the plot and t = η when the line is crossing through origin. In figure 1.13, an example of Gumbel plot, where typical t_{BD} distributions of SiO_2 layers are represented for several oxide thicknesses, is shown [Wu 05].

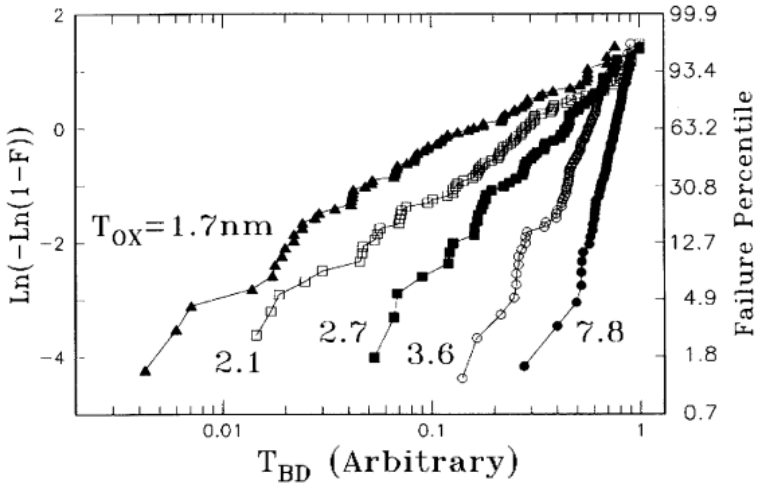

Figure 1.13: Typical normalized t_{BD} distributions for different oxide thicknesses [A75 Wu 05]

Trap generation rates (which clearly determine the formation of the percolative path, and therefore, the time to BD, t_{BD}) have been shown to be strongly dependent on the temperature [Moazzami 89, Chen 99], affecting consequently, to the Weibull parameters (β and η). Therefore, temperature dependence is also an important factor to be considered when t_{BD} reliability predictions have to be made. However, the temperature dependence of TDDB (Time Dependence Dielectric Breakdown) distributions remains an open issue. Although it is commonly assumed that temperature dependence follows the Arrhenius law (1.7) due to its simplicity, there is some evidence that non-Arrhenius behaviour may occur in ultra-thin oxides [Wu 05]. In this thesis, an Arrhenius relationship is assumed to analyze the temperature dependence of TDDB (see chapter IV).

$$t_{BD}(T) = A \cdot e^{\left(\frac{E_a}{RT}\right)} \tag{1.7}$$

Where A is a constant, E_a is the activation energy for the deffects to be generated, k_B is the Boltzmann constant, T is the temperature (in kelvin) and R is the gas constant.

1.3.3 Dielectric Breakdown and Resistive Switching

In section 1.3.1, dielectric breakdown was treated as an important reliability problem in microelectronics. However, it is worthy to mention that it may even be useful for some applications. Traditionally, this phenomenon was considered to be irreversible. Nevertheless, some authors have demonstrated that BD could be occasionally reversible in SiO_2 [Nafria 93, Suñe 93, Porti 02] if the current through the oxide is limited. Recent works have shown that, under current limited conditions, dielectric BD in ultrathin Hf based high-*k* gate dielectrics can also be a reversible phenomenon exhibiting two interchangeable conductivity states when the correct stress scheme is applied [Crespo-Yepes 09, Crespo-Yepes 10, Rodriguez 12]. On one hand, from the reliability point of view, the existence of two conductivity states indicates that the insulator properties of the dielectric can be at least partially recovered. On the other hand, this effect reveals similar characteristics with the resistive switching (RS) phenomenon observed in Metal-Insulator-Metal/Semiconductor (MIM/MIS) structures [Crespo-Yepes 09, Crespo-Yepes 11].

RS is known as the capability of some materials to switch between two conductivity states, denominated Low Resistive State (LRS) and High Resistive State (HRS). Although this phenomenon is known since a long time ago, in the early 1960s [Gibbons 64, Simmons 67], lately, it is becoming a prominent issue and it is being widely investigated since it is one of the best solutions to overcome the several technical limits of memory technology [Valov 11]. Among next generation of non-volatile memory (NVM), which uses RS as operating principle, random access memory (ReRAM) technology is standing out. This technology is one of the most promising emerging nonvolatile memories because of its simple structure, high switching speed, high scalability, low power and good compatibility with the standard CMOS process [Waser 07]. ReRAM is featured with reversible switching between two resistance states in metal oxide based materials normally implemented in MIM/MIS structures. [Waser 07, Sawa 08]. Normally, an initial “forming process” as a current-limited electric breakdown is needed to get the switch between both states. RS can be classified in terms of current-voltage (I-V) characteristics into two types: unipolar (nonpolar) and bipolar. It is called unipolar, or nonpolar, when the switching procedure does not depend on the polarity of the voltage and current signal. Otherwise, it is called bipolar when SET and RESET processes are operated using opposite voltage polarities. In order to show bipolar switching behavior, the structure of the system must have some asymmetry, such as different electrode materials or the voltage polarity during the initial electroforming step [Waser 07]. Figure 1.14 illustrates the I-V curves characteristics for unipolar and bipolar switching.

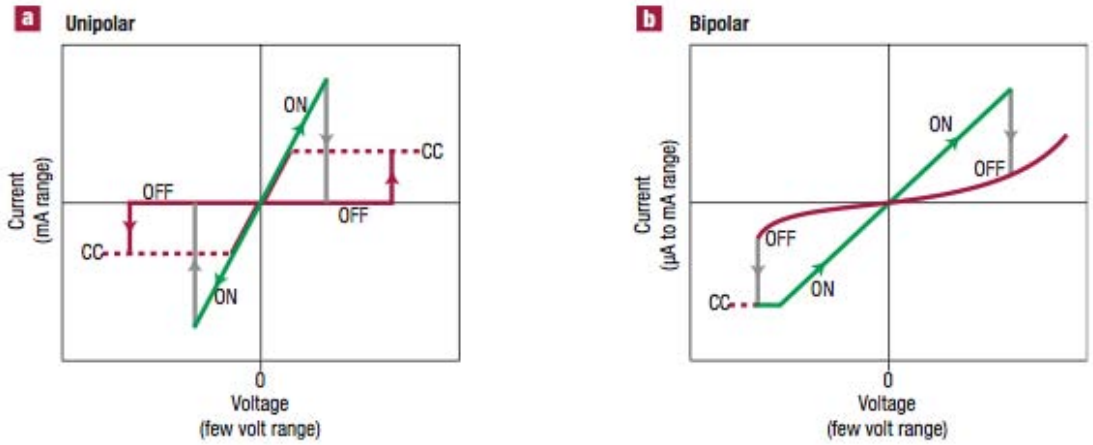

Figure 1.14: I-V characteristics for (a) unipolar and (b) bipolar switching. CC denotes the compliance current often needed to limit the ON current [94]

In addition, the physical mechanisms leading to the creation of the conductive path are also used to categorize the RS [Sawa 08, Waser 09]. Taking into account that the resistive state will be mainly determined by the electrical properties of the dielectric, the election of the convenient material is a challenge for the new generation of NVM based in MIM/MIS structures. HK materials also are being hardly investigated to be used into the ReRAM technology. However, there are still many open questions about the physics related to its working principle and many efforts are focused on the understanding about the switching mechanism. Recent studies have shown that the switching mechanism observed in some high-k dielectrics is based on a conductive filament (CF) through the insulator stack that can be created/destroyed depending on the applied voltage [Rozenberg 04]. However, other works suggest that the HRS should be related to the conduction of multiple filaments since I_{HRS} has been observed to scale with the device area [Xu 08]. Besides these reports about filamentary-type resistive switching, a so called homogeneous interface-type switching, which is observed at the interface between different complex oxides and the metal electrode, has been reported [Asanuma 09]. With the aim of clarifying the origin of the conductance, in chapter V, different CAFM analysis of the RS phenomenon in HfO_2 films are presented.

1.4 Standard characterization techniques

In order to study the degradation process and to evaluate the electrical properties and failure mechanisms of micro- and nanoelectronic devices, electrical tests are applied to test structures. This section is devoted to introduce the characterization techniques used to perform this analysis.

The expected lifetime of MOS devices under normal operating conditions could be of several years, therefore, the time required to deteriorate the gate oxide under these conditions is too large to be investigated in reasonable time scales. For this reason, it is necessary to have a methodology that allows to extrapolate the expected lifetime.

According to this, accelerated electrical test are commonly used to degrade the electrical properties of test structures and to study the reliability of gate oxides. The electrical tests normally used consist of the application of voltages or the injection of currents (called electrical stresses) through test structures (generally MOS capacitors or transistors [Pierret 90]) and the measurement of the evolution of their electrical properties. Next lines will briefly describe the most common tests used in dielectric yield and reliability assessment. A more exhaustive description can be found at [Martin 98].

Constant Voltage Stress (CVS) is one of the most common electrical tests. It consists of the application of a constant voltage to the stack and the measurement of the gate current evolution over time until the dielectric breakdown is triggered. In this test, BD is detected as an increase of the leakage current through the gate. This type of stress is used to analyze the TDDB by measuring t_{BD}, that is, the time-to-breakdown.

Constant Current Stress (CCS). In this case a constant current is injected until breakdown. The voltage evolution over time is monitored through a voltage versus time curve. Breakdown is detected when a sudden drop of voltage ocurs. This stress is used to measure the injected charge to BD and, in some cases, t_{BD}, as well.

Ramped Voltage Stress (RVS). A continuous increasing voltage is applied to the structure until BD. During this test, gate current is measured and plotted in current-voltage (I-V) characteristics. BD is detected as a sudden increase at the gate current. Figure 1.15 illustrates two typical I-V curves measured during two consecutive RVS to a capacitor with a 3.5nm thick SiO_2 layer [Lanza 10]. During the first voltage ramp, a sudden increase of current is observed at 0.5V, which is related to a HBD phenomenon. Afterwards, the gate dielectric loses its isolator properties showing very high post-BD currents, as it can be checked in the second I-Vcurve.

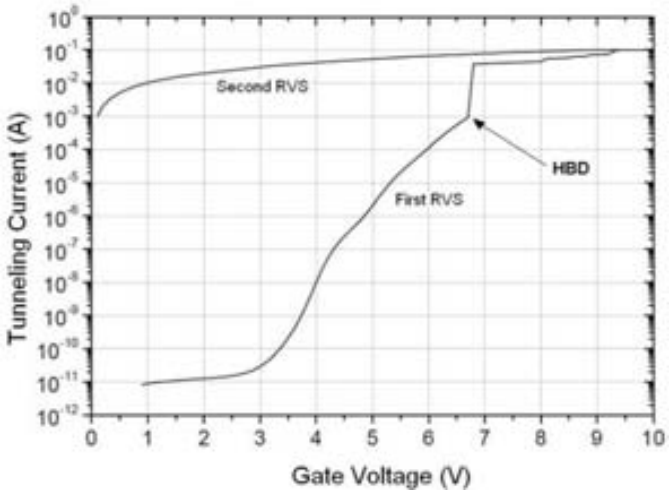

Figure 1.15: I-V curves obtained during the application of two consecutive RVS on 3.5 nm thick SiO_2 based capacitor [68].

The accelerated electrical tests mentioned above are usually applied to gate devices, that is, to MOS capacitors or transistors with a gate electrode, and are usually referred as

standard characterization techniques. These tests allow to measure the global electrical properties through the gate. Therefore, they provide spatially average information of the oxide electrical properties. However, information at the nanometric scale is not available. To get a nanoscale analysis and to achieve a better understanding of the electrical properties, alternative techniques with a nanoscale resolution are required. Next section is devoted to describe those techniques.

1.5 Tools with a nanometer resolution

In the case of ultra-reduced dimension transistors, inhomogeneities and microstructural defects must be taken into account because intrinsic parameter fluctuations associated to the discrete nature of matter and charge could have a strong impact on the global behaviour of the device. Local variations of electrical properties could have an important influence on the leakage current characteristics leading to a significant device-to-device variability. The main sources of variability are related to atomic level phenomena, the operating environment and the manufacturing process. Foremost among them are: *Random Dopant Distribution* (doping introduces a random distribution of discrete ions which create potential fluctuations affecting to the threshold voltage); *Line Edge Roughness* (roughness in the surface of gate transistor, due to intrinsic imperfections of the photolithographic process, can affect to the effective channel length); and, *surface roughness* (atomic-scale thickness variations which leads to fluctuations in the gate current and device threshold) [Asenov 08, Zhang 00, Aikaterini 12]. Furthermore, the homogeneity of the morphological and electrical properties of the high-*k* layer can also affect the variability of electrical properties of scaled devices [Bayerl 11]. Considering that these phenomena occur at the sub-micron scale, macroscopic analyses (standard characterization techniques) are not suitable, because local variations of the electrical properties and failure mechanism (which also happen at the nanoscale), as for example dielectric breakdown, cannot be measured. For this reason, measurement techniques with high lateral resolution (at the same scale as the material inhomogeneities) become indispensable for a better understanding.

On this matter, different microscopy techniques have been used to investigate the properties of different materials at a nanometer scale. The choice of the technique depends on the objectives pursued and the sample that wants to be analysed. *Scanning Electron Microscopy* (SEM), for example, is a very useful tool to analyse surfaces and to obtain information about the composition of the sample. [Goodhew 88]. *Transmission Electron Microscopy* (TEM) allows to obtain internal structural information (arrangement of atoms, defects, etc.) and compositional features of a sample using different imaging and diffraction techniques. Moreover, over the past few years, transmission electron microscopy has been revolutionized by the development of new techniques, among which *electron holography* allows to obtain magnetic and electrical information [Midgley 09, Midgley 01].

However, although both techniques are very powerful tools which have allowed to obtain useful information about different properties of the sample, SEM and TEM experiments need to be operated in vacuum chambers and require a laborious and complicated preparation of the surface under analysis. In this direction, since 1990s, a

new family of microscopes, called Scanning Probe Microscope (SPM), have been started to be used to investigate topographical and electrical properties of surfaces. SPM, are a family of microscopes that basically collect topographical images using an extremely sharp tip that scans the sample. SPMs allow to obtain a sub-nanometric lateral and vertical resolution as well as 3D quantitative information of the investigated surface. Scanning Tunneling Microscope (STM) [Binnig 86] and Atomic Force Microscope (AFM) are two outstanding scanning probe microscopes.

STM was developed in 1981 and their inventors, Gerd Binnig and Heinrich Rohrer (at IBM Zürich), received the Nobel Prize in Physics in 1986. The invention of the Scanning Tunnelling Microscope was a landmark in the birth of nanotechnology. It was the first instrument that generated atomic images of surfaces [Binnig 83]. STM is based on the concept of quantum tunnelling, being able to detect the tunnelling current that flows between a metallic tip and a conductive sample, separated just few nanometers, when a bias is applied between both. This current, which depends on the tip-sample distance, is used to evaluate the topographical properties of the surface. The exponential dependence of the current on the tip-sample distance implies that small changes in topography lead to large changes in current. Its high resolution (~ 1 Å) permits to image atoms within materials. In spite of this high resolution, STM shows some drawbacks. It is necessary to keep in mind that the measured topography (obtained form the measurement of the tunnelling current) does not only depend on the sample morphology but also on the electronic properties of different atoms of the surface, which can also lead to changes in the tunnelling current. Therefore, any change measured in the topography could be caused by changes in the electrical or morphological properties, being not possible to know exactly its origin. Moreover, STM can only measure conductive surfaces and requires ultrahigh vacuum environments. In order to overcome some of these limitations, the AFM was developed in 1986. AFM resolution is not as high as with a STM, but sample preparation is not required and a wide range of materials can be analyzed (not just conductive samples as for STM). The ability to operate on insulating surfaces is essential for the development and testing of nanoscale devices. Although specific environments are not required to work with AFM, they can be useful to improve some kind of measurement resolution [Lanza 10'].

There are several AFM based techniques especially focused on the simultaneously topographical and electrical characterization of materials used in semiconductor industry [Oliver 08, De Wolf 01, Kalinin 07]. Some of the most relevant are the Conductive Atomic Force Microscope (CAFM) [Murrell 93], Spreading Resistance Microscope Scanning (SSRM) [De Wolf 99, De Wolf 98], Kelvin Probe Force Microscope (KPFM) [Nonnenmacher 91] and Scanning Capacitance Microscope (SCM) [Martin 88, Dreyer 95)]. Conceptually, CAFM and SSRM are quite similar. In both cases a bias is applied to a conductive tip and the resulting tip-sample current is measured simultaneously to the topography. However, CAFM is usually used to measure the properties of the sample collecting the tunneling current through an oxide layer, whilst SSRM measures the spreading resistance, derived from the measured

electrical current, to determine primarily the distribution of dopant concentrations within semiconductors. Although all of them have been shown to be powerful tools for characterizing the electrical properties of dielectrics and semiconductors at the nanoscale, since the topic of this thesis is mainly focused in the CAFM, our attention will be aimed to this technique.

CAFM, also known under the term tunneling atomic-force microscopy (TUNA), has been developed in the mid 1990s in order to measure currents through thin silicon oxide gate dielectrics at the nanometer scale [O'Shea 95, Murrell 93, Welland 93, Ruskell 96, Olbrich 98, Kremmer 02]. Simultaneously to the topography, the current between tip and sample is also recorded when a bias is applied to the sample. The CAFM is usually used to simulate a MOS structure, which is the most common test structure in these fields. The tip (which is conductive) of the CAFM plays the role of the gate electrode (Figure 1.16). It means that a MOS capacitor with an area that corresponds to the contact area between the tip and the sample is defined. Taking into account that this area is of the order of 10-100nm^2, the properties of the oxide can be investigated at the nanoscale range.

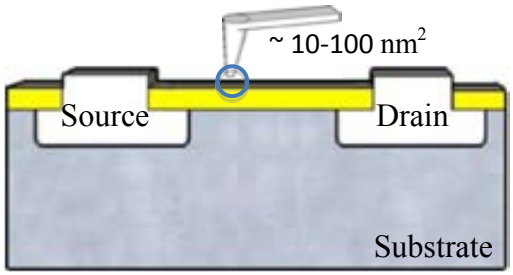

Figure 1.16: Illustration of an experimental configuration to characterize MOS structures at the nanoscale with CAFM. (~10-100 nm^2). When the tip of the CAFM contacts with the surface, a MOS structure of nanometric dimensions is simulated.

In contrast to the STM, the CAFM can measure electrical properties on insulating surfaces and, moreover, the measured current is not influenced by the surface morphology of the dielectric. This shows the CAFM as a superior tool to study the quality of dielectric thin films [Olbrich 98', Olbrich 99, Frammelsberger 06]. Since its inception, CAFM has demonstrated to be useful to characterize electrical properties of ultrathin SiO_2 films before, during and after degradation at a nanometer scale [Porti 01, Degraeve 01', Pakes 04, Wu 06, Fiorenza 06, Polspoel 07]. It has been used to measure the dielectric strength of SiO_2 gate oxides [Olbrich 98, Ruskell 96], local variations of the gate oxide thickness [Olbrich 98] and the electrical degradation and breakdown of ultra thin SiO_2 gate oxide layers subjected to electrical stress [X. Blasco 05] and irradiation [Wu 07]. The local character (~100 nm^2) of the BD event was experimentally demonstrated [Porti 02] for the first time with the CAFM. In the same way, this tool has been useful to observe that, in spite of the local character of the BD phenomenon, it can be propagated (depending on the BD hardness) laterally affecting neighbor areas

[Blasco 05', Wu 08]. This propagation, as well as the post-BD conduction, was observed to increase with the level of current injected during the stress [Porti 04]. That is, with the hardness of the BD event. On the other hand, statistical analyses performed at the nanoscale also confirms that t_{BD} follows a Weibull distribution [Sire 07, Fiorenza 07, Erlbacher 11], as it is observed at device level.

In the early 2000, the CAFM was used to investigate high-k materials [Landau 00]. However, it was not until a few years ago that its use was widespread to study high-k based gate stacks. The first works were published in 2004. There, the electrical homogeneity of HfO_2 and $HfAlO_x$ films on silicon was studied [Blasco 04, Petry 04]. Afterwards, a variety of single high-k dielectrics or high-k based stacks (based, for example, on Al_2O_3 [Lanza 09], Pr_2O_3 [Lo Nigro 03], ZrO_2 [Engel-Herbert 09], Ta_2O_5 [Atanassova 09], $SrTiO_3$ [Kraya 12]) were successfully analyzed confirming the CAFM technique as a powerful tool to study their electrical properties at nanoscale [Yanev 08]. For example, CAFM has been extensively used to study the electrical properties of as-grown (before an electrical stress) high-k dielectrics. Conduction by trap assisted tunneling (TAT) due to the higher density of native defects in high-k materials [McKenna 11, Aguilera 06, Lanza 11] or morphological and electrical changes due to its polycrystallization (as a consequence of an annealing treatment at temperature T_A during the fabrication process) are some examples of its applications. At this respect, this technique has been helpful to show the contribution of dominant TAT and FN current transport mechanism to the oxide leakage [Uppal 09, Lanza 11] as well as the impact of the T_A [Lanza 07, Lanza 11]. It has been shown that the electrical inhomogeneity of Hf-based high-k layers increase for annealing temperatures above the crystallization temperature [Blasco'' 05] as a consequence of the high-k layer polycrystallization [Bayerl 11', Lanza 07, Pawlak 10]. Other issues, as the conductions mechanisms through high-k stacks with SiO_2 as interfacial layer [Aguilera 07] or the effect of gate dopant diffusion on the leakage current of Poly-Si/HfO_2 stacks [Yu 07], also have been studied through CAFM. Moreover, this technique has allowed identifying different conduction regimes in as-grown HfO_2/SiO_2 stack, at different voltage ranges, which cannot be detected by standard electrical characterization techniques [Blasco 05].

Studies performed with CAFM about the degradation of the gate stack can be also found in the literature. Some of these works suggest that this degradation is due to the pre-existing electron traps in polycrystalline high-*k* gate stacks, which are the precursors of stress-induced defects [Paskaleva 08]. Recently, nanoscale electrical characterization has been performed to determine the cumulative failure distribution of TDDB [Wu 08, Erlbacher 11], which shows a bimodal shape for bilayer stacks [Delcroix 11].

Nowadays, the microscopic study of Resistive Random Access Memory (ReRAM) devices is being also a current issue [Polspoel 12, Muenstermann 10, Son 08, Jeong 12, Bersuker 11, Lanza 12]. A resistive switching phenomenon has become especially significant as an option for future memory devices. The study of the transport

characteristics of reduced oxide metal nanoparticle interfaces, as well as the influence of the contact size at the interface can be used to understand resistive switching mechanisms and the effects of ohmic and tunnel contacts to switching phenomena [Kraya 12]. The nanoscale current distribution and switching properties of thin film heterostructures, as well as the investigation of the scaling capabilities of MIM structures, which exhibit whether filamentary or interface-type switching, can also be addressed by using CAFM technique [Muenstermann 10].

In addition to the study of gate oxides, CAFM is used for other topics in microelectronics fields. An important application of CAFM, although this is not the topic of this thesis, is its use to modify surfaces and create structures on the nanometer scale by local oxidation [Kim 11, Xie 06, Kremmer 03] allowing even to fabricate nanoscale devices [Campbell 95, Held 97, Tachiki 02]. Also new emerging materials as graphene or carbon nanotubes are being studied using this technique [Ahmad 11, Noël 10]

Summarizing, AFM techniques and specially CAFM, have been shown to be powerful tools for researching the electrical properties and reliability of gate dielectrics (SiO_2 and high-k). In this thesis, the CAFM technique has been used to analyse the influence of the polycrystallization on the morphology, electrical properties and reliability of a HfO_2 based gate stack. The impact of an electrical stress is also evaluated. Finally, RS in MIM structures based on HfO_2 was also investigated.

CHAPTER II

Atomic Force Microscope and related techniques

This chapter is devoted to the Atomic Force Microscope (AFM) and related techniques, concretely the Conductive Atomic Force Microscope (CAFM) and the Kelvin Probe Force Microscope (KPFM), both used in this thesis. The work principles of AFM and its related techniques are introduced, as well as the modifications that must be applied to the conventional AFM to measure the electrical properties of surfaces. In addition, since the tips are a critical point to perform AFM measurements, a section is dedicated to discuss them in detail. Finally, a presentation of the different set-up used in this thesis is presented.

2.1 Atomic Force Microscope

The AFM is a measuring instrument that belongs to the SPM family which, as previously introduced in Chapter I, allows obtaining topographical images of a given surface when an extremely sharp tip scans the sample [Oliver 08]. Its work principle is based on the measurement of the interaction forces that appear between the tip and the sample when the distance between both is in the nanometric range. Since the tip is located at the end of a cantilever, any force applied to the tip causes a deflection of the cantilever, Δx, which is proportional to the force according to the Hooke's law, $F= -k\Delta x$ (where k is the spring constant of the cantilever). This deflection is detected by an optical system, which reflects a laser beam off the back of the cantilever. The reflected laser beam strikes a position-sensitive photodetector consisting of four side-by-side photodiodes that allows measuring the vertical and lateral deflections. The signal received by the four photodiodes indicates the position of the laser spot on the detector and consequently the deflection of the cantilever. This deflection can be registered during the scan of the sample, performed by a tube scanner (made from piezoelectric materials) as a 3D image that represents the surface of the sample. Figure 2.1 shows a schematic of an AFM with all their main components

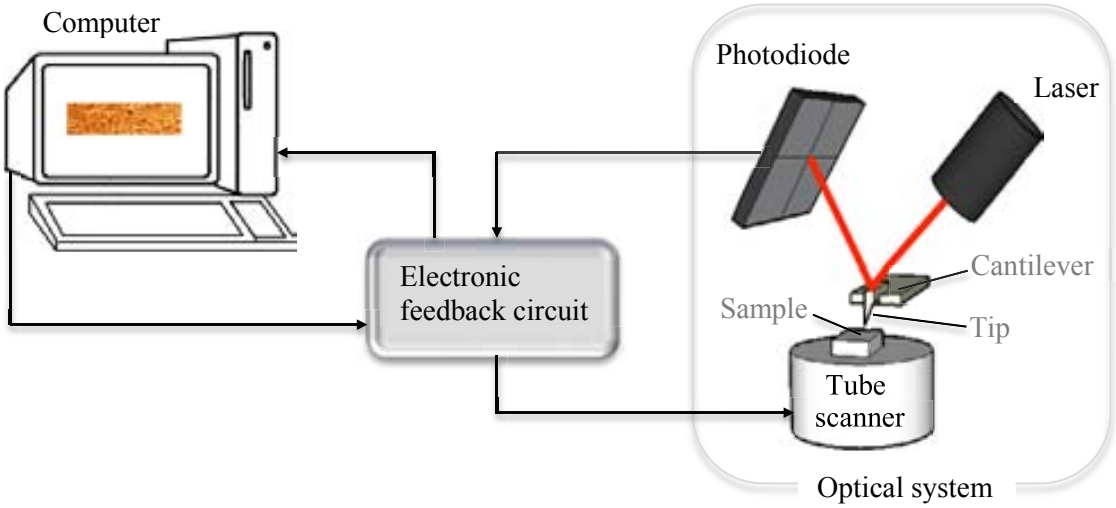

Figure 2.1: Schematics of an AFM. The optical system is used to detect the cantilever deflection when the tip contacts the surface. The optical system consists of a laser spot that is focused on the back of the cantilever. The reflected beam (which gives information about the cantilever bending) is detected by a photosensitive detector.

The AFM not only measures the force applied to the tip (and, therefore, the tip-sample distance) but also can regulate it through a feedback loop, which consists of the tube scanner, the cantilever, the optical system and a feedback circuit . The tube scanner, as already commented, is responsible for the movements of the tip on the X, Y or Z axis, so, it controls the position of the cantilever in the z-axis. The cantilever and the optical system measure the local distance between the tip and the sample. Finally, the feedback circuit will act depending on the user. If the user wants to maintain the tip-sample distance constant (the most common, to avoid to crash the tip to the sample), the feedback circuit will be turned on and it will attempt to keep the cantilever deflection

(and therefore, the tip-sample distance) constant by adjusting the voltage applied to the scanner during the scan. The constant deflection can be set by the user to control the force applied to the surface. On the other hand, when the feedback circuit is switched off, the Z-position of the tip is maintained constant and the cantilever deflection is recorded during the scan. AFM measurements are normally performed with the feedback loop on.

To perform AFM measurements, the sample is located on a holder-sample that, depending on the AFM model, can hold samples in the range of a few cm^2 or whole wafers. In addition, taking into account that an AFM works on the nanometric scale, a mechanical anti-vibration system is necessary to isolate the AFM from external vibrations.

2.2 Operation modes

Depending on the distance between tip and sample, and therefore, on the forces detected by the tip, two regimes of forces are mainly detected: short-range and long-range forces [García 00].

- *Short-range forces*: detected at distances of the order of 1-3Å. They are repulsive. These forces are due to the overlapping of the electron clouds, which is a quantic phenomenon related with the wave function symmetry without classic analogy, of the sample and cantilever's atoms.

- *Long-range forces*: detected approximately at distances larger than 5Å. They are mainly attractive. Examples of these forces are capillary, electrostatic, magnetic and Van der Waals forces.

Depending on the distance between tip and sample, two different operation modes can be described: *contact mode* (repulsive regime) and *non-contact mode* (attractive regime).

2.2.1 Contact mode

The atoms at the end of the tip are close enough to the sample surface (1-3Å) and interact with the superficial atoms of the sample in the repulsive regime [San Paulo 00]. One of the main drawbacks of this method is the tip wearing, due to the continuous "contact" with the surface during the scan [Bloo 99]. In addition, in ambient environments, capillary forces generated by a water layer present on surfaces (due to the humidity) pull the cantilever by surface tension towards the sample surface [San Paulo 00]. Capillary problems can be avoided by immersing the sample in liquids. However, not all samples can be immersed in liquids, as for example, in the micro- and nanoelectronics field (the present case).

2.2.2 Non-contact mode

In this mode, the tip is operating in the attractive regime, quite close to the sample, but without being in contact. Therefore, the tip-sample contact is minimized, avoiding to damage the surface and the tip. The forces between tip and sample are quite low, of the order of pN (10^{-12} N). Consequently, the vertical resolution obtained in non-contact mode is lower than that obtained in contact mode [Kitamura 95]. Such small forces are

generally detected by exciting the tip and making it oscillate. That allows to use AC detection methods to monitor these forces by measuring the change in amplitude, phase or frequency of the oscillating cantilever in response to the force gradient applied to the tip. In order to improve both modes, a new one was developed: tapping mode.

2.2.3 Tapping mode

Tapping mode [Zhong 93] is an intermediate method between contact and non-contact mode which overcomes the problems associated with friction and electrostatic forces related to contact mode and, on the other hand, offers a very high resolution. In this case, the cantilever is oscillating close to its resonance frequency and the tip intermittently contacts or "taps" the surface. During tapping mode operation, the cantilever oscillation amplitude is maintained constant by the feedback loop and the force on the sample is automatically set and maintained at the lowest possible level. Therefore, when, for example, the tip scans a protuberance on the surface, the tip-sample distance and the amplitude of the oscillation decreases while when the tip scans a depression, the amplitude increases since the tip-sample distance increases. In both cases, the AFM detector measures the oscillation amplitude of the tip and the feedback loop adjusts the tip-sample separation to maintain a constant amplitude and force.

Table I summarizes the main characteristics of the three operation modes. In addition, in figure 2.2, the force-distance curve between the tip and the sample and the regions where the different modes operate are shown.

Table I. Characteristics of the different AFM operation modes

OPERATION MODE	CONTACT MODE	NON-CONTACT MODE	TAPPING MODE
Contact with sample surface	Yes	No	Intermittently
Resolution	High	Medium	High
Tip-sample force	High	Low	Low
Tip wearing	High	Low	Low

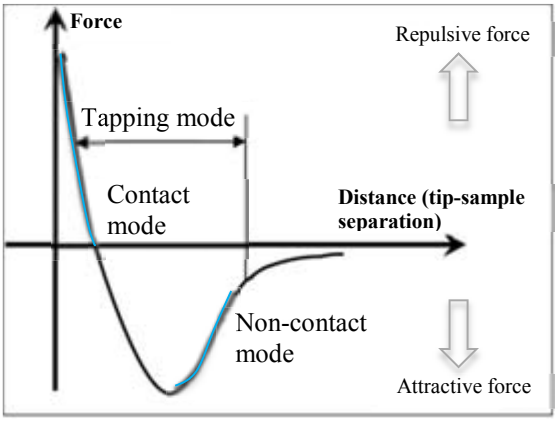

Figure 2.2: Interatomic force versus distance between AFM tip and sample and operation modes. Note that in contact and non-contact mode the AFM works in the repulsive and attractive force regime.

Since this thesis is focused on the electrical characterization and reliability of gate oxides, a good contact between tip and sample is necessary to perform conductivity measurements, as for example, when using the CAFM technique. Therefore, in CAFM experiments, contact mode is required. Nevertheless, when measuring with a Kelvin Probe Force Microscopy (KPFM), which gives information about the Contact Potential of the sample, this technique combines tapping mode and non-contact mode to be less aggressive. Further details about CAFM and KPFM (used in this thesis) are given in the following sections.

2.3 Conductive Atomic Force Microscope

The CAFM (Conductive AFM) is an AFM based technique that allows to perform simultaneously topography and electrical conductivity measurements, enabling to correlate spatial features on the sample with its conductivity. To carry out this kind of measurements, a conductive tip is absolutely necessary as well as a very low noise preamplifier, which works as an I-V converter that collects the current flowing through the tip. Figure 2.3 illustrates the CAFM experimental configuration, which is basically an AFM with the additional elements: a conductive tip, a preamplifier and a voltage source to bias the sample.

CAFM is normally used to obtain electrical information through the measurement of current maps in a given area (simultaneously with the topographical images) or I-V curves at fixed locations of the sample. Current maps allow to analyze the conductivity changes and homogeneity on a selected area. This test is performed by applying a constant voltage to the sample meanwhile the tip scans the analyzed area. On the other hand, I-V curves allow to analyze the different conduction mechanisms that can appear in different voltages range. In this case, this test is performed by applying a voltage ramp meanwhile the tips remains on a fixed position.

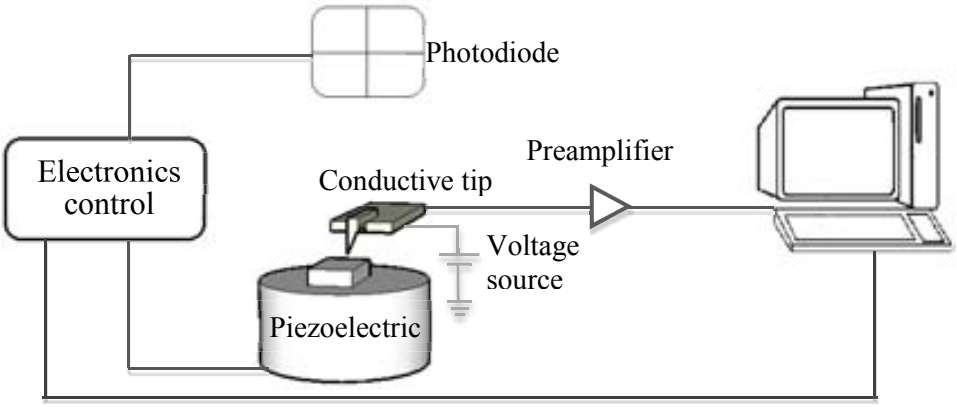

Figure 2.3: Atomic Force Microscope with the additional elements to configure a Conductive Atomic Force Microscope: conductive tip, preamplifier and voltage source to bias the sample.

Although CAFM is a very powerful tool, its current dynamic range (typically of three orders of magnitude, from 1pA to 1nA, limited by the characteristics of the pre-amplifier), cannot be enough to measure large current ranges as those involved as for example in HBD (Hard Dielectric Breakdown) events. Since the measurement of the complete I-V curve during a BD event is very important because it can provide information about the BD mechanisms, standard CAFMs have been improved to allow this kind of measurements. Blasco et al. [Blasco 05'''], for example, developed the Enhanced CAFM (ECAFM) to increase the current dynamic range of a CAFM. The main idea of this set-up is the substitution of the I-V converter by Source Measurement Units (SMU) connected to a Semiconductor Parameter Analyzer (SPA). Note that in this configuration, the position of the tip on the surface (size of the scan, speed of the tip, etc.) is controlled by the AFM, as well as the topographical information compilation, while the electrical tests and measurements of the electrical properties of the sample are controlled by the SPA. Despite the improvement of the electrical specifications of the ECAFM, the use of two different equipments (the AFM and the SPA) to, on the one hand, control the tip position and, on the other, measure the electrical variables, makes their synchronization difficult and the measurement of current maps slow, which is a handicap for obtaining reliable data due to the drifts of the piezos and the wear out of the tip. Another alternative to increase the current dynamic range of a CAFM is, for example, by means the use of a log amplifier [Aguilera 08], where the output is proportional to the natural log of the input current. However, in order to make accurate measurements with a log amplifier, it has to be carefully calibrated. This can be quite demanding and often hinders the use of a log amplifier by wide spread users. At this respect, Scientec has introduced a new commercial module (called Resiscope) which extends the current range from 100fA to 1 mA. The Resiscope is a system able to measure resistance over 10 decades with a high sensitivity and resolution when applying a V_{dc} bias between the sample and the conductive AFM probe. With this setup, it is possible to get I-V spectroscopy curves for each measured point as well as current maps. Current can be obtained, directly measuring the real current over the sample, or indirectly measuring the sample resistance. Last option is less aggressive to the sample [Scientec]. The Resiscope, as well as the ECAFM, have been used to perform some of the measurements presented in this thesis.

2.4 Kelvin Probe Force Microscope

Kelvin probe force microscopy (KPFM) is a non-contact AFM related technique developed by Nonnenmacher et al. [Nonnenmacher 91], which provides the capability to image the local surface potential of a sample with high spatial resolution. In particular, it allows to image surface electronic properties such as the contact potential difference (V_{CPD}) between the tip and the sample, which is related to the sample's work function and the presence of local charge on insulators (when gate dielectrics are, for example, analyzed). Therefore, KPFM provides complementary information to that obtained with a CAFM.

The local contact potential difference (V_{CPD}) between the tip and the sample is defined as:

$$V_{CPD} = \frac{\phi_{tip} - \phi_s}{-e} \qquad \text{Eq. 2.1}$$

where Φ_s and Φ_{tip} are the work functions of the sample and tip respectively, and e is the electronic charge. Figure 2.4 illustrates the V_{CPD} concept. Figure 2.4a shows two metals (tip and sample) in close proximity, but without electrical contact between them. Their vacuum levels (E_V) are aligned but Fermi energy (E_F) levels are different. The energy difference between the Fermi and vacuum levels correspond to the respective work functions Φ_s and Φ_{tip}. When tip and sample are in electrical contact, electrons flow from the metal with the smaller work function (higher Fermi level) to the metal with the larger work function (lower Fermi level). This creates an electric potential between the two metals, V_{CPD}, figure 2.4b. The electron transfer process continues until both Fermi levels are equalled. Once the equilibrium is reached, an electrical force acts on the contact area, due to V_{CPD}. This force can be nullified by applying an external bias (V_{DC}) having the same magnitude as the V_{CPD} with opposite direction Figure 2.4(c). Note that the amount of applied external bias (V_{DC}) that nullifies the electrical force due to the V_{CPD} is equal to the work function difference between the tip and sample. So, the goal of a KPFM is to measure such difference.

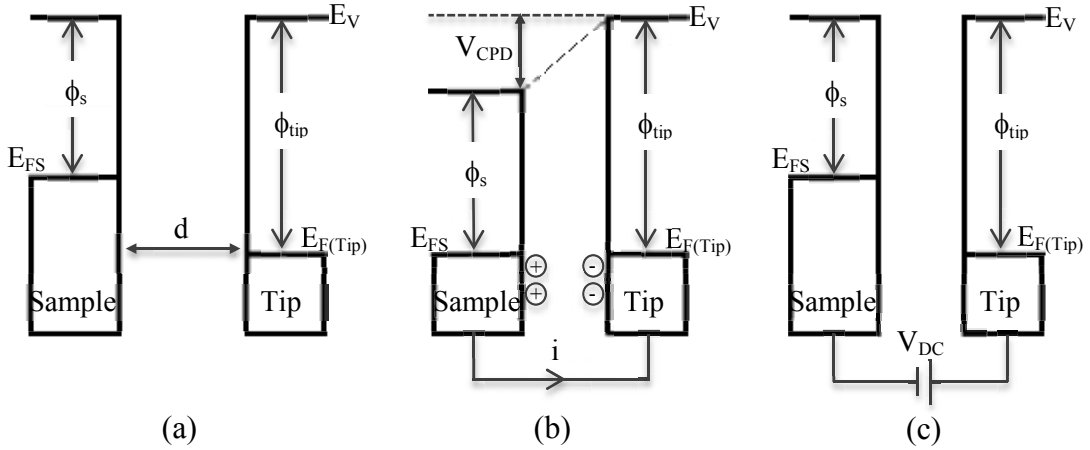

Figure 2.4: Electronic energy levels of the sample and AFM tip for three cases: when (a) tip and sample are separated by distance *d* without electrical contact, (b) tip and sample are in electrical contact, and (c) an external bias (V_{DC}) is applied between tip and sample to nullify the CPD and, therefore, the tip–sample electrical force. Ev is the vacuum energy level. E_{FS} and E_{FT} are Fermi energy levels of the sample and tip, respectively. Φ_s is the work function of the sample and Φ_{tip} is the work function of the tip.

Usually, KPFM measurements are performed scanning twice each line of the image. During the first scan, the topography of the sample is measured in contact or tapping mode. In the interleave scan, the stored topography is reproduced with the tip at a certain constant distance of the sample to detect the CPD signal (Figure 2.5). During this second pass, a voltage containing a *DC* an *AC* component is applied to the tip (V_{tip}) (Eq. 2.2).

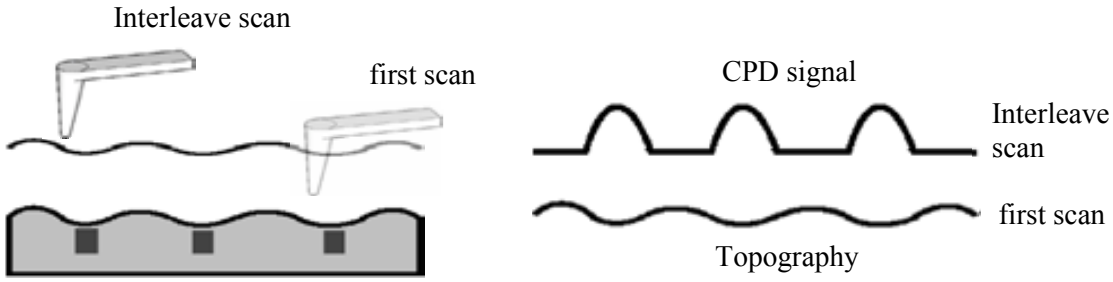

Figure 2.5 Schematics of KPFM procedure. During the first scan the topography is measured and "memorized". During the interleave scan the "memorized topography" is reproduced and the CPD is measured.

$$V_{tip} = V_{dc} + V_{ac} \cdot \sin(\omega t) \qquad \text{Eq. 2.2}$$

where ω is the resonant frequency of the cantilever. Assuming that the tip-sample system (figure 2.4) is equivalent to a nano-capacitor, the electrostatic energy stored at this capacitor is:

$$U = \frac{1}{2} C \Delta V^2 \qquad \text{Eq. 2.3}$$

So, the electrostatic force will be:

$$F_{elec}(Z) = \frac{dU}{dZ} = \frac{1}{2}\frac{\partial C}{\partial Z}(\Delta V)^2 \qquad \text{Eq. 2.4}$$

Taking into account Eq. 2.2:

$$F_{elec}(Z) = \frac{1}{2}\frac{\partial C}{\partial Z}[V_{CPD} - V_{dc} - V_{ac}\sin(\omega t)]^2 \qquad \text{Eq. 2.5}$$

This equation can be separated into three contributions: one due to the continuous component (Eq. 2.6) and two due to the frequentials components ω and 2ω (Eq. 2.7 and Eq. 2.8 respectively):

$$F_{dc}(Z) = \frac{1}{2}\frac{\partial C}{\partial Z}(V_{CPD} - V_{dc})^2 + \frac{1}{2}V_{ac}^2 \qquad \text{Eq. 2.6}$$

$$F_{\omega}(Z) = -\frac{\partial C}{\partial Z}\left[\left(V_{CPD} - V_{dc}\right)\cdot V_{ac}\sin(\omega t)\right] \qquad \text{Eq. 2.7}$$

$$F_{2\omega} = -\frac{1}{4}\frac{\partial C}{\partial Z}V_{ac}^{2}\cos(2\omega t) \qquad \text{Eq. 2.8}$$

From them all, only the component at ω (resonance frequency, eq. 2.7) makes the tip oscillate. The component with frequency 2ω is far away from the resonance frequency, ω, so, the oscillation induced due to this component is negligible. Therefore, when during the second scan the tip is oscillating at ω, V_{CPD} is obtained by nullifying these oscillations. To do that, the feedback of the KPFM changes $V_{dc,}$ until the ω component of the cantilever oscillation vanishes and, therefore, $F_{\omega}(Z) = 0$. Looking at the equation this happens when $V_{dc} = V_{CPD}$. So mapping $V_{dc}(x)$ gives information on the CPD between the tip and sample along the scan.

Since in a MOS capacitor, the CPD depends not only on the materials of the structure but also on the presence of charge in the dielectric, this technique can provide information about the charge trapped in the gate stack, which can be considered to be proportional to the density of defects [Bayerl 11]. For this reason, this technique will be also used in this thesis. That is, to analyze the presence of charge in gate dielectrics. More exhaustive description about KPFM can be found at [Melitza 11].

2.5 AFM Probes

One of the critical points to obtain accurate data when working with AFM are the tips, since the microscope resolution depends on its geometrical and mechanical characteristics. As previously commented, the tip is located at the end of a cantilever. Both, tip and cantilever, can show different shapes, dimensions or composition, depending on the final use as operation mode, environmental conditions and analyzed sample. Figure 2.6 illustrates SEM images of different kind of tips (Figure 2.6a) and cantilevers (Figure 2.6b). Figure 2.7 illustrates a schematics chip where the cantilever is mounted and approximate dimensions for standard Silicon AFM probes.

(a) (b)

Figure 2.6: a) Different kind of AFM probes [Nanoworld]. b) Different shapes of AFM cantilevers [Cantilevers]

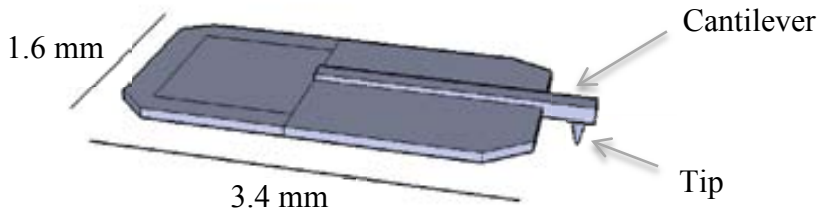

Figure 2.7: Typical schematics chip where the cantilever is mounted. Approximate values for standard Silicon AFM probes are also given.

Ideally, AFM tips are modeled as a cone with a semi-sphere at its apex (Figure 2.8) [Sadewasser 11]. Hence, geometrically, the curvature radius and the half-cone angle define the tip characteristics. The curvature radius, R, is defined as the radius of the semi-sphere located at the apex. The curvature radius determines the limit to detect structures with lateral dimensions in the order of the tip diameter (Figure 2.9) and, therefore, it defines its resolution. On the other hand, the half-cone angle, θ, indicates the ability to image steep side-walls (Figure 2.10). Therefore, the quality of an AFM image strongly depends on the shape and size of the tip, since it is a convolution between the real topography and the tip geometry. To get high resolution images, small curvature radius and small half-cone angles are required. The use of complex algorithms allows to correct this convolution providing an accurate information of the surface [Jóźwiak 12].

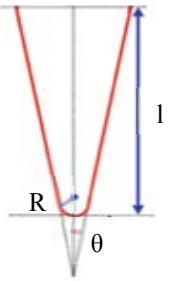

Figure 2.8: Geometrical cross-section of a tip, with a finite length *l*, half-cone angle θ_0, and spherical apex radius *R*

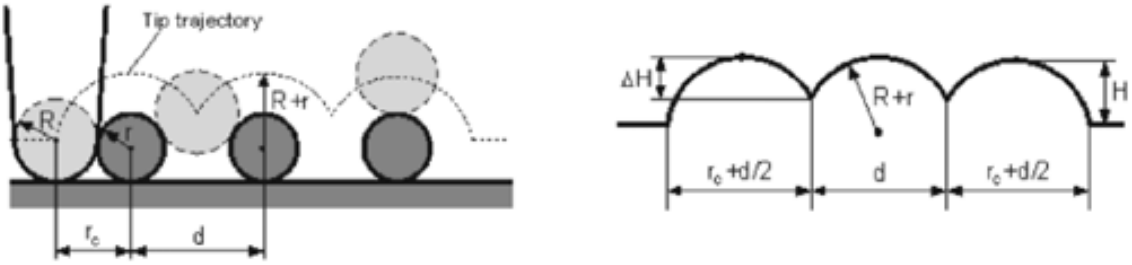

Figure 2.9: Influence of the curvature radius to detect structures. (Left) Schematics of tip apex geometry and studied structures in case $R \approx r$. Smaller tip radius leads to a better AFM resolution.(Right) Image profile of the studied structures. (Image extracted from www.ntmdt.com)

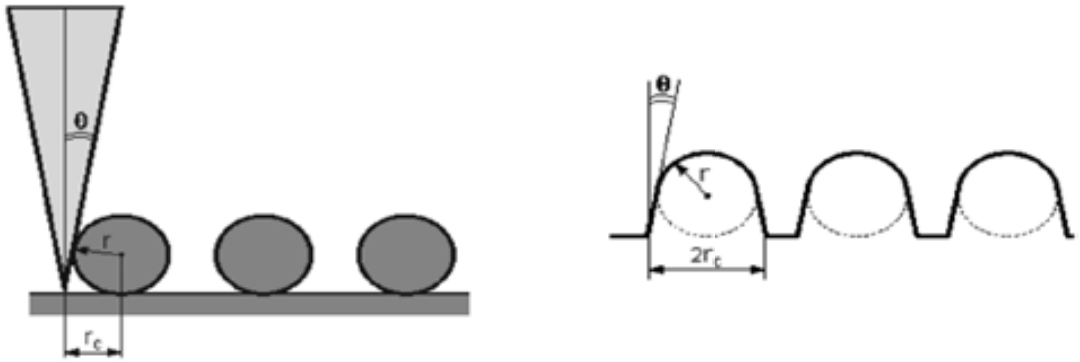

Figure 2.10: Influence of the half-cone angle to image steep side-walls. (Left) Schematics of conical tip geometry and studied structures. Smaller θ leads to a better definition of top side walls. (Right) Image profile of the studied structures. (Image extracted from www.ntmdt.com)

The properties of the tips are also determined by the fabrication process and the used materials. Tips can be entirely fabricated with the material required for a specific application, or with conventional tips (usually Si or N_4Si_3 tips) recovered with different materials as metallic alloy or diamond. The second option is normally preferable since is easier and cheaper than the first one. However, there is not a perfect tip for every measurement. The election of the tip becomes a tradeoff depending on the finality of the experiment. Usually, it is a tradeoff between lateral resolution and coated tip wear. Initially, CAFM probes were fabricated with doped silicon (with a tips radius of less than 10 nm), but the tip wearing and anodic oxidation, when working in air, led to wrong results [O'Shea 95', Murrell 93]. Trying to strengthen the tips, coated tips were fabricated using different materials such as titanium, platinum, cobalt, chromium or diamond and many combinations among them. This coating implies an increase in the tip radius (figure 2.11). Moreover, for most of the metallic coatings, it has been demonstrated that the wearing can be relatively fast due to the electrical as well as the mechanical stress. Figure 2.12, extracted from [Lantz 98], shows a Pt/Ir coated silicon tip after a CAFM experiment. Figure 2.13 shows an example of what happens when a surface is scanned with a new and worn out coated tip during CAFM experiments. Current image of figure 2.13(a) was obtained with a new Co/Cr coated Si tip while in figure 2.13(b) an old Co/Cr coated tip was used. Conductive rings (darker areas implies larger currents) are observed when the wearing of the tip is too high (figure 2.13b) leading to wrong information and an impoverishment of the resolution of the measure [Lanza 10].

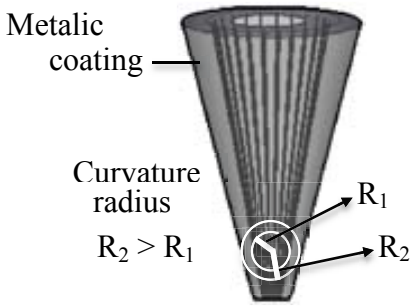

Figure 2.11 Tip radius increase due to the coating

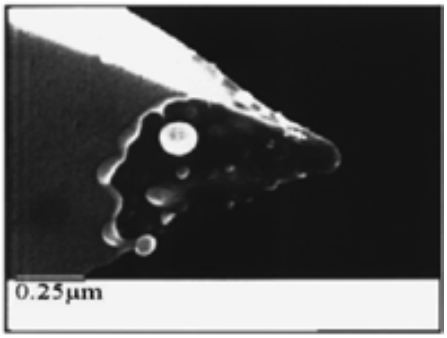

Figure 2.12 STEM backscatter image of a Pt/Ir coaten silicon tip in which the coating appears to have melted. The underlying silicon appears dark and the Pt/Ir appears light in the image.

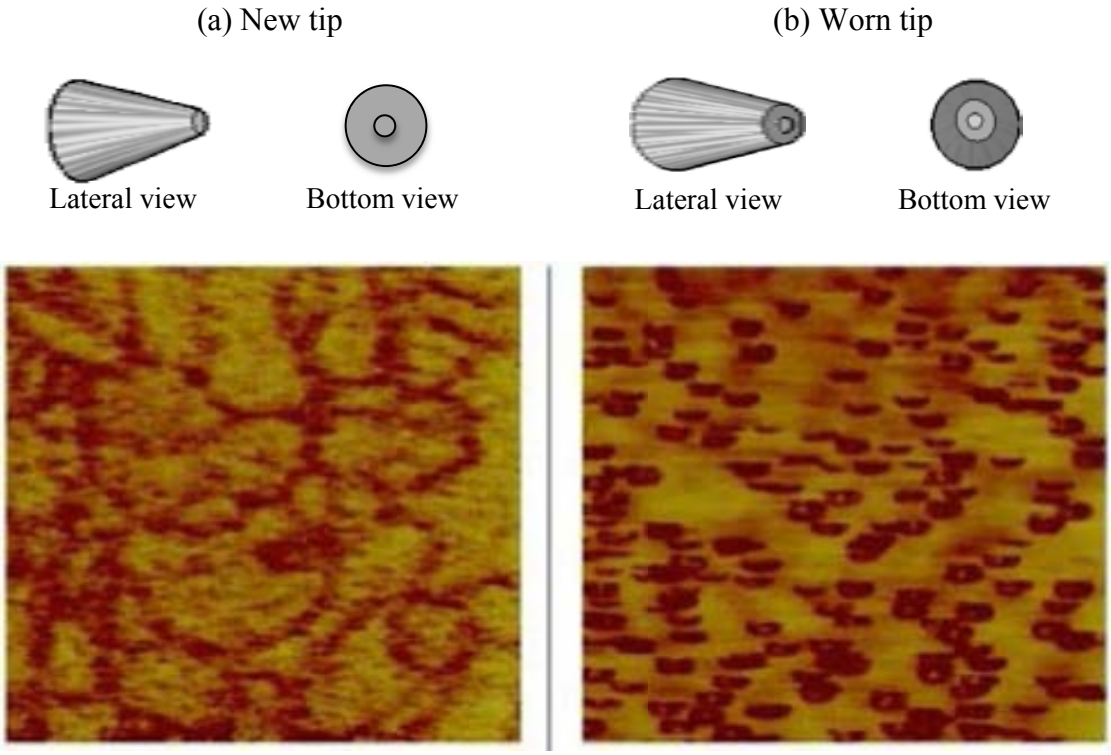

Figure 2.13: Current maps obtained with a new, (a), and a used, (b) Co-Cr coated tip. In (b) the lateral resolution is worse due to the tip wearing. Moreover, no-conductive areas surrounded by conductive regions can be measured, related to the wear out of the coating of the tip apex. [Lanza 10]

On the other hand, silicon tips coated with a high boron doped diamond layer have shown a very large resistance even after a lot of scans. In contrast, their lateral resolution is lower as a consequence of the tip radius increase [Lantz 98, O'Shea 95']. Super sharp doped diamond coated tips are also available, but the price is much more expensive than metallic coated ones.

Usually, one should take into account that the tips that offer higher mechanical resistance have large radius in front the tips that show a relative fast wearing. In

addition, operation mode, environment and sample must be also taken into account to choose the most suitable tip for a given application. A comparison among different tips, environments and operation modes will be shown in chapter III when analysing the topographical and electrical properties of polycrystalline HfO_2 based gate dielectrics. The most suitable conditions will be determined to optimize the data obtained in such samples.

2.6 Setups used in this investigation

This thesis has been performed at different laboratories, therefore, different set-ups with different characteristics have been used. In this section, their main characteristics are presented.

I. Agilent 5100 AFM located at the laboratories of the Electronic Engineering department of the Universidad Autónoma de Barcelona (UAB). This setup allows to work in contact or tapping mode. Topography, CAFM and KPFM measurements can be performed in air and controlled atmospheres. In addition, an external temperature module that can operate at temperatures up to 240ºC and a RESISCOPE module (see section 2.3) were incorporated to the AFM system during the development of this thesis.

II. Omicron variable temperature (VT) UHV (Ultra High Vacuum) AFM located at the laboratories of the Materials Research and Technology Department at the Leibniz-Institut für innovative, IHP (Innovations for High Performance Microelectronics), in Frankfurt Oder (Germany). The main characteristic of this setup is the possibility to perform CAFM measurements in UHV (10^{-10} mbar).

III. Digital Instruments 3100 AFM located at the University of Applied Sciences of Deggendorf (Germany). This setup allows to perform topography, CAFM and KPFM measurements in air.

IV. Bruker Dimension ICON AFM located at the laboratories of the Fraunhofer Institute for Integrated Systems and Device Technology in Erlangen-Nuremberg (Germany). This system is equipped with a NanoScope V controller (closed-loop system), and an extended module to perform CAFM measurements. Measurements at different temperatures are also available.

CHAPTER III

Impact of the tips characteristics and environmental conditions on CAFM resolution

In chapter I, high-k materials were introduced as the replacement dielectrics for the SiO_2/SiON of MOS structures. As it was appointed, an increase of the electrical properties inhomogeneity associated, for example, to its polycrystallization, and new reliability concerns, due to, for example, a still unclear mechanism of stress-induced degradation and breakdown, is observed. Therefore, these materials must be still deeply studied to achieve a better understanding about them. However, note that polycrystallization and failure mechanisms (as dielectric breakdown) are phenomena that take place at the nanoscale. Therefore, to get better insight into high-k materials electrical properties, it is necessary to measure the electrical characteristics of such dielectrics at the nanoscale. In this respect, the CAFM has demonstrated to be a very promising technique. However, sometimes, the lateral resolution of the technique might not be sufficient when working in ambient conditions and a different environment could be required to improve it. In this chapter, the influence of the environment on the AFM resolution as well as the influence of the used tips is investigated. Previously, an introduction to the sample characteristics that is going to be studied and the etching used to remove the top layer (which protect the high-k layer) before the CAFM analysis is presented.

3.1 Sample description

The gate dielectric stack analyzed in chapter III and IV consists of a 5 nm thick atomic layer deposited (ALD) HfO_2 film and a 1 nm interficial (IL) SiO_2 layer grown on a Si epitaxial p-substrate. The gate stack was annealed at 1000°C for 60 sec in N_2 ambient to simulate the thermal budget of the gate-first transistor fabrication process that results in the polycrystallization (compared to as-deposited) of the high-k film. The nominal oxide thickness, 5nm, was chosen in order to get a HfO_2 monolayer with nanocrystals as big as possible, as can be shown in the schematics of figure 3.1(a), which improve the experiments resolution. Thicker films would lead to the formation of several layers of grains. A HfO_2 multilayer would make more difficult the analysis of single crystals, figure 3.1(b). On the other hand, thinner layers could lead to the formation of smaller grains, beyond the resolution of the CAFM, making more difficult the analysis of nanocrystals and grain boundaries (GB), figure 3.1(c).

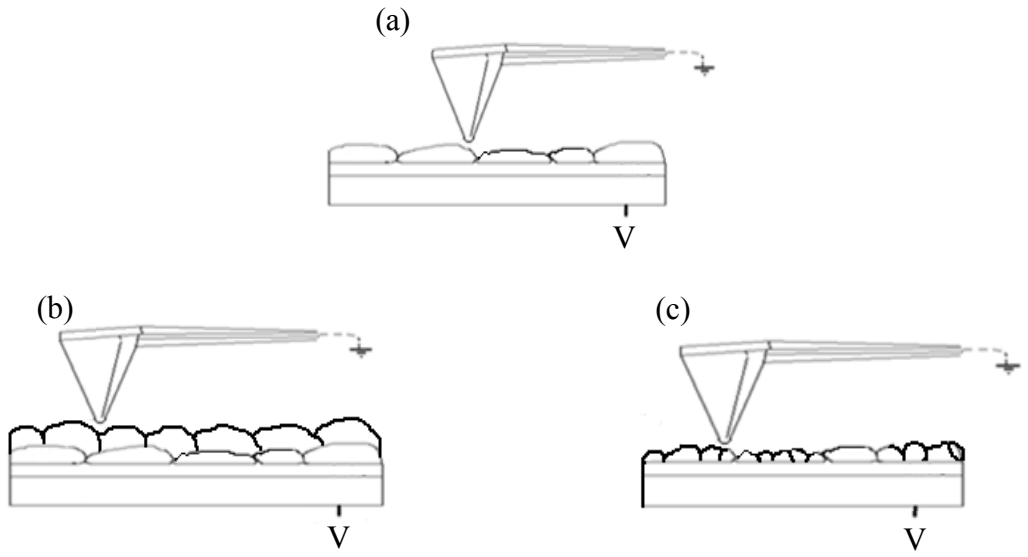

Figure 3.1: Different polycrystalline high-k layer structures depending on the thickness of the high-k layer. (a) Monolayer with nanocrystals as big as possible that facilitates the study of individual grains. (b) Multilayer of nanocrystals which difficults the analysis of single grains. (c) When the thickness of the layers is too thin, smaller grains could hinder the distinction between grains and grain boundaries.

Since the sample has not been fabricated in our laboratory, a protective layer of amorphous Si (100 nm) was grown on top to avoid any contamination of the HfO_2 layer from its manufacture up to the AFM measurements. This protective layer must be eliminated before any AFM analysis. Next section describes the different tests performed to optimize the etching process and to verify that the Si removal does not affect the properties of the HfO_2 layer.

3.2 Etching of the top layer.

To perform AFM measurements with the highest resolution, the tip must be in contact with the surface that wants to be analyzed, that is, in our case, the HfO_2 layer. The amorphous Si protective layer, therefore, is an obstacle between the tip and the HfO_2 film, being a basic requirement its removal. The characteristics of the etching mainly depend on the material that has to be eliminated as well as the material that is in contact with it and wants to be analysed. The etching must be highly selective in order to eliminate the layer that must be removed without affecting the layer of interest (in this case the HfO_2) that is, without changing its structural and electrical properties significantly. For this reason, it is very important to look for the appropriated etching of every material. In this case, a chemical etching provided by Sematech which consists of a NH_4OH:H_2O deionized (DI)/1:10 solution at 60ºC during 13'19'' (calculated from an estimated etching rate of 75Å/min and taking into account the thickness of the protective layer, 100nm), was initially used as orientation. From it, different tests, changing different parameters as etching time, temperature or concentrations, have been used to optimize the procedure. Table II shows the data of some attempts carried out. Numbers in the columns indicate the proportion of the different elements used in each case. Note that NH_3 was used instead NH_4OH since:

$$NH_3(aq) + H_2O(l) \longleftrightarrow NH_4^+(aq) + OH^-(aq)$$

In the same way, figure 3.2 illustrates AFM topographical images at different stages of the etching process: (a) corresponds to the sample with the Si protective layer (prior to the etching), (b), (c) and (d) after the Si removal using the etchings reflected in table I, and (e), a HfO_2 layer of a test structure in which the protective layer was not grown (taken as reference). From the images of figure 3.2, it is possible to appreciate a clear evolution in the etching process. In (b) and (c), for example, big residual islands are still present in the oxide, which can be related to the top layer material. However, image (d) is quite similar to the reference sample, (e). The comparison of the reference sample (e) with image (d) suggests that this procedure, although not ideal (sometimes some small islands seem to remain in the oxide), allows to reach the high-k dielectric without affecting the morphological properties.

Table II: concentration of the different components, time and temperature of several etchings used to remove the protective layer.

Image in figure 3.2	*H_2O (ml)*	*NH_3 (ml)*	*T (ºC)*	*Time*
b	4	2	~ 60	~ 13´20´´
c	1.5	5	~ 60	~ 14´
d	10	8	~ 70	~ 13´20´´

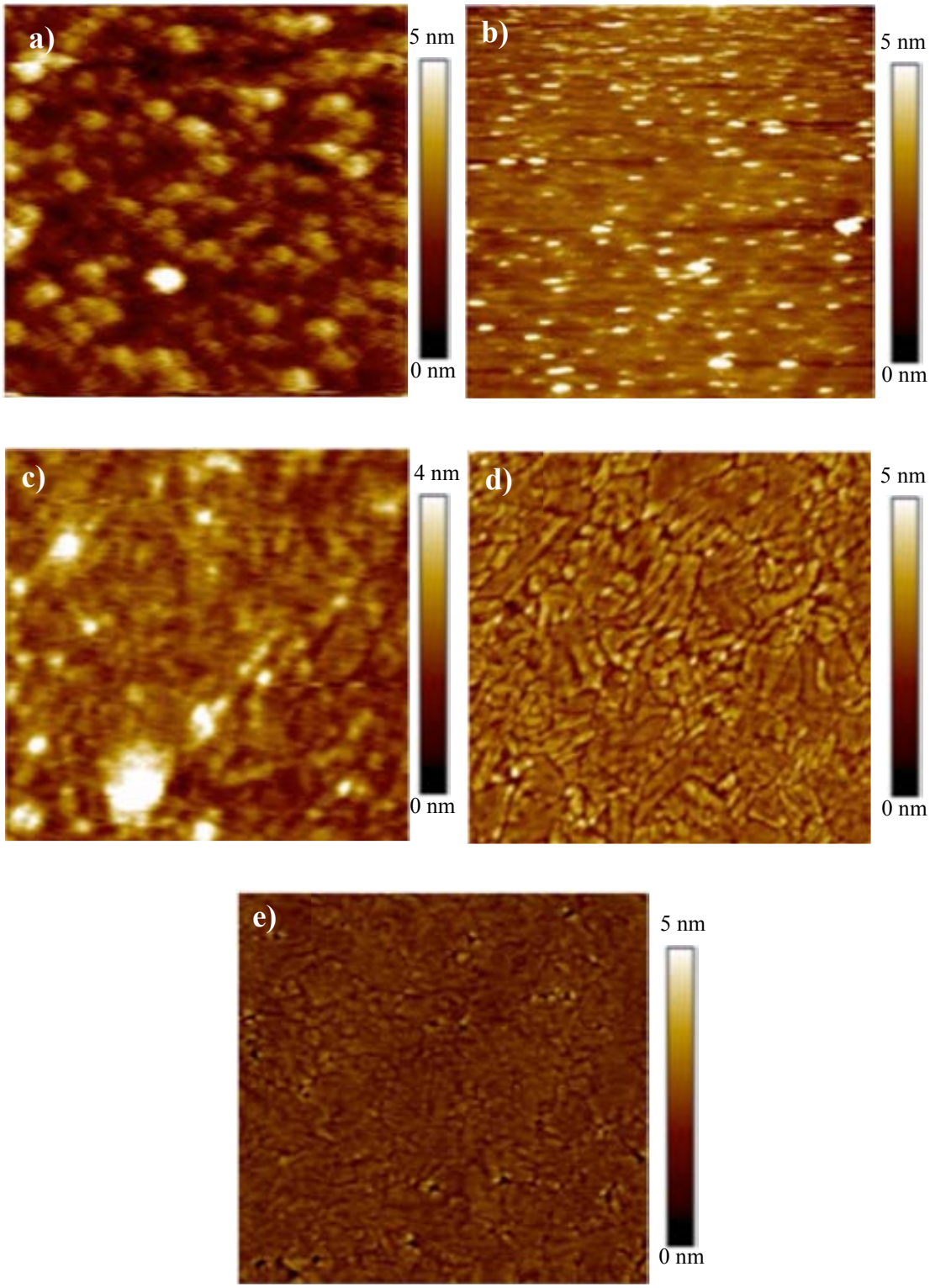

Figure 3.2 AFM topographical images obtained at different stages of the etching process on an area of 1μm^2. (a), before the etching and (b), (c) and (d) after different etching times compositions and temperatures (see table II). (e) is a reference image (provided by Sematech) where the protective layer was not grown.

To further verify if the Si layer has been removed and the high-k dielectric has not been affected by the etching, complementary tests have been performed in the Leibniz-Institut für innovative, IHP (Innovations for High Performance Microelectronics). For example, a XRR (X-Ray Reflectivity) analysis [Parrat 54], which is a non–destructive method to study the thickness and roughness of thin layers and multilayer systems, shows that the protective layer is not on the sample since amorphous Si is not detected on the experiment, figure 3.3. On the other hand, the values exhibit on the inset of figure 3.3 show that the HfO_2 and SiO_2 layers have a thickness of ~ 5 and ~1 nm, respectively, confirming that both layers are still present and that HfO_2 has not been damaged. The roughness value measured through this technique on the HfO_2 is ~0.46 nm (see the inset of figure 3.3), which is similar to the roughness obtained from figure 3.2(d) (~0.42nm), further supporting this hypothesis. However, in some samples, the use of the SAM (Scanning Auger Microscopy) technique [Castle 92], which allows to obtain SEM images (figure 3.4(a)) and AES (Auger Electron Spectroscopy) measurements (figure 3.4(b)), show the existence of some isolated amorphous-Si islands on the HfO_2 layer, in agreement with some of the AFM topographical images obtained after the etching. In figure 3.4(a), these islands are highlighted with a square. Their corresponding Auger electrons kinetic energy spectrum (that acts as a fingerprint of the elemental composition of the probed surface) is displayed in figure 3.4(b). Despite this, these islands shouldn't suppose any problem to perform the AFM analysis because these regions are easily detectable and ruled out from the topographical point of view (Figure 3.5).

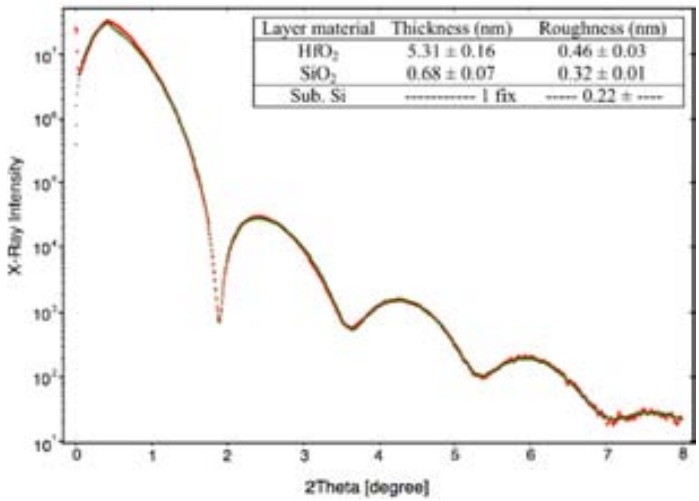

Figure 3.3: X-Ray Reflectivity analysis of the HfO_2 based gate stack after the etching ***d*** of table II. Experimental data (green colour) was fitted (red colour) with specific software. The thickness and roughness of the layers are exhibited in the inset. These results agree with the nominal thickness of the layers indicating that amorphous Si is not present in the sample and that the HfO_2 layer has not been damaged by the etching.

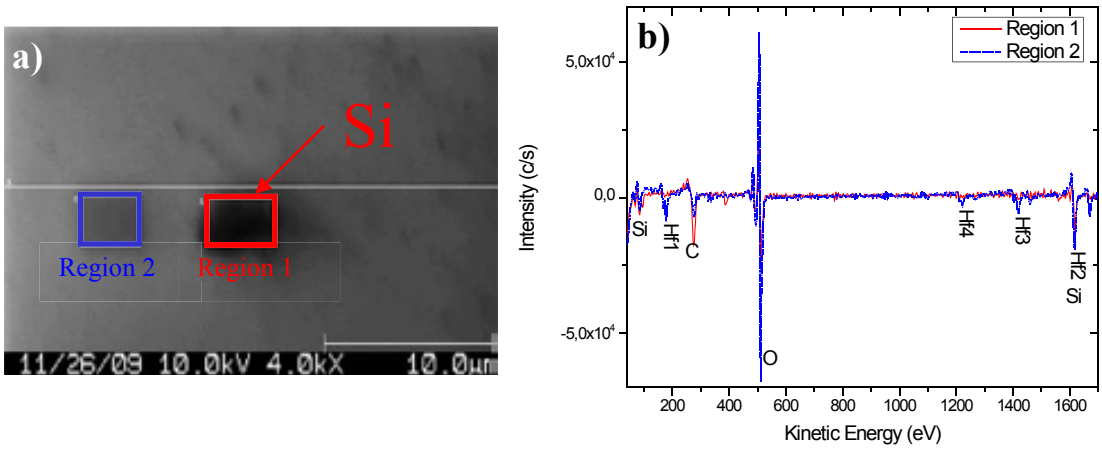

Figure. 3.4: SAM (Scanning Auger Microscopy) analysis. (a) SEM images showing Si islands. The squares marked in the SEM image, region 1 and region 2, indicate the areas where the AES (Auger Electron Espectroscopy) spectrum was performed (b)

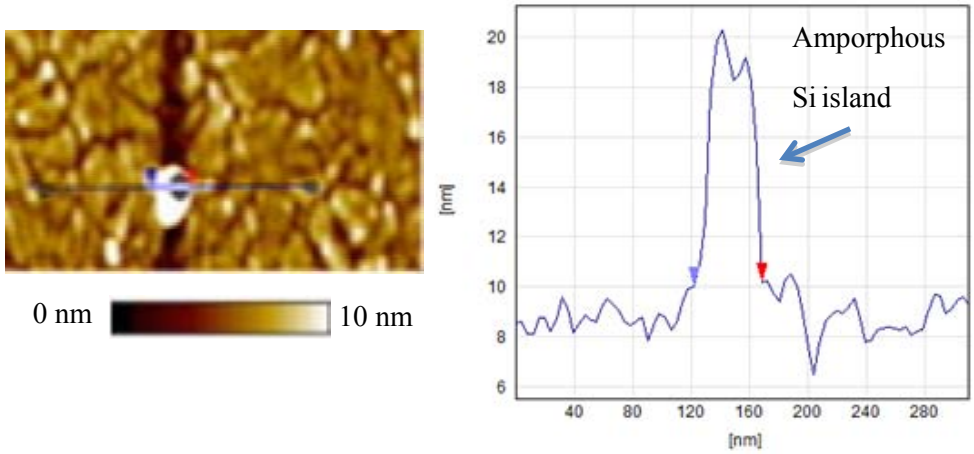

Figure 3.5: Si island detected in an AFM topographical image after etching

In addition, other measurements as XRD (X Ray Diffraction) [Snyder 99] were also performed to obtain further information about the composition of the sample. The diffraction pattern of the HfO_2 film is illustrated in figure 3.6. The different diffraction peaks observed in the figure can be related to the monoclinic phase of HfO_2 as it can be checked in [ICDD]. A peak related to either tetragonal or orthorhombic HfO_2, often appearing at $2\theta = 30.4^{\circ}$ in HfO_2 films deposited by atomic layer deposition and sputtering was no detected in this case. It could be as a consequence of the higher annealing temperature since with the increasing temperature annealing, the orthorhombic or tetragonal phase decreases and disappears [Terasawa 05]. Since relative intensity ratios between diffraction peaks are close to powder diffraction patterns in HfO_2, a preferred orientation in these films is not appreciated. That means that crystals with different orientations are present in the oxide, which is in concordance with the granular structure observed in the AFM images in figure 3.2.

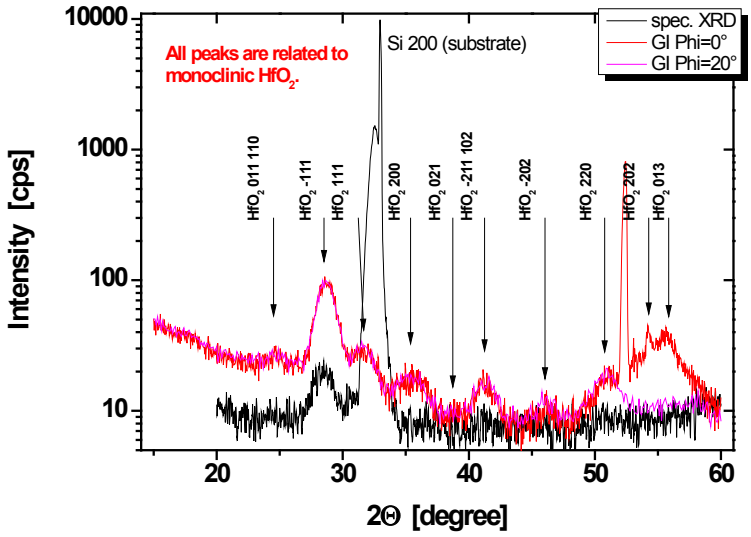

Fig. 3.6. XRD (θ-2θ scan) pattern of HfO_2 film deposited on SiO_2/Si substrate. A preferred orientation is no appreciated suggesting a polycrystalline structure of the HfO_2 layer.

To conclude this section, these tests have demonstrated the optimization of the etching process to remove the amorphous Si layer as well as the confirmation that the HfO_2 layer, which shows a polycrystalline structure, is not affected.

3.3 Optimization of the AFM resolution: Impact of the environment and tip characteristics

Once the protective layer has been satisfactorily removed, if a correlation of the topographical and electrical properties of the polycrystalline HfO_2 layer (if any) wants to be performed, the nanocrystals should be firstly identified in topographical images. However, the dimensions of smaller grains, and especially the grain boundaries' width, which may exceed the limits of AFM lateral resolution, could difficult this issue. Since AFM resolution strongly depends on the tip characteristics and the measurement environment [Lantz 98, Lanza 10], both issues were first analyzed. The goal was to find the optimal experimental conditions to perform the AFM analysis with the highest resolution to guarantee that single nanocrystals could be detected with the AFM.

First the effect of the tip characteristics on the topographical maps of the polycrystalline HfO_2 layer was analysed by comparing topographical images obtained with the AFM working in contact mode and air and using different tips (non-coated Si tips and Si tips coated with different materials). Figure 3.7 shows topographical images of the HfO_2 layer obtained in air with (a) a non-coated Si tip (radius ~10nm), (b) a Si tip coated with a Pt/Ir layer (radius ~25nm), (c) a Si tip coated with a Co/Cr layer (radius ~50nm) and (d) a doped Diamond coated Si tip (radius ~100nm) respectively.

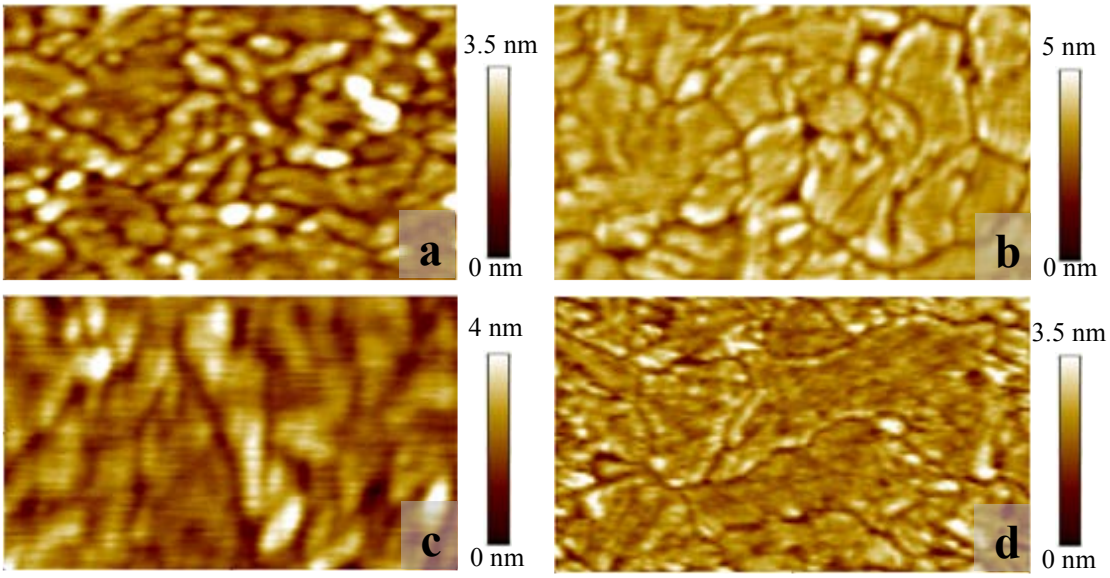

Figure 3.7: AFM topographical images obtained in an area of 300x500 nm^2 with (a) a non-coated Si tip (radius ~10nm), (b) a Si tip coated with a Pt/Ir layer (radius ~25nm), (c) a Si tip coated with a Co/Cr layer (radius ~50nm) and (d) a doped Diamond coated Si tip (radius ~100nm)

Note that a granular structure, related to the polycrystallization of the high-k layer, can be distinguished in all images. However, from the analysis of such images, it can be concluded that the tip radius clearly affects the AFM resolution. At first glance, the grains seem to be larger in those cases when the tip radius is bigger. That is, figure 3.7(c), for example, obtained with a tip with a radius of ~50 nm, shows larger grains than figure 3.7(b), obtained with a tip with a radius of ~25 nm and, in this case, grains are even larger than in figure 3.7(a), where the tip radius was ~10 nm. This qualitative observation is further supported by the statistical estimation of the average grain size and image roughness in each topographical map. Figure 3.8 shows the average grain size (circles) and image roughness (triangles) for each of the used tips (line is guide to the eye). A clear enhancement of the grain size can be observed when the tip radius increases. This increase could be due to unresolved grains, that is, less defined borders between grains maybe as a consequence of the larger radius. This hypothesis is also supported by the roughness values, which reveal a decrease of this value when the tip radius increases. The reduction of the roughness could be explained by considering that coated tips (i.e., tips with a larger radius) are not enough resolutive to reproduce drastic changes on the surface, leading, therefore, to smoother surfaces. That is, tips with a high radius are not able to completely penetrate into the GB (with a width of a few nanometers ~2nm [McKenna 09]); hence, the difference between GB and grain height seems to be less. Therefore, from these results one can conclude that, the larger the tip radius, the lower the image resolution. Surprisingly, with diamond coated tips, resolution is sometimes better despite having a larger radius. This is because diamond coated tips can have diamond crystallites tending to have sharp edges at their apex and, therefore, leading to a nanoscale roughness of the tip that can lead to higher resolution. However, it is important to emphasize that these results are not always reproducible.

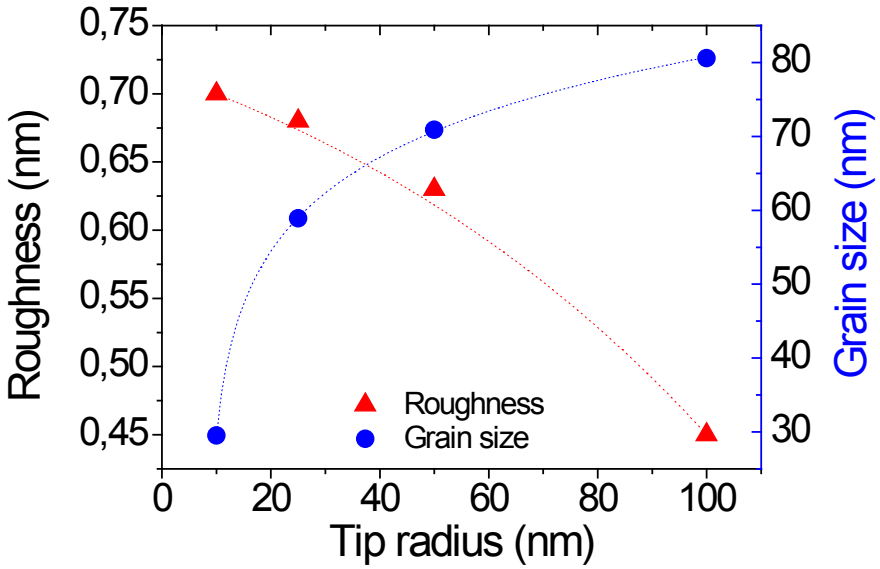

Figure 3.8: Influence of the tip radius in the grain size (circles) and roughness (triangles) measurements. Whit the tip radius increment an enhancement of the size grain, as well as a roughness decrease, is observed.

Although coated tips show lower resolution than non-coated ones (and, consequently, they are not a good choice to investigate single nanocrystals), it is important to emphasize that CAFM measurements must be performed with conductive tips, which are normally Si tips coated with a metal. Therefore, non-coated Si tips are usually ruled out. In addition, coated tips normally imply higher mechanical resistance, which depends on the coated material, leading to a higher lifetime of the tip. This is especially important in AFMs working in contact mode, (as the CAFM). For this reason, coated tips are normally used in CAFM experiments: although they have larger radius and, therefore, the resolution is not the best, they provide a good conductivity and mechanical resistance (especially, diamond coated tips). Therefore, since the goal of this section is to improve the CAFM resolution and tip radius cannot be reduced because coated tips are required, other experimental conditions should be considered as, for example, environmental conditions during the measurements. Note that when measuring in air, a water meniscus is usually present at the point of contact between the tip and the surface due to the ambient humidity [Lanza 10'', Polspoel 12], which can increase the contact area and, therefore, reduce the experiments resolution. On the other hand, UHV measurements could minimize the influence of this meniscus, improving the resolution. This will be the goal of the next experiment.

To analyze the impact of the environment on CAFM experiments, topographical and current measurements performed in air and in UHV (10^{-10} mbar) have been compared when using diamond coated tips. In addition, in the UHV experiments, the sample was previously heated indirectly (radiative) at 150 °C in order to free the film from hydrocarbon and water contamination. Figure 3.9 shows some examples of topographical (left) and current (right) images obtained in air (top) and UHV (bottom) with a doped diamond coated Si tip.

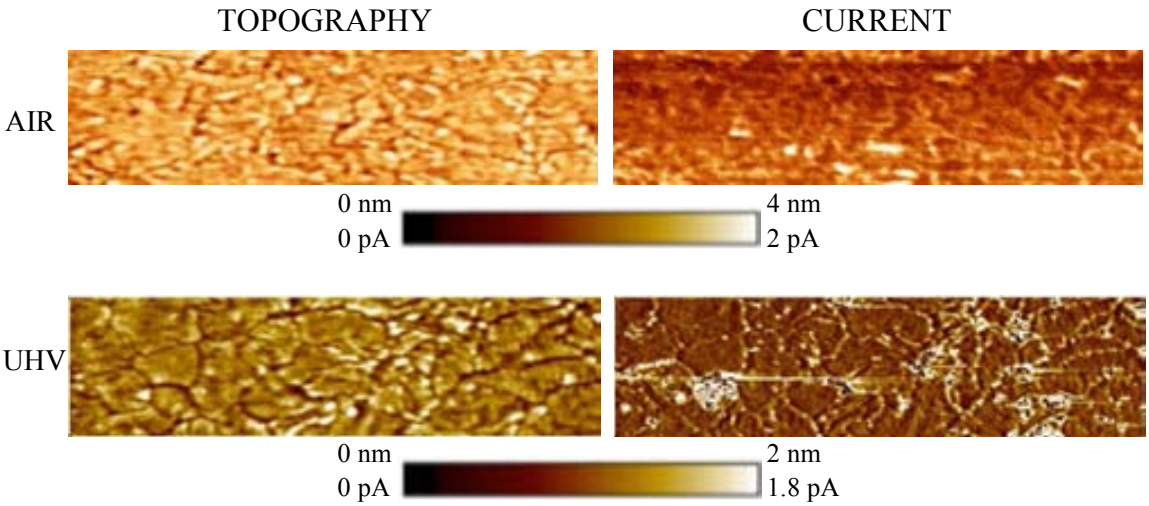

Figure 3.9: Topographical (left) and current (right) images obtained with a CAFM working in air (top) and UHV (bottom) and using a diamond coated tip. Image size: 1000x250 nm^2

At first glance it can be observed that the topographical image obtained in UHV shows a higher definition. This assumption is further supported from the estimation of the roughness in both images (1.40 nm in UHV and 0.5 nm in air). However, the main difference between air and UHV can be observed in the current image. Note that the current image obtained in UHV shows a granular pattern more clear and with GBs much more defined than the current image obtained in air. Therefore, the results suggest that UHV conditions improve the lateral resolution of the CAFM experiment. When such experiments are performed with Pt/Ir and Co/Cr tips the differences are even large.

Therefore, to conclude this section, it has been demonstrated that tip radius clearly affects the AFM resolution. In particular, coated Si tips (normally used in CAFM experiments) do not clearly allow to distinguish Gs and GBs in a polycrystalline structure, as polycrystalline HfO_2 layers. To improve such resolution, experiments in UHV conditions can be performed (information reflected in paper A). Next chapter is devoted to analyze the topography and the electrical properties of a polycrystalline HfO_2 based gate stack from CAFM images obtained in UHV.

CHAPTER IV

Polycrystallization effects on the electrical properties and reliability of HfO_2/SiO_2 based high-k stacks

In chapter I, it was introduced that high-*k* dielectrics have associated new challenges and reliability concerns. Among them, the impact of their polycrystallization on the morphological and electrical properties is still an open question. In this chapter, the effect of the polycrystallization of the HfO_2 based gate stack (described in chapter III), after an annealing process, is investigated at the nanoscale with AFM related techniques (CAFM and KPFM). Its influence on the electrical characteristics as well as its impact on the dielectric breakdown is deeply analyzed. In the same way, TDDB distributions obtained with CAFM at different temperatures in the polycrystalline HfO_2 gate stack are analyzed to investigate the role of the interfacial layer on the BD stack.

4.1 Topographical and electrical properties of as-grown polycrystalline HfO_2 gate stacks

In this section, the impact of the polycrystallization of the HfO_2 layer on the topographical and electrical properties of a HfO_2/SiO_2 gate stack is analyzed at the nanoscale. In chapter III, the influence of the environment on AFM measurements was described. In particular, it was found that UHV measurements allow obtaining the largest resolution. According to this, the correlation between the topographical and electrical properties of the polycrystalline HfO_2 based gate stack (if any) has been evaluated with a CAFM working in UHV to improve the AFM experiments resolution. Diamond-coated Si tips were used to perform the measurements in UHV.

4.1.1 Topographical and electrical correlation

The morphology of the high-k layer was investigated first. Figure 4.1 presents a topographical image (a) showing a surface of 200x200nm^2 and a topographical profile (b), which corresponds to the line shown in the image. Note that a granular structure can be observed in (a). This granular structure has been attributed to the polycrystallization of the high-k layer after annealing (see section 3.2) [Yanev 08]. The grains that can be appreciated in the image correspond to individual (or a cluster of) randomly oriented nanocrystals separated by grain boundaries (GBs, depressions in the figure 4.1.b, indicated by triangles along the profile). A statistical analysis of the grains shows that their mean size is approximately 15 nm, information that is compatible with the grain size obtained from TEM images and with the data reported by other authors [Ho 03].

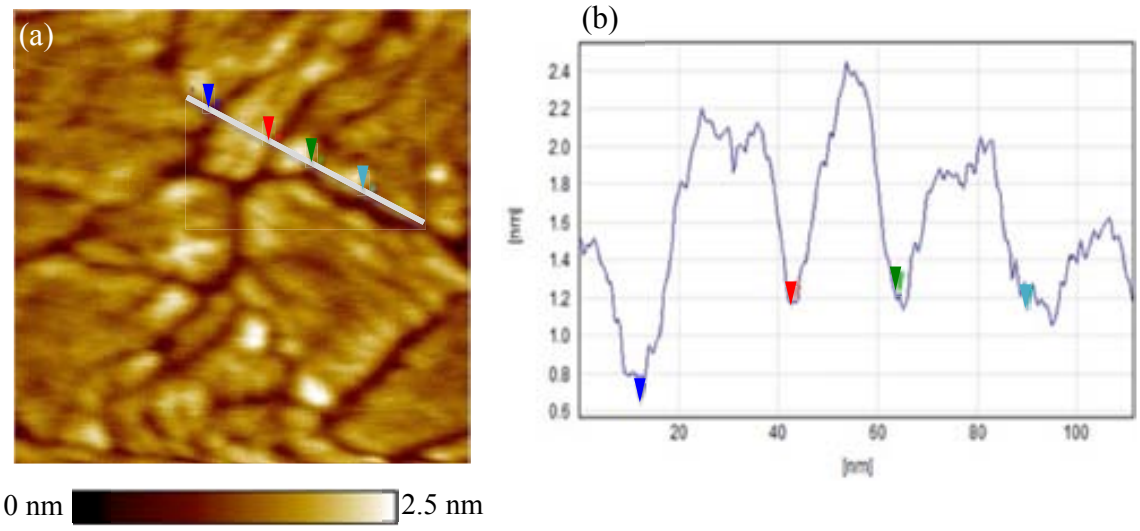

Figure 4.1 (a) Topographical image of a $HfO_2/SiO_2/Si$ structure obtained in UHV (area 200 x 200 nm^2). (b) Topographical profile corresponding to the line shown in (a). Triangles in the profile mark the deeper sites that correspond to GBs.

Note that, although the depressions in figure 4.1 (which correspond to GBs) can be quantified, direct information about the oxide thickness t_{ox} cannot be obtained from this image because t_{ox} of the HfO_2 layer depends not only on the morphology of the scanned

top (dielectric/gate) interface, but also on that of the dielectric/substrate interface, and this information is not available in this experiment. However, despite that, it is reasonable to assume similar grain morphology at both interfaces. Therefore, if this assumption is true, from the results presented in figure 4.1, it can be concluded that t_{ox} is somehow thinner at the grain boundaries. The width of the GBs has also been statistically determined from the AFM image. A value of about 4 nm was estimated. Note that this value is slightly higher than what is obtained from *ab initio* calculations [McKenna 09] (~2 nm), probably because of the proximity to the resolution limits of this technique.

Once the impact of the HfO_2 polycrystallization on its morphology was investigated, its effect on the electrical properties of the gate stack has also been analyzed from the measurement of IV curves and current images. As an example, figure 4.2 shows different IVs curves obtained on both, Gs (filled squares) and GBs (open circles), by applying ramped voltage stresses (RVS) from 0 to -10V to the substrate (these IVs curves were performed in air-conditions and with Pt/Ir coated silicon tips). For low voltages (< 2V), only noise is measured. For high voltages (> 6V) a constant current of 120 pA was measured, which corresponds to the saturation of the setup. From these IVs curves, it can be observed that leakage currents at GB start at lower voltages than at G positions. Therefore, GBs seems to show a larger conductivity.

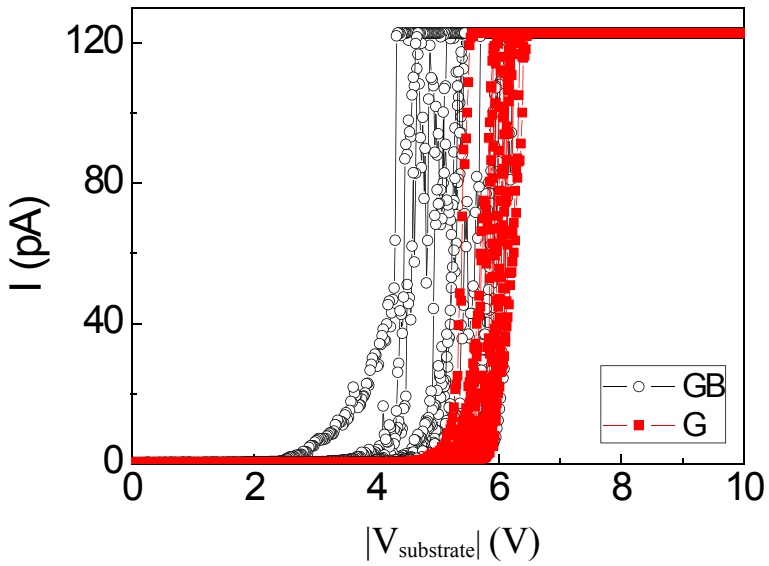

Figure 4.2: IV curves obtained in air on both, Gs and GBs, by applying ramped voltage stresses (RVS) from 0 to 10V. GBs show higher conductivity than grains. Note that currents above 120 pA cannot be measured due to the saturation of the setup.

These results are further supported from current images obtained simultaneously to topographical images (figure 4.3), which will also help to check if there is any correlation between the morphology and the electrical properties of the gate stack. Figure 4.3(a) corresponds to the current image obtained simultaneously at the region of figure 4.3(b), which shows a map of the surface. Note that in the current image a granular pattern is clearly visible, which is practically identical to that measured in the topographical map. In particular, one can see that leakage sites, with currents above the

background level (which was measured over the nanocrystals), are mainly located at the depressions, that is, at GBs. In figure 4.4(a) a zoom of figure 4.3 is showed. In this image, a profile has been drawn and represented in figure 4.4(b) to clearly observe the correlation between topography and current. The topography has been represented by a dashed line meanwhile the current has been represented by a continuous line (current).

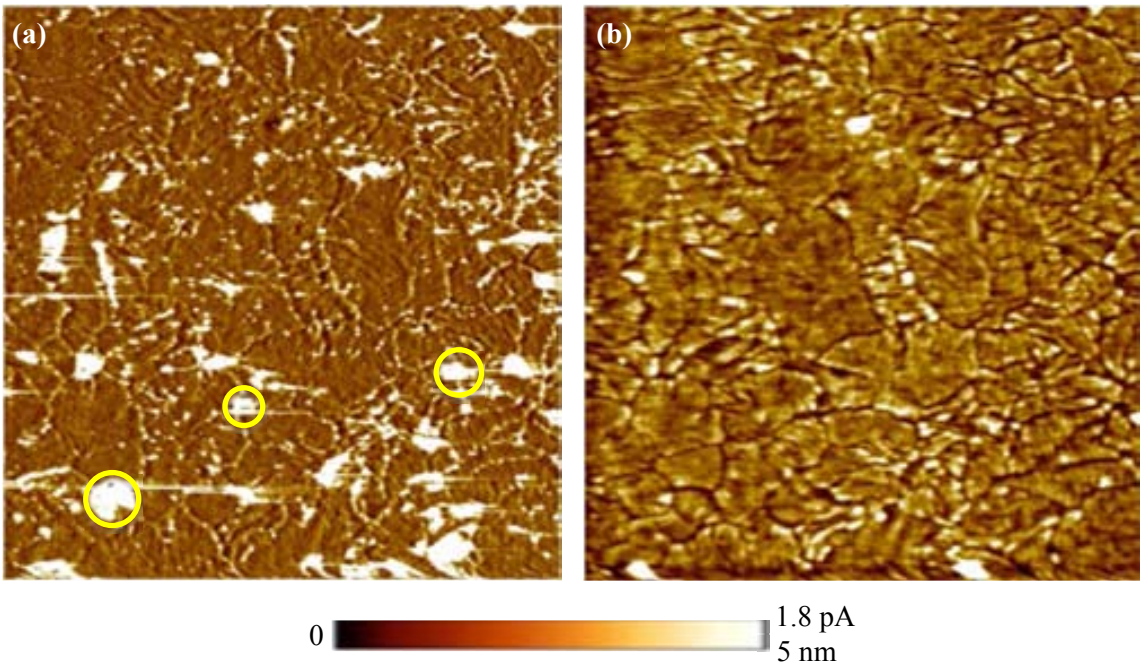

Figure 4.3: Current (a) and topographical (b) image obtained simultaneously in UHV at V_{sub}= - 6.5 V on a $HfO_2/SiO_2/Si$ structure with an area of 1x1 μm^2. Note that leakage sites at the pA-range in (a) are related to GBs in (b). Circles in (a), also located at GB, indicates BD spots with currents in the nA range.

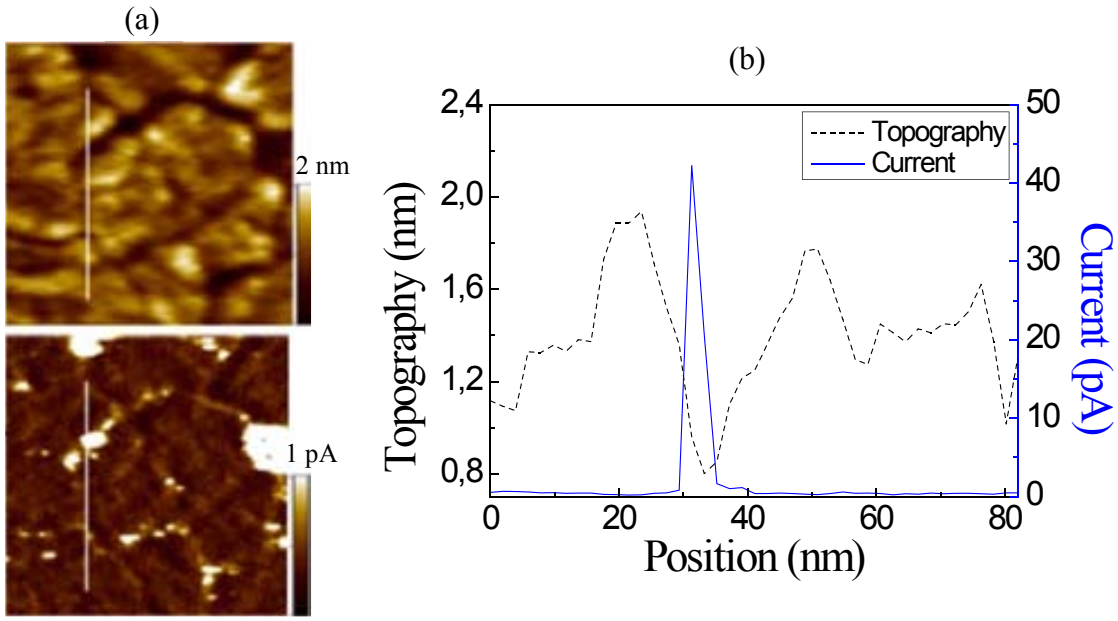

Figure 4.4: (a) Zoom-in of the topographical (top) and current (bottom) image shown in figure 4.3 (with an area of 168x168 nm^2). (b)Topographical (dashed line) and current (continuous line) profiles obtained along the white lines in the zoom-in images. Note that higher leakage current are measured at the topographical depressions associated with the GBs.

From these results, it seems that only those positions located at the GBs show higher currents compared to those measured on the grains (background current). This qualitative observation has been verified statistically. Figure 4.5 shows the Z-axis relative position (Z_{rel}) of more than 70 leakage spots (exhibiting a current greater than 0.5 pA) with respect to the Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level (dashed line) versus their maximum current. Note that most of the leakage sites are below the zero-reference level (i.e., in the topographical depressions and, therefore, in the GBs). Moreover, two groups of sites can be clearly distinguished, one with currents in the picoampere-range (leaky sites) and other with currents in the nanoampere range (BD spots). (Information reflected in paper B). In this section, the attention is mainly focused on the leaky sites, meanwhile the second group, BD spots, will be treated in section 4.1.2.

Since leaky sites are mainly concentrated at GBs and, on the other hand, these sites could show a smaller t_{ox} (figure 4.1), it could reasonable to conclude that GBs are more conductive because the gate stack is thinner in such positions. However, there are other reasons that could also explain this increase of conductivity, as the presence of an excess of defects. Therefore, do leaky sites show larger currents because they are located in positions with a smaller oxide thickness or because they are weaker from an electrical point of view (for example, due to a higher density of traps at the GB, which could support the TAT, Trap Assisted Tunneling)? This is the next objective that will be attempted to answer in the following.

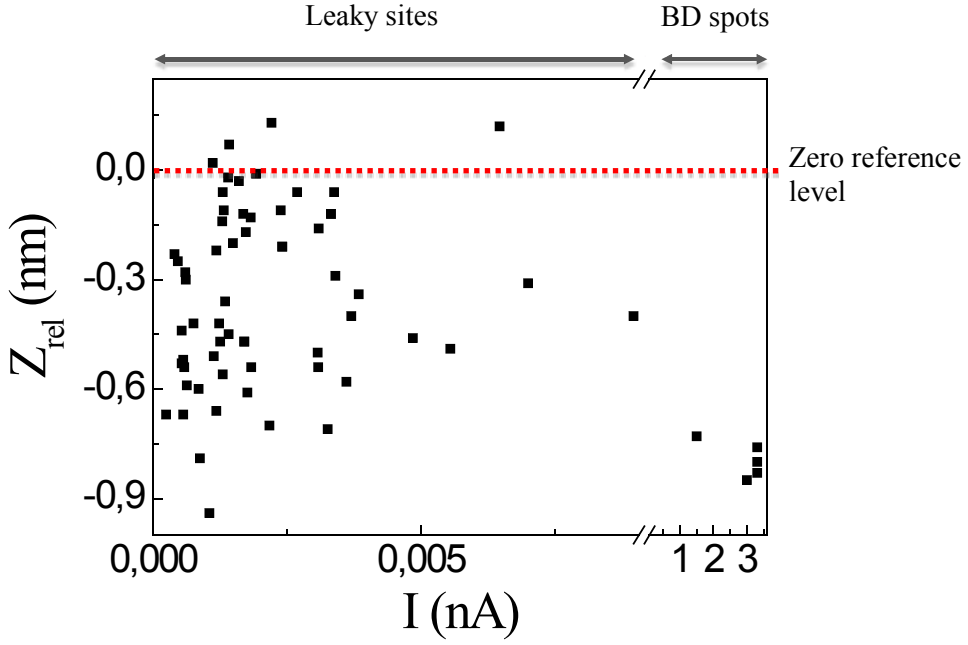

Figure 4.5: Z-axis relative position (Z_{rel}) of more than 70 leakage spots (with currents greater than 0.5 pA) vs their maximum current. Z_{rel} of a leakage site is defined as its Z-position with respect to Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level (dashed line). Note that most leaky sites are located in topographical depressions (below the reference level), that is, at the GBs.

To try to answer this question first it must be analyzed if there is any correlation between the Z_{rel} position of the leaky sites, which reflects the dielectric thickness at a given location, (that is, lower Z_{rel} values correspond to thinner dielectrics), and their current level. Taking a look at the group of the leakage sites in figure 4.5, there seems not to be any apparent correlation between the leakage currents and Z_{rel}, that is, the dielectric thickness. This suggests that the conductivity of the leaky sites, although it could be somehow affected by the dielectric thickness, is primarily determined by the electrical properties of the GBs. Actually, this hypothesis is further supported by KPFM measurements. In addition to CAFM measurements, KPFM has been employed to obtain topography and the probe tip-sample CPD (Contact Potential Difference) maps of the same structures, which can give information about the amount of trapped charge in the dielectric at the probe tip position. Figure 4.6 shows a topographical (a) and CPD (b) image obtained simultaneously with a KPFM working in air conditions on the same gate stack than that analyzed in figure 4.3. Topographical (circles) and CPD (continuous line) profiles along the lines drawn at both images are also shown in (c).

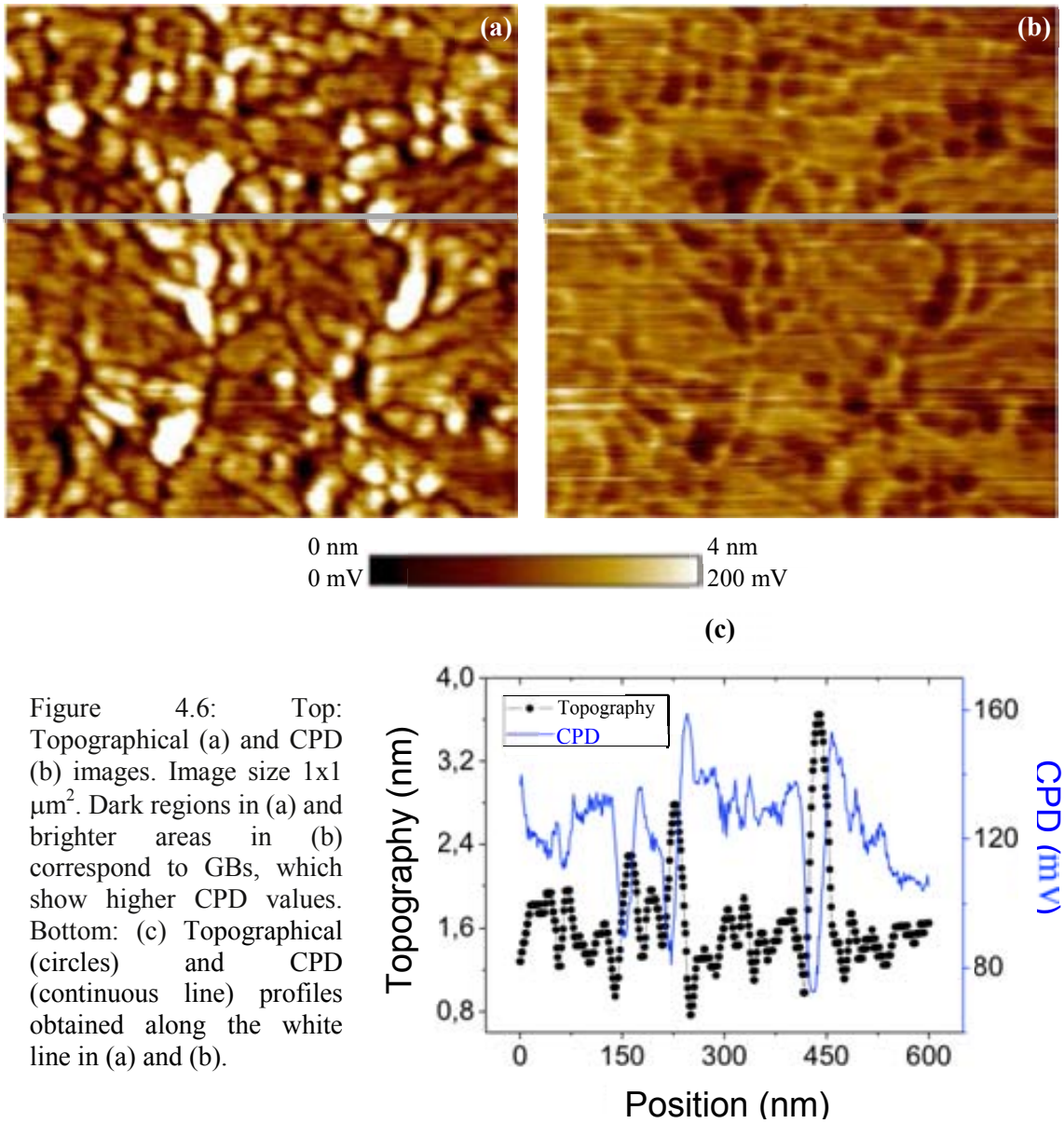

Figure 4.6: Top: Topographical (a) and CPD (b) images. Image size 1x1 μm^2. Dark regions in (a) and brighter areas in (b) correspond to GBs, which show higher CPD values. Bottom: (c) Topographical (circles) and CPD (continuous line) profiles obtained along the white line in (a) and (b).

Again, two identical patterns (related to the polycrystallization of the high-k layer) are observed in both images. In this case, an increase of the CPD signal (brighter colors) is detected at the GBs (depressed regions in (a)). As other authors already pointed out (Son 08, McKenna 09), a higher CPD signal can be interpreted as downward band bending, which indicates a larger concentration of positive charges (or absence of negative charges) at a given location. A statistical analysis of the CPD signal (figure 4.7) at the locations, reveals an absence of correlation between the CPD signal at the GB sites and the depth of these sites with respect to the surface of the adjacent grains (h_{nc} - h_{GB}). Therefore, the concentration of positive charges (proportional to the CPD signal) at the GBs does not depend on the magnitude of their surface depression. These results agree with the previous CAFM measurements, suggesting that the increase of current through GBs cannot be only related to the reduction of the thickness of the stack (if any), but also to the electrical properties of them, as for example, an increase/decrease of the positive/negative charge concentration at these positions. As other works indicated [McKenna 09], the variations of charge concentration at GBs with respect to nanocrystals could be related to the diffusion of positive charged oxygen vacancies to the GB. At high enough density of O-vacancies at the GB, a localized conductive "sub-band" is formed along the GB, which effectively constitutes a percolation path for the current flow [Bersuker 10]. The injected electrons captured by the GB defects are effectively transported through the percolation path along the GB. Therefore, electron hopping between the vacancies along the GB (between the localized states in the gap) could be responsible for the leakage current at the GBs observed in figure 4.3.

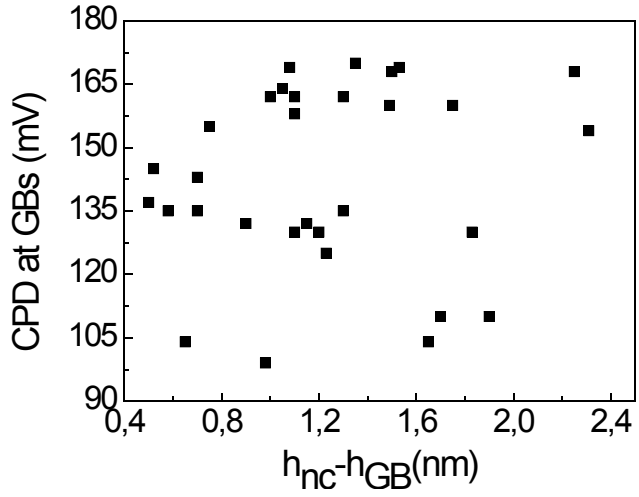

Figure 4.7 (c) Statistical analysis of the CPD signal showing the potential on the GB sites (V_{GB}) vs. the depth of these sites with respect to the surface of the adjacent grains (h_{nc} - h_{GB}). Absence of a correlation between the CPD signal and (h_{nc} - h_{GB}) indicates that the CPD profile is not caused by the surface topography.

Therefore, to conclude this section, it has been demonstrated that a clear correlation between the oxide morphology (determined by the polycrystallization of the high-k layer) and the electrical properties of the gate dielectric exists: conductivity through the dielectric film is higher along the GBs probably due to its electrical weakness.

Moreover, since the average size of leaky sites was statistically estimated to be 3 nm (comparable to the width of the GBs), these results suggest that they are completely located in the GBs, without affecting the grains of the structure. (Paper C)

As it was previously announced, in addition to the leaky sites, figure 4.3 and figure 4.5 also show the existence of other sites with currents greater than nanoamperes (some examples are marked in circles in figure 4.3). The current level of these sites reveals the possible existence of BD spots. Although figure. 4.3 corresponds to an as-grown oxide, these BD events were, probably, triggered by the constant voltage applied during the scan to obtain the topographical and the current image. In next section, a detailed analysis of the BD spot characteristics as their conduction, size, location where they are preferentially triggered and propagation (if any) is performed.

4.1.2 Analysis of the BD spots.

In this section, the attention will be centered on the characteristics of the BD spots observed in figure. 4.3. Regarding their dimensions, note that BD spots seem to be much larger (~ 20nm) than the leakage spots (~3nm) and GBs width (~4nm). To investigate in more detail their characteristics, a quantitative analysis has been performed on several spots. Table III shows the diameter, area and maximum current of 12 BD spots. Note that two values of the area are given at the area column. Area 1 corresponds to the area of the BD spot with currents larger than 1nA and Area 2 to the area with currents larger than 1 pA above the background level. Last row shows the average of such parameters.

Table III: Diameter, area and maximum current of several BD spots measured in figure 4.3

Spot	Diameter (nm)	Area (nm^2)		I_{max} (nA)
		Area 1(I >nA)	Area 2 (I >pA)	
1	6.2	30.6	968	3.3
2	3.1	7.7	1374	3.3
3	3.1	7.7	716	2.6
4	3.8	11.5	245	1.8
5	5.4	23.0	903	3.3
6	2.2	3.8	1260	2.3
7	3.8	11.5	600	3.3
8	2.2	3.8	834	1.7
9	7.3	42.1	3933	3.3
10	3.8	11.5	134	3.3
11	3.1	7.7	1681	2.8
12	2.2	3.8	3140	1.7
Mean	3.5	13.7	1241	2.7

From the data presented on table III, different observations can be extracted. First of all, the distinction of two regions, with very different current levels. A first region (Area 1), which reaches currents of nA, whose area is in the range of few tenths of nm^2, and a

second region (Area 2), which shows lower currents (~pA), but a greater affected area ($10^3 nm^2$). This suggests that the BD affected area (much larger than the dimensions of leaky sites and GBs) spreads to the neighbourhood. Since these areas (Area 2) show a higher conductivity than the background current registered in nanocrystals, it can be concluded that BD propagate beyond GBs, reaching closer nanocrystals. However, another feature that was observed is that BD propagation, beyond the point where it is triggered, is not uniform. As an example figure 4.8 illustrates a topographical (a) and current (b) image of a BD spot and the current (triangles) and topographical (circles) profiles obtained along (c) and across (d) the BD spot. Arrows in image (a) and (b), indicate where the profiles were obtained.

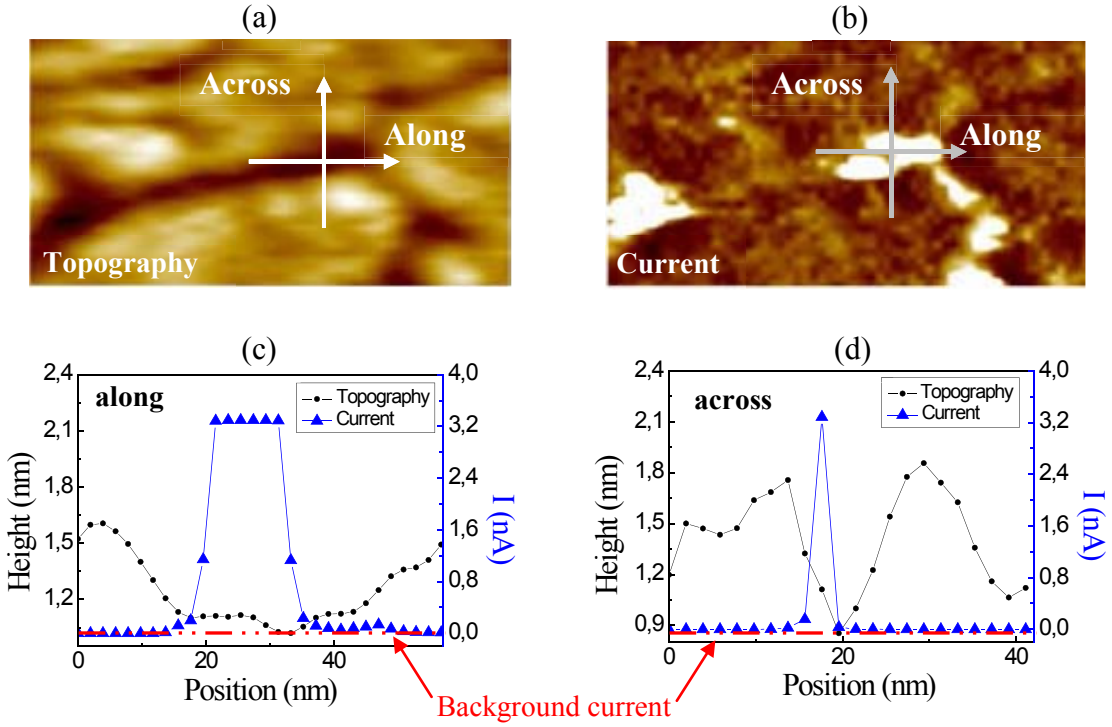

Fig. 4.8: (a) topographical and (b) current images with arrows that indicates the across/along direction in the GB. Current (triangles) and topographical (circles) profiles of the BD spot along and across the grain boundary were plotted in (c) and (d) respectively.

Note that Area 1 (with currents of nA) is wider along the grain boundary than across. The average width along and across the GB was found to be about 15nm and 5nm, respectively, which, in the last case, is of the order of the width of the grain boundary. Hence, the area that confines most of the current flowing through the BD spot (Area 1), is located entirely in the grain boundaries, suggesting that BD basically occurs in that positions. Taking into account that weak spots are also mainly located in the grain boundaries (figure 4.3), it could be suggested that the leaky sites are probably the precursors of BD events. Some of these weak spots degrade faster than nanocrystals, mainly due to their electrical weakness, triggering a BD event. Once BD is triggered, currents of nA in areas of ~$10nm^2$ (BD spot) can be measured. These areas are compatible with the BD spot area statistically suggested and are entirely located in the GB. However, BD propagates to larger areas. The results show that they are mainly propagated along the grain boundaries: their width along the grain boundary is larger

than across. Actually, only the Area that corresponds to the grain boundary is really affected showing currents of nA. In the transversal direction, BD propagation does not advance significantly due to the presence of the nanocrystals, with a harder dielectric strength. Nanocrystals are only slightly affected: the electrical damage spreads to the surrounding area, including nanocrystals, although with currents much smaller than those measured in the grain boundaries.

Until now, as-grown polycrystalline HfO_2/SiO_2 gate stacks were analyzed. In next section, this structure will be subjected to different electrical stresses and the evolution of the electrical properties and breakdown spot properties will be studied in more detail.

4.2 Electrical properties of stressed polycrystalline HfO_2 gate stacks

The impact of an electrical stress on the electrical properties of the polycrystalline HfO_2/SiO_2 gate stack was studied after measuring consecutive current maps on the same area and sequences of I-V characteristics at single locations. Although UHV has demonstrated to improve the AFM resolution and to be a good environment to perform this kind of measurements, in this case, the experiment was performed in air conditions. Pt/Ir tips were used in this experiment. In figure 4.9, three consecutive current maps obtained with CAFM on the same area by applying a substrate voltage of -4.2V are shown. Although Gs and GBs are not so well defined as the image obtained under UHV conditions, the current maps again seem to show a granular structure, related to the polycrystallization of the high-k dielectric, with leaky sites (brighter areas) concentrated around the GBs. In this case, the width of the GBs (figure 4.9(a), fresh oxide) was measured to be ~15 nm, which is wider than the extracted value from UHV results (~ 4 nm) and simulation-based estimations (< 2 nm), [Bersuker 10] probably due to the lower CAFM resolution in air. [Frammelsberger 07] This could also explain why leaky sites are larger (~50 nm) than those measured in UHV and why the grains are larger (Ø ~100 nm) than the size obtained by TEM experiments (~15 nm) and in figure 4.3. The grains shown in figure 4.9 could correspond to a subset of a larger grain cluster in the sample. Despite the limited resolution, the experiment does not impede the ability of CAFM to distinguish the most conductive GBs and analyze their evolution with the stress.

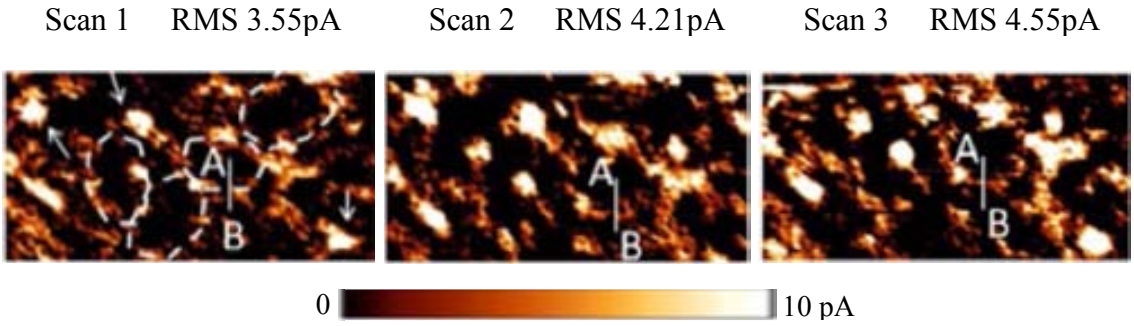

Figure. 4.9. Changes of the current through the HfO_2 polycrystalline layer (with the grains clearly distinguishable) obtained by three consecutive current scans of the same area (750 nmx400 nm). The current through the GBs (outlined by the dashed lines) increases with each subsequent scan, i.e., with longer stress time. In particular, the maximum values of the current measured along the A-B line during the scans 1, 2, and 3 are 2.1 pA, 2.4 pA, and 4.0 pA, respectively. Arrows indicates BD spots, which propagate into the surrounding grains.

The evolution of the leakage current with subsequent scans over the same area is equivalent to that caused by electrical stress of different durations. The conductivity of the leakiest spots is observed to gradually increase under subsequent CAFM scans of the dielectric surface; in other words, under continuous stress, the GBs become more conductive and bigger. These qualitative results have been further verified by analyzing the evolution of the maximum current and area of different weak spots as the stress proceeds (Table IV). As it can be observed, the global tendency is that the leaky sites (at GBs) become bigger and more conductive with the stress. On the other hand, the magnitude of the background current in figure 4.9 (grains, dark areas) seems to be very stable under electrical stress (0.5 pA for all images), and no new conductive spots were generated. As a result, the overall current level and inhomogeneity of the electrical conduction through the gate stack increases with stress time, which can also be quantitatively observed from the current dispersion magnitudes (rms values, see figure 4.9) after different scans. Hence, the gate stack around the grain boundary regions becomes more conductive than the grain regions under the stress.

Table IV: evolution of the maximum current and area of different weak spots as the stress proceeds during the scans shown in figure 4.9

Spot Number	Magnitude	Scan 1	Scan 2	Scan 3
Spot 1	I_{MAX} (pA)	27	30	33
	Area (10^3 nm^2)	3.9	6100	9.7
Spot 2	I_{MAX} (pA)	14	23	17
	Area (10^3 nm^2)	1.7	3.3	1.6
Spot 3	I_{MAX} (pA)	16	23	25
	Area (10^3 nm^2)	1.9	2.0	2.7
Spot 4	I_{MAX} (pA)	6	11	21
	Area (10^3 nm^2)	-	1.1	1.8
Spot 5	I_{MAX} (pA)	6	12	25
	Area (10^3 nm^2)	-	0.5	1.2
Spot 6	I_{MAX} (pA)	9	17	19
	Area (10^3 nm^2)	0.2	0.2	1.0
Spot 7	I_{MAX} (pA)	20	18	21
	Area (10^3 nm^2)	2.6	3.4	1.2
Spot 8	I_{MAX} (pA)	8	10	17
	Area (10^3 nm^2)	0.5	2.9	4.8

A comparative analysis of conduction characteristics of the GBs and grains was performed from the measurement of I-V curves on fresh and electrically stressed sites. Figure 4.10 shows typical sets of four I-V curves sequently measured on the NCs (filled symbols) and GBs (open symbols) regions. By comparing the first measurements on the fresh locations (NC_IV1 and GB_IV1), it appears that the grains are less conductive than the GBs, in agreement with Shubhakar 11 and figure 4.3. Qualitatively different I-V dependencies measured on the GB and grain sites indicate that conduction through these structural features might be governed by different mechanisms (Murakami 11). For the GBs, note that after the first I-V curve (squares, open symbols), the second one (circles, open symbols) show much larger currents, suggesting that a dielectric BD was triggered by the first I-V sweep (figure 4.10, GB_IV1 and GB_IV2). On the contrary, when bias is applied to the grains (figure 4.10, NC_IV1- NC_IV4), the I-V curves progressively shift to lower voltages (stress-induced leakage current [Shubhakar 11) and BD is not triggered until several I-V sweeps have been applied. However, when BD is reached, it seems stronger than on the GBs: NC_IV4 exhibits an ohmic characteristic indicating its metallic nature [Szot 06].

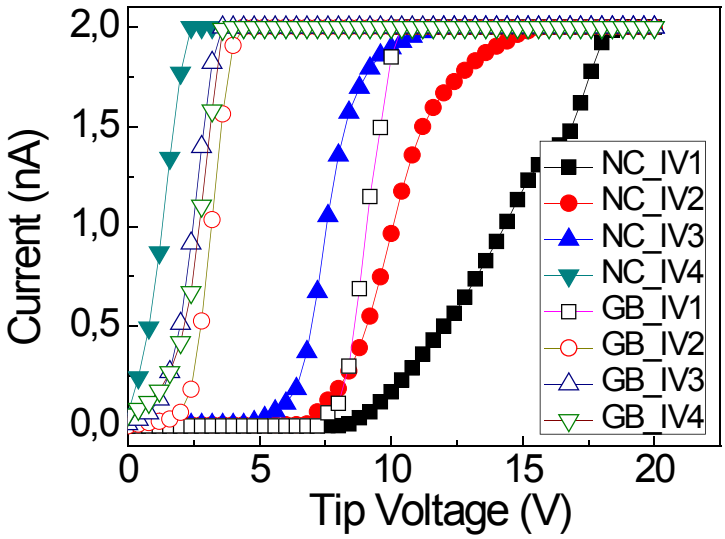

Figure: 4.10. Example of the evolution of the current, through a grain (NC IV) and GB (GB IV), after applying 4 consecutive voltage ramps at each position. The maximum current that can be measured with this setup is 2nA.

To further analyze electrical conduction at these locations, the I-V curves were measured with the enhanced-CAFM (having a larger dynamic range) [Blasco 05 ^{IV}] (figure 4.11) on both GBs (open symbol) and grains (filled symbol). Again, the fresh I-V curves (GB/NC_IV1)) show greater currents at the GB locations (with two conduction regimes), similar to those observed in other HfO_2-based stacks [Uppal 09, Aguilera 06, Murakami 11], at which the BD generally occurs at lower voltages. For grains (filled symbol), the initial current is lower and the pattern of the two conduction regimes is not seen. Moreover, the BD is triggered only after several I-V sweeps, indicating greater grain robustness to electrical stress [Lanza 11].

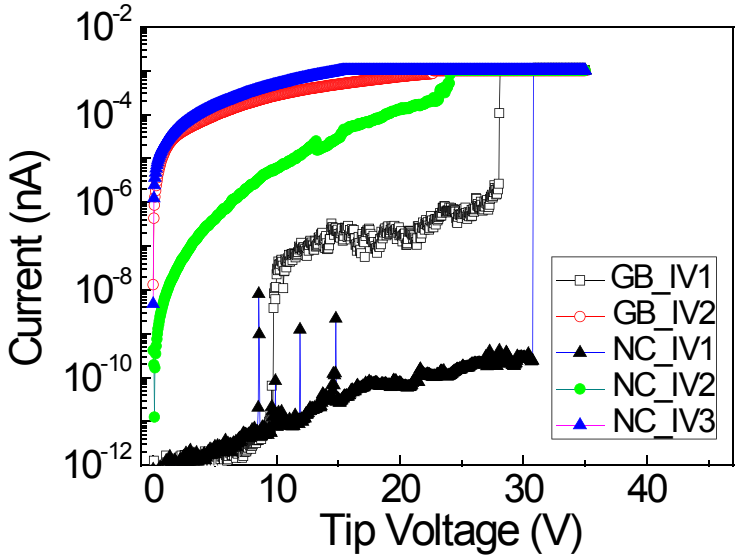

Figure. 4.11 Example of the evolution of the current through a grain (NC IV) and GB (GB IV) after applying 3 consecutive voltage ramps at each position, using an ECAFM. With this configuration a maximum current of 1mA can be measured.

Higher initial currents at the GBs could be related, as it has been previously commented, to the higher concentration of positive charges there (figure 4.6(b)), likely associated with the segregation of positively charged oxygen vacancies at the GBs [Bersuker 10]. This conclusion is consistent with earlier reported simulations of the trap-assisted tunneling current through these defects [McKenna 09]. Since the GBs in the HfO_2 film are more conductive, more of the voltage applied to the dielectric stack drops across the region of the interfacial SiO_2 layer overlaid by the GBs than the SiO_2 region under the grains. This could lead to greater degradation of the former [Bersuker 11'] resulting in a gradual increase in the current measured at the GBs as the stress proceeds and eventual BD of the entire gate stack. That would explain why BD occurs first at GBs: since SiO_2 (which actually controls the breakdown of the stack [Aguilera 06]) degrades faster at GBs, the gate stack loses its dielectric properties first at these positions than in nanocrystals.

In conclusion, in this section, the impact of an electrical stress on polycrystalline HfO_2/SiO_2 gate stacks has been analysed. Under an electrical stress, GBs become more and more conductive than nanocrystals, which could be related to the degradation of the SiO_2 interface layer, enlarging the electrical inhomogeneity of polycrystalline high-k layers and impoverishing the gate stack reliability, since BD occurs before at GBs than at nanocrystals. However, when BD is reached at the grains, it seems stronger than at the GBs. (Information reflected in paper C)

4.3 BD distributions and the role of the interfacial layer in polycrystalline HfO_2 based gate stacks

In the previous section it was demonstrated that BD is triggered mainly at GBs, probably due to a faster degradation of the SiO_2 interfacial layer (IL) at these sites.

However, the evaluation of the breakdown mechanism in high-k gate stacks in advanced transistor technology is significantly complicated, due in part to their multilayer structure. As an example, the different defect generation rates of high-*k* and the SiO_x IL may lead to bimodal BD statistical distributions [Nigam 09]. Alternatively, one of the layers may control the overall high-*k*/IL stack breakdown, specifically the IL, while the high-*k* may have little impact on device lifetime [Blasco 05', Bersuker 08, Degraeve 99]. It is, therefore, critical to investigate the roles of the IL and HK dielectric on the overall degradation and breakdown of the gate stack. This issue will be addressed in this section. The impact of the HfO_2 polycrystallization on the BD distributions is also studied.

To do that, time dependent dielectric breakdown (TDDB) has been studied at the nanoscale by applying a CVS using the AFM tip. This experiment has been performed within a wide range of temperatures: 30ºC, 60ºC, 90ºC, 120ºC, 180ºC, and 210ºC, using a CAFM, which can operate up to 240ºC. A statistically significant number of data points was collected for each T and the corresponding Weibull distributions [Erlbacher 11] was analyzed. The CAFM, as already shown in section 2.3, offers high lateral resolution (~10 nm)[Fiorenza 06, Lanza 11], allowing to perform a statistical analysis of t_{BD} on the grain (G) and grain boundary (GB) locations, independently. The electrical BD was induced applying a CVS of -8.2V to the sample (tip was grounded) and t_{BD} was extracted by measuring current-time characteristics. When the current reached 10nA, which corresponds to the saturation of the setup electronics, BD was assumed to occur. This can be observed in figure 4.12, where an example of the I-t characteristics is shown.

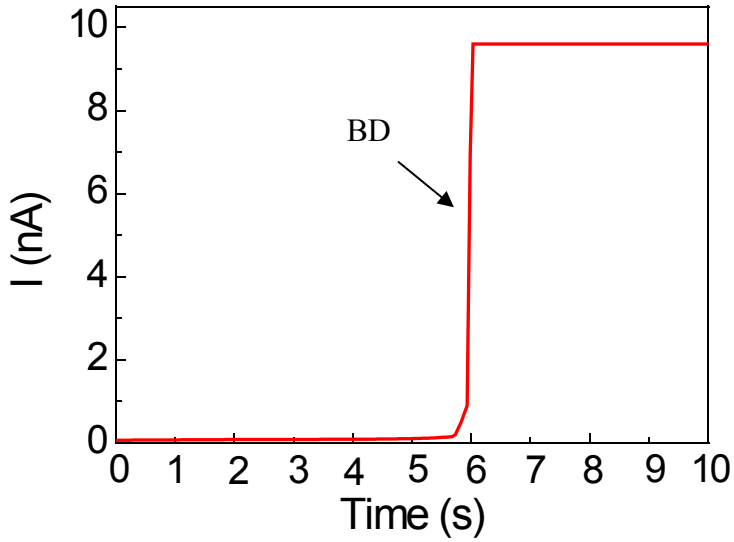

Figure. 4.12: Example of an I-t characteristics when a CVS of -8.2V is applied to the polycrystalline HfO_2 based gate stack. T_{BD} is considered to happen when I reaches 10 nA, which corresponds to the saturation of the setup.

Figure 4.13 shows the t_{BD} Weibull distributions obtained at different temperatures. Note that a bimodal behaviour (indicated by the dashed line) with smaller slopes (β) for longer t_{BD} can be observed. Since the HfO_2 of the stack is polycrystalline and Gs and GBs have different electrical properties, one could wonder if this bimodality could be related to the sample polycristallization. To investigate the origin of the bimodality, the

t_{BD} distributions measured on GBs and Gs were analysed independently. To establish a distinction between G and GB locations, the magnitude of the initial current [I(t=0s)] was considered. Since GBs have been shown, in previous sections, to be leakier than Gs (in these HK layers), those positions with higher initial currents were assumed to correspond to GBs. As an example, figure 4.14(b) shows the cumulative probability distribution of I(t=0s) of the sites stressed at 60ºC. Two clear regions can be distinguished, which have been attributed to Gs (low currents) and GBs (high currents), respectively. Once the sites corresponding to Gs and GBs were distinguished, the Weibull plot was represented independently for both positions. Figure 4.14(a) shows the Weibull plots of the t_{BD} distributions measured on Gs (squares) and GBs (circles) at 60ºC, which can be fitted by Weibull distributions (continuous lines).

Note that, although at first glance it could be interpreted as a bimodal behavior, this assumption cannot be concluded so clearly as in figure 4.13. First, because the criterion to discern between the sites corresponding to G and GB is not totally accurate. Therefore, some of the points with low t_{BD} in the G distribution could correspond to GB sites and viceversa. Second, the tails at small t_{BD} in the GBs distribution correspond to times close to the setup resolution. In figure 4.15, G and GB TDDB data are analyzed independently. Figure 4.15(a) and 4.15(b) show the Weibull slope, β, and, scale factor, η (time for a 63% probability of BD occurrence), respectively, experimentally obtained at Gs (squares, filled symbols) and GBs (circles, filled symbols) for all T. Numerical values are shown in table V.

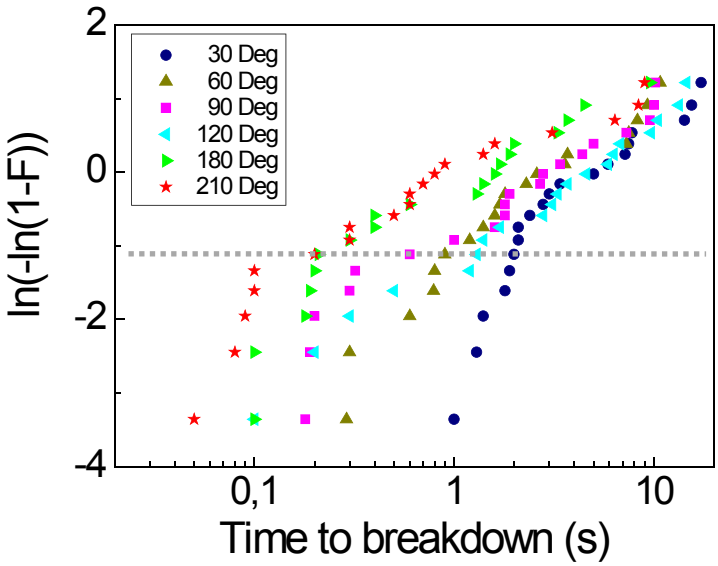

Figure 4.13: TDDB distributions obtained at different temperatures. Dashed line outline the bimodal character of the distributions.

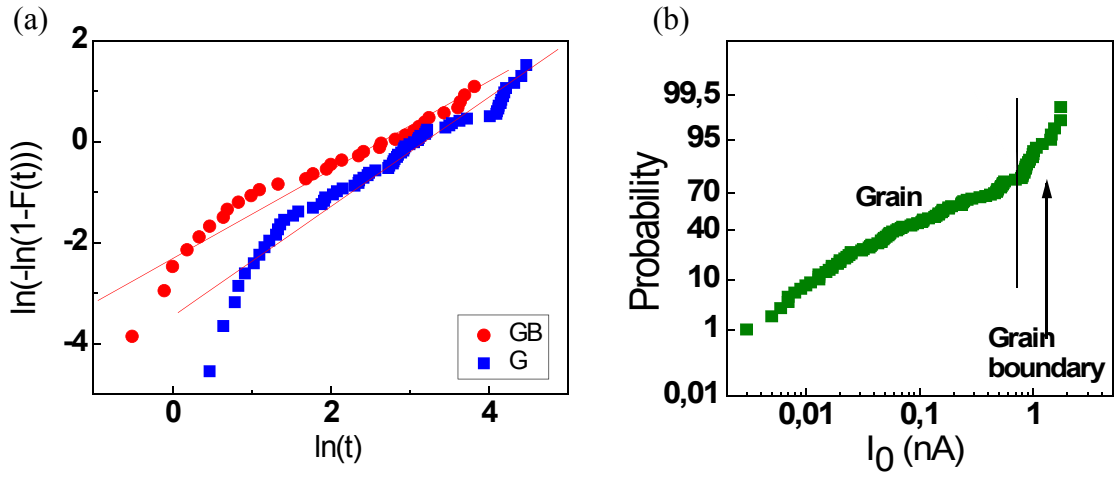

Figure 4.14: (a) Example of TDDB Weibull distributions obtained at 60ºC, at G (squares) and GB (circles) sites. (b) Cumulative distribution of the initial leakage currents, I(t=0s). Two types of locations with low (G) and high (GB) currents can be discerned

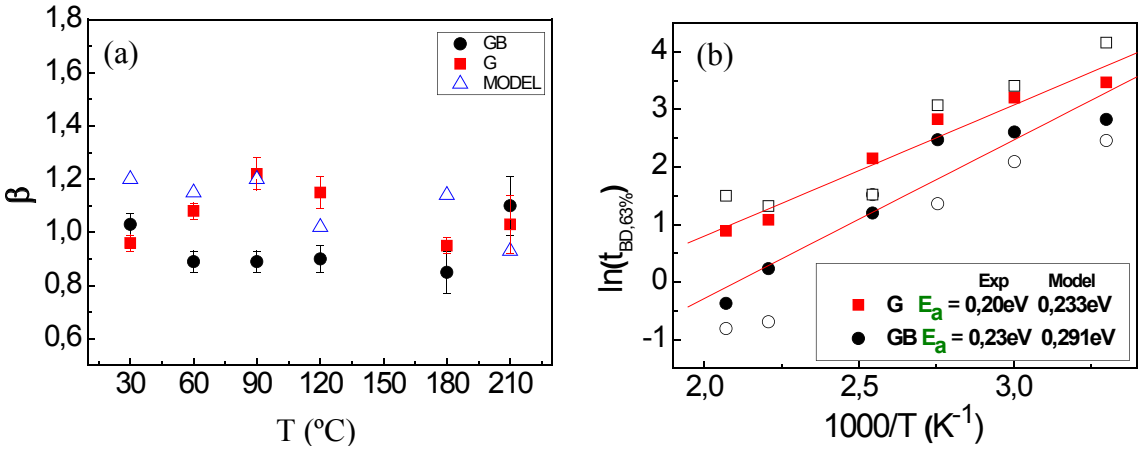

Figure 4.15: Experimental (filled simbols) and modeled (open symbols) values of β (a) and η (b). Squares correspond to G and circles to GB sites (in (a); β was assumed to be the same at both sites in the model). The lines in (b) correspond to the Arrhenius dependency of the η values. E_a is the extracted activation energy for the G and GB data sets.

Table V shows the numerical values of the Weibull parameters extracted from G and GB distributions at different T Plotted in figure 4.15

	GB		G	
T(º)	η	β	η	β
30	**16.86**± 0.14	**1.03**± 0.04	**32.10**± 0.15	**0.96**± 0.03
60	**13.55** ± 0.13	**0.89**± 0.03	**24.62**± 0.15	**1.08**± 0.03
90	**11.84**± 0.19	**0.89**± 0.04	**16.91**± 0.13	**1.22**± 0.06
120	**3.32** ± 0.10	**0.90**± 0.05	**8.64** ± 0.15	**1.15**± 0.06
180	**1.42** ± 0.12	**0.85**± 0.08	**2.96** ± 0.05	**0.95**± 0.03
210	**0.69** ± 0.11	**1.10**± 0.11	**2.44** ± 0.14	**1.03** ± 0.11

Note that when G and GB TDDB data are analyzed independently (figures 4.14(a) and 4.15), the Weibull distributions exhibit similar slopes. Moreover, the bimodal feature arises only when G and GB data are combined within the same Weibull distribution (figures 4.12 and 4.13), suggesting that differences in the electrical properties of both types of sites in the HK layer can be the origin of such bimodal behavior. This hypothesis is supported by modeling the global TDDB distribution, F(t), as a combination of two different breakdown distributions corresponding to G and GB:

$$F(t) = P_{GB} \cdot F_{GB}(t,\beta,\eta_{GB}) + (1 - P_{GB}) \cdot F_G(t,\beta,\eta_G) \qquad \text{Eq. 4.1}$$

Being F_G and F_{GB} theWeibull distributions for Gs and GBs. P_{GB} and P_G are the probability that the randomly positioned CAFM tip was over a GB or G respectively:

$$P_G = \frac{N_G}{N_T} \quad P_{GB} = 1 - P_G \qquad \text{Eq. 4.2}$$

Where, N_G is the number of measurements on a grain, N_{GB}, the number of measurements on a grain boundary and N_T, the total number of measurements. Assuming that β is similar at Gs and GBs (see figure 4.15 and table V), the same β values were considered in both cases, as suggested by the data in figure 4.15. Figure 4.16 shows the global Weibull distributions F(t) at 60ºC (circles) and 210ºC (squares) fitted to the model (continuous line) proposed in equation 4.1 (dashed lines help to see the bimodal behavior of the distributions). The proposed equation 4.1 fits the global TDDB distributions well, with β and η values close to those experimentally obtained over the entire range of temperatures (open symbols in figure 4.15(a) and (b)). Analyzing the Weibull parameters extracted from G and GB distributions at different T in more detail, (figure 4.15 and Table II), it can be concluded that β is independent of the measurement position (G or GB) and temperature. However, for a given T, η is lower for GBs than for Gs. This means that, on average, the GBs sites break faster, which is consistent with the observed preferential BD at the leakiest positions (GBs) probably due to the excess of O-vacancies accumulated in these sites.

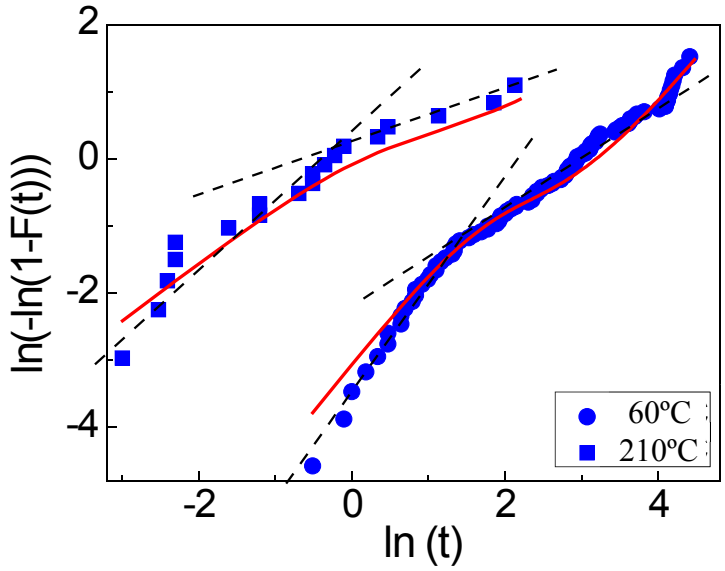

Figure 4.16: TDDB distributions at 60ºC (circles) and 210ºC (squares) fitted using the model proposed in equation 4.1 (continuous line). Broken lines outline the bimodal character of the distributions.

Moreover, η decreases with T [Wu 05], which could be related to a higher rate of trap generation at higher temperatures [Chowdhury 09]. From the temperature dependency of η, the activation energies (E_a) of BD-related traps at Gs and GBs have been estimated assuming an Arrhenius dependency. In figure 4.15(b), the lines correspond to the Arrhenius dependency of η for the data measured on Gs (filled circles) and GBs (filled squares) locations. Similar activation energies (E_a) of 0.20±0.04 and 0.23±0.02eV were extracted for Gs and GBs, respectively. These values are also close to those obtained from equation 4.1 (figure 4.15(b), open squares). Since E_a reflects the nature of the defects, this result suggests that defects with similar characteristics are likely responsible of the BD triggered at both G and GB sites. The similar β and E_a values at Gs and GBs (though with smaller η for the latter) suggest that the same process could trigger BD at both sites. Considering also that SiO_2 β does not depend on T [Wu 05] and an E_a of ~0.2-0.25eV has been extracted for the SiO_2 IL in the HK gate stack [Chowdhury 09, Shanware 00], these results indicate that the stack BD could be triggered by the BD of the IL underlying the HfO_2 film, as was suggested earlier [Bersuker 08, Bersuker 10', Bersuker 07]. In particular, [Bersuker 10] proposed that the formation of the BD path in HK gate stacks might be initiated by the degradation of the SiO_2 film. Then, the smaller η values for the GBs t_{BD} data are associated with the faster degradation of the SiO_2 region under the GBs. Indeed, higher currents through the GBs indicate that the GBs represent less resistive HfO_2 regions and that, as a result, the voltage drop is greater across those regions of the SiO_2 film. The IL beneath GBs therefore undergoes accelerated degradation resulting in smaller t_{BD} values in these sites [Iglesias 10]. Thus, the SiO_2 IL experiences two different degradation rates determined by the morphology of the overlaying HK dielectric, which could explain the global bimodal TDDB distributions given in 4.13 and 4.15.

Therefore, it can be concluded that bimodal characteristic observed in the BD distributions collected at multiple, randomly chosen locations across the dielectric surface could be attributed to the different electrical properties of Gs and GBs in the polycrystalline HfO_2. In addition, similar temperature-independent slopes were found in the Weibull distributions of t_{BD} values collected either on G or on GB sites, as well as, similar activation energy values extracted from the t_{BD} temperature dependencies at both types of sites. However, the GB sites show overall smaller t_{BD} values (smaller η). From these results, it could be concluded that the gate stack BD is triggered by the BD of the SiO_2 layer. The smaller t_{BD} values measured on GBs can be attributed to a higher electrical stress experienced by the SiO_2 regions underlying the GB sites due to lower resistivity of the GBs, as was proposed earlier [Bersuker 07]. Therefore, the polycrystalline nature of the HK layer may strongly influence the BD properties of HfO_2-based gate stacks. (Annex I)

CHAPTER V

Nanoscale observation of Resistive Switching on HfO_2 based MIM structures

Due to the introduction of high-k dielectrics in the Complementary Metal Oxide Semiconductor (CMOS) technology for the fabrication of advanced devices, high-k materials have also found applications in the field of non-volatile data memories (NVMs). Resistive Random Access Memory (RRAM) technology, based on a reversible and repeatable change of the resistance (Resistive Switching, RS) of a metal-insulator-metal (MIM) memory cell, is one of the most promising emerging NVMs due to its simple structure, high switching speed, low operating voltage and excellent scalability. Although a large variety of binary and ternary oxides, as for example, Cr-doped $SrZrO_3$, $SrTiO_3$, NiO, TiO_2, Cu_2O and HfO_2-based devices (among others), exhibit resistive switching (RS) phenomena, the details of the complex microscopic mechanisms are rarely understood and depend strongly on the specific material combination. On the other hand, the scalability of the oxide materials for future NVMs is an essential point to take into account if the Moore´s law has to be extended over the few next decades. Since scaling is strongly linked to the question of whether the switching current is distributed homogeneously across the device area or localized to one or a few conducting filaments, special attention has to be paid to this issue. Moreover, most of the analyses of RS are performed at device level, that is, with standard characterization techniques, which only provide average information of the electrical properties over the whole gate area. Therefore, an experimental evidence (if any) of the local behavior of the RS and details of its conduction properties and switching cannot be provided by these techniques. In this chapter, the RS phenomena in MIM structures with polycrystalline HfO_2 layers as dielectric is studied at device level using standard characterization techniques and at the nanoscale using a CAFM.

5.1 Samples and experimental set-up

The samples used to investigate the RS phenomena consisted of a 10.6 nm thick Hf layer deposited by sputtering (and followed by a 600ºC annealing in O_2 ambient for 30 minutes to form a HfO_2 layer) on a Pt/Ti/SiO_2/Si substrate. After that, a 100 nm thick TiN top electrode was deposited at room temperature. Devices were patterned by lithography technique to form isolated square-shape memory cells with sizes ranging from 2x2 μm^2 to 100x100 μm^2. Figure 5.1 shows a schematic of the structure of the sample. These capacitors were analyzed at device level by using an Agilent 4156C Semiconductor Parameter Analyzer (SPA) and at the nanoscale by using CAFM related techniques. The CAFM was used to measure I-V curves when applying ramped voltage tests at a given location of the structure and topographical and current maps of a given area when applying a constant voltage during the scan. As it was already introduced in chapter I, since a standard CAFM current window is typically of three orders of magnitude (from ~pA to ~nA) and that would not be enough to measure the complete I-V characteristics, different set-ups that improve this limitation have been used. In particular an Enhanced CAFM [Blasco 05 [IV]] and a standard CAFM with the Resiscope module [Scientec] (which provide a much larger current dynamic range, from 1pA to 1mA, making possible the observation of the set/reset curves) have been used. To measure a bipolar RS, the CAFM measurements were performed in N_2 environment to avoid anodic oxidation when the electrons were injected from the tip [Lanza 10 [I]]. Since high current densities are measured during the electrical measurements and topographical and current images are obtained in contact mode, conductive doped diamond coated silicon tips have been used to improve their resistance to wearout. In addition to CAFM measurements, a morphological and structural characterization was already performed at the Peking University (China) using Transmission Electron Microscopy (TEM) and X-Ray Diffraction (XRD) to obtain information about the impact of the annealing on the morphology of the high-k dielectric.

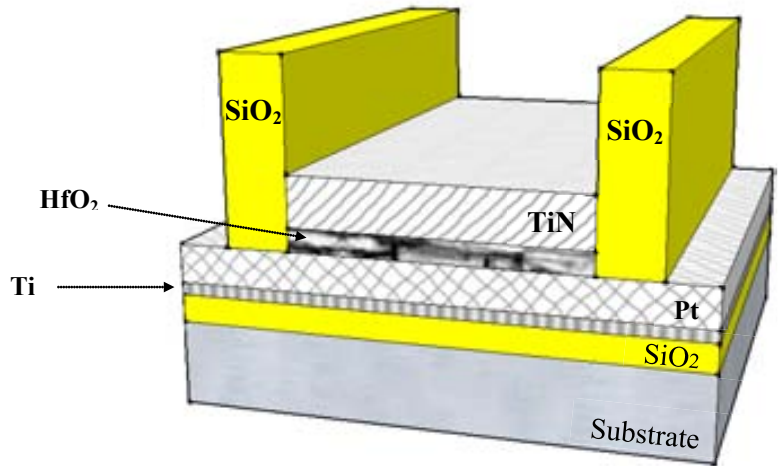

Figure 5.1: Schematic structure of the sample under study. MIM structure with a HfO_2 layer as dielectric were analysed, with areas ranging from 2x2 μm^2 to 100x100 μm^2

5.2. Morphological characterization

In this section, a morphological characterization of the sample has been performed. On one hand, TEM images were obtained to analyse the structure of the sample (figure 5.2). As it can be observed, the TiN/HfO_2/Pt/SiO_2/Si structure maintains its integrity after the 600ºC annealing and no significant Pt diffusion into the HfO_2 layer is detected. However, a thickness increases of the deposited Hf layer from 10nm (as grown Hf) to ~16nm (HfO_2 after annealing) is observed.

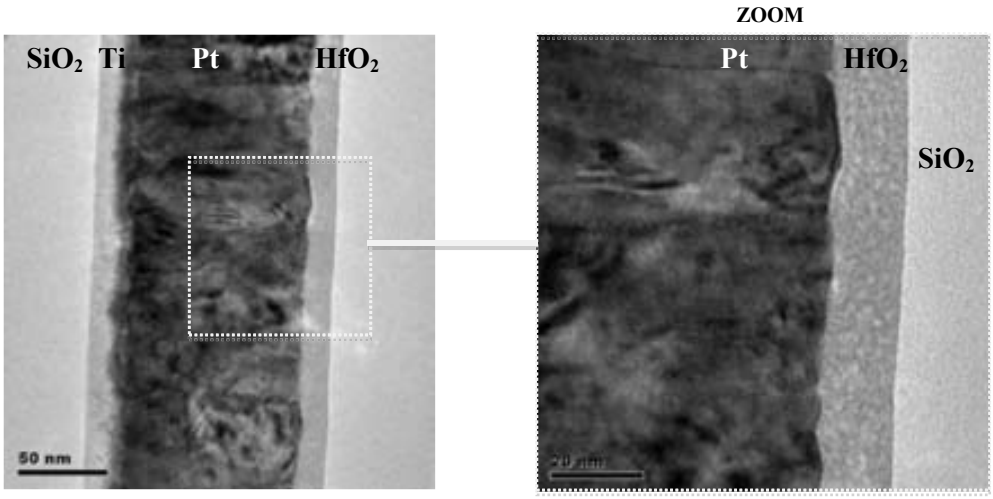

Figure 5.2: TEM images of the MIM structure under analysis. After the 600ºC annealing, a 16nm thick HfO_2 layer was measured.

XRD measurements were also performed to investigate the HfO_2 morphology. The results show that polycrystallization of the HfO_2 layer took place after the annealing. The crystallite size of the prepared HfO_2 film has been calculated from XRD line broadening using Debye–Scherrer equation:

$$d = \frac{K\lambda}{\beta}\cos\theta$$

where λ is the wavelength of the X-ray radiation (Cu–Kα=1.5406 Å), K is a constant taken as 0.89, β is full width at half maximum height (FWHM) and θ is the diffraction angle. The results indicate that the HfO_2 layer present a polycrystalline structure with an average grain size in the range of Ø ~13 nm. These results agree with the values presented in chapter IV, where the average grain size of a HfO_2 monoclinic layer was estimated to be 15 nm (see chapter IV).

In addition, a topographical (figure5.3(b)) and current (figure 5.3(a)) image of a blanket HfO_2 layer surface (without the top electrode), with identical characteristics to those used as the dielectric in the capacitors, has been measured with the CAFM to evaluate the impact of the polycrystallization on the morphology and conductivity of the HfO_2 layer . Note that, although the achieved resolution is not the best, a granular structure can be distinguished in the current image (figure 5.3(a)), which include non-conductive areas (dashed circles) surrounded by the conductive borders. The non-conductive areas could be associated with clusters of nanocrystalls meanwhile the conductive borders can

be attributed to the Grain Boundaries (GBs) of the structure, which is consistent with the results presented in chapter III and IV [Iglesias 10]. The size of the non-conductive regions, highlighted with dashed circles in figure 5.3(a), has been measured to be ~150nm. This value is really bigger (one order of magnitude higher) compared with the values obtained from XRD measurements or the results present in chapter IV. This difference could be attributed to the lower resolution observed in the image, maybe due to a tip wearing, environment conditions (water meniscus) or both. This lack of resolution also can be appreciated on the simultaneously obtained topographic image (figure 5.3b), which doesn't show any special point-to-point correlation to the current image, as in other works [Iglesias 10]. In this case, this effect could also be attributed to the lower annealing temperature used since, it is shown, that the grains in polycrystalline samples can be distinguished in topographic maps only when the annealing temperature is sufficiently high, which is not our case [Pétry 04 [I]].

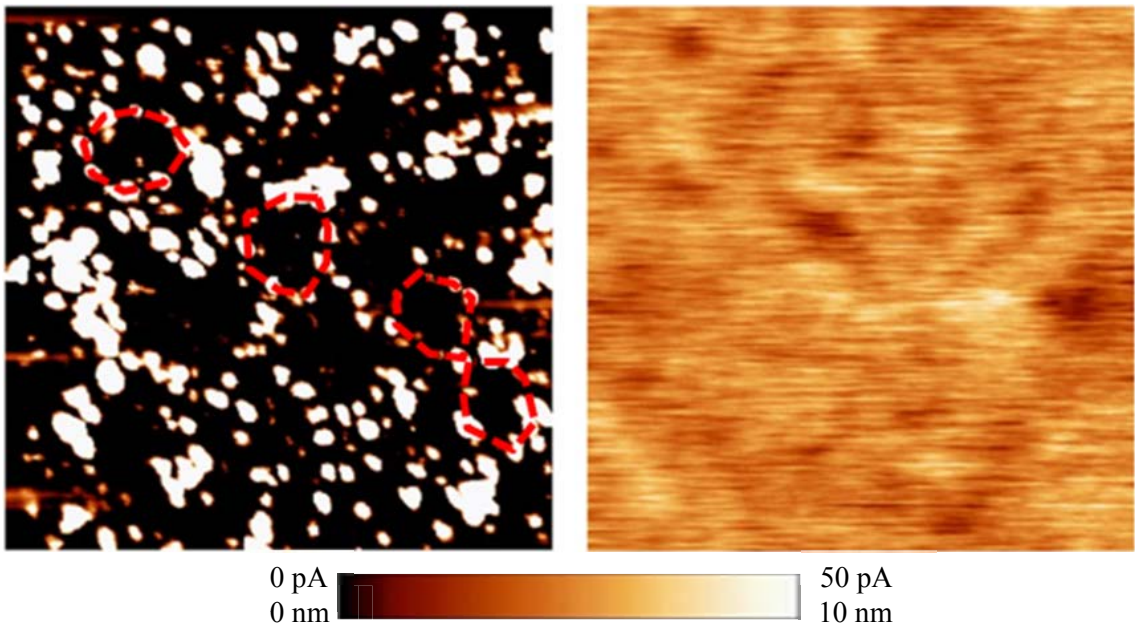

Figure 5.3: Simultaneously obtained current (a) and topographic (b) maps on the HfO_2 layer. Current map shows a polycrystalline structure, with current flowing mainly through the Grain Boundaries. Red dashed lines highlight non-conductive areas attributed to nanocrystals. Image size 1.5x1.5 μm^2

5.3 Resistive Switching on TiN/HfO_2/Pt structures.

In this section, the RS, that is, the capability of the HfO_2 to switch between two resistive states, is analyzed at the device level and at the nanoscale using the SPA and the CAFM, respectively, on TiN/HfO_2/Pt MIM structures. To study this, first, two different TiN/HfO_2/Pt MIM structures were stressed at device level and, after the forming, 5 complete set/reset cycles were measured. Figure 5.4 shows a typical RS cycle (filled squares, curves #1-#4). A common feature of most switching materials is that an initial electroforming step before stable RS can be achieved is needed. In this case, an external voltage sweep from 0 up to 20V (positive forming) was applied for the electroforming meanwhile a current limit of 100 μA was forced. During the electroforming (curve #1

of figure 4), the current gradually increases until a sudden jump up to higher currents is observed, at about 7V, indicating that BD took place (the maximum current for voltages larger than 7V corresponds to the current compliance, set by the user). After forming, the device resistance decrease by several orders of magnitude remaining in a LRS state (curve #2 of figure 4). After that, when an opposite voltage sweep (negative) is applied (curve #3 of figure 4), the device recovers partially its resistance (in our case at -2.5V) achieving a HRS state where will remain until a new ramped voltage is applied (curve #4 of figure 4). The repeatable switching between the LRS and HRS when successive bipolar ramped voltage cycles are applied (not shown) indicates the observation of the RS phenomenon.

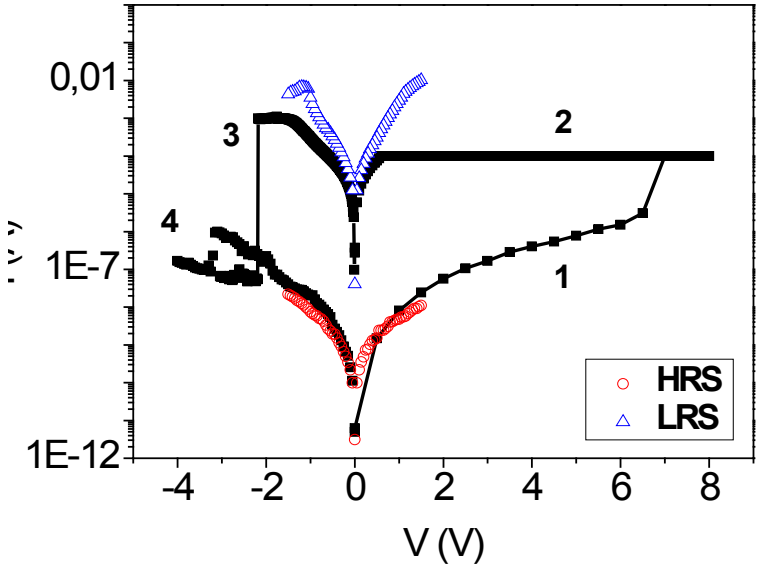

Figure 5.4: Typical complete cycle (filled squares, #1-#4) of a sequence of 5 measured at device level in a MIM structure. Triangles and circles correspond to the last I-V curve measured in two different capacitors at which, after a sequence of 5 cycles, they were kept at the LRS and HRS, respectively.

Note, however, that the current measured by the SPA not only includes the current through different filaments that can coexist in both HRS and LRS, but also the contribution of tunneling current (Fowler Nordheim and/or direct tunneling) at the rest of gate area. Therefore, the observation of RS in these analyses is indirect and there is no way to study the details of the electrical properties of the CFs (if any). To investigate the nature of this reversible conduction phenomenon at a single location, the samples have also been analyzed at the nanoscale using CAFM.

To do so, the electrical conduction of structures at the HRS and LRS have been analyzed and compared. After forming, 5 complete set/reset cycles were measured in two different TiN/HfO_2/Pt MIM structures, and after the 5 cycles, one of the structures was kept at the HRS (figure 5.4, circles) and the other at the LRS (figure 5.4, triangles). Once both structures were established in one of the states (LRS/HRS), the top electrode (TiN layer) of the capacitors was scanned with the tip of the CAFM. Although the top electrode should be removed to achieve a better resolution, in this preliminary study it remains at the stack, since a selective etching without damaging the gate oxide has not been determined yet. Obviously, when scanning the gate, resolution is not as good as

when working directly over the dielectric and, moreover, a point-to-point correlation between the topography of the HfO_2 layer and its electrical properties cannot be performed. However, a preliminary nanoscale analysis can also be performed as it was already demonstrated in [12 ESREF Kim 11].

Taking into account these considerations, figure 5.5 shows the current maps measured at the HRS (a) and LRS (b) capacitor when applying a voltage of 1.5V between the top and bottom electrodes, which simulates a read process. Note that when a current scale of 700pA is used, multiple locations drive current in both cases. However, a uniform current distribution is not observed, demonstrating that, at least in these structures, current mainly flows through CFs. When the scale is increased up to 33nA, no conductive spots are observed in the HRS structure (not shown). On the contrary, in the LRS capacitor, even at this scale (shown in the inset), one CF with larger current than the rest is observed. These results suggest that although the current in the HRS can flow through many nanosized partially formed conductive filaments of similar properties (probably related to Soft Breakdown events), the high current measured in the LRS is mainly driven by only one completely formed CF (Hard Breakdown, which is a unique event [23 Suñe 90]) with larger conductivity.

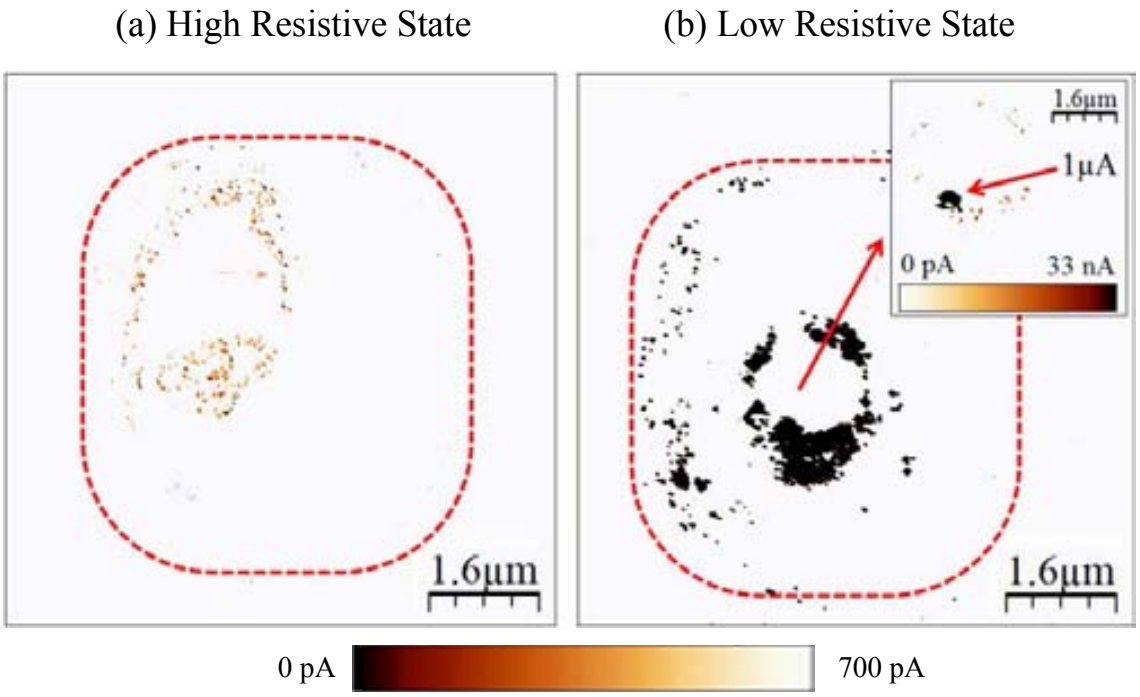

Figure 5.5: Current images of (a) HRS and (b) LRS (with different scales) when scanning the capacitor with the tip of the CAFM by applying 1.5V. The red dotted line outlines the capacitor.

That would explain, as shown in figure 5.6 (which corresponds to the resistance of the LRS and HRS of different capacitors with the same characteristics as a function of their area) and as reported in other works [11 Xu 08], why the conduction in the HRS scales with the device area and in the LRS does not. At the LRS, although many conductive

filaments could also be formed (as for the HRS), the main part of the current flows through a unique location, masking the current flowing through the rest of partially formed CF.

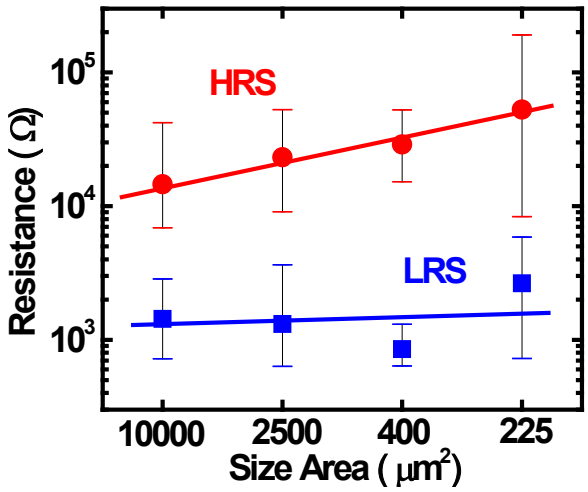

Figure 5.6: Resistance of MIM structures at the LRS and HRS as a function of the gate area. At the HRS, conduction shows area dependence.

5.4 Resistive Switching on HfO_2/Pt structures triggered with the CAFM tip.

Since the CAFM images described in figure 5.5 were obtained on the top electrode of the capacitor, information about the origin of RS cannot be extracted. Topography images do not reflect the morphological properties of the high-k dielectric, but of the TiN electrode. To determine which features in the insulator stack promote the formation of reversible CFs, blanket HfO_2 layers (without the top electrode) with identical characteristics to those used as dielectric in the capacitors has been analyzed at the nanoscale with the CAFM. In this case, since its resolution is of few nm (of the order of the width of GBs [20 Iglesias 10]) the set-up allows to analyze grains and GBs of the polycrystalline HfO_2 layer independently.

Using this set-up, ramped voltages have been applied by the CAFM tip at 24 different locations of the HfO_2 layer. The recorded I-V curves clearly show two different behaviours (see representative examples in figure 5.7): most of the curves (at 21 locations) show forming voltages above 11V, while the others (at only 3 locations) exhibit a lower BD voltage (V_{BD}~4V). After the CF formation, an additional set and reset cycle was performed to determine the electrical properties of each of the analyzed locations. Only those sites which exhibit lower forming voltages (see figure 5.7) demonstrate a typical bipolar RS (figure 5.8) similar to that in the MIM structures (figura 5.4), with comparable magnitudes of the LRS and HRS currents. Note that the set/reset cycle measured at the nanoscale with CAFM show strong similarities with those observed at device level. Therefore, these results further support the hypothesis that RS is a local phenomenon that takes place in nanosized areas. On the other hand, the sites with larger forming voltages (most of them) do not show the RS effect meaning that an irreversible breakdown is induced by the forming process. Therefore,

from these results, one can conclude that the RS observed at device level is not only controlled by a very reduced area, as demonstrated in previous section, but also RS phenomenon takes place only at those positions featuring higher current and sufficiently lower BD voltage values. Since in previous sections, especially in chapter 4, it has been clearly demonstrated that the leakiest positions correspond to GBs, it could be suggested that from the obtained results in polycrystalline HfO_2 gate dielectrics, the RS phenomenon is principally registered at these positions. Note also that the probability of probing a GB by the CAFM tip at a randomly selected location, and therefore observing the RS, is much smaller than contacting a grain, which explains a low count for the RS sites compared to the number of position where RS was not observed.

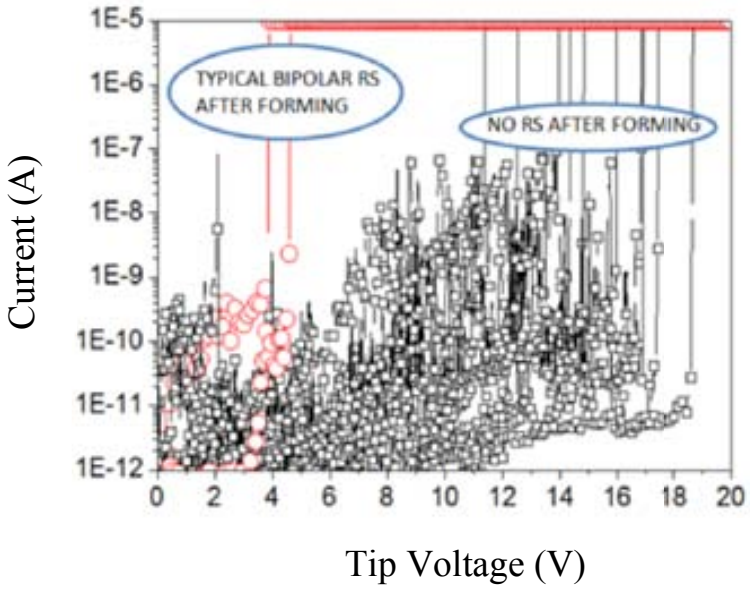

Figure 5.7: Typical examples of forming process observed on the bare HfO_2 layer with the CAFM tip after applying ramped voltages at different locations. [APL Mario: Lanza 12].

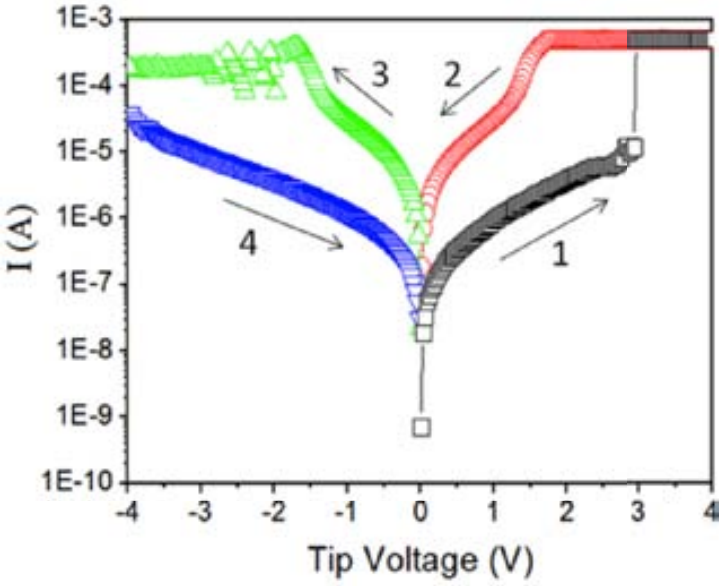

Figure 5.8: Typical RS behaviour observed on the bare HfO_2 layer with the CAFM tip on such positions where low BD voltages were registered.

As it was already mentioned, earlier reports have suggested that higher conductivity of the GBs comparing to that of the grains is related to an excess of the oxygen vacancies at the GBs, which were shown to control the trap assisted tunneling current through the dielectric [Ref 15 APL Mario: Bersuker 11]: Higher currents are associated with lower breakdown voltages along the current paths, as observed in figure 5.7. Lower forming voltages ensure smaller cross-sections of the created CFs, in part by limiting the overshoot current during the transient BD event, which is too fast to be controlled by the compliance limit set on the electrical tester [REF 16,17 APL Mario: Gilmer 11, Kalantarian 11]. The CF with a smaller radius is easier to reoxidate during the reset operation thus enabling a transition to the HRS and subsequent switching [REF 18 APL Mario: Bersuker 10].

So, to conclude, the observation of strong similarities between the device and nanoscale level (with CAFM) set/reset cycles measured after the forming and the measurement of nanosized conduction filaments on capacitors that were kept at the HRS and LRS, suggest that the RS in RRAM devices based on polycrystalline HfO_2 layers is controlled by a localized process taking place at the nano-size area of the dielectrics. The local I-V curves obtained with the CAFM point out that RS is only observed at those CF which were formed at sufficiently low voltages at the electrically leaky sites located at GBs in polycrystalline layers. This result is consistent with the previously reported high concentration of the oxygen vacancies at GBs, which are responsible for higher observed leakage currents along the GBs.On the other hand, the area dependence of the HRS conductivity has also been explained from the comparison of current maps measured on MIM structures in the LRS and HRS states. While in the LRS a single CF drives most of the current flowing through the device, in the HRS, multiple partially formed filaments could be the origin of the observed current area dependency. (Information reflected in paper D)

Summary and conclusions

The evolution of MOS (Metal Oxide Semiconductor) devices, main component of silicon-based integrated circuits, has led to a reduction of their dimensions in order to improve their performance. In the range of dimensions of the current devices, gate oxide thicknesses of ~1nm are of interest, leading to quantum phenomena, as for example an excess of gate leakage current, which increase the power consumption as well as impoverish the reliability of the device. Therefore, the physical limit imposed by the thin insulating layer of SiO_2 has forced the search for new alternatives in order to continue supplying the demanding technology market. The substitution of the traditional gate oxide (SiO_2 or SiON) by high-k dielectrics to reduce the gate leakage current, however, has introduced new issues that must be studied deeper, as for example, an increase of the variability of the MOSFET electrical properties and the apparition of new failure mechanisms. Since these phenomena occur at the nanoscale, characterization techniques with a large lateral resolution are required to investigate them in detail. In this sense, Atomic Force Microscope (AFM) related techniques, such as the C-AFM (Conductive AFM), can provide information of the electrical properties of the gate dielectrics that would be masked when studied with standard characterization techniques on fully processed devices. This thesis, enshrined in the field of microelectronics and, specifically, in the reliability and electrical characterization of MOS devices based on high-k dielectrics, has been devoted to the analysis of nanoscale morphological and electrical properties of thin HfO_2 layers with the aim to gain more insight in these new materials and related problems. Concretly, the influence of their polycrystallization on the electrical properties and breakdown (BD) of a HfO_2 based gate stack has been evaluated. The study of the Resistive Random Access Memory (ReRAM) operating principle, Resistive Switching (RS), has been also investigated in this thesis. These analyses have been performed with CAFM because of its ability to study the local electrical behaviour of dielectrics with a high spatial resolution (~10 nm).

Since grain dimensions and grain boundaries width of polycrystalline HfO_2 layers may exceed the limits of the lateral AFM resolution and such resolution strongly depends on the tip characteristics and measurement environment, first, the impact of the environment and tip characteristics on the CAFM resolution has been analysed. The first goal was to find the optimal experimental conditions to perform the CAFM analysis with the highest resolution in order to guarantee that single nanocrystals could be detected. The main results can be summarized in the following points:

- Topographical images obtained with different tips on the same sample have shown that tip radius clearly impacts on the AFM resolution. The observed grains have been found to be larger in those cases when the tip radius is bigger (for example, coated tips). This increase of the measured grain size can be due to unresolved grains as a consequence of the larger radius. Moreover, a decrease on the roughness surface value is also observed when the tip radius increases. The reduction of the roughness could be explained by considering that tips with a larger radius are not enough resolutive to reproduce drastic changes on the surface, leading, therefore, to smoother surfaces. Therefore, the results show that with the commonly used conductive CAFM tips, such as PtIr-, CoCr-, or diamond-coated Si tips, it might be difficult to achieve, in air, the resolution required to study *individual* nanocrystals and to clearly distinguish Gs and GBs in a polycrystalline HfO_2 layer.

- Topographical and electrical images performed in air and in UHV (10^{-10} mbar) have shown that environmental conditions also affect the CAFM resolution. In particular, grains and grain boundaries have been clearly distinguished with a better definition when analysing polycrystalline HfO_2 layers in UHV. Therefore, the AFM lateral resolution can be improved when working in UHV conditions.

Once the optimal experimental conditions for the analysis of polycrystalline HfO_2 layers were found, the relationship between electrical and structural characteristics of polycrystalline $HfO_2/SiO_2/Si$ structures and their reliability has been investigated by CAFM. The main results are:

- Highly conductive sites are concentrated mainly at the grain boundaries, GBs. The size of the leakage sites is comparable to the estimated width of the GBs. Therefore, these results suggest that they are completely located in the GBs, without affecting the grains of the structure.

- GBs correspond to regions with a thinner HfO_2. However, the larger conductivity observed at GBs cannot be only related to the reduction of the thickness at these sites. Higher conductivity at the GBs is also found to be related to their intrinsic electrical properties. In particular, the higher conductance could be related to the presence of some kind of defects that could favour TAT.

- The presence of defects at GBs is supported by KPFM analyses, which show an elevated concentration of positive charges at these locations. Those positive charges have been presumably associated with the segregation of positively charged oxygen vacancies near the GBs, which at high densities could form a

percolation path through the dielectric, leading to the higher conductivity observed at these sites.

- BD spots are also concentrated mainly at the GBs. However, BD propagates to larger areas. In particular, they are mainly propagated along the GB. In the transversal direction, BD propagation does not advance significantly due to the presence of the nanocrystals, which show a harder dielectric strength. Nanocrystals are only slightly affected, with currents much smaller than those measured at the GBs.

- The evolution of the electrical properties of polycrystalline $HfO_2/SiO_2/Si$ structures under an electrical stress were also investigated. Under electrical stress, GBs, which are initially more conductive, degrade faster than the grains, enlarging the electrical inhomogeneity of polycrystalline high-k layers and leading to BD events. Therefore, leaky sites at GBs are probably the precursors of the BD events.

- The Weibull distributions of t_{BD} values collected either on G or on GB sites exhibit similar temperature-independent slopes. Moreover, similar activation energy values were extracted from the t_{BD} temperature dependencies at both types of sites. From these results, it is concluded that the gate stack BD is triggered by the BD of the SiO_2 layer.

- The GB sites show not only a faster degradation, but also smaller t_{BD} values. The faster degradation of GBs and the smaller t_{BD} measured on GBs could be attributed to the fact that, since these sites are more conductive, most of the voltage applied to the dielectric stack drops across the region of the interfacial SiO_2 layer overlaid by the GBs than the SiO_2 region under the grains. This leads to greater degradation of the SiO_2 resulting in a gradual increase in the current measured at the GBs as the stress proceeds and eventually leading to the BD of the entire gate stack due to lower resistivity of the GBs.

- The BD distributions, collected at multiple and randomly chosen locations across the dielectric surface, show a bimodal characteristic that has been fitted to a model that combines the BD distributions obtained at Gs and GBs. Therefore, the bimodal BD distribution has been attributed to the different electrical properties of Gs and GBs in the polycrystalline HfO_2.

The CAFM was also used to study, at the nanoscale, the Resistive Switching phenomenon in MIM structures with polycrystalline HfO_2 films as insulator. The main results are:

- Strong similarities between the device and nanoscale RS features were observed, suggesting that the RS observed at device level is controlled by a localized process taking place at the nano-size area of the dielectric, that is, conductive filaments (CF).

- RS is only observed at those CF which were formed at sufficiently low voltages at the electrically leaky sites located at the grain boundaries, suggesting that failure mechanisms such BD could be related to the RS observed in our structures. This result is consistent with the previously reported high

concentration of the oxygen vacancies at the GBs, which are responsible for higher observed leakage currents along the GBs.

- The area dependence of the HRS conductivity has been explained from the comparison of current maps measured on different MIM structures kept in the Low Resistive State (LRS) and High Resistive State (HRS). While the high current measured in the LRS is mainly driven by only one completely formed CF, which could be related with the Hard Breakdown (HBD), the current measured in the HRS seems to flow through many nanosized partially formed CF of similar properties probably related with the Soft Breakdown (SBD). This would explain the origin of observed current area dependency in the HRS state and the absence of this in the LRS state.

Therefore, to conclude, this thesis has shown that CAFM is a very useful tool to study the electrical properties and reliability of high-k based MIS/MIM structures. The nanoscale resolution of the CAFM has allowed to investigate details of the electrical properties of gate oxides that would not be observed with standard characterization techniques. In particular, the results have shown that the polycrystallization of the HfO_2 is an important source of the nanoscale variability that affects the electrical properties of these layers. As a consequence, these variations in the local characteristics of the high-k film, caused by its crystallization, could strongly affect the electrical characteristics and reliability of HfO_2 based dielectric stacks and their corresponding devices.

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PAPERS A - D

Dielectric breakdown in polycrystalline hafnium oxide gate dielectrics investigated by conductive atomic force microscopy

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The relationship between the topographical and electrical properties of the polycrystalline HfO_2 layer has been investigated using conductive atomic force microscopy under ultrahigh vacuum conditions. Its high lateral resolution identified the grain boundaries (GBs) as a primarily conduction path through the dielectric. Electrical stress-induced breakdown sites were also found to be located at the GBs, suggesting that the polycrystalline phase of the gate dielectric may impair reliability.
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I. INTRODUCTION

In recent years, metal oxide high-*k* dielectrics have become a feasible replacement for conventional SiO_2 gate oxides in metal oxide semiconductor field effect transistors. High-*k* dielectrics not only reduce the gate leakage current but also improve the short channel effects in scaled devices.[1] However, the introduction of high-*k* dielectrics engenders a new set of reliability concerns since the mechanism of their stress-induced degradation and breakdown is still unclear. Several studies have focused on the electrical characteristics of the gate dielectric measured on fully processed metal oxide semiconductor capacitors and transistors.[1–4] Since the device dimensions (in micrometers) significantly exceed those of the characteristic structural features of the material (in nanometers), these tests can provide information on only the averaged electrical properties of the material. To gain better insight into possible mechanisms controlling high-*k* dielectric electrical performance, the electrical characteristics of the material need to be measured on a scale comparable to its structural properties, specifically its grain structure. For this, conductive atomic force microscopy (CAFM), which has demonstrated nanometer-resolved characterization of the electrical and topographical properties of SiO_2 and other insulators,[5–12] including Hf-based high-*k* dielectrics,[13] appears to be a promising technique. For example, using this technique, it was found that crystallization of the high-*k* dielectric[14] impacts its electrical homogeneity.[15] However, a direct correlation between electrical and topographical properties sometimes cannot be established[15] because the lateral resolution of the technique (when working in ambient conditions) may not be sufficient to clearly distinguish the grain boundaries. In this study, CAFM measurements were performed both in air and under ultrahigh vacuum (UHV) to determine the best experimental conditions to establish such a correlation. Based on the data obtained, the relationship between the electrical and structural characteristics of a polycrystalline HfO_2 film was analyzed.

II. EXPERIMENT

The dielectric studied consists of a HfO_2 film with a nominal thickness of 5 nm deposited by atomic layer deposition on a native 1 nm thick SiO_2 layer. The gate stack was grown on a *p*-type Si epitaxial substrate and annealed at 1000 °C to induce crystallization of the high-*k* layer. The HfO_2 thickness (5 nm) was chosen to form a layer with the crystallites as large as possible (to improve the experimental resolution) while avoiding the formation of several layers of grains (such multilayers would make the analysis of individual crystals more difficult). To avoid contaminating the HfO_2 film, a protective layer of amorphous Si was deposited on the high-*k* film after it was grown; this layer was selectively removed [using a solution of $NH_4OH:H_2O$ (de-ionized) 6:10 for 13 min at 60 °C] before the CAFM analysis. Since it has been demonstrated that, when working on air, some undetermined reaction occurs between the tip and the sample (probably related to water and/or hydrocarbons present in the stack), which can cause loss of conductivity and resolution, the time between Si removal and atomic force microscopy (AFM) measurements has been kept as short as possible (maximum of few days) to avoid any effect of the contamination deposited in the sample. Complete elimination of the Si film with no effect on the underlying high-*k* dielectric was confirmed by complementary tests, such as x-ray reflectometry measurements (not shown). X-ray diffraction analyses also identified the presence of HfO_2 crystals in the stack. Once the protective layer was removed, the sample was analyzed with an Omicron CAFM working either in air or in UHV (10^{-10} mbar) using different tips including Si tips either noncoated or coated with a layer of different conductive materials. The noncoated

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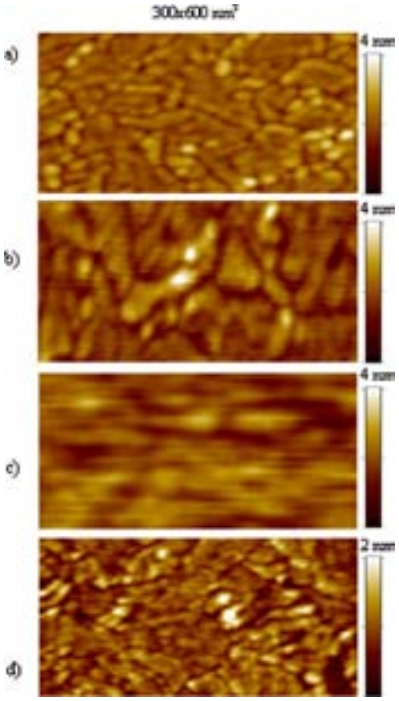

FIG. 1. (Color online) AFM topographic images (300×600 nm^2) obtained in air with (a) a Si tip, (b) a Pt/Ir-coated tip, and (c) a diamond-coated tip. (d) was obtained in UHV with a diamond-coated tip. All images were obtained without applying any voltage to the tip-sample system.

Si tips with a nominal radius of ~10 nm were provided by Veeco (NCHV model). Nanoworld Pt/Ir-coated Si tips (EFM model) had a nominal radius of ~25 nm. Diamond-coated Si tips, supplied by Nanosensors (PointProbe®Plus model), had a nominal radius of ~100 nm, although microroughness at their apex could reduce the effective contact area with the sample. Since the tip properties (especially the radius) are sensitive to the number of scans performed (due to mechanical and/or electrical wear), all the images shown in this work were measured with fresh tips.

III. RESULTS AND DISCUSSION

A. Effect of the environment and tip characteristics

To correlate the morphological and electrical properties of polycrystalline high-k dielectrics, the nanocrystals must be identified in topographical images. However, the dimensions of smaller grains, and especially the grain boundaries' width, may exceed the limits of AFM lateral resolution. Since AFM resolution strongly depends on the tip geometry and the measurement environment,[16] we first analyzed the effect of the tip characteristics on the topographical maps of the polycrystalline HfO_2 layer by comparing topographical images obtained in air using different tips (noncoated Si tips and Si tips coated with different materials). Figure 1 shows topographical images (obtained without any applied voltage to the tip-sample system) of the HfO_2 layer obtained *in air* with (a) a noncoated Si tip (radius ~ 10 nm) and (b) a Si tip coated with a Pt/Ir layer (radius ~ 25 nm). (a) was obtained in tapping mode, and (b) was obtained in contact mode. As expected, the tip radius clearly affects AFM resolution. Note that although a granular structure can be distinguished in both images, the borders between grains are wider and less defined in (b) than in (a) due to the lesser resolution obtained with the coated tip. Moreover, the grains seem to be larger in (b) than in (a), which is due to unresolved grains in (b). Therefore, the grains observed in (b) could actually correspond to the grain clusters. The lesser resolution of coated tips is also supported by the different heights of the grain boundaries (GBs) and grains (defined as the GB depth) since they are also affected by the tip radius. The GB depth has been statistically estimated in Figs. 1(a) and 1(b), showing average values of 1.6 ± 0.4 and 1 ± 0.4 nm, respectively. Note that in Fig. 1(b), the GB is not as deep, which can be explained by considering the lower resolution when using coated tips: Coated tips (i.e., tips with a larger radius) are not able to completely penetrate into the GB (with a width of a few nanometers); therefore, the difference in GB and grain height is less. Tips with larger radii, such as Co/Cr- or diamond-coated Si tips, demonstrated similar or worse resolution. As an example, Fig. 1(c) shows a topographical image obtained in air (contact mode) with a diamond-coated Si tip. Note that the granular structure is not visible. Although nanocrystals at the apex of these tips might reduce the contact area with the sample, the lower resolution can be attributed to their larger radius and to the ambient conditions (measurements in air). However, it is important to emphasize that conductive tips are required to perform CAFM measurements; these are normally Si tips coated with a metal. The results show that with the commonly used conductive CAFM tips, such as PtIr-, CoCr-, or diamond-coated Si, it might be difficult to achieve, in air, the resolution required to study *individual* nanocrystals.

To analyze the impact of the environment on the lateral resolution of the CAFM, the topographical images obtained in air [Figs. 1(a)–1(c)] were compared to topographical images obtained in UHV (at 0 V). Since more resistant tips are necessary under UHV conditions,[17] the topographical images [Fig. 1(d)] were obtained with doped diamond-coated Si tips (radius of ~100 nm) because of their greater mechanical resistance than Co/Cr- or Pt/Ir-coated tips. Note that the granular structure is again clearly observed (with a GB depth of $\sim0.8\pm0.2$ nm) even when using a tip with a larger radius; the grain sizes and grain boundary widths are similar to those in Fig. 1(a). Though different tips were used to obtain Figs. 1(c) and 1(d), a factor that could somehow affect the measurement, the remarkable differences between both figures suggest that ambient conditions have a clear effect in the resolution of the images. Therefore, to conclude, although nanocrystals can at times be observed in air,[9] the results suggest that UHV improves lateral CAFM resolution. This was reported in a previous work,[18] in which resolution diminished after several scans when working in air when compared to measurements in vacuum.

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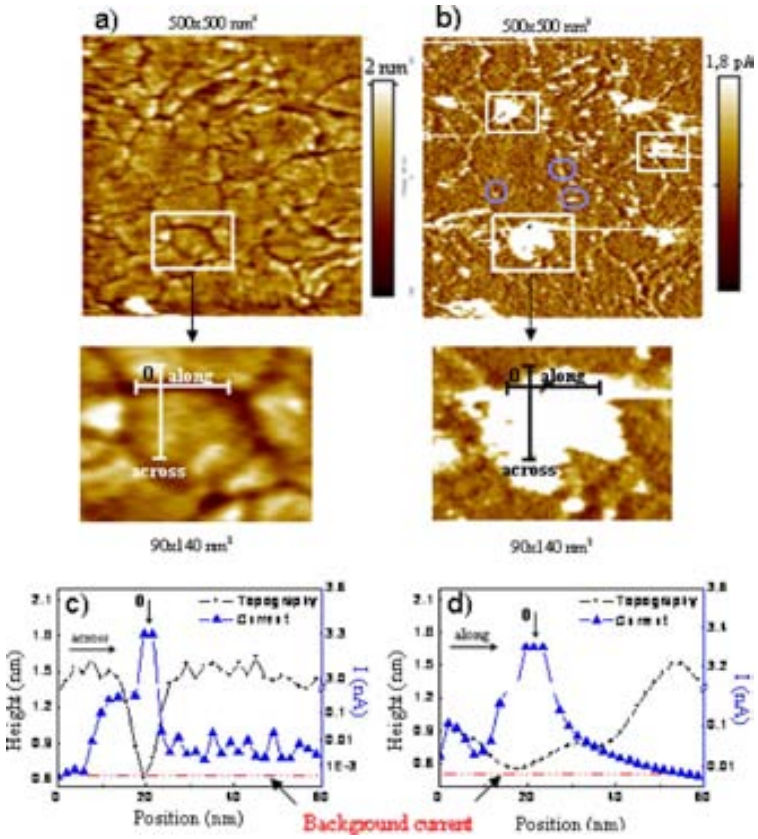

FIG. 2. (Color online) (a) Topographical and (b) current images (500×500 nm^2) obtained at -6.5 V (applied to the substrate, tip grounded) in UHV. Circles and squares represent leakage sites and BD spots, respectively. (c) and (d) correspond to topographical and current profiles obtained across and along the GB, respectively, at the site of the largest BD spot (point 0 is the position of maximum current). The background current line corresponds to the current through the area unaffected by BD.

B. Topographical and electrical correlation

Once the best experimental conditions to resolve GBs were determined, in this section we will center our attention on the main goal of the work, that is, on the effects of polycrystallization on the electrical properties of high-k stacks. The topographical and electrical properties of the polycrystalline HfO_2/SiO_2 stack were then evaluated in UHV with a diamond-coated tip. Figure 2 shows a (a) topographical and (b) current image obtained using a -6.5 V bias applied to the substrate (tip grounded and electrons injected from the substrate). In the topographical image (a), a granular structure, which was attributed to the crystallized high-k layer, is observed. Grains in the image correspond to individual (or a cluster of) randomly orientated nanocrystals, separated by GBs associated with the depressed regions. Therefore, the image in Fig. 2(a) suggests that the oxide is thinner (t_{ox}) at the grain boundaries (depression). The width of the GBs was statistically estimated from the topographical image by considering the width of the region at 75% depth counting from the level of the adjacent nanocrystals. From the analysis of $\sim$50 GBs, the average width was estimated to be $\sim$4 nm.

The current map [Fig. 2(b)] obtained on the same area exhibits a granular pattern, which overlaps with the pattern registered in the topographical image. In particular, leakage sites [e.g., those circled in Fig. 2(b)] with current values in the range of picoamperes above the background level (measured over the nanocrystals) are located along the topographical depressions associated with the GBs. The average size of the leakage sites was statistically estimated from the analysis of 20 weak spots. In particular, the regions that drive a current of 1 pA above the background level were considered. Assuming that the leakage sites are circular, a mean radius of $\sim$3 nm was estimated. Note that although this value could be underestimated due to the relatively larger radius of the tip than the GB width (and subsequent poor electrical contact with the GB), the estimated width of $\sim$3 nm is comparable to the GB width of $\sim$4 nm, as determined from the topographical images, suggesting that the leakage did not spread beyond the GBs. In addition, breakdown (BD) spots with currents in the nanoampere range were also identified. These BD events were presumably triggered by the voltage applied during the scan. The diameter of these spots was estimated to be $\sim$20 nm (the thin and long extensions observed in some BD spots are artifacts related to the dynamic especs. of the I-V converter). Note that, in this case, the BD spots are much larger than the regular leakage sites, indicating that the former spread outside the GBs into the nanocrystals. To study the area affected by the BD event in more detail, the topography and current profiles of several BD spots were analyzed [those in squares in Fig. 2(c)]. As a typical example, Figs. 2(c) and 2(d). show the topographical and current profiles of the largest BD spot in Fig. 2 (a zoom-in is shown), (c) across and (d) along the GB where it was triggered. The profiles are centered at the point that the

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greatest current was measured (point 0). Note that the nanoampere-range currents are registered only at the GB (depression in the topographical profiles), suggesting that BD is triggered at these positions. However, the BD event affects the adjacent nanocrystals since the current through them is greater than that in the unaffected areas while still lower than that through the GB area [Fig. 2(c)]. A comparison of current profiles also suggests that the BD tends to propagate along the GB since the full width at half maximum value is higher in that direction [Fig. 2(d)]. The results thus show that although BD spots are primarily triggered at the GBs (and the leakage sites observed in Fig. 2 could be precursors of the BD event), they tend to expand outside the initial leakage areas. However, since the BD spot does not expand as much into the grain body as along the GB, the grain boundaries of the crystalline structure seem to have a smaller "dielectric strength" than the nanocrystals.

IV. CONCLUSIONS

This work investigated the relationship between electrical and structural characteristics of polycrystalline HfO_2 layers. First, the optimal experimental conditions allowing distinguishing nanocrystals in the structure were determined. Topographical measurements performed with different CAFM tips under different ambient conditions showed that the grain structure can be better resolved under UHV. By correlating the topographical and current images, it was determined that the leakage current through the high-*k* dielectric stack preferentially flows through the GBs. The BD spots found to be located at the GBs propagated into the surrounding regions, preferentially along the GBs.

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Correlation between the nanoscale electrical and morphological properties of crystallized hafnium oxide-based metal oxide semiconductor structures

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The relationship between electrical and structural characteristics of polycrystalline HfO_2 films has been investigated by conductive atomic force microscopy under ultrahigh vacuum conditions. The results demonstrate that highly conductive and breakdown (BD) sites are concentrated mainly at the grain boundaries (GBs). Higher conductivity at the GBs is found to be related to their intrinsic electrical properties, while the positions of the electrical stress-induced BD sites correlate to the local thinning of the dielectric. The results indicate that variations in the local characteristics of the high-k film caused by its crystallization may have a strong impact on the electrical characteristics of high-k dielectric stacks. © *2010 American Institute of Physics*. [doi:10.1063/1.3533257]

Electrical characteristics of highly scaled devices may exhibit significant device-to-device variability,[1] which is ultimately associated with the discrete nature of charge and matter. Several variability sources, such as random dopant distribution, line edge roughness, gate oxide roughness, and granularity of the poly-Si gate (either during deposition or fabrication), have been identified.[2] In particular, as modeling results have shown, these may lead to variations in threshold voltage and mobility values.[2] Crystallization of the high-k gate dielectrics may also be expected to affect the electrical properties of scaled devices, leading—for instance—to device-to-device variations in the gate leakage current that influences device reliability. However, since standard characterization techniques can provide only averaged information about the electrical properties of devices, addressing the origin of the variability in the nanoscale requires advanced characterization methods with a high lateral resolution. In this respect, scanning probe microscopes have been shown to be powerful tools for characterizing the electrical properties of dielectrics.[3–7] Conductive atomic force microscopy (CAFM) has been widely used to evaluate the electrical conduction of polycrystalline high-k dielectrics. Whereas some studies have suggested that conduction through the polycrystalline films occurs primarily through the bulk of the grains,[8,9] others have demonstrated that the leakage current flows preferentially through the grain boundaries (GBs),[3,7,10,11] which agrees with the results of *ab initio* calculations.[12] Besides generally expected differences associated with the intrinsic properties of the studied materials, such a discrepancy could be caused by the limits of the CAFM lateral resolution, which are close to the characteristic GB width. As a consequence, topography can be directly correlated with current maps only under carefully selected measurement conditions. In this work, CAFM used under ultrahigh vacuum (UHV) conditions, which improve lateral resolution, has been employed to evaluate, at the nanoscale, the impact of crystallization of the high-k material in $HfO_2/SiO_2/Si$ structures on the morphological and electrical properties (and their relation, if any) of the stack.

Gate stack dielectrics consisting of a 5 nm thick atomic layer deposition HfO_2 film and a 1 nm SiO_2 interface layer grown on a Si epitaxial P-substrate were investigated. The gate stack was annealed at 1000 °C, which induced the crystallization of the high-k layer. Following earlier suggestions[13] to achieve the high lateral resolution required to correlate the morphological and electrical properties of the nanocrystalline dielectric, CAFM measurements were performed in UHV ($\sim 10^{-10}$ mbar). Current and topography maps were obtained in contact mode by applying a constant voltage to the tip (substrate grounded). Since under UHV conditions higher resistant tips are necessary to improve the lateral resolution,[13] although their radius is larger than that of other conductive tips, diamond-coated silicon tips were used for the conductivity measurements.[14]

The morphology of the high-k layer was investigated first. Figure 1(a) presents a topographical image showing a surface (1×1 μm^2) with a granular structure. A statistical analysis of the grains shows that their average size is ~ 15 nm,[15] information that is compatible with the grain size obtained from transmission electron microscope images. This granular structure has been attributed to the crystallization of the high-k layer after annealing;[7] grains in the image correspond to individual (or a cluster of) randomly oriented nanocrystals separated by GBs (depressions in the image). Note that direct information about the oxide thickness t_{ox} cannot be obtained from this image because t_{ox} depends not only on the morphology of the scanned top (dielectric/gate) interface [Fig. 1(a)], but also on that of the dielectric/substrate interface, and this information is not independently available in this experiment. However, it is reasonable to assume a similar grain morphology at both interfaces. Therefore, Fig. 1 suggests that t_{ox} is less at the grain boundaries (depression). The width of the GBs has been statistically estimated to be ~ 4 nm. This value is slightly higher than what is obtained from *ab initio* calculations[12] (<2 nm),

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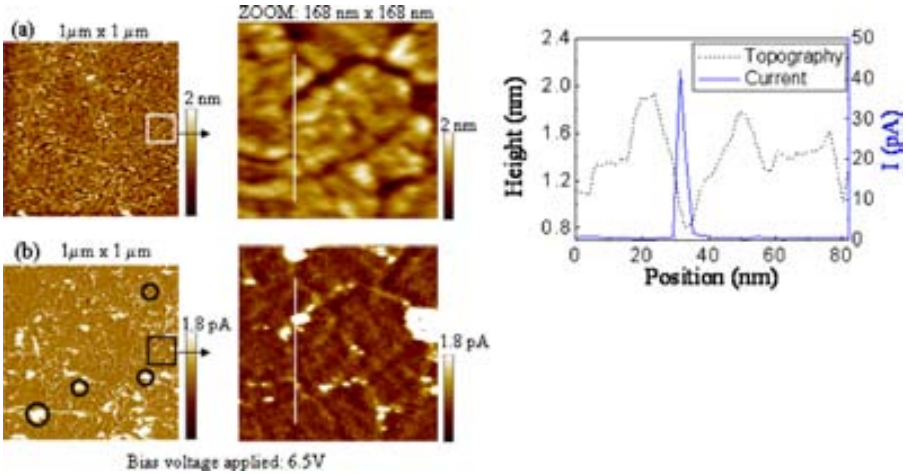

FIG. 1. (Color online) (a) Topographical and (b) current images obtained at 6.5 V of the $HfO_2/SiO_2/Si$ structure (area of 1×1 μm^2). A granular pattern is associated with the presence of nanocrystals. A zoom-in of both images is also shown. Circles in the current image correspond to the BD sites. (c) Topographical (dashed line) and current (continuous line) profiles obtained along the white lines in the zoom-in images show higher leakage current at the topographical depressions associated with the grain boundaries.

probably because we are close to the resolution limits of this technique.

The effect of the high-k crystallization on the electrical properties of the gate stack was investigated based on the image of the leakage current through the film [Fig. 1(b)] measured at 6.5 V at the same surface region as in Fig. 1(a). Note that in Fig. 1(b) a granular pattern overlaps with that of the topographical image (an enlargement of both images is also shown); leakage sites with current values on the order of picoamperes above the background level, which was measured over the nanocrystals, are mainly located at GBs.[16,17] For example, Fig. 1(c) shows topographical (dashed line) and current (continuous line) profiles across the white line plotted in Figs. 1(a) and 1(b) (zooms). Note that the positions with higher currents (leakage sites) are located along the topographical depressions associated with GBs. This qualitative observation has been verified statistically. Figure 2 shows the Z-axis relative position (Z_{rel}) of more than 70 leakage spots (exhibiting a current greater than 0.5 pA) with respect to the Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level (dashed line) versus their maximum current. Note that most of the leakage sites are below this reference level (i.e., in the topographical depressions and, therefore, in the GBs). The average size of the leakage sites, those with current values of picoamperes, was also statistically estimated to be ~3 nm, which is comparable to the width of the GBs, consistent with the suggestion that they are confined within the GB region. In addition to these leakage sites, breakdown (BD) sites [in circles in Fig. 1(b)], with currents greater than nanoamperes, can also be identified. These BD events were probably triggered by the constant voltage applied during the scan to obtain the topographical and the current image. Note that the BD spots are much larger (~20 nm) than the leakage spots, suggesting that BD may affect a larger area surrounding the GB. However, within the BD spot, the current measured over the GB region (~nA) is much greater than the current through the adjacent nanocrystals (~pA). Therefore, the results show a clear correlation between the oxide morphology (determined by the crystallization of the high-k layer) and the electrical properties of the gate dielectric: conductivity through the dielectric film is higher along the GBs, and the leakage and BD sites are mostly located near the GBs.

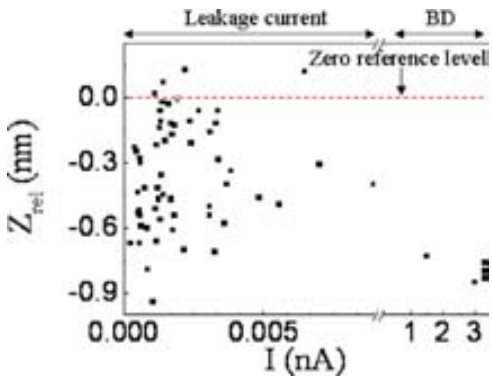

FIG. 2. (Color online) Z-axis relative position (Z_{rel}) of more than 70 leakage spots (with currents greater than 0.5 pA) vs their maximum current. Z_{rel} of a leakage site is defined as the Z-position with respect to Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level (dashed line). Note that most are located in topographical depressions (below the reference level), that is, at the GBs.

The localization of leakage and BD spots around the GBs could be related to (1) a decrease in the dielectric thickness, as observed on the topographical images, or (2) a higher density of traps at the GB, which could support the trap-assisted tunneling (TAT) current. To determine which factor dominates (if any), we investigated whether there is any correlation between the current through the leakage or BD sites and their Z_{rel}, which reflects the dielectric thickness at a given location: lower Z_{rel} values correspond to thinner dielectrics. Note that, in Fig. 2, two groups of sites can be distinguished. The first corresponds to the sites with the currents in the picoampere-range, where there is no apparent correlation between the leakage currents and dielectric thicknesses. This suggests that the conductivity of the leakage sites is primarily determined by the electrical properties of the GBs, which could be related to the O-vacancies accumulated at the GBs, as pointed out in other works,[12,18] rather than the dielectric thickness across the GB area. The second group in Fig. 2 includes the sites with the current values in the nanoampere-range (BD spots). These sites exhibit lower Z_{rel}'s, which correspond to the locations with smaller dielectric thicknesses. These results indicate that BD in the $HfO_2/SiO_2/Si$ stack is assisted by the higher electric field across the stack. However, the exact mechanism of the BD remains unclear. One of the possible scenarios is that a locally thinner high-k film results in a larger applied voltage

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drop across the underlying SiO_2 film, causing its BD and, subsequently, overall stack BD, at this location.[19] Further studies of the HfO_2/metal stacks will help address the role of the electric field in the BD process.

In conclusion, the results show that crystallization of the HfO_2 layer is an important source of the nanoscale variability that affects the electrical properties of the material. As follows from the topography maps, the GBs correspond to the regions of thinner dielectrics. The accompanied current maps demonstrate that the leakage (in the picoampere-range) and BD (in the nanoampere-range) sites are concentrated mostly near the GBs. While the size of the leakage sites is comparable to the width of the GBs, the BD sites seem to encompass much larger areas reaching into the adjacent nanocrystals, although the conductivity across the BD area is still much higher over the GB. The analysis shows that the electrical properties of the GBs (e.g., the presence of the TAT defects) are responsible for their higher conductance than that of the grains. The BD sites were found to be induced primarily at the strongly depressed GB sites, suggesting a significant contribution from the electric field to the overall BD of the multilayer dielectric stack. Further work is needed to clarify the role of the dielectric thickness in the BD mechanism.

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Degradation of polycrystalline HfO_2-based gate dielectrics under nanoscale electrical stress

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The evolution of the electrical properties of $HfO_2/SiO_2/Si$ dielectric stacks under electrical stress has been investigated using atomic force microscope-based techniques. The current through the grain boundaries (GBs), which is found to be higher than thorough the grains, is correlated to a higher density of positively charged defects at the GBs. Electrical stress produces different degradation kinetics in the grains and GBs, with a much shorter time to breakdown in the latter, indicating that GBs facilitate dielectric breakdown in high-k gate stacks. © *2011 American Institute of Physics*. [doi:10.1063/1.3637633]

Intrinsic process variability and aging mechanisms can strongly affect the performance and reliability of MOS devices. The polycrystallization of high-k-based gate dielectrics, which can occur even during relatively low temperature device fabrication steps (e.g., atomic layer deposition, forming gas anneal),[1] has been identified as one of the device-to-device variability sources. Conductive atomic force microscope (CAFM) experiments, which may address nanoscale topographical and electrical properties of dielectric stacks,[2–5] reveal significantly higher leakage currents through the grain boundaries (GBs) than through nanocrystal (NC) grains.[3,6] Theoretical models[7] suggest that the current through the GBs could be related to a large concentration of oxygen vacancies at the GBs, which might effectively act as conductive paths through the dielectric film.[8] However, the relative role of the vacancies vs. topological factors (e.g., the dielectric thickness at the GB region) as well as the evolution of GB electrical properties under electrical stress remains unexplored. In this work, a CAFM technique has been applied to investigate conduction characteristics of the GBs in polycrystalline HfO_2 gate dielectrics. Kelvin probe force microscope (KPFM) measurements were used to assess the charge state of defects in these structures.

The dielectric stack under investigation consists of a 5 nm atomic layer deposited (ALD) HfO_2 film (annealed at 1000 °C to induce polycrystallization) and a ~1 nm SiO_2 interfacial layer grown on a Si substrate. Gate stack properties were investigated using CAFM (air conditions and contact mode). Current and topography maps were measured by applying voltage between the tip and the substrate, and current-voltage (*I-V*) data were collected in a ramped voltage mode at different oxide locations (GBs and grains). Some *I-V* characteristics were also measured with a modified CAFM approach to provide a larger current dynamic range (enhanced-CAFM (Ref. 9)). KPFM (air conditions) was employed to obtain topography and the probe tip-sample contact potential difference (CPD) map, which is proportional to the amount of charge trapped in the dielectric at the probe tip position.[10]

Topographical (a) and CPD (b) images obtained with the KPFM on a fresh (before electrical stress) gate stack are shown in Fig. 1. The map of the topographical depressions associated with the GBs (Ref. 3) and higher CPD signals overlap. A higher CPD signal can be interpreted as downward band bending,[11,12] which indicates a larger concentration of positive charges at a given location. Note that the concentration of positive charges (based on the CPD signal) at the GBs does not depend on the magnitude of the surface depression at the GB, as can be seen in Fig. 1(c). Therefore, GB electrical properties are not caused by the thinner dielectric that is characteristic of the GB region. Fig. 2 shows three consecutive current maps obtained with CAFM on the same area at 4.2 V. The images again exhibit a clear granular structure (dashed lines), related to the polycrystallization of the high-k dielectric, with leaky sites (brighter areas) concentrated around the GBs.[3] The width of the GBs (Fig. 2(a), fresh oxide) was measured to be ~15 nm, which is wider than simulation-based estimations, <2 nm,[8] probably due to the limited CAFM resolution in air, Ø ~ 10 nm.[13] This could also explain why the grains are larger (Ø ~ 100 nm in Fig. 2) than the size obtained by transmission electron microscopy (TEM) experiments (~15 nm); the grains shown in Fig. 2 could correspond to only a subset of larger grains out of all grains in the sample. However, the limited resolution does not impede the ability of CAFM to clearly distinguish the most conductive GBs. Fig. 2 also shows larger (Ø ~ 50 nm) leaky sites. These sites are the breakdown (BD) spots (indicated by arrows) that are centered at the GBs and laterally propagate into the surrounding grains as was discussed in Ref. 14. The evolution of the leakage current with

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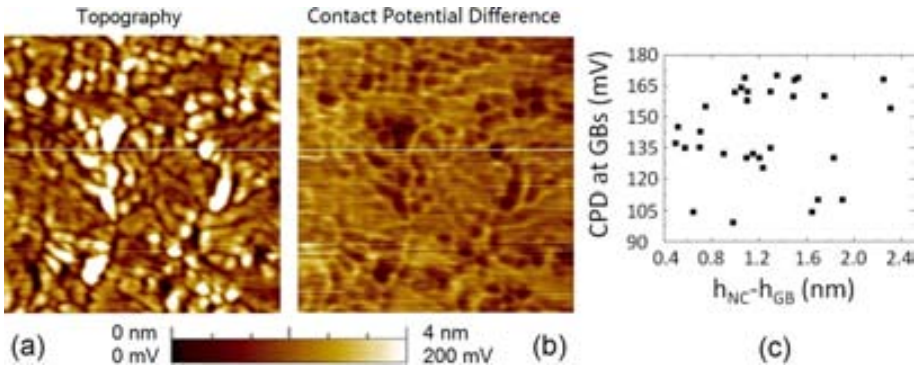

FIG. 1. (Color online) Topographical (a) and CPD (b) 1 $\mu m \times 1$ μm images. Dark lines in (a) and brighter lines in (b) correspond to GBs and higher CPD, respectively. (c) Statistical analysis of the CPD signal showing the potential on the GB sites (V_{GB}) vs. the depth of these sites with respect to the surface of the adjacent grains ($h_{NC} - h_{GB}$). Absence of a correlation between the CPD signal and magnitude of the GB recess indicates that the CPD profile is not caused by the surface topography.

subsequent scans over the same area is equivalent to that caused by electrical stress of different durations. The conductivity of the leakiest spots is observed to gradually increase under subsequent CAFM scans of the dielectric surface; in other words, under continuous stress, the GBs become more conductive. These qualitative results have been further verified by analyzing the evolution of the maximum current through different GBs as the stress proceeds. As an example, Fig. 2 shows that the maximum current through the GB crossing the A-B line for scans 1, 2, and 3 is 2.1 pA, 2.4 pA, and 4.0 pA, respectively. On the other hand, the magnitude of the background current in Fig. 2 (grains, dark areas) seems to be very stable under electrical stress

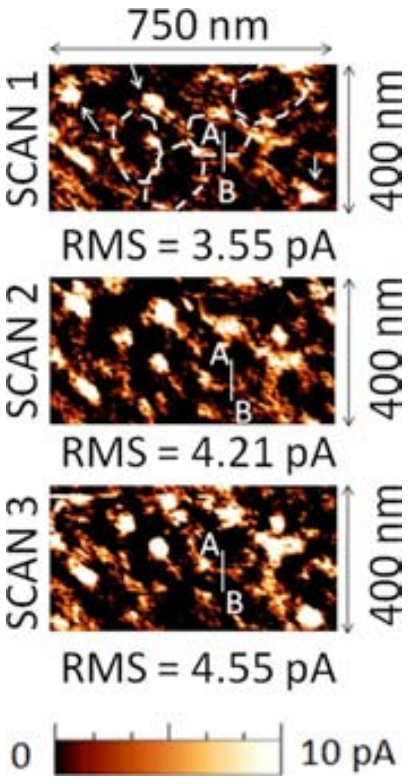

FIG. 2. (Color online) Changes of the current through the HfO_2 polycrystalline layer (with the grains clearly distinguishable) obtained by three consecutive current scans of the same area (750 nm $\times$ 400 nm). The current through the GBs (outlined by the dashed lines) increases with each subsequent scan, i.e., with longer stress time. In particular, the maximum values of the current measured along the A-B line during the scans 1, 2, and 3 are 2.1 pA, 2.4 pA, and 4.0 pA, respectively. Arrows indicates BD spots, which propagate into the surrounding grains.

(0.5 pA for all images), and no new conductive spots were generated. As a result, the overall inhomogeneity of the electrical conduction through the gate stack increases with stress time, which can also be quantitatively observed from the current dispersion magnitudes after different scans. Hence, the gate stack around the grain boundary regions becomes more conductive than the grain regions under the stress.

A comparative analysis of conduction characteristics of the GBs and grains used *I-V* curves measured on fresh and electrically stressed sites. Figure 3(a) shows typical sets of four *I-V* curves subsequently measured on the NCs (filled symbols) and GBs (open symbols) regions. By comparing the first measurements on the fresh locations (NC_IV1 and GB_IV1), it appears that the grains are less conductive than the GBs, in agreement with Ref. 15. Qualitatively different *I-V* dependencies measured on the GB and grain sites indicate that conduction through these structural features might be governed by different mechanisms. For the GBs, a dielectric BD was triggered by the first *I-V* sweep (Fig. 3(a), see differences between GB_IV1 and GB_IV2). On the contrary, when bias is applied to the grains (Fig. 3(a), NC_IV1-NC_IV4), the *I-V* curves progressively shift to lower voltages (stress-induced leakage current[15]) and BD is not triggered until several *I-V* sweeps have been applied. However, when BD is reached, it seems stronger than on the GBs: NC_IV4 exhibits an ohmic characteristic indicating its metallic nature.[16]

To further analyze electrical conduction at these locations, the *I-V* curves were measured with the enhanced-CAFM (having a larger dynamic range) on both GBs and grains (Fig. 3(b)). Again, the fresh *I-V* curves show greater currents at the GB locations (with two conduction regimes,

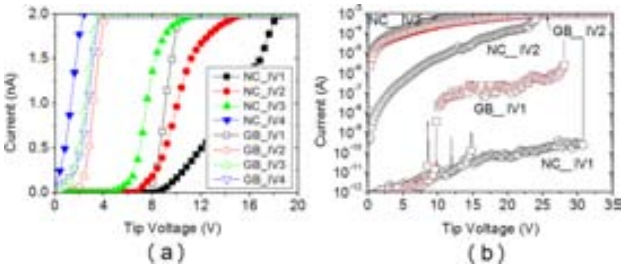

FIG. 3. (Color online) A typical example of the evolution of the current through the grain (NC IV) and GB (GB IV) during the sequential CAFM (a) and ECAFM (b) *I-V* measurements on the same spot. The maximum currents, which can be measured by CAFM and ECAFM, are 2 nA and 1 mA in (a) and (b), respectively. The first *I-V* curves (IV1) were taken on a fresh site.

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similar to those observed in other HfO_2-based stacks[17,18]), at which the BD generally occurs at lower voltages. For grains, the initial current is, as a rule, lower, and the pattern of the two conduction regimes is not seen. Moreover, the BD is triggered only after several *I-V* sweeps, indicating greater grain robustness to electrical stress.[19] Higher initial currents at the GBs could be related to the higher concentration of positive charges there (Fig. 1(b)), likely associated with the segregation of positively charged oxygen vacancies at the GBs.[8] This conclusion is consistent with earlier reported simulations of the trap-assisted tunneling current through these defects.[7] Since the GBs in the HfO_2 film are more conductive, more of the voltage applied to the dielectric stack drops across the region of the interfacial SiO_2 layer overlaid by the GBs than the SiO_2 region under the grains. This leads to greater degradation of the former,[20] resulting in a gradual increase in the current measured at the GBs as the stress proceeds and eventual BD of the entire gate stack.

In conclusion, analysis of the electrical properties of GBs and crystal grains in $Si/SiO_2/HfO_2$ stacks before and after electrical stress demonstrates that the GBs are more conductive than the bulk of the grains. This higher electrical conductivity is caused by a different conduction mechanism through the GBs rather than the thinner dielectric regions associated with the GBs. This conclusion is supported by the observation of an elevated concentration of positive charges at GB locations, presumably due to the segregation of positively charged oxygen vacancies near the GBs, which were shown to form a conductive path through the HfO_2 dielectric.[8] Under electrical stress, the GBs degrade faster than the grains, which may be attributed to the degradation of the underlying SiO_2 interfacial layer, eventually leading to the dielectric breakdown of the entire stack.

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Nanoscale observations of resistive switching high and low conductivity states on TiN/HfO_2/Pt structures

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ABSTRACT

Resistive Switching (RS) phenomenon in Metal–Insulator–Metal (MIM) structures with polycrystalline HfO_2 layers as dielectric has been studied at the nanoscale using Conductive Atomic Force Microscope (CAFM). The CAFM measurements reveal that (i) the conductive filaments (CFs) created at very small areas are the origin of the RS phenomenon observed at device level and (ii) RS conductive filaments are primarily formed at the grain boundaries, which exhibit especially low breakdown voltage. CAFM images obtained on MIM structures at the Low and High Resistive states also show that, although the current in the Low Resistive State is mainly driven by a completely formed single CF, the cell area dependence of the conductivity in the High Resistive State could be explained by considering the presence of multiple partially formed CFs.

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1. Introduction

The introduction of high-k dielectrics (materials with a high permittivity constant) in the Complementary Metal Oxide Semiconductor (CMOS) technology enables fabrication of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) with the gate stacks of low Equivalent Oxide Thickness (EOT) required for advanced devices. High-k materials have also found applications in the Resistive Random Access Memory (RRAM) technology, which is considered to be very promising for a variety of information storage applications due to its high switching speed, low operating power and excellent scalability [1–4]. The RRAM principle of operation is a reversible and repeatable change of the resistance (known as Resistive Switching (RS) of a dielectric in a MIM memory cell [5]. Although different high-k materials such as PCMO, Cr-doped $SrZrO_3$, $SrTiO_3$, NiO, TiO_2, and Cu_2O (among others) have been suggested as suitable dielectric in the MIM structures [6], the HfO_2-based devices are considered to be one of the front runners.

To improve performance of the HfO_2-based devices, it is essential to understand the RS mechanism. Recent studies have shown that the RS observed in a wide class of materials [7], as well as in HfO2-based dielectrics [8], can be described by employing a concept of a conductive filament (CF), which can be formed/disrupted in the insulator stack depending on the applied voltage [9]. This characteristic shows strong similarities with the well-known current limited reversible Dielectric Breakdown (BD) [10]. Therefore, an accurate analysis on the formation and characteristics of the CF can also be useful for failure analysis field. On the other hand, the I_{HRS} (High Resistive State current) dependency on the device area observed under certain conditions [11] suggest that the High Resistive State (HRS) might be related to the conduction through multiple filaments. Note that the above mentioned studies have been performed at the device structures which provide electrical characteristics averaged over the entire gate area and, therefore, are not sensitive to the RS properties controlled by localized material features [12]. To clarify the origin of the conductance, one may apply a CAFM (Conductive Atomic Force Microscope) technique capable of the nanometer scale resolution. The conductive tip of a CAFM allows obtaining simultaneously topographic and electrical information of the sample under analysis with a lateral resolution of about 10 nm. This technique has already been extensively used to investigate the electrical properties and reliability of SiO_2 and high-k dielectrics [13–16]. In this work, RS phenomenon on MIM structures with HfO_2 layers as insulator is studied using both device structures and at a nanoscale level with CAFM. The large resolution of the CAFM allows for studying the electrical properties of isolated conductive filaments and the locations where RS is observed.

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2. Experimental

The samples consisted of a 10.6 nm thick Hf layer deposited by sputtering (and followed by a 600 °C annealing in O_2 ambient for 30 min to form a HfO_2 layer) on a Pt/Ti/SiO_2/Si substrate. After that a 100 nm thick TiN top electrode was deposited at room temperature. Devices were patterned by lithography technique to form isolated square-shape memory cells with sizes ranging from $2 \times 2\ \mu m^2$ to $100 \times 100\ \mu m^2$. These capacitors were analyzed at device level by using an Agilent 4156C Semiconductor Parameter Analyzer (SPA) and at the nanoscale by using CAFM related techniques. The CAFM allows to measure *I–V* curves when applying ramped voltage test at a given location of the structure, and topographical and current maps of a given area when applying a constant voltage during the scan. Note that a standard CAFM current window is typically of three orders of magnitude (from ~pA to ~nA) and that would not be enough to measure the complete *I–V* characteristics. To solve this inconvenient, in this work different set-ups that improve this limitation have been used. In particular an Enhanced CAFM [17] and a standard CAFM with the Resiscope module [18] (which provide a much larger current dynamic range, from 1 pA to 1 mA, making possible the observation of the set/reset curves) have been used. To enable a bipolar RS, the CAFM measurements were performed in N_2 environment to avoid anodic oxidation when the electrons were injected from the tip [19]. Since high current densities are measured during the electrical measurements and topographical and current images are obtained in contact mode, conductive doped (Boron 6000–8000 ppms) diamond coated silicon tips have been used to improve their resistance to wearout. In addition morpholical and structural characterizations were performed using Transmission Electron Microscopy (TEM) and X-ray Diffraction (XRD). TEM sample was prepared by mechanically thinning followed by ion polishing for final thinning of the sample. Ar + bombardment at 5 keV with an incident angle of 5° was used for ion polishing.

3. Results

3.1. Morphological analysis

In this section, a morphological analysis of the sample has been performed. Fig. 1 corresponds to a cross section TEM image of the structure under analysis. As it can be observed, the TiN/HfO_2/Pt/SiO_2/Si structure maintains its integrity after the 600 °C annealing and no significant Pt diffusion into the HfO_2 layer is detected. However, a thickness increase of the deposited Hf layer from 10 nm (as grown Hf) to ~16 nm (HfO_2 after annealing) is observed. On the other hand, to corroborate that the polycrystallization of the HfO_2 layer (an effect that enhances RS) has been successfully induced during the annealing process, the morphology of the Hafnium Dioxide film has been analyzed from XRD measurements. The crystallite size of the prepared HfO2 film was calculated from XRD line broadening using Debye–Scherrer equation, $d = K\lambda/\beta \cos\theta$, where λ is the wavelength of the X-ray radiation (Cu Kα = 1.5406 Å), K is a constant taken as 0.89, β is full width at half maximum height (FWHM) and θ is the diffraction angle. The results (not shown) indicate that the HfO_2 layer is polycrystalline with grain sizes in the range of Ø ~ 130 nm. A topographical and current image of the HfO_2 surface has been measured with the CAFM to evaluate the impact of the polycrystallization on the morphology and conductivity of the HfO_2 layer (Fig. 2). Note that a granular structure can be observed in the current image (Fig. 2a), which include non-conductive areas (~150 nm, dashed circles) surrounded by the conductive borders. Clusters of nanocrystalls that cover larger areas have also been detected. Interestingly, the size of the non-conductive regions highlighted in Fig. 2a (Ø ~ 150 nm, dashed circles) are in the range of the grain area measured with XRD (Ø ~ 130 nm, data not shown), suggesting that the conductive borders can be attributed to the Grain Boundaries (GBs) of the structure, consistent with the earlier reports [20]. However, the simultaneously obtained topographic image (Fig. 2b) does not show any special point-to-point correlation to the current image, as in other works [20]. This behavior can be explained taking into account that the impact of the polycrystallization on the HfO_2 morphology depends on the annealing temperature [21]. Around the crystallization temperature, the sample does not show any significant change of its topography (although changes in the electrical properties cannot be ruled out) and, therefore, topographic–current correlation [22] is not visible, as in our case. Significant surface changes only happen at very high temperatures that which cannot be endured by the HfO_2 layer, leading to morphological formation of grain boundaries [20,22] (between 900 and 1050 °C depending on the film).

3.2. Resistive switching on TiN/HfO_2/Pt structures

In this section, the RS phenomenon on TiN/HfO_2/Pt will be analyzed at the device level and at the nanoscale using the SPA and the CAFM, respectively. First, we stressed two different TiN/HfO_2/Pt MIM structures at the device level and, after the forming, 5 complete set/reset cycles were measured. Fig. 3, squares, shows a typical forming *I–V* curve (#1) and the *I–V* curves measured during a complete set/reset cycle (#2–#4). After the five cycles, one of the structures was kept at the HRS (Fig. 3, circles) and the other at

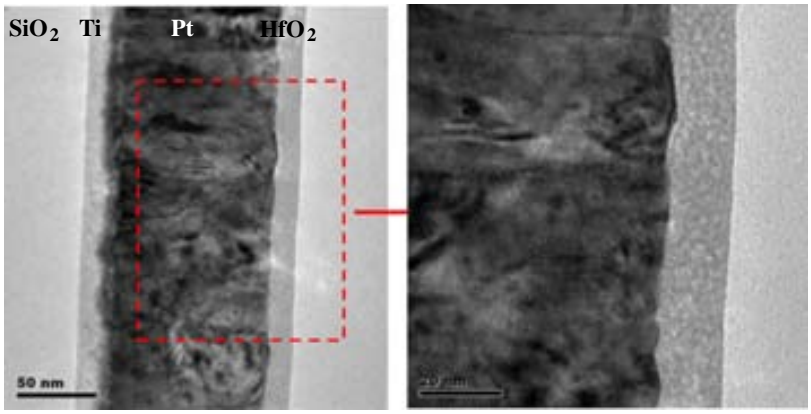

Fig. 1. TEM images of the MIM structure under analysis. After the 600 °C annealing, a 16 nm thick HfO_2 layer was measured.

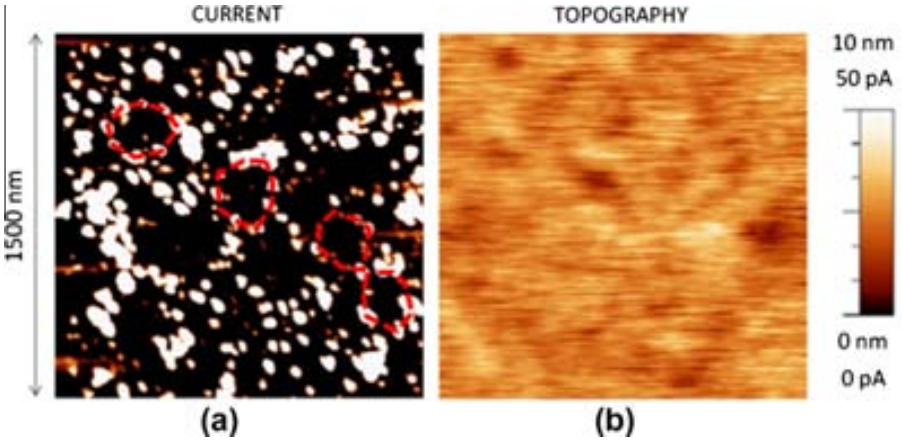

Fig. 2. Simultaneously obtained current (a) and topographic (b) maps on the HfO_2 layer. Current map shows a polycrystalline structure, with current flowing mainly through the Grain Boundaries. Red dashed line highlights nanocrystals with(For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.).

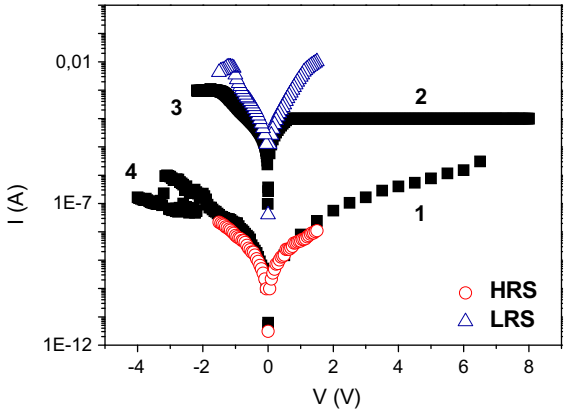

Fig. 3. Typical complete cycle (squares, #1–#4) of a sequence of 5 measured in MIM structures at device level. Triangles and circles correspond to the last *I–V* curve measured in the HRS and LRS capacitor, respectively.

the LRS (Fig. 3, triangles). Finally, the top electrode (TiN layer) of both structures was scanned with the tip of the CAFM [12]. Fig. 4 shows the current maps measured at the HRS (a) and LRS (b) capacitor when applying a voltage of 1.5 V between the top and bottom electrodes, which simulates a read process. Note that when a current scale of 700 pA is used, multiple locations drive current in both cases. However, when the scale is increased up to 33 nA, no conductive spots are observed in the HRS structure (not shown). On the contrary, in the LRS capacitor, even at this scale (shown in the inset), one CF with larger current than the rest is observed. These results suggest that although the current in the HRS can flow through many nanosized partially formed conductive filaments of similar properties (probably related to Soft Breakdown events), the high current measured in the LRS is mainly driven by only one completely formed CF (Hard Breakdown, which is a unique event [23]) with larger conductivity. That would explain, as shown in Fig 5 (which corresponds to the resistance of the LRS and HRS of different capacitors as a function of their area) and as reported in other works [11], why the conduction in the HRS scales with the device area and in the LRS it does not. At the LRS, although many conductive filaments could also be formed (as for the HRS), the main part of the current flows through a unique location, masking the current flowing through the rest of partially formed CF.

3.3. Resistive switching on HfO_2/Pt structures triggered with the CAFM tip

Since CAFM images of Fig. 4 were obtained on the top electrode of the capacitor, not information about the origin of RS can be

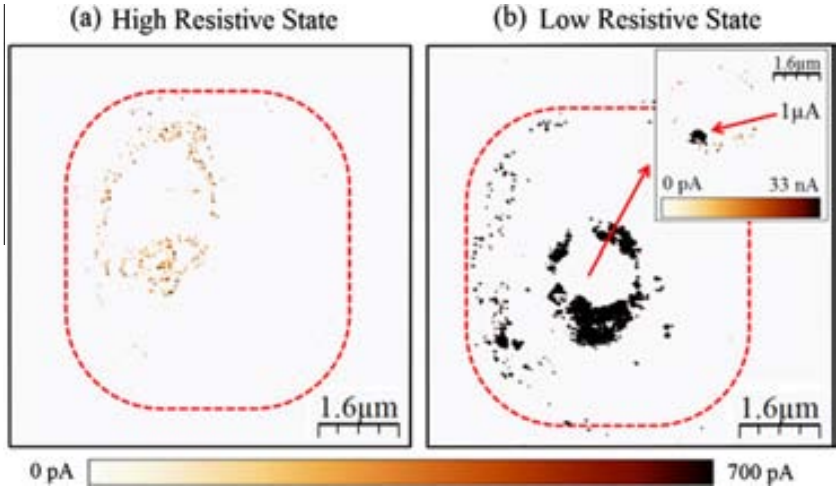

Fig. 4. 2D Current images of (a) HRS and (b) LRS (with different scales) when scanning the capacitor with the tip of the CAFM by applying 1.5 V. The red dotted line outlines the capacitor.(For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

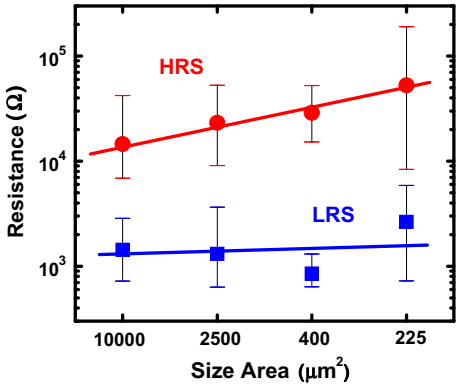

Fig. 5. Resistance of MIM structures at the LRS and HRS as a function of the gate area. At the HRS, conduction shows area dependence.

extracted. Topography images do not reflect the morphological properties of the high-k dielectric, but of the TiN electrode. To determine which features in the insulator stack promote the formation of reversible CFs, blanket HfO_2 layers (without the top electrode) with identical characteristics to those used as dielectric in the capacitors have been analyzed at the nanoscale with the CAFM. In this case, since the CAFM resolution is of few nm (of the order of the width of GBs [20]), and the set-up allows to analyze grains and GBs of the polycrystalline HfO_2 layer independently (Fig. 6). Using this setup, ramped voltages have been applied by the CAFM tip at 24 different locations of the HfO_2 layer, and two types of the *I–V* curves were observed (see representative examples in Fig. 7a): most of the curves (at 21 locations) show forming voltages above 11 V, while the others (at only 3 locations) exhibit a lower BD voltage ($V_{BD} \sim 4$ V), which is comparable to that measured at the device level, see Fig. 3. After the CF formation, an additional set and reset cycle was performed to determine the electrical properties of each of the analyzed locations. Only those sites which exhibit lower forming voltages (see Fig. 7a) demonstrate a typical bipolar RS (Fig. 7b) similar to that in the MIM structures (Fig. 3), with comparable magnitudes of the LRS and HRS currents. The sites with larger forming voltages do not show the RS effect meaning that an irreversible breakdown is caused by the forming process. Therefore, from these results one can conclude that the RS observed at device level is not only controlled by a very reduced area, as demonstrated in previous section, but also RS phenomenon takes place only at those positions in the device with a weaker "dielectric

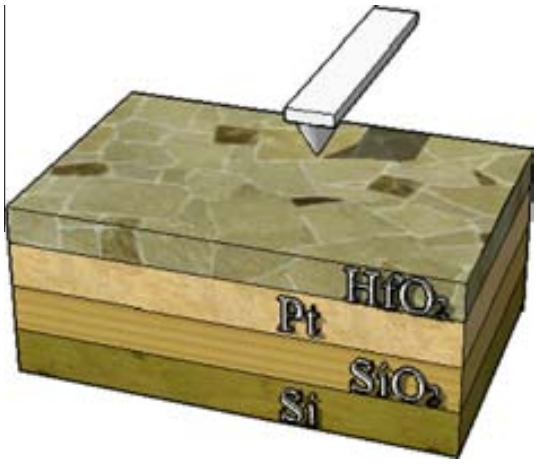

Fig. 6. Schematics showing the experimental setup when working directly on the HfO_2 layer. The CAFM tip of a nanoscale dimension acts as the metal electrode of a MOS structure with enough resolution (few nm) to study grain and GBs.

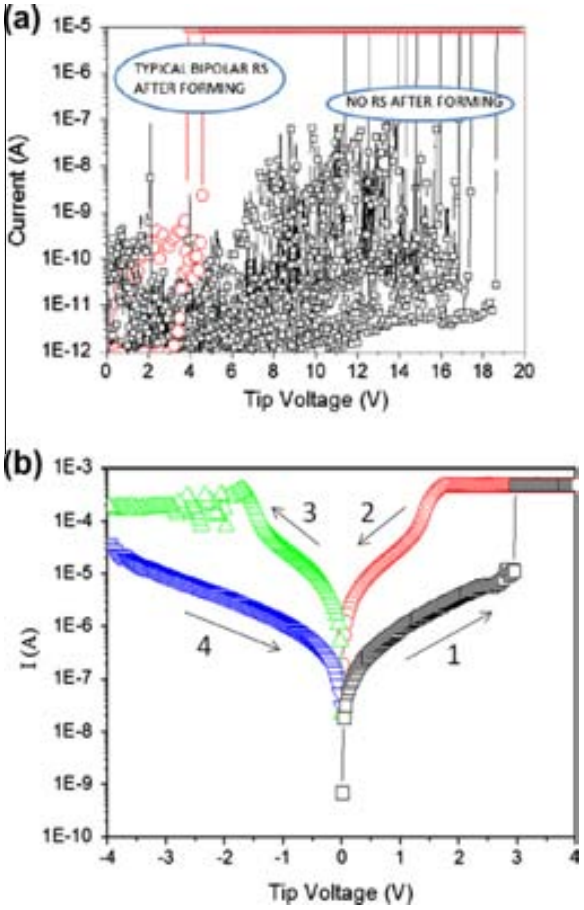

Fig. 7. Forming process (a) and typical resistive switching behavior (b) observed on the bare HfO_2 layer with the CAFM tip.

strength". Since in Section 3.1 it was demonstrated that the leakiest positions correspond to GBs [20], our measurements demonstrate that in polycrystalline HfO_2 gate dielectrics the RS phenomenon is basically registered at these positions.

4. Conclusions

In conclusion, the RS phenomenon in polycrystalline HfO_2 films has been analyzed at the nanoscale and device levels. The results show strong similarities between the device and nanoscale RS features suggesting that the RS in RRAM devices is controlled by a localized process taking place at the nano-size area of the dielectrics. CAFM results point out that RS is only observed at leaky dielectric locations, that is, at the grain boundaries, suggesting that failure mechanisms such BD could be related to the RS observed in our structures. The area dependence of the HRS conductivity has also been explained from the comparison of current maps measured on MIM structures in the LRS and HRS states. While in the LRS a single CF drives most of the current flowing through the device, in the HRS, multiple partially formed filaments could be the origin of the observed current area dependency.

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ANNEX

Temperature dependence of CAFM TDDB distributions in polycrystalline HfO_2 gate stacks: The role of the interfacial layer and grain boundaries

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Abstract—***Dielectric breakdown (BD) in polycrystalline HfO_2 gate stacks with a SiO_2 interfacial layer (IL) has been studied using a conductive atomic force microscopy (CAFM) technique, which allows a nanosize probe to apply a highly localized electrical stress. The resulting BD statistics indicate that BD preferentially occurs in the IL beneath the grain boundaries (GBs) of the overlaying polycrystalline HfO_2 film due to the GB conductivity being higher than that of the grains.***

Index Terms— ***Dielectric breakdown; Conductive Atomic Force Microscopy; high-k; grain boundaries.***

I. INTRODUCTION

In advanced transistor technology the high-k (HK) gate stacks complicates the evaluation of the dielectric breakdown mechanism. The different defect generation rates of HK and the SiO_x interfacial layer (IL) may lead to bimodal BD statistical distributions [1]. Alternatively, one of the layers may control the overall HK/IL stack breakdown, specifically the IL, while the HK may have little impact on device lifetime [2,3]. It is, therefore, critical to investigate the roles of the IL and HK dielectric on the overall degradation and breakdown of the gate stack.

Time-to-breakdown (t_{BD}) is usually obtained by applying an accelerated electrical test to MIS devices. However, the local nature of BD [3] difficults the correlation of BD to the nanoscale features of the dielectric. Alternatively, Scanning Tunneling Microscope (STM) [4] and Conductive Atomic Force Microscopy (CAFM), which offer high lateral resolution, are effective techniques for addressing localized electrical material properties [5]. In particular, in this work, a CAFM, which allows to investigate simultaneously and independently the topographical and electrical properties of gate stacks with a quite simple experimental set-up, was used to study the time-dependent dielectric breakdown (TDDB) in polycrystalline HfO_2 gate stacks at the nanoscale by applying a constant voltage stress (CVS) with the CAFM tip. A statistical analysis of t_{BD} distributions measured on the grain (G) and grain boundary (GB) locations is performed in a wide range of temperatures. The roles of the HK and IL layers, as well as the impact of the HfO_2 polycrystalline structure on the gate stack BD, are evaluated.

II. EXPERIMENTAL

Gate dielectric stacks consisting of a 5 nm thick atomic layer deposited (ALD) HfO_2 film and a 1 nm SiO_2 IL grown on a Si epitaxial p-substrate were investigated. The gate stack was annealed at 1000°C in N_2 ambient to simulate the thermal budget of the gate-first transistor fabrication process that results in further crystallization (compared to as-deposited) of the HK film. The gate stack properties were investigated using a CAFM (in air ambient and working in contact mode) that can operate at temperatures up to 240ºC. The electrical BD was induced by biasing the substrate with respect to the tip of the microscope (a PtIr-coated silicon tip, which acts as a metal electrode in a MOS structure) placed at random locations on the surface of the gate stack . A CVS of -8.2V was applied to the sample (tip was grounded) to avoid anodic oxidation, and t_{BD} was extracted by measuring current-time characteristics. BD was assumed to occur when a sudden increase of current was observed, reaching 10nA, which corresponds to the saturation of the electronics. These measurements were perfomed at different temperatures: 30ºC, 60ºC, 90ºC, 120ºC, 180ºC, and 210ºC. To collect a statistically significant number of data points, an average of 60 positions was studied for each T, and the corresponding Weibull distributions [6] were analyzed.

III. RESULTS AND DISCUSSION.

Fig. 1 shows a topographical, left, and current, right, image obtained on the HfO_2 layer. Note that the surface exhibits a granular structure (Gs), surrounded by depressed regions (GBs). Moreover, in current image, a granular pattern overlaps with that of the topographical image. These results show that, a good topographical-current correlation is detected in such sample, which has been mostly adscribed to an excess of O-vacancies at GBs [7],. Fig. 2a shows examples of the t_{BD} Weibull plots obtained at 60ºC (circles) and 210ºC (squares). The TDDB distributions show a bimodal behavior (dashed lines are guides to the eye for the different modes). To investigate the origin of the bimodality, the t_{BD} distributions measured on Gs and GBs were analyzed independently. To distinguish the G and GB locations, the

magnitude of the initial current [I(t=0s)] was considered. Since GBs are leakier than Gs in these HK layers [8], those positions with higher initial currents were assumed to correspond to GBs. Fig. 2b shows the Weibull plots of the t_{BD} distributions measured on Gs (squares) and GBs (circles) at 60ºC, which can be fitted by Weibull distributions. Note that, although at first glance it could be interpreted as a bimodal behavior, this assumption cannot be concluded so clearly as in Fig. 2a. First, because the criteria to discern between the sites corresponding to G and GB is not totally accurate. Therefore, some of the points with low t_{BD} in the G distribution could correspond to GB sites. Second, the tails at small t_{BD} in the GBs Distribution correspond to times close to the setup resolution. Fig. 3a and 3b show the Weibull slope, β, and, scale factor, η (time for a 63% probability of BD occurrence), respectively, experimentally obtained at Gs (squares, filled symbols) and GBs (circles, filled symbols) for all T. Note that when G and GB TDDB data are analyzed independently (Fig. 2b and 3), the Weibull distributions exhibit similar slopes. The bimodal feature arises only when G and GB data are combined within the same Weibull distribution (Fig. 2a), suggesting that differences in the electrical properties of both types of sites in the HK layer can be the origin of such bimodal behavior. This hypothesis is supported by modeling the global TDDB distribution (Fig. 1) as a combination of two different BD distributions (Fig. 2) corresponding to Gs and GBs (Eq. 1),

$$F(t) = P_{GB} \cdot F_{GB}(t,\beta,\eta_{GB}) + (1-P_{GB}) \cdot F_G(t,\beta,\eta_G) \quad (1)$$

where P_{GB} is the probability that the randomly positioned CAFM tip was over a GB, and F_G and F_{GB} are the Weibull distributions for Gs and GBs. The same β values were considered in both cases, as suggested by the data in Fig. 3a. The proposed Eq. (1) fits the global TDDB distributions (continuous line, Fig. 1) well, with β and η values close to those experimentally obtained over the entire range of temperatures (open symbols in Fig. 3a and b). The Weibull parameters extracted from G and GB distributions at different T were analyzed in more detail. Fig. 3 shows that β is independent of the measurement position (G or GB) and temperature. However, for a given T, η is lower for GBs than for Gs. This means that on average the GBs sites break faster, which is consistent with the observed preferential BD at the leakiest positions (GBs), likely because an excess of oxygen vacancies tend to accumulate there [7,8]. Moreover, η decreases with T [9], which could be related to a higher rate of trap generation at higher temperatures [10]. From the temperature dependency of η, the activation energies (E_a) of BD-related traps at Gs and GBs have been estimated assuming an Arrhenius dependency. In Fig. 3b, the lines correspond to the Arrhenius dependency of η for the data measured on Gs (filled circles) and GBs (filled squares) locations. Similar activation energies (E_a) of 0.20±0.04 and 0.23±0.02eV were extracted for Gs and GBs, respectively. These values are also close to those obtained from Eq. (1) (Fig. 3b, open squares). Since E_a reflects the nature of the defects, this result suggest that defects with similar features are likely responsible of the BD triggered at both G and GB sites. The similar β and E_a values at Gs and GBs (though with smaller η for the latter) suggest that BD at both sites could be triggered by the same process. Considering also that SiO_2 β does not depend on T [9] and an E_a of ~0.2-0.25eV has been extracted for the SiO_2 IL in the HK gate stack [11,12], these results indicate that the stack BD could be triggered by the BD of the IL underlying the HfO_2 film, as was suggested earlier [12].

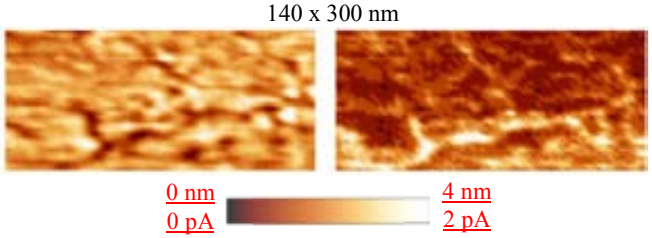

Fig.1. Topograhical (top) and current (down) images at -8V. A granular pattern is associated with the presence of nanocrystals. Note that leaky sites are basically detected at Grain Boundaries.

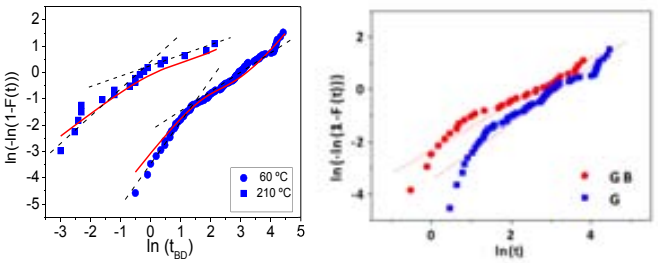

Fig.2.a. Examples of TDDB distributions at 60ºC (circles) and 210ºC (squares), fitted using Eq. (1) (solid lines). Broken lines outline the bimodal character of the distributions. (b) Example of TDDB Weibull distributions obtained at 60ºC at G (squares) and GB (circles) sites.

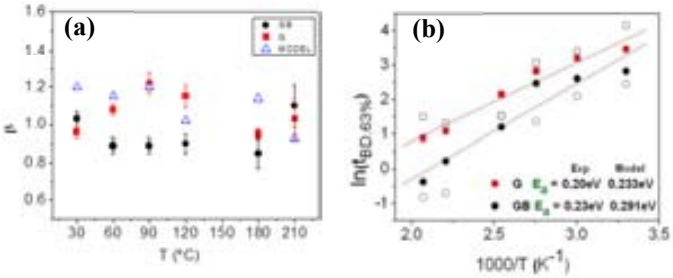

Fig. 3. Experimental (filled symbols) and modeled (open symbols) values of β (a) and η (b). Squares represent G and circles G_B sites (in (a); β was assumed to be the same at both sites in the model). The lines in (b) match the Arrhenius dependency of the η values. E_a is the extracted activation energy for the G and G_B data sets.

In [12] it is proposed that the formation of the BD path in HK gate stacks might be initiated by the degradation of the SiO_2 film. Then, the smaller η values for the GBs t_{BD} data are associated with the faster degradation of the SiO_2 region under the GBs. Indeed, higher currents through the GBs indicate that the GBs represent less resistive HfO_2 regions and that, as a result, the voltage drop is greater across those regions of the SiO2 film. The IL beneath GBs therefore undergoes accelerated degradation resulting in smaller t_{BD} values [8]. Thus, the SiO_2 IL experiences two different degradation rates determined by the morphology of the

overlaying HK dielectric, which could explain the global bimodal TDDB distributions given in Fig.2a.

IV. CONCLUSIONS.

The impact of the HfO_2 morphology on the TDDB distribution in HK gate stacks with a SiO_2 interfacial layer has been analyzed within a nanoscale spatial resolution using CAFM. The BD distributions collected at multiple, randomly chosen locations across the dielectric surface show a bimodal characteristic, which has been attributed to the different electrical properties of Gs and GBs in the polycrystalline HfO_2. The Weibull distributions of t_{BD} values collected either on G or on GB sites exhibit similar temperature-independent slopes. Moreover, similar activation energy values were extracted from the t_{BD} temperature dependencies at both types of sites. However, the GB sites show overall smaller t_{BD} values (smaller η). From these results, it is concluded that the gate stack BD is triggered by the BD of the SiO_2 layer. The smaller t_{BD} values measured on GBs can be attributed to a higher electrical stress experienced by the SiO_2 regions underlying the GB sites due to lower resistivity of the GBs, as was proposed earlier [12]. Therefore, the polycrystalline nature of the HK layer may strongly influence the BD properties of HfO_2-based gate stacks.

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