Silicon Nanowire growth technologies for nanomechanical devices

Thesis presented to apply for the degree of

Doctor in Electronic Engineering

by

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CERTIFICAN

Que la memoria "*Silicon Nanowire growth technologies for nanomechanical devices*" presentada por Marta Fernández Regúlez para optar al grado de Doctora en Ingeniería Electrónica por la Universitat Autònoma de Barcelona ha sido realizada bajo su dirección en el Instituto de Microelectrónica de Barcelona del Consejo Superior de Investigaciones Científicas.

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Contents

Introduction **iii**

1 State of the art in Si Nanowires growth technologies **1**

1.1 Vapor Liquid Solid growth mechanism 3

1.1.1 VLS-CVD growth of Si nanowires 4

1.2 Other growth techniques 5

1.2.1 Thermal evaporation 5

1.2.2 Molecular Beam Epitaxy 6

1.2.3 Laser ablation growth 7

1.2.4 Solution growth methods 7

1.3 Methods for deposition of metal catalyst nanoparticles 8

1.3.1 Thin film deposition 9

1.3.2 Lithography deposition techniques 9

1.3.3 Colloidal gold nanoparticles 10

1.3.4 Galvanic displacement techniques 12

1.4 Control of Nanowire properties 12

1.4.1 Nanowire diameter 12

1.4.2 Crystallography growth direction 14

1.4.3 Nanowire morphology 15

1.4.4 Growth Rate 17

1.4.5 Conductivity on nanowires 20

1.5 Fabrication of complex structures based on nanowires 21

1.5.1 Fabrication of heterosturctures by bottom up approach 21

1.5.2 Integration on complex architectures 22

References 28

2 Optimizing Si nanowire growth via the VLS growth mechanism 39

2.1 Introduction and objectives 41

2.2 Catalyst deposition via galvanic displacement 42

2.2.1 Galvanic displacement optimization for the synthesis of high density Si nanowire arrays 42

2.2.2 Galvanic displacement optimization for the synthesis of single nanowire 45

2.3 Silicon nanowire growth optimization 46

2.4 Doping of Si nanowires 51

2.5 Conclusions 53

References 55

3 Application of Si nanowire array fabrication technologies: Piezoresistive Cantilever 57

3.1 Introduction 59

3.2 Piezoresistance in Si nanowires 61

3.3 Cantilever sensor design and theoretical performance 63

3.3.1 Motivation and objectives 63

3.3.2 Sensitivity 64
3.3.3 Theoretical analysis of mechanical properties 68
3.3.4 Noise 71
3.3.5 Resolution 75
3.4 Fabrication technology 76
3.4.1 Substrates 76
3.4.2 Process Flow 76
3.4.3 Chip design 78
3.5 Fabrication results 80
3.6 Characterization of the cantilevers 84
3.6.1 Noise characterization 85
3.6.2 Sensitivity and detection limit characterization. 90
3.7 Conclusions 93
References 94

4 Single Si nanowire device fabrication technology: application to nanomechanical sensors based on nanowire resonators 97

4.1 Introduction and motivation 99
4.2 Technologies based on colloidal catalyst 100
4.3 Technologies based on galvanic displacement 103
4.3.1 Objectives 103
4.3.2 Process Flow 103
4.3.3 Fabrication Results 105
4.4 Characterization results 108

4.4.1 Nanomechanical resonators for optical readout 108

4.4.2 Nanomechanical resonators for electrical readout: capacitive sensing 110

4.4.3 Nanomechanical resonators for electrical readout: piezoresistive sensing 110

4.5 Conclusions 111

References 113

Introduction

Motivation

Silicon nanowire growth based on the vapor-liquid-solid (VLS) mechanism is one of the most promising bottom-up nanofabrication approaches currently under research. Si nanowires grown by this mechanism are typically single-crystalline, highly anisotropic and high aspect ratio nanostructures that result from rapid crystal growth in one direction. The great importance of VLS growth is that it offers the possibility of achieving otherwise unfeasible structural conformations and material combinations at the nanoscale. This results in exceptional morphological, structural and functional properties with an enormous potential to be exploited for the development of ultra-high performance nanomechanical devices.

In the last years, advances in nanofabrication methods have led to an ever increasing progress in size reduction of nanomechanical devices. Size reduction is critical for nanomechanical devices because mechanical phenomena are greatly influenced by scaling-laws, thus resulting in completely extreme or different properties. Such properties can provide novel sensing and transduction mechanisms that push the performance of mechanical devices to their fundamental limits or, more importantly, to enable completely new device concepts. However, the practical development and widespread use of nanomechanical devices still faces important challenges that require intensive research efforts in several directions. Among these, two particular ones are considered as particularly important limiting factors: first, large scale/high-yield fabrication of sub-100 nm mechanical structures, and second, efficient transduction of very small displacements at very high frequencies into readable electrical outputs.

VLS-grown Si nanowires offer many extraordinary properties to face such challenges. Si nanowires can be predictably used to obtain single and double clamped nanobeams with many key parameters manipulated during growth, including diameter (down to 10 nm), length (arbitrarily long), and orientation (parallel to $\langle 111 \rangle$ or $< 110 >$ directions). In addition, their ability to result in double-clamped horizontally self-assembled nanobeams, together with their recently reported giant piezoresistance, enable an unprecedented approach to develop highly sensitive piezoresistive transduction schemes with applications in many nanomechanical devices. However, many Si nanowire properties, including giant

piezoresistance, are not yet fully applicable due to the lack of fabrication technologies that provide reliable means to integrate nanowires into functional devices.

General objective

The overall objective of this thesis is to achieve the capability of controlled manipulation of Si nanowire properties to be exploited for developing nanomechanical devices with performance characteristics at their fundamental limits or based on new working principles. To this end, the work developed has compromised all the following aspects:

- Optimization of a new atmospheric pressure chemical vapor deposition (AP-CVD) system installed at the IMB-CNM clean room for the synthesis of Si nanowires. The influence of growth parameters has been studied for different nanowire density and characteristics. The AP-CVD system has been modified to include an additional gas line for nanowire doping with boron atoms which has entailed a readjustment of growth parameters.

- Optimization of the selective area deposition of catalyst nanoparticles via galvanic displacement for the synthesis of individual Si nanowire and arrays.

- Development of fabrication technologies for the large scale integration of single nanowire and arrays that exploit their exceptional properties. These technologies has been successfully adapted for the fabrication of a piezoresistive cantilever based on Si nanowire arrays and of the mass sensor resonators based on single Si nanowires with different transduction mechanism (optical, capacitive and piezoresistive).

- Demonstration of a piezoresistive cantilever based on Si nanowire arrays. The integration of Si nanowire arrays as piezoresistive strain gauges provides an improvement in sensitivity that could reach more than two orders of magnitude.

- Demonstration of nanomechanical sensors based on single nanowire resonators.

This is the first thesis at the IMB-CNM (CSIC) that fully addresses a bottom-up Si nanowire fabrication technology from Si nanowire growth optimization to the proof-of-concept of Si nanowire based devices. Additionally, the nanowire growth technologies developed in this thesis have been adapted and used for the fabrication of other kind of devices in collaboration with several research groups. We might particularly note the fabrication of a planar thermoelectric generator developed in collaboration with the Thermoelectrics Group and the development of novel microbarcode devices for single cell labeling and tracking in collaboration with the group of Micro and Nanotools for Life Sciences, both groups at the IMB-CNM (CSIC).

Funding projects involved

The scientific activities realized in this thesis were developed in the frame of four main projects:

- **Title of the project:** Micro/nano systems fabrication by Nanoimprint Lithography.
  Reference: NILSIS-10039
  Duration: 2006-2009
  Kind of contract/Program: National I+D program 2004-2007.
  Financing organization: Spanish Ministry of Science and Education
  Institutions involved: Instituto de Microelectrónica de Barcelona (IMB-CNM, CSIC); Tekniker Foundation, Gaiker Foundation
  Main Researcher: Xavier Borrisé Nogué (IMB-CNM)

- **Title of the project:** Si nanowire based NEMS (NANOSi)
  Kind of contract/Program: Intramural Frontier Projects - CSIC
  Financing organization: CSIC
  Reference: NANOSi-200650F0091
  Duration: 2006-2007
  Institutions involved: Instituto de Microelectrónica de Barcelona (IMB-CNM, CSIC); Instituto de Microelectrónica de Madrid (IMM-CNM, CSIC); Instituto de Microelectrónica de Sevilla (IMS-CNM, CSIC); Instituto de Ciencia de Materiales de Barcelona (ICMAB, CSIC).
  Main Researcher: Alvaro San Paulo (IMB-CNM, CSIC), coordinator

- **Title of the project:** Advanced NEMS with applications to ultrasensitive biological detection
  Kind of contract/Program: National I+D program 2008-2011
  Financing organization: Spanish Ministry of Science and Innovation
  Reference: ANEM! (TEC2009-14517-C02)
  Duration: 2010-2012
  Institutions involved: Instituto de Microelectrónica de Barcelona (IMB-CNM, CSIC); Instituto de Microelectrónica de Madrid (IMM-CNM, CSIC);
  Main Researcher: Francesc Perez-Murano (IMB-CNM, CSIC)

- **Title of the project:** Towards the ultimate limit of mass detection by the manipulation of multimodal vibration in Si nanowire resonators
  Kind of contract/Program: Explora Program
  Financing organization: Spanish Ministry of Science and EducationReference: YOCTOMASA (TEC2009-07707-E/TEC)
  Duration: 2010-2011
  Institutions involved: Instituto de Microelectrónica de Barcelona (IMB-CNM, CSIC)
  Main Researcher: Alvaro San Paulo (IMB-CNM, CSIC)

Structure of the thesis

The thesis has been organized as follows:

- An introduction about the state of the art in Si nanowire growth technologies is given in the **Chapter 1**. Here, advances in catalyst deposition and control of nanowire properties such as length, diameter, morphology, composition and conductivity are described as well as recent reported progresses on large scale nanowire device integration.

- **Chapter 2** describes the optimization of selective area deposition of catalyst gold via galvanic displacement as well as of the Si nanowire growth and doping processes. These conditions will be applied in next Chapters for the fabrication of devices based on single nanowires and arrays.

- The design, fabrication and characterization of a piezoresistive cantilever based on Si nanowire arrays will be described in **Chapter 3**. These devices take advantage of the giant piezoresistive coefficients of Si nanowires compared with bulk.

- **Chapter 4** shows the fabrication technology of nanomechanical resonators based on Si nanowires for sensing applications. This technology has been used for the fabrication of singly and doubly clamped Si nanowire resonators with different transduction mechanisms (optical, capacitive and piezoresistive).

Scientific contributions

The results described in this thesis have led to the publication of the following peer reviewed papers and patents:

Publications

- **Authors:**M. Fernández-Regúlez, M. Sansa, M. Serra-García, E. Gil-Santos, J. Tamayo, F. Perez-Murano, A. San Paulo.
  Title: Horizontally patterned Si Nanowire growth for nanomechanical devices
  Journal: SMALL (in preparation; submission scheduled for July 2012)

- **Authors:**S. Durán, S. Novo, M. Fernández-Regúlez, M. Duch, R. Gómez-Martínez, A. San Paulo, E. Ibáñez, J. Esteve and J. A. Plaza
  Title: Silicon nanovelcro to attach inorganic microdevices to biological material
  Journal: Nano Letters (in preparation; submission scheduled for september 2012)

- **Authors:**M. Fernández-Regúlez, A. San Paulo.
  Title: Ultra high density nanowire arrays from galvanic displacement deposition of Au catalyst nanoparticles
  Journal: Nanotechnology (in preparation; submission scheduled for october 2012)

- **Authors:**: D. Davila, A. Tarancón, C. Calaza, M. Salleras, M. Fernández-Regúlez, A. San Paulo, L. Fonseca
  Title: Integration of multiple linked arrays of silicon nanowires into planar thermoelectric microgenerators
  Journal: Nano Energy (in press)

- **Authors:**E. Gil-Santos, J. Martinez, M. Fernández-Regúlez, R. García, A. San Paulo, M. Calleja, J. Tamayo.
  Title: Nanomechanical mass sensing and stiffness spectrometry based on two-dimensional vibrations of resonant nanowires
  Journal: Nature Nanotechnology 5 (9) pp. 641-645 (2010)

- **Authors:**: D. Ramos, E. Gil-Santos, V. Pini, J.M. Llorens, M. Fernández-Regúlez, A. San Paulo, M. Calleja, J. Tamayo
  Title: Optomechanics with Silicon Nanowires by Harnessing Confined Electromagnetic Modes.
  Journal: Nano Letters 12 (2) pp. 932-937

- **Authors:**: D. Davila, A. Tarancón, M. Fernández-Regúlez, C. Calaza, M. Salleras, A. San Paulo, L. Fonseca
  Title: Silicon nanowire arrays as thermoelectric material for a power microgenerator.
  Journal: Journal of Micromechanics and Microengineering 21 (2) pp. 104007 (2011)

- **Authors:**: D. Davila, A. Tarancón, D. Kendig, M. Fernández-Regúlez, N. Sabate, M. Salleras, M. Calaza, C. Cane, I. Garcia, E. Figueras, J. Santander, A. San Paulo, A. Shakouri, L. Fonseca
  Title: Planar Thermoelectric Microgenerators Based on Silicon Nanowires
  Journal: Journal of Electronic Materials 40 (5) pp. 851-855 (2011)

- **Authors:** M. Fernández-Regúlez, J.A. Plaza, E. Lora-Tamayo, A. San Paulo
  Title: Lithography guided horizontal growth of silicon nanowires for the fabrication of ultrasensitive piezoresistive strain gauges.
  Journal: Microelectronic Engineering 87 (5-8) pp. 1270-1273 (2010)

Patents

- **Dispositivo de generación termoeléctrica, generador termoeléctrico y método de fabricación de dicho dispositivo de generación termoeléctrica**
  Thermoelectric generation device, thermoelectric generator, and method for producing said thermoelectric generator device.

Inventors: A. Tarancón, D. Dávila, N. Sabaté, A. San Paulo, M. Fernández-Regúlez, L. Fonseca
Patent Ref.: ES1641731 (2010)

Chapter 1

State of the art in Si Nanowires growth technologies

Contents

1.1 Vapor Liquid Solid growth mechanism . . . 3
1.1.1 VLS-CVD growth of Si nanowires . . . 4
1.2 Other growth techniques . . . 5
1.2.1 Thermal evaporation . . . 5
1.2.2 Molecular Beam Epitaxy . . . 6
1.2.3 Laser ablation growth . . . 7
1.2.4 Solution growth methods . . . 7
1.3 Methods for deposition of metal catalyst nanoparticles . . . 8
1.3.1 Thin film deposition . . . 9
1.3.2 Lithography deposition techniques . . . 9
1.3.3 Colloidal gold nanoparticles . . . 10
1.3.4 Galvanic displacement techniques . . . 12
1.4 Control of Nanowire properties . . . 12
1.4.1 Nanowire diameter . . . 12
1.4.2 Crystallography growth direction . . . 14
1.4.3 Nanowire morphology . . . 15
1.4.4 Growth Rate . . . 17
1.4.5 Conductivity on nanowires . . . 20
1.5 Fabrication of complex structures based on nanowires . . . 21
1.5.1 Fabrication of heterosturctures by bottom up approach . . . 21
1.5.2 Integration on complex architectures . . . 22
References . . . 28

1.1 Vapor Liquid Solid growth mechanism

The Vapor-Liquid-Solid (VLS) mechanism, introduced by Wagner [1] in 1964 for the growth of Si whiskers, is most widely employed to growth Si nanowires. This technique has been woldwide accepted and applied for understand the synthesis of a great variety of inorganic nanowires [2].

In this mechanism a liquid gold/silicon alloy droplet, over the eutectic temperature (363°), enables the highly anisotropic growth in a crystallographic direction. The silicon source is supplied by a gaseous silicon precursor. At the droplet surface, the precursor molecules are cracked and the resulting Si atoms are incorporated. When the alloy droplet became supersaturated, the precipitation of the solid silicon atoms is produced forming the nanowire. The name VLS refer to the fact that silicon from vapor passes through a liquid droplet and finally ends up as a solid. Parallel to the VLS growth Si deposition take place on the nanowire walls, by the Vapor Solid (VS) mechanism. Nevertheless, the accommodation coefficient on a solid surface is several orders of magnitude lower than liquid, and the deposition rate on sidewalls is negligible.

After the synthesis process, the alloy droplet remains at the tips of the nanowires. This was the only one evidence of the growth mechanism after the beginning of this century. Then, in-situ observation of the synthesis process was realized by Wu and Yang by transmission electron microscopy (TEM) for the growth Ge nanowires [3] and, posteriorly, by Ross and co-workers for Si nanowires [4]. The observations suggested that the process could be summarized in three main steps: alloying, nucleation and crystallization Fig 1.1.

Respect to the catalytic particle, several kinds of materials have been used as seed in the VLS process, but since the early publications the most commonly used has been Au. This present some advantages such as the high chemical stability, no toxicity and the formation of low melting eutectic temperatures with many of the semiconductors components. The binary Au-Si phase diagram is represented in the Fig 1.1. A simple deep eutectic is formed at the temperature of $363°C$ which means an important reduction of the melting temperature with respect to the pure components. However, for electronic devices, gold become unwanted since creates an impurity energy level within closer to the Si band gap middle or deep impurities. This can affect to the charge carrier lifetime by acting as a recombination center. In addition, due to its chemical stability, contaminated samples and equipments cleanness become impracticable. After gold, a great variety of materials have been reported to be used as catalyst in the VLS. The successful growth of Si nanowires has been obtained by many of them (Ag, Al, Bi, Cd, Co, Cu, Dy, Fe, Ga, Gd, In, Mg, Mn, Ni, Pb, Pd, Pt, Te, Ti and Zn) [5]. In spite of it all, gold already is the most frequently used by different causes. For example, some of the materials used, such as Ag, Co, Fe, Ni, Pd or Pt present a much higher eutectic point than the Au/Si system so a very high growth temperature is needed. Other with a very low eutectic point, such as In or Ga, present loss of catalyst material during the growth with the consequent tapered effect. And the Al, which was presented as an interesting alternative due to their compatibility with electronic devices, entail the doping of the nanowire during the growth

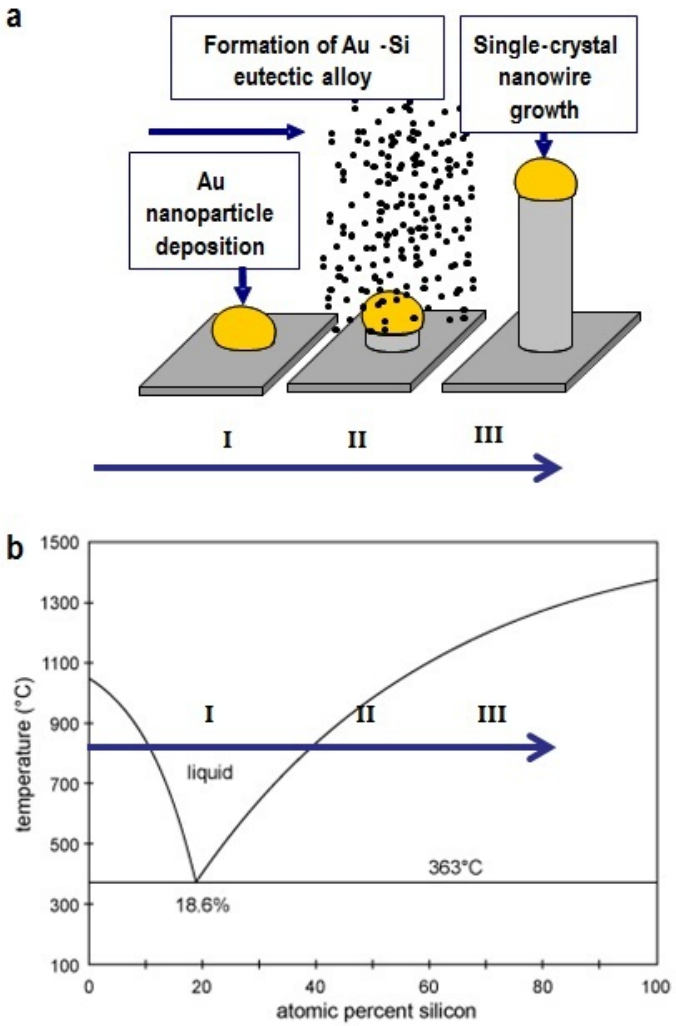


Figure 1.1: A) Schematic illustration of nanowire growth mechanism including three states: (I) Alloying, (II) Nucleation and (III) Axial growth. b) Compositional and phase evolution during the nanowire growth.

and his facility to be oxidized can difficult the epitaxial growth.

1.1.1 VLS-CVD growth of Si nanowires

Several techniques has been used for the VLS growth of nanowires, however, the most popular seems to be chemical vapor deposition CVD. In this technique typical Si precursor gases used for the synthesis of thin films in a CVD such as silicon tectrachloride, $SiCl_4$, in an atmospheric pressure CVD (AP-CVD), and silane, SiH_4, for a low pressure CVD (LP-CVD), are used. At catalyst surface precursor are cracked by following the next reactions:

$$SiCl_4(g) + 2H_2(g) \rightleftarrows Si(s) + 4HCl(g)$$
$$SiH_4(g) \rightleftarrows Si(s) + 2H_2(g)$$

However, the growth temperature is lower since metal nanoparticles catalyse the decomposition of the precursor gas employed. For instance, the Gibbs free energy of this reaction is positive up to $1550°C$ [6] so this means that, for the range of growth temperatures (around $800°C$), it is not produced. Only in the proximities of the catalytic gold surface the precursor molecules crack and solid Si is produced for the nanowires growth. Also Clorhidric Acid HCl is formed during as the by-product of the reaction. The presence of the HCl in the synthesis have important advantages respect to the nanowire epitaxy and morphology that will be explained in more detail in next sections. Similar results have been obtained by intentionally introducing a gas flow of HCl into the SiH_4/H_2 system.

In order to enhanced the effectiveness of the CVD growth at low temperatures for example, a plasma can be used to pre-crack the silicon precursor molecules and facilitate thereby the growth of nanowires[7].

1.2 Other growth techniques

Fabication of nanowires can be accomplished by a variety of techniques. The formation of one dimensional structures thus depends on the enhancement of the crystal growth rate in one dimension, and/or the suppression of the growth in the other. The growth mechanism can be classified following different aspects such as, the presence or not seed particle and the composition of the same, the phases involved in the process or the conditions in which the process is carried.

Although nanowires has been successfully synthesised by different methods, is important taking into account characteristics of the growth mechanism such as yield, compatibility or cost production in order to know which one could be the best way for the integration of nanowires on a device. Some of the most representative methods used at moment are described below and the main advantages and disadvantages of each are discussed.

1.2.1 Thermal evaporation

Nanowires can be fabricated by the simple method of evaporate a suitable source material and then depositing, at cooler temperatures, without the need of a catalytic particle. In many cases, growth is analogous to the VLS differing in that here one component of the vapor phase play the role of catalyst itself. This technique is also knowed as a Vapor Solid growth since no liquid metal nanoparticles is involved in the process. Typical materials

suitable this technique are metal oxide and some semiconductors. The diameter of the nanowires can be tunning by changing the evaporation and collection temperatures as well as the vapor pressure but high control of the spatial arrangement is difficult to achieve.

There are some materials contining no metal elements that can also develop into nanowires form their oxide decomposition by VS mechanism. A model called Oxide Assisted (AO) growth was therefore proposed with evidence form experiments on several kind of semiconductors such as Si [8], Ge and III-V [9, 10]. The OAG can be combined with the VLS mechanism for the growth of Si nanowires. In this case, gold nanoparticles are used as seed particles that became supersaturated due to constant supply of silicon from the disproportionation of silion oxide. The use of a catalytic particle defined preferred growth sites for nanowires. In other cases, a quasi-liquid metal oxide nanoparticle appears at the base of the nanowire [11] and the growth seems to follow an VLS mechanism.

1.2.2 Molecular Beam Epitaxy

In the Molecular Beam Epitaxy (MBE) the gas source of the VLS method is replaced by a solid high purity silicon target. The source is heated until evaporation and carried by a inert gas flow to the chamber where the substrate containing metal clusters is placed. This method was used for film deposition, but similar to the VLS, it was observed that metal impurities on the substrate produced nanowire growth. The precursor atoms are physically deposited onto all the substrate but, with higher deposition rate over the metal droplets producing the anisotropic growth. The atoms that form the nanowire came from two sources in the MBE [12]. First the direct flow of Si from the target; and second, the flux of the diffusing atoms from the silicon surface. The growth is carried in Ultra High Vacuum system in order to prevent contamination or oxidation.

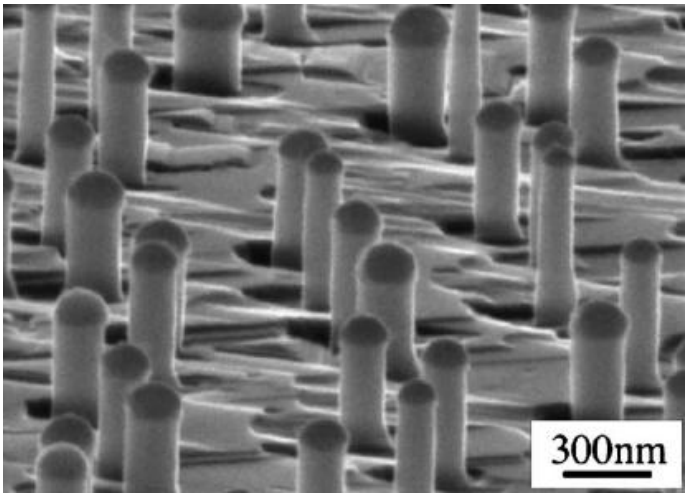


Figure 1.2: Si whiskers grown on a Si 111 substrate by MBE technique [13]

This mechanism has been used for the fabrication of a great diversity of nanowires such as Si [12, 14], ZnSe [15], ZnO [16], GaAs . One of the main advantages of the MBE is

that the source fluxes can be accurately controlled. This give the possibility of synthesis of heterostructures [13] by simply switching sources or well controlled doping profiles [17] when the MBE is equipped with evaporation sources of dopants. Nevertheless, this method present some disadvantages such as slow growth rate and the difficult to obtain nanowires with small diameters.

The Chemical Beam Epitaxial (CBE) can be consider like a variation of the MBE process. The CBE is a high vacuum system, similar to the MBE, but with the difference that vapour or liquid precursors are used instead of solid. This mechanism, initially also used for the synthesis of films and [18] and then for the synthesis of nanowires. This method has been employed for the fabrication of nanowires made of materials with drastically different lattice constant by simply combining the source materials.

1.2.3 Laser ablation growth

At difference with MBE process nanowires growth the Laser ablation technique allows the growth of ultrathin nanowires with very high aspect ratios. A metal coated target, placed in a tube furnaced, is ablated and vaporized by a high-power pulsed laser. The material ablated form the target cools by colliding with inert gas molecules, and the atoms condense to metal liquid nanodroplets with the same composition as the target. The growth process is similar to the VLS but, in this case, a substrate is not necessary since catalyst seeds are also dissolved in the vapor phase [19]. Nanowires with complex composition can be fabricated since only is necessary to use a simple mixture of elements.

However, the nanowire synthesis of many other materials has been possible by Laser Ablation without the need of adding any catalyst particle by the called self-catalyst growth. The materials include metal oxides, some semiconductors [20]and multicomponent materials with complex stoichiometries grow by OA mechanism. Unfortunately, the equipments used in this technique are considerably more expensive and complicated than simple thermal evaporation technique.

1.2.4 Solution growth methods

Solution growth methods have demonstrated to be a promising alternative technique for mass synthesis of metal, semiconductor and oxide nanostructures with relative low cost and easy fabrication techniques. For the fabrication of nanowires from solution, several routes have been developed, such as metal catalyzed solution-liquid-solid growth from metal seeds, self-assembly attachment growth and anisotropic growth of crystal by thermodynamic or kinetic control.

In the mid-1990 an alternative catalytic growth mechanism, which the precursor vapor phase is replaced by a liquid solution, was discovered. This mechanism was named

Solution-Liquid-Solid (SLS) growth by analogy with the previously reported VLS. This method was first developed by Buhro and co-workers for the synthesis of semiconductor nanowires of the group III-V [21] , and then, extended to a great variety of semiconductor materials[22, 23, 24, 25]. The main steps of the process are summarize in the figure 1.3. In this process, metal nanoparticles of low melting point, such as Bi, In or Sn, are used to catalyst nanowire growth in solution. The soluble precursors dissolve into the liquid to form nanowires after saturation.

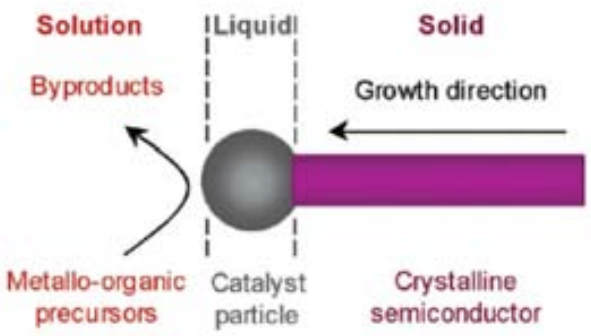


Figure 1.3: Nanowire SLS growth mechanism proposed by Buhro and co-workers

Nevertheless, semiconductors of the group IV materials, such as Si and Ge, have been extremely challenging to synthesize in solution due to difficulties associated with the precursor chemistry and the significant energy barrier to crystallization. The growth of Si and Ge nanowires in solution was achieved by Korgel and coworkers by using monodisperse gold nanoparticles under extreme temperatures and pressures that exceed the critical point of the solvent [26, 27]. This method was named Supercritic-Fluid-Liquid-Solid $SFLS$ also by analogy to the VLS. This method allowed the growth of nanowires with a very degree of control, narrow diameter distribution of only a few nanometers ans aspect ratios greather than 1000. Although very high quality nanowires are obtained, it would be more desirable to synthesize crystalline nanowires under milder conditions. The growth of Si and Ge nanowires by the SLS technique [28, 29] was finally reported the first decade of the XXI century.

1.3 Methods for deposition of metal catalyst nanoparticles

The integration of bottom-up nanowires on devices, nowadays, it is not absolutely resolved. A critical issue for fabrication is to develop an effective method to integrate a large number of nanowires on functional devices with control of their properties and dimensions. In some approaches nanowire arrays are created by controlled transfer process that pick up nanowires from the grown substrate and deposit them onto a different devices

substrate. Nevertheless, this technique is high time consuming and unsuitable for large scale manufacturing.

However, the direct growth of nanowires on top down prefabricated architectures could simplify the process. The control of nanowire position and diameter is determined by the gold catalyst nanoparticle. Gold particles generated and deposited with different techniques exhibit differences in the control of size, position, surface density and cleanliness so the election of the optimal deposition technique is determinant in the device fabrication process.

1.3.1 Thin film deposition

A commonly used procedure for generation of gold particles is thermal evaporation of a gold film onto the substrates. Following deposition, the substrates are heated up to high temperatures to split up the film in particles. The diameter and density of the resulting particles is determined by the thickness of the gold layer and the annealing temperature and time. A higher temperature, density and annealing time produce larger particles with lower density. Regardless of these parameters, is extremely difficult to obtain a low surface density and independently control of particles dimensions and density.

Although the extremely poor controllability, this method had advantages. It is a fairly simple, reasonably cheap and very clean method. This deposition technique can be used for the fabrication of vertical arrays of nanowires but become complicate for the growth of horizontal nanowires between the sidewalls of a prefabricated trenches. The deposition of gold catalyst was possible by tilting the samples inside an electron bean evaporation chamber [30].

1.3.2 Lithography deposition techniques

Lithography deposition of thin films could be consider as the evolution of the film deposition technique. This method starts with the deposition areas definition, by a lithography step, and follows with a thin film gold deposition, usually by evaporation. Different lithography techniques, such as Electron Beam [31, 32], Nanoimprint [33], nanosphere self-assembly [34, 35]and masks based on alumina template [36, 37, 38], has been used to define the catalyst deposition areas .

Electron Beam lithography allows the deposition of well defined gold clusters in the order of nanometers and with a high position accuracy. Nevertheless, this is a very expensive technique and became high time consuming for large scale deposition. Nanoimprint lithography is in many aspects capable of reproduce the results of those of Electron Beam lithography but a considerably high cost and with higher throughput. The main disadvantage could be the need of adjusting more parameters for optimization and alignment.

On the other hand the deposition of gold noparticles on sidewalls of a microtrench, by this technique, seems to be complicate.

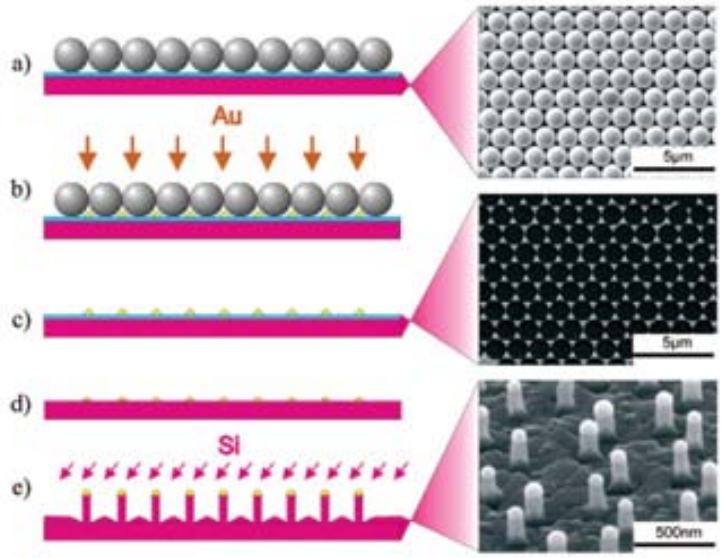


Figure 1.4: Steps for the synthesis of ordered arrays by nanosphere lithography: (a) Deposition of a mask of polystyrene particles on a Si(111) substrate covered by 2 nm thick oxide layer (blue), (b) deposition of gold by thermal evaporation, (c) removal of the spheres, (d) thermal annealing and cleaning steps to remove the oxide layer and, (e) Si nanowire growth by MBE. (Right) corresponding SEM images of wafers at different steps[34].

The use of masks such as spheres, of silica or polystyrene , in nanosphere lithography(Figure 1.4) or Anodic Aluminum Oxide (AAO) templates could be a solution for the fabrication of devices based on vertical ordered nanowire arrays. These two tecniques allow the deposition of hexagonal ordered monodisperse nanoparticle arrays for the subsequent synthesis of nanowires over a cm^2 scale. However, the fabrication of devices based on individual nanowires or horizontal nanowires seems to be impracticable by these kind of deposition techniques.

Recently, nanostencil lithography technique has been reported for the deposition of catalyst [39]. A shadow mask was used to deposit gold nanoclusters in the sidewalls of prefabricated trenches [40]. It was possible by tilting the sample inside the evaporation chamber.

1.3.3 Colloidal gold nanoparticles

Colloidal particles are synthesized by a chemical reaction, where chloroauric acid $HAuCl_4$ is reduced by citric acid or trisodium citrate in aqueous solution [41]. Commercially water solution of colloidal nanoparticles are commonly used for the fabrication of devices based on Si Nanowires. A wide range of diameters with a very narrow distribution is available. The colloids was first used by Lieber and co-workers for the growth of Si

nanowires [42], and previously for GaAs nanowires [43]. The nanowires produced in this way had narrow diameter distributions since nanowire distributions mirrors those of the colloids. Posteriorly the integration on prefabricated silicon microtrenches with control of the diameters, lengths and densities was possible demonstrating that nanowire growth and device fabrication was possible at the same time[44].

Gold colloidal nanoparticles are normally citrate stabilized to avoid the agglomeration. At a neutral pH, the citrate ions coat the gold particles, creating a negative charge which provide Coulombic repulsion between particles. This negative charge also prevent the deposition on silicon surfaces, because Si is expected to be negatively charged at neutral pH. For the deposition, a positively charged polyelectrolyte layer is needed as linker simply to dry the gold colloid solution on Si substrate. The polyelectrolite charge every surfaces and the deposition is not selective and nanowires are grown on all over substrate. However, if the polyelectrolyte is patterned in determined area the selective growth of nanowires is possible [45]. The selective deposition was demonstrated by Yang and co-workers by using a polyelectrolyte inked stamp Fig 1.5.

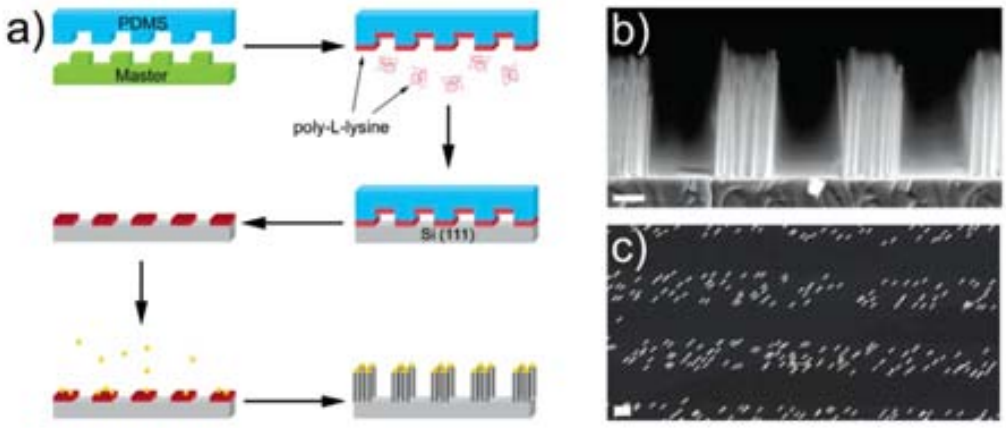


Figure 1.5: (a) Schematic of PDMS patterning of Au colloids. Briefly a PDMS stamp is molded to the relief pattern of a photoresist master. After curing the polymer the stamp is removed from the master and inked with solution of poly-L-lysine. The stamp pattern is transferred to the Si (111) substrate, which is then immersed in the Au colloid solution. The colloid-patterned substrate is grown using the conventional VLS-CVD synthesis, resulting in a corresponding pattern of Si nanowires grown. (c) plane view SEM image of the same scale bars are $1\mu m$ [45].

The addition of an acid to the colloidal solution was reported as a possible method to selectivity deposit the gold nanoparticles [46]. At low pH, the citrate ions are neutralitzed and the linker layer is not needed for the deposition on Si surface. Otherwise, the adhesion of this nanoparticles onto silicon oxide surfaces is poor. This selectivity for colloid deposition on silicon versus silicon oxide may provide a way to pattern gold colloids by selective deposition onto exposed silicon windows etched in overlying silicon oxide mask. Unfortunately, as a consequence of the citrate ions layer neutralization the colloidal decomposition and agglomeration is producer faster. For that is critical to acidify the nanoparticles just before the gold deposition.

1.3.4 Galvanic displacement techniques

The electroless plating deposition is defined as the deposition of a metal coating on a substrate from an aqueous plating solution without the need of any external voltage or current. When the deposition occurs through a reducing agent which reduce the metal ions in solution to metal the process is known as autocatalytic deposition. However, for galvanic displacement technique, reduction of metal ions in solution is effected by the substrate itself upon immersion in the plating bath, without the need of the reducing agent. It is a versatile method, well suited to yield films with high purity and substrate adhesion, and with complete substrate selectivity. Metal is deposited by a two half cell processes:

$$M^{m+} + me^- \rightarrow M^0$$
$$Sub \rightarrow Sub^{n+} + ne^-$$

Metal deposition occurs only on oxidizable substrates, such as Si or Ge, and is more thermodynamically favorable for metals with higher redox potential. In the case of Si substrate addition of fluoride ions in solution through HF helps to sustain the reaction by dissolving the silicon substrate as silicon hexafluoride, avoiding the formation of Silicon Oxide which stops the reaction. The global reaction of the process will be:

$$M^{n+}(aq) + Si^0(s) + 6F^- \rightarrow M^0(s) + SiF_6^{2-}$$

The deposition of diameter controlled gold nanocluster by galvanic displacement technique was achieved by Magagnin and co-workers in 2002 [47]. They used a water based plating solution, containing hidrofluoridic acid and a gold salt, with a surfactant sodium bis (2-ethylhexyl) sulfosuccinate (commonly known as AOT). High control of the micellar size was achieved by the microemulsion parameter ($R = [water] \,/\, [AOT]$). The substrate immersion on the solution produces a selective nanocluster deposition by galvanic displacement. Diameter and density of the deposited particles can be tunned by changing the micellar size and deposition time. The selectively growth of Si nanwires by gold seed deposited from these microemulsions was demonstrated some years later [48].

1.4 Control of Nanowire properties

1.4.1 Nanowire diameter

The VLS methods works correctly for a wide range of nanowire diameters. From whiskers of several to nanowires of only a few nanometers can be grown by this technique. The

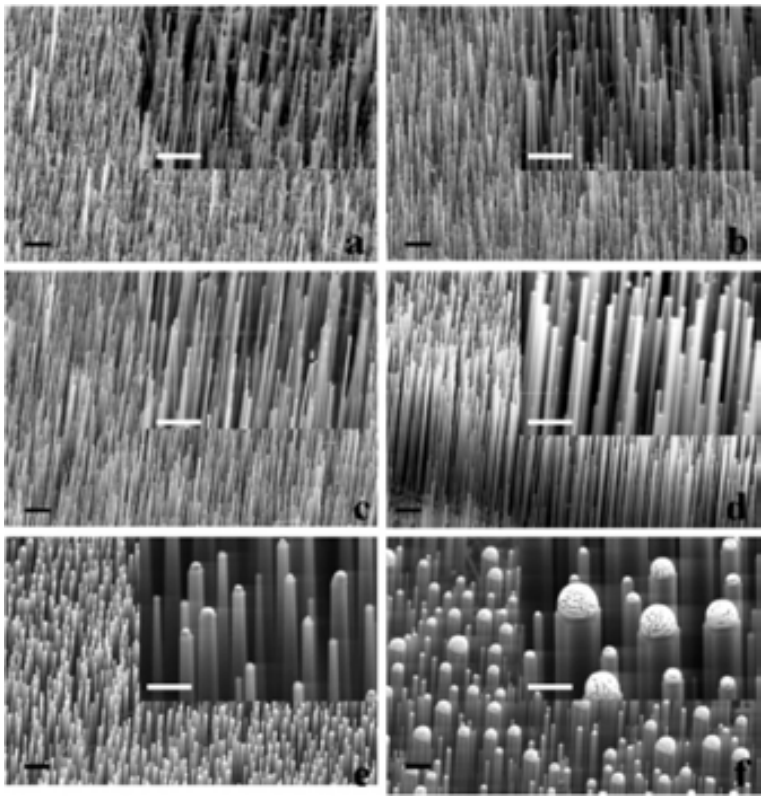


Figure 1.6: SEM images (with inset of close-up images) of vertical aligned Si nanowire arrays grown from Au clusters deposited by Galvanic displacement. The R parameter used in the process is 16(a), 25(b), 50(c), 100(d) and 200 (e), respectively. Au clusters deposited from water-based solution in (f). The scale bar is 300nm [48]

diameter will be determined by the size of the catalytic particle and the growth conditions used.

As it was explained in a previous section, the nanowire distribution mirror that of the catalytic particle. This means that, the uniformity of the nanowire array will be defined by the size dispersion of the catalytic particle. However, in the VLS mechanism, the diameter of the nanowire it is often noted to exceed that of the nanoparticle [49]. This is consistent with the supersaturation of the nanoparticle during the growth with the correspondent size increase. The relation between the nanowire and nanoparticle diameter can be derivate as [50]:

$$D = d\sqrt{\frac{1}{1-(\sigma_{ls}/\sigma_l)^2}}$$

where σ_{ls} and σ_l are the surface tension of liquid solid interface and of the catalyst. On the other hand, variations on the nanowire diameter along the wire can be occur by vapor solid deposition or lose of the catalyst particle by diffusion with the consequent tapering effect. These two effects can be avoided by tunning the optimal growth conditions to obtain a uniform diameter along the length. Only at the base of the epitaxially grown Si

nanowires they present an expansion in the region where the nanowire is attached to de substrate. This effect is not explained by a VS deposition, but by a change of the droplet shape in the initial growth stage[51].

1.4.2 Crystallography growth direction

The growth direction is an important parameter to control since this affects to nanowire properties, such as mecanical, optical and electrical transport. For Si nanowires growth in the ⟨111⟩, ⟨110⟩, ⟨112⟩ and rarely in the ⟨100⟩ has been observed. The growth direction depends of the catalytic particle involved in the process and the diameter. On gold catalysed Si nanowires, for diameters smaller than 20 nm the ⟨110⟩ direction is the preferred while for diameters larger than 30 nm the ⟨111⟩ direction become dominant. Transition between the two orientations takes place at a diameter of approximately 20 nm where the ⟨112⟩ orientation is also present although in low amount.

Lieber and co-workers [52] studied the diameter dependence for gold catalyzed Si nanowires. They found that the lowest growth energy is determined by the free energy solid-liquid alloy interface and the nanowire surface energy. For nanowires with larger diameters, the growth direction was determined by the lowest-free-energy solid liquid interface and this was parallel to {111} planes. However, for nanowires with smaller diameter the surface energy played an important role and, the favored growth direction was the ⟨110⟩. They also found that instead of grow in the ⟨110⟩ the front growth planes continued being the {111}, Fig 1.7. This demonstrate that the lowest solid liquid interface energy remain being in this direction and this is because the {111} surface has the largest density of surface atoms when acting as an interface.

The growth of nanowires with intermediate-diameter in the ⟨112⟩ was considered as a transitional growth direction since {112} is a stepped plane between the {111} and the {110}.

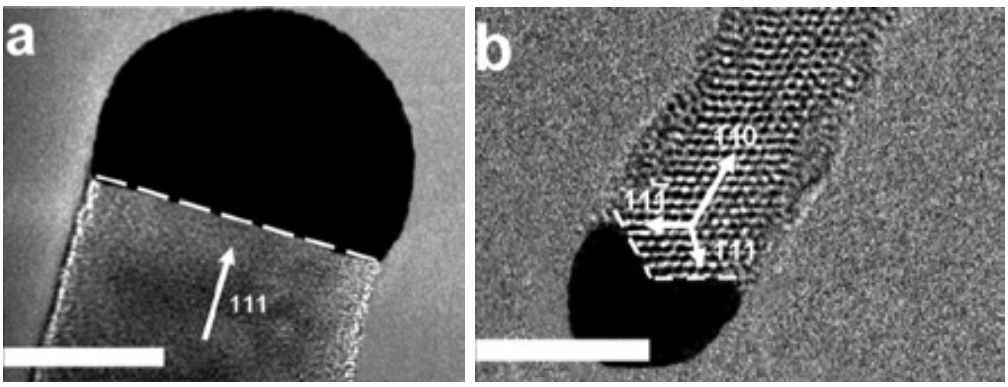


Figure 1.7: (a) HRTEM image of catalyst alloy/nanowire interface with ⟨111⟩ growth axis. Scale bar 20 nm (b) HRTEM image of catalyst alloy/nanowire interface with ⟨110⟩ growth axis. Scale bar 5nm

The next year, Schmidth and co-workers [53], studied the growth direction diameter

dependence from their experimental data and proposed a theoretical model that studied the effect liquid-solid interface and surface energies. They concluded with the existence of a transitional diameter around 20 nm. Under this diameter the surface energy had a decisive role and will be determined by the crystal orientation of the nanowire sidewall that will be analysed with more detail in the next subsection. Recently, Lugstein and co-workers [54] demonstrated that, a change in the growth direction from ⟨111⟩ to the ⟨112⟩ can be carried out by dramatically changing the system growth pressure and they suggested that an additional analysis will be need in the future to include this effect in the theory.

1.4.3 Nanowire morphology

At a difference from top-down fabricated nanobeams, catalytic grown Si nanowires have well faceted side surfaces. Nanowire surface, for a determined growth direction, is defined by crystalline planes which minimize the surface energy. This can be expressed as follow:

$$\Delta G_{surf} = \sum_j \gamma_j S_j$$

where γ_j is the surface energy per area unit of the jth crystal face, and S_j is the area of said surface. For Si crystals, the surface with lowest energies are in this order, (111) , (100) and (110). However, these surface energy relationships cannot solely predict the cross-section as minimization of the surface-to-volume-ratio must be consider. A review about the different growth directions and cross section was writing by Fortuna and Li [55].

The ⟨111⟩ growth direction of Si nanowires presents two possible perpendicular planes to form the sidewalls, the {110} and {112}. For Si whiskers, with diameters in the order of microns, both planes have been observed to form the side surfaces. However, the nanowires are preferentially enclosed by six {112} crystallographic planes forming an hexagonal cross section. Ross and co-workers [56] observed that the sidewalls were not completely flat but a secondary sawtooth faceted with a regular periodicity was present. Small {111} and {113} secondary facets growing in the {112} facets formed the secondary faceting. This faceting was explained as fluctuations during the growth in any VLS system in which there are no stable parallel growth direction. Nanowires can also exhibit six additional {110} facets, which form a 30° with the {112}, truncating the edge of the usual hexagonal cross-section. These additional facets also present sawtooth faceting tilted with respect to the horizontal and seems to be only present at the top of the cantilever where the VS deposition is lower.

Nanowires grown in the ⟨110⟩ direction present available low free energy sidewalls in the {110} and {111} planes. As these surfaces are energetically more favourable, a secondary faceting is not presented. Several geometries can be formed by these crystallographic planes but the most commonly observed is the hexagonal enclosed by two planes

{110} and four planes {111} [52].

In contrast with the previous nanowire orientations, the ⟨112⟩ oriented ones presents only a one possible low index plane configuration. Zhang et al [57] found that the possible cross section had rectangular shape with two {111} and two {110} planes. This was experimentally observed [58].

Finally, the only Si planes available for ⟨100⟩ oriented nanowires are {110} and {100} [59]. Thus, the surface energy of these wires are relatively high. For these reason the frequency of occurrence of ⟨100⟩ oriented wires is small and no many references about these kind of wires are presented in the bibliography [60].

1.4.3.1 Effects of the HCl and doping on Nanowire morphology

The presence of HCl during the nanowire growth has been reported to reduce the vapor solid deposition on the sidewalls. The main cause is the surface clhoration by the Cl atoms[61, 62]. The VS mechanism is slowed by the passivated surface which, at the same time, inhibits the gold diffusion during the growth that could act as catalyst for the lateral growth. The vapor-solid deposition on Si nanowire surface produce not only an increment on the diameter but also a secondary faceting enlarging. These effects would be more pronounced in the nanowire bottom zone than in the top zone, since the exposure time is longer. While the HCl concentration is increased the VS deposition is decreased until at a optimum value where it is no produced. If the HCl concentration increase over this value the nanowire surface etching starts [63].

An evolution on the number of sidewalls has been also observed with an increase of the sidewall deposition. As the amount of deposited Si is increased, due to an increase of either the vapor solid deposition rate or exposition time, the number of sidewalls decreases. The cross section of nanowires can adopt various shapes: dodecagon, deformed dodecagon, hexagon, deformed hexagon and even triangle for more extreme conditions.

On the other hand, the introduction of some impurities in the catalytic particle can alter the growth mechanism . Especially Boron doping, which is known to promote the $SiCl_4$ decomposition adding another complication factor to optimize the growth conditions [64]. The surface effects observed by the B dopant atoms is the opposite than in the case of Cl attoms. Here, at higher B concentrations, an increment in the nanowire diameter and a gold catalyst instability with the consistent loss of Au during the growth has been observed [65]. The nanowire diameter increment is attributed to an VS deposition enhancement by B presence and an increment in the secondary faceting has been observed [66].

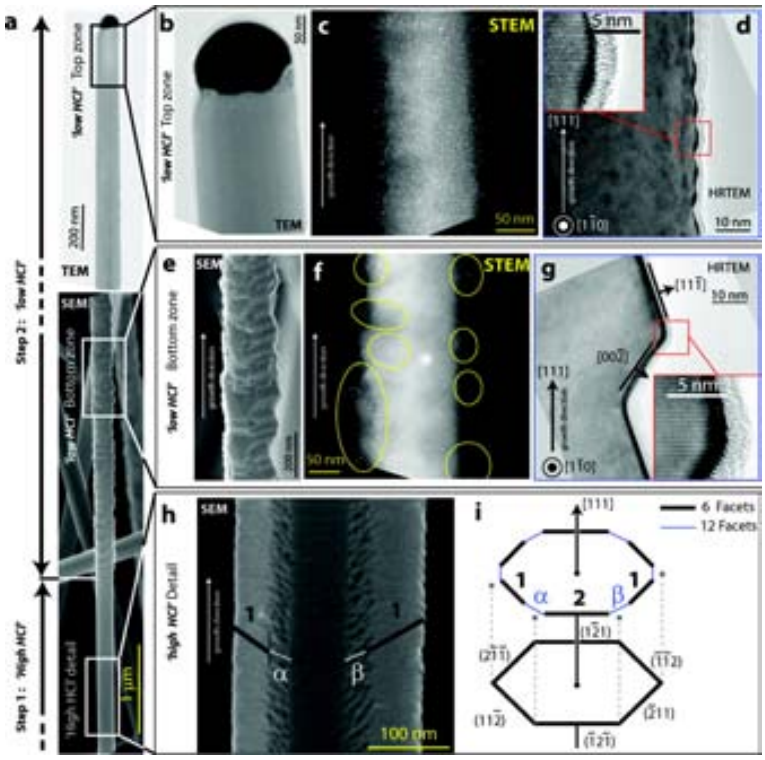


Figure 1.8: Morphology of two-step nanowire. Step 1 is a high HCl step (SiH_4 50 sccm, HCl 100 sccm, 650°). (a) Overview of the wire shape, SEM and TEM images. (b), (c) and (d) are respectively TEM, STEM-HAADF (high angle annular dark field), and HRTEM images of the top of the wire (low HCl zone). (h) Surface at high HCl segment, showing a dodecagonal shape. (i) Schematic of corresponding dodecagonal primary faceting. [62]

1.4.4 Growth Rate

1.4.4.1 Diameter dependence

A diameter dependence of the nanowire growth rate has been reported by several authors. In general, nanowires with smaller diameters present a slower growth rate than thicker ones. However, for whiskers with diameters of several microns the opposite behaviour has been observed and the growth rate decrease when the diameter is increased. These contradictory observations have made difficult to reach an agreement on which is the delimiting mechamism in the growth rate.

As it has been explained previously, nanowire growth process can be summarized in three main steps, Fig 1.1: (i) the incorporation of Si atoms to the liquid droplet, (ii) Si diffusion through the droplet and (iii) crystallization of the Si at the liquid-solid interface to form the nanowire. The nanowire growth rate will be delimited by the slowest step[67]. From the three, the second one, the diffusion of Si atoms through the droplet is rejected since for droplets of microscopic dimensions, diffusion through the droplet is too fast. Respect to the other two steps, arguments in favour of both has been presented.

The incorporation rate, $\rho_{inc}\left(p, \mu^{vl}\right)$, depends of pressure and chemical potential be-

tween liquid and vapor μ^{vl}, which may be proportional to the probability of precursor molecules to stick on the droplet, and the pressure which is proportional to the number of molecules. On the other hand, the crystallization rate, $\rho\left(\mu^{ls}\right)$, depends on the droplet supersaturation $\mu_{ls} = \mu_l - \mu_s$, where μ_l and μ_s are the chemical potential of liquid catalyst and nanowire respectively. The μ_s can be expressed by the Gibbs-Thomson effect as follow:

$$\mu^s = \frac{C^s}{r}$$

where r is the nanowire radio and C^s is defined as $C^s = 2\Omega^s\sigma^s$ with Ω^s and σ^s being the molar and the surface tension of silicon respectively. Then the crystallization rate is radio dependent via the Gibbs Thomson effect.

In 1971, Bootsma and Gassen [68]observed a growth rate pressure dependence which demonstrated that the delimiting step was the first one, the incorporation of vapor molecules to the droplet. A few years later, Guivargizov [69] in disagreement with that, took the opinion of that the crystallization was rate determining. He found that the growth rate decreased for smaller diameters according to the Gibbs-Thomson effect. The same behaviour was observed by Weyher [70] for Pt catalysed Si whiskers but only for diameter smaller than $5\mu m$. For larger diameters the whiskers presented the opposite behaviour. He suggested that, in that case, the diffusion in the liquid phase, negligible for smaller diameters, play here the VLS step rate determined. However, posterior contradictory experiments have made difficult the formulation of a theoretical model about the diameter dependence. Finally, a thermodynamical model about the growth rate dependence was developed by Schmidt and co-workers [67]. They proposed that the assumption of a single rate-determining step had to be rejected. The interplay of both, incorporation and crystallization had to be consider. Taking into account that, under steady conditions, incorporation and crystallization rate must be equal, they concluded that the dependence of the growth velocity and nanowire diameter is a consequence of a Gibbs-Thomson effect and the interplay between the incorporation of Si at the vapor liquid interface and their crystallization at the solid-liquid interface. The resulting growth velocity have the shape:

$$v = v_0 + \Gamma\frac{\Omega_m\sigma^s}{r}$$

where v_0 is the steady growth velocity when the radius tends to infinite. The second term on the right hand comes from the Gibbs-Thomson effect and it is modulated by the Γ parameter which accounts for the coupling between the incorporation and the crystallization. The model explained the contradictory experimental observations about the diameter dependence since Γ could reach negative and positive values. Finally, by assuming a maximum of the incorporation velocity, where the diameter dependence was reversed, they could derive an analytical expression for the growth velocity which fitted correctly the experimental results. Recently, Dhalliun et al [71] reported that the behaviour of the thicker nanowires could be due to the existence of an apparent delay in time which can be due either to an increment in the incubation time or an increase in the growth velocity at early growth stages. This delay increase with the diameter so, for

thicker nanowires, is not vanished and must be taking into account. While for thinner nanowires Schmidt's model describes correctly the growth dependence.

1.4.4.2 Density dependent growth rate

Growth rate on nanowires is also affected by the presence of another ones. Different growth velocities have been observed for high density nanowire arrays than for individual nanowires. But, the relation between density and growth rate is not always the same. Depending on the wire-to-wire distance three different regimens have been defined [72]: competitive, synergetic and independent. In competitive regimen, the wires are very close and precursor material is shared between them. By increasing the spacing, the surface collection area of each nanowire can collect more Si species without a competing with neighbouring wires and this results in an increment of the growth velocity. On synergetic regiment, however, nanowires are close but not enough to overlap the surface collection areas and interaction between wires occurs through diffusion Fig 1.9. This means that an increment in the nanowire density will produce diffusion of more Si species with the consequent rate increment. Finally, for independent regimen, nanowires are separated by relatively large distances and diffusion does not occur. Then, a variation in the nanowire distance will not produce any change in the growth rate.

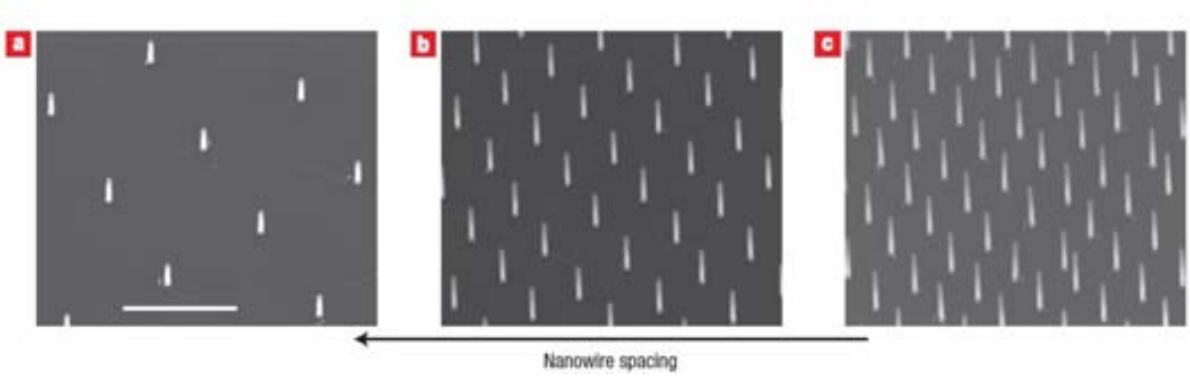


Figure 1.9: SEM image of GaP nanowire patterns. a-c, A nanowire growth rate increase is observed by decreasing wire spacing L from 1000nm (a), to 500nm (b) to 400 nm (c) for a constant nanowire diameter of 25 nm.[72]

In silicon nanowires, the synergetic growth was observed and explained as arising from an increment in the catalyst decomposition of SiH_4 into silynene species SiH_2, which are more reactive species, for higher density arrays [73]. In contrast, the competitive regimen was observed for wires, with diameters in the order of microns [74] that will have larger collection areas.

1.4.5 Conductivity on nanowires

The doping control of nanowires is a critical step for the fabrication of devices. Dopants are shallow level impurities, such as B, P, As Ga, Al or Sb, that acts as donors, in n-type semiconductors, or acceptors, in p-type semiconductors, of charge carriers. In order to become electrically active, the dopants atoms need to be substitutionally incorporated into the Si lattice. The VLS growth mechanism offers several mechanism for doping. During the growth process, impurities can be introduced by some components of the catalytic particle or by an small amount of a gaseous dopant precursor.

Because of the growth conditions, contamination from the catalyst droplet appears on the nanowire. Depending of the seed particle chemical nature, the impurities are not desired for the fabrication of electronic devices. Especially gold contamination on Si nanowires which is known to create a very effective recombination center of Si. But, in other occasions, the catalyst nanoparticle, present impurity levels close to the valence or conduction bands and can be used to dope the nanowires during the growth. In Fig 1.10, are represented ionization energies of materials used for the synthesis of nanowires. The elements close to the Conduction Band, such as Bi, Li, Sb and Te, will produce a n-type doping during the growth. While, elements close to the Valence Band, such Ga, Al and In, will produce a p type doping. Another possibility is to introduce in the seed particle the dopant element. Lieber and co-workers used a Au/P mixture as catalyst [75] for the growth of heavily n-doped Si nanowires.

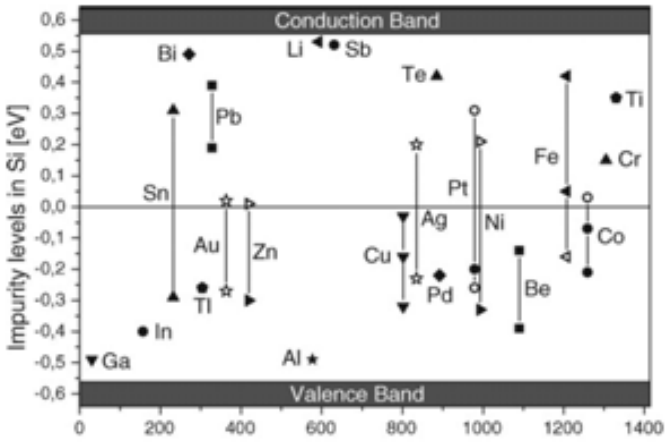


Figure 1.10: Ionization energies of various impurities in Si given with respect to the middle of he bandgap (assuming a Si bandgap of 1.12 eV) as a function of the minimum temperature for the VLS growth.[5]

Other employed method to obtain dopant distributions, which offers more controllability, is the incorporation of an additional precursor gas or vapor during the VLS growth. This method gives the opportunity of tuning the doping level by changing the partial pressure of the doping source. Typical p-doping sources are diborane B_2H_6, trimethylboron TMB for LP-CVD and BBr_3 and BCl_3 for AP-CVD. However, the availability of similar precursor for n-type doping of Si nanowires is more limited. In the 2004 Lieber

and co-workers reported the first example of controlled growth and phosphorous doping of Si nanowires. They used phosphine, PH_3 as gas doping precursor [76].

However, sharp transitions between differently doped nanowire regions, seems hard to achieve experimentally by VLS since the Au/Si droplet might act as a reservoir for the dopant atoms and another growth mechanism, that will be explained in the next section, could be more appropriated for the growth of this kind of heterostrucures. In addition, recent studies about in-situ doped LP-CVD grown Si nanowires have shown no uniform doping profiles [77, 78]. Koren et al.[79] demonstrated that this problem can be solvented by a low temperature post growth annealing or by increasing the H_2 partial pressure.

Finally, to dope nanowires after growth is also possible. Some of these techniques include, ion implantation [80, 81], electrochemical injection [82] or gas phase doping [83]. The ex-situ doping of nanowire, in a different step, simplifies nanowire growth process since in-situ doping can produce modifications in nanowire growth conditions or morphology.

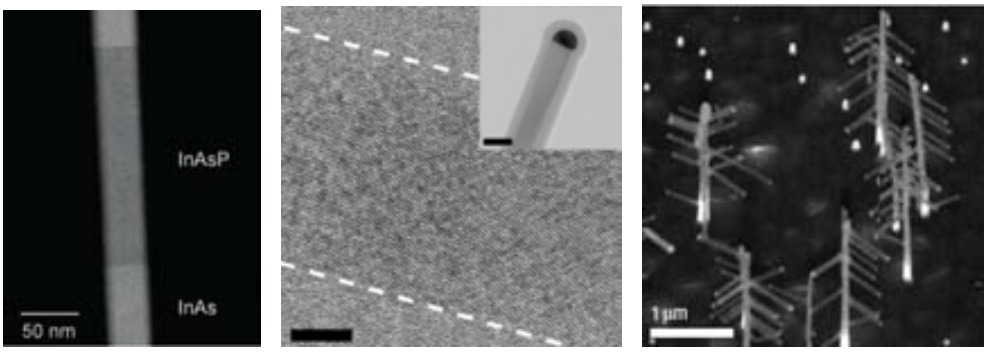
1.5 Fabrication of complex structures based on nanowires

The study of one-dimensional structure has been rapidly grown because of their numerous potential application in multicomponent architectures. The fabrication of these structures can be achieved both, by the bottom-up synthesis of heterostructures or by the integration on complex top down architectures. These two techniques have allowed the fabrication of devices such as field effect transistors, mechanical sensors and photodetectors which present a superior performance than their competitors or even exhibit novel properties.

1.5.1 Fabrication of heterosturctures by bottom up approach

Heterostructures of one dimensional materials offer the same advantages than single-component materials, but with the added benefit of multifunctionality or, new properties arising from combining different materials. Potential applications are nanoscale electronic or optoelectronic devices. Their fabrication is similar to bottom-up simple component materials but including multiples additional steps. These can be formed by a single component or contain a combination of semiconductors, metals, oxides, or other materials. A wide variety of complex heterostructures is reported in the literature[84] but, three can be defined like the most representative: axial, core-shell and branched, Fig 1.11. In many situations, the top down fabrication of similar structures is very challenging to match or even unobtainable.

The synthesis of segmented, or axial nanowire heterostructures, Fig 1.11(a), is performed by introducing two or more precursors in the growth chamber by sequential fashion. The synthesis is favourable if a catalyst nanoparticle is suitable for growth of the different



(a) (b) (c)

Figure 1.11: a) STEM image of axial nanowire heterostructure[85]. b)TEM image of an i-Si/SiO_x/p-Si core -shell nanowire [86]. c) SEM image of nanoscale forest grown in MOVPE [87]

components under similar conditions. Lieber and co-workers found that gold nanoclusters meet this requirement for a wide range of III-V and IV materials [88]. By similar way, nanowires of one component can be synthesized with segmented doping profile by switching between different vapor concentration of dopant[89, 90].

Coaxial or core-shell heteroestructures, Fig 1.11(b), are also formed in two or more step procedures where either the growth parameters or the synthesis methods are changed. Due to the fact that, layer growth onto a surface can be carried out without the impact of a growth seed, the interfaces are grown with high purity and control over the thickness. Different materials can be combined for the formation of core/shell [91] and core/multishell [92] structures. Similar than in segmented nanostructures, the synthesis of coaxial nanowires with different doping levels [86] is possible. These are a promising structure for electronic and photonic applications.

Finally, branched nanowires, Fig 1.11(c) are formed by two consecutive VLS growth process [87, 93]. In a first growth step, usual nanowires are grown. Then, after a second catalyst deposition, nanobranches are grown on sidewalls. These structures are known also as nanotrees or nanobrushes.

1.5.2 Integration on complex architectures

The great variety of nanowires synthesized of different materials and the complex heterostructures explained previously, present potential characteristics for its use in new technologies. Their application in multiples areas, such as electronics, photonics and sensing, has been demonstrated. However, the next step to exploit their real potential, the large scale, high yield device integration is still not completely resolved and more enforces are required in this field.

Common for the bottom-up methods is difficult to implementation into large scale technologies, and so far they have been not used in any commercial devices. Complex

device structures based on nanowires are fabricated by either nanowire grown in a separate substrate and then transfered to a different device substrate or, epitaxially nanowires directly grown in the location and with the morphology and orientation required for the device.

1.5.2.1 Post-growth alignment

The direct epitaxial growth of nanowires on functional devices is not possible in many situations and post-growth alignment mechanism is necessary. A clear example is nanowires that have been grown in solution, by SLS or SFLS mechanism. In other situations, due to the substrate nature, it is necessary to separate the high temperature nanowire growth process from the devices substrate to avoid possible damages. This is the case for example of plastic or glass substrates in which the high temperature process could damage the samples[94, 95, 96]. Nanowires must be transfered to a structure in a postgrowth process with control of the orientation and position for the fabrication of functional devices.

A simple way for self-assembly of nanowires is by electrostatic interactions. Nanostructures with inherent polarizability or modification of the surface to adopt an specific charge can be used to pattern the deposition of charged nanowires. An example is the silicon oxide layer that at neutral pH present a negative surface charge. This surface can be patterned by micro contact printing techniques and amine terminated nanowires [97] can be electrostatically deposited onto not covered surfaces. Other structures, such as ZnO [98] or V_2O_5 [99, 100] nanowires, present an inherent charge and do not need surface modification to be electrostatically deposited.

An interesting approach for the self assembly of nanowires, which offers more control on the nanowire orientation than the simple electrostatic deposition, is the dielectrophoresis. This mechanism is based on the fact that, nanowires in solution can adopt a polarization within an applied field. Diametrically opposed microelectrodes can be used to position the polarized nanowires and form bridge structures. This mechanism can be applied to a large variety of materials, such as metallic [101] or semiconductor nanowires [102] and, has been used for the fabrication of devices like for example transistor [103] or resonators [104] Fig 1.13. The dielectrophoresis has some limitations, such as the need of microelectrode definition to orient nanowires and interactions between close electrodes which can produce some misalignments.

An alternative method based on direct flow assembly was proposed by Lieber [105] and Yang [106] groups at the same time. In this approach, a nanowire solution flows through a microchannel formed between a poly(dimethylsiloxane) PDMS mold and a silicon glass substrate. After solvent evaporation and PDMS removal nanowires present an alignment in the flow direction. This mechanism allows the fabrication of more complex structures by combining sequential flows of nanowire solutions and the formation of heterostructures by changing the nanowires suspended into the solution. However, large scale fabrication of structures becomes complicated.

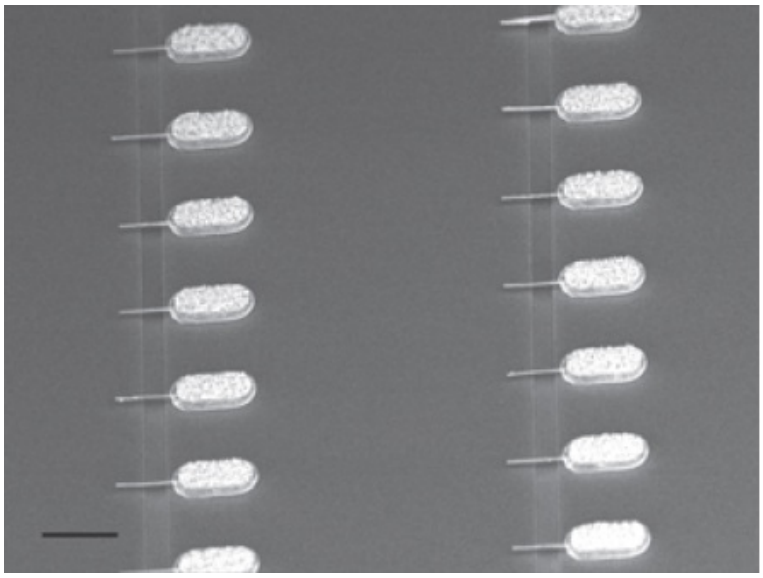


Figure 1.12: SEM image of large area Si nanowire resonators assembled by dielectrophoresis mechanism [104]

For large area and mass fabrication of building blocks an alternative method was proposed by the same two groups [107, 108]. This approach is based on the Langmuir-Blodget assembly technique. A colloidal suspension of nanowires-surfactant is spread onto a water surface forming a monolayer. Under a determined range of uniaxial compression nanowires are aligned along their long axis. The nanowire-to-nanowire distance is controlled by the compression process from the nanometer to micrometer scale. Then, the ordered nanowires are transferred in a single step to the substrate yielding parallel nanowires that cover the entire substrate in the centimeter scale. In addition, this mechanism allows the deposition of sequential nanowire layers with different nanowire orientation or composition to form more complex structures. A selective deposition is also possible by removing a sacrificial layer once transferred the nanowires [108]. This mechanism has been explored for the fabrication of ultra-high density nanowires arrays with nanometer spacing in the micrometer scale [109].

1.5.2.2 In situ alignment

While the post-growth assembly techniques looks to have advanced impressively towards achieving large scale nanowire device integration, the integration problems of epitaxially grown semiconductors nanowires are already not completely resolved. Most nanowires devices are limited to the demonstration of single device, not adequate for production on large scale at low cost. However, direct integration of nanowires into devices on desired locations present important advantages over the transfer methods and advances in this field are continuously emerging. First, transfer media, which usually is a liquid, could produce contamination problems especially when the surface cleanness are critical for device performance, such as on detectors and sensors. And, on the other hand, if a substrate with the correct lattice match is chosen, nanowire can be grown either horizontally or

vertically presenting better alignment than transferred nanowires.

1.5.2.3 Vertical aligned nanowires

A simple strategy for the fabrication of nanowire devices is the growth of vertical aligned silicon nanowires. For that, the substrate crystallographic orientation must be perpendicular to the growth direction. By using this approach, the fabrication of device based on nanowire arrays and single nanowires has been demonstrated.

Vertical aligned dense nanowire arrays has been used for the fabrication of devices such as nanolasers[110], light-emitting diodes (LEDs)[111], energy storage[112] and solar cells[113]. In these kind of devices the precise control of the nanowire position is not the critical step. However, devices like LEDs can improve their applications by controlling density and position in high performance devices such as high resolution electronic displays, optical interconnect and high density data storage. In this way, Xu et al used a conjuntion of low temperature wet chemical methods and EBL [114]. They also proposed to replace the expensive EBL by more convenient and low cost patterning techniques, such as nanosphere photolithograpy.

Controlling density, position, and arrangement of nanowires is of great interest for most applications on large scale fabrication of single vertical nanowire devices. VLS nanowires will copy the pattern of seed nanoparticles so precise low cost deposition techniques are needed. Some of the deposition techniques described previously, such as EBL, nanosphere and nanoimprint lithography and nanoporous mask patterning allows an ordered deposition. Combining these techniques and VLS growth the diameter, height, orientation and position of the nanowire can be simultaneously controlled.

A demonstrative device using highly ordered vertical nanowires is the nanowire vertical surround-gate field-effect transistor (VSG-FET). In this kind of devices, the transistor gate is wrapped around the vertical aligned nanowire and the substrate acts as a drain. Its fabrication was first reported by Ng and co-workers [115] by using gold nanoparticles deposited by e-beam lithography for the growth of ZnO nanowires over a heavily doped SiC substrate. This two materials present a very small lattice mismatch so epitaxial vertical nanowires were grown. A similar fabrication scheme was used by Schmidt and co-worker [116] by using homoepitaxially grown Si nanowires. Although VGS-FETs presented a superior performance over conventional FETs their fabrication was limited only for single device demonstration. One of the problems was the presence of underlying semiconducting substrate which precludes electrical isolation and individual addressability of single nanowires. To solve this problem, Dayeh and co-workers [117] proposed and interesting approach for large scale applications. They used a layer transfer technique, commonly used for the fabrication of Silicon on insulator (SOI) wafers, that combines hydrogen ion implantation and wafer bonding, known as ion-cut or Smart cut process. As result an ordered, vertical and electrically isolated InAs nanowire array was obtained. The technique can be extended to the different semiconductors materials and would allow

the realization of individually addressable, high density VGS-FET arrays suitable for 3D circuit applications.

1.5.2.4 Horizontally aligned nanowires

In contrast to vertically aligned nanowire, the horizontal growth presents more difficulties and has been less studied. In this case, the seed nanoparticle have to be deposited onto a vertical wall which introduces additional complications. Nevertheless, the direct epitaxial growth of horizontal nanowires on desired location reaches important advantages with respect to the transferred nanowires. For instance, their mechanically rigid clamps[118] together with the low nanowire-substrate contact resistance[119] have important advances for the fabrication of nanoelectromechanical systems (NEMS).

The epitaxial growth of horizontal nanowires form interconnects without the need of additional fabrication process. This means that, if a catalytic particle is deposited on the sidewall of a prefabricated trench, the nanowire growth from one side to the opposite one forming double clamped nanobeams. This growth mechanism was first demonstrated for the growth of GaAs nanowhiskers [120] and posteriorly extended to other materials. In the case of Si nanowires Islam and co-workers [30] demonstrated the growth of high density $\langle 111 \rangle$ Si bridging nanowires on $\{110\}$ Si substrate. However, the bottom part of the wafer was still conductive shortcuting the nanowires. This was efficiently solved by using a SOI wafer with a Si device layer oriented in the $\{110\}$ direction. The trench is then etched into the SOI until reaching the buried insulator layer. The nanowire connects two isolated electrodes and can be used to build a sensor system.

The horizontal growth of nanowires is also possible in a different crystallographic orientation than that defined by the nanoparticle and growth conditions. Quitoriano and co-workers [121] developed a fabrication technique in which the horizontal growth was guided by the presence of an oxide layer. By this technique, the fabrication of a top-gated MOSFET was demonstrated.

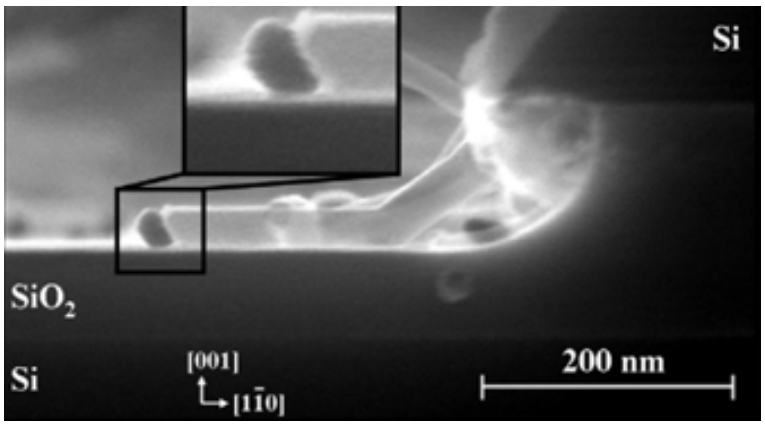


Figure 1.13: Cross sectional SEM shows a nanowire growing against the BOX [121]

A possible alternative for low cost device fabrication that, will be analysed in next sections could be the galvanic displacement to deposit gold nanoparticles. It was proposed by San Paulo and co-workers [122] for the fabrication of nanowire arrays with control of the position, density and diameter but, until the moment, it has not been exploited for device fabrication. This technique will be studied in more detail in next chapter.

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Chapter 2

Optimizing Si nanowire growth via the VLS growth mechanism

Contents

2.1 Introduction and objectives **41**

2.2 Catalyst deposition via galvanic displacement **42**

2.2.1 Galvanic displacement optimization for the synthesis of high density Si nanowire arrays 42

2.2.2 Galvanic displacement optimization for the synthesis of single nanowire 45

2.3 Silicon nanowire growth optimization **46**

2.4 Doping of Si nanowires **51**

2.5 Conclusions **53**

References **55**

2.1 Introduction and objectives

The ability to control nanowire size and location during the growth is highly desirable from the design and manufacturing perspective. Indeed, if nanowire growth and assembly is combined in a single step, subsequent fabrication processes are facilitated by the epitaxial nature of nanowire-surface interface, which implies good electrical[1] as well as mechanical[2] contacts between nanowire and substrate.

Nanowire diameters synthesized by VLS mechanism are large determined by the size of metal clusters that serves as nucleation sites[3]. Then, the key step for the large scale integration of nanowires into functional devices is the control of catalyst dimensions and location. In the previous chapter, a great variety of techniques to deposit catalyst gold for the growth of Si nanowires were described. However, there are still problems to simultaneously achieve a precise control of catalyst dimensions and position. From the described methods, probably lithographic deposition techniques offer the best control over catalyst deposition, nevertheless, most of these patterning strategies result highly time consuming to be adapted to large scale integration or may not be easily applied to substrates with varied topography (i.e. non planar).

Chemical deposition via galvanic displacement could be an alternative for the selective deposition of gold catalyst, specially for the growth of horizontally aligned nanowires. This technique was proposed for the deposition of catalyst with control of location and diameter for both nanowire arrays[4, 5] and individual nanowires[6]. However, their use for the integration on functional devices has not been exploited. For that, an improvement on the deposition condition and patterning techniques to defined deposition areas is needed. In this chapter, we will optimize the galvanic deposition of gold catalyst for the growth of both high density nanowire arrays and individual silicon nanowires. In the following chapters, these deposition conditions will be then applied for the fabrication of functional devices in which nanowire size, position and/or location are critical for device performance.

After catalyst deposition optimization, we will analyse the conditions for the growth of silicon nanowires in our CVD system. We found that nanowire growth conditions are dependent of the sample characteristics which imposes important difficulties for optimizing the growth process. On the other hand, the ability to incorporate dopants into nanowires is important for a variety of device applications. For this reason, the CVD system has been equipped with an extra gas line to dope nanowires with boron during the growth. Additionally, we have studied a new method to ex-situ dope nanowires after the growth. As it will be explained, this process has many advantages compared with the simultaneous growth/doping of nanowires which introduces more variables to the nanowire growth and makes more difficult the optimization of the growth conditions.

2.2 Catalyst deposition via galvanic displacement

2.2.1 Galvanic displacement optimization for the synthesis of high density Si nanowire arrays

Electroless deposition techniques are frequently used to deposit thin films of different metals. A deposited gold thin film could be simply used to catalyse Si nanowire growth. However, the simultaneous control of density and diameter from annealed thin films results complicated. On the other hand, the use of gold nanoparticles deposited by galvanic displacement could give us a better control over deposition characteristics.

Gold nanoparticle catalyst deposition from reverse micelle microemulsions via galvanic displacement gives the possibility of controlling the location and diameter[7]. A microemulsion is made by mixing two solutions. The first one, the organic solution, is prepared by dissolving 0.33M of surfactant 2-sulfonate sodium bis(2-ethylhexyl) sulfosuccinate (commonly knew as Aerosol-OT or AOT) in n-heptane. The other one, the plating solution is obtained by adding 0.02M of potassium tetrachloraurate, $KAuCl_4$, and 0.2 M of hydrofluoric acid, HF, in deionized water. Then, after 30 min of sonication the micelle microemulsion is formed.

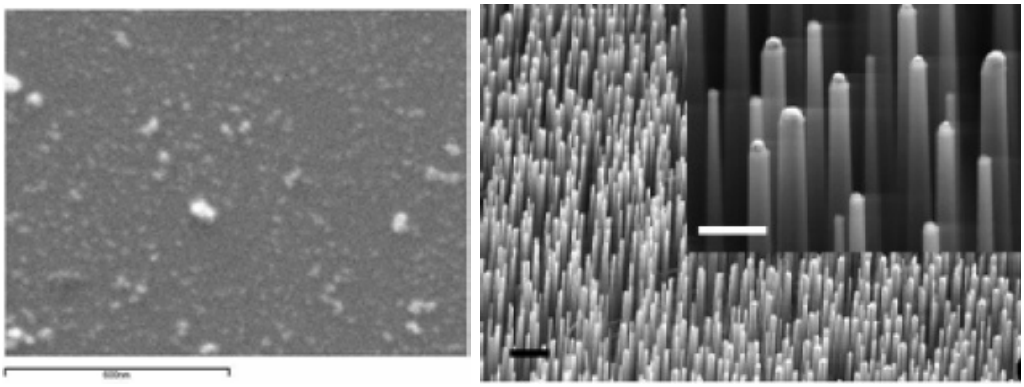
The micelle radius, R_m, is known to be proportional to the micellar parameter which is defined as the ratio between water and surfactant molecules ($R = N_{H_2O}/N_{AOT}$). For this kind of micelles, Magagnin et al found that the size followed the next expression[7]:

$$R_m\,(nm) = 0.175R + 1.5 \tag{2.1}$$

Gold deposition is produced by immersing the growth substrates on microemulsion. The Substrates are previously patterned with a mask of oxide, nitride or some polymers to define the deposition areas. Gold clusters are deposited by collision of micelles on the exposed silicon surfaces. Metal ions are spontaneously reduced by electrons provided through oxidation of the underlying substrate according to the two half-cell reaction:

$$\begin{aligned} &\text{Anodic:} && Si + 6F^- \rightarrow SiF_6^{2-} + 4e^- \\ &\text{Cathodic:} && Au^{3+} + 3e^- \rightarrow Au \end{aligned} \tag{2.2}$$

Gold nanoparticles deposited by this method presented two main characteristics. First, the diameter of the resulting gold nanoclusters is directly proportional to the diameter of micelles. And, on the other hand, nanoparticle diameter does not depend on the immersion time which means that density could be controlled by changing deposition time. However, analysing results from previous works, Fig 2.1, it can be observed observe that despite cluster/nanowire diameter is effectively determined by the micellar parameter, R_m,

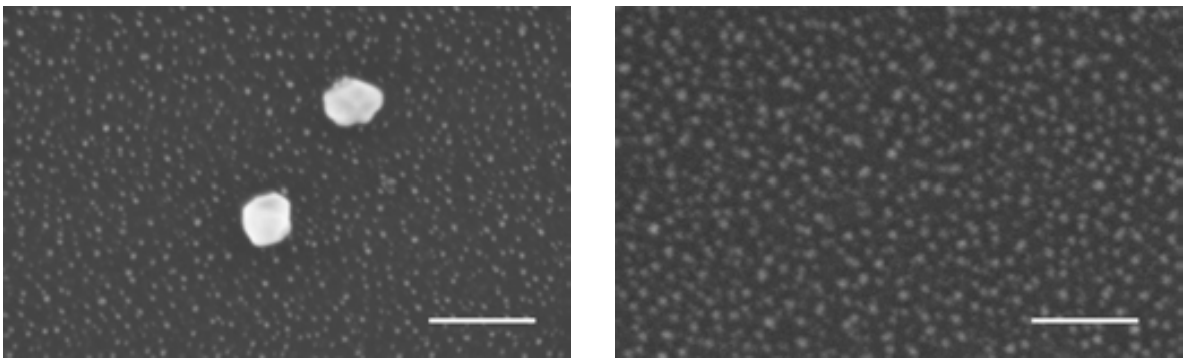


(a) (b)

Figure 2.1: Previous works about galvanic displacement from microemulsions.a) SEM image of Au clusters on silicon deposited by galvanic displacement by immersion into microemulsion with R=50[7] b) SEM image(with inset of close-up image) of vertical aligned Si nanowire array grown from Au clusters deposited on Si (111) substrate by galvanic displacement R=200[4]. Scale bar 300 nm

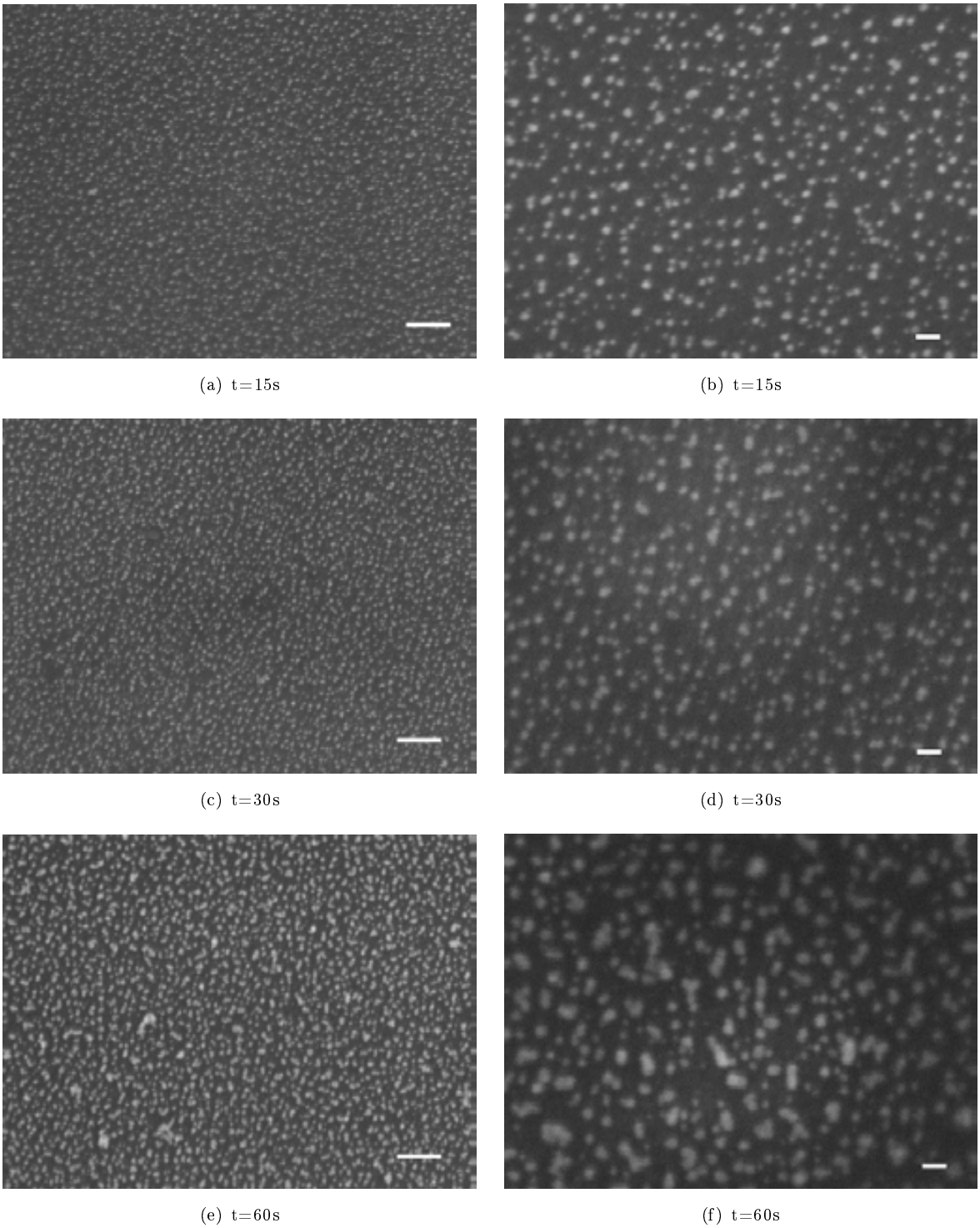
for a wide range of values[7, 4], there is not a very uniform distribution. A phenomenon that could increase the formation of big deposited big clusters is the flocculation. This is defined as a process of contact and adhesion whereby the particles of dispersion form larger-size clusters. Low temperature or longer times after micelles formation will promote flocculation.

In order to improve the homogeneity of deposited nanoclusters, we have studied the effect of the temperature. For that, micelles with R=20 were deposited on clean Si surfaces just after ultrasonic mixing at different temperatures. In the first experiment, bath temperature was hold at $20°C$ while in the second one the temperature was increased to $50°C$. As result an increase in the nanoparticle homogeneity was clearly observed for heated solution. In the colder case, we observed a bimodal distribution of nanoparticles comprised of small particles with a diameter of a few nm together with larger particles of around 100 nm. This cluster agglomeration was not observed in the case of the microemulsion heated to 50°C, where a very uniform distribution of clusters of a few nanometers was observed.



(a) $T = 20°C$ (b) $T = 50°C$

Figure 2.2: SEM image of gold clusters on silicon surface after immersion into a microemulsion with R=20 for 15s at different temperatures. Scale bar 100nm



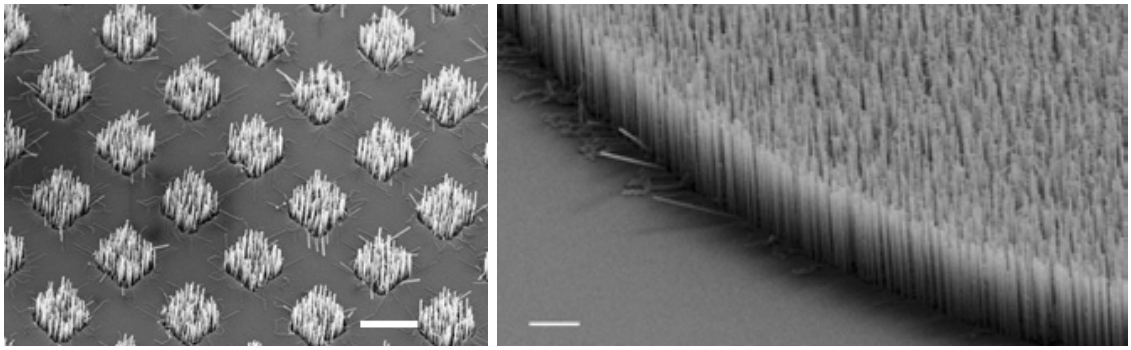
(a) t=15s (b) t=15s

(c) t=30s (d) t=30s

(e) t=60s (f) t=60s

Figure 2.3: SEM image of gold clusters on silicon after immersion into a microemulsion with R=20 for 15s (a) and (b), 30s (c) and (d) and 60 s (e) and (f). Scale bar 100nm in (a), (c) and (e) and 20 nm in (b), (d) and (f).

On the other hand, we have studied the effect of deposition time in cluster aggregation, Fig 2.3. In theory, density of nanoparticles could be controlled by changing deposition time. We have observed this behaviour and only for longer deposition times we observed the formation of larger aggregates which produce a poor uniformity and decrement of



(a) (b)

Figure 2.4: SEM images of nanowire growth in patterned substrates. {111} Si substrates where covered with 200nm of thermal oxide and then Si areas were exposed by a lithography and a dry etching step. Scale bar $2\mu m$

nanoparticle density. In the example shown in Fig 2.3, gold nanoparticles has been deposited by immersing substrate in a micellar microemulsion with R=20 during 15, 30 and 60s. For low time deposition, 15 s, a very high density nanoparticle distribution is formed. Nanoparticle density is of around 3000 per micron square while the mean diameter is around 5 nm. When deposition time is increased to 30s, nanoparticle density is increased and even nanoparticle diameter start to growth due to agglomeration. Finally, when deposition time reach to 60s, nanoparticle density decrease considerabily, up to $2400\mu m^{-2}$, and a large diameter distribution is observed.

After gold deposition optimization, substrates are introduced in the CVD to grow nanowires. For this process, samples are heated at temperatures higher than the eutectic point. Then, silicon is incorporated to the droplet producing a phase change to liquid which favours deposited clusters movement. As consequence small nanoparticles merge to form larger ones which will define the final nanowire diameter. As example nanoparticles showed in Fig 2.2(a) will produce a nanowire array of around 25 nanowires per micron square and with a uniform diameter of around 50 nm.

2.2.2 Galvanic displacement optimization for the synthesis of single nanowire

When, dimensions of defined deposition areas are in the submicron scale, one single nanowire can be obtained in each site if the deposited Au is previously annealed so that merges into a single nanoparticle. Upon annealing the gold film at temperature above the eutectic temperature ($363°C$), silicon from substrate will diffuse into the gold layer, producing a liquid Au/Si alloy. In order to reduce its total surface and interface energy, the Au/Si film breaks up into a distribution of Au/Si droplets. Then, due to the thermal annealing temperature, small clusters, will tend to form larger ones by sintering process. This process will be governed by two main mechanisms: coalescence and Ostwald rippening. Coalescence occurs when two particles are in contact and merge to form one larger reducing the interfacial energy of the system. In contrast, Ostwald ripenning occurs by

removal of atoms from smaller particles and transfer to larger ones.

Bechelany et al.[8] studied the organization, morphology and crystallinity of nanoparticles in different atmospheres and annealing temperatures of Au thin layers deposited by sputtering through polystyrene nanosphere shadow mask. They observed that, under annealing of $1000°C$ in atmosphere of N_2, Ar or Air, during 2 hours nanoparticles merged into a center nanodot.

In our case we have used a gold thin film deposited by dipping into an aqueous solution of 5 M of HF and $5\mu M$ of $KAuCl_4$ for 10-30s. Gold is deposited by galvanic displacement only in Si areas, with size lower than $1\mu m^2$, that have been previously defined by a combination of standard micro-fabrication steps. Then, samples are annealed in Ar atmosphere inside the CVD chamber forming a single nanoparticle in each predefined small area. Finally, this nanoparticle will be used to catalyze the nanowire growth.

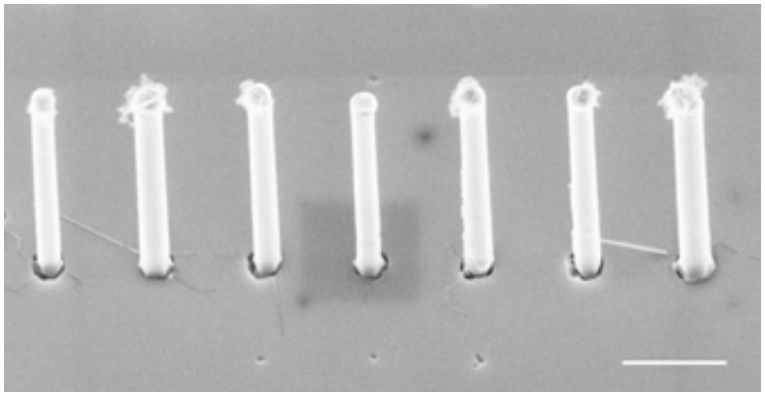


Figure 2.5: SEM image of individual nanowires catalyzed by galvanic displacement thin film. Scale bar $2\mu m$

This method has been used for the synthesis of both vertical and horizontally oriented nanowires. In the case of vertical aligned nanowires exposed Si areas for gold deposition are limited by the resolution of lithography technique used. In our case, as we are interested in a large scale integration of nanowires, we have used optical lithography which is limited to $0.7\mu m$. On the other hand, in the case of horizontally aligned nanowires deposition areas can be reduced by a combination of oxidation and etching steps that we explained in chapter 4.

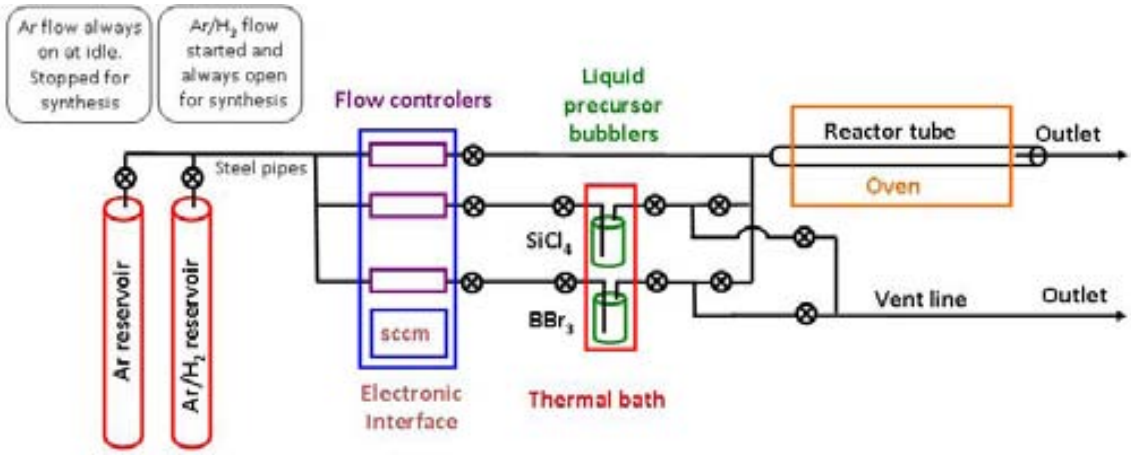
2.3 Silicon nanowire growth optimization

Silicon nanowires are grown in an atmospheric pressure CVD system (AP-CVD) via vapor-liquid-solid (VLS) mechanism. The CVD image and flow diagram is shown in Fig 2.6. The silicon precursor employed in our system is Silicon tetrachloride, $SiCl_4$, which is held at liquid phase in a bubbler at $0°C$ to maintain a low constant vapour pressure. A direct flow of Ar is continuously injected to the reactor tube to avoid that oxygen or humidity can contaminate the system. During the growth, the flow is switched to a mix

of %10 of H_2 in Ar which is used as both the reaction gas, directly injected to the reactor tube, and the carrier gas, through the precursor bubbler carrying the vapour molecules to the reactor where the silicon substrate is heated at growth temperature after catalyst deposition. At the Au/Si liquid droplet surface precursor molecules react with the H_2 by the next chemical reaction:

$$SiCl_4(g) + 2H_2(g) \rightleftarrows Si(s) + 4HCl(g)$$

(a) (b)



(c)

Figure 2.6: CVD system for nanowire growth

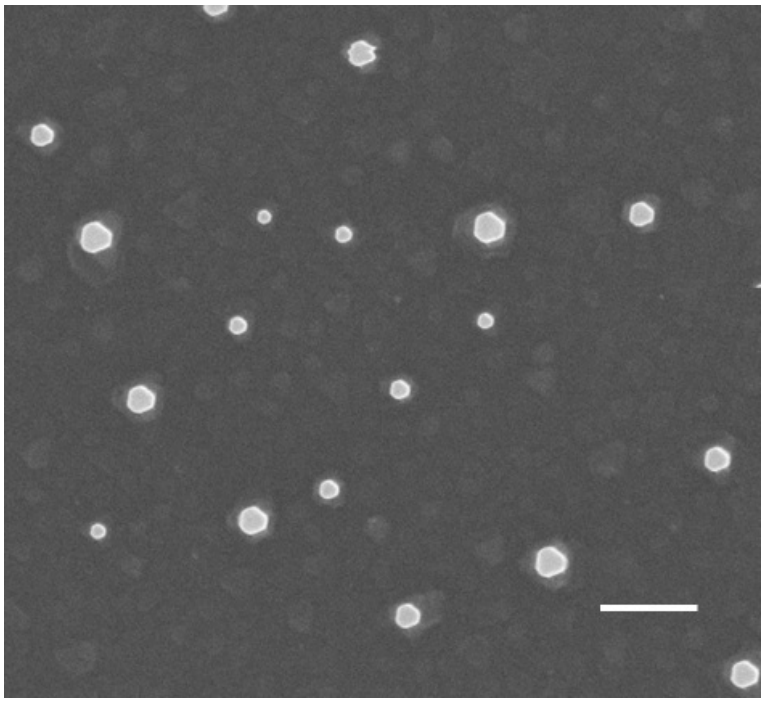
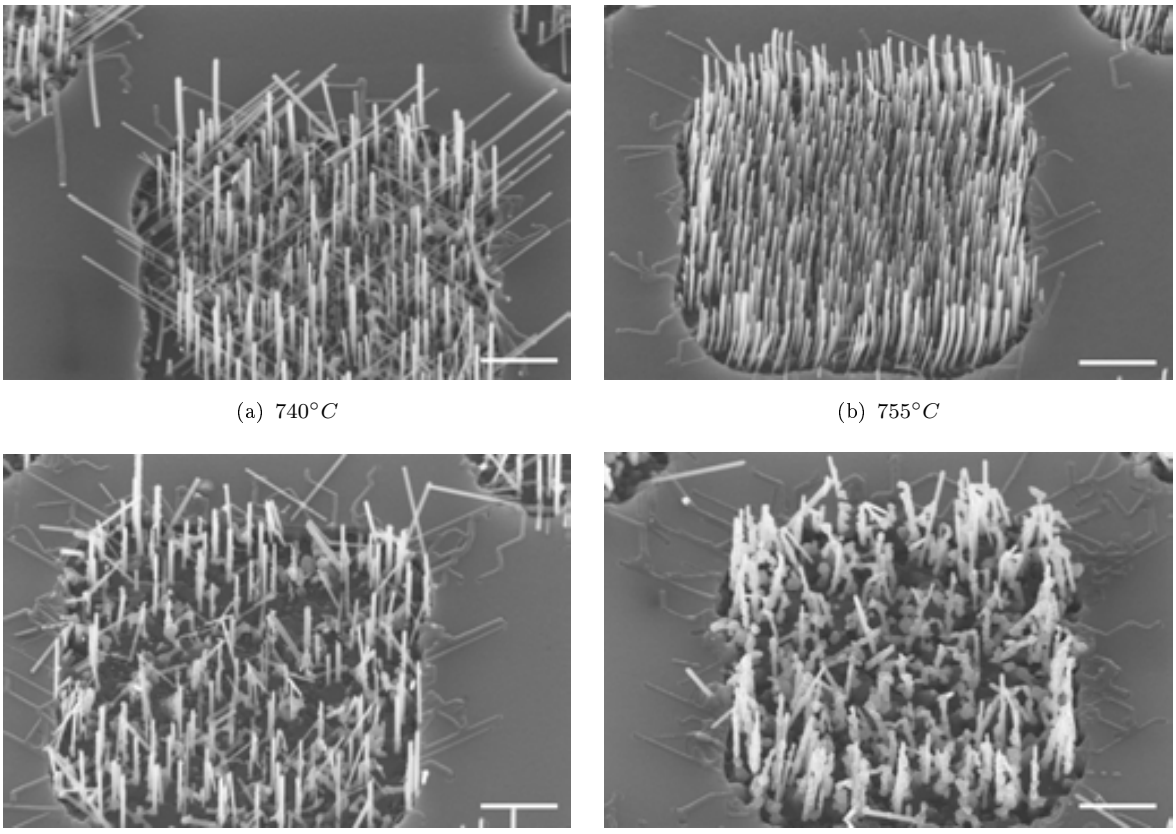


Figure 2.7: Cross section of ⟨111⟩ oriented nanowires. Scale bar 500 nm

The Gibbs free energy of this reaction is positive up to 1550°C [9] so this means that, for the range of growth temperatures, it is not produced. Only in the proximities of the catalytic gold surface the precursor molecules crack and solid Si is produced for the nanowires growth. Also Clorhidric Acid HCl is formed during as the by-product of the reaction. As it was explained in the previous chapter, the presence of the HCl in the synthesis have important advantages respect to the nanowire epitaxy and morphology but an excess of this gas could produce damage at the nanowire surface and it must be taking into account for the parameter optimization.

Nanowire grown in the CVD presented ⟨111⟩ crystallographic orientation as it is expected for the range of diameters, between 25 nm and several hundreds of nanometer. Cross section is enclosed by six {112} planes forming an irregular hexagonal cross section. A top view of nanowire is shown in the Fig 2.7.

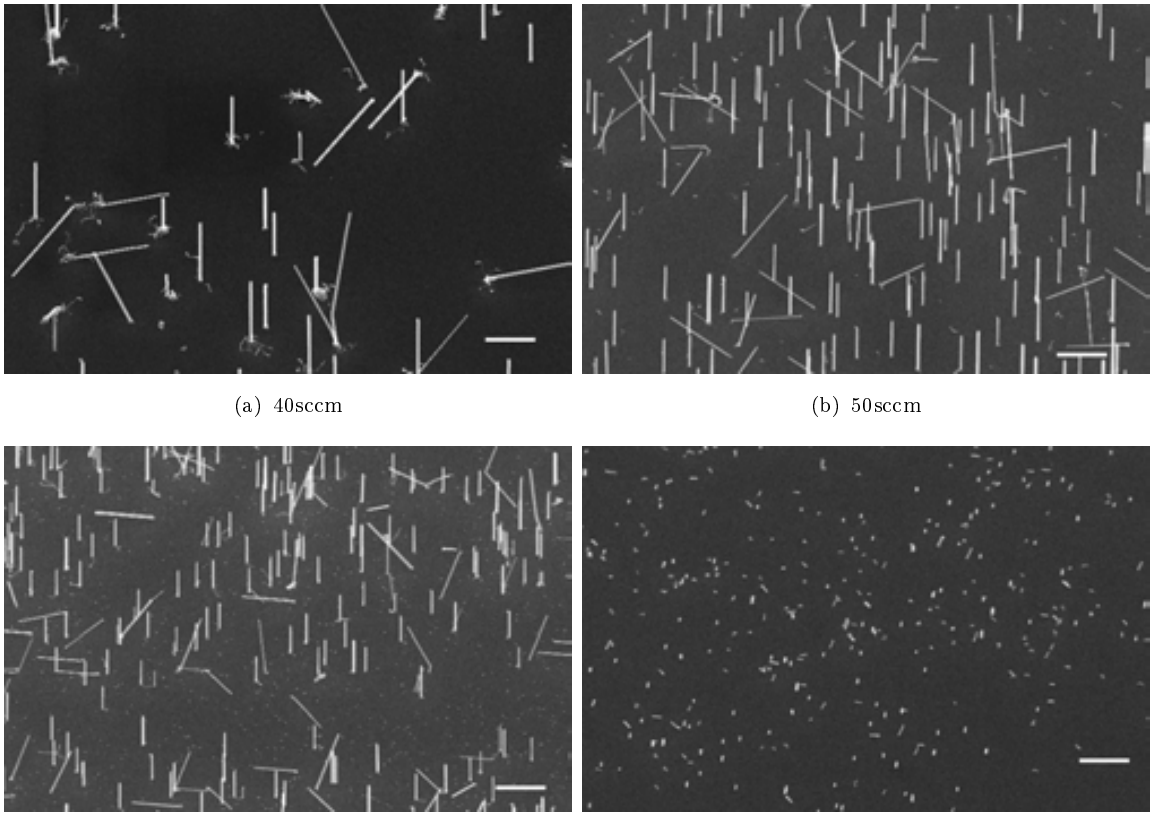
In our optimization process we found a narrow temperature window for the synthesis of well-ordered silicon nanowire arrays. In this case, by following a defined galvanic displacement procedure, four different growth temperatures were tested while keeping the other growth conditions constant, Fig 2.8. Substrate are oriented in the ⟨111⟩ so, at optimal growth conditions, in this case 755°C nanowire growth direction is perpendicular to the substrate surface. We can observe that with a variation of 15°C in growth temperature nanowire growth change from a very well ordered vertically aligned nanowire array to a low density completely amorphous whisker array. On the other hand, when temperature is decreased the same amount we found the other two ⟨111⟩ no perpendicular to the surface.



(a) $740°C$ (b) $755°C$

(c) $770°C$ (d) $800°C$

Figure 2.8: SEM image silicon nanowire growth at different growth temperatures. Scale bar $1\mu m$



(a) 40sccm (b) 50sccm

(c) 60sccm (d) 70sccm

Figure 2.9: Influence of precursor carrier gas flow in the growth of silicon nanowires. Direct flow is 270sccm and growth temperature 800°C

An extra difficulty in the growth condition optimization was the dependence of the sample characteristics. While for nanowire catalysed from colloidal nanoparticles, which usually produces a relatively low density arrays, or single nanowires grown by galvanic displacement technique, the optimum growth temperature was in the range of 800°C, however, it decreases to 755°C for high density nanowire arrays catalysed from galvanic displacement deposited nanoparticles or even lower temperatures for samples in which beside gold catalyst there is extra metal in pads for electrical characterization (such as Tungsten which is compatible with the high growth temperatures).

In general, an decrease in the growth temperature is observed when the amount of metal in the sample is increased. When metal nanoparticle are distributed forming dense arrays, it produces an increment in the available silicon species or reaction intermediate products to synthesized nanowires, enhances by the inter-diffusion among neighbours. For low nanowire density, however, the concentration gradient around each wire is more abrupt and there is not inter diffussion between nanowires. Then the available silicon species, for a given temperature, is lower for low density arrays. It can be compensated by increasing the synthesis temperature and then the reactivity of species inside CVD.

The influence of the amount of precursor gas in the reaction has been also studied. In the case showed in the Fig 2.9, the optimum carrier gas flow is 50sccm (standard cubic

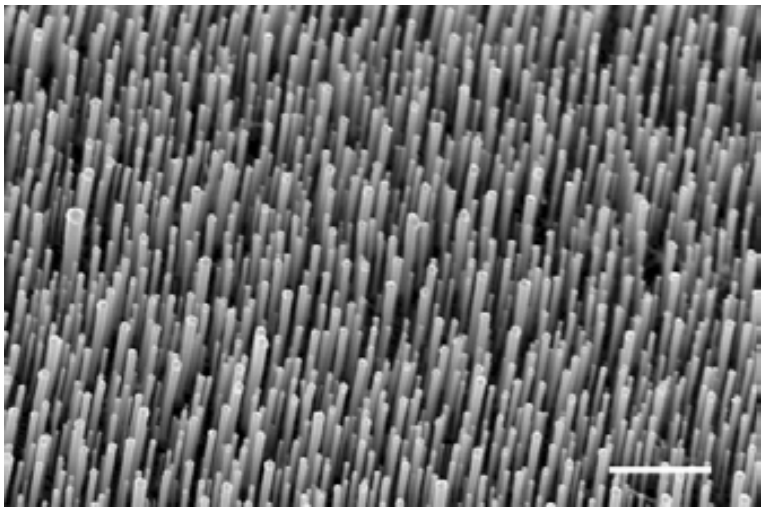


Figure 2.10: SEM image of a nanowire array catalysed by galvanic displacement deposited gold nanoclusters (R=20, t=120s). Nanowires with larger diameter present higher growth rate than nanowires with smaller diameters. Scale bar $1\mu m$

centimeter) but, as in the case of the temperature, this value can fluctuate depending of the sample characteristics but is typically between 50 and 40 sccm. At low $SiCl_4$ concentration we observed some amorphous growth at the base of the nanowire. Changing carrier gas flow we change not only the available amount of Si atoms for the growth but also the HCl that, as it was explained in the previous chapter, avoid the gold diffusion of gold atoms and the vapour solid growth of nanowires. Gold diffusion during the first stages of growth can produce the growth of this amorphous small nanowires at the base. In the case of high $SiCl_4$ concentration, 60 sccm, we observed a slower growth rate and even the growth was inhibited in many catalyst nanoparticles. If the precursor is increased more then nanowire growth is completelly inhibited due to the excess of HCl.

The growth rate is also dependent of the sample characteristics and growth conditions. The mean velocity is around $1\mu m/min$ but it can varies between around $250nm/min$ to $2\mu m/min$. As growth conditions change for different densities or sample characteristics results complicated to stablish a clear dependence of growth rate. However comparing nanowires with different diameters in the same sample, we can observe a dependence of nanowire growth rate. In Fig 2.10 nanowires were catalysed from gold nanoparticles deposited by galvanic displacement. We used a long deposition time, 2 min, so then nanowire array have a wide diameter distribution, between 30 and 200nm. We observed than nanowires with large diameter grew faster than nanowires with small diameters. This behaviour is in agreement with reported works that has been described in the previous section.

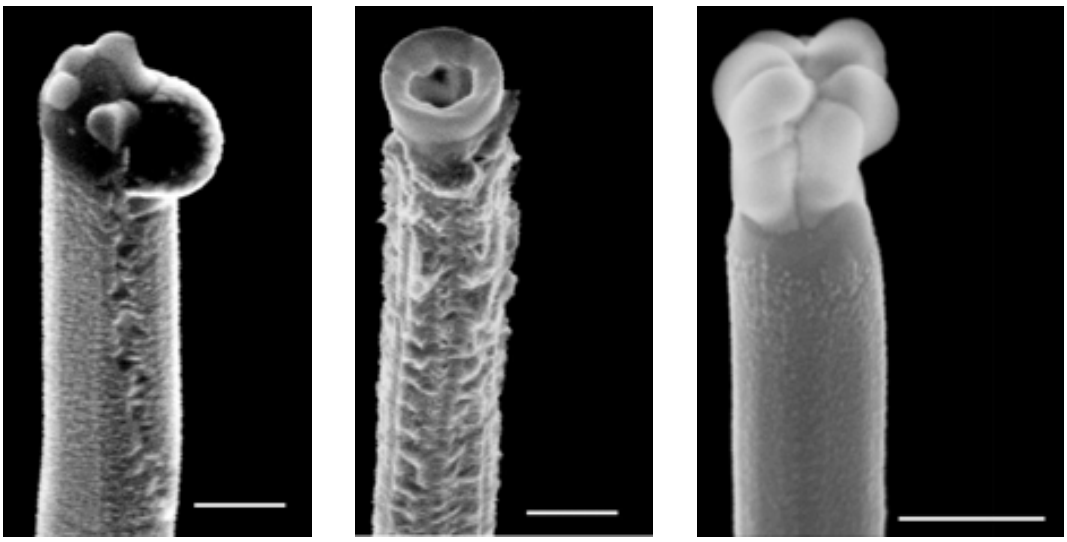
2.4 Doping of Si nanowires

An important issue for different device applications is the control of nanowire resistivity. With this objective, the CVD system was equipped with an extra gas line for the dopant

precursor, Fig 2.6. A small flow of Ar/H_2 is passed through a bubbler containing liquid boron tribromide, BBr_3, carrying vapour molecules to the furniture chamber during the nanowire growth. The dopant precursor is held at $0°C$ in a thermostat bath in order to have a constant low vapour pressure. As it was commented in previous chapter, dopant precursor molecules are cracked at catalyst droplet surface by next reaction.

$$BBr_3 + \frac{3}{2}H_2 \longleftrightarrow B + 3HBr \tag{2.3}$$

Then boron atoms are incorporated to nanowire producing bromide acid as by-product. The incorporation of boron atoms to the catalyst nanodroplet together with the action of acid produced during the reaction have negative effects on nanowire morphology. This effect has been observed on nanowires synthesized in our CVD system. While nanowires without doping, Fig 2.11(a), present a relatively smooth surface, nanowires in which dopant source is present during the growth can present a surface roughness increment. Initially, the mass flow installed to control the volume of carrier gas presented a full scale of 200sccm which allows. The MFC can be given a set point from 0 to 100 per cent of its full scale range but, it is typically operated in the 10 to 90 per cent of the full scale where the best accuracy is achieved. Then, in this case the minimum accuracy flow will be 20 sccm which produces not only a very high doping level but also a considerable increase of nanowire roughness, Fig 2.11(b). Smaller flows could be used but, it made difficult the reproducibility due to fluctuations in the dopant carrier gas flow. Posteriorly, the MFC for dopant source was replaced for another with a full scale of only 10 sccm which allows to control gas flows as small as 1 sccm. The nanowire surface was also characterized for nanowires grown with smaller dopant flows and we do not observed an important increase of roughness compared to intrinsic nanowires, Fig 2.11(c).



(a) (b) (c)

Figure 2.11: SEM image of nanowires with different doping levels. (a) Intrinsic nanowire; (b) Nanowire doped by using the initial nanowire. The dopant carrier gas 20sccm; (c) Nanowire doped after dopant mass flow modification. Dopant carrier gas 1sccm. The scale bar is 300 nm in the three images.

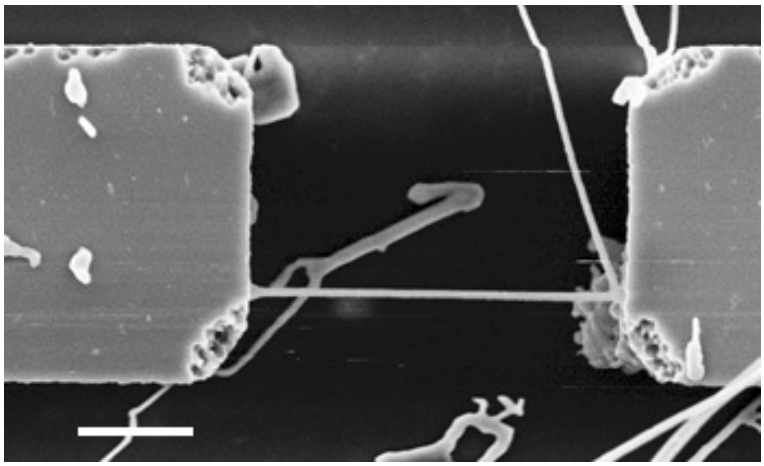


Figure 2.12: SEM image of a ex-situ doped nanowire. The nanowire resistance is $50k\Omega$. Scale bar $1\mu m$.

An alternative method for doping silicon nanowires was also used. Nanowires were doped in a post-growth process by diffusion of Boron attoms from a solid source. We used a chip extracted from a Boron Nitride wafer (BN-1250 from PDS products). This kind of source is frequently used to dope Si wafers by diffusion of boron atoms from donor wafer to process wafer are annealed in a N_2 atmosphere. Doping level will be determined by the annealing temperature, that for these wafers are in the range of $1000 - 1250°C$ and the time.

The use of a ex-situ doping process have important advantages. In-situ doping of nanowires can affect to the growth conditions of nanowire which makes more difficult the process optimization. On the other hand, as it has been shown, the in-situ doping can affect to the nanowire morphology. However, in nanowires, the surface to volume ratio increases and lower temperatures are needed for the process. An extra tube was chosen for the CVD to dope Si nanowire. The dopant chip was place over the nanowire sample at a distance of 1 mm and introduced inside the CVD tube at a temperature of $800 - 900°C$ with a N_2 direct flow of 50sccm. Then the reactor temperature is risen up at $1000°C$ and lower at the initial temperature with a rate of $5°C$ per minute. The initial temperature is chosen in function of the desired doping level. Results are repetitive but again depend of the sample characteristics and a more detailed studied is required to control the process. An example of doped nanowire is shown in the Fig 2.12.

2.5 Conclusions

In this chapter the process for the catalyst deposition, nanowire growth and doping has been described. Galvanic displacement technique has been used to selectively deposit gold catalyst for the growth of high density Si nanowire arrays and individual nanowires. In the case of high density arrays, we have improve the deposition condition of gold nanoparticles from micellar microemulsions that allows us to have more control over nanowire dimension and density. For the growth of single nanowire, however, we have used the deposition via

galvanic displacement of thin gold film on predefined areas that typically have dimensions lower than $1\mu m^2$. After an annealing process the deposited gold film will produce a single nanoparticle that will be used for the synthesis of a single nanowire.

After catalyst deposition optimization, we have described the CVD growth process and doping. We have described the effects of temperature and precursor flow. However, optimal growth conditions are dependent of samples characteristics and an this has complicated the process. Finally, the process was optimized for the different devices that will be fabricated for the thesis.

The CVD reactor also presented an extra line for the nanowire doping. The process of doping can affect negatively to the nanowire morphology. In order to solve this inconvenient the mass flow controller was replaced for more accurate one. On the other hand, an alternative method has been presented for ex-situ dope nanowire that present important advantages such as make synthesis and doping process independent.

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Chapter 3

Application of Si nanowire array fabrication technologies: Piezoresistive Cantilever

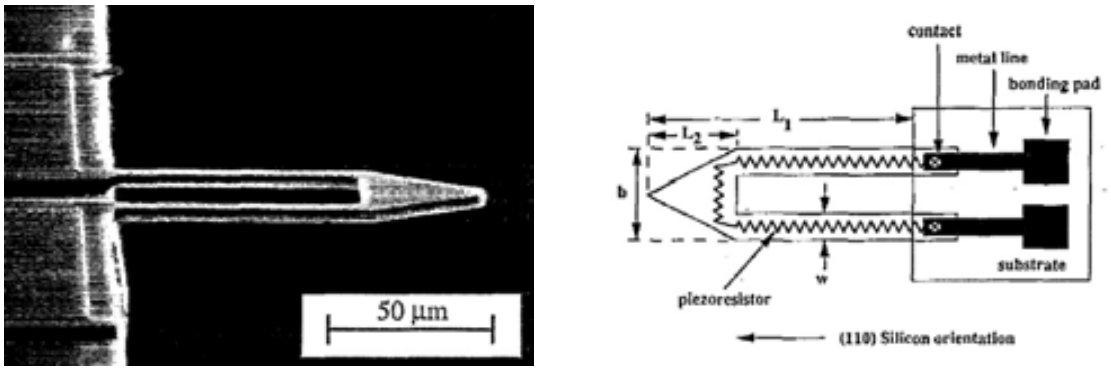
Contents

3.1 Introduction 59
3.2 Piezoresistance in Si nanowires 61
3.3 Cantilever sensor design and theoretical performance 63
3.3.1 Motivation and objectives 63
3.3.2 Sensitivity 64
3.3.3 Theoretical analysis of mechanical properties 68
3.3.4 Noise 71
3.3.5 Resolution 75
3.4 Fabrication technology 76
3.4.1 Substrates 76
3.4.2 Process Flow 76
3.4.3 Chip design 78
3.5 Fabrication results 80
3.6 Characterization of the cantilevers 84
3.6.1 Noise characterization 85
3.6.2 Sensitivity and detection limit characterization. 90
3.7 Conclusions 93
References 94

3.1 Introduction

Cantilever devices are frequently used as mass, force or displacement sensors. Different schemes, such as piezoresistive, optical and capacitive, have been used for transduction. In the piezoresistive scheme, a thin piezoresistor is located at the base of a cantilever and furthest of the neutral plane where the stress is maximum when cantilever is deflected. This stress will produce a resistance change that can be measured by applying current through the cantilever. This method is attractive due to its simplicity and versatility. The absence of external sensing elements simplifies the design and reduces the experimental costs. Device operation is further simplified by eliminating the need of a precise alignment and that makes it possible to use them under specific environment conditions such as ultra high vacuum UHV [1], low temperature [2] and liquids [3] that, in the case of optical detection, usually requires the use of a complex and expensive set up or is even impracticable. In addition, integrated strain sensors also imply important advantages for the characterization of nanoscale devices. Optical characterization is limited by diffraction effects that occur when device dimensions are scaled far below the wavelength of the available illumination, while capacitive becomes inefficient due to signal overwhelmed by uncontrollable parasitic effects in nanoscale devices. However, despite of these advantages, most AFM do not use piezoresistive readout, mainly because the piezoresistors do not achieve the resolution of the optically detected cantilevers.

The first piezoresistive cantilever was designed by Tortonese in 1991 for AFM applications [4, 5]. A Boron implanted resistor was used to measure the cantilever deflection obtaining a vertical resolution of 0.1 A in a 10Hz-1kHz bandwidth Fig 3.1.



(a) SEM image

(b) Squeme of the cantilever

Figure 3.1: Piezoresistive cantilever fabricated by Tortonese [4, 5].

Subsequently, improvements for this kind of devices have been realised by different authors. A more detailed study about the cantilever parameter optimization was realized by Harley and Kenny[6]. They studied the performance parameters for a piezoresistive cantilever sensor, sensitivity, noise, spring constant and bandwidth. Improvements in the scanning velocity speed by tuning the cantilever layout are also important for data storage applications [7]. Other option to take to reduce the scanning time, will be by the use of

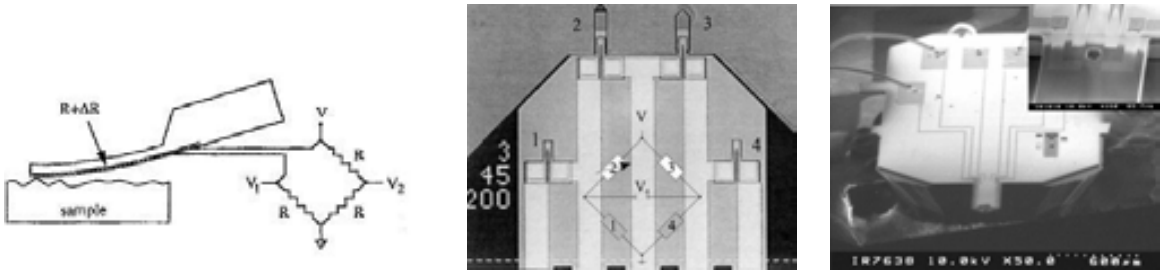


Figure 3.2: Different piezoresistive characterization setups. a) Schematic diagram of a piezoresistive detection scheme for AFM in which a external Wheatstone bridge is used to measure the relative change of resistance $\left(V_1 - V_2 = -V\frac{\Delta R}{4R}\right)$[5]; b) Optical microscope image of the thermally symetric AFM probe used by Thaysen et al. [13]The left cantilever has the integrated tip while the right cantilever serves as reference. The inserted drawing shows the setup of the Wheatstone bridge. c)SEM image of piezoresistive cantilever chip designed by Gotszalk et al [14]. Inset image of piezoresistors area located at the base of the cantilever. The piezoresistive detector contains four active resistors and then the output signal is four times higher compared with cantilevers with a single piezoresistor.

array of piezoresistive cantilevers working in parallel[8, 9, 10] that, in the case of optical readout complicates the characterization set up.

Another possibility to increase the cantilever sensitivity was by changing the number of resistors. In the first cantilevers, a single piezoresistor was placed at the base of the cantilever and then lateral stiffness and sensitivity were low because the maximum stress was located only on a part of the piezoresistor, and the change in the resistance was characterized by an external Wheatstone bridge [5], Fig 3.2(a). Su and co-workers proposed to place two implanted piezoresistor at the base of a V shape cantilever demonstrating an improvement in the cantilever performance[11]. Subsequently, the integration of the Wheastone bridge on the cantilever chip allows improve the device performance by ensure a higher thermal stability. Boisen and co-workers fabricated a chip with two resistor placed on cantilever and two on the substrate [12, 13], Fig 3.2(c) . This eliminates possible unintended drifts in the readout that can be caused by temperature fluctuations. Gotszarlk et al. [14] incorporate the full Wheatstone bride in the cantilever sensor allowing perpendicular and lateral force characterization, Fig 3.2(c).

Finally, the most obvious way to increase the cantilever resolution will be by the correct choice of the piezoresistor material with a high gauge factor and low level of noise. Gauge factor is a figure of merit of piezoresistive sensing. This, $G = (dR/R)/\epsilon$, gives the relative change in the total resistance as a consequence of an applied strain ϵ. Two different mechanisms generate piezoresistivity. First, reversible elastic deformation of material, that results in a change to the conduction geometry giving a modest change in the resistance. And, second, perturbation in the intrinsic conduction mechanisms arises from dilatation of material. These two effects are represented separately by the first and the second term of the next expression:

$$G = \frac{1}{\epsilon}\frac{dR}{R} = (1+\nu) + \frac{1}{\epsilon}\frac{d\rho}{\rho} \tag{3.1}$$

where ν is the Poisson's ratio and ρ the resistivity. The first term, associated with material deformations, is typically in the order 1 or 2. The second one, however, can typically vary from a few units for metals to a range of 10 to 100 for semiconductors materials. For this reason, efforts to optimize piezoresistive sensors have been focused in the use of doped semiconductors materials that can provide of large gauge factor. However, for cantilever with piezoresistive readout the minimum detectable displacement or force depends not only on its sensitivity but is mainly limited by the noise of the piezoresistor. In general, piezoresistors with large gauge factors are normally associated with high resistivity materials, which entails, as it will be explained in next sections, an increment of the noise. Then the influence of different parameters, such as piezoresistor geometry and material, doping doses and annealing processes must be taken into account for the cantilever design[15].

In this work, a Si nanowire array is proposed as piezoresisitive strain gauge in a cantilever sensor. In 2006, He and Yang reported an unusually high piezoresistive gauge factor that can be one or two orders of magnitude higher than previously reported for Si bulk [16]. In consequence, the use of a high density nanowire array allows to take advantage of this unprecedented gauge factor for the fabrication of high sensitivity piezoresistive sensors. On the other hand, as it will be explained in next sections, the noise level for these devices will be in the order of magnitude of those based on Si bulk but with an increase in the sensitivity proportional to the increase in the gauge factor.

3.2 Piezoresistance in Si nanowires

Unexpectedly high piezoresistive coefficients were observed for the first time by He and Yang in 2006[17]. They studied the longitudinal piezoresistive coefficient π_l^σ for $\langle 111 \rangle$ and $\langle 110 \rangle$ oriented nanowires, which is defined as the relative change in conductivity per unit of uniaxial stress, X, applied in the same direction as the electric field and current.

$$\pi_l^\sigma = \frac{1}{X}\frac{\Delta\sigma}{\sigma_0} \tag{3.2}$$

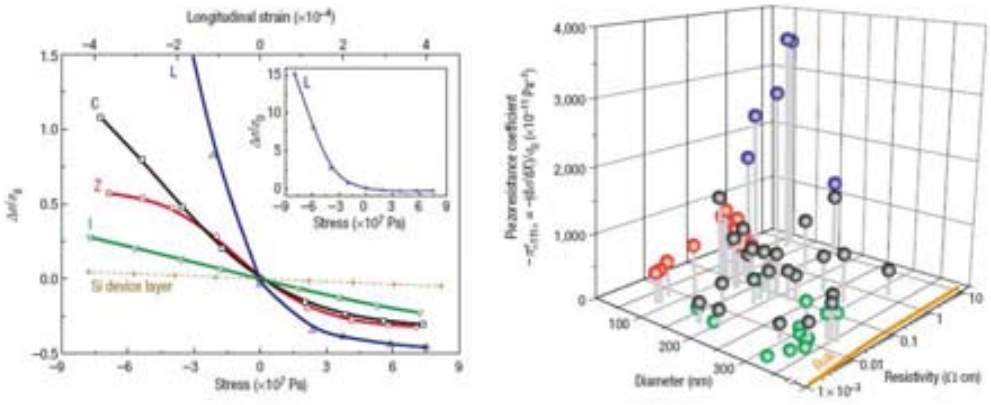
In therm of the resistivity, ρ, we can also defined the piezoresistive coefficient $\pi_l^\rho = 1/\epsilon(\Delta\rho/\rho)$ which for small changes in the resistivity satisfy $\pi_l^\rho = -\pi_l^\sigma$

Another extensively used quantity is the Gauge factor defined in the equation 3.1. This is a useful parameter because it relates magnitudes directly measured in the experiment. It can be related to the piezoresistive coefficient by:

$$G = \frac{1}{\epsilon_l}\frac{\Delta R}{R_0} = (1+\nu) + \frac{1}{\epsilon}\frac{\delta\rho}{\rho} = (1+\nu) + E\pi_l^\rho \tag{3.3}$$

where ϵ_l is the longitudinal strain and ρ the resistivity.

As a difference from bulk Si which is essentially linear, He and Yang found that piezoresistance in nanowires is generally nonlinear. These nonlinearities were classified into four categories based on the shape of the $\Delta\sigma/\sigma - X$ curves Fig 3.3(a). These curves were fitted by McLaurin series to the third power and the first order term was identified as the piezoresistive coefficient. In Fig 3.3(b) can be observed the piezoresistive coefficient for different nanowire resistivity and diameters. The piezoresistive coefficient was one or two orders of magnitude higher than typical values for bulk Si represented by the orange line in the figure. Resistivity dependence follows a similar trend to that of bulk: the piezoresistive coefficient increases as the resistivity decreases. On the other hand, an increase of the piezoresistive effect was observed for nanowires with smaller diameters while for nanowires with diameters larger than 300 nm and resistivities less than $0.004\Omega cm$ values reached close to bulk.



(a) (b)

Figure 3.3: Longitudinal piezoresistance coefficients $\pi^{\sigma}_{\langle 111\rangle}$ of p-type Si nanowires[17]. a)Relationships between the relative change in conductivity $\Delta\sigma/\sigma$ and the stress/ longitudinal strain. Four types of nonlinear behaviours of nanowires are labelled letters 'I', 'C', 'L' and 'Z' respectively. Inset shows an overview of 'L' b) First-order longitudinal piezoresistance coefficient on p-type silicon nanowires and their dependence on diameter and resistivity. $-\pi^{\sigma}_{\langle 111\rangle}$ is plotted since $\pi^{\sigma}_{\langle 111\rangle}$ is negative. Different colors represent different nonlinearities. Colour code: green 'I', black 'C', blue 'L' and red 'Z' The piezoresistive coefficients of Si bulk are represented by the orange line

They found that the large piezoresistive coefficients derive mainly from changes in the carrier mobility. This suggested that the enhanced piezoresistive effect came from modifications on the band structures. Additionally, surface states played an important role in this effect. An increment was observed just after HF treatments and a decrement after wet oxidation by HNO_3. There have been some efforts to elucidate the origin of this unexpected phenomenon. First, one year later, Cao et al [18] explained it by a surface quantization effect in the first silicon monolayer. However, not long after that, Rowe[19] proposed that it was produced by stress-induced shift of the surface Fermi level in depleted structures resulting from a change in surface charge. In favour of this hypothesis, Neuzil et al [20] demonstrated that the gauge factor could be controlled by electrical modulation of the carrier depletion. Finally Milne et al [21] found that, in depleted structures, resistance changes were dominated by electron and hole trapping at surface which results in apparent giant piezoresistance. Though their experiments were not perfomed with VLS growth nanowires, their results point out that the true piezoresistive coefficients can only be measured by modulating the mechanical stress. To date, a full understanding of the

underlying mechanism behind giant piezoresistance in VLS growth Si nanowires has not been elucidated.

3.3 Cantilever sensor design and theoretical performance

3.3.1 Motivation and objectives

Si nanowires obtained via the VLS growth mechanism offer many extraordinary properties to be exploited for improving the sensitivity of piezoresistive electromachanical transduction. In particular, their piezoresistive behaviour [16], explained in the previous section, together with their double-clamped horizontal self assembly growth [22, 23], enables an unprecedented approach to obtain highly sensitive piezoresistive strain gauges. Nevertheless, the use of Si nanowires as piezoresistive sensor in mechanical devices has not been completely exploited. So far, piezoresistive sensing on devices based on bottom up nanowires has been used only on mass sensor devices [24]. Later, in 2010, Songsong et al. [25] presented the fabrication of a pressure sensor transducer based on embedded top down Si nanowires. They found a very high sensitivity compared with the state of the art of piezoresistive pressure sensors. However, recently, Koumela et al. [26] demonstrated an improvement in piezoresistive strain gauges for released nanowires due to a surface effect. This means than the use of bottom up or top down released nanowires will allow the fabrication of more sensitive devices.

In this case, we propose the fabrication of a piezoresisitive cantilever based on catalyst grown Si nanowire arrays to be used as displacement sensor. This device will allow to exploit the piezoresistive behaviour observed in Si nanowires and to contribute to the characterization of piezoresistive behaviour of nanowires which is not completely understood yet. On the other hand, we will develop a fabrication process that should allow the large scale integration of Si nanowire arrays in semiconductor devices not only useful for this kind of devices but that could also be extended to other kind of devices based on Si nanowires.

For a piezoresistive cantilever, the important performance parameters are sensitivity, noise, bandwidth and spring constant. The minimum detectable displacement is given by the noise, integrated in the measure bandwidth, over the sensitivity. In principle, by choosing a high enough spring constant, a piezoresistive cantilever can be given arbitrarily good sensitivity; however, the required forces to bend it may be extreme and, for example, in the case of contact AFM imaging, a stiff cantilever exerts large forces which may damage the sample. In order to know the optimal cantilever layout, mechanical simulations and theoretical model of their mechanical and electrical behaviour will be needed.

3.3.2 Sensitivity

The cantilever sensitivity determines how large is the output signal given a particular input signal. For a force sensor, it will be given in units of V/N while for a displacement sensor in units of V/m. However, in a piezoresistive sensor, the resistance change is usually measured by a Wheatstone bridge, Fig 3.2 , followed by an instrumentation amplifier. This means that sensitivity can be arbitrarily large by varying the gain and the bias voltage of the characterization circuit. For this reason, a magnitude more frequently used is the relative change of resistance per unit of force or displacement applied to the cantilever tip $(\Delta R/R)\,1/F$ and $(\Delta R/R)\,1/d$ respectively.

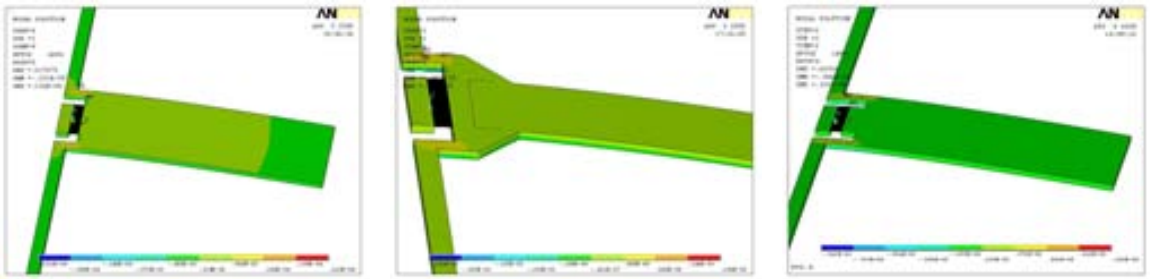
A cantilever sensor can be used for displacement or force sensor and both sensitivities will be related by the spring constant following the Hooke's law. Then the spring constant of a cantilever beam is critical to the usefulness of the sensor. In general, increasing the cantilever stiffness improves its displacement sensitivity, while decreasing the stiffness improves the force sensitivity. In principle, by choosing a high or low enough spring, depending of if we want to fabricate a force or a displacement sensor, a piezoresistive cantilever can be given arbitrarily good sensitivity. However, this can have negative consequences. A displacement cantilever sensor typically used in contact mode AFM imaging, a stiff cantilever exerts large forces which may damage the sample. On the other hand, in the case of too soft cantilever, if the force to be measured has a gradient greater than the cantilever spring constant, then the cantilever is unstable, and will snap down along the gradient[6].

The piezoresistive cantilever that will be studied will be focused to sensor displacement applications. The fabrication of a cantilever for force measurements would require a low spring constant. The way to reduce the cantilever spring constant requires to reduce the cantilever thickness to a few hundreds of nanometers. Due to the bad homogeneity of the commercially available wafers with the correct crystallographic orientation, in the order of cantilever thickness, the fabrication process would be impracticable. On the other hand, the fabrication of cantilever for displacement sensors does not require the reduction of the device layer thickness and this simplifies the process.

In our case, due to the complexity of the structure an analytical model could be complicated and inaccurate. Then a Finite Element Analysis software, ANSYS, will be necessary to optimize the cantilever layout in order to have the maximum displacement sensitivity. This will be given then by:

$$\frac{\Delta R}{R} d^{-1} = G\beta \tag{3.4}$$

Where β is a parameter defined as the strain produced in the nanowire per unit of cantilever deflection ($\beta = \epsilon/d$) and in general will be dependent of device geometry. The parameter β will be extracted from the simulations.



(a) (b) (c)

Figure 3.4: Cantilever designs studied to find the optimum layout

A standard double leg cantilever design will be used for the cantilever fabrication. The nanowire array will be grown at the base of the cantilever, between the two legs, well above or below of the neutral axis to ensure that only compressive or tensile stress occurs when the cantilever is deflected. However, the influence of the array in the mechanical behaviour of the structure becomes important for high density arrays and a previous analysis of the structure is required before starting with the fabrication process.

In our model the XYZ axes are oriented in the $\langle 111 \rangle$, $\langle 112 \rangle$ and $\langle 110 \rangle$ silicon crystallographic directions respectively. The corresponding material properties used for our model are showed in the Table 3.1. For simplicity, nanowire cross section has been supposed square instead of hexagonal. Their mechanical properties can be considered similar to bulk properties so the definition of an additional material is not necessary. Element type used for the simulations has been SOLID95, composed by 20 nodes. For cantilever deflection a perpendicular force has been applied to the cantilever end.

Young Modulus	Shear Modulus	Poisson Coefficients
$E_X = 169GPa$	$G_{XY} = 0.509GPa$	$\nu_{XY} = 0.062$
$E_Y = 169GPa$	$G_{XY} = 0.796GPa$	$\nu_{XZ} = 0.278$
$E_Z = 130GPa$	$G_{XY} = 0.796GPa$	$\nu_{YZ} = 0.278$

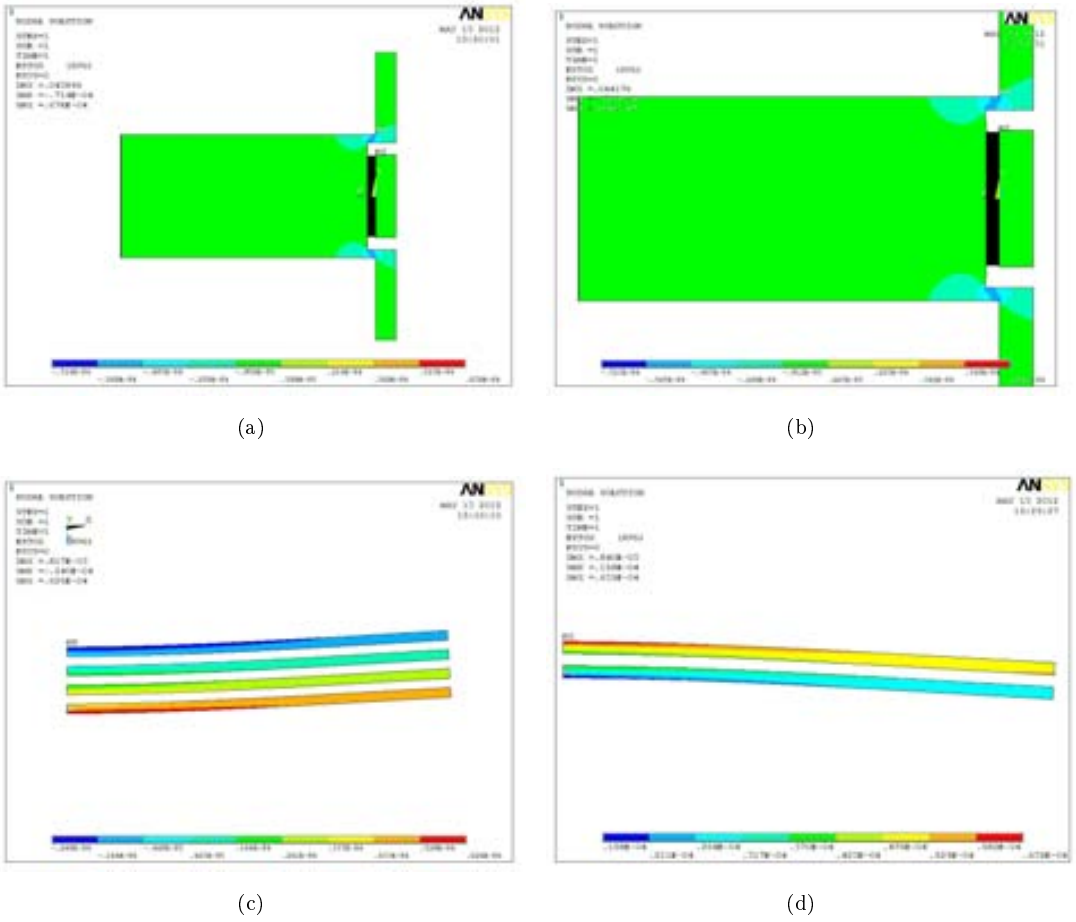
Table 3.1: Si properties in the employed reference system.

Three different cantilever layout were considered in order to obtain the maximum sensitivity Fig 3.4. The first one, Fig 3.4(a) was chosen because it presented a more uniform stress in the nanowire array and the higher sensitivity.

The first effect studied is the nanowire array mean stress and the position of the neutral plane. Neutral plane in the cantilever is defined like the area along which there are no longitudinal stresses or strains. If the cross section is symmetric, isotropic and not curved before a bend occurs, like in the cantilever without nanowires, then the neutral plane is the geometrical centroid. When the cantilever is deflected, all the elements in one side of the neutral plane will be in state of tension while those on the opposite side are in compression.

Nanowires are so much softer than cantilever legs so, in a cantilever with low density

of nanowires, simulations show that neutral plane is not significantly affected. However, as the cantilever legs become softer or the nanowire density increases, the neutral plane of the structure is situated closer to the array decreasing the mean array strain for a deflection. It can be observed, for example, in Fig.3.5.



(a) (b)

(c) (d)

Figure 3.5: FEM simulation of a piezoresistive cantilevers with different nanowire array thickness. (a)and (c) General cantilever layout and longitudinal strain distribution of a cantilever with a nanowire array thickness of 400nm (1/3 of total) and 200nm (1/5 of total) respectively. Cantilever length, width and thickness are $60\mu m$, $30\mu m$ and $1\mu m$ respectively, leg dimensions are $2\mu m$ length and width and nanowire array have a density of $50nw/\mu^2$. (c) Longitudinal strain of nanowire array with a thickness of 400 nm. Negative and positive values of strain appear in the nanowire array. There are positive (blue color) and negative values (d) longitudinal strain of nanowire array of 200nm thickness. Only positive values of strain can be observed in the nanowire array.

In Fig. 3.5 two cantilever with the same geometry but with different nanowire array thickness is studied. In the first one, Fig 3.5(a) nanowire are only located in the 1/3 of the total cantilever thickness at the top part. If we analyse the longitudinal strain distribution, Fig 3.5(b), in the nanowire array we can observe that positive and negative strains appears at the same time when cantilever is deflected. This caused some nanowires to have opposite change of resistance than the rest of nanowires in the array decreasing the relative change in the resistance and then the sensitivity. In the second cantilever, Fig 3.5(c), the nanowire array are only confined in 1/5 of the total cantilever thickness. When the longitudinal strain is analysed, it can be observed that only strains of one sign are present in the array when it is deflected. The nanowire array is then located far from the neutral axis, which produces an increase in the sensitivity. From the simulations, we

can compare the β factor to observe the influence in the sensitivity of the cantilever array thickness. For the cantilever with the thicker array $\beta = 429$ while for the cantilever with the thinnest array $\beta = 896$.

In order to ensure a proper location of the neutral axis, we have estimated that nanowire array must be located at around a quarter or a fifth of the total thickness of the cantilever well above o below of the neutral axis. The neutral axis will be out of the nanowire array thickness, and as it will be explained next, ensure a high number of nanowires which is beneficial to reduce the noise of the cantilever and is technologically attainable.

On the other hand, a study about the stress distribution on the nanowire array was realized for different leg sizes Fig 3.6. A high sensitivity array, of 100 nanowires per square micron, was used in the simulations in order to maximize their effect in the structure. We chose this density because is the higher density that we have observed in nanowires grown by galvanic displacement in our test structures. In general, cantilever legs are stiffer than the array and the deflection shape is not significantly affected. However, for short cantilevers with thinner legs, array effects become significant.

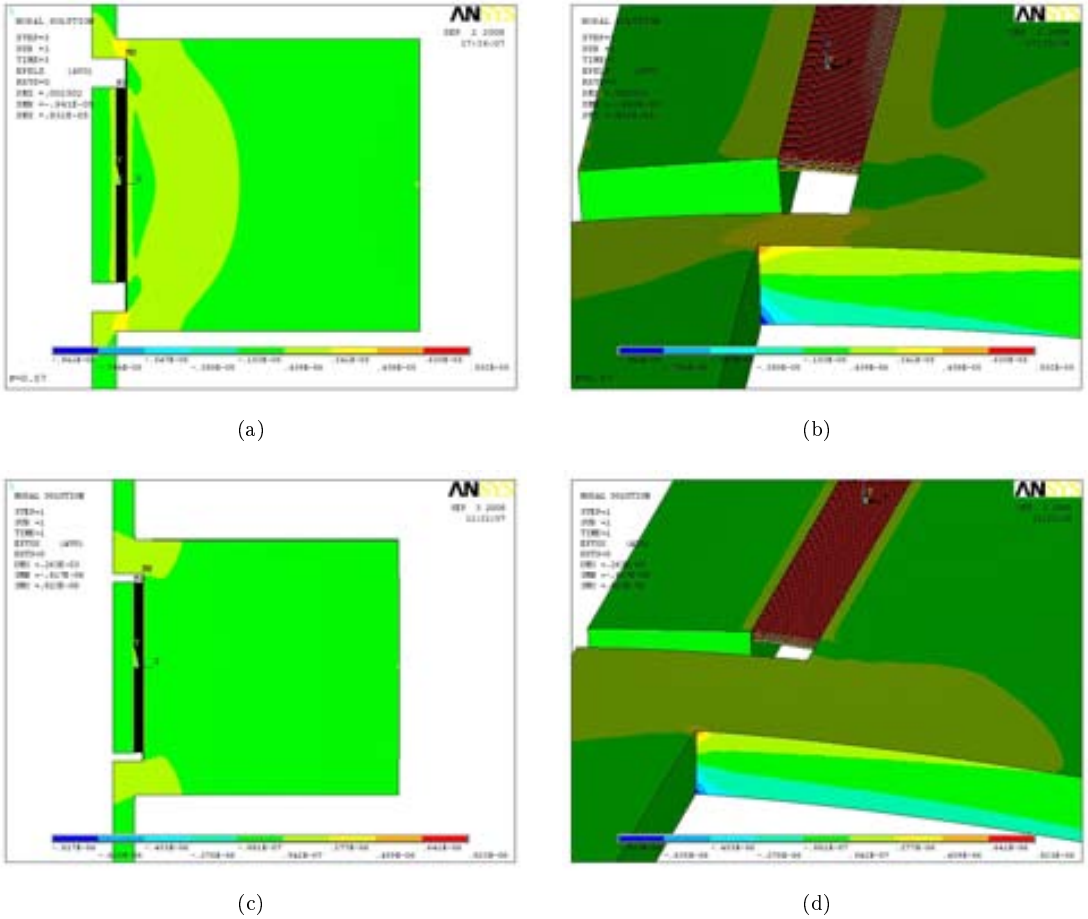
No uniform stress distribution across the array width for cantilevers of thinner legs. This effect is especially important for shorter cantilevers and have negative consequences in the sensitivity. For this reason, cantilevers designs with this geometries has been eliminated from the final design. On the other hand, we observed that an increment in the cantilever leg width does not affect significantly to the cantilever sensitivity. An example of variation of elastic constant and factor β is shown in the table 3.2.

w_l/μ	β/m^{-1}	$K/(Nm^{-1})$
2	651	4.37
4	709	5.52
8	730	6.93

Table 3.2: Study of cantilever elastic constant and β parameter ($\beta = \epsilon/d$) for different cantilever leg width, w_l. The cantilever thickness, width and length are $2\mu m$ $60\mu m$ and $60\mu m$ respectively. Cantilever leg length is $2\mu m$ in the three studied cantilevers.

Finally, cantilevers with different geometries have been chosen to be fabricated. Cantilever elastic constant are in the order of 0.1 to 10 N/m and the estimated sensitivities are in the order of $10^4 - 10^6 m^{-1}$ depending of the cantilever dimensions for a gauge factor of 1000. This sensitivity is one or two orders of magnitude higher than typical sensitivities of cantilevers with similar elastic constants based on Si bulk[4, 27, 11, 13, 12, 15]. The increment on the sensitivity is due not only to the gauge factor but also to the fact that Si nanowires act as a strain accumulators.

The higher sensitivity corresponds to a stiff cantilever shown in the Fig 3.7. From the simulations we can extract the relationship between strain and cantilever deflections which gives $\beta = 4873$. Assuming a gauge factor of 1000 the displacement sensitivity will be $4.87\,10^6 m^{-1}$.



(a) (b)

(c) (d)

Figure 3.6: FEM simulation of piezoresistive cantilevers to study the effect of leg width in the longitudinal strain. Both cantilever have square shape of $60\mu m$ width and length, $2\mu m$ thickness and cantilever length of $2\mu m$. (a) and (b) The cantilever leg width is $4\mu m$. The strain is not uniform in the cantilever width due to the nanowire array effect. (c) and (d) cantilever leg width is $6\mu m$. The strain is uniform, the effect of the legs dominate over the array.

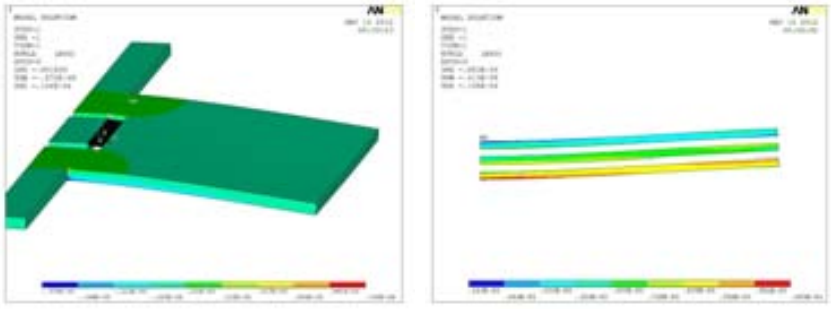
3.3.3 Theoretical analysis of mechanical properties

Despite the simulations give us a more precise estimation of the cantilever mechanical properties this are high time consuming and an analytical model could be useful to extract information about the optimization of the parameters. The geometrical parameters used in the model are represented in the Fig 3.8.

An approximate expression for the cantilever deflection can be extracted from the elementary beam theory. According to this theory under the approximation of small deflections the cantilever profile can be estimated from:

$$\frac{d^2}{d^2x}z(x) = \frac{M}{EI} \tag{3.5}$$

where M is the torque moment, I the area moment of inertia, E the young modulus



(a) (b)

Figure 3.7: FEM simulations of the piezoresistive cantilever with the highest sensibility. Cantilever length, width and thickness are $30\mu m$, $30\mu m$ and 1.5μ.

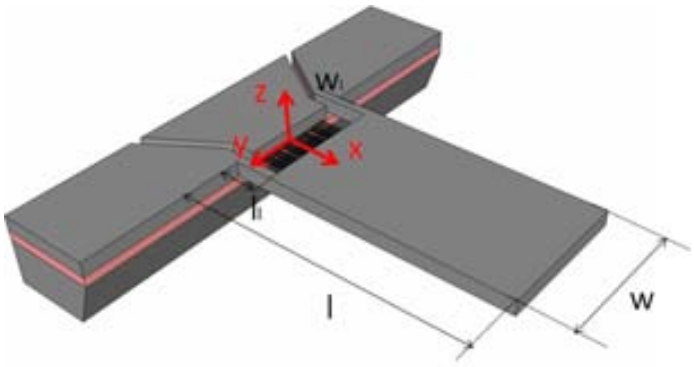


Figure 3.8: Geometrical considerations for cantilever calculations.

and M the torque moment that external force applied to the cantilever tip is $F(l-x)$. On the other hand, the cross section of the cantilever is not uniform, so the moment of inertia is expressed as a function of the coordinate x as follow in the equation 3.6:

$$I = \begin{cases} w_{leg}t^3/6 + I_{array} & x \leq x_{leg} \\ wt^3/12 & x \geq x_{leg} \end{cases} \tag{3.6}$$

Where, I_{array} is the flexural moment of inertia of the nanowire array and it can be calculated by the Stainer theorem:

$$I_{nw} = \sum_{i=1}^{n} n_i \left(I_{nwi} + A_{nwi}s_i^2\right) \tag{3.7}$$

where I_{nwi}, A_{nwi} and s_i are the moment of inertia, the area and the distance to the neutral axis of the nanowire i. If, for simplicity we consider an homogeneous array formed

by n nanowires with a square cross section of side d and located at a mean distance s of the neutral axis, then:

$$I_{array} = \sum_{i=1}^{n} n_i \left(\frac{d_i^4}{12} + d_i^2 s_i^2 \right) \simeq \frac{nd^4}{12} + nd^2 s^2 \tag{3.8}$$

In general the contribution of the array to the moment of inertia could be considered negligible for low nanowire densities because the nanowire diameter will be in the order of 50-100nm while the cantilever thickness will be between $1 - 2\mu m$. However, for higher density nanowires arrays, since nanowires have to be grown furthest of the neutral axis, the second term of the equation becomes important. Nanowires will be grown in around a quarter of the cantilever, so the mean distance s to the neutral plane will be between t/4 and t/2.

Integrating the equation 3.5 and appliying the boundary conditions at the base of the cantilever $y(0) = 0$ and $y'(0) = 0$ and at $x = l_{leg}$ the cantilever deflection.

$$\begin{array}{rcll} z & = & \frac{F}{EI}\left(\frac{lx^2}{2} - \frac{x^2}{6}\right) & x \leq x_{leg}, \quad I = \frac{w_{leg}t^3}{6} + I_{array} \\ & = & \frac{F}{EI}\left(\frac{lx^2}{2} - \frac{x^2}{6}\right) + ax + b & x \geq x_{leg}, \quad I = \frac{wt^3}{12} \end{array} \tag{3.9}$$

where a and b can be calculated from the boundary conditions at $x = x_{leg}$.

$$\begin{array}{rcl} a & = & \frac{6F}{E}\left(ll_{leg} - \frac{l_{leg}^2}{2}\right) \\ b & = & \frac{F}{EI}\left(\frac{lx^2}{2} - \frac{x^2}{6}\right) + ax + b \end{array} \tag{3.10}$$

What yields the following elastic constant:

$$K = \frac{E}{\frac{4l^3}{wt^3} + \left(\frac{l_{leg}^3}{3} - ll_{leg}^2 + l^2 l_{leg}\right)\left(\frac{1}{I_1} - \frac{1}{I_2}\right)} \tag{3.11}$$

That in the case of a cantilever without nanowires or with a low density, the elastic constant is:

$$K = \frac{Et^3}{\frac{4l^3}{w} + \left(2l_{leg}^3 - 6ll_{leg}^2 + 6l^2 l_{leg}\right)\left(\frac{1}{w_{leg}} - \frac{2}{w}\right)} \tag{3.12}$$

Equations 3.11 and 3.12 were very useful for quick estimation of the order of magnitude. However, we have to take into account that in the case of short and wide legs the

beam theory can not be used. FEM simulations give more precise value of the cantilever mechanical behavior. In addition, simulations can predict undesired mechanical effects. The mechanical effect of the wires can be also estimated from the equation. As representative example, we consider a typical cantilever of $120\mu m$ of length, $30\mu m$ of width and $4\mu m$ and $2\mu m$ of cantilever leg length and width. The cantilever without nanowires has a elastic constant estimated by the equations of 1.5N/m while if we included a high density array placed in a quarter of the cantilever of 150 nanowires the elastic constant changes to 1.6 N/m. From the FEA simulations we obtained a spring constant of 1.12N/m for the same cantilever with this number of nanowires.

On the other hand, due to the complexity of the structure, the deduction of a resonant frequency expression directly from the movement equation results difficult and the use of an approximation method is necessary. An approximate expression can be deduced by the Rayleigh method based on the energy conservation. The energy under maximum deflection, which is stored entirely as potential energy, is transformed entirely to kinetic energy at zero deflection. For a double leg cantilever without considering the nanowire array the resonant frequency could be approximate to:

$$\omega^2 = \frac{140}{33}\frac{K}{tlw\rho}\frac{(\frac{l}{w}+\frac{3}{2}l_l(1-\frac{l_l}{l})(\frac{1}{w_l}-\frac{2}{w}))^2}{(\frac{l^2}{w^2}+\frac{35}{11}l_l^2(\frac{1}{w_l}-\frac{2}{w}))^2} \tag{3.13}$$

3.3.4 Noise

Noise is a random current fluctuation that can be produced by different electrical or acoustic sources. Two types of noise must be considered for this kind of devices, intrinsic noises and external noise. The external noise makes reference to unwanted environment interferences. These signals in general can be avoided by the correct shielding and proper wiring. However, the intrinsic noise is due to the electrical or mechanical devices properties and considerations in device design must be taking into account in order to minimize it. Noise is often described by the power spectral density (PSD). The PSD is defined by the Fourier transform of the autocorrelation function of the parameter of interest. This magnitude, with units of $[]^2 Hz^{-1}$, specifies the shape of the noise as a function of frequency.

When the noise comes from several sources, total PSD can be estimated by adding noise. In the case of piezoresistive cantilevers, there are three dominant sources of noise: thermal noise, Hooge or 1/f noise and thermomechanical noise. So then, the total PSD will be:

$$S_T(f) = S_J(f) + S_H(f) + S_{th}(f) \tag{3.14}$$

The total noise of the experiment is given by the square root of the integral of the

PSD over the experimental frequency bandwidth.

$$X_{noise}^2 = \int_{BW} S(f)^2 df \tag{3.15}$$

3.3.4.1 Thermal noise

Thermal noise describes voltage fluctuations caused by random vibrations of charge carriers in equilibrium at a finite temperature. Works of Johnson and Nyquist [28, 29]led to the expression of the thermal noise power spectral density S_J (units V^2/Hz):

$$S_J = 4K_BTR \tag{3.16}$$

where K_B is the Boltzmann constant, R the total resistance and T the absolute temperature in Kelvin. Thermal noise is independent of the applied voltage since the thermal fluctuations are present regardless of the applied tension. However, a temperature increase, given for example by Joule effect, will produce an increment in thermal noise. Furthermore, thermal noise is called a white noise because it is not frequency dependent since thermal fluctuations are not related with any time constant.

In the designed cantilever, the piezoresistor is based on an array which nanowires are electrically connected in parallel. The piezoresistive coefficients are higher for lightly doped nanowires which will give a higher thermal noise. A simple way to reduce it is increasing the number of nanowires in the array either by increasing the nanowire density or by increasing the array width. Either way does not change the mechanical properties of the cantilever. Considering an uniform array of n nanowires with a resistance R_{nw}, the total thermal noise given by the array is then:

$$S_J = 4K_BTR_{array} = 4K_BT\frac{R_{nw}}{n} \tag{3.17}$$

3.3.4.2 Hooge or 1/f noise

The power spectral density of the Hooge or 1/f noise $S_{1/f}$ is not constant through the frequency spam, but it is inversely proportional to the frequency over a wide range of frequencies. At low frequencies, its importance grows and can even become the main source of noise.

Their origin mechanism is not clear yet and despite several theories has been proposed, none of them is able to reproduce the experimental results in the wide range of frequencies.

There is not an agreement about if Hooge noise is produced by conductivity variations ($\sigma = \mu nq$) due to fluctuations in carrier mobility ($\Delta\mu$) or density Δn. A semi-empirical law was proposed by Hooge by fitting one experimental parameter which is dependent of material[30].

$$S_H = \frac{\alpha V_{cc}}{N}\frac{1}{f} \tag{3.18}$$

where N is the number of carriers in the region where noise is generated, V_{cc} is the applied voltage and α is a empirical dimensionless constant with values usually between 10^{-6} and 10^{-4}. This noise is only present when a bias voltage is applied and is inversely proportional to the number of carriers by trapping and de-trapping mechanism. Unlike carbon nanotubes, which present a large Hooge noise [31], studies based on Si nanowire have demonstrated that these are an order of magnitude less noisy [32]. The calculated Hooge parameters were in the order of 10^{-5}. In general, the value of the Hooge parameter is a good indicator of the process quality and the values obtained for Si nanowires are comparable to Hooge parameters for low noise Si bulk devices[33]. That makes Si nanowires good candidates for the fabrication of electronic devices. An important magnitude, related to the two electrical sources of noise explained so far, is the corner frequency. This is the frequency between the region dominated by the low frequency Hooge noise and the flat noise, the Thermal noise. This is given by:

$$f_c = \frac{\alpha V_{cc}^2}{N 4 K_B T R} \tag{3.19}$$

For higher frequencies than the corner frequency, the electrical noise will be limited only by thermal noise. This means that, if this frequency is low enough, the low end of the measurement bandwidth can be chosen in such a way that Hooge noises do not have to be considered. For a uniform array the number of carriers will be proportional to the number of nanowire so then the Hooge noise of a nanowire array will be given by:

$$f_c = \frac{\alpha V_{cc}^2}{N 4 K_B T R_{array}} = \frac{\alpha V_{cc}^2}{N_{nw} 4 K_B T R_{nw}} \tag{3.20}$$

where N_{nw} is the number of carriers in a single nanowire. This means that, for a uniform nanowire distribution, corner frequency is independent of the number of wires in the array. However, the Thermal noise, which appears at every frequency is decreased as a consequence of a reduction in the total resistance.

3.3.4.3 Thermomechanical noise

Thermomechanical noise can be considered as the mechanical analogue of the Thermal noise. Thermomechanical noise is produced by mechanical cantilever oscillations due to the thermal energy. The cantilever movement will produce a change in the piezoresistor stress with the consequent change in the resistance value. However, the other two sources of noise will contribute in general more than this one.

Thermomechanical noise is effectively a white noise drive (N^2/Hz) of force power spectral density:

$$S_{F_{th}} = \frac{4KK_BT}{w_0Q} \tag{3.21}$$

where K is the cantilever spring constant, K_B is the Boltzmann constant, T the absolute temperature in Kelvin, w_0 is the resonant frequency and Q the quality factor of the cantilever. The force power spectral density will be related to the displacement power spectral density through the transfer function:

$$H(w) = \frac{1/m^2}{(w_0^2 - w^2)^2 - (w_0w/Q)} \tag{3.22}$$

with m the effective mass, w_0 the resonant frequency and Q the quality factor. So the resulting displacement noise in units of m^2/Hz is:

$$S_{th}(w) = \frac{4w_0K_BT}{mw_0Q}\frac{1}{(w_0^2 - w^2)^2 - (w_0w/Q)^2} \tag{3.23}$$

At low frequencies, the displacement noise is independent of the frequency and can be rewritten:

$$S_{th}(w) = \frac{4K_BT}{Kw_0Q} \tag{3.24}$$

which is frequency independent. Finally, thermomechanical noise can be expressed in units of V^2/Hz by multiplied the displacement noise by the cantilever sensitivity.

Unlike the other two sources of noise previously analyzed, this one will be determined by geometrical characteristics of cantilever. However, except at resonance frequency, this source of noise has been smaller than Hooge and Thermal noise in practice. Since the measurement bandwidth is typically restricted to frequencies below the first resonance, this noise can be neglected.

3.3.5 Resolution

Cantilever resolution is the most important magnitude because it determines the minimum detectable displacement or force that can be measured. Resolution is given by the noise integrated in the measurement bandwidth divided by the sensitivity.

$$z_{min} = \frac{\left(\int_{BW} S_T(f)^2 df\right)^{1/2}}{Sen} \tag{3.25}$$

First we studied the cantilever sensitivity. From the FEM simulations we have estimated the optimal cantilever layout to maximize the strain produced in the nanowire array for a given cantilever deflection. We have estimated that nanowire array must be located only between a quarter or a fifth plane of the total cantilever thickness well above or below of the neutral axis to ensure that only compressive or tensile stresses are present when cantilever is deflected. Another important point, that we have been studied, is the mechanical behavior of cantilever when nanowire array density and/or dimensions increase. This produces that not homogeneous stress is distributed in the nanowires resulting in a sensitivity decrease. Assuming a gauge factor of 1000 the cantilever sensitivity has been estimated to be in the range of 10^4 to $10^6 m^{-1}$.

From noise analysis we have concluded that the two dominant sources of noise are Thermal and Hooge noise. The Johnson noise is proportional to the density of material while the Hooge noise is inversely proportional to the number of carriers. An increment in the nanowire resistivity will produce a reduction of both sources of noise; however, this will produces a reduction in the nanowire array gauge factor and then of sensitivity. The other way to reduce the noise level is by increasing the number of nanowires in the array. This will produce a reduction of the total array resistance since nanowires are electrically connected in parallel and an increment of number of carriers because it is proportional to the piezoresistor volume. On the other hand, we have demonstrated that an increment of the number of nanowires will not produce an increment of the corner frequency.

Other parameter that has to be taken into account when we study resolution is the measurement bandwidth. The total amount of noise is dependent of the measurement bandwidth, since filters are used to remove noise outside of the bandwidth of interest. As a result, resolution should be quoted as the minimum detectable displacement in a given bandwidth. The bandwidth is limited by the cantilever application. In this case, the lower limit will be set preferentially to frequencies higher than the corner frequency while the upper limit will be chosen under the resonant frequency.

3.4 Fabrication technology

3.4.1 Substrates

The main characteristics of the wafers used for the device fabrication are represented in table 3.3. Device layer presents a special crystallography orientation in the $\langle 110 \rangle$. This enables the fabrication of microtrenches with sidewalls oriented in the $\langle 111 \rangle$ for the horizontal growth of Si nanowires. Another important characteristic of substrates is that they were selected with the highest commercially available doping level. This is important since non-metallic lines will be defined and electrical contact will be made directly over the substrate to prevent the CVD contamination during the growth.

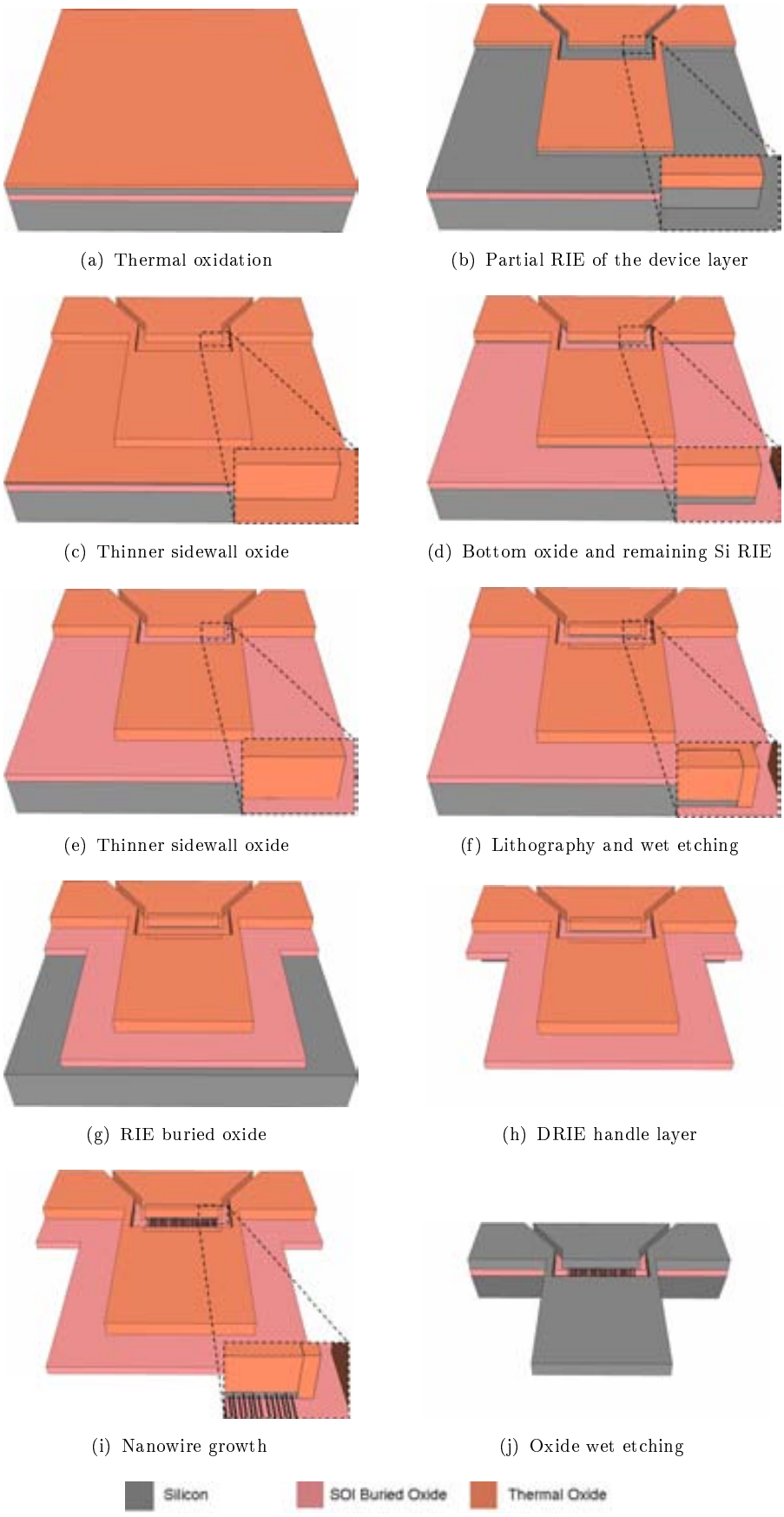
Device Layer	Thickness Crystallographic Orientation Main Flat Doping	$2 \pm 0.5 \mu m$ $\langle 110 \rangle$ $\langle 111 \rangle$ p-type with B $\rho = 0.095 - 0.110 \Omega cm$
Oxide Layer	Thickness	$2 \mu m \pm 5$
Handle Layer	Thickness Crystallographic Orientation Doping	$500 \pm 10 \mu m$ $\langle 100 \rangle$ p-type with B $\rho = 1 - 30 \Omega cm$

Table 3.3: SOI wafer characteristics

3.4.2 Process Flow

For the optimum performance of the cantilever, Si nanowire array must be selectivity grown at the base of the cantilever and only in a partial of the total thickness of the cantilever. This means that, as the catalytic deposition will be made by galvanic displacement, Si surfaces must be selectivity exposed only in areas where nanowire growth is wanted. In order to obtain such structures a fabrication technology has been developed and main steps are represented in the Fig. 3.9.

The fabrication process starts with a thermal oxidation of around 600nm, Fig 3.9(a), followed by a lithography step and a reactive ion etching (RIE) of the full oxide and of around three quarters of device layer thickness, Fig 3.9(b). In this step, the cantilever layout is defined. Then a second oxidation of 200nm, Fig 3.9(c) is realized to cover exposed silicon surfaces. After that, 200nm of oxide and then the rest of the device layer until the buried oxide, are removed with a RIE without the use of a lithography mask, Fig 3.9(d). The RIE conditions are selected to be very anisotropic so, this means that, vertical sidewalls remain covered with oxide while at the bottom part of the trenches, Si surface is exposed.



(a) Thermal oxidation

(b) Partial RIE of the device layer

(c) Thinner sidewall oxide

(d) Bottom oxide and remaining Si RIE

(e) Thinner sidewall oxide

(f) Lithography and wet etching

(g) RIE buried oxide

(h) DRIE handle layer

(i) Nanowire growth

(j) Oxide wet etching

Figure 3.9: Main Fabrication steps

In this point the device surface is covered with silicon oxide except at the bottom part of the cantilever thickness where Si surface is exposed. However, we need to laterally confine this Si exposed area to the cantilever base. To that end, a third thinner oxidation Fig 3.9(e), of 50 nm, is made to cover the bottom part of the trench sidewalls. Next, a window is open with a lithography step to remove just this 50 nm of oxide by a wet etching only at the base of the cantilever Fig 3.9(f). And, due to the difference of the oxide thickness at the bottom and at the top part, we will have only the device Si surface exposed at one fraction of the total thickness of the cantilever. Before the oxide wet etching, an extra plasma was made to remove possible rests of the resin at the bottom part of the trench.

Now, the cantilever layout and the nanowire growth areas are defined. The next step will be a back side etching by deep reactive ion etching (DRIE) to release the cantilever. However, before that, a previous step is introduced to prevent that internal compressive stress, formed during the thermal oxidation to form the buried oxide of the SOI, could damage the cantilever structure [34]. This effect is specially important for cantilevers with thickness comparable to the buried oxide like in our case. So then, the buried oxide is removed with a RIE Fig 3.9(g), leaving an oxide membrane only under and just around the cantilever protecting the structure from silicon etching during the back side DRIE Fig 3.9(h). So then, with this technological step, the oxide is cracked at the appointed place to avoid the cantilevers breaking [34].

Once the cantilever is realised, we continue with the catalyst deposition and the nanowire growth Fig 3.9(i). To that end,chips of around one square centimeter are subtracted from the wafer for the nanowire growth in a small tube CVD. Due to the small shape of the holder, only a maximum of three or four chips are growth at the same time.

Finally, after nanowire growth, a wet etching is made to remove the oxide at the electrodes surface and under the cantilever releasing completely the structure Fig 3.9(j). Then, the cantilever is bonded and ready for characterization and testing. For that is very important to etch the surface oxide just before bonding to prevent the native oxide formation.

3.4.3 Chip design

Four mask levels were needed to complete the fabrication process described previously. This set of masks was named CNM391 and some representative images are shown in the Fig 3.10. First layer, device layer, for the cantilever shaping, second one, array layer, for the nanowire array growth, the third level, oxide layer, for the buried oxide RIE and the fourth level for the back side DRIE.

Hence, four different levels were designed. In Fig.3.10 the whole wafer design is shown. This is formed by 38 large chips of around one centimetre square. In turn, these large chips are formed by six smaller chips and each one of these smaller chips is composed by four

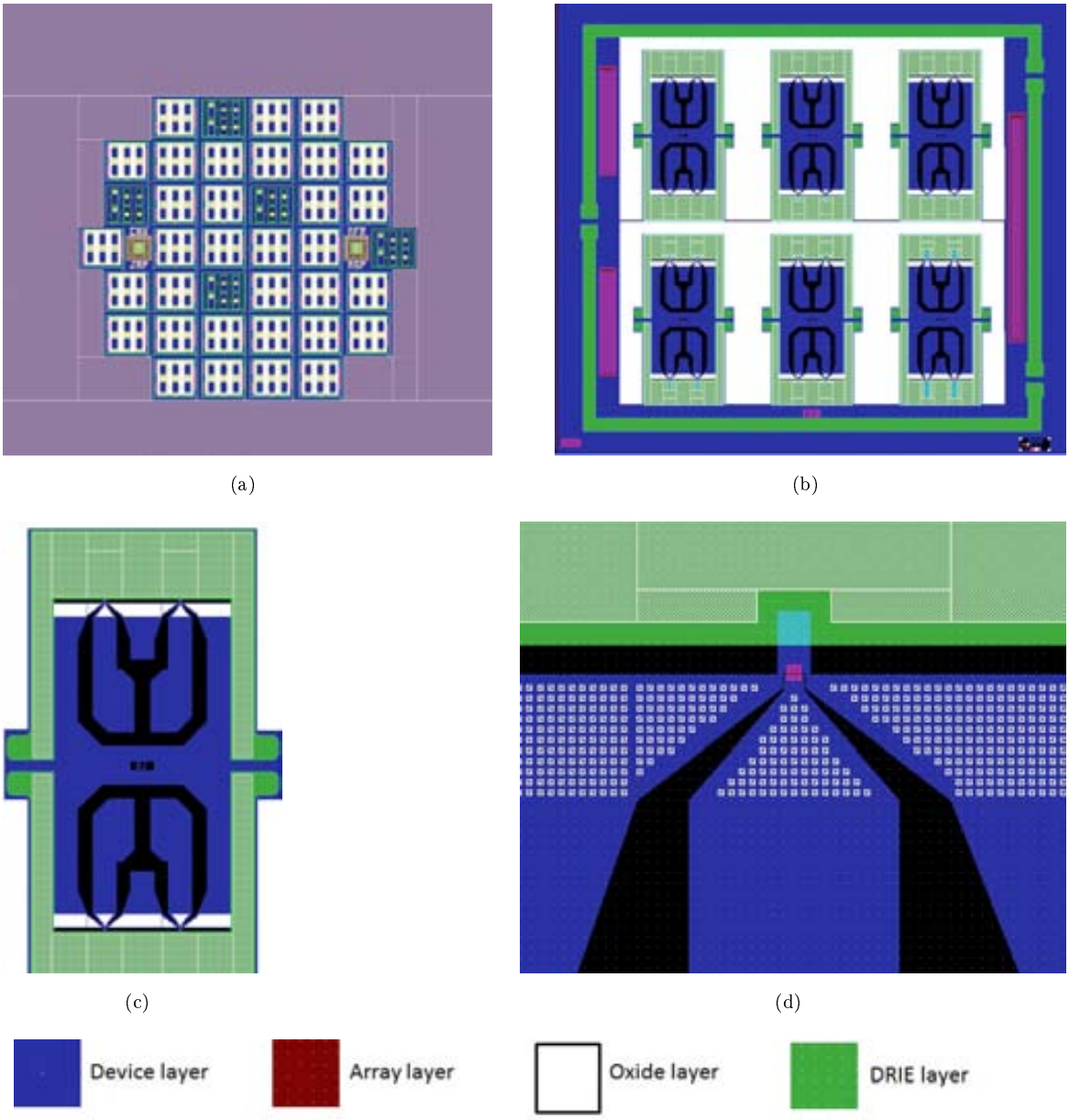


Figure 3.10: CNM 391 set of mask. a) Full design, b) large chips for the nanowire growth, d) small AFM shape chips, and e) cantilever detail.

different cantilevers. In the DEVICE layer (blue color), the cantilever and chip shapes are defined. Three different chip designs were included in the wafer. Each one of these chips was designed for a different nanowire length ($2\mu m, 4\mu m, 8\mu m$). This is important, since the nanowire growth is made at chip level and the nanowire length is mainly controlled by the growth time. So then, it is desired that in each individual growth, every device has the same nanowire length. In addition, each chip is formed by six smaller chips, with standard AFM shape, which are extracted from the large chip after nanowire growth for bonding and characterization. Each one of these smaller chips has four cantilevers with his own electrodes for characterization and testing.

The second level is the ARRAY layer (red color). This layer is located at the base of the cantilever where the nanowire growth is desired. This layer was designed taking into account possible misalignments in the lithography step preventing nanowires from growing in areas where no stress is produced when the cantilever is deflected.

The third mask level, the OXIDE level (white color), as was explained before, was used to etch the oxide membrane around the cantilevers and prevent damage during the back side DRIE step. In addition, in this layer, additional square areas were also introduced on surface device. This made that, during the buried oxide dry etching, some areas over the device layer surface were etched exposing the silicon surface. Then, nanowires will grow also on these surfaces making nanowire growth more homogeneous over the substrate. The growth of highly density arrays in very isolated areas is more difficult because the catalyst decomposition is affected by the catalyst nanoparticles size and density [35] and, we have observed, that no homogeneous nanowire distribution can affect nanowire growth.

Finally, the DRIE mask (green color), as its name suggests, defines the zones where the DRIE will machine the silicon. Previous experience has shown that angular corners were very difficult to accomplish using DRIE. To that end, the mask corners of these layer were directly rounded in order to obtain devices more similar to what it had been designed. On the other hand, when performing bulk micromaching with DRIE the window of silicon designed to be opened grows. For that, the DRIE mask designed is not aligned at the cantilever base but it is separated from this around $20\mu m$ which is the distance that we have estimated from previos works at the CNM.

In addition, chip cut lines are defined in DEVICE and DRIE masks suspending large and small chips by three and two small legs. This legs can be easily broken with tweezers to extract chips without the need of a diamond saw that could damage and contaminate the structure.

3.5 Fabrication results

For the fabrication of the devices three different RUNs have been done. In the first one, very good results were observed but the yield production was very low. The main cause of this was produced by the poor uniformity of the commercially available SOI wafers. The fact that the device layer is oriented in the especial $\langle 110 \rangle$ direction made it more difficult to find uniform wafers. Despite that device layer was previously characterized and wafers were selected with the highest homogeneity possible, they presented at least 500 nm of dispersion. As the average device layer is of $2\mu m$, the thickness of the array growth area that we needed to grow in the device, is in the order of the minimum dispersion found in the wafers. This made that in some devices the nanowire area at the vertical sidewalls is higher than desired, which compromises the expected device performance, whereas in other it is completely etched in the first Si RIE step ending up with no area at all for nanowires growth. To that one should add the error made during the wafer

characterization and during the RIE etch process. This made that only a few devices presented the desired nanowire growth area for the optimal performance Fig.3.11. For next RUNs we were less conservative for this critical step to ensure that at least all the devices had nanowire growth area.

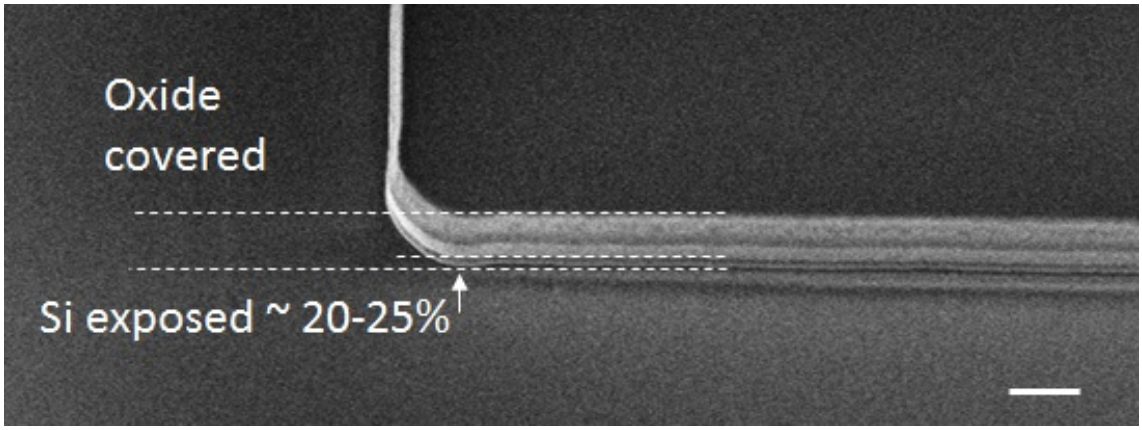


Figure 3.11: SEM image of cantilever thickness after the second Si RIE in which device layer is etched up to the buried oxide layer. The cantilever surface is covered with native oxide except at the bottom part of the trench sidewall where Si is exposed. Scale bar $1\mu m$.

Another critical step during the process was to open laterally the areas where nanowires are expected to grow. This is done, as is shown in the Fig.3.11 , by a lithography process that allows to etch the oxide of walls only at such areas. We took into account possible misalignments (of around $1\mu m$ for this kind of optical lithography) and overexposures, that could move or increase the window size making that nanowires could shortcut the electrodes in areas where the stress is null when the cantilever is deflected. Due to these consideration the process was successfully carried out in all the RUN process.

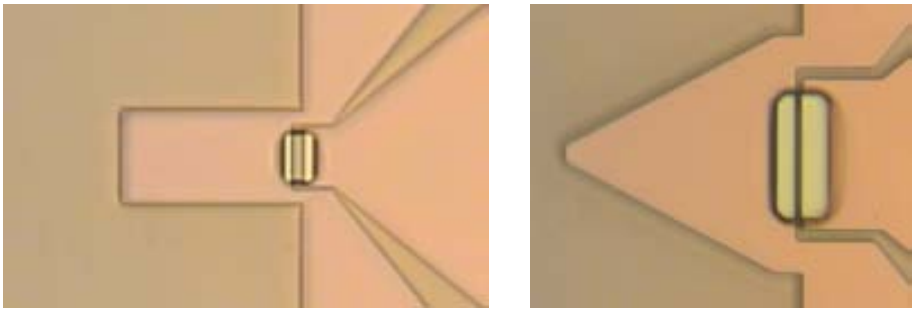


Figure 3.12: Cantilever images after the lithography step to define the nanowire growth areas by a wet etching. Images were taken from an optical microscope

Finally, the last critical step during the fabrication process is the back side DRIE to release the cantilever structure. The mask used for this process in the first RUN was the $6\mu m$ of annealed resist and the thermal oxide produced during the thermal oxidations of the process, of around $600nm$. The resist is normally deposited by spinning three layers until reach the $6\mu m$. Unfortunately, only the first two layers (around $4.5\mu m$) were deposited due to the bad adherence. Initially, we had estimated that, considering the selectivity of these two masks with respect to the DRIE, that would be enough for the

process. Unfortunately, the etch rate was slower than previously estimated and the two masks used for the process were consumed before that the etch process was completely finished. Here, we decide to continue with the process without use a mask and the handle layer of the wafer was etched uniformly until the buried oxide of the wafer was exposed in all the desired areas. As a consequence of this, one of the three wafers used in the process was broken. The other two wafers were satisfactorily etched except for some chips at the edge where a thin silicon film remained under the buried oxide, Fig 3.13.

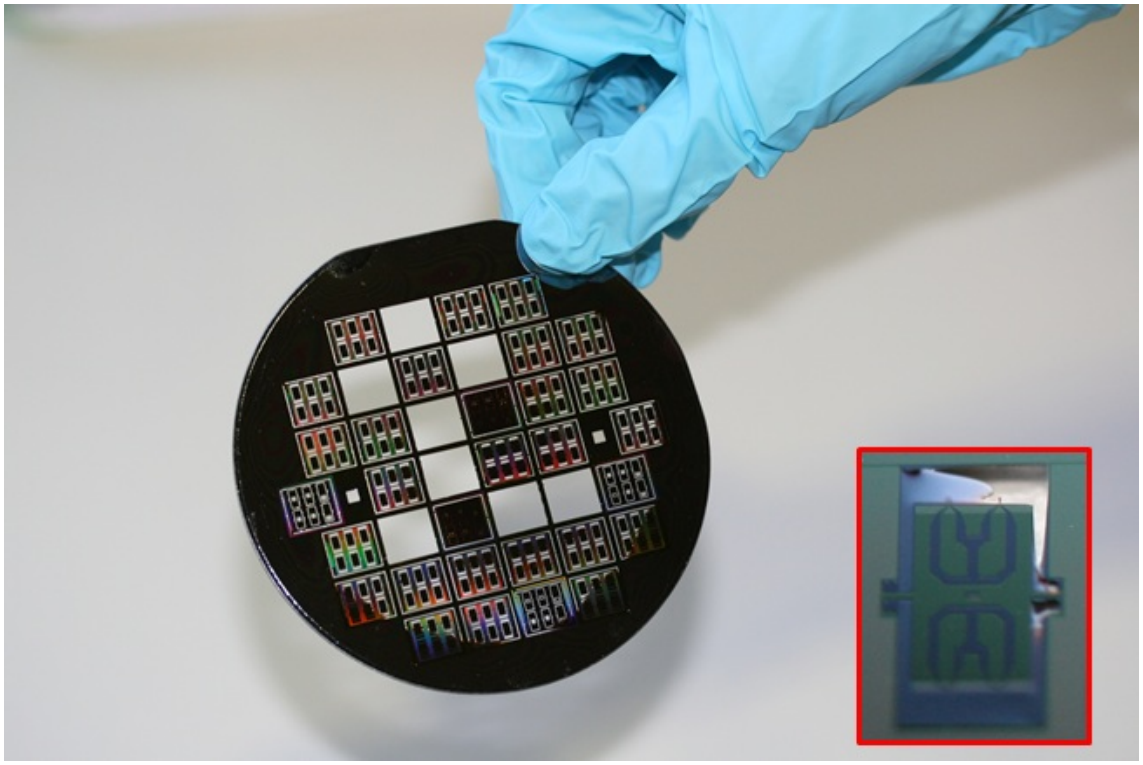


Figure 3.13: Piezoresistive canitilever wafer made in RUN1. Cantilevers in the central part of the wafer are correctly released while the DRIE has not finished releasing cantilevers from the edge of the wafer. In the red square, an image of one cantilever chip in which the cantilevers are not completely released.

Usually, in standard backside DRIE processes, an aluminum layer is used as a mask. However, we used an oxide layer to avoid possible metal contamination during this step that could alter the nanowire growth. Due to the bad results in the first RUN we decided to increase the oxide layer for the second one. A $2\mu m$ of deposited layer was used as a mask. Despite the oxide layer was thicker, it was consumed before releasing completely the cantilevers. Finally we made some successfully tests with aluminum masks and we decided to use them for the last RUN. The problem was then solved.

Taking into account these considerations in the technology process, the cantilevers were fabricated and ready for the nanowire growth. Chips were extracted from the wafer with the help of tweezers. In the Fig 4.5(a) a representative result of the fabrication process can be observed. A very selective growth of the nanowire array is observed just at the base of the cantilever and only in a small fraction of the total thickness. There are not any nanowires that can short-cut the electrodes in areas were the stress is null when the cantilever is deflected.

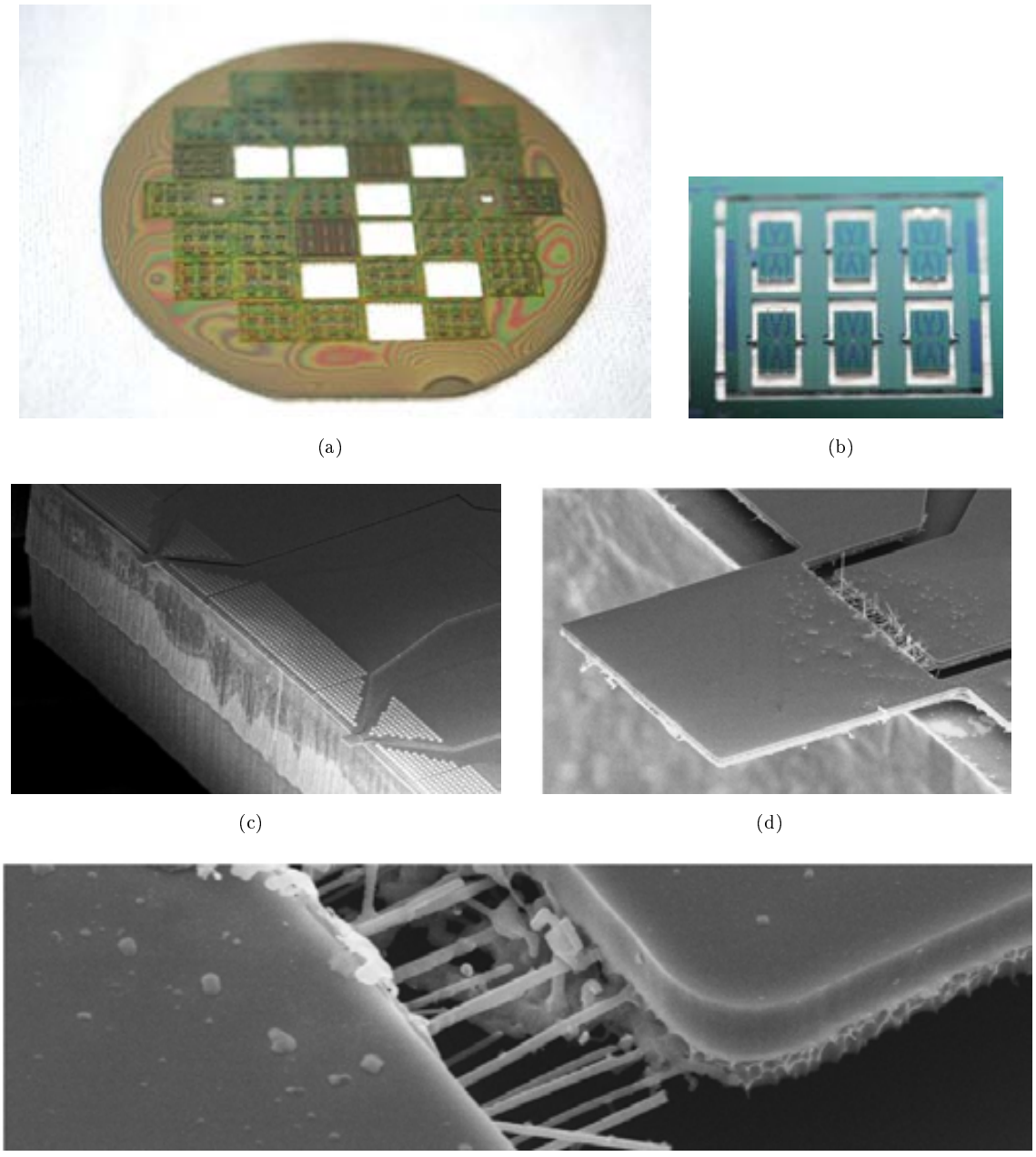
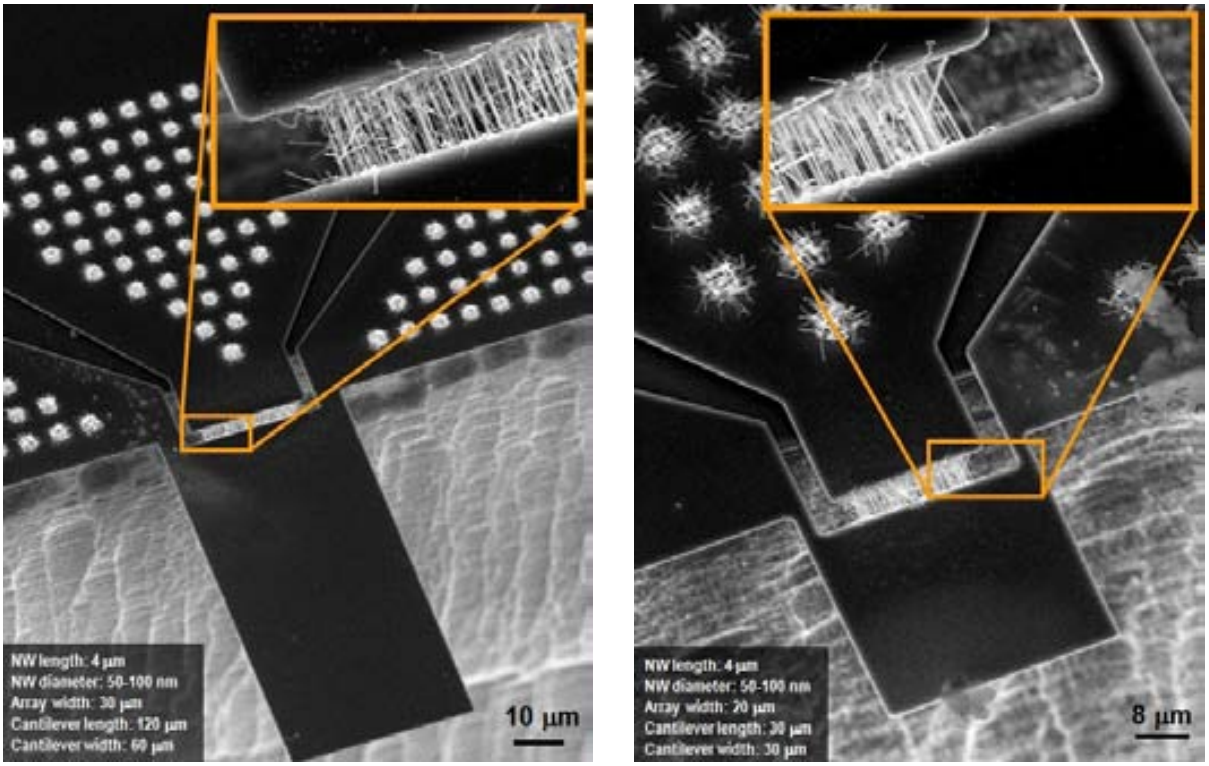


Figure 3.14: a)Typical piezoresistive cantilever wafer. b)Large chip for nanowire growth. The chip is composed by six small chips with typical AFM shape. c)SEM image of two cantilevers at the edge of the chip. d) SEM image of one of the cantilevers of previous image. The cantilever has $30\mu m$ of width and length, the nanowires has $2\mu m$ in length. e) SEM image of nanowire growth area in the cantilever. The growth is selective in a fraction of the cantilever thickness. However, improvements in array morphology and epitaxy are needed.

However an improvement in the growth conditions was necessary in order to obtain a more uniform array. In addition, amorphous growth was observed in the cantilever array and in some cases nanowires grown over the cantilever neutral plane. An improvement in the nanowire array was observed by tuning the growth conditions. Arrays with lower distribution of diameters and with better epitaxy were achieved by tuning the growth conditions, Fig 3.15.



(a) (b)

Figure 3.15: Piezoresistive cantilever fabrication results. In this case the cantilever present better epitaxy, lower diameter distribution and higher density than in the Fig 4.5(a). The catalyst deposition conditions are microemulsion parameter R=20, deposition time 15s and temperature 50°C. Growth temperature 755°C, direct flow Ar/H_2 270 sccm $SiCl_4$ flow 40sccm. Insitu p-doping with B (1sccm of BBr_3).

3.6 Characterization of the cantilevers

For the kind of devices that have been designed the most important parameter is the displacement resolution which is given by the noise level over the sensitivity. First we perform IV measurements to check the ohmic electrical behaviour. We get typical resistances in the 10 to 100 $k\Omega$ range.

3.6.0.1 Chip Encapsulation

For cantilever characterization, geometries of the AFM holder have been considered in order to choose the PCB in which the cantilever is integrated. It is important that the PCB design gives the possibility of made measurements both in tension and in compression with the use of an AFM tip. For the measurement one of the PCB used at the CNM for the encapsulation of other kind of devices has been employed. A small finger has been added to the original layout to ensure that the two kinds of measurements can be realized without any part of the AFM holder.

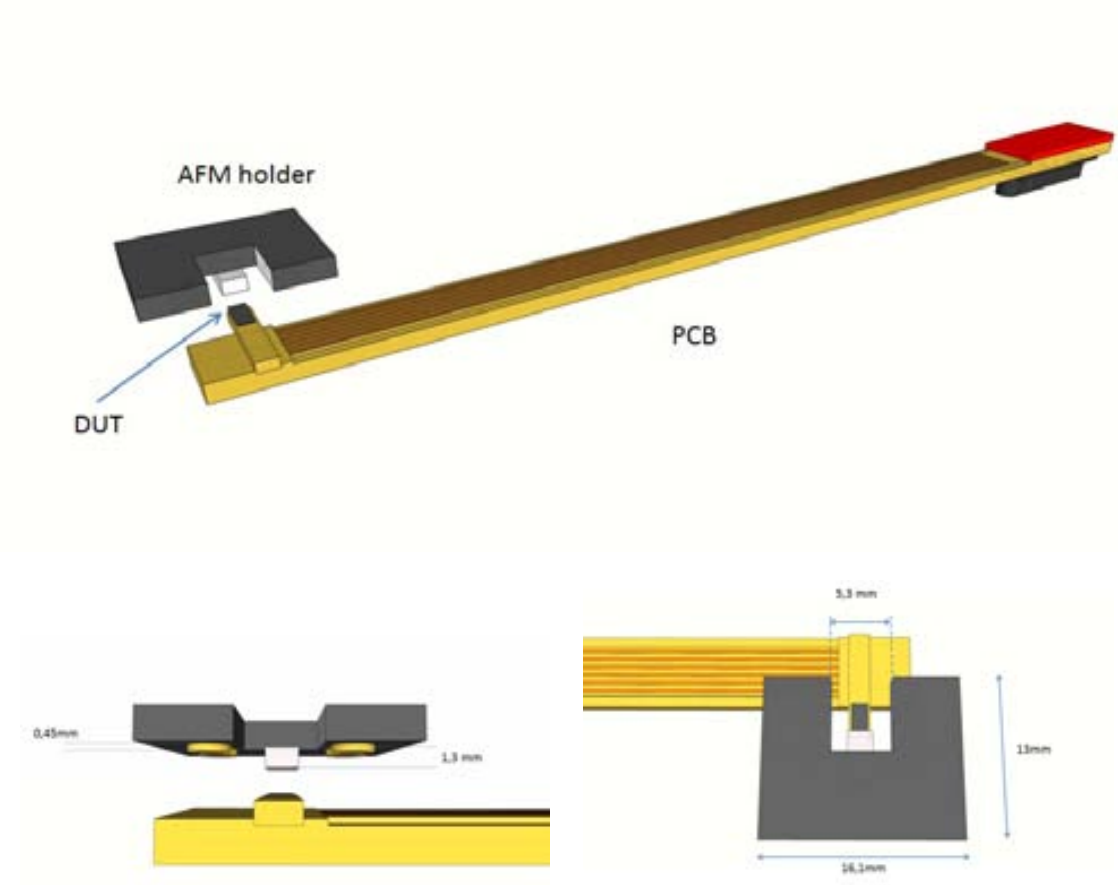


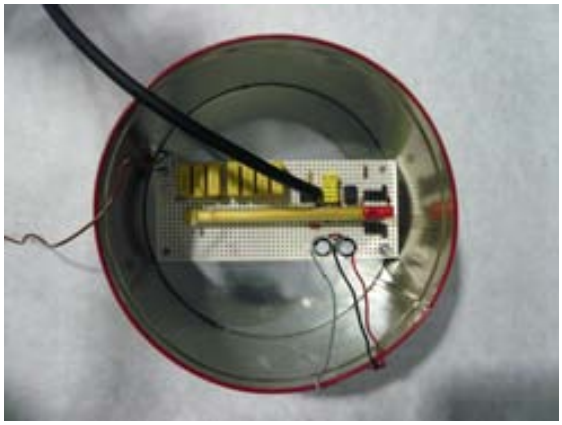
Figure 3.16: Cantilever chip encapsulation for AFM measurements

Electrical bonding has been made directly over the silicon pads. For this is critical that an HF etching of the native oxide must be realized just before of the bonding to ensure ohmic contacts. The contact resistance of the pads was measured by using a four prove set up resulting in a resistance in the order of few hundreds of ohms to one $k\Omega$. Considering than the device total resistance is one or two orders of magnitudes higher, the effects in the cantilever performance are negligible. However, for future fabrication of this kind of devices the metallization of the electrical pads could simplify the wire bonding process, by elimination the need of a wet etching only a few minutes before.

3.6.1 Noise characterization

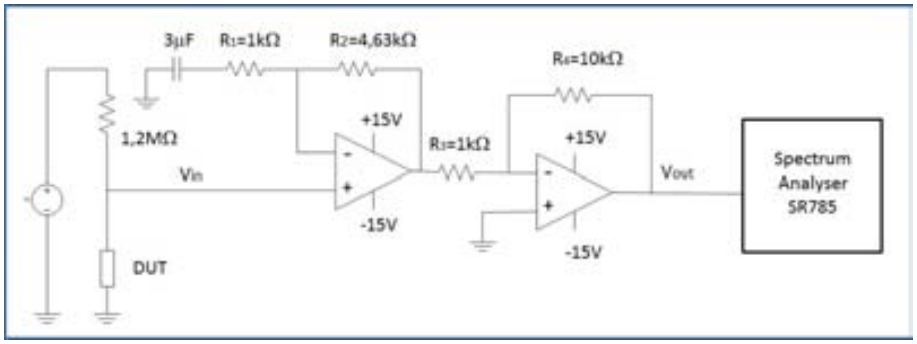
For device noise characterization the design of an amplification circuit has been needed. As it was explained previously the dominant sources of noise are given by the thermal and the Hooge noise at low frequencies. So then, the amplification circuit has been designed to analyse low frequency noise. The characterization set-up is shown in the Fig. 3.17.

For the realization of the custom amplifier a low noise operational amplifier has been used. The main characteristics are represented in the table 3.4.



(a) Image of custom amplifier

(b) Spectrum analyser SR785



(c) Schematic for custom amplifier

Figure 3.17: Set up for noise characterization

Equivalent input Voltage noise	$12nVHz^{-1/2}$ f=1000 Hz
Equivalent input Current noise	$0.01pAHz^{-1/2}$ f=1000 Hz
Gain Bandwidth Product	5 MHz

Table 3.4: AC Electrical characteristics LF356 JFET Operational Amplifier.

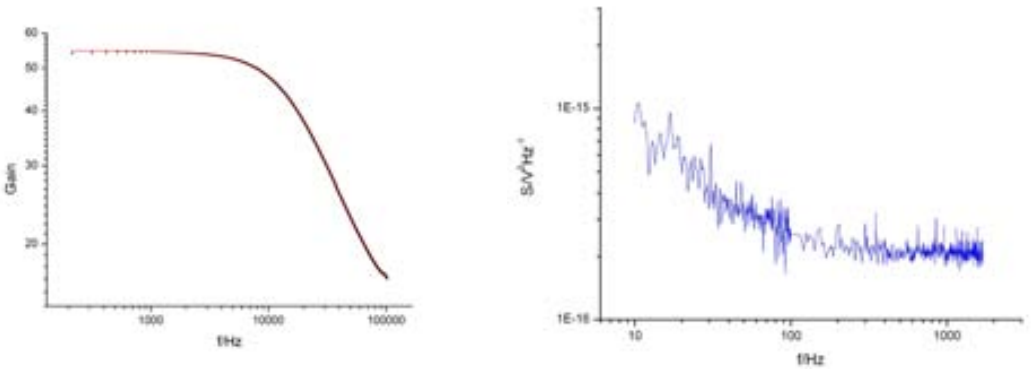
The amplifier circuit gain Fig 3.18(a) and noise spectrum have been characterized with the help of the spectrum analyser. The Gain curve,, is relatively flat over the region of interest ($\langle 10kHz$) with a gain of around 54.

For a more precise study of the gain, G, as a function of the frequency f, the curve has been fitted to the next function:

$$G = \frac{V_{out}}{V_{in}} = A + (B - A)\frac{f^n}{k^n + f^n} \tag{3.26}$$

where A, B, k and n are the fitting parameters whose values are showed in the next table:

The noise of the amplification circuit is shown in the Fig 3.18(b). The noise floor



(a) Gain curve for the custom amplifier (b) Amplifier noise floor

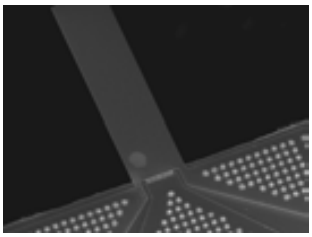
Figure 3.18: Amplifier circuit characterization

A	54.80 ± 0.01
B	13.37 ± 0.02
k	24879 ± 15
n	1.732 ± 0.002

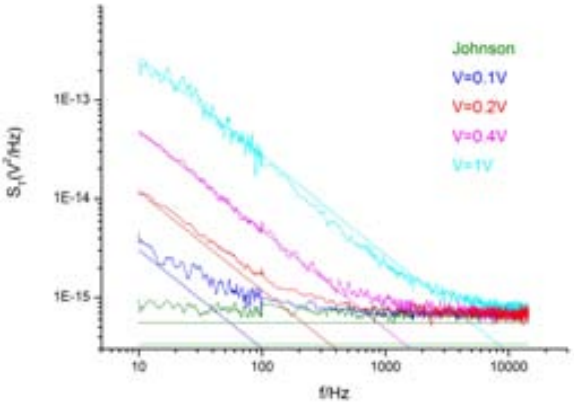
Table 3.5: Coefficient for the Gain equation

is in the order of $1.410^{-8} VHz^{-1/2}$ which corresponds to the thermal noise of an equivalent resistance of around $12k\Omega$. This means that the designer circuit is valid for noise amplification in devices with a higher resistance value than the equivalent resistance of the amplifier. In our devices typical resistance values are between 10 and $100k\Omega$ so the amplifier circuit is valid for their characterization.

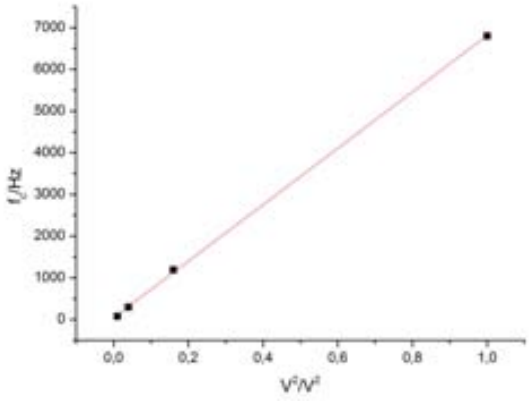
The noise has been characterized for cantilevers of different dimensions. The two dominant sources of noise observed in all of them are thermal and Hooge noise as it is expected for this kind of devices. In order to have a higher sensitivity, nanowires are lightly doped. That could have negative effects in the piezoresistive cantilever noise. Due to Si nanowire in the array are electrically connected in parallel a simple way to reduce the total resistance and the number of carriers in the array is increasing the number of nanowires. To study the effect of the number of nanowires in the noise spectrum, the noise of cantilevers with different array dimensions has been studied.



(a) SEM image

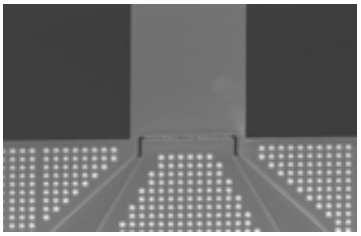


(b) Noise spectrum and fitting

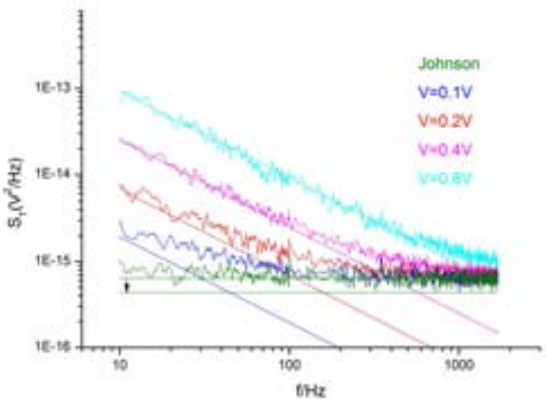


(c) Corner frequency

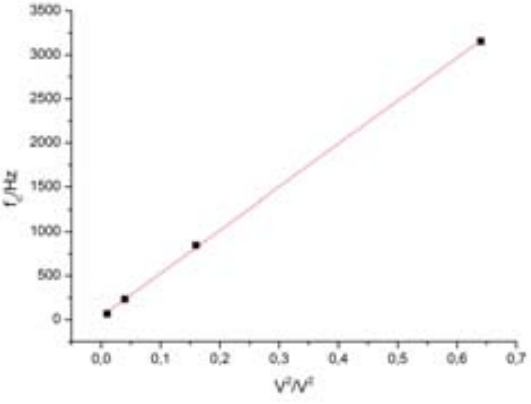
Figure 3.19: Noise characterization of a piezoresistive cantilever of 60μm width and 480μm lenght and 2μm of nanowire length. Cantilever resistance 24500Ω



(a) SEM image



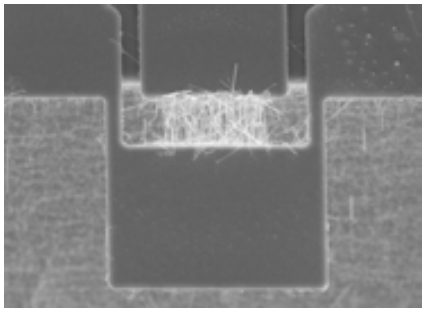
(b) Noise spectrum and fitting



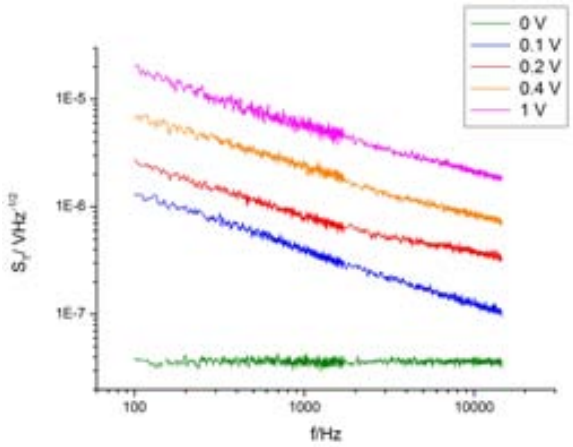
(c) Corner frequency

Figure 3.20: Noise characterization of a piezoresistive cantilever of 120μm width and 120μm lenght and 2μm of nanowire length. Cantilever resistance 17900Ω

In Fig 3.19 and Fig 3.20 two cantilevers can be observed with nanowires of $2\mu m$ in length. The cantilevers have different width, the first one is $60\mu m$ width while the second one is of $120\mu m$. Both cantilevers belong to the same chip in the wafer and then the catalyst deposition and the nanowire growth have been made at the same time. This means that we can expect similar nanowire doping, density and diameter distribution. The theoretical Johnson noise has been represented by a green line in the noise spectrum. This noise corresponds with the measured experimentally if we extract the noise of the operational amplifier. The Hooge noise has been correctly fitted to a f^{-1} function. From the fitting we can extract the corner frequency for devices. It can be observed that they present similar and relatively low corner frequency, in the range of 1kHz-10kHz for 1V of polarization, but the second cantilever presents a lower thermal noise due to the higher number of wires connected in parallel.



(a)



(b)

Figure 3.21: Cantilever noise spectrum. The cantilever width is of $30\mu m$ and the nanowire length of $8\mu m$

However, some characterized cantilevers presented unusually high Hooge noise. The corner frequency increases to frequencies higher than 100kHz, which is the bandwidth of the spectrum analyzer. From SEM image, Fig 3.21, of cantilevers with unexpected high noise we concluded that this noise was produced due to the poor epitaxy of nanowires. It was observed preferably in cantilevers with longer nanowires, of $8\mu m$. Long and thin nanowires usually present buckling and form bad electrical connections with the opposite wall. A representative example is plotted in the Fig 3.21. The corner frequency for this device is in the order of megahertzs.

In conclusion, the noise spectrum measured in piezoresistive cantilevers shows that two dominant sources of noise were thermal and Hooge noise. The noise measured is in the order of noise that we can expect for silicon nanowires. Corner frequencies have been estimated from the fit of Hooge noise and the thermal noise. These frequencies are in the order of a few kHz for 1V of applied voltage. These means that, a high pass filter can be used to remove the Hooge noise from our measurements.

3.6.2 Sensitivity and detection limit characterization.

Piezoresistive transduction was characterized by applying a controlled normal force on top of the cantilever with an AFM tip and simultaneously measuring the change in the resistance of the array by using a lock-in amplifier. An AC voltage is applied to one electrode while the other is connected to the lock-in input in a half-wheastone configuration. A representative plot of the measurement set up is shown in Fig 3.22.

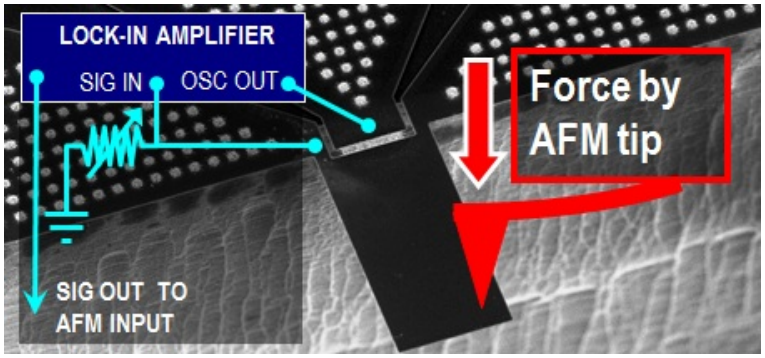
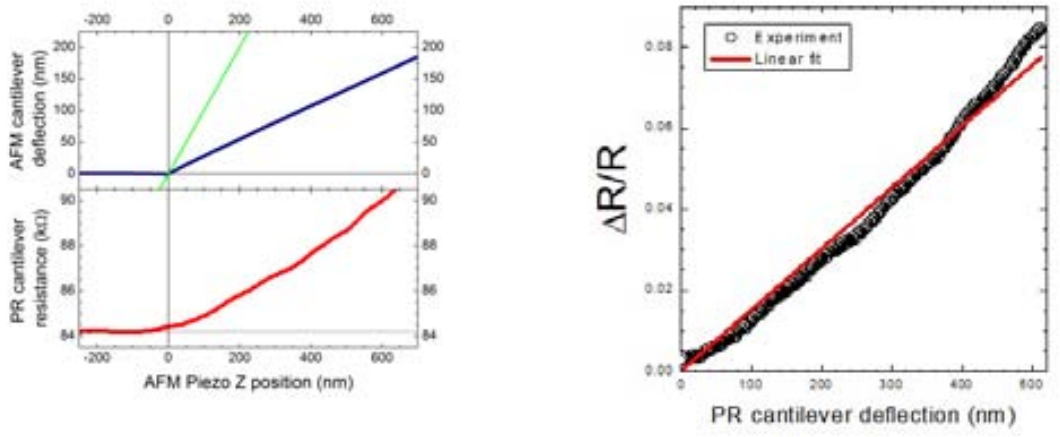


Figure 3.22: Sensitivity characterization set up

Some representative results of characterization are analysed next. The Fig 3.23(a) is a typical measurement in which we simultaneously measure the AFM cantilever deflection and the nanowire array resistance as we move the AFM tip towards the cantilever by means of the AFM vertical piezo. In the AFM cantilever deflection measurement (blue line) we get a typical contact mode curve except for the slope in the contact region, which is different from one (green line) due to the piezoresistive cantilever bending. In the resistance measurement we observe that a change in resistance starts right at the point when the AFM tip begins to apply a force, and increases monotonically as the force keeps on increasing. This increment is positive since the mean stress in the nanowire array is tensile. From this two measurements we can extract a plot of change in resistance vs piezoresistive deflection. The slope of this curve will be the sensitivity for the device that in this case is of 1.5 $10^5 m^{-1}$ which is around one order of magnitude larger than typical values of conventional piezoresistive cantilevers.

The minimum detectable displacement or resolution will be given by the noise in the bandwidth of measurement over the sensitivity. The bandwidth of measurement has been fixed by the locking amplifier. For these measurements, as it has been commented previously, the performance was 1kHz of bandwidth around the central frequency of 10kHz.

For this range of frequencies, the dominant source of noise will be the thermal noise which integrated over the bandwidth will produce a noise of $1\mu V$. Then, the cantilever resolution is 6pm while state of the art in piezoresistive cantilevers based on Si bulk with similar characteristics is 10pm [4].



(a) (b)

Figure 3.23: Characterization of a piezoresistive cantilever (dimensions length $60\mu m$, width $30\mu m$ nanowire length $2\mu m$ resistance $R = 84k\Omega$). The voltage applied in the semi-Wheatstone bridge is $2.5V$, the reference frequency in the lock-in is 10kHz and the time constant 1 ms.

The curve in the Fig 3.24 has been extracted from the characterization of a piezoresistive cantilever with similar dimensions to the previous one but in this case the measurement range has been increased. First, it can be observed that the relative change in the resistance is nonlinear. It could be easily understood since the gauge factor in Si nanowires studied by He and Yang was in many cases nonlinear [17].

In this case the curve can be fitted correctly to a second degree polynomial. The sensitivity can be approximate to the first order term that in this case is 4.5 $10^{-4}m^{-1}$. On the other hand, we can observe that the cantilever change of resistance saturates for values higher than $2\mu m$. The order of magnitude of applied strain is similar to that applied using the four-point bending set up used by He and Yang. It can be estimated from the FEM simulations. However, a precise estimation of mean strain is not possible due to the complexity of the structure. This means that we can estimate a precise value of the gauge factor for the structure. Nevertheless, the values of sensitivity obtained for this cantilever are compatible with high piezoresistive coefficients.

The cantilever characterized in the Fig 3.25 have a very low doping level. The resistance is non linear and has been polarized with 3V to obtain a resistance of $300k\Omega$. The applied stress in nanowire array is compressive and then the resistance decreases when the cantilever is deflected. In this case, the relative change of resistance can be correctly fitted by a line. From the slope we have obtained a sensitivity of 0.9 $10^{5}m^{-1}$. This value is also compatible with high values of gauge factor.

On the other hand, similarly to the second device analyzed, Fig 3.24, there is a maxi-

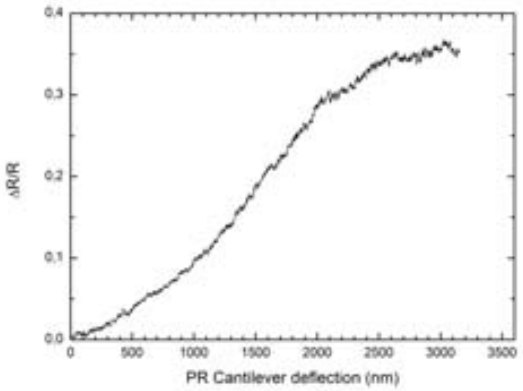


Figure 3.24: Characterization of a piezoresistive cantilever (dimensions: length $60\mu m$, width $30\mu m$ nanowire length $2\mu m$ resistance $R = 118.5k\Omega$).Relative change of resistance vs cantilever deflection. The voltage applied in the semi-Wheatstone bridge is $2.5V$, the reference frequency in the lock-in is 10kHz and the time constant 1ms

mum in the cantilever change of resistance. In this case the dynamic range of device only reaches $1\mu m$. In this case we can assume that the piezoresistive behavior of nanowires is similar to curves type z, Fig 3.3(b) observed for bottom up nanowires **??**. The noise in this cantilever due to the low doping level is high and therefore, despite it has a high sensitivity, the resolution will be very high.

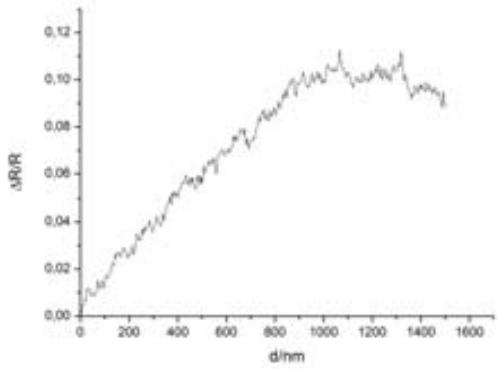


Figure 3.25: Cantilever characterization. Cantilever dimensions: length $120\mu m$ and width $30\mu m$ The nanowire array is lightly doped and the IV curve is not lineal. The cantilever resistance is $300k\Omega$ when is polarized with 3V.

In conclusion, the sensitivity characterization has been realized. Results showed that sensitivity values are compatible with high values of gauge factor although a precise value can be extracted due to the complexity of the structure. On the other hand we have observed that some devices have nonlinear sensitivity and the dynamic range of devices is limited in the range of few microns. We assume that this behavior is similar to that obtained for nanowires with higher resistivity and small diameters in previous studies **??**. However, we found a very high sensitivity compared with similar devices based on bulk Si.

3.7 Conclusions

The fabrication of a cantilever that exploits the extraordinary piezoresistive properties of Si nanowires has been demonstrated. The design is based on the standard double leg piezoresistive cantilever. The use of a nanowire array improves the sensitivity not only due to the giant piezoresistance characteristic reported in nanowires but also because nanowires act as stress accumulators. The cantilever array has been successfully grown selectively at the base of the cantilever and only in a fraction of the total thickness of the cantilever to ensure that only compressive or tensile stress occurs when the cantilever is deflected. However, due to the low homogeneity of the SOI device layer we did not have a precise control in the array thickness which in some case compromised the cantilever performance and the yield production has been lower that the initially desired. By some modifications in the process flow we have been able to improve the yield fabrication but the control in the array thickness continues being low and more uniform wafers would be necessary.

The noise and sensitivity characterization of the cantilevers has been realized. The noise analysis shows that the two dominant sources of noise are the Thermal and Hooge noise due to the high nanowire resistance. Most of cantilevers present a relatively low corner frequency so this means that the noise can be limited to the Thermal noise. The sensitivity has been characterized by applying a controllable normal force with an AFM and simultaneously measuring the change of the resistance with a lock-in amplifier. A high sensitivity was obtained compared to similar devices based on piezoresistive Si bulk. The best value obtained for the cantilever minimum detectable displacement is of 6 pm which is lower than that previously reported for cantilevers with similar characteristics based on Si bulk. These values of sensitivity and resolution are comparable with the previously estimated by FEM simulation which means that are compatible with high values of gauge factor.

Future improvements of technology process would allow the fabrication of higher sensitive piezoresistive devices. The electrode metallization, for example, would result in a decrement of the parasitic resistance that in some cases are comparable with the array resistance. SOI wafers with higher homogeneity would allow a higher control of cantilever thickness and then of the cantilever fabrication yield. And finally, a higher density array with smaller nanowire diameters and narrow distribution would also produce an improvement in the cantilever performance.

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Chapter 4

Single Si nanowire device fabrication technology: application to nanomechanical sensors based on nanowire resonators

Contents

4.1 Introduction and motivation 99

4.2 Technologies based on colloidal catalyst 100

4.3 Technologies based on galvanic displacement 103

4.3.1 Objectives 103

4.3.2 Process Flow 103

4.3.3 Fabrication Results 105

4.4 Characterization results 108

4.4.1 Nanomechanical resonators for optical readout 108

4.4.2 Nanomechanical resonators for electrical readout: capacitive sensing 110

4.4.3 Nanomechanical resonators for electrical readout: piezoresistive sensing 110

4.5 Conclusions 111

References 113

4.1 Introduction and motivation

Nowadays, trends in semiconductor devices are rapidly being miniaturised into submicron scale. Nanomechanical structures provide extremely high resonant frequencies in microwaves, small active masses in femptograms and high quality factors (Q in the range $10^3 - 10^5$)[1, 2]. This powerful combination translates into opportunities for nanoelectromechancial sensors (NEMS) and in particular for mass sensing applications. These devices operate by providing a shift of resonant frequency when a small amount of mass is deposited on the mechanical structure surface. In general, the smaller is the resonator, the more sensitive it is, because the relative change of mass is larger and the frequency quality Q factor should decrease as the nanowire dimension decreases, due to effect related with surface losses[3].

For a mechanical resonator, assuming that the added mass, δm, is a small fraction of the resonator effective mass, M_{eff}, and does not modify sensor stiffness, the mass resolution (i.e. the minimum mass detectable) can be approximated by:

$$\delta m = \frac{\partial M_{eff}}{\partial \omega_0}\delta\omega_0 = R^{-1}\delta\omega_0 \tag{4.1}$$

where $\delta\omega_0$ is the minimum detectable frequency shift, delimited by the intrinsic and extrinsic sources of noise[1], and R the mass frequency responsivity. Using the approximation of harmonic oscillator where the resonant frequency is related with the effective spring constant, K_{eff} and the resonator effective mass by: $\omega_0 = \sqrt{K_{eff}/M_{eff}}$, the mass frequency responsivity is given by:

$$R = \frac{\partial\omega_0}{\partial M_{eff}} = -\frac{\omega_0}{2M_{eff}} \tag{4.2}$$

From this expression we can observe that the responsivity will be improved by the use of smaller devices, with higher resonant frequency and lower effective mass.

Nanoscale resonators have been traditionally fabricated by top-down lithography techniques. However, while resonators fabricated by top-down technologies have achieved mass sensitivities in the zemptograme range, $(10^{-21}g)$ [4, 5, 6], devices based on nanowires and nanotubes have approached the yoctogram scale $(10^{-24}g)$ [7, 8, 9, 10, 11, 12] and the ultimate detection limit corresponding to mass of one single atom $1Da = 1.66yg$. Bottom-up approaches provide nanowires with unique attributes such as high crystalline quality and atomically smooth surfaces. Additionally, they can offer the advantages of higher throughput, as well as access to length scales smaller than those which can be traditionally achieved with standard fabrication techniques which are limited by the lithography resolution, the etch roughness and the synthesis of epitaxially grown substrates.

However, in spite of their potential, device integration of bottom-up horizontal aligned silicon nanowires is not completely controlled. The more extended approach for the bottom-up nanostructure integration in functional devices involved the off-chip synthesis followed by its deposition on the substrate surfaces[9]. This soft assembly approach for resonator fabrication offers limited stiffness of clamping point, which has negative consequences in the resonant quality factor of devices. Otherwise, the direct growth of epitaxially grown suspended nanowires presents important improvements in their mechanical[13] and electrical[14] properties coming from their rigid and electrically continuous clamping points. So far, the fabrication of devices based on epitaxially grown single nanowires has been made by the deposition of colloidal nanoparticles into substrates with predefined microtrenches and structures. Statistically, some of these deposited catalyst nanoparticles produce the growth of nanowire growth in a desired position and can be used for the device. Then a more precise control of the nanowire growth position is needed in order to improve the device yield.

4.2 Technologies based on colloidal catalyst

Colloidal nanoparticles are frequently used as catalyst seeds for nanowire growth[11, 9, 15]. There is a large range of commercially available nanoparticle diameters with a very narrow size distribution. Since nanoparticle size distribution mirrors the nanowire diameter[16, 17] their use as seeds gives us a precise control over nanowire dimensions. However, nanoparticles are randomly deposited and this do not allow a large scale integration of single nanowire devices.

Nevertheless, some transduction mechanisms, such as optical detection, do not require of nanowire integration on complicated structures. Here the use of colloidal nanoparticles for nanowires growth could simplify the process and additionally give a precise control over nanowire dimensions. These nanoparticles were used for catalyst grown silicon nanowires at the sidewalls of prefabricated trenches of SOI wafers with sidewalls oriented in the $\langle 111 \rangle$. An example is shown in the Fig 4.1.

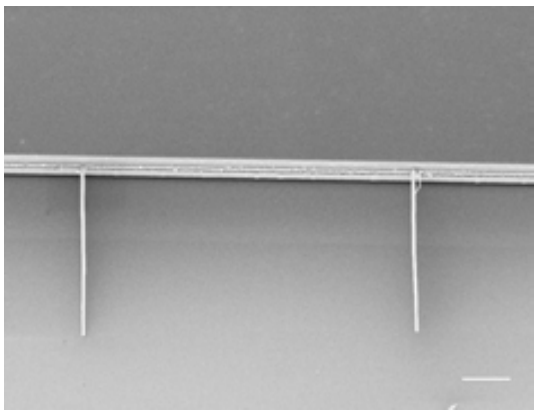
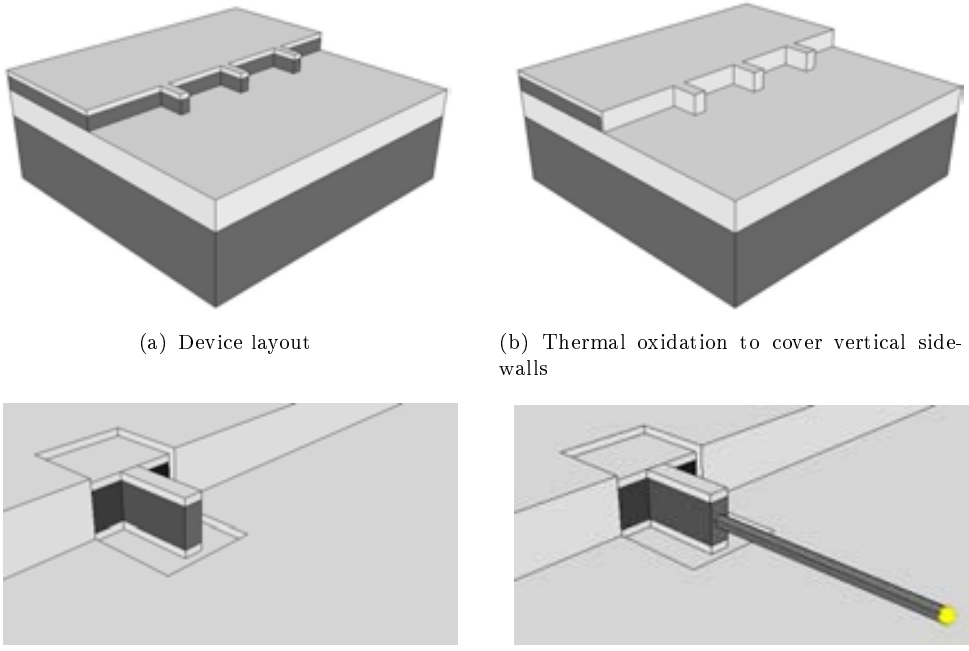


Figure 4.1: SEM image of Si nanowires grown from colloidal nanoparticles. Scale bar $5\mu m$

Before catalyst deposition, substrates are cleaned in acetone and isopropanol for 10 min and then rinsed with deionized water before drying in gentle N_2. Then sort wet etching with HF is made to remove the native oxide layer on Si surface. And finally, a thin film deposited polyelectrolite layer, poly-L-lysine is used to electrostatically attract to and immobilize gold colloids on the substrate to act as seeds for Si nanowire growth. The nanowire density can be controlled by diluting the colloidal solution in deionized water or changing the deposition time.

On the other hand, the integration of nanowires in more complex structures requires a more precise control of nanowire position and, in this case, colloidal nanoparticles are only useful for prototype fabrication. As it was commented previously, the addition of an acid to the colloidal solution can be used to improve the selectivity[18]. At low pH, negative ions covering colloids surface to avoid agglomeration, are neutralized. The resulting neutral nanoparticles present a poor adhesion onto silicon oxide surfaces that can be used to selective growth of nanowires.



(a) Device layout

(b) Thermal oxidation to cover vertical sidewalls

(c) Wet etching of thermal oxide on areas for nanowires growth

(d) Colloidal nanoparticles deposition and nanowire growth

Figure 4.2: General process for the fabrication of Si nanowire resonator with colloidal nanoparticles.

We have used acidified colloids for the fabrication of prototype devices based on single Si nanowires. For this we have defined electrodes layout covered with oxide and then we have exposed Si surface in areas where nanowires have to be grown. The main fabrication steps for this technology are shown in the Fig 4.2. First, device microstructures are defined by lithography and dry etching steps on device layer of SOI wafer and then covered with a thermal oxide. After that, oxide is removed by wet etching in areas where nanowire growth is desired Fig 4.2(c). Then acidified colloidal nanoparticles are used to catalyze the nanowires growth, Fig 4.2(d). The solution was prepared by adding a 0.1 M of HF to the colloidal solution previously diluted to obtain the desired nanoparticle concentration.

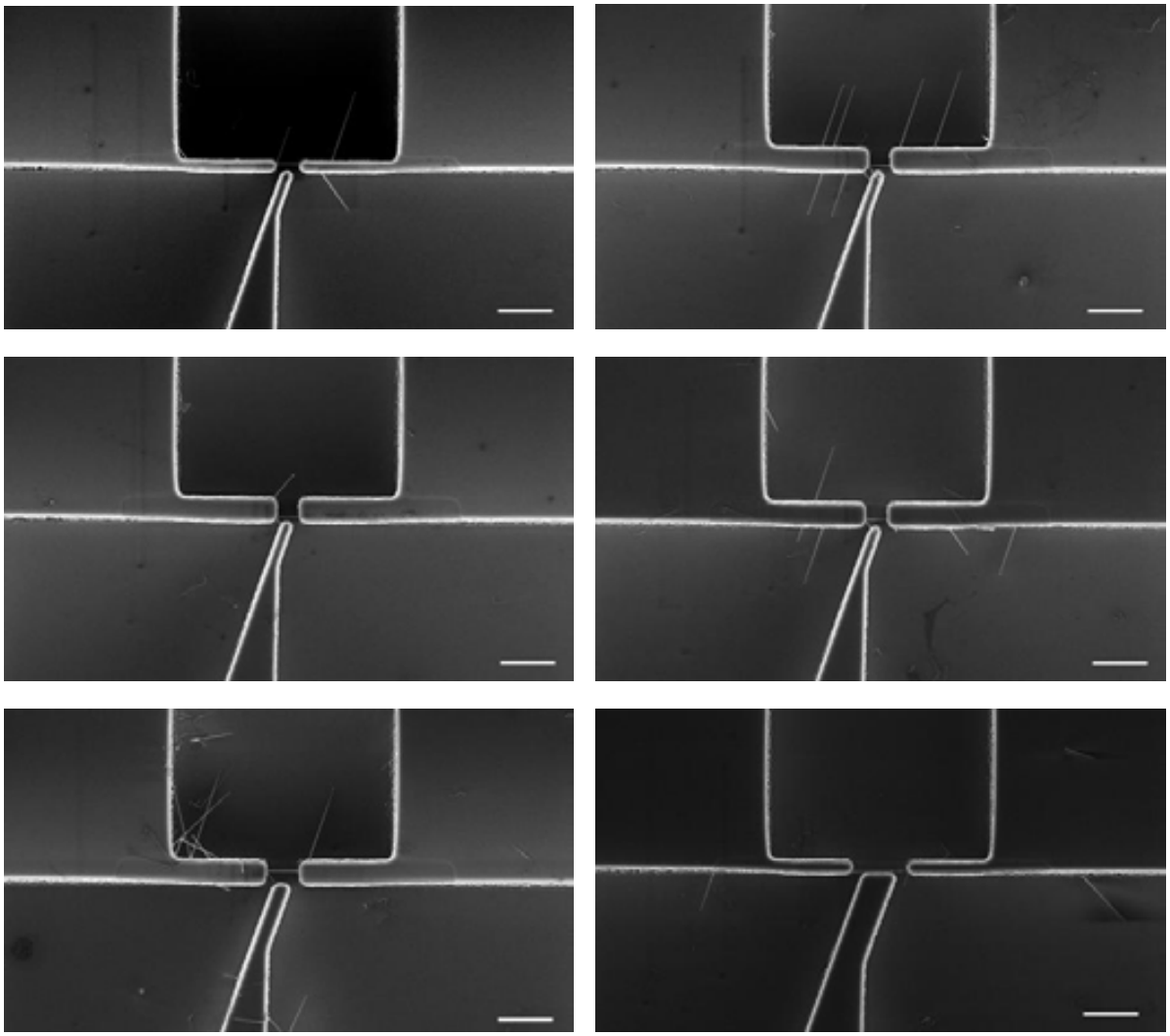


Figure 4.3: Single nanowire resonator. Catalyst nanoparticles are colloidal nanoparticles diluted in DI water and with HF. Scale bar $5\mu m$.

Gold nanoparticles deposition was realized by immersing substrates during 2 min and without any previous polyelectrolyte deposition.

Some representative results of the use of acidified colloids are shown in Fig 4.3. Nanowires grow preferentially in areas where Si surface is exposed. We have a very good control over nanowire dimension; however, the yield with this technology is still very low. Defined areas for nanowire growth are so big and deposition is not very uniform in the chip. We have reduced the probability that some additional nanowires, that do not form part of the device, can produce undesired shortcuts, but many electrodes are bridged by several or any nanowire instead of a single one. Then this technology is only valid for the fabrication of test structures but not for large scale.

4.3 Technologies based on galvanic displacement

4.3.1 Objectives

In the case of resonators with capacitive actuation and/or readout a more precise control of nanowire position is required. The nanowire must be located as close as possible of the excitation and readout electrode to increase the actuation force and the signal respectively. In addition, for double clamped nanobeams the nanowire must bridge the two electrodes taking care of possible shortcuts produced by other nanowires. As it was explained in the previous section, the use of acidified colloids improves nanowire position control; however, the catalyst deposition is not very homogeneous and device yield is still very low.

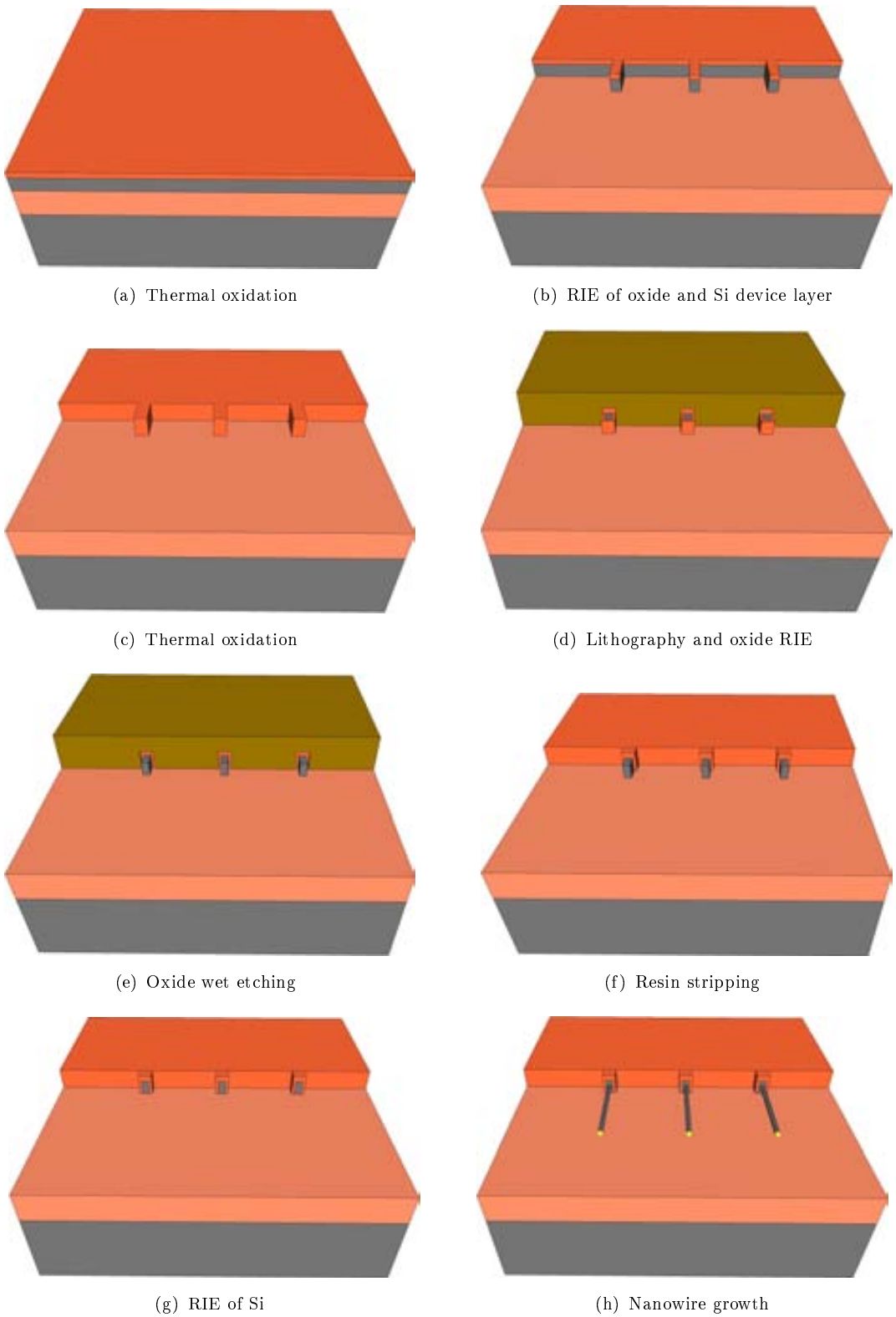
An alternative technological process has been designed for device integration of individual Si nanowires in NEMS devices. In this case, galvanic displacement techniques will be used for selectivity deposit gold on small Si areas previously defined by a combination of oxidation and lithography steps. Unlike colloidal deposition, galvanic displacement techniques produce a very selective and uniform catalyst deposition which is beneficial for large scale device fabrication.

4.3.2 Process Flow

A general process, Fig 4.4, for the fabrication of horizontal single nanowire into devices has been designed. This process has been used for the fabrication of different kind of devices in which more specific additional considerations must be considered with device design. For this process, SOI wafers with $2\mu m$ of Si device layer oriented in the $\langle 110 \rangle$ are used. Device layer of the SOI wafer was reduced to $1\mu m$ by several steps of thermal oxidation and oxide wet etching.

The fabrication process started with a thick thermal oxidation of around 400nm Fig 4.4(a). Then device layout is defined by a stepper optical lithography followed by a dry etching of the full oxide and of the device layer until the buried oxide layer, Fig 4.4(b). In this step, thinner fingers are defined at the position where nanowire growth is desired. The width of these structures will delimit the exposed area for the catalyst deposition and for that we chose it to be the critical dimension of the lithographic technique used, 700nm.

In the next step, a second thinner oxidation, of 100nm, is made to cover vertical surface, Fig 4.4(c). By effect of the oxidation, lateral dimensions of structures are reduced by effect of the Si consumed during the step (around a 45 nm per each 100nm of the total grown oxide thickness). Finally, fingers are cut close to the base showing a small silicon surface at the vertical walls. However, to ensure that the cut is realized correctly and exposed Si is only at vertical $\langle 111 \rangle$ surface and not in other directions, which could produce the



(a) Thermal oxidation

(b) RIE of oxide and Si device layer

(c) Thermal oxidation

(d) Lithography and oxide RIE

(e) Oxide wet etching

(f) Resin stripping

(g) RIE of Si

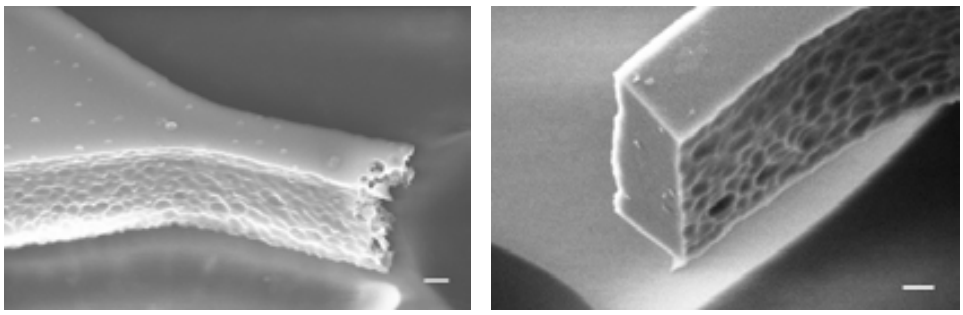
(h) Nanowire growth

Figure 4.4: Main Fabrication steps for the fabrication of devices based on single nanowires. Color grey silicon, orange oxide and green color photolitho resin.

nanowire growth in a non-horizontal orientation, the process is made by a combination of fabrication steps. First, a second lithography is made to cover with a resin all surface except the small fingers followed by an oxide RIE to remove the 400 nm of oxide at their top surface, Fig 4.4(d). Then, the 100nm of oxide at vertical walls is removed by a HF wet etching showing completely the Si finger bond Fig 4.4(e). This etch process is anisotropic so this means that the same amount of oxide has been etched under the resin. Then the resin is stripped, Fig 4.4(f), and Si is etched by a RIE using the top oxide as mask, Fig 4.4(g). In this way, we ensure that non silicon surface remains exposed at the top surface. Finally we proceed to the catalyst deposition followed by the nanowire growth, Fig 4.4(h).

4.3.3 Fabrication Results

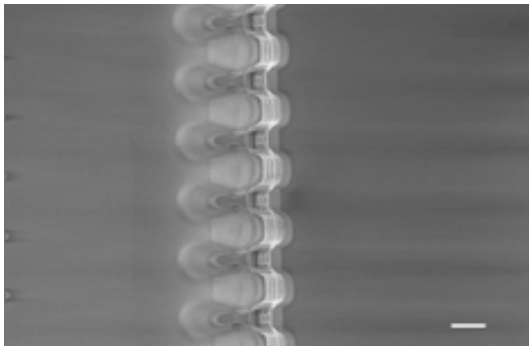
The fabrication process was successfully realized and adapted for different structures, Fig 4.5. The simplest ones were designed for the growth of ordered nanowires arrays ideal for the optical characterization Fig 4.5(a). Then, the technology has been adapted for the integration of electrodes or structures needed for the characterization of more complex devices. We have fabricated coupled cantilevers in which one of cantilevers is defined by optical lithography and the other by a single nanowire selectivity growth at the end of the first cantilever, Fig 4.5(b). And finally, we have designed structures for the piezoresistive transduction and capacitive actuation of double clamped beams in which the nanowire must be located as close as possible of electrodes, Fig 4.5(c) and Fig 4.5(d).



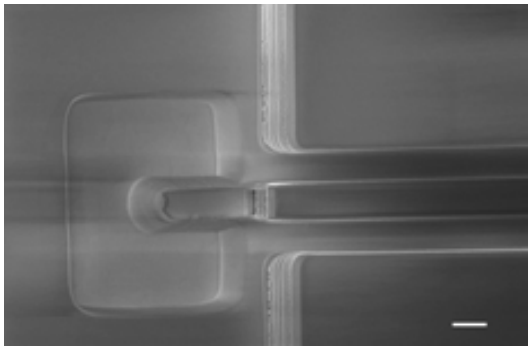
(a) (b)

Figure 4.6: SEM image of nanowire growth areas after oxide wet etching. a) Irregular surface due to the over etched during the Si dry etching. b) The surface roughness has been improved by a anisotropic wet etching by KOH during 1 min. Scale bar 200nm

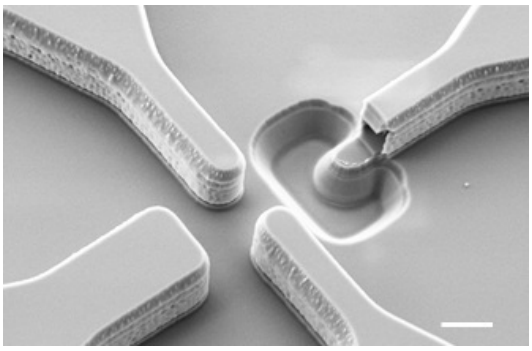
A critical step was the silicon RIE to define the growth areas. We had to ensure that the etching was made until the buried oxide. However, the over-etching produced an increment in the exposed silicon roughness that could help that nanowire growth in a $\langle 111 \rangle$ non perpendicular to the exposed surface. Due to the low uniformity of wafers some areas were over-etched for longer time producing a very irregular surface, Fig 4.6(a). In order to improve the surface roughness an anisotropic wet etching of Si was made by Potassium Hydroxide (KOH). In this case, anisotropic means that different crystals directions are



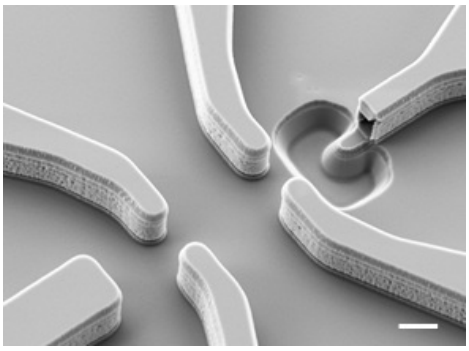
(a) Ordered Si nanowire arrays for optical detection



(b) Coupling cantilevers



(c) Piezoresistive double clamped beams.



(d) Piezoresistive double clamped beams for the excitation of higher modes.

Figure 4.5: SEM image of different structures fabricated, Scale bar $1\mu m$

etched with different etch rates. This differences between etch rates make the slower planes, the {111}, remain when the etching is being performed. Silicon oxide, with etch rate in the range of $10nm/min$ is used as a masking layer in the process. As result, after 1 min of KOH etching a perfectly flat $\langle 111 \rangle$ is shown for nanowire growth, Fig 4.6(b).

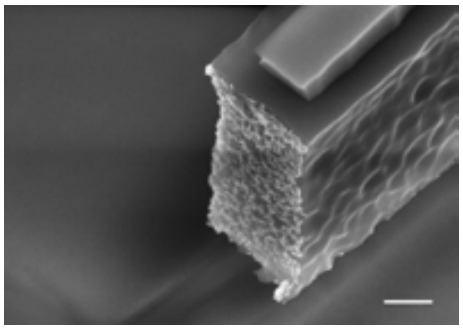


Figure 4.7: SEM image of nanowire growth areas after gold deposition. Scale bar 200 nm.

The gold deposition was realized by galvanic displacement, following the steps described in chapter 2. A thin film of few nanometers was deposited in predefined silicon areas, Fig 4.7. For double clamped beams, we had previously made an HF etch to remove the oxide of the opposite sidewall and ensure epitaxial clamps. For long wet etching after gold deposition we can have problems with possible gold migrations. A possible solution

is the oxide etching by HF vapors.

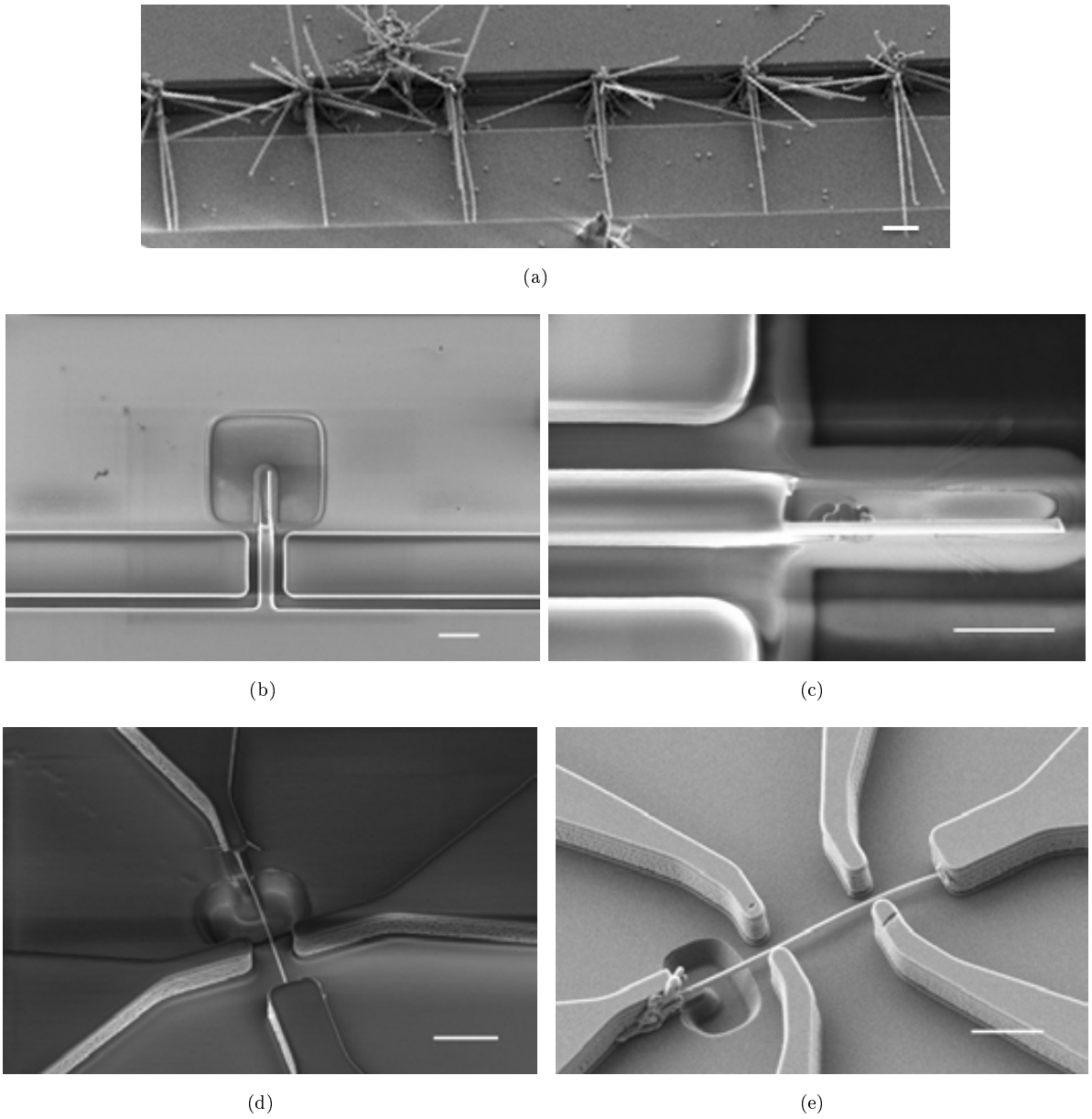


Figure 4.8: SEM image of single nanowire devices fabricated by technologies based on galvanic displacement. Scale bar $2\mu m$ in (a),(b) (d) and (e) and $1\mu m$ in (b)

After deposition we proceeded to the nanowire growth. In general, the gold deposition was very selective but growth results were not as good as we expected. Contamination and instability problems in the CVD system made it difficult the catalyst deposition and nanowire growth optimization. Best results are in the range of 20 per cent per chip but are difficult to repeat. However, we can expect better results in view of previous works with the use of annealed gold thin films with similar dimensions[19] and more efforts are needed to optimize the process.

4.4 Characterization results

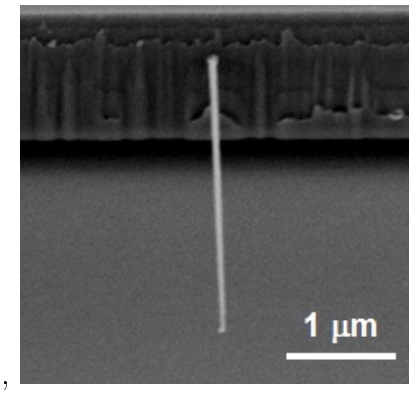
Mechanical resonances of obtained resonators can be measured by several techniques. However, due to the minuscule amplitudes in nanomechanical resonators, displacement transducers with extremely high sensitivities are needed. In this case, fabricated resonators will be characterized either optically or electrically by piezoresistive transduction or capacitive transduction of a coupled microresonator. Controlling nanowire resonator position provides important advantages to improve the output signal. For instance, electrical readout is only possible if the nanowire is placed properly between the reading electrodes. In addition, side-gate electrodes with a narrow gap for electrostatic actuation can improve the driving efficiency. Electrostatically driving can be addressed anyway via the back-gate substrate electrode, but multiple side-gate electrodes can provide further means to optimize more complex actuation schemes, such as parametric amplification, electromechanical switching or modal coupling. On the other hand, optical readout can benefit from the well-ordered disposition of the nanowire resonators into arrays with well-defined pitch, so that laser beam alignment on each nanowire is simplified or even automatized with commercially available readout systems. And finally, for capacitive transduction of a coupled resonator, the nanowire must be grown at the maximum displacement point to magnify effects on microresonator movement.

4.4.1 Nanomechanical resonators for optical readout

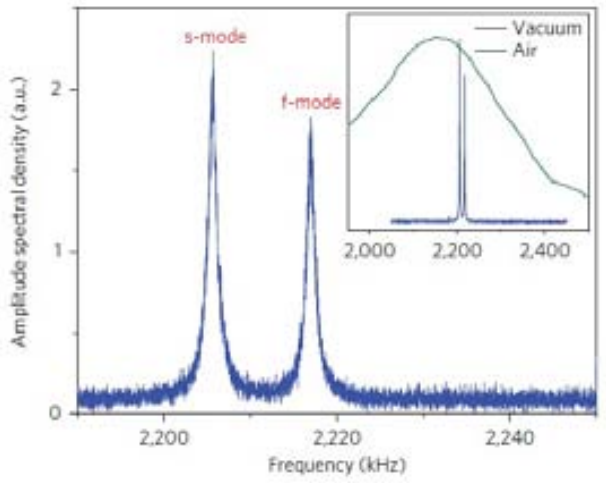
The optical characterization of stochastic Brownian displacement of horizontal Si nanowires were realized in collaboration with the Group of Bionanomechanics at the Instituto de Microelectronica de Madrid. Colloidal nanoparticles were used for catalyst grown Si nanowires at the sidewall of pre-fabricated trenches on SOI wafers with sidewalls oriented in the $\langle 111 \rangle$. Nanowire length and diameter were in the range of $5 - 10\mu m$ and $100 - 300nm$, respectively.

Thermal displacement fluctuations of horizontal Si nanowires at room temperature have been measured using a home-made optical interferometer[20]. The characterization of thermal displacement fluctuations of the nanowires exhibited two resonance peaks, Fig 4.9(b). For a perfectly regular hexagonal or circular cross section, these nanowires should vibrate in all planes of flexural vibration with the same frequency. However, structural defects or irregularities in their hexagonal section cause a rupture in the beam symmetry and the mode degeneration breakage as a consequence. Experimentally this causes the observation of the two peaks instead of a single peak. In air Q factor is too low, but in vacuum, two peaks can be perfectly observed. These peaks correspond to two modes termed z and y, each of them corresponding to vibrations with the largest projection along the vertical and horizontal planes respectively.

This effect has interesting applications for mass detection. First of all, it enables differential detection based on a single mode without the need of using much larger frequencies



(a)



(b)

Figure 4.9: a) SEM image of a typical nanowire used for this measured. c) A fast Fourier transform of the signal from the photodetector is dominated by the displacement thermal fluctuation of the nanowires. Only single resonant peak can be seen in air (green line in inset), but two resonant peaks can be clearly seen in vacuum (blue lines)[20].

of higher order mode, which are more difficult to detect. Second, it provides better stability, as the effect of thermal drift and other external effects is lower on the difference in frequencies between the two modes than on each of their absolute resonance frequencies.

Finally, it allows a way to determine the mass adsorption, which is a crucial advance toward atomic mass spectrometry based on nanomechanical resonators, because the sensitivity depends largely on the adsorption location. As it is predicted by theory of elasticity, it was observed in the experiments: adsorption on the free end produces the same effect on both modes, shifting their frequencies equally to lower frequencies. However, adsorption at the base makes no effect on the y mode but a large shift of the z mode resonance frequency to higher frequencies. Basically what we see is that mass adsorption makes different effect on the effective elasticity of each mode, and then this theory can be used in the opposite direction to determine the position of mass adsorption.

4.4.2 Nanomechanical resonators for electrical readout: capacitive sensing

The capacitive actuation of NEMS resonators can be driving using capacitive actuation, because electrostatic forces can be scaled by increasing signal power or DC bias voltage to generate enough electrostatic forces compensating the small resonator surface. However, capacitive sensing of NEMS resonator motion is much more difficult[2]. As device dimensions decrease, capacitive coupling between NEMS resonators and capacitive electrodes decrease. Parasitic capacitances become quite large in relation to the small capacitive currents from resonator. Then, capacitive detection method necessitates CMOS integration due to the need to minimize the parasitic capacitance contribution, which otherwise would screen the resonance signal[21].

The use of a hybrid system that combines a microresonator mechanically coupled to a nanoresonator is an interesting alternative. This structure takes advantages of the responsivity of the smaller component and of the detectability of the larger one. The use of coupling top-down micro and nanocantilevers has been demonstrated to produce an enhancement on the operating mass sensor performance in terms of mass responsiveness and detectability[22]. We have been working in collaboration with Department of Electronic Engineer at the Universitat Autonoma de Barcelona in the fabrication of coupling nanocantilever in which a single clamped bottom-up nanowire is coupled with a cantilever defined by optical lithography, Fig 4.8(b). We expect additional improvements in the mass responsivity given by the smaller dimension and the higher crystal quality given by the bottom up nanowire. However, additional experiments are needed to optimize the nanowire growth process and obtain more conclusions.

4.4.3 Nanomechanical resonators for electrical readout: piezoresistive sensing

Nanowire giant piezoresistance behavior observed by He and Yang[23] provides excellent strain transducers that are naturally integrated within nanowires themselves. This mechanism was used for the transduction of double clamped Si nanowires capacitive actuated[24]. Their resonance produces a nonvanishing longitudinal strain through the nanowire. This longitudinal strain is small magnitude for slightly deflected nanowires; however, the large gauge factors compensates this and readily provides a detectable change in resistance that is measured by means of a signal down-mixing technique. In the case of technology based on galvanic displacement, described in this chapter, the nanowire growth area is limited to a small surface making it possible to grow the nanowire close to the excitation gate which implies the need of a lower actuation voltage. On the other hand, in contrast to technology designed for the use of acidified colloids, Fig 4.3, in the process designed for galvanic displacement deposition, exposed Si surfaces are always perpendicular to the nanowire growth direction, $\langle 111 \rangle$, which avoids unwanted shortcuts between nanowire and driving electrode. This also facilitates the fabrication of multiple side-gate

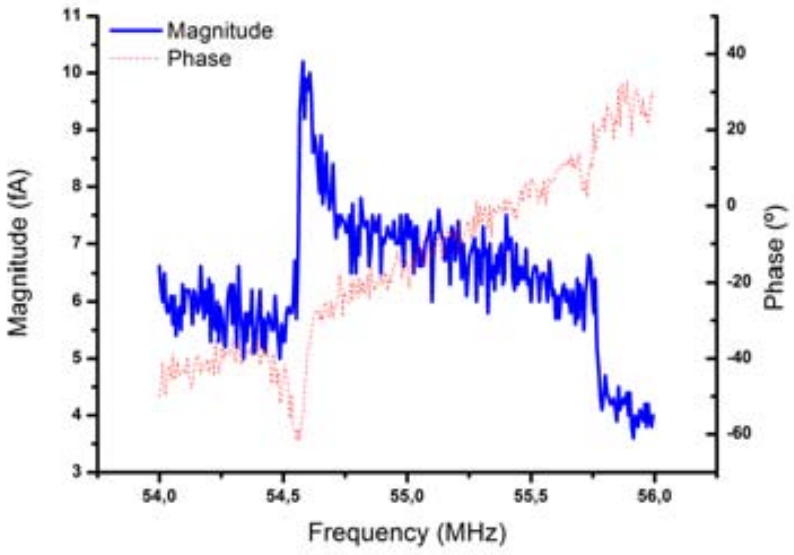


Figure 4.10: Characterization results of the mechanical resonances of doubly clamped nanowire resonators via by electrical signal downmixing ($V_{bias} = V_0 \cos(2\omega t)$; $V_{drive} = V_{DC} + V_{AC} \cos(\omega t)$; $V_{DC} = 0.3V$; $V_{AC} = 1.4V$); see ref.[24] for setup details.

electrodes enabling more complex actuation schemes, such as parametric amplification[?], electromechanical switching[?] or modal coupling[?].

Another advantage of the fabrication method based on galvanic displacement is that it provides the means to extend the observation and application of the resonant mode splitting effect to electrical read-out methods, provided the proximity of the side-gate driving electrodes to the nanowire. This has the advantage of allowing the detection of much higher resonance frequency modes, which improves the device sensitivity and resolution limits given the typically higher frequency bandwidth of electrical detection methods. Fig 4.10 shows the mechanical resonance peaks corresponding to a doubly clamped nanowire detected by signal downmixing around the first-order flexural mode. The measurement was made by following the method described by He and coauthors[24]. The nanowire length and diameter are $3\mu m$ and 80 nm, respectively. Note the much higher resonance frequencies detected in this case (54.5 and 55.7 MHz). Remarkably, this demonstrates that resonant mode splitting in Si nanowire resonators is also observable in the case of electrostatically driven vibrations. The observation of the two peaks indicates that in this particular case both orthogonal vibrations have a component along the direction parallel to the driving force.

4.5 Conclusions

Single bottom-up Si nanowires are a promising candidate for the fabrication of nanomechanical devices. Specifically, their use in mass sensing applications has been demon-

strated to improve the sensitivity with respect to devices based on top-down nanostructures.

In this chapter, we have developed and adapted different technological processes for the fabrication of devices based on single Si nanowires with different transduction mechanism. Single nanowires for optical readout do not require of a precise control of nanowire position. For this reason, colloidal nanoparticles have been used to catalyze the horizontal growth of nanowires on prefabricated microtrenches. The thermal spectrum characterization showed a mode degeneration which has important implications for mass sensing applications. For future experiments, galvanic displacement deposition will allow the synthesis of well ordered arrays simplifying the laser alignment process or automatizing the measurement mechanism.

In the case of capacitive actuation, with capacitive or piezoresistive readout, the position of nanowires could be critical for device performance. For this reason, we have studied different technologies in order to have a more precise control over catalyst deposition. We first used acidified colloidal nanoparticles for device fabrication. Catalyst nanoparticles are selectively deposited in Si device areas previously defined by removing oxide with a lithography step and a wet etching. However, this technique is only valid for prototype fabrication. Deposition areas are so large, due to the fabrication technology used, and nanoparticles are deposited randomly, which makes it difficult the deposition of a single catalyst nanoparticle per device.

On the other hand, galvanic displacement techniques offer a more precise control of the metal deposition. A thin gold film is deposited selectively on Si surfaces but not on oxidized ones. Additionally, the technology process designed allows defining smaller deposition areas, which gives us more control over the catalyst position, very important for the proposed application.

Resonance of nanowire devices has been characterized by two mechanisms. Single clamped nanowires have been characterized optically, while double clamped nanowires electrically. In both situations, it can be observed the resonant mode splitting effect caused by a rupture in the beam symmetry which has interesting applications for mass sensor detection.

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