Avalanche Ruggedness of Local Charge Balance Power Super Junction Transistors

Thesis dissertation presented to obtain the qualification of
Doctor of Philosophy from the Electronic Engineering
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Dr. David Flores Gual, Dr. Peter Moens and Dr. Jaume Roig Guitart certify that this thesis dissertation entitled *"Avalanche Ruggedness of Local Charge balance power Super Junction transistors"* is presented by Ana Villamor Baliarda to obtain the PhD in Electronic Engineering in Universitat Autònoma de Barcelona. They certify that it is ready to be presented for lecture and defense.

Cerdanyola del Vallès, May 2013

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Abstract

The main objective of the thesis is the reliability increase of high voltage (600 V) power MOSFETS based in the Super Junction concept when they are submitted to the most extreme conditions in DC/DC converters and Factor Power Correction circuits and the intrinsic body diode has to handle a big amount of energy in a very short period of time. The research has been carried out in the framework of a collaboration between Institut de Microelectrònica de Barcelona (IMB-CNM-CSIC) and ON Semiconductor (Oudenaarde, Bèlgica).

The process technology of the new Super Junction power MOSFET transistors designed in ON Semiconductor (named UltiMOS) has been optimized with the aim of robustness enhancement, which has to be totally independent of the charge balance in the device. The transistors are destined to 400 V line applications that require a voltage capability above 600 V and a minimal on-state resistance to operate at high frequency. The thesis starts with an introduction to the state of the art of Super Junction transistors, including a description of the different process technologies used in the commercial counterparts. Afterwards, the most relevant electrical and technological parameters are introduced and linked to the electrical characterization of the UltiMOS transistor.

The research is centered in the study of the physics involved in the failure mechanisms combining TCAD simulations and experimental measurements, from where it is concluded that a technological solution to increase the energy capability of UltiMOS transistors is needed, with a wide CB manufacturability window. Different devices derived from the UltiMOS structure (conventional UMOS transistor, SJ Diodes and SJ Bipolar transistors) were fabricated in the ON Semiconductor's Clean Room and tested under the same avalanche conditions as UltiMOS transistors. All the results derived from complementary techniques (*Unclamped Inductive Switching*, *Emission Microscopy*, *Thermal Infrared Thermography*, *Transmission Line Pulse*, *Transient Interferometric Mapping*, etc.) lead to the same conclusion: the current is focalized at a certain region of the UltiMOS transistor, enhancing the activation of the parasitic bipolar transistor. Two approaches are proposed to increase the energy capability of UltiMOS transistors and, once its efficiency has been demonstrated, they have been included on the process technology of the device designed to go into production.

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Table of Contents

List of Symbols and Acronyms

Symbols

μ_n	Permeability of the silicon
A	Area
AAV_{bd}	Active area breakdown voltage
A_N	$P_{connection}$ implant angle
C	Capacitance
C_{ds}	Drain-Source capacitance
C_{gd}	Drain-Gate capacitance
C_{gs}	Gate-Source capacitance
C_{iss}	Input capacitance
C_{oss}	Output capacitance
C_{rr}	Reverse transfer capacitance
d	Depletion width
D_N	$P_{connection}$ implant dose
E_{AR}	Energy under repetitive avalanche UIS test
E_{AS}	Energy under single avalanche UIS test
E_C	Critical electric field
E_F	Electric field
E_N	$P_{connection}$ implant energy
E_{off}	Energy dissipated at turn-off
E_{on}	Energy dissipated at turn-on
$\mathcal{E}s$	Permittivity of the silicon
f	Frequency
h_{fe}	Gain
I_{AS}	Failure current under single avalanche UIS test
I_{body} *or* I_b	Body current
I_c	Collector current
I_d	Drain current
I_g	Gate current
I_{RRM}	Reverse recovery maximum current
I_{snap}	Snapback current
I_{source}	Source current
L	Inductance value
l	Depletion extension
n-BAL or NB	N_{buff} layer dose
N_{conc}	Doping concentration of the N-type pillar
N_D	Donor concentration
n_i	Intrinsic carrier density

Opt ±#	Different CB condition notation
p	Cell pitch
P_{conc}	Doping concentration of the P-type pillar
Q_g	Gate charge
Q_{gd}	Gate-Drain charge
Q_{gs}	Gate -source charge
Q_{rr}	Reverse recovery charge
R_g	Gate resistance
R_{on}	On-resistance
sR_{on}	Specific on-resistance
t1	Fall time during reverse recovery test
t2	Rise time during reverse recovery test
T-BAL or NT	N_{buff} layer thickness
T_{in}	Intrinsic temperature
T_{max}	Maximum temperature in the device
T_{rr}	Reverse recovery time
TV_{bd}	Termination breakdown voltage
V_{bd}	Voltage capability /breakdown voltage
V_{bi}	Built-in potential
V_{ce}	Emitter collector voltage
V_{dd}	Drain voltage
V_{ds}	Drain-source voltage
V_{gs}	Gate voltage
V_{in}	Input voltage
V_{out}	Output voltage
V_{pinch}	Pinch-off voltage
V_{TH}	Threshold voltage
W	Perimeter
W_b	Spacing between rings
W_N	Width of N-type column
W_P	Width of P-type column
W_r	Width of the rings

Acronyms

BJT	Bipolar transistor
BPSG	Borophosphosilicate
CB	Charge Balance
CIBH	Controlled injection of backside holes
CMP	Chemical Mechanical Polishing
DIBET	Department of Biomedical, Electronics, and Telecommunications Engineering from University of Naples Federico II

DRIE	Deep Reactive Ion Etching
DUT	Device under test
EMMI	Emission microscopy
ESD	Electrostatic discharge
FA	Failure analysis
FCS	Fairchild
FOM	Figure of Merit
FOX	Field Oxide
GaN	Gallium Nitride
GR	Ground ring
IPA or IFX	Infineon
IT	Information Technology
JFET	Junction field effect transistor
KUL	University of Leuven
ME/MI	Multi-epitaxy/Multi-implant
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NDR	Negative differential resistance
N_{rich}	Negative Charge Balance condition
PDR	Positive differential resistance
PFC	Power Factor Correlation
P_{rich}	Positive Charge Balance condition
SCM	Scanning Capacitance Microscopy
SEM	Scanning Electron Microscope
SH	Self-heating
Si	Silicon
SiC	Silicon Carbide
SIMS	Scanning ion mass spectometer
SJ	Super Junction
ST or STF	ST semiconductor
STUBA	Slovenská Technická Univerzita V Bratislave
TCAD	Technology Computer Aided Design
TEOS	Tetraethylorthosilicate
TIM	Transient Interferometric measurement
TLP	Transmission line pulse
TUV	Vienna University of Technology
UIS	Unclamped Inductive Switching
VDMOS	Vertical Diffused Metal Oxide Semiconductor

CHAPTER I

I.1. Motivation

New application fields such as power electronics in aircrafts[1] are very restrictive in terms of efficiency, compactness, weight and losses. Indeed, active pulse width modulation (PWM) rectifiers (see Fig.1.1) with minimized total harmonic distortion of the input current and high power factor have to be designed for future electric power control. Advanced architectures for three-phase/level rectifiers have a reduced power semiconductor stress, allowing the use of high-efficiency power MOSFETs with a voltage capability in the 600 V range.

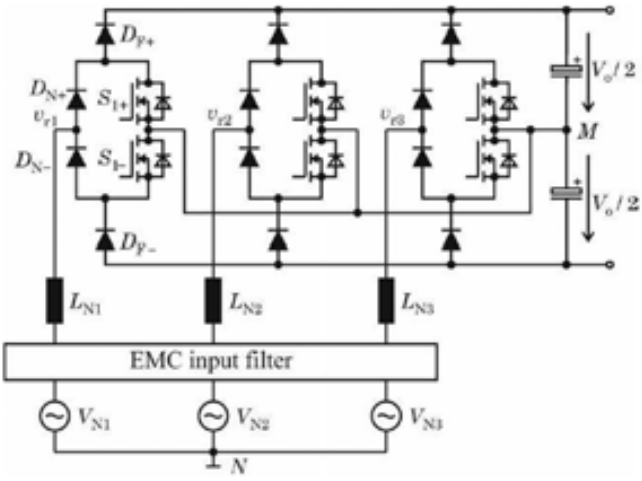

Fig.1.1. Typical application for 600 V power MOSFETs: active three-phase/level PWM rectifier. Adapted from [1].

Today, the 600 V power MOSFET market is dominated by switching power mode supplies (SMPS) and LCD-TV applications, although power factor correction[2] (PFC, see Fig.1.2) and lighting applications also require high-efficiency power semiconductor switches[3]. The market distribution for 600 V power MOSFETs is shown in Fig.1.2-(a).

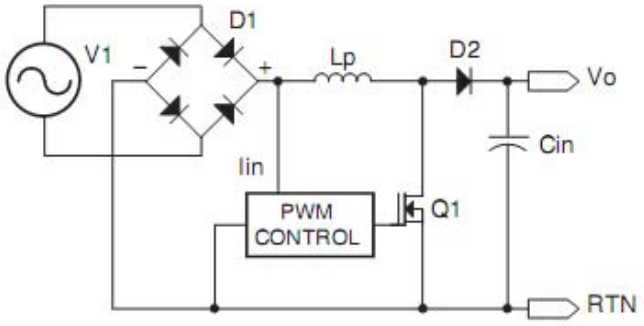

Fig.1.2. Typical application for 600 V power MOSFETs: PFC Boost pre-regulator. Adapted from[2].

A high performing – high voltage power MOSFET requires very low conduction and transient losses. Conduction losses are basically driven by the specific on-state resistance (sR_{on}) value but transient losses are determined by several electrical parameters which mainly depend on the transistor architecture and the process technology. Moreover, transient losses are dominant in high frequency applications where the parasitic capacitances of the power MOSFET have to be minimised. In some particular applications, the performance of the body diode of the power MOSFET transistor is crucial.

In the late 1990s, a new device concept was introduced to decrease the sR_{on} value of power MOSFETs without degrading the voltage capability: the Super Junction (SJ) architecture with charge balance in the drift region. The drastic sR_{on} reduction to the 10-30 mΩ·cm^2 range when the SJ concept is implemented favoured the development of different techniques for the fabrication of 600 V power MOSFETs (multi epitaxial growth and deep trench etch). Today, different manufacturers as Infineon, Fairchild, STMicroelectronics, Toshiba and Vishay are already power SJ MOSFET suppliers, with a great success in the market (see Fig.1.2-(b)). Although the performance of the first generations of power SJ MOSFETs are much superior than those of the conventional VDMOS counterparts, there is still a long way to go in the optimisation of their performance and robustness.

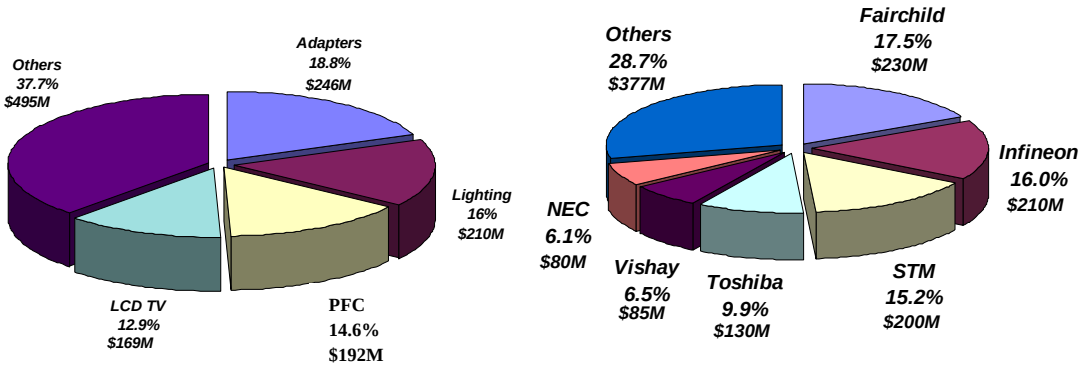

Fig.1.2. Market distribution from the point of view of (a) application or (b) manufacturer for high-efficiency 600 V power SJ MOSFETs.

New base materials are emerging to fabricate power electronic devices, such as Gallium Nitride (GaN) or Silicon Carbide (SiC). Although SiC JFETs, SiC Schottky Diodes and GaN HEMTs have been proven to be far superior than Si SJ power MOSFETs in several electrical parameters, it is still not clear what chances are offered by SiC and GaN technologies to address the global needs of power switches better and/or cheaper. Last generation of SJ MOSFETs have reached an sR_{on} value in the range of 10 mΩ·cm^2 but the sR_{on} values of SiC and GaN prototypes are one order of magnitude lower and will be further reduced in the next decade. Calculations made on SJ MOSFETs with a cell pitch of 2 µm predict a minimum sR_{on} of 1 mΩ·cm^2 by introducing doping variation along the SJ columns.

The energy stored in the output capacitance (E_{oss}) is crucial to determine the losses in hard switching applications. Power SJ MOSFETs exhibits E_{oss} values even lower than those of the SiC JFETs but GaN switches will sure be far better. Charge stored in the output capacitance (Q_{oss}) limits the maximum frequency, specially in resonant applications. Q_{oss} can hardly be improved in SJ MOSFETs but it will be reduced by a factor of 5 in SiC and GaN.

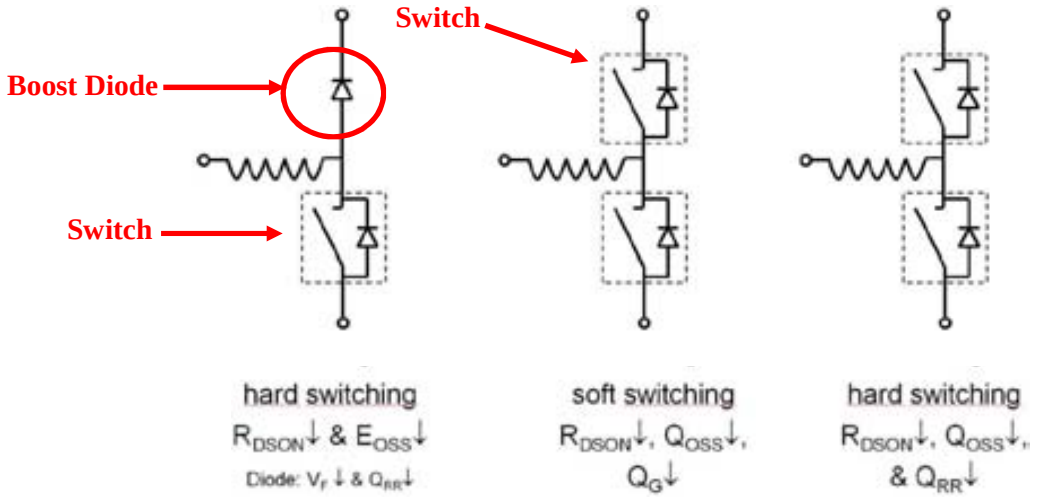

Fig.1.3. Typical switching applications and basic requirements for the switch and the boost diode. Adapted from [4].

Three topologies are usually implemented in switching applications using a power MOSFET and a boost power diode, each one with specific requirements on the conduction and transient performance, as shown in Fig.1.3[4]. SJ MOSFETs with very low E_{oss} values are suitable for the hard switching topology with the boost diode implemented with a SiC Schottky. The topologies where two switches are used will sure be implemented with SiC and GaN switches in the future since SJ MOSFETs cannot compete in terms of very low Q_{oss}.

Although SiC and GaN are very promising technologies due to their good performance, they still have a long way to be able to fill the whole semiconductor market since they are competing with the Silicon, which is a mature and very good established base material. Nevertheless, serious improvements have to be done in power

SJ MOSFETs in terms of high frequency operation, where the risk of ringing oscillations in the gate electrode is not accepted, and robustness performance. The enhancement of the power SJ MOSFETs robustness performance is mandatory in applications where voltage spikes coming from the mains can occur due to the instability of the infrastructures. Indeed, hard switching conditions, such as Unclamped Inductive Switching (UIS) can also easily destroy the power semiconductor device when the energy stored in an inductor is directly dumped to the body diode. Today, power SJ MOSFETs are much more robust than SiC and GaN switches but the continuous reduction of the sR_{on} value leads to smaller chip size with the subsequent increased risk of thermal destruction due to current crowding in avalanche conditions.

Voltage spikes can go to 1/3 over the operating voltage. Due to the complex architecture of power SJ MOSFETs from the manufacturing point of view, small technological variations during the wafer processing can eventually lead to failures when the switch operates in hard switching conditions. In this sense, the research reported in this document is focussed on the robustness enhancement of the ON Semiconductor 600 V power SJ MOSFET based on the deep trench technology, known as UltiMOS.

1.2. Framework and Thesis Outline

The robustness enhancement of the UltiMOS transistor, which is the final goal of this PhD, has been done in the framework of the collaboration between Instituto de Microelectrónica de Barcelona (IMB-CNM-CSIC) and ON Semiconductor (Oudenaarde, Belgium). The set-up of the UltiMOS process technology started with the initial test masks used to define the correct technological parameters for the different fabrication steps as etch of layers, epitaxial growths, implantations, diffusion times, etc. The sR_{on} value had to be low and independent of technological variations, and this is achieved by an accurate control of the process technology.

Afterwards, the layout was optimized to enhance the most relevant electrical parameters, but this first optimization steps are not subject of study on this document. The edge termination layout was also optimized before starting the PhD research when the device was process stable but not yet reliable due to the low current capability performance. The most relevant electrical parameters under study are the voltage and energy capabilities since the R_{on} and V_{TH} targets were already accomplished. Therefore, mainly the off-state performance is analysed. Nevertheless, the optimisation of V_{bd} and E_{AS} has also impacted the conduction performance with the necessary re-optimisation work.

The thesis document is structured in 6 chapters and 2 appendices:

- Chapter 1 describes the motivation, framework and outline of the performed research.
- The basic SJ MOSFET theory is reported in Chapter 2 where the development of the different SJ architectures and their main requirements are described. A final comparison of the electrical performance of the commercially available power SJ MOSFETs is provided.
- Solid state concepts and tools needed to follow the investigation presented in this thesis are explained in Chapter 3. The chapter is split into Active area and Edge Termination regions to better study their electrical performance and to determine the impact of the technological parameters on each region. Two ways to determine the CB on the UltiMOS transistor are also presented, although it could be used on other SJ MOSFET architectures.

- The improvement of the edge termination robustness is studied in Chapter 4. It concludes with the analysis of the active area electrical performance when the edge termination is already optimized.

- The ruggedness of the active area is reported in Chapter 5. Different power structures derived from the UltiMOS transistor are simulated and fabricated to understand the failure mechanisms with the aid of the experimental techniques described in Appendix B (EMMI, Thermal Mapping, TIM, TLP, etc.).

- Different approaches implemented in commercial SJ MOSFET devices to improve its robustness of are reported in Chapter 6. Afterwards, two approaches to improve the robustness of UltiMOS transistors under the UIS test are presented. The energy capability improvement is accomplished in both proposed cases.

- The conclusions of this thesis are finally drawn in Chapter 7 together with the recommendations for future work.

- The UltiMOS process technology is detailed in Appendix A.

- Experimental techniques used in the performed research are reported in Appendix B, including the test set-up. ON Semiconductor cannot perform all the necessary tests at the Oudenaarde site. Therefore, a brief description on where each type of measurement was performed is provided.

1.3. References

[1] M. Hartmann, H. Ertl, J. W. Kolar, "*On the trade-off between Input Current Quality and Efficiency of High Switching Frequency PWM Rectifiers*", ITPE vol. 27, No. 7, pp. 3137-3149 (2012).

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[4] M. Treu, E. Vecino, M Pippan, O. Häberlen, G. Curatola, G. Deboy, M. Kutschak, U. Kirchner, *"The role of silicon, silicon carbide and gallium nitride in power electronics"*, Proc. IEDM ´12, pp. 147-150 (2012).

CHAPTER 2

Introduction

In this chapter the fundamentals of Power MOSFET are introduced. One of the most important parameters to optimize for the design of these devices is the V_{bd}-R_{on} trade-off. The principal applications of these devices are discussed in this section. A new concept is introduced: the Super Junction. The relation V_{bd}-R_{on} can be highly improved, breaking the so-called Silicon Limit.

2.1. Fundamentals of Power MOSFETs

The power MOSFET (*metal-oxide-semiconductor field-effect transistor*) was developed in the 1970s to overcome the intrinsic limitations of power bipolar transistors (BJT), inherent to the current control process. Thus the necessary base current to maintain the BJT in the on-state leads to an inefficient energy operation at high frequency. In fact, the bipolar nature of power BJTs limits their switching speed. Power MOSFETs are majority carrier devices with positive temperature coefficient and high switching speed, even at high temperatures in contrast with the power BJT, where electrons and holes need to be removed during the turn-off process[1]. In addition, power MOSFETs have a more linear characteristics and better temperature stability with enhanced performance in linear applications and less complex feedback circuitry. Finally, the leakage current of power MOSFETs is extremely low (nA) and no conduction threshold is present, eliminating electrical noise in sensitive AC switching applications. These devices found applications in power electronic circuits operating at low voltages (<150 V).

The vertical power MOSFET, known as VDMOS (*Vertical Double Diffused MOS*) transistor, is implemented as n-channel device due to the higher electron mobility. The charge modulation in the N-type inversion layer created at the Silicon surface is achieved with a metal plate (gate electrode, *G*) located above the P-type body region (P_{body} in the VDMOS cross section plotted in **Fig.2.1-(a)**) and insulated by the gate oxide from the active Silicon area and by an interlevel oxide from the source electrode. The

source (*S*) and drain (*D*) electrodes of the power VDMOS transistor are connected to high doped N-type regions to obtain a good ohmic contact while a low doped N-type epitaxial region (N^-_{epi}), grown on the N^+ substrate (N^+_{sub}), is necessary to reach the desired blocking voltage capability (V_{bd}). The P_{body} region is also contacted to the source electrode in the third dimension to avoid the eventual activation of the inherent parasitic NPN bipolar structure[2]. When a gate voltage higher than the threshold voltage (V_{TH}) is applied, an inversion channel is created at the top of the P_{body} region and electrons can flow from source to drain, provided a positive drain bias is applied. The power MOSFET structure includes a body diode with the cathode connected to the drain contact and the anode to the source contact. This diode can be used as a freewheeling diode or can be driven in avalanche during operation.

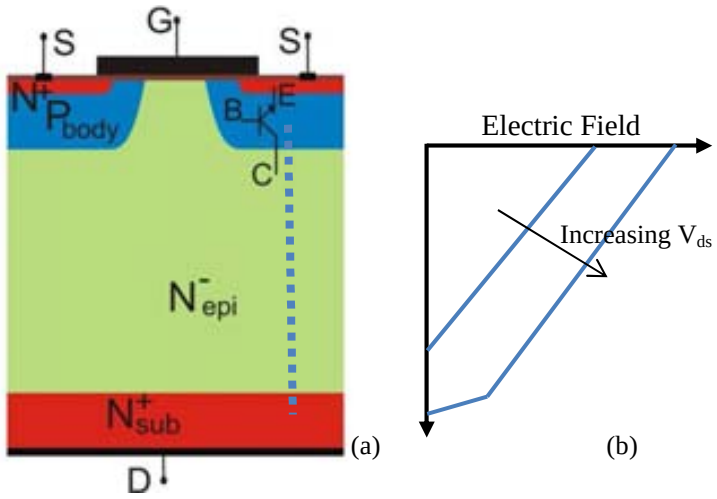


Fig.2.1. (a) Cross section of a conventional power VDMOS structure and (b) schematic electric field cut in the same structure as increasing the positive drain bias.

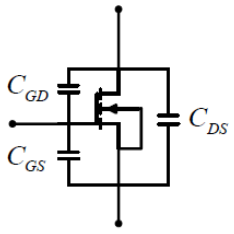
The doping and thickness of the N^-_{epi} layer are determined by the V_{bd} value since in the off-state (*G* grounded) the depleted region is mainly spread into this layer. As a consequence, the N^-_{epi} layer properties are responsible for the vertical electric field profile and avalanche process. A high V_{bd} value can only be achieved if the doping concentration and the thickness of the N^-_{epi} layer are increased, sustaining more drain voltage before reaching the critical electric field (E_C) at the P_{body}/N^-_{epi} junction[1]. If the depleted region reaches the N^+_{sub} a reach-through breakdown will happen with a trapezoidal electric field shape.

The main concern when a device is chosen for a certain application is the losses that will be introduced in the circuit by the device: the conduction losses (ruled by the on-resistance, (R_{on})) and the switching losses (mainly depending on the capacitive behaviour of the device). The R_{on} value is the added contribution of the channel resistance, the resistance of the accumulated layer under the gate electrode, the JFET resistance between adjacent cells and the epitaxial resistance[3]. The substrate and the package resistances contribution to the total R_{on} is very low and are not taken into account. The resistance of the N^-_{epi} layer is the most important contribution in the case of high voltage transistors (approximately 95% in 600 V Power MOSFETs) due to the

necessary thick and low doped N^-_{epi} layer to reach high V_{bd} values. The relation between two relevant parameters is usually described by a figure of merit (FOM)[4]. The most important FOM that has to be improved in a power VDMOS transistor is the reduction of the specific on-state resistance (sR_{on}) defined as the product of the R_{on} and the active area of the device (A). Another important FOM for the design of a power VDMOS transistor is the sR_{on}-V_{bd} trade-off described by Eq.1 (ideal R_{on}) where ε_s and μ_n are the permittivity the permeability of the silicon, respectively, and Ec is the critical electric field[4] .The R_{on} value increases with the V_{bd} value since a thicker and less doped N^-_{epi} layer is needed. The sR_{on}-V_{bd} trade-off has to be optimised with the aid of 2D TCAD simulations in real power VDMOS transistors, taking into account the process technology.

$$\boldsymbol{R_{on-ideal} = \frac{4V_{bd}^2}{\varepsilon_s \mu_n E_C^3}} \qquad \textbf{(Eq.1)}$$

The switching losses on a Power MOSFET depend on the inherent capacitances since they work as energy storage centres. The C_{gd}, C_{gs} and C_{ds}, are the gate-to-drain, gate-to-source and drain-to-source capacitances, respectively (see Fig.2.2). However, in the commercial datasheets the capacitances are labelled as input (C_{iss}), reverse transfer (C_{rss}) and output (C_{oss}) capacitances, according to Eq.2, Eq.3 and Eq.4, respectively. C_{oss} for a 600 V VDMOS can be approximated to C_{ds} since the C_{gd} value can be neglected when compared to C_{ds}. C_{gd} can be divided in two parts: the capacitance related with the overlap between the polysilicon gate and the silicon drift region under the gate, and the capacitance associated to the depletion region under the gate coming from the P_{body}/N_{drift} junction. C_{gs} is the capacitance derived from the overlap between the gate electrode and the source and channel regions. This capacitance mainly depends on the geometry of the device. Finally, C_{ds} is the capacitance associated with the P_{body}/N^-_{epi} diode[1]. Typical values of the intrinsic capacitances of a 600 V-20 A VDMOS transistor with R_{on}=0.55 Ω are provided in Fig.2.3. C_{oss} gradually decreases with the applied drain voltage[1,5]and the C_{rss} curve exhibits a similar behaviour than C_{oss}, but at lower capacitance values. It is worth to say that a minimised C_{rss} value leads to a faster depletion and a higher switching speed. Finally, C_{iss} is almost constant with the drain voltage.



$$C_{rss} = C_{gd} \qquad \textbf{(Eq.2)}$$

$$C_{oss} = C_{ds} + C_{gd} \qquad \textbf{(Eq.3)}$$

$$C_{iss} = C_{ds} + C_{gs} \qquad \textbf{(Eq.4)}$$

Fig.2.2. MOSFET capacitance equivalent circuit

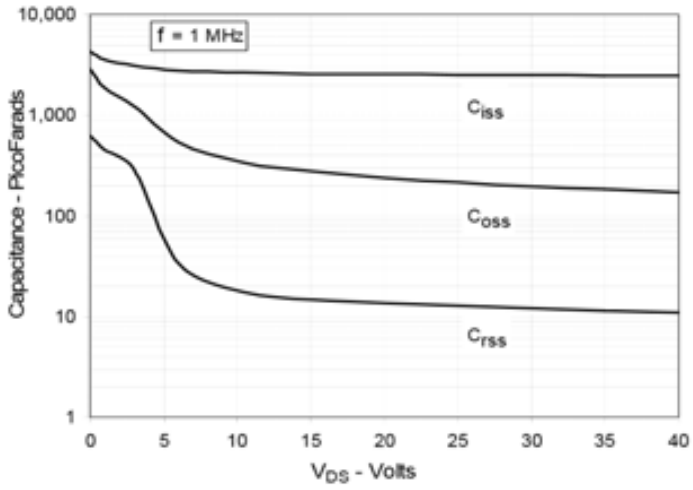


Fig.2.3. Typical capacitive behaviour of a power VDMOS transistor (IXFH14N60P, from Infineon).

The Q_g accounts for the gate charge that needs to be removed during the turn-on process of a power MOSFET, and it depends on the total gate width. Q_g determines the gate peak current (I_g) and the drive loss[6]. As expected, the lower the Q_g value, the faster the charges are removed, leading to a lower switching time. Therefore, an optimised R_{on}-Q_g trade-off is crucial for the conduction and switching losses. The gate architecture is also a key point for the optimisation of the power MOSFET performance. The original planar gate was substituted by advanced trench gate designs in the 1990's, in almost all the commercial power VDMOS transistors due to the strong increase of the integration density and the current capability[7]. The sR_{on} can be reduced when a Trench MOS (UMOS) is used because the channel density is larger if a smaller cell pitch is used[4]. However, the large trench wall area leads to an increase of the Q_g value, typically twice of the corresponding planar gate value with the subsequent reduction of the operating frequency[4]. Cross sections of power VDMOS and UMOS transistors are plotted in Fig.2.4, respectively.

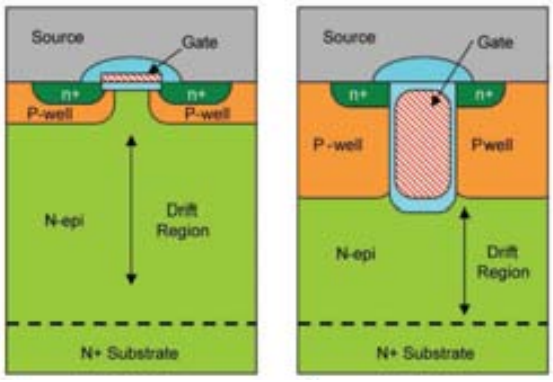


Fig.2.4. Cross sections of power transistors. (a) VDMOS with planar gate and (b) UMOS with trench gate.

The real V_{bd} value of a power VDMOS is lower than that of its basic cell due to the high electric field peaks at edge of the active area where the curvature of the P_{body}/N^-_{epi} junction is not self-protected, leading to the crowding of the potential lines.

Therefore, the implementation of a robust and area-efficient edge termination is crucial to achieve reliable operation in the field[1]. The edge termination is basically used to smooth the electric field from the end of the active area to the edge of the device, avoiding a premature breakdown in the curvature of the P_{body} diffusion. There are two ways to implement an efficient edge termination for power VDMOS and UMOS transistors: floating guard rings or metal field plates, depending on the desired voltage capability. The metal field plate is typically used in low voltage power MOSFETs (V_{bd}<50 V) while the floating guard rings are used for medium and high voltage power MOSFETs. A Field Oxide (FOX) growth is required in both cases to protect the Silicon surface from high electric field peaks at the metal corners. The floating guard rings are implemented by implanting several P-type rings, whereas the metal field plate consists on the enlargement of the source metal over the FOX[4]. An edge termination combining floating guard rings and a metal field plate is also feasible.

The main FOMs for a 30V VDMOS and UMOS transistors are presented on Table 2.1 (see definitions in Eq. 5-7) [7]. Notice that in all cases, the performance of UMOS transistors is better than that of the VDMOS counterparts, since the R_{on} decrease is more relevant than the Q_g increase. Therefore, nowadays the power MOSFET market is dominated by the UMOS architectures even if its switching performance is slightly degraded.

FOM	VDMOS (30V)		UMOS (30V)	
	V_{gs}= 4.5 V	V_{gs}=10 V	V_{gs}= 4.5 V	V_{gs}=10 V
A	64000	32000	7085	3720
B	30,9	15,5	15,6	8,2
C	303	152	120	63

Table 2.1. Basic FOMs for a 30 V VDMOS and UMOS transistors.

$$FOM\ (A) = \frac{R_{on}}{C_{in}} \qquad \text{(Eq.5)}$$

$$FOM\ (B) = R_{on} * C_{iss} \qquad \text{(Eq.6)}$$

$$FOM\ (C) = R_{on} * Q_{gd} \qquad \text{(Eq.7)}$$

Power UMOS transistors are basically addressed to low voltage DC/DC converters[2] for telecommunication applications and switched mode power supplies (basically for the Power Factor Correction circuits[8]). Applications for medium voltage range (150 to 600 V), basically in the automotive industry, were implemented with power BJTs. However, the limited switching frequency of BJTs due to their bipolar nature and the need to increase the switching frequency of the systems, lead to the gradual replacement of the BJTs by power MOSFETs. As an example, a basic Boost Converter (step-up converter) is shown in Fig.2.5-(a), with a power MOSFET as a switch. A voltage pulse is applied to the gate of the MOSFET to control the duty cycle and output voltage. When a positive bias is applied to the gate, the MOSFET turns-on and

the power diode turns-off. On the opposite, when the gate is ramped down to ground the MOSFET turns-off and the power diode starts conducting. The inductor is charged when the MOSFET is in the on-state, as shown in the *I-V* curves plotted in Fig.2.5-(b), while the output voltage comes from the capacitance. Once the MOSFET is turned-off the output voltage comes from the inductor, whereas the capacitor is charged. The switching frequency has to be high enough to be sure that the inductor is not completely discharged at the end of each period with the subsequent output voltage fluctuations. Typical V_{in} and V_{out} values in automotive applications are 90 and 400 V, respectively, what means that the MOSFET has to sustain at least 400 V in the off-state. Therefore, when the power MOSFET is turned-off, its intrinsic diode has to handle 400 V. Unexpected transients can appear in real converter application, as device snappy switching behaviour, voltage spikes, static discharge, and oscillations[9], which will make V_x be greater than 400 V (even 1/3 higher). These transients are voltage or current changes in a short period of time (100 ns range)[10]. Although these transients do not occur in every switching cycle during normal circuit operation, as a protection, the MOSFET has to properly operate in the off-state (when it behaves as a diode).

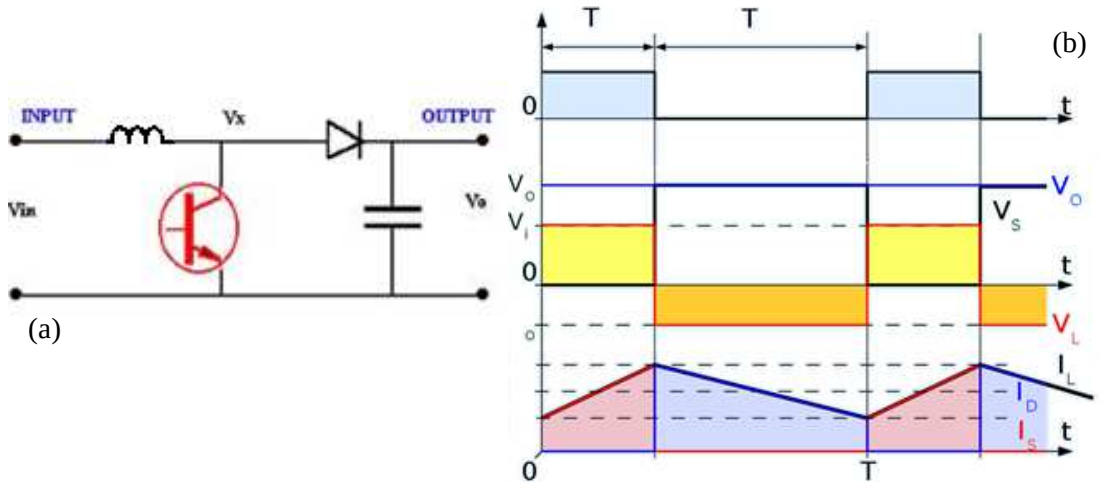


Fig.2.5. (a) Basic schematic circuit of a Boost converter. (b) *I-V* curves for the Boost converter.

2.2. Enhancing the vertical Power MOSFET: SJ Concept

As already stated, the most important contribution to the sR_{on} value in a power 600 V VDMOS transistor comes from the N^-_{epi} layer and the series resistance of this layer increases with the V_{bd} due to the necessary reduction of the doping concentration. In this sense, the only possible way to integrate power MOSFETs combining a high voltage capability (> 600 V) and a competitive on-state resistance is using a new device concept to break the so-called "Silicon Limit" of conventional architectures, which is proportional to $R_{on}\alpha V_{bd}^{2.5}$ [11]. Focused on the improvement of the sR_{on}-V_{bd} trade-off, the Super Junction (SJ) concept was introduced in the late 1990s[12,13]. The key point is to replace the N^-_{epi} layer by alternating thin columns of opposite doping, as shown on the

schematic cross-section drawn in Fig.2.6-(a). When the drain bias is applied, a depletion layer is simultaneously created under the gate electrode (P_{body}/N^-_{epi} junction) and in the vertical junction formed by the P/N columns in the drift region, in such a way that a 2D charge coupling that improves the electric field distribution is feasible[4]. As a consequence, the N^-_{epi} doping level can be increased and the final R_{on} value is significantly lower than that of the conventional power VDMOS counterpart, breaking the "Silicon Limit" as shown on the sR_{on}-V_{bd} FOM reported on Fig.2.6-(b). This graph is based on the drift region of a SJ power MOSFET as the one drawn in Fig.2.6-(a) with identical N and P pillars width.

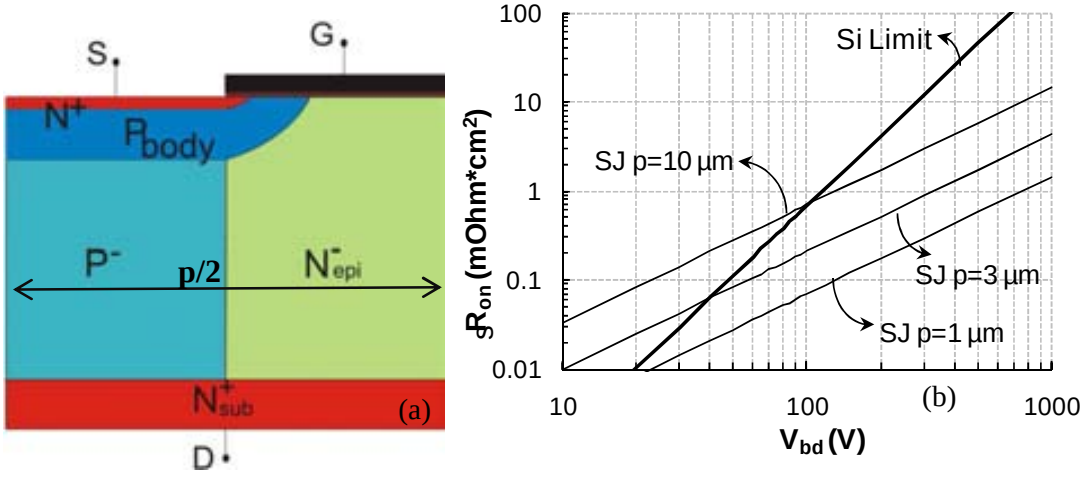


Fig.2.6. (a) Cross section of a basic SJ structure (half-cell). (b) V_{bd}-sR_{on} FOM for SJ power MOSFETs for different cell pitch (p).

The electric field in the Silicon volume of SJ devices is determined by the net charge in both columns (P and N). The ratio between the charges in each column is defined as the Charge Balance (CB) and it is normally given as a percentage (see Eq.8, being N_{conc} the Phosphorous concentration in the N column and P_{conc} the Boron concentration in the P column). When the net charge is perfectly compensated between the columns (Optimum CB condition) a rectangular vertical electric field distribution is achieved in the P/N columns junction, leading to the highest V_{bd} value. The V_{bd} value of the SJ structure strongly depends on the net charge balance, as shown in Fig.2.7. Positive or negative CB conditions leads to the bending of the equipotential lines and to the creation of an electric field peak at bottom or top of the SJ structure, respectively with the subsequent reduction of the V_{bd} value. The fast V_{bd} decrease with a small variation of the CB condition leads a CB margin for the process sensitivity in the range of 10%. In this thesis, positive and negative CB conditions account for P_{rich} and N_{rich} SJ structures, respectively. A more detailed study on the electrical behaviour of devices with different CB conditions is reported on Chapter 3.

$$CB = \frac{P_{conc} - N_{conc}}{N_{conc}} \quad (\%) \qquad \textbf{(Eq.8)}$$

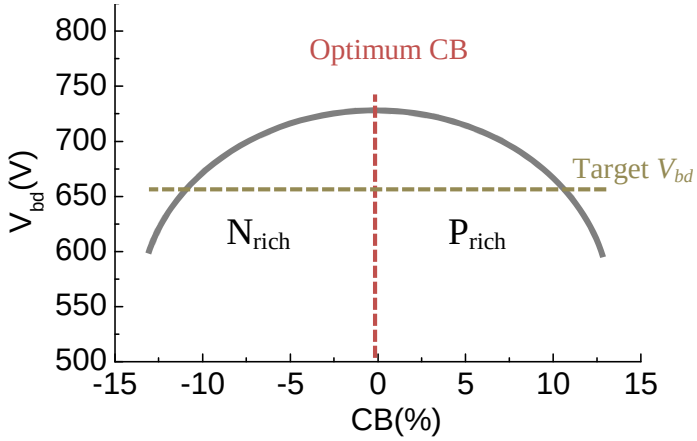


Fig.2.7. Schema of the V_{bd} dependence on the CB condition.

Going back to the FOM reported in Fig.2.6-(b), notice that the sR_{on}-V_{bd} trade-off decreases with the p value. The sR_{on} is reduced since the width of the pillars decreases with the p value and the doping concentration is increased to maintain the desired voltage capability[1]. The V_{bd} value is not degraded since the doping concentration of both pillars can be increased. Therefore, if the p reduction is feasible from the lithography point of view, a better sR_{on}-V_{bd} trade-off can be achieved. The new ideal sR_{on}-V_{bd} trade-off in the SJ structures is described by Eq.9, where W_N and W_P are the widths of N and P columns, respectively, and E_C is the critical electric field[4]. The improvement of the R_{on} value is basically due to the modified depletion process as a consequence of the P column implementation, leading to an almost rectangular equipotential distribution in the basic cell of the SJ structure[4].

$$\boldsymbol{R_{on-ideal\ SJ} = \frac{V_{bd}}{\varepsilon_s \mu_n E_C^2}\left(\frac{W_N + W_P}{2}\right)} \qquad \text{(Eq. 9)}$$

It was described that the C_{oss} and C_{rss} values decrease with the drain voltage in the case of a power VDMOS transistor. However, the full depletion of the SJ pillars is typically achieved at low voltage values (less than 100 V), leading to a sharp decrease on the capacitance values at low voltage and to a significant improvement of the switching frequency in comparison with the power VDMOS counterpart[14]. The Q_g is also reduced when using a SJ MOSFET instead of a UMOS transistor. A more detailed study on the capacitive behaviour of SJ MOSFETs for different CB conditions is reported on section 3.3.2.

2.3. Different SJ-MOSFET structures

The idea of this section is to give a brief description of the different technologies used to implement power SJ transistors. The first commercial power MOSFET implemented with the Super Junction concept was called the CoolMOS™ (by Infineon)[15]. The technological integration of a CoolMOS™ transistor requires the

repeated iteration (5-6 times) of the growth of several microns of N doped epitaxial layer followed by the subsequent Boron masked implantation (Fig.2.8), known as multi-epitaxy/multi-implant (ME/MI) technology. The exact number of iterations depends on the desired final column depth which will set the V_{bd} value. It has to be considered that the first Boron implant is submitted to the thermal budget of the 5-6 epitaxial growths. Opposite, the last Boron implant is just submitted to one drive-in process. As a consequence, different mask windows are mandatory to implement straight vertical pillars at the end of all the ME/MI steps. This is a Global CB approach, meaning that the whole silicon active area contributes in the charge balance when the structure is reversed biased.

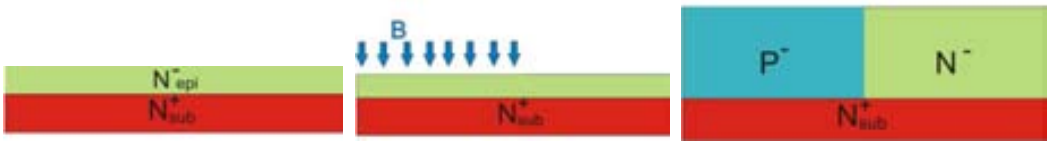


Fig.2.8. Basic schema of the ME/MI technology for the integration of a CoolMOS™ transistor: (a) N^-_{epi} growth, (b) Boron implant and (c) final structure after 5 iterations.

The area of power devices has to be minimized in order to increase the number of devices per wafer in a production line. There are different ways to reduce the device area, as implementing a trench gate or increasing the doping concentration of the pillars to make them thinner[16]. However, the cell pitch in the case of the ME/MI structure is limited by the multiepitaxial growth process. When Boron implants are diffused at high temperature during the epi growth steps, it is necessary to have a minimum pitch to ensure the correct fabrication of the separated deep P columns. The cell pitch could be reduced if a lower thermal budget is used. Therefore, less Boron would laterally diffuse but the number of subsequent epitaxial growths would increase to reach identical column depth and so the cost of each CoolMOS™ transistor. The edge termination of the CoolMOS™ transistor is also implemented with alternating P and N-type columns, thicker and more spaced than those of the active area, using the same mask sequence. In this way, the electric field will decrease smoothly in the edge termination region. The last Boron implant is skipped and a Field Plate is used to enhance the field distribution on the edge termination[17]. A top view of the CoolMOS™ SPP02N80C3 transistor is shown on Fig.2.9-(a)[18], with the gate located at the left side and the remaining metal of the source wire in the middle of the active area. Two P-type pillars are shown in the image obtained with the Scanning Capacitance Microscopy (SCM) technique (Fig.2.9-(b)[18]). The waved shape of the pillar walls gives evidence about how the pillars are formed: six epitaxial layers are grown with the Boron implant after each growth step.

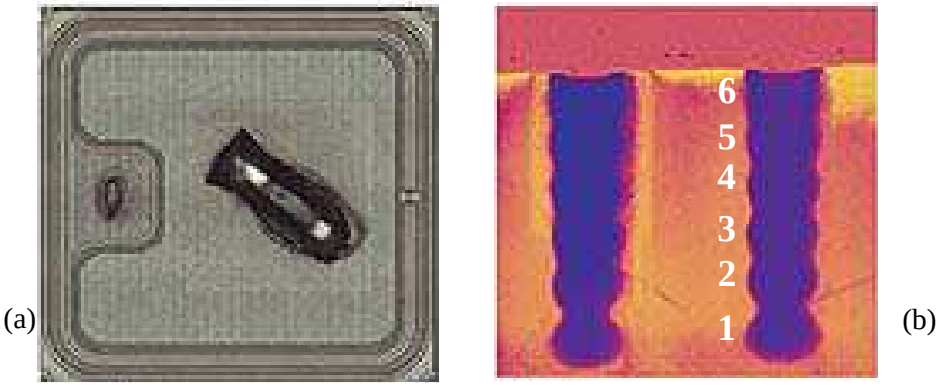


Fig.2.9. (a) Top view and (b) SCM image of the ME/MI technology for the integration of the CoolMOS™ SPP02N80C3 MOSFET. Adapted from [18].

Another approach to implement a Global CB MOSFET is based on deep trenches etched on a high doped N-type substrate and filled with a selectively grown P-type epitaxial layer[19,20,21] (Toshiba, Fuji Electric, Fairchild and Toyota). The resulting SJ power MOSFET exhibits a lower sR_{on} value since the N-type pillar is thinner than that of the CoolMOS™ counterpart implemented with the ME/MI technique. The main drawback of the filled deep trench approach is the eventual creation of a void in the middle of the P-type trench during the epitaxial growth when the trench becomes closed before the complete fill. This effect can be observed on the SEM images corresponding to the DTMOS-4 transistor (Toshiba) captured on Fig.2.10[19]. These devices use a trench gate architecture that contributes to the reduction of the gate charge and the switching losses. The trench gate is shown in Fig.2.11, located in between the P-type pillars, labelled as Poly. The N-type substrate can be seen at the bottom of the trench gate.

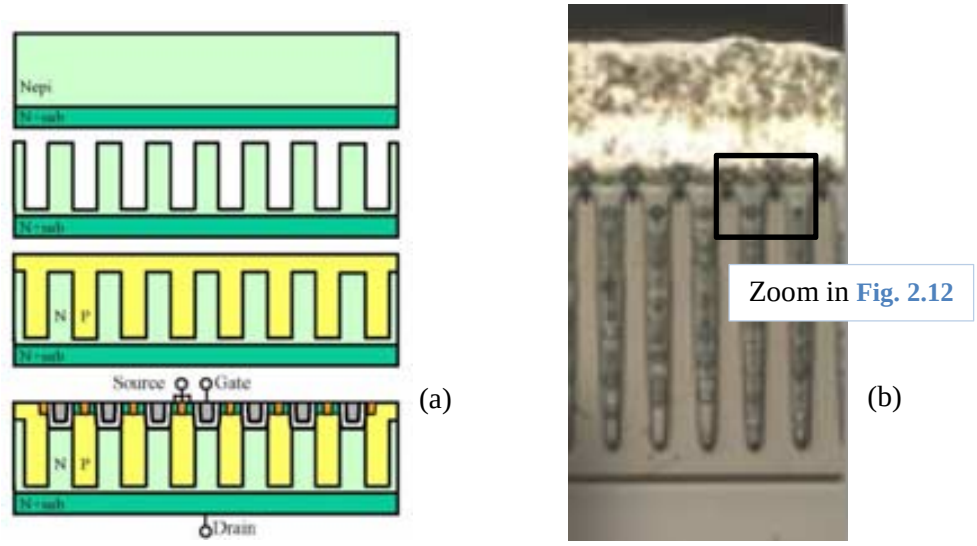


Fig.2.10. (a) Basic schema of the trench fill technology and (b) SEM cross section of the DTMOS-4 transistor (Toshiba). Adapted from [19].

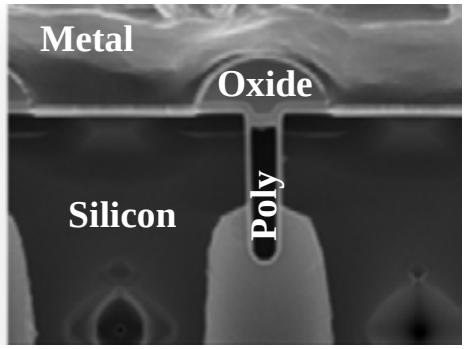


Fig.2.11. SEM cross section showing the trench gate and the top of the pillars for the DTMOS-4 transistor (Toshiba). Adapted from [19].

A novel possibility to apply the SJ concept to high voltage MOS transistors is known as Local CB, meaning that just a region of the structure contributes to the charge coupling in the silicon volume. The UltiMOS transistor (ON Semiconductor) is a vertical Local CB device: the first one was presented 10 years ago[21], but it is not reported that it ever went in production. The UltiMOS structure is implemented by etching deep trenches in a lowly doped N-type substrate with the subsequent filling of the trench with a high doped N and P-type epitaxial layers[22,23](see Fig.2.12) and the final sealing of the trenches with an oxide plug. Given that the N^-_{epi} layer basically works as a mechanical support, the cell pitch can be reduced if compared with the previous Global CB approach, since only the width of the gate trench needs to be ensured between adjacent deep trenches, leading to a reduction of the on-state resistance. The SEM image of the UltiMOS active area (see Fig.2.13) shows the gate trench at the top of the structure and the void in the middle of the SJ trenches with the oxide plug on top. The edge termination of the UltiMOS transistor is implemented with the conventional floating guard rings technique, in contrast with the Global CB SJ power MOSFETs where this technique cannot be used due to the high doping concentration of the epitaxial layer[4].

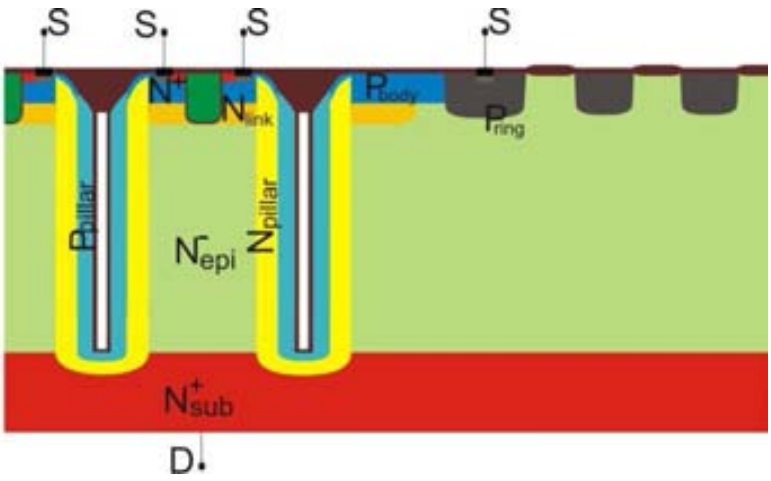


Fig.2.12. Cross section of the UltiMOS structure.

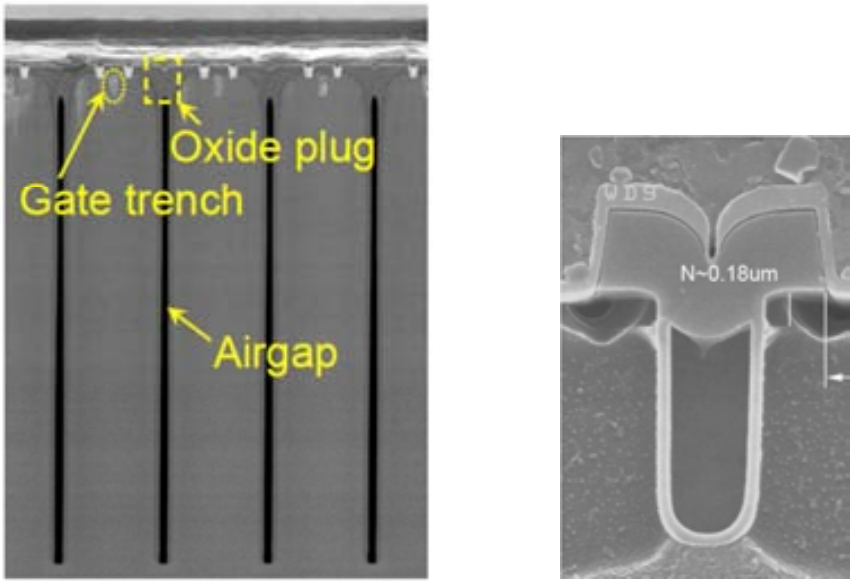


Fig.2.13. SEM image of an UltiMOS transistor. (a) Complete vision of the vertical pillars and (b) zoom in the gate region. Adapted from[23].

2.4. Main requirements of the SJ MOSFET transistors

This thesis is dedicated to the study of the 20 A SJ power MOSFET transistors with a voltage capability in the range of 600 V. Nowadays, there are several companies that have launched their SJ MOSFET into the market. An exhaustive optimisation task has to be performed in every new power device before becoming a commercial product to be sure that the electrical performances in the state-of-the-art and superior to the competitors in some of the most relevant parameters. Moreover, new power devices have to be competitive on cost and energy efficient in circuit operation. There are several standard tests to quantitatively compare power MOSFETs when making a choice for a certain application. As introduced, the SJ power MOSFET transistors are basically designed to be used in applications such as switched mode power supply synchronous rectifiers where the internal body diode can be activated when the device turns off[24]. Different parameters have to be optimized in a power transistor to accomplish with the market requirements:

- An optimum R_{on}-V_{bd} trade-off minimizes the conduction losses. The R_{on} of a SJ power MOSFET has to be in the range of 150-250 mΩ to be commercially competitive in the 600 V, 20 A market. The R_{on}-V_{bd} values for different commercial power MOSFETs are plotted in Fig.2.14.

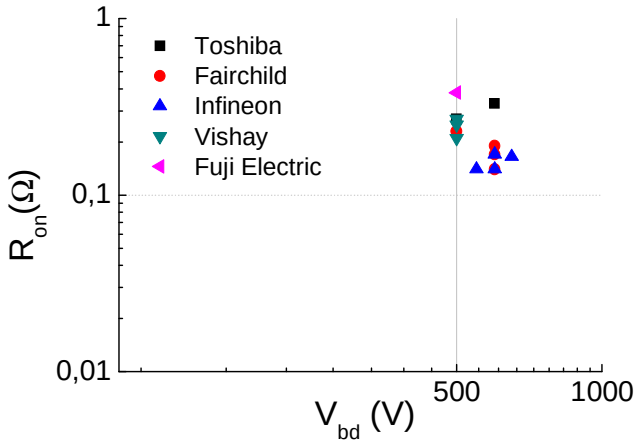


Fig.2.14. V_{bd}-R_{on} FOM for commercial SJ power MOSFETs.

- The C_{rr} and the C_{oss} capacitances have a strong impact on the switching time, thus they need to be minimized. The Q_g value (Q_{gs}+Q_{gd}) determines the gate drive loss and it is extremely dependant on the gate voltage[6]. In high-frequency applications (higher than the standard 100-300 kHz) a low FOM $sR_{on}{\cdot}Q_g$ is required to obtain a high performance transistor[25]. On the other hand, C_{oss} is ruled by the C_{ds} capacitance as already explained, which basically depends on the device architecture. Competitive capacitive values for four commercial 600 V and 20 A SJ power MOSFETs are detailed in Table 2.2. The voltages at which the measurements are performed are defined in Table 2.3. However, Infineon's counterpart is rated for I_d=25-30 A (IPB60R125CP), where the chip area might be increased, leading to a lower R_{on} value. The package for all the devices is the TO-220FP. Notice that the Toshiba counterpart has the lower $R_{on}{\cdot}Q_g$ value. Thus, from the point of view of reducing the swithing losses, this device should be selected.

	Toshiba ***TK20E60U***	**STMicroelectronics** ***STP26NM60N***	**Infineon** ***IPB60R125CP***	**Fairchild** ***FCP20N60***
R_{on} **(Ω)**	0.165	0.135	0.125	0.15
Q_g **(nC)**	27	60	53	75
Q_{gs} **(nC)**	16	8.5	12	13.5
Q_{gd} **(nC)**	11	30	18	36
$R_{on}{\cdot}\,Q_g$ **(mΩ nC)**	4455	8100	6625	11250
C_{iss} **(pF)**	1470	1800	2500	2370
C_{oss} **(pF)**	3500	115	120	1280
C_{rss} **(pF)**	150	1.1	-	95

Table 2.2. R_{on}, Capacitive and charge values for commercial SJ MOSFET.

Measurement voltage	Toshiba *TK20E60U*	STMicroelectronics *STP26NM60N*	Infineon *IPB60R125CP*	Fairchild *FCP20N60*
Q	400 V	480 V	350 V	480 V
C	10 V	50 V	100V	25 V

Table 2.3. V_{ds} at which the capacitance (C) and charge values (Q) listed in Table 2.2 are measured.

- The Reverse Recovery characteristics of the internal diode determine the reverse recovery time (T_{rr}) value, quantifying the time to remove the charge during turn-off and **how fast the device can be switched off under extreme conditions** (see Appendix B). Therefore, the T_{rr} needs to be as short as possible since no positive bias can be applied to the gate until the diode is completely turned off, thus limiting the device operating frequency. The reverse recovery charge (Q_{rr}) to be removed during the diode turn-off has to be also minimized to decrease the switching time. However, the turn-off behaviour of the intrinsic diode of all the SJ power MOSFETs is relatively poor when compared with an optimized equivalent power diode. Since the recovery of the SJ diode has a very steep di/dt, the occurrence of high frequency and high amplitude recovery oscillations during transients is more possible[24]. The comparison of the T_{rr} and Q_{rr} values for commercial SJ power MOSFETs is provided in Table 2.4. From the point of view of recovering after a high voltage peak, the more robust device is the STMicroelectronics counterpart.

	Toshiba *TK20E60U*	STMicroelectronics *STP26NM60N*	Infineon *IPB60R125CP*	Fairchild *FCP20N60*
T_{rr} (ns)	450	370	430	530
Q_{rr} (µC)	8.1	5.8	9	10.5
Test Set-up	20 A, di/dt=100µA/µs	20 A, di/dt=100µA/µs	400 V, di/dt=100µA/µs	20 A, di/dt=100µA/µs

Table 2.4. T_{rr}, Q_{rr} and measurement conditions for diferent commercial SJ power MOSFETs.

- The UIS test evaluates the **energy capability when an inductor is discharged through the internal body diode of a power MOSFET**. The body diode is forced to handle a high voltage during a certain periode of time, which is translated in a lot of power dissipation requirements. Normal values of commercial SJ power MOSFET transistors are in the range of 340-600 mJ for a given area (from commercial datasheets). Values for different commercial components are detailed in Table 2.5. Notice that the Toshiba counterpart is measured with a fixed inductance value whereas all the other are performed at a fixed current level, sweeping the inductance. For further details on these tests, see Appendix B. Notice that, even the Toshiba counterpart would be selected for the swithing characteristics, the E_{AS} value is quite low.

	Toshiba *TK20E60U*	STMicroelectronics *STP26NM60N*	Infineon *IPB60R125CP*	Fairchild *FCP20N60*
E_{AS} (mJ)	114	610	636	690
Test set-up	L=0.63mH, R_g=25Ω	V_{dd}=50V, I_d=6 A	V_{dd}=50V, I_d=5.2 A	V_{dd}=50V, I_d=10 A

Table 2.5. E_{AS} and measurement conditions for diferent commercial SJ power MOSFETs.

UIS and Reverse Recovery tests are performed under extreme conditions and the device under test is usually driven to failure. In this sense, both tests provide relevant information about the device robustness. However, just the UIS test is used in commercial datasheets to give the amount of energy that the device can handle while the Reverse recovery is used to quantify the time to recover when the device is submitted to hard switching conditions.

Concluding, the main commercial SJ power MOSFETs have been presented. The selection of a particular device is strongly dependent on the requirements of each application (switching speed, robustness, internal diode behaviour).

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CHAPTER 3

UltiMOS structure

The main part of the experiments, measurements and simulations reported in this thesis have been performed on the power SJ UltiMOS structure. This chapter is basically conceived to have an insight in the device requirements based on the application which is designed for, the structure design, the electrical behaviour, and the available parameters to vary. The goal is to provide all the necessary information for a complete understanding of Chapters 4, 5 and 6. The technology process and the different used experimental techniques and simulation methods are detailed in Appendix A and B, respectively.

3.1. UltiMOS target

The UltiMOS structure is a SJ power MOSFET rated to 600 V applications, with a sR_{on} in the range of 20-25 mΩcm^2 and a nominal current of 20 A[1]. As a rule of thumb, a power device designed for a certain voltage application range has to exhibit a higher voltage capability for a safe operation. In this sense, the target UltiMOS V_{bd} value is 650 V, although some measured devices and simulated structures during the investigation reach higher V_{bd} values, in the range of 750-800 V. The V_{bd} value is basically determined by the doping and the thickness of the SJ trenches[2]. A wide UltiMOS manufacturing window is needed to be able to go into the market and to ensure a high enough V_{bd} value to get the maximum yield (see schema on Fig.3.1). The 650 V needs to be still guaranteed even if the CB is varied, copping with the possible manufacturability variation. Therefore, different CB conditions are normally implemented for the different experiments performed during the UltiMOS optimization. Once the required sR_{on} value is reached, the N_{conc} is fixed in the fabrication process and the P_{conc} is modified to get the different CB conditions. The variation of the P_{conc} is not high enough to modify the sR_{on} value[3]. From the manufacturing point of view, there are different process steps that

need to be accurately defined to get the required results, as the SJ trench etch or the epitaxial growth (Appendix A).

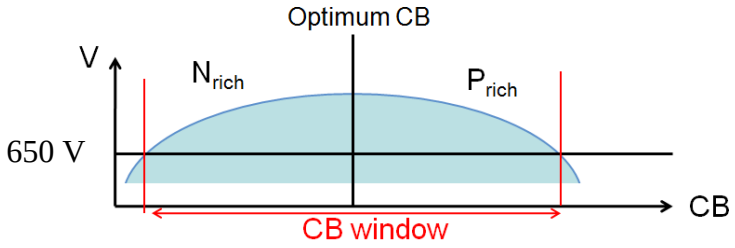

Fig.3.1. A wide CB window has to be defined to have a manufacturable technological process.

3.2. Device description

The development of a new power device starts with the procuring of the main requirements, as the sR_{on} and the C_{rr} values. These basic parameters are optimised by a suitable choice of the active area design criteria with the help of TCAD simulations and clean room experiments. In this chapter the electrical behaviour of the UltiMOS transistor is explained and the technological requirements for the desired electrical performance are described. The function of the different layers and the critical parameters directly impacting the UltiMOS electrical performance (doping concentrations, junction depths, etc.) has to be studied. If an initial parametric analysis is performed, the tuning of the critical parameters during the UltiMOS optimization will be time efficient. The effect of the different parameters on the electrical UltiMOS performance is analysed separately for the active area and the edge termination due to the strong impact of the device periphery on its reliability in avalanche conditions.

3.2.1. Active Area

The UltiMOS active area consists on a thick N^-_{epi} layer, grown on the starting N^+ substrate (N^+_{sub}), where deep trenches are etched[1]. N and P-type epitaxial layers are grown on the sidewalls of the trenches (N_{pillar} and P_{pillar} layers). These trenches go into the N^+_{sub} layer, as shown in Fig.3.2, and are sealed with oxide, leaving a void in the middle. The regions directly contributing to the UltiMOS switching performance are implemented at the top of the structure: the N^+, P_{body} and N_{link} diffusions and the gate trench. A P-type region is present at the top of the N_{pillar} to connect the P_{body} and the P_{pillar} regions to do not have a floating P_{pillar} that could introduce instabilities, parasitic diodes or BJT's activation, etc. The structure is homogeneous in depth from the bottom of the gate to the N^+_{sub} layer. The shallow N^+ diffusion is placed at both sides of the gate trench top to minimise the on-state resistance and the consumed Silicon area at a given

current capability. The P_{body} layer is used to implement the MOSFET channel and mainly determines the V_{TH} value of the power transistor. Therefore, the channel length depends on the depth of the P_{body} diffusion. The source metal contacts the shallow N^+ diffusion but also the P_{body} diffusion to do not leave this diffusion floating. The drain contact is placed at the bottom of the structure, on the N^+_{sub} layer. A detailed explanation of the whole technological process to achieve the described structure can be found in Appendix A.

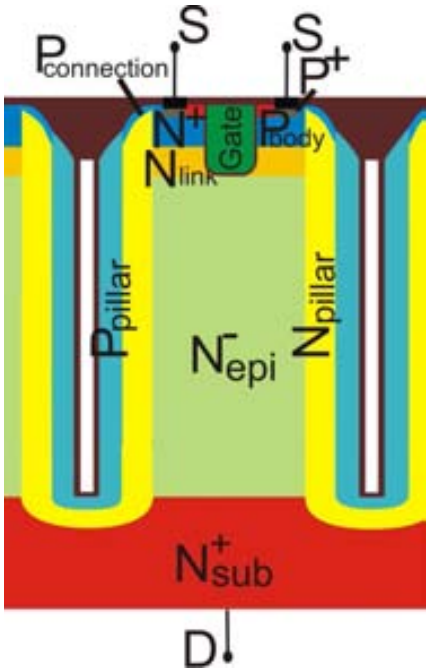

Fig.3.2. Cross-section of UltiMOS active area.

3.2.1.1. Electrical behaviour and role of different regions

The main technological parameters are determined by the electrical requirements, and the device design needs to be done accordingly. For instance, the gate trench has to go into the N_{link} diffusion to avoid an increase on the sR_{on} and V_{TH} values. Moreover, the N_{link} needs also to be deep enough to do not counter dope the P_{body} region.

- **Threshold voltage (V_{TH})**

On Fig.3.3-(a) the simulated I_d-V_g is plotted showing a V_{TH}=4.5 V, taken at I_d=250 µA. It can be observed that when the device is switched on at high temperature, the I_d value in the on-state decreases a 50%, leading to a heavy increase of the sR_{on} value due to the decrease in mobility at high temperatures. On the other hand, when the temperature increases from 25 to 125 ºC the V_{TH} decreases from 4.5 to 3.7 V, taken at I_d=250 µA. Therefore, if the device is heated during its normal operation, it will not turn on provided the gate voltage is relatively high. On Fig.3.3-(b) the isothermal simulated I_d-

V_{ds} characteristics for different V_g values are plotted. Note that when V_g is higher than 5 V the curves exhibit a slight current increase in the saturation mode.

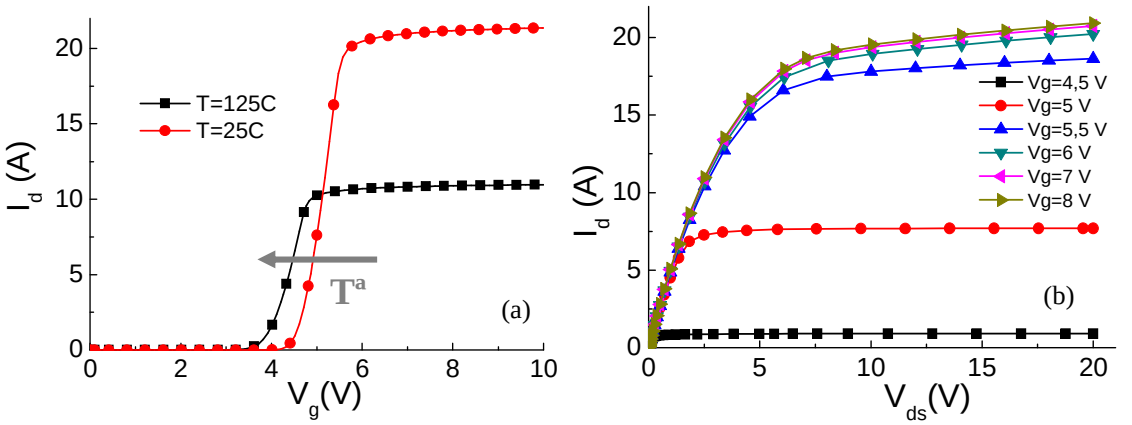

Fig.3.3. Simulated UltiMOS (a) I_d-V_g curves for different temperatures and (b) I_d-V_{ds} curves for different V_g values.

- **Specific On-Resistance (sR_{on})**

The N_{link} diffusion is used to reduce the sR_{on} value: when the device is in the on-state, the current flows from the N^+ source through the channel created in the P_{body} region, the N_{link} diffusion and the N-type pillar to the drain contact (see Fig.3.4-(a) and (b)). The sR_{on} versus the I_d value is plotted in Fig.3.5. The sR_{on} value at 10 A is 22 $m\Omega \cdot cm^2$, taking into account the W of the device. Notice that the sR_{on} strongly increases when the current is in the range of 20 A (current saturation).

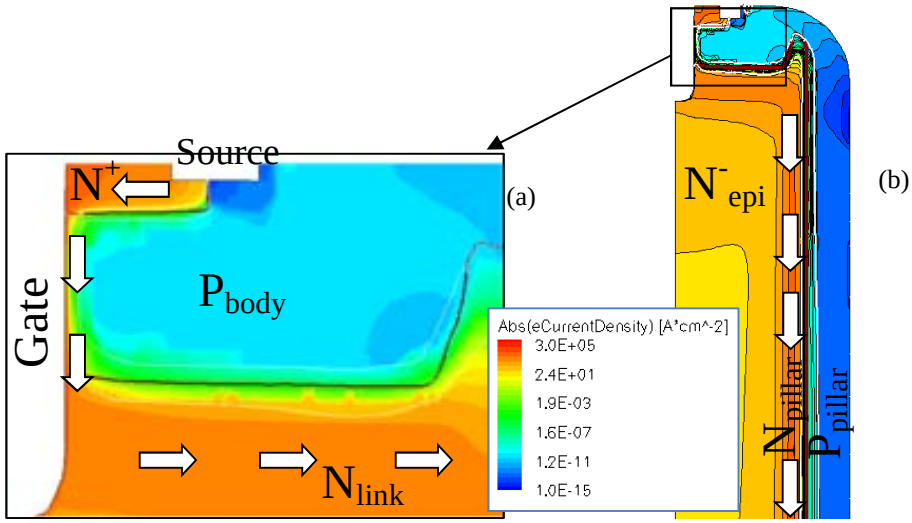

Fig.3.4. Simulated current flow at the top of the UltiMOS structure in the on-state when V_g=12 V and V_{ds}=20 V. (a) Zoom of the top part and (b) half-cell.

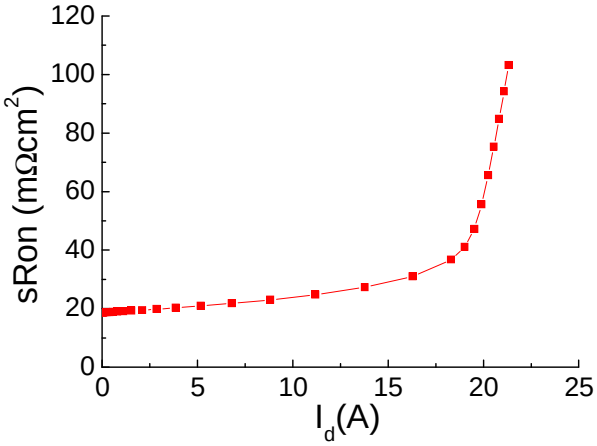

Fig.3.5. (a) Measured UltiMOS sR_{on}-I_d curve at V_g=20 V.

- ## Charge balance and voltage capability (V_{bd})

As introduced, the UltiMOS transistor is a Trench SJ power MOSFET structure, based on the Local CB approach where the two pillars (N-P) are the main contributors to the charge balance when the device is in the off-state. The N^-_{epi} contribution on the CB is in the range of 3.3%, as derived from simulation results. This is translated as a 3.3% addition of majority carriers to the N_{conc} for the CB calculation. The depletion behaviour of the structure depends on the CB condition, but all the structures become fully depleted at 15-20 V for any CB condition. The complete explanation of the depletion process at different CB conditions is detailed in section 3.3.2.

The V_{bd} value is one of the most important parameters on the UltiMOS design and it is very sensitive to small CB variations. Therefore, the V_{bd} value needs to be high enough to ensure a wide manufacturing window. The isothermal simulated I_d-V_{ds} curves for different CB are plotted in Fig.3.6. The curves are scaled taking into account that the current is equally distributed in the whole active area. As expected, the V_{bd} value is maximum for the Optimum CB I_d-V_{ds} curve, decreasing for both N_{rich} and P_{rich} cases (see Fig.3.6). The potential lines for different V_{ds} values are plotted in Fig.3.7. The vertical line where the potential distribution changes its shape is the interface between the N-P pillars. See that the lines tend to flatten when the V_{ds} increases. As inferred from Fig.3.8, the potential lines get closer at the top or at the bottom of the structure, for N_{rich} or P_{rich} devices, respectively. Accordingly, one can see in Fig.3.9 how the E_F peak has a different location depending on the CB condition: at the bottom of the SJ trench for the P_{rich} and at the gate bottom/top of the SJ trench for the N_{rich} case, following the potential lines crowding placement. This effect is typical for SJ structures, in exception of the E_F peak at the bottom of the gate, which is due to the trench gate architecture and the E_F crowding in that region[4,5]. The creation of an E_F peak at the gate bottom can be used to determine the CB condition, as detailed in section 3.3.1.

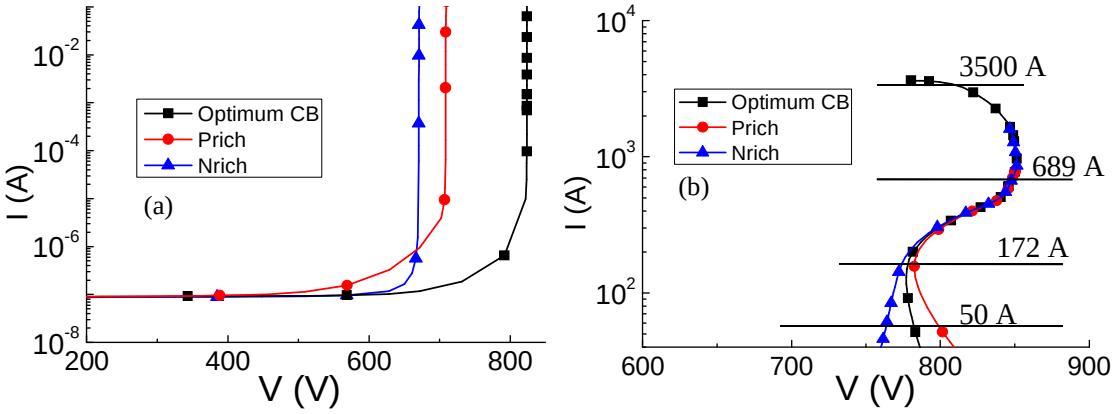

Fig.3.6. Isothermal simulated I_d-V_{ds} curves of the UltiMOS active area to determine the V_{bd} value for N_{rich}, Optimum CB and P_{rich} cases at (a) avalanche current level and (b) high current. The curves are scaled by the whole active area.

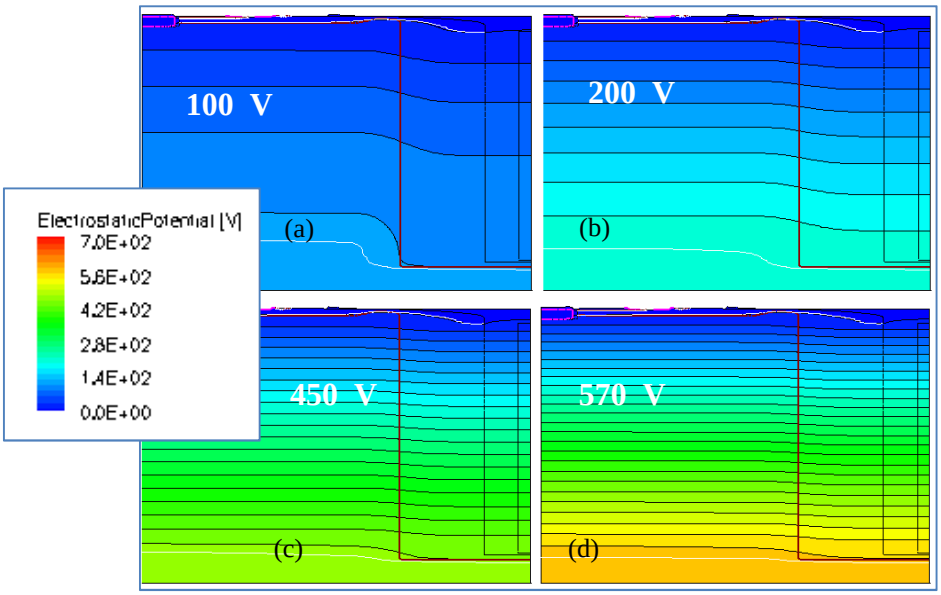

Fig.3.7. Snapshot of potential lines at (a) 100 V, (b) 200 V, (c) 450 V and (d) 570 V for an N_{rich} device. Correspondence with curves in Fig.3.6-(a).

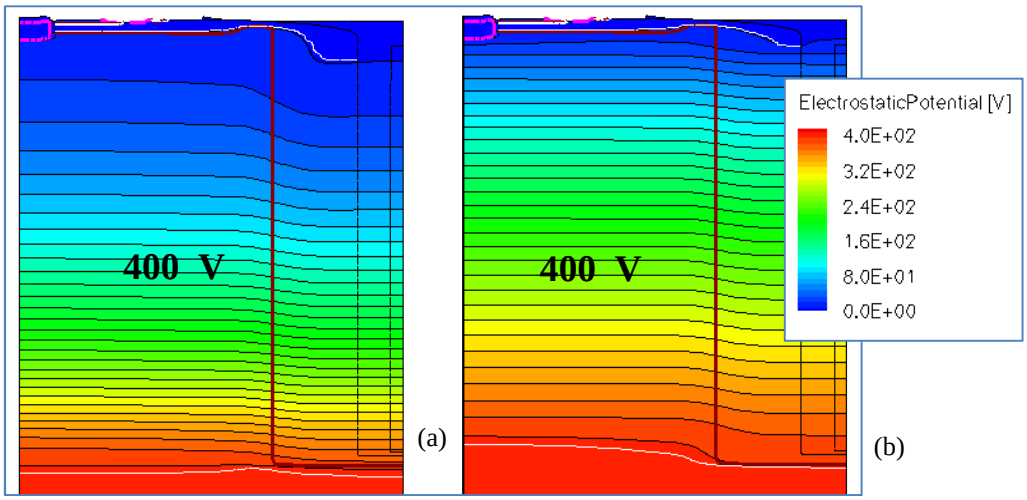

Fig.3.8. Snapshot of potential lines at 400 V for (a) P_{rich} and (b) N_{rich} structures. Correspondence with curves in Fig.3.6-(a).

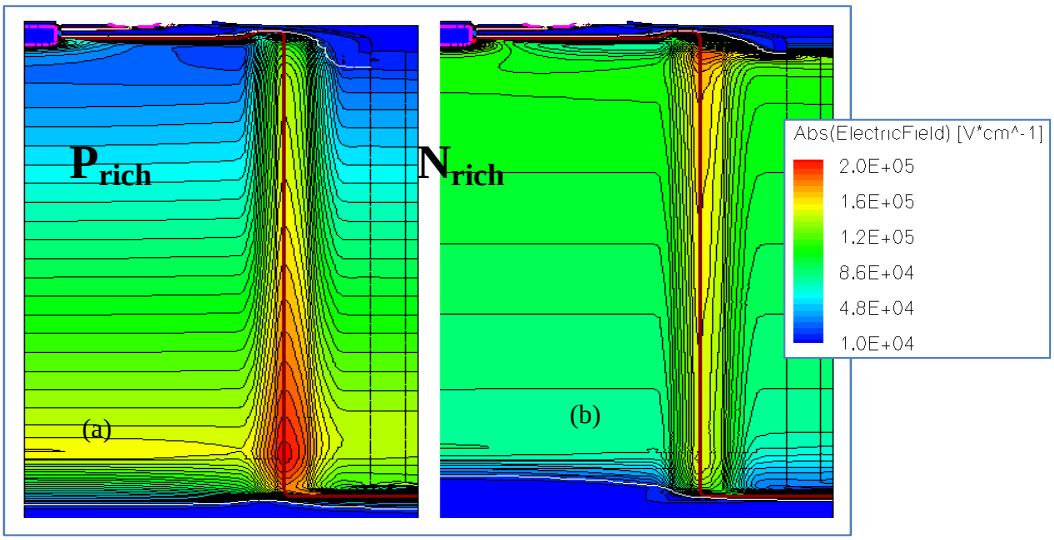

Fig.3.9. Snapshot of the electric field distribution at 1× 10^{-6} A for (a) P_{rich} and (b) N_{rich}. Correspondence with curves in Fig.3.6-(a).

- **Snapback in avalanche conditions**

The device performance at very high current is not relevant since the device will be already destroyed due to the high current density values. As detailed in Appendix B, the simulated I_d-V_{ds} curves are normally scaled taking into account that the current is homogeneously distributed in the whole active area, as for the I_d-V_{ds} curves in Fig.3.6. The snapback occurs at a current level in the range of 700 A, which is physically impossible to be achieved. Therefore, if the current is focalized in a small region of the device, the current density flowing through that region would be even much higher than de current density at 700 A[6]. Therefore, the I_d-V_{ds} curve should be rescaled. For instance, if the current is focalized in the periphery of the device, the curve should be scaled for the corresponding area and the resultant curve is like the one plotted in Fig.3.10. As derived, the snapback current level is in the range of 1 A when the current is focalized.

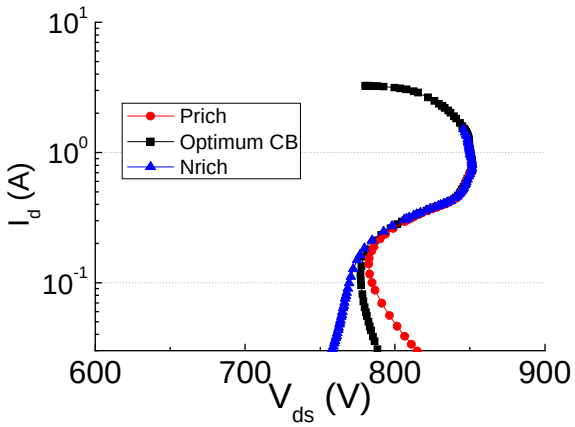

Fig.3.10. Isothermal simulated I_d-V_{ds} curves of an UltiMOS transistor, scaled taking into account that the current is focalized in the device periphery.

It is worth to say that a first Negative Differential resistance (NDR) branch is sometimes present for certain CB conditions (see Fig.3.11). This effect is induced by changes on the electric field distribution in the device active area and it can be destructive if the current cannot be properly re-distributed in the device[6,7]. Nevertheless, this effect cannot be further studied since simulations are just a qualitative tool to describe the current distribution on the 2D half-cell of the active area, without taking into account the 3D nature of the device. Moreover, no measurements can show this type of behaviour.

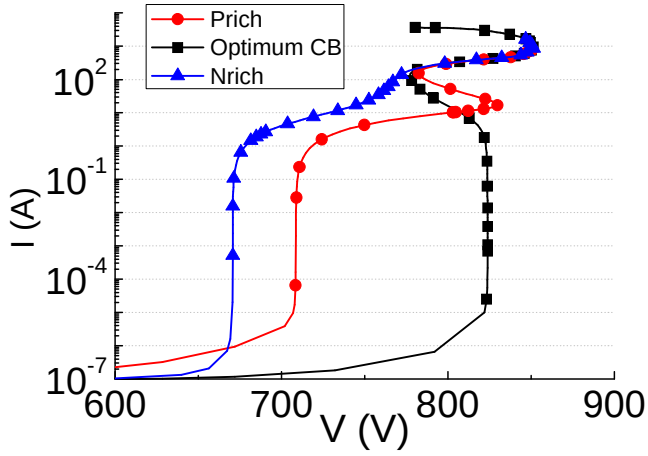

Fig.3.11. Isothermal simulated I_d-V_{ds} curves of the UltiMOS transistor for different CB conditions. All the curves are scaled by the whole active area.

Snapshots of the electron current density are taken at the current levels where the last snapback takes place, according to Fig.3.6. As shown in Fig.3.12, above 800 A the I_d-V_{ds} curves go into snapback since the parasitic bipolar transistor ($N^+/P_{body}/N_{link}$) is activated[8]. This snapback effect is independent of the CB condition and it happened when the potential in the P_{body}/N^+ junction reaches the V_{bi} (built-in potential) value, forward biasing this junction. On Fig.3.12 the electron current density in the top region of a half cell of the active area is plotted at different current levels. The gate is at the left side of each picture and the horizontal line in the middle-bottom of the trench gate corresponds to the P_{body}/N_{link} junction. It can be deducted from Fig.3.12-(b) to Fig.3.12-(c) that the main electron current flux moves from the P_{body}/P_{pillar} path to the $N^+/P_{body}/N_{epi}$ path when the total current is increased. The NDR branch starts at 689 A, leading to the device destruction. The electrical behaviour at low current levels depending on the CB condition and a detailed bipolar activation study can be found in Chapters 4 and 5.

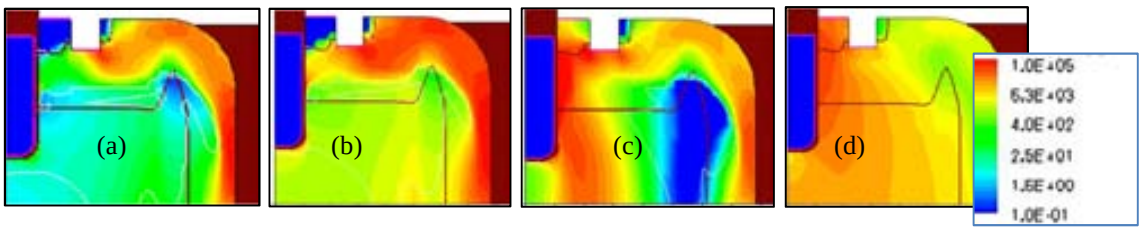

Fig.3.12. Snapshot of the simulated electron current density at (a) 50 A, (b) 172 A, (c) 689 A and (d) 3000 A.

3.2.1.2. Impact of the main technological parameters

The effect of the main technological parameters on the electrical behaviour of the UltiMOS structure is presented in this section. The studied parameters are sR_{on}, V_{bd} and V_{TH}, since they are strongly dependent on the changes in the technological process. The study is basically performed with TCAD simulations (technological and electrical simulations) to see how the electrical performance of the device changes both in the active area and in the periphery/edge termination regions. To know more about how the TCAD simulations are performed, see Appendix B.

- **Specific On-Resistance (sR_{on})**

The sR_{on} value is used to quantify the conduction losses in a device with certain area, and it is measured at I_d= 10 A when the drain voltage is swept from 0 to 20 V at V_g=10 V. As already stated, the electrons flow in the on-state regime through the N_{link} and the N_{pillar} regions. Therefore, the sR_{on} value basically depends on the resistivity of the two regions (see Fig.3.4), decreasing with the total length of the resistive electron current path. Different parameters can be tuned to optimise the sR_{on} value: the N_{link} length (layout optimisation), the N_{link} dose and depth and the N_{conc}. For instance, if the device cell pitch (p) is reduced, the N_{link} region becomes smaller and the required area for the device with the same current capability decreases, thus the sR_{on} value can be decreased. This effect is shown in Fig.3.13-(b), where different p values are plotted. On the other hand, if the N_{link} region was not present, the current would flow through the N^-_{epi} to reach the N_{pillar} and as a consequence, the sR_{on} would be highly increased (see Fig.3.13-(a), where no N_{link} is present in the simulated structure). When the N_{link} is implemented, the sR_{on} value saturates as the implanted dose is increased, as shown in Fig.3.13. This is because the contribution of the N_{link} starts to be lower than the influence of the N_{pillar} resistance, but the fact that the area remains the same is also important.

The N^-_{epi} concentration has no influence on the sR_{on} since the on-state current does not flow through that region (see Fig.3.14-(a)). An increase of the N_{conc} enhances the sR_{on} value, but an increase of the N^-_{epi} thickness degrades the total resistance, as shown in Fig.3.14-(b) since the depth of the SJ trench also increases to be sure that the bottom of the trench reaches the N^+_{sub}, forcing the current to flow through more microns of N_{pillar}. Finally, an increase of N_{conc} has to be compensated by the corresponding increase of P_{conc} to accomplish the CB between pillars and the targeted V_{bd} value. However, the increase of the doping concentration of the pillars is electrically limited by the creation of an abrupt junction between the N_{link} and P_{body} layers.

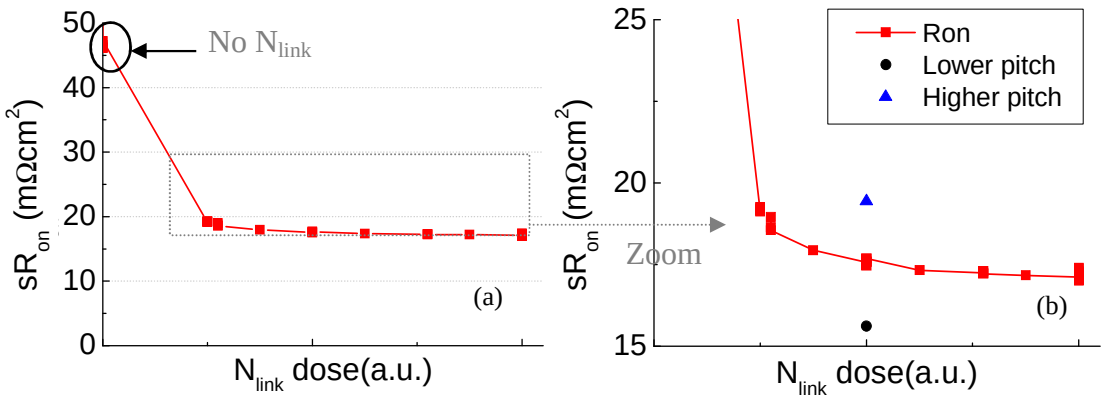

Fig.3.13. Simulated dependence of (a) the sR_{on} with the N_{link} dose and (b) zoom of the saturation of the sR_{on} value when increasing the N_{link} dose. On (b) the sR_{on} for different p is also plotted.

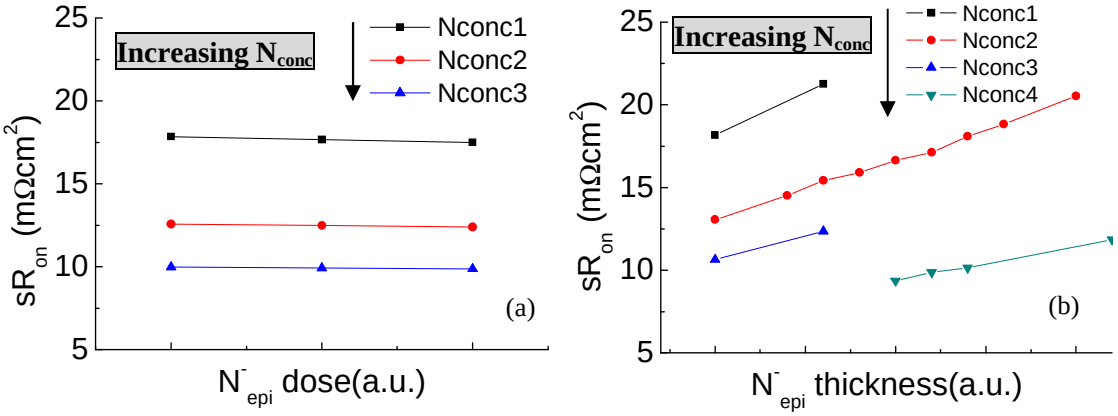

Fig.3.14. Simulated dependence of the sR_{on} with the (a) N^-_{epi} concentration and (b) N^-_{epi} thicknesses for different N_{conc}.

- ## Breakdown Voltage (V_{bd})

The V_{bd} value is typically measured at 250 µA, once the device is already in the avalanche regime. The V_{bd} value depends mainly on the doping and thickness of the N-P pillars, although there are other parameters with a direct impact, as the N^-_{epi} concentration or the SJ trench depth. The V_{bd} value for different CB conditions for structures and SJ trench depths are plotted in Fig.3.15. There is no difference between the square and circle curves, since both SJ trench reaches the N^+ substrate in both cases. However, when the SJ trench depth is further decreased it does not reach the N^+ substrate, an N-type layer (N^-_{epi}) remains at the bottom of the SJ trenches and a shift on the CB curve towards the N_{rich} side is present (triangle curve in Fig.3.15).

The V_{bd} value decreases when increasing the N_{conc}, as shown in Fig.3.16-(a). The epitaxial growth of the N-P pillars has to be accurately processed due to the large variation of the V_{bd} value when the doping concentration of the pillars is slightly modified. Furthermore, the N_{conc} needs to be high to get a low enough sR_{on}. Note that the V_{bd} value saturates with increasing the N_{conc} for Optimum CB structures due to the creation of a high E_F peak in the N_{pillar}/P_{body} junction (the junction is too abrupt).

The N^-_{epi} layer thickness has also a huge impact on the V_{bd} value (see Fig.3.16-(b)). As expected, the V_{bd} value increases with the N^-_{epi} layer thickness when the N_{conc} and P_{conc} are kept constant. This effect is evident for optimum CB devices but for N_{rich} and P_{rich} devices the V_{bd} value saturates due to the bending of the potential lines at the top or bottom of the SJ pillars (N_{rich} and P_{rich}, respectively). As a consequence, the E_c value is reached at lower voltage values. On the other hand, no degradation on the voltage capability is found when modifying the N_{link} or the P_{body} concentration, because both regions become completely depleted at 10-20 V.

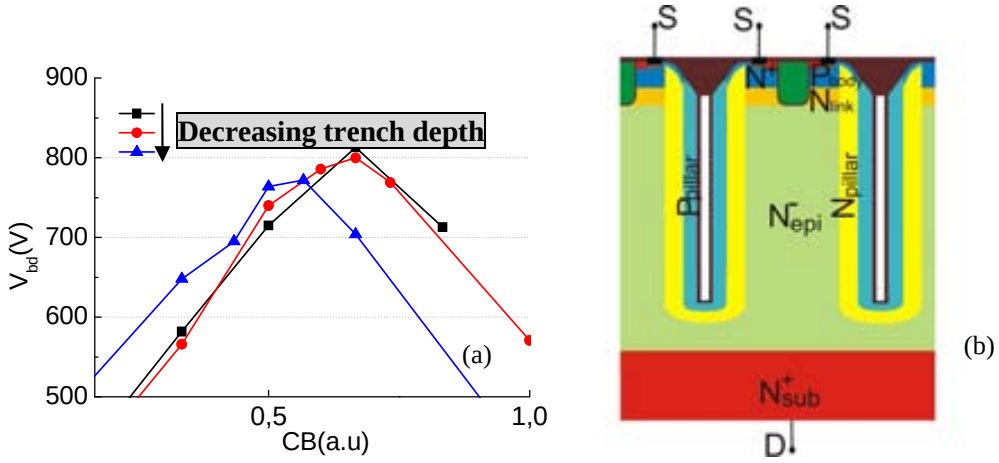

Fig.3.15. (a) Simulated dependence on the depth of the SJ trenches for different CB conditions. (b) Cross-section of an active cell with reduced SJ trench depth.

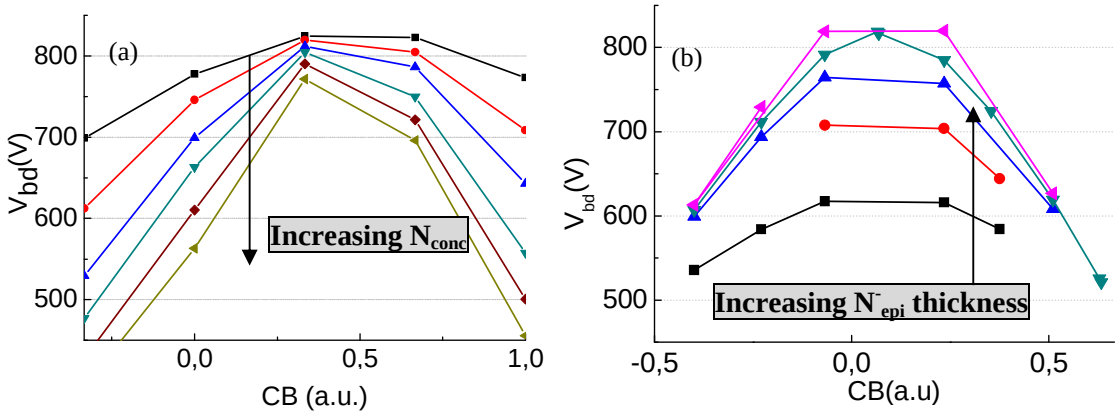

Fig.3.16. Simulated dependence of the V_{bd} value on (a) N_{conc} and (b) on N^-_{epi} thickness, for different CB conditions. All the other parameters are fixed.

Different N^-_{epi} concentrations have been used to simulate the active area of the UltiMOS structure, extracting the corresponding V_{bd} value. No variation is expected as deducted from Fig.3.17-(a). It can be concluded that the N^-_{epi} concentration has no relevant impact on the V_{bd} value in the active area since the contribution of the N^-_{epi} to the CB is just a 3.3%, as already introduced. The V_{bd} variation for different P_{body} and N_{link} doses is plotted in Fig.3.17-(b). For P_{rich} devices the variation is almost zero since the E_F peak is at the bottom of the structure. On the other hand, N_{rich} devices show a spread on V_{bd} values because the E_F peak is at the top. Since the N_{link} and the P_{body} doping

levels are modified, small changes on the impact ionization values are forced, thus the V_{bd} value slightly varies.

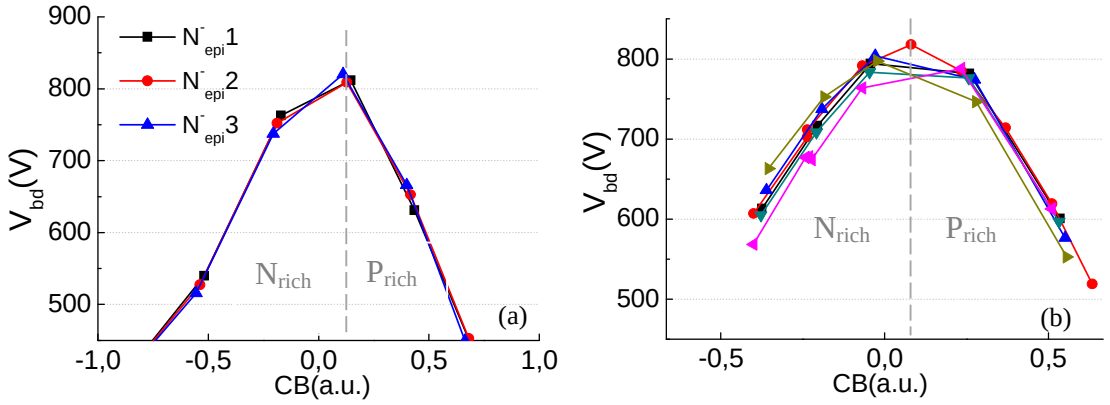

Fig.3.17. Simulated dependence of the V_{bd} value on (a) the N^-_{epi} concentration and (b) the P_{body}-N_{link} doses for different CB conditions.

- **Threshold voltage (V_{TH})**

The V_{TH} is measured at 250 µA when the drain and gate electrodes are swept from 0 to 10 V. The V_{TH} value is targeted at 3.5-4.5V for the UltiMOS transistor, being basically determined by the P_{body} dose, the gate oxide thickness and the channel length. As shown in Fig.3.18-(a) V_{TH} increases with the P_{body} dose, but the N_{link} dose has no influence on the V_{TH} value. The channel length mainly depends on the depth of the P_{body} diffusion and it is technologically determined by the gate trench architecture. The gate trench has to reach the N_{link} layer and it has to be deep enough to be filled even in the trench ending, where the contact is placed and the trench is wider. Indeed, the trench has to be properly planarized on its total length. No study has been carried out on the gate oxide thickness variation, although it is well known that the thicker the oxide, the higher the V_{TH}[9]. Notice in the I_d-V_g curves plotted in Fig.3.18-(b) that the V_{TH} value does not depend on the CB condition.

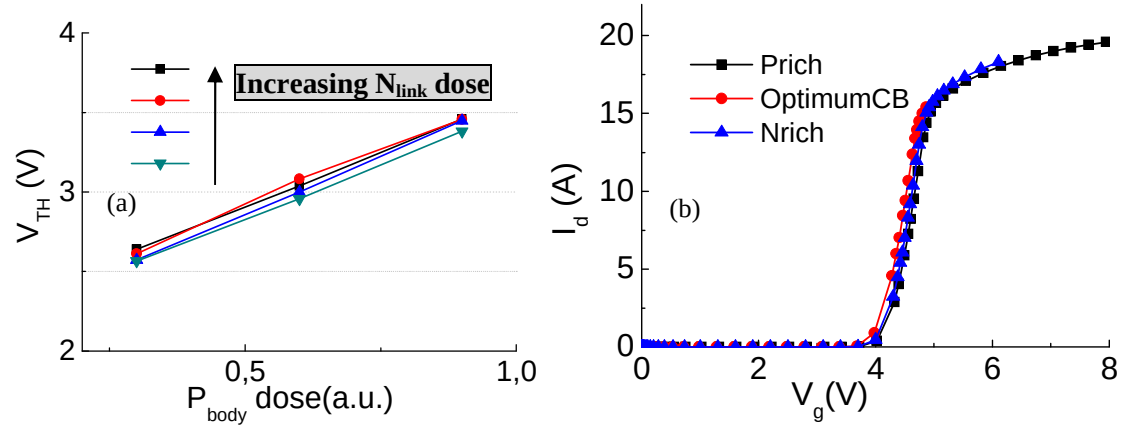

Fig.3.18. Simulated dependence of the (a) V_{TH} on the P_{body} and N_{link} doses and (b) simulated I_d-V_g curves for different CB conditions.

3.2.2. Edge termination

Different approaches for the edge termination can be used in a Power SJ MOSFET (e.g. pillar termination[10] or oxide box filled[11]), although a floating guard-ring termination[12,13] is preferred in the UltiMOS transistor(see cross section in Fig.3.19). As introduced in Chapter 2, a simple guard-ring edge termination is feasible in the UltiMOS architecture due to the low N^-_{epi} concentration and the subsequent high V_{bd} value (the physical explanation is detailed later in this section). Two additional masks on the process flow (see Appendix A for the fabrication process) are used to grow the Field Oxide (FOX) and to create the floating rings (P_{ring} diffusions). Since these steps are done at the very beginning of the technological process, the SJ structure is not affected by the long thermal budget used to grow the FOX and to diffuse the rings. It is of big relevance to realize that the edge termination structure forms basically a PiN diode.

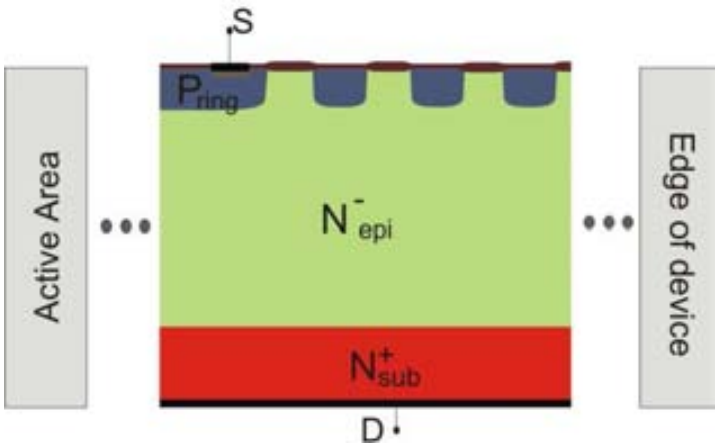

Fig.3.19. Cross section of a conventional Floating Guard Ring edge termination structure.

The UltiMOS edge termination surrounds the active area, starting at the outmost SJ trench. The N_{link} and P_{body} diffusions of the last active cell are enlarged to reach the first P_{ring} diffusion (see Fig.3.20). The region in between the active area and the edge termination is defined as periphery since it does not act as active area because there is no SJ trench, no N^+ nor gate trench, but it neither has the edge termination function of smothering the electric field. The P_{body}-N_{link} diffusions of the last active cell are connected to a P_{ring} diffusion with higher dose than the P_{body} diffusion to avoid a premature breakdown at the curvature of the P_{body}-N^-_{epi} junction. This first grounded P-type diffusion is called Grounded Ring (GR), and has to be grounded to take profit of the floating ring design[14]. All the other P-type rings are floating with a metal on top to have a good potential distribution all along the ring area. To confirm the lower V_{bd} value when no GR is present, a layout with no GR is added to the test mask set (referred to FET10). The GR is not required in a power diode since the dose implanted on the rings is the same as the dose implanted in the active area of the device. If the P_{body} diffusion

in UltiMOS transistor had the same dose as the P_{ring} the V_{TH} value would be higher than the requirements (since $P_{ring}>P_{body}$). Therefore, an extra parameter is added to the UltiMOS structure optimization when a floating ring edge termination is used: the P_{ring} dose, setting the location of the $E_{F\ peal}$: active area or edge termination. The P_{ring} dose is also used to tune the edge termination breakdown voltage (TV_{bd}) without degrading the active area characteristics. A detailed study on the performance of the designed floating ring edge termination can be found in Chapter 4.

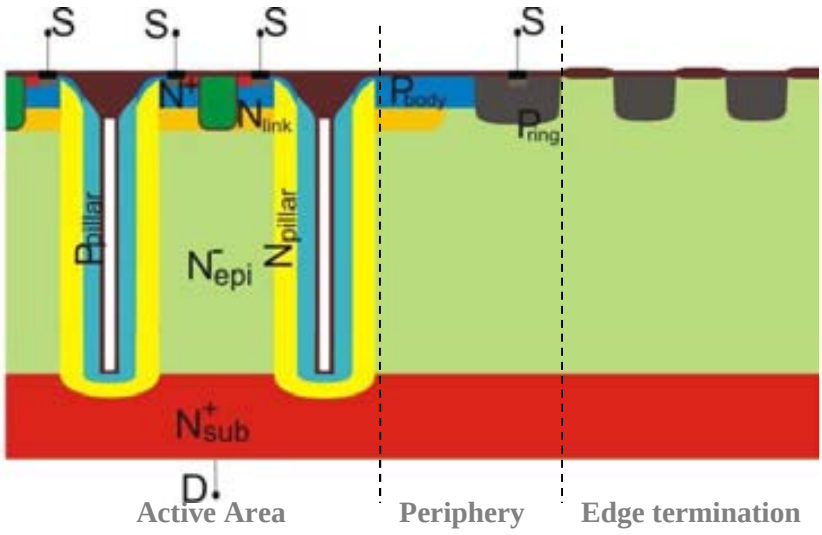

Fig.3.20. Cross section of the UltiMOS last active cells, periphery and edge termination

3.2.2.1. Electrical behaviour

The physics of a floating ring edge termination is based on the uniform lateral electric field distribution to handle the high voltage[9]. Each ring takes up part of the lateral voltage between the source contact (at ground) and the edge of the device, where the so-called channel stopper is placed, and hence shapes the lateral electric field. The channel stopper is an N^+ diffusion at the very edge of the device and it is normally implemented by using the same mask as the N_{link} or the N^+ layers (highly doped). Therefore the channel stopper is biased close to the drain voltage (e.g. at 600V) since it is directly implanted on the N^-_{epi} layer. At the same time that the E_F is being laterally distributed over the ring termination, a vertical electric field between each P-type ring and the N^+ drain builds up. The interaction between both electric field distributions will determine the V_{bd} value of the device.

The number of rings is chosen during the optimization of the edge termination. The simulated cross-section of the 8 ring edge termination of an UltiMOS structure is drawn in Fig.3.21-(b). Last microns of the active area are included for the sake of accuracy. The isothermal and non-isothermal I_d-V_{ds} curves of an 8 ring edge termination are shown in Fig.3.21-(a), where the V_{bd} value is in the range of 675 V. On the same plot,

different measured curves are added to see the accuracy that is reached by TCAD simulations[15].

The evolution of the vertical and lateral E_F when the current is increased is plotted in Fig.3.22. The vertical E_F is taken at the GR region, where it is maximal, while the lateral E_F is plotted along the Silicon surface. The lateral E_F exhibits the typical peaks located at the right edge of each P_{ring}[9]. In the performed simulations, at I_d=10 nA the device is already in avalanche and both vertical and lateral E_F rise with the current (see Fig.3.22). At higher current levels, the E_F can be slightly increased, as shown in the vertical E_F cuts on Fig.3.22-(b) (from $1x10^{-8}$ to 0.17 A), creating a Positive Differential Resistance (PDR) branch. On the other hand, the lateral E_F is not increasing with the current after the impact ionisation starts, as deducted from Fig.3.22-(a).

If the current is further increased, the charge induced by the impact ionisation becomes higher than the background doping of the N^-_{epi} layer[16,17]. Thus, the voltage is reduced with increasing the current, creating an NDR branch. This phenomenon was reported for the first time by Egawa[18]. As shown in Fig.3.22-(b) (1.3 A), there is a huge increase of the E_F value at the top and bottom of the N^-_{epi} layer, while there is a decrease in the E_F value in the whole centre region of this layer. As inferred from the electric field snapshots shown in Fig.3.23 from simulations, the electric field is not homogeneously distributed at high current level as it happens at lower current levels. The higher electric field is mainly located in the GR region, where the resistance of the current path from ground to high voltage is minimal. This effect leads to the well-known **current focalization in that area and the device is destroyed** due the huge amount of current density. This effect in normally not desired in an edge termination, where the electric field needs to be homogeneously distributed on the whole edge termination area to get the highest voltage capability.

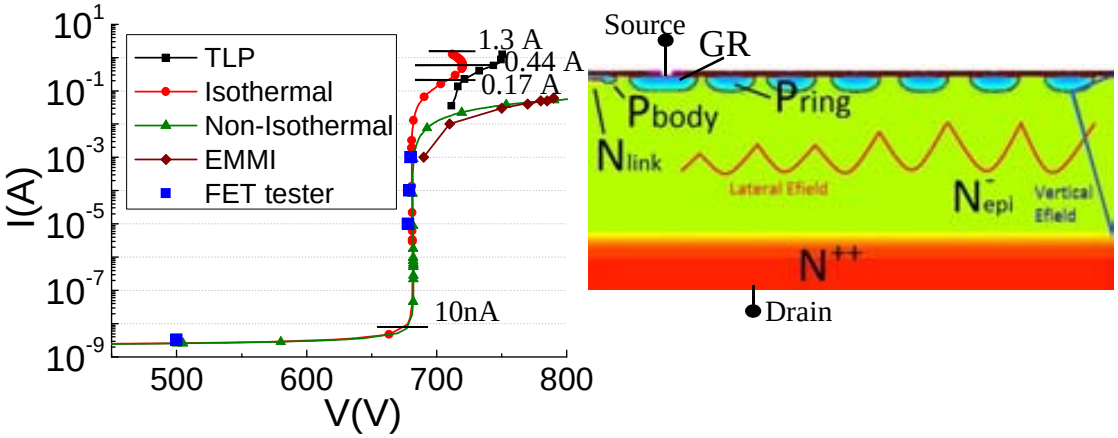

Fig.3.21. Simulated (isothermal and non-isothermal) and measured (TLP, EMMI, FET tester) I_d-V_{ds} curves corresponding to an 8 ring edge termination structure. Current levels are marked for correlation with E_F cuts reported inFig.3.23 and Fig.3.22.

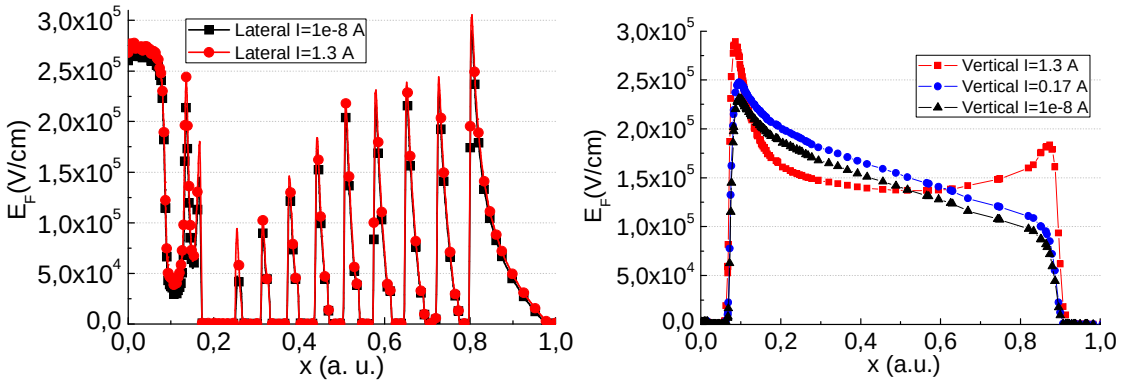

Fig.3.22. Lateral E_F distribution at 10 nA and 1.3 A and vertical E_F distribution at 10 nA, 0.17 A and 1.3 A for the edge termination with the *I-V* curve reported on Fig.3.22.

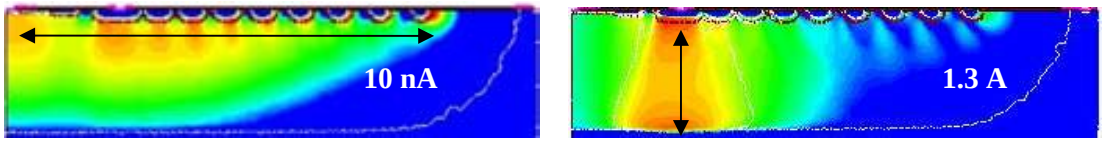

Fig.3.23. Snapshots of the simulated electric field distribution at 10 nA (left) and 1.3 A (right) for an 8 ring edge termination structure.

3.2.2.2. Impact of the main technological parameters

As in all edge termination designs, there are different parameters to tune to get the maximum voltage capability[13]. The spacing between rings (W_b) and the width (W_r) of each ring have to be optimised to obtain the desired smooth lateral electric field distribution which leads to the maximum V_{bd} value (see Fig.3.24 for parameter correspondence). There are two main ways to optimise the W_r and W_b values: varying the spacing between rings and the width of the rings or keeping both parameters constant for the whole edge termination area[9]. However, it is assessed by Brieger[19] that the optimum design is reached following the second approx. The selected optimized UltiMOS edge termination is implemented with 8 (1st approx.) or 6 (2nd approx.) rings, using the same silicon area in both cases. The resulting I_d-V_{ds} curves for both structures with the same P_{ring} dose are plotted in Fig.3.25. A similar V_{bd} value is reached in both cases but lower than the ideal value which is extracted from the 1D simulation. As expected, the 1D V_{bd} value is higher than the 2D one since no junction curvatures are considered with no potential lines bending and the subsequent reduction of the V_{bd} value. The first measurements and simulations reported on Chapter 4 are performed on the 8 rings edge termination structure to assess that the electrical performance is the same for both designs. However, the main results on the thesis are extracted from devices with 6 ring edge termination structure.

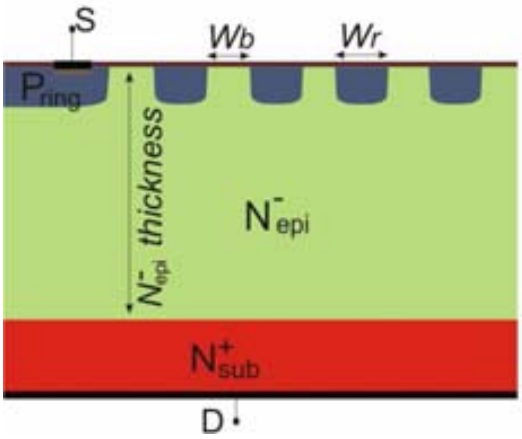

Fig.3.24. Cross section of the edge termination region with the parameters to be tuned.

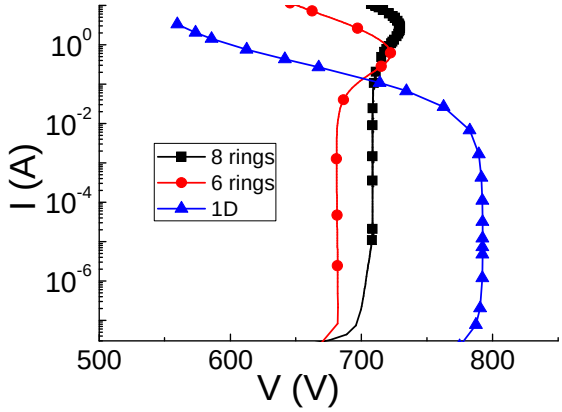

Fig.3.25. 1D and 2D simulated I_d-V_{ds} curves. 2D simulations are for PiN diodes with the 6 and 8 rings edge termination structures shown on Fig.3.24.

As already introduced, a GR is needed to do not degrade the V_{bd} value [14]. If the highly doped GR would not be implemented, the P_{body} implant should be used for the rings, with the subsequent increase of consumed area due to the shallower and lower doped diffusion in comparison with the P_{ring} diffusion. However, the optimization of the edge termination region does not concern this thesis since the layout was already defined and optimized. In Fig.3.26 the cross sections of the structures with and without GR are drawn. The comparison on the V_{bd} value for devices in the same wafer with-without GR is provided on Fig.3.27-(b) where it can be inferred that the V_{bd} value is always higher when the GR is present. This is because the potential lines are more crowded in the curvature of the P_{body} region when the GR is not present. The P_{ring} dose has to be tuned to get the highest possible V_{bd} value on this termination structure. Thus, the dependence of the V_{bd} value on the P_{ring} dose is plotted in Fig.3.28.

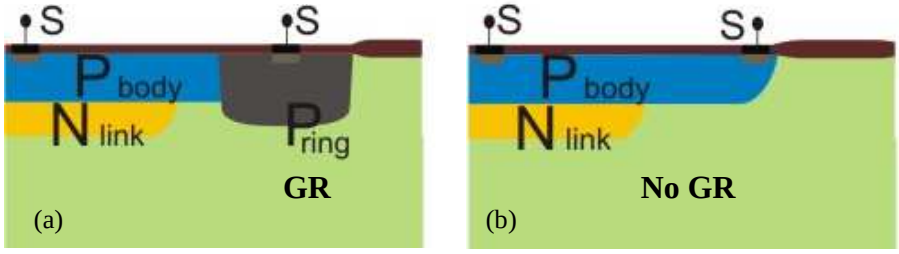

Fig.3.26. Cross section of a structure (a) with and (b) without GR.

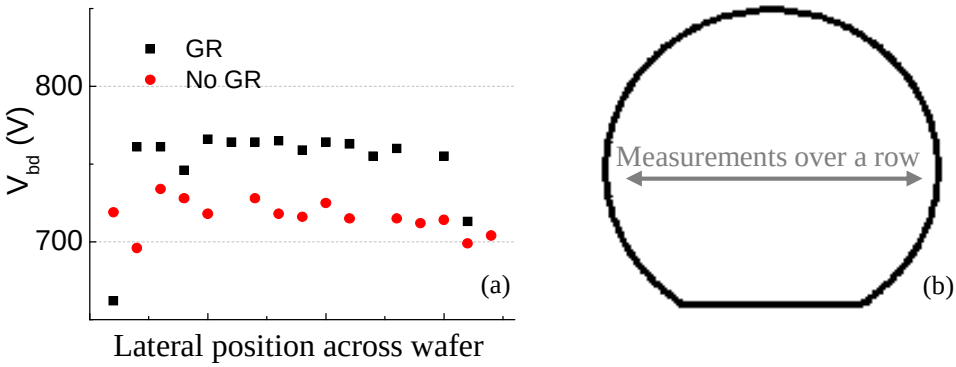

Fig.3.27. (a) Comparison of the measured V_{bd} values corresponding to a PiN diode with and without GR at the edge of the active area. (b) Schema of where the measurements are done in the wafer.

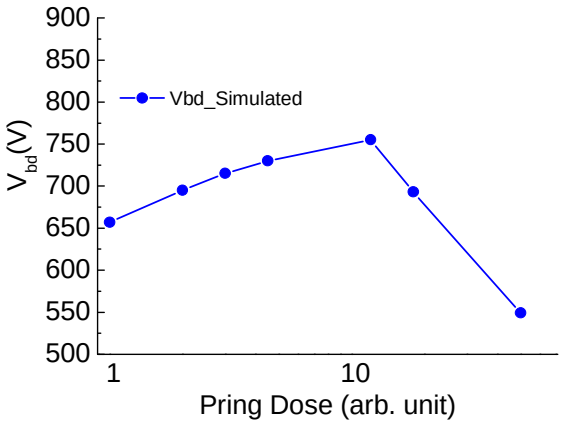

Fig.3.28. Dependence of the V_{bd} value on the P_{ring} dose.

The peaks of the lateral E_F distribution are uniform along the rings at the optimal P_{ring} dose, as shown in Fig.3.29-(a), leading to the highest voltage capability. On the other hand, the lateral E_F distribution exhibits a peak at the outmost ring for high P_{ring} doses while the peak is at the end of the active area for low P_{ring} doses. In both cases, the unbalanced lateral E_F first tries to balance with the increase of the avalanche current level, leading to a more uniform distribution of the electric field over the rings, as observed in Fig.3.29-right. However, before reaching a balanced lateral E_F distribution, the vertical electric field collapses and the negative resistance effect takes place (as shown in Fig.3.22-right).

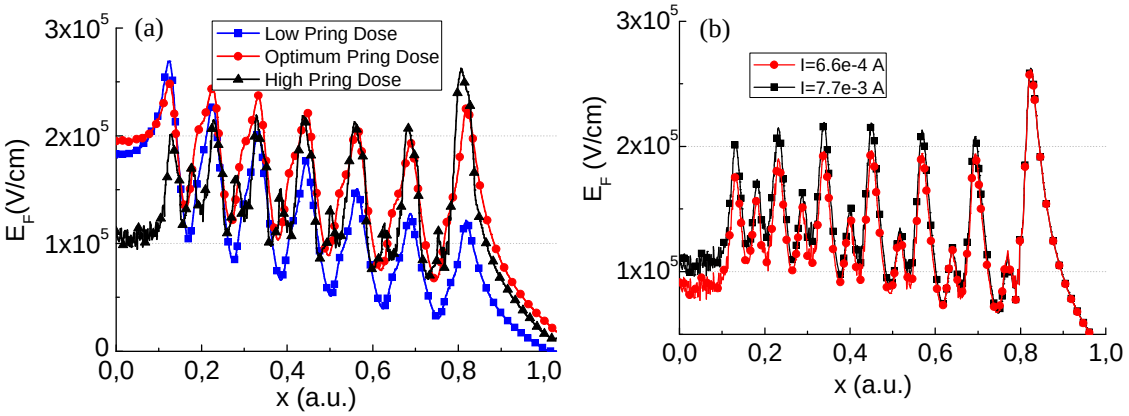

Fig.3.29. Lateral E_F distribution at 7 mA for (a) different P_{ring} doses and for (b) a high P_{ring} dose at different current levels.

The N^-_{epi} thickness has to be also tuned to reach high V_{bd} values. If the N^-_{epi} layer is thicker, the vertical E_F can be further increased before going into snapback due to the Egawa effect. The effect of the N^-_{epi} thickness on the V_{bd} value of the edge termination is plotted in Fig.3.30. Note that if the N^-_{epi} thickness is increased, the electrical performance of the active area will be affected; increasing the V_{bd} and the sR_{on} values (see Fig.3.16-(b) and Fig.3.14-(b)). On the other hand, if the N^-_{epi} concentration is increased, the V_{bd} value is reduced to values out of the target. In the active area this would be translated in a shift in the V_{bd}-CB curve since majority carriers are introduced. With the standard N^-_{epi} doping concentration, the contribution of this region to the CB is just a 3.3%, but if the dose is increased, the percentage will be also increased.

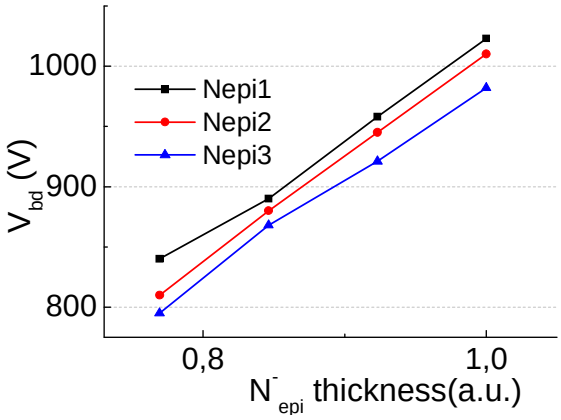

Fig.3.30. Simulated dependence of the V_{bd} value on the N^-_{epi} thickness and concentration, being the concentrations Nepi1<Nepi2<Nepi3.

3.3. Experimental techniques to determine CB condition

During the development of the thesis, two techniques to determine the CB value of a fabricated SJ transistor have been set up. The first technique was discovered while performing UIS measurements on different CB conditions, using different measurement systems, located at different sites: when the gate is switched off, one system grounds the gate but the second system applies -10 V to the gate. Different results on the V_{bd} value, depending on the gate off-state bias, were found for devices that should behave identically (see Fig.3.31) and, as a consequence, a study to dig into the root cause was performed[5]. The second technique was investigated during the study of the depletion behaviour of the UltiMOS active area depending on the CB condition and it is based on the evolution of the C_{rr} curve. As it is shown in section 3.3.2, the C_{rr} curve is highly dependent on the CB condition.

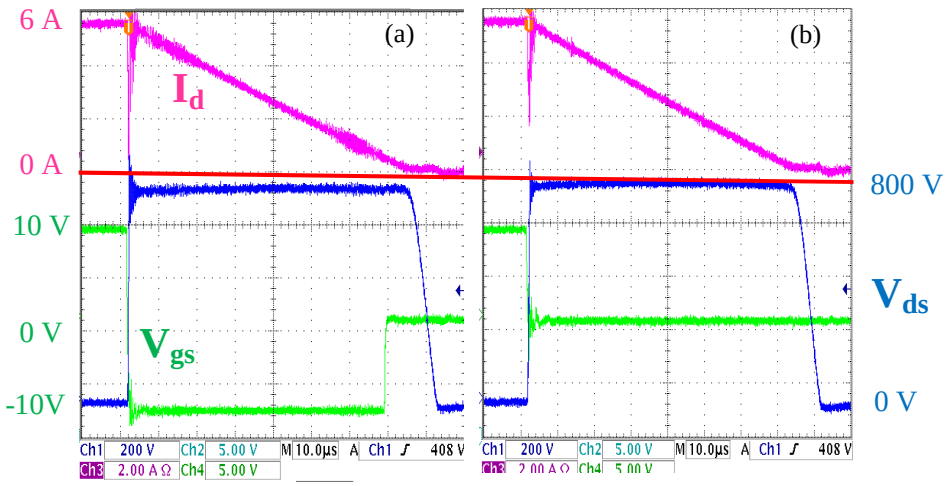

Fig.3.31. Measured I_d, V_{ds}, V_{gs} curves from a UIS pulse on an N_{rich} device with the gate going to (a) -10 V and (b) to 0 V at switch off.

3.3.1. Negative gate voltage effect on the UltiMOS transistors

The experimental data plotted in Fig.3.32-(a) is derived from conventional I_d-V_{ds} curves at different V_{gs} values. The V_{bd} values are taken at 100 µA with V_{gs} values set to 0, -5 and -10 V in the off-state. Note that the voltage capability decreases when a negative V_{gs} value is applied in the off-state for N_{rich} transistors. On the contrary, the V_{bd} value does not show any dependence on the CB for P_{rich} structures. TCAD simulations (see Fig.3.32-(b)) are performed to be able to find the root cause of the different behaviour depending on the CB condition. The main difference between the electrical behaviour for the two structures is that the maximum E_F is at the bottom of the SJ trench for the P_{rich} structure whereas it is at the gate bottom/top of the SJ trench for the N_{rich} case, as it has been already shown in Fig.3.9.

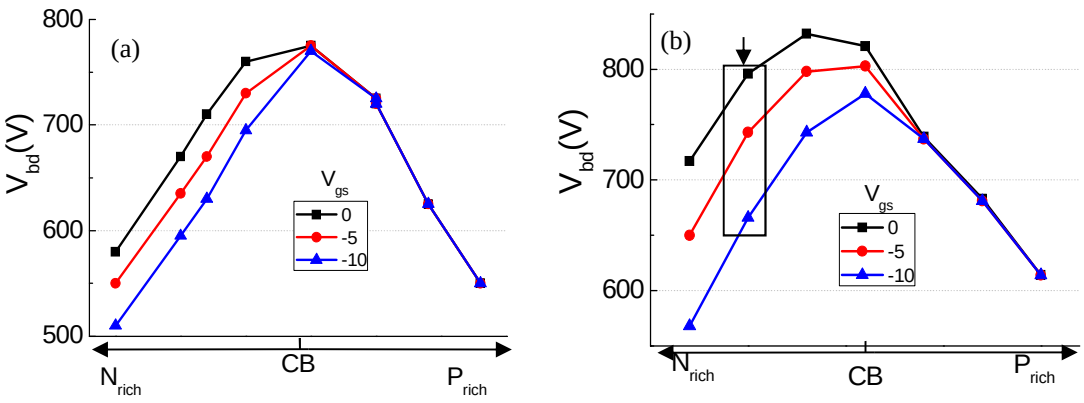

Fig.3.32. (a) Measured and (b) simulated V_{bd} values at 100 µA in UltiMOS transistors with different CB conditions for V_{gs} = 0, -5, -10 V.

The simulated I_d-V_{ds} curves in the off-state for an N_{rich} SJ MOSFET structure are plotted in Fig.3.33. At low avalanche current levels the voltage capability is strongly influenced by the applied off-state gate voltage. The V_{bd} value decreases with the gate voltage from 790 to 660 V when the V_{gs} varies from 0 to –10 V, respectively. At high avalanche current levels (I_d > 100 A) the E_F peak is at the gate corner region for any V_{gs} value and the I_d-V_{ds} shape is no longer dependent on the off-state gate conditions. It is worth to analyse the potential and electric field distribution in the Silicon to understand the I_d-V_{ds} behaviour.

As shown in Fig.3.34-(a), at low avalanche current regime, the potential distribution in the vicinity of the trench gate region depends on the applied V_{gs} value. The potential lines are crowded at the bottom of the trench gate for negative V_{gs} values, at an avalanche current level of 3 A, thus leading to a reduction on the V_{bd} value. The electric field distribution is also modified by the applied off-state gate voltage, as depicted in Fig.3.34-(b). The E_F peak at the corner of the gate trench increases when the gate voltage shifts towards negative values in the analysed N_{rich} structures, where the maximum E_F values are found at the top of the SJ trench, much closer to the gate trench than in the P_{rich} counterparts.

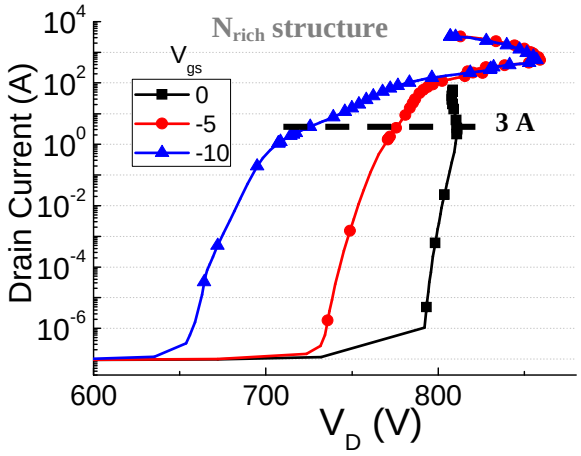

Fig.3.33. Simulated I_d-V_{ds} off-state characteristics for an N_{rich} device at different V_{gs} values (indicated in Fig.3.32).

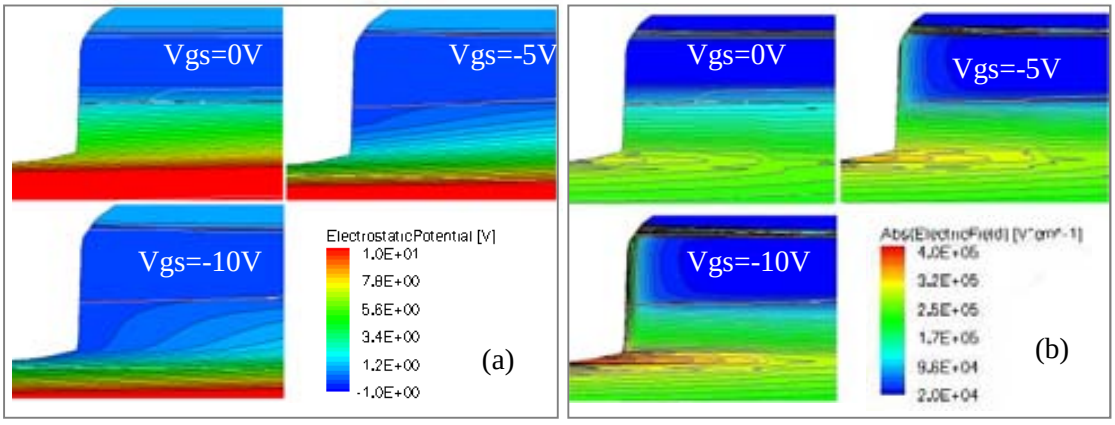

Fig.3.34. Snapshots on the potential (a) and E_F (b) distributions for an N_{rich} device at different V_{gs} values at I_d=3 A. The snapshots are taken at the gate trench corner.

In the case of P_{rich} structures, the maximum E_F is located at the bottom of the SJ trench and, as a consequence, the off-state V_{gs} value will not enhance the focalization of the current at the gate trench corner since the electric field value and the inherent carrier generation due to impact ionisation are much lower than the corresponding values obtained at the bottom of the SJ trench. Therefore, more avalanche current is needed to have a high E_F value at the trench gate bottom and the V_{bd} value is independent of the applied negative gate voltage in the P_{rich} part of the graph. The relation between V_{bd} value and CB conditions plotted in Fig.3.32 is in agreement with the explained behaviour of the E_F distribution inside the Silicon volume.

Finally, a planar gate SJ transistor has been simulated to corroborate that the difference in V_{bd} values comes from the trench gate architecture. The structure presented on Fig.3.35-(a) has been simulated with the SDE editor, adding two high doped pillars (P and N-type), a P_{body} layer where the channel is formed, and a shallow N^+ diffusion to implement the source of the MOSFET. The architecture and the doses of the simulated device are extracted from a reference CoolMOS™ article[3]. The V_{bd} value of the simulated planar gate structure for different CB conditions when V_{gs} is swept from 0 to -10 is plotted in Fig.3.35-(b). The V_{bd} value does not depend on the V_{gs} value even when the devices are N_{rich} (since the curves are overlapped).

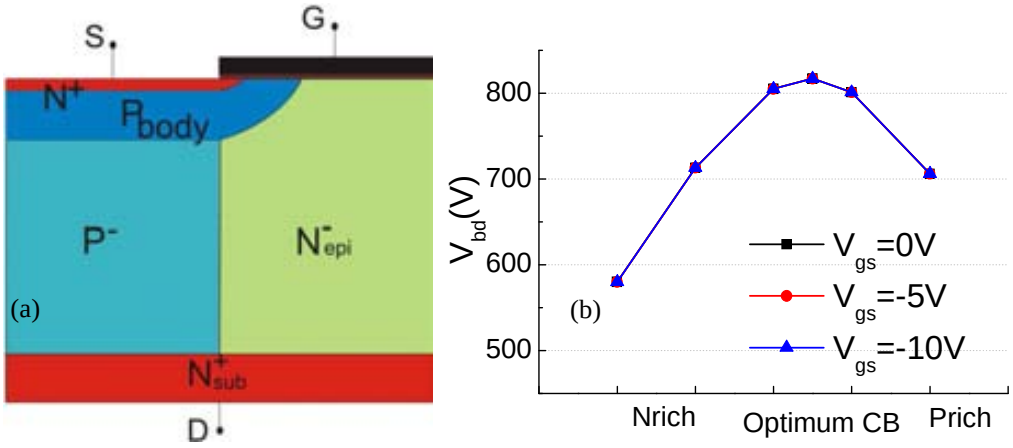

Fig.3.35. (a) Cross-section of the simulated SJ MOSFET with planar gate. (b) Simulated V_{bd} values for different CB conditions when the V_{gs} is negatively swept in a planar gate MOSFET.

It is worth to mention that although the V_{bd} variation effect has been studied, there is no concern on the SJ MOSFET behaviour in real applications since V_{gs} is always set from 10 V to 0 V, with the eventual negative gate voltage values coming from switching transients, as observed in the V_{gs} curve provided in Fig.3.31-(b). As a conclusion, the experimental V_{bd} values at different V_{gs} conditions are a simple and direct way to know which is the CB condition of fabricated trench gate SJ MOSFET transistors, although measurements on other fabricated SJ MOSFETs should be done to corroborate this statement.

3.3.2. Depletion behaviour and C_{ds}-V_{ds} / C_{gd}-V_{ds} curves

The depletion behaviour of the UltiMOS structure has been analysed from TCAD simulations for three different CB conditions: P_{rich}, N_{rich} and Optimum CB. Two main junctions are depleted when a positive drain bias is applied: P_{body}/N_{link} (J1) and P-N pillar (J2) (see Fig.3.36). On the same figure, *d1* and *l1* corresponds to the depletion width and the extension of the depletion, respectively, of junction J1 when the device is in the off-state[20]. On the other hand, *d2* and *l2* correspond to the same parameters for junction J2. The total C_{ds} capacitance can be seen as the addition of the J1 and J2 junction capacitances. Each junction capacitance value can be deduced from Eq.1 with the suitable *l* and *d* values. In the same way, C_{gd} is the capacitance seen from the gate when the drain is positively biased. Thus, the total capacitance depends on the potential lines crowding at the gate bottom-side.

$$C = \varepsilon_s \frac{l}{d} \qquad \text{(Eq.1)}$$

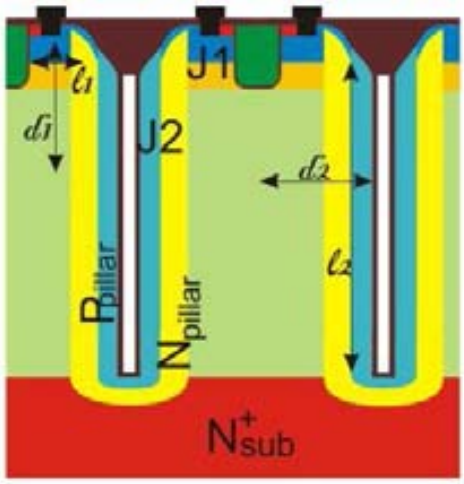

Fig.3.36. Cross section of a half cell indicating the main junctions and distances.

C_{gd} and C_{ds} exhibit an initial decrease at low applied drain bias[21] (< 15 V), as shown in the simulated C_{ds}-V_{ds} (left) and C_{gd}-V_{ds} (right) curves plotted on Fig. 3.37. For the Optimum CB case, the C_{ds}-V_{ds} curve exhibits a minimum before reaching V_{ds}=10 V and the drain voltage at which the C_{ds} suddenly drops is higher than that of the N_{rich} and P_{rich} counterparts. This effect is not visible for C_{gs} since it only depends on the top layers of the structure, not varying with the CB. The value where the C_{ds} slope is maximal is referred as V_{pinch} and it is calculated by the maximum value on the $(dC_{ds}/dV)*C_{ds}$ curve (see Fig. 3. 38)[22]. The C_{ds} drop is basically due to the expansion of the vertical and horizontal depletion regions into the N^-_{epi} layer, as a consequence of the high doped regions. Nevertheless, the expansion of the depletion region into the N^-_{epi} layer depends on the CB between the pillars, as reported later in this section. The N_{rich} device exhibits a drop of the C_{ds} at a lower V_{ds} value since the fast depletion of the P-type pillar makes the depletion region reach the oxide faster. The C_{gd}-V_{ds} curve decreases further as the device goes towards a positive CB value (P_{rich}). Notice that this drop is in excess of 5 decades for the P_{rich} case.

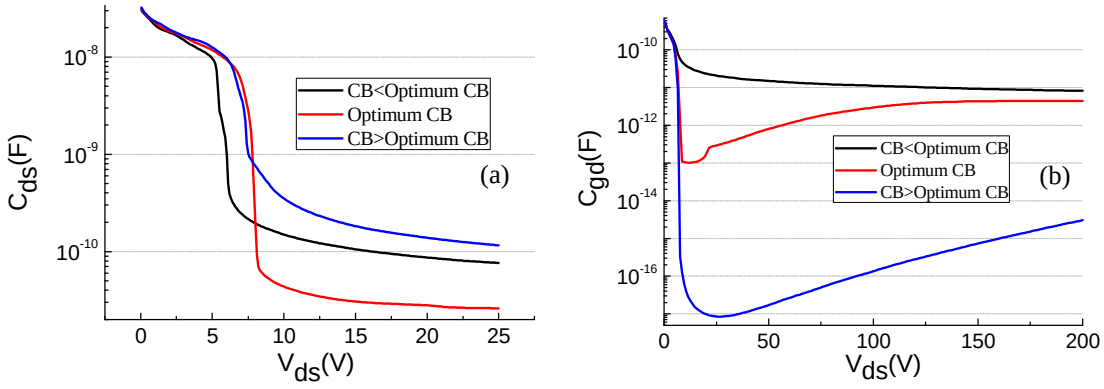

Fig. 3.37. Simulated (a) C_{ds}-V_{ds} and (b) C_{gd}-V_{ds} curves for different CB conditions.

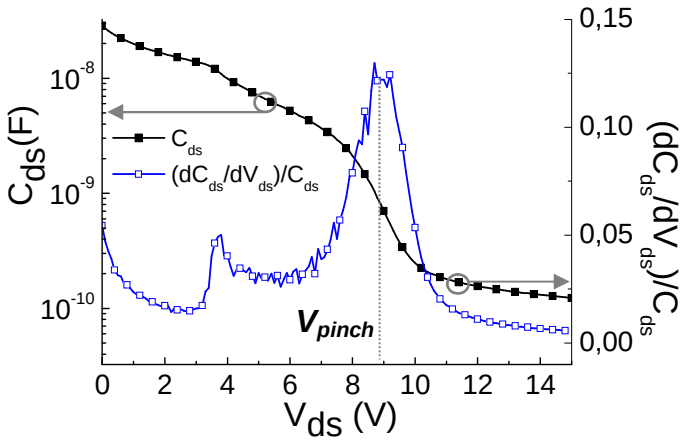

Fig. 3. 38: Extraction of V_{pinch} from an experimental C_{ds}-V_{ds} curve. In this case V_{pinch}=8.8 V.

TCAD simulations are performed according to the defined splits for fabrication tests on UltiMOS transistors, and the simulation results are compared with the experimental electrical performance to ensure accurate simulation results. Fig.3.39 shows the comparison between experimental and simulated C_{ds}-V_{ds} (a) and C_{gd}-V_{ds} (b) curves for different CB conditions. It can be observed that the experimental curve shape is very well replicated by the simulated one. It can be assessed that the measured device has a CB between 0 and 10% (thus, slightly P_{rich}) since the measured C_{gd}-V_{ds} curve fits in the middle of the other two curves.

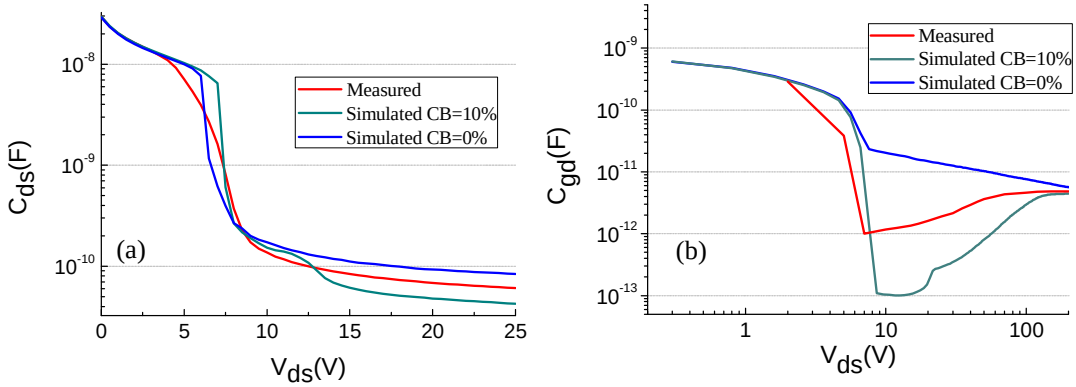

Fig.3.39. Comparison between experimental and simulated (a) C_{ds}-V_{ds} and (b) C_{gd}-V_{ds} curves. The x axes on (b) is in log scale.

Simulations on the same planar gate SJ MOSFET presented in Fig.3.35 have been performed to prove that the C_{gd} value increase is not depending on the gate architecture (trench or planar). The C_{gd}-V_{ds} curve is anyway depending on the CB condition, decreasing the C_{gd} drop as increasing the P_{conc}, as shown in Fig.3.40. The C_{gd}-V_{ds} curve (equivalent to C_{rr}) has been checked on the datasheet of a device with a planar gate (see Fig.3.41 captured from IPx60R190C6 part from CoolMOS^{TM}), and there is a slightly increase of C_{rss} with the V_{ds} value, what means that the selected device is P_{rich}.

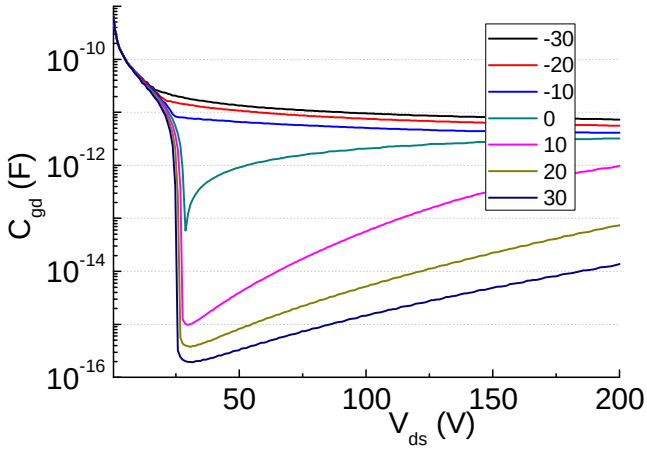

Fig.3.40. Simulated C_{gd}-V_{ds} curves for different CB conditions in a planar gate SJ MOSFET.

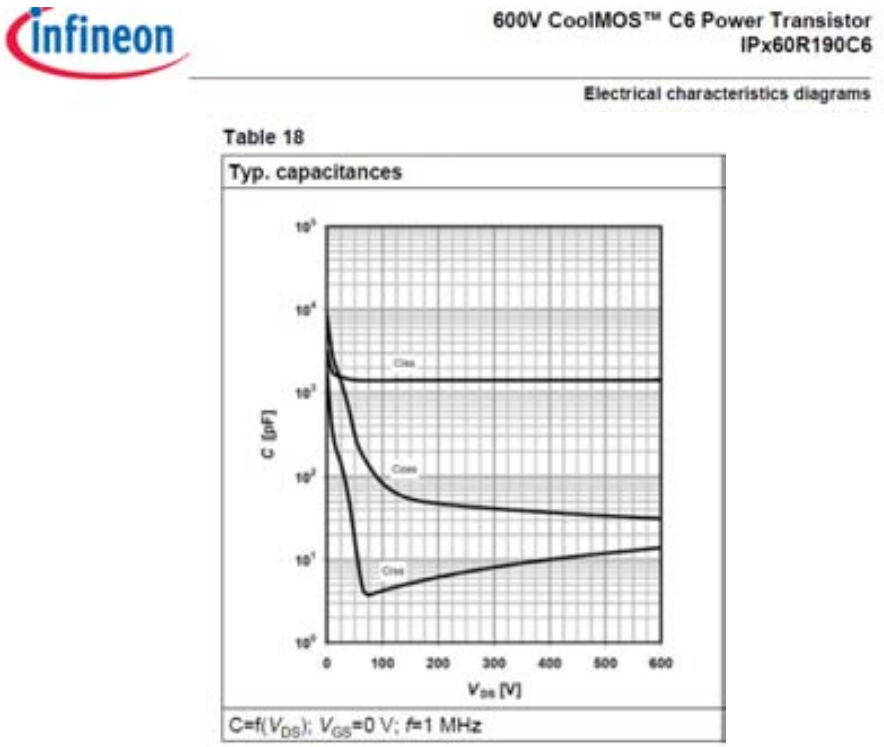

Fig.3.41. Capacitance values for the CoolMOS ™ C6. Adapted from the IPx60R190C6 datasheet.

Depletion behaviour

The snapshots presented in this section have been obtained from the capacitive simulations at the V_{ds} values where both C_{ds} and C_{gd} suddenly drop (between 0 and 20 V). The white lines in the captured snapshots delimit the extension of the depletion region of the main junctions. Snapshots of the potential distribution as a function of the drain voltage are also plotted to full understand the C_{gd} capacitive behaviour for different CB condition. It is easier to understand the depletion process with the help of Eq.1 and the capacitive curves analysis, shown on Fig. 3.37. From Fig.3.43, Fig.3.44 and Fig.3.45 one can observe that *l* reaches the maximum value from the very beginning for both J1 and J2 junctions. Therefore, the drop on the capacitive curves depends on the *d1* and *d2* increase. Once the top of the N-type pillar and the N_{link} diffusion are already depleted, the N^-_{epi} region becomes depleted due to the P-type pillar and the P_{body} donor compensation. At high drain voltage values (100 V) the C_{ds} value is the same for all the CB conditions since the structure is completely depleted for all of them.

C_{ds}

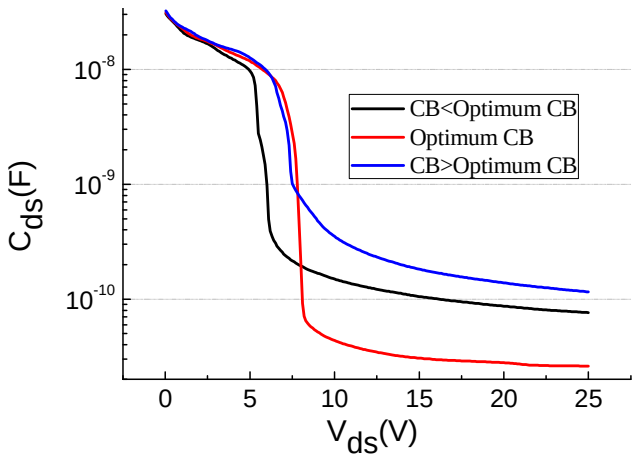

Fig.3.42. Simulated C_{ds}-V_{ds} curves for different CB conditions.

The expansion of the depletion process of both P and N-type pillars for the **Optimum CB case** is completely symmetrical, as inferred from Fig.3.43. The fully depletion of the N-type pillar at the region close to the N_{link} diffusion can be observed when the drain bias reaches the 5-6 V range and both depletion regions merge (see top of the structure in Fig.3.43). If the drain voltage is further increased, the depletion region reaches the trench oxide in the right edge of the plotted structure. At that voltage, the drop in the capacitive curves starts. Once the depletion reaches the N^-_{epi} region, the depleted area is accelerated as a consequence of the low N^-_{epi} doping concentration. The *d* value in J1 and J2 is already maximal at 25 V, leading to the minimum possible C_{ds} value.

When the device is $\mathbf{P_{rich}}$, the depleted region does not reach the trench oxide until a high drain voltage value is applied since more donors are needed to compensate

the total charge of the P column. It can be envisaged from the snapshots of Fig.3.44 that the N_{link} diffusion and the N column are depleted as the drain potential increases and the N^-_{epi} layer becomes completely depleted before the extension of the depletion region reaches the trench oxide. As a consequence, the C_{ds} drop is not so sharp since the lateral depletion through the P column is not completed, thus the *d* value is not maximal.

As in the previous cases, for **N_{rich} devices** the P_{body} region helps to deplete the N_{link} diffusion which becomes fully depleted before the N-type pillar starts depleting, and that is when the vertical depletion between P_{body} and N^-_{epi} also starts. The merging of the vertical and lateral depletion regions as deducted from Fig.3.46. At that voltage, with also the depletion getting to the trench oxide, the drop in the C_{ds} is present, since the maximal *d* can be taken into account in the top region of the N_{pillar}.

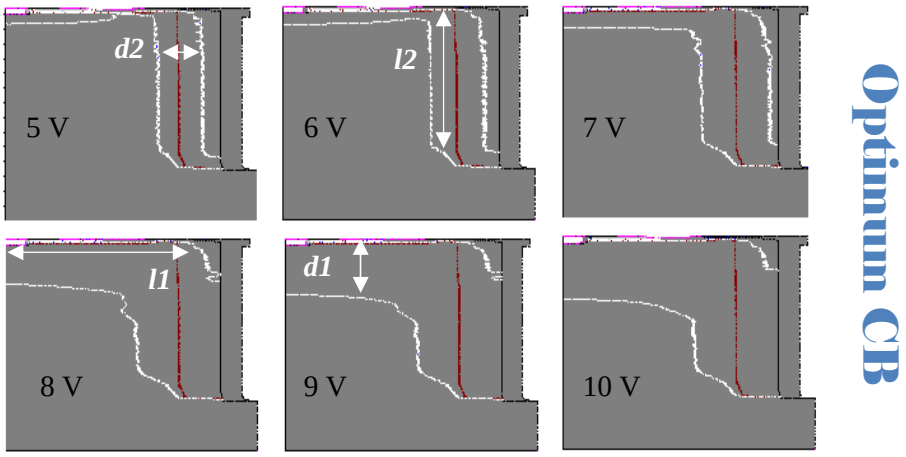

Fig.3.43. Depletion in an Optimum CB SJ Trench structure. X and Y are not drawn to scale.

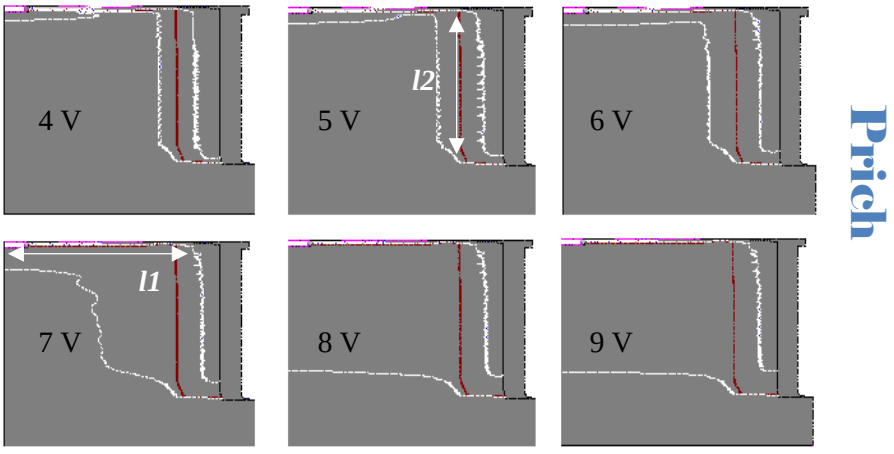

Fig.3.44. Depletion in a P_{rich} SJ Trench structure. X and Y are not drawn to scale.

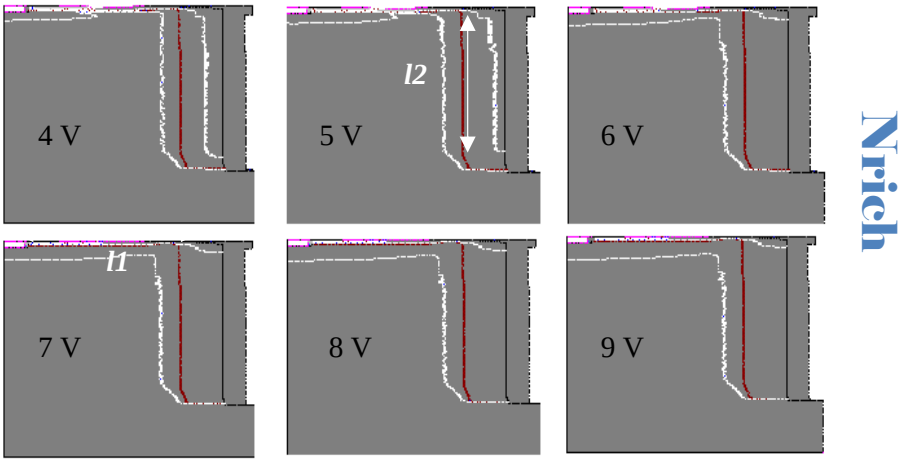

Fig.3.45. Depletion in an N_{rich} SJ Trench. X and Y are not drawn to scale.

Fig.3.46. Depletion zoom in the gate region in an N_{rich} SJ Trench structure. X and Y are not drawn to scale.

C_{gd}

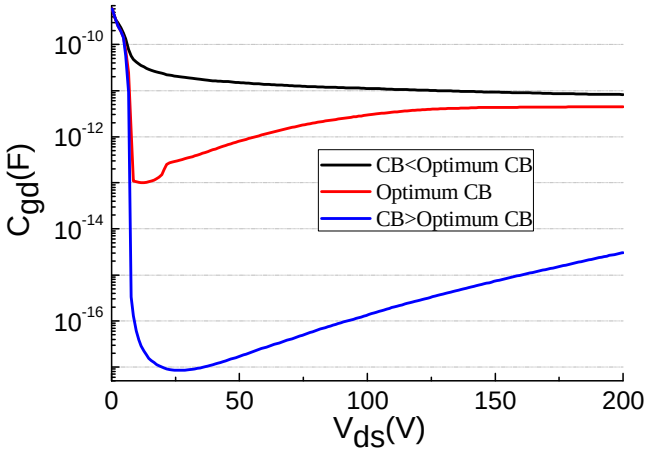

Fig.3.47. Simulated C_{gd}-V_{ds} curves for different CB conditions.

The potential distribution in the UltiMOS structure has to be taken into account to study the evolution of the C_{gd}-V_{ds} curves. Since different CB condition leads to a very different shape of the C_{gd}-V_{ds} curves, the snapshots of the potential distribution for N_{rich} and P_{rich} devices are plotted in Fig.3.48-Fig.3.49. The bottom region of the UltiMOS structure is also plotted due to variations on the potential distribution with the applied drain bias on that region, for the P_{rich} case. On the other hand, the bottom of the N_{rich} devices is not plotted since no difference on behaviour was found. The region under the gate is rapidly depleted at low drain bias, leading to the potential lines spacing.

The first decrease of the C_{gd} curve is due to the fast depletion on the gate region. This effect is exactly the same for both N_{rich} and P_{rich} CB conditions (see capture at 6 V in Fig.3.48-Fig.3.49). When the device is N_{rich}, the potential lines are crowded at the bottom of the trench gate with increasing the voltage (40-70 V). Therefore, the C_{gd} value does not exhibit a huge decrease (just 1 decade), even at very high V_{ds} values, due to the crowding of the potential lines close to the gate[5]. In the case of P_{rich} devices, the potential lines crowd at the bottom of the structure when the V_{ds} is increased. The C_{gd}-V_{ds} value drops enormously at low drain voltages (0-10 V) since no crowding of the potential lines is present close to the gate trench. However, at the 30-40 V range, the crowding of the potential lines at the bottom of the structure starts to increase from the bottom to the top, leading to an increase of the C_{gd} value. See that the P-type pillar is still being depleted at that voltage range. Normally, at very high voltages (600 V), the C_{gd} would be the same for all the CB conditions.

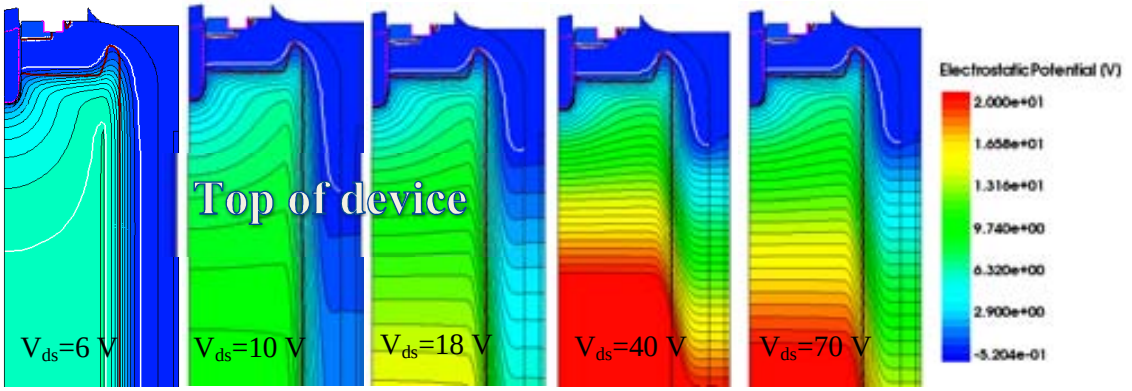

Fig.3.48. Potential distribution in an N_{rich} SJ Trench structure at increasing V_{ds}. X and Y are not drawn to scale.

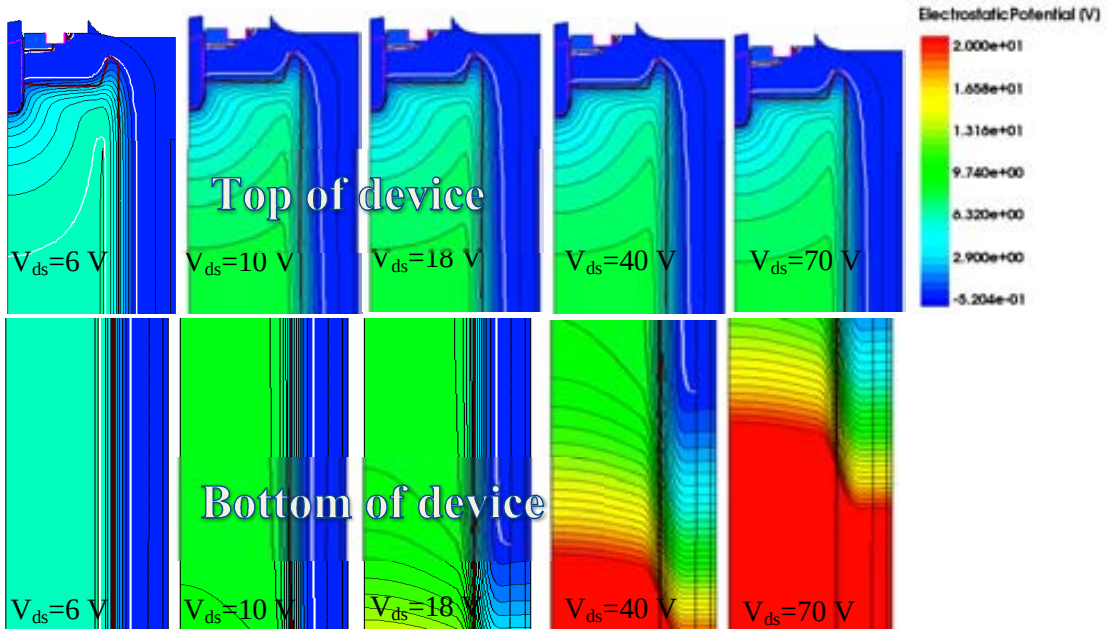

Fig.3.49. Potential distribution in a P_{rich} SJ Trench structure at increasing V_{ds}. X and Y are not drawn to scale.

Capacitance dependence on different parameters

The C_{ds}-V_{ds} simulated curves for different N_{conc} at CB=10% are plotted in Fig.3.50. The capacitance curve shifts to the right when increasing the N_{conc}, since more potential is needed to deplete the same area in comparison with the lower N_{conc} case. The shape of all curves is the same since the P_{dose} is also proportionally increased (same CB for all of them). The experimental and simulated V_{pinch} values as a function of the N_{conc} are also plotted in Fig.3.50. The mismatch between simulated and measured V_{pinch} values, depending on the N_{conc}, is a direct consequence of the lower N_{conc} obtained in the fabricated transistors. Nevertheless, the V_{pinch} value increases with the N_{conc} and, since V_{bd} increases when decreasing the N_{conc} (see Fig.3.16), a trade-off between N_{conc} and V_{bd} has to be set, taking into account that a low N_{conc} leads to a high sR_{on} value. The CB is set to 10% instead of 0%, since not just the pillars but the N^-_{epi} region have to be also depleted, thus more P is needed to contribute in the counter doping.

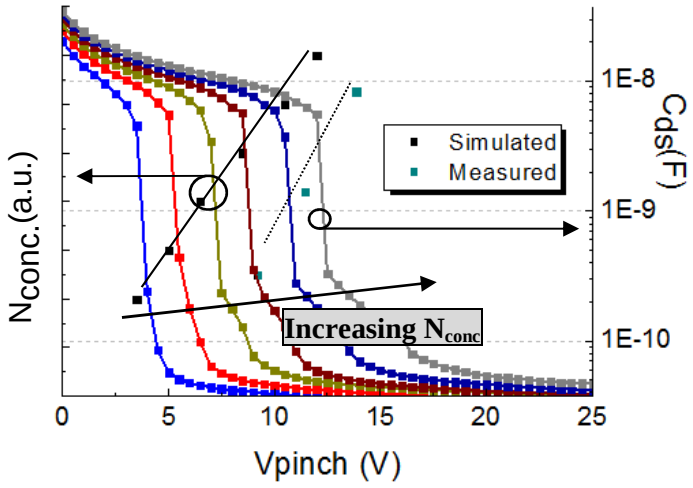

Fig.3.50. Simulated C_{ds}-V_{ds} curves for different N_{conc} (being N_{conc}1 the lower level and N_{conc}6 the higher). The squares correspond to V_{pinch} simulated and measured values for different N_{conc} level (left axis).

The relation between V_{pinch} and V_{bd} is shown in Fig.3.51-(a), where the performed measurements on transistors fabricated with different N_{conc} and CB values are plotted. From this graph it can be concluded that the low V_{pinch} values lead to high voltage capability. The evolution of C_{ds}@25 V, V_{pinch} and V_{bd} (scaled as V_{bd}/50) over a whole row in a wafer of UltiMOS transistors is plotted in Fig.3.51-(b). The wafer was processed to do not have a uniform CB in the entire surface, corroborating that C_{ds}@25 V is minimal when V_{bd} is maximal. It can also be inferred that V_{pinch} is following the C_{ds} curve since the minimal V_{pinch} corresponds to the maximal V_{bd}.

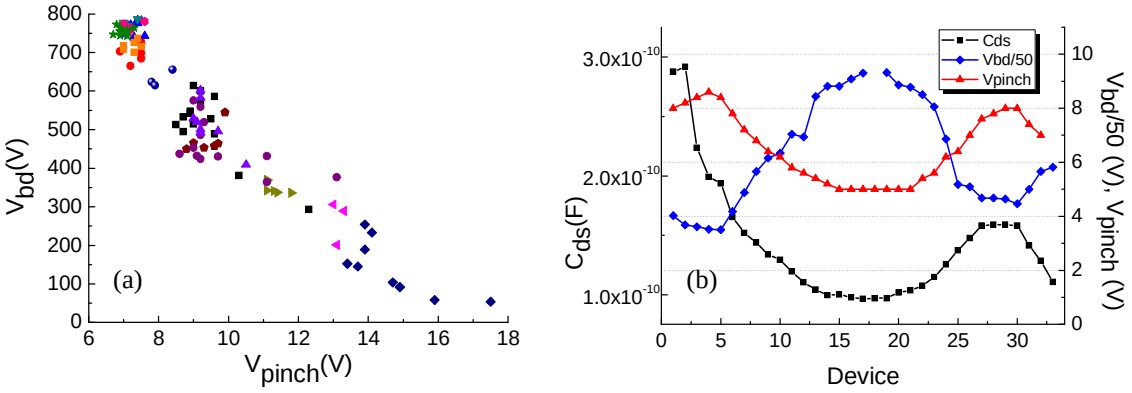

Fig.3.51. (a) Experimental V_{bd} -V_{pinch} trade-off for UltiMOS transistors in the central row of processed wafers with different N_{conc}. (b) V_{bd}/50, V_{pinch} and C_{ds}@25V for UltiMOS transistors in the central row of a wafer (right).

3.4. UltiMOS transistor performance

On this section, a comparison between experimental results obtained with the most common test techniques for SJ power MOSFETs (ME/MI, Trench fill and UltiMOS) is provided. It is discussed why the electrical performance is not the same for all the SJ power MOSFET architectures. The section is divided in two parts: study of the conduction and switching losses and robustness measured under the UIS and Reverse Recovery tests.

3.4.1. Conduction and Switching Losses

- **Conduction losses**

The V_{bd}-R_{on} FOM for power transistors implemented with the different technologies described in Chapter 2, including the UltiMOS transistor are plotted in Fig.3.53 , where transistors rated at a current range of 16 to 23 A are included, with the corresponding range of R_{on} values due to the different active area. The R_{on} of the UltiMOS transistor exhibits the lowest R_{on} value since the cell pitch is not limited by the process technology and a thin high doped N-type pillar can be implemented. The Infineon transistor with R_{on} =0.165 Ω is rated to 23 A. However, the R_{on} value would be in the range of 0.2 Ω for a device rated at 20 A. On the other hand, the ST device is rated at 20 A, with a R_{on} value of 0.13 Ω, very close to the UltiMOS transistor since the trench fill technique is used to implement the SJ MOSFET.

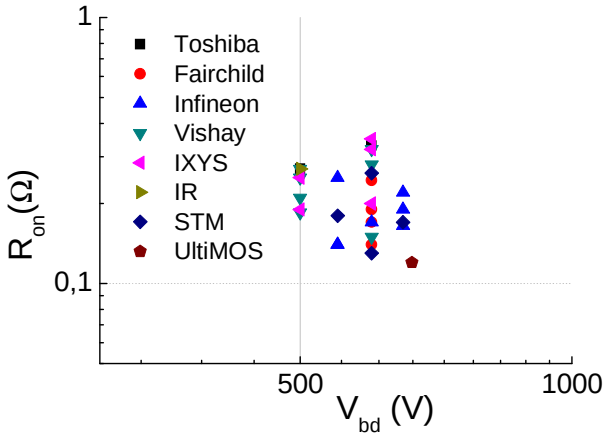

Fig.3.52. V_{bd}-R_{on} FOM for commercial SJ power MOSFETs. Adapted from the commercial datasheet.

- **Switching losses**

As introduced, the Q_g and Q_{gd} (gate-drain charge) relevant parameters when designing power MOSFETs for high frequency (f >1 MHz) applications[23]. A low gate charge value improves the switching performance but degrades the di/dt control at turn-off (see *reverse recovery*)[23]. The simulated V_{gs}-Q_g curve for an UltiMOS transistor at I_d=9.5 A and V_{ds}=480 V is plotted in Fig. 3.53-(a). The Q_{gd} corresponds to C_{rss}, which depends on the applied V_{ds} value and has a direct impact on the switching characteristics. Due to the fast depletion of the UltiMOS transistor, the C_{rss} curve exhibits a drop at a drain voltage in the range of 10 V (see Fig. 3.53-(b)). On the other hand, the C_{oss} is also required to be minimal since the energy stored in the output capacitance is dissipated in the device every turn-on process.

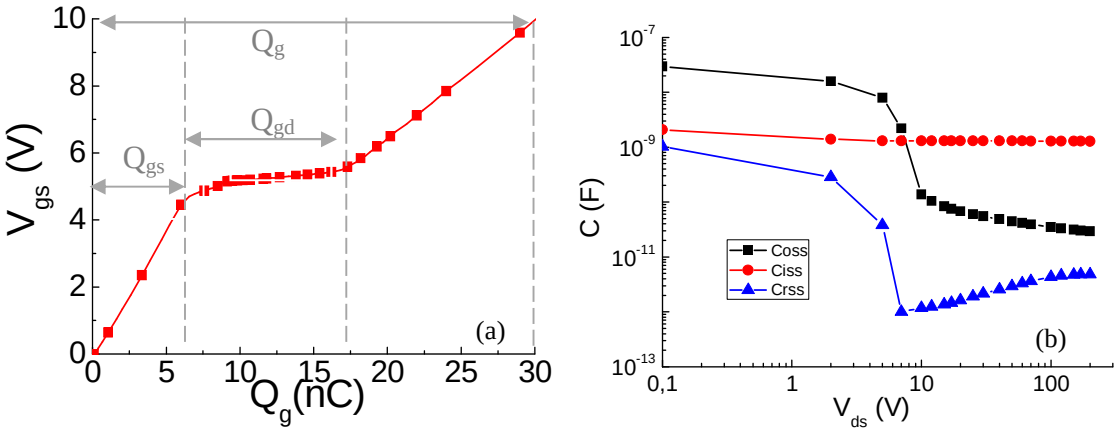

Fig. 3.53. (a) Simulated V_{gs}-Q_g for an UltiMOS transistor with I_d = 9.5 A, T^a= 25 ºC and V_{ds}=480V (right). (b) Typical experimental behaviour of UltiMOS capacitances.

The Q_g evolution with V_{ds} for the UltiMOS, the ME/MI and the Trench filled SJ MOSFETs is plotted on Fig.3.54-(a). The curves corresponding to the Trench fill and UltiMOS are similar due to the gate trench architecture. On the other hand, the ME/MI

counterpart has a planar gate[3], resulting in a higher Q_{gd} value. The comparison of the C_{rss} curves for the UltiMOS and the Trench fill SJ MOSFET is plotted in Fig.3.54-(b). Notice that the capacitance decreases at lower drain voltage in the UltiMOS case. This is basically due to the use of a low doping concentration of the N^-_{epi} layer and the presence of the oxide inside the SJ trenches, which allows a fast depletion of the device active area. Conversely, the Trench fill SJ MOSFET needs a higher doping concentration (higher than the N^-_{epi} layer concentration) in the N-type pillar to get a low R_{on}, leading to slower device depletion and higher capacitive values, as inferred from the Toshiba values reported in Table 2.2.

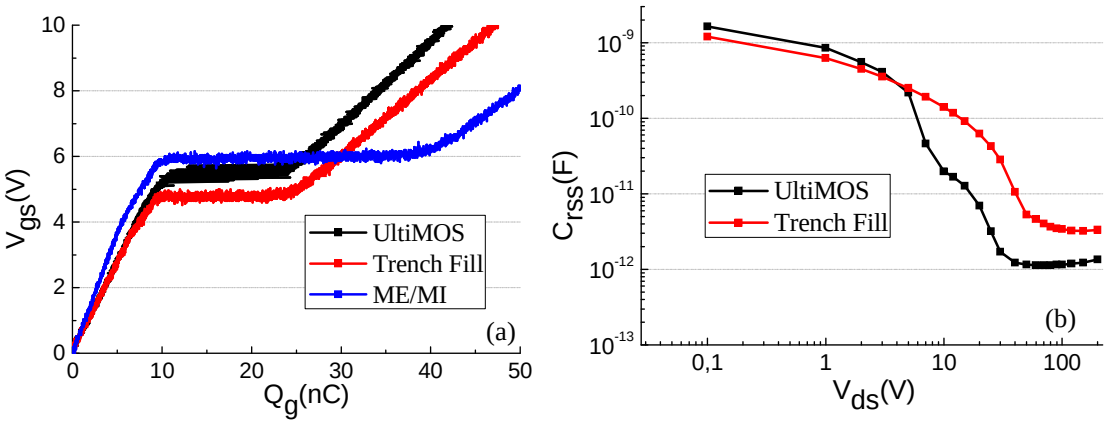

Fig.3.54. (a) Q_g evolution for the three SJ MOSFET architectures with I_d = 9.5 A, T^a= 25 ºC and V_{ds}=480V. (b) C_{rss} evolution for UltiMOS and Trench filled SJ MOSFETs.

Parameters	On Semiconductor (*UltiMOS*)
R_{on} (Ω)	0.12
Q_g (nC)	41
Q_{gs} (nC)	9.4
Q_{gd} (nC)	14
$R_{on}\cdot Q_g$ (mΩnC)	4920
C_{iss} (pF)	1860-1949
C_{oss} (pF)	247-358
C_{rss} (pF)	1.9-3.4

Table.3.1. Capacitive and charge values for UltiMOS, where the capacitances are measured at 25 V and the charge at 480 V. For the values of commercial SJ MOSFETs refer to Table.2.2.

It can be concluded that the smaller the $R_{on}\cdot Q_g$ or $R_{on}\cdot Q_{gd}$ FOM, the better the switching performance since the total losses will be lower. From the $R_{on}\cdot Q_g$ FOM point of view, the Toshiba transistor is the best (see Fig.3.56), with a similar performance than the UltiMOS counterpart. The $R_{on}\cdot(E_{on}+E_{off})$ FOM, where E_{on} and E_{off} are the energy dissipated during the turn-on and the turn-off process, respectively, is a useful to determine the switching performance of a given power transistor. The measured E_{on} and

E_{off} values at different switching frequencies for UltiMOS transistors are plotted in Fig.3.57. Measures are performed at 300 V (as detailed in appendix B) and compared with other commercial SJ MOSFETs (being UltiMOS=XCB, Fairchild=FCP, Infineon=IPA and STMicroelectronics= STF). It can be observed that he lowest E_{on} and E_{off} values are reached in the UltiMOS case, in accordance with the excellent performance of the UltiMOS transistor presented in Fig.3.56. A similar switching behaviour can be achieved by the Toshiba counterpart (but no data is available).

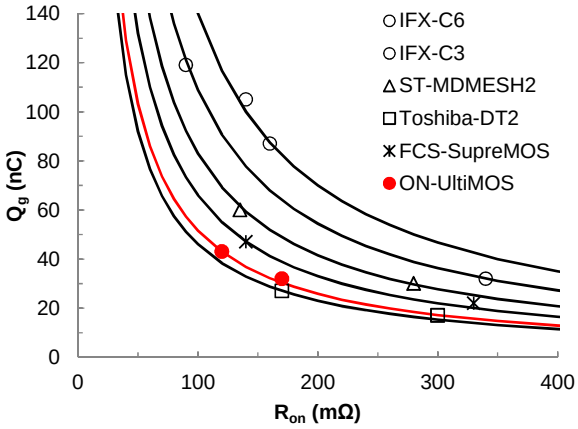

Fig. 3. 55: Q_g-R_{on} FOM for the UltiMOS transistor and different commercial SJ MOSFET.

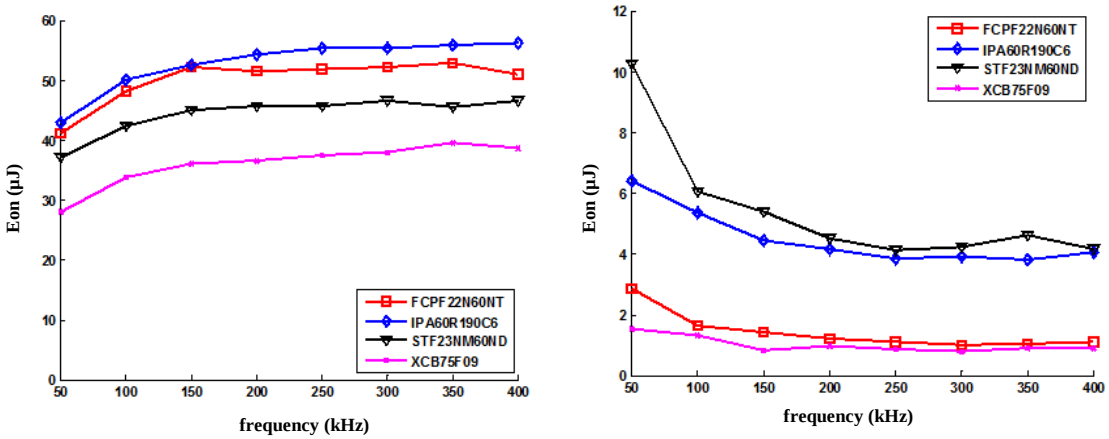

Fig. 3. 56: (a) E_{on} and (b) E_{off} evolution with the frequency at 300 V, when I_{ds}=4 A, V_{gs}=12 V and R_g=10 Ω. Courtesy of KUL.

3.4.2. Robustness

Different destructive mechanisms can be found in real operating conditions, when the power MOSFET is driven to the limits of its safe operating area: thermal breakdown, dynamic avalanche, overvoltage and the parasitic bipolar activation[24]. The thermal breakdown happens when the device temperature is high enough to dramatically increase the n_i (intrinsic carrier density) value. The intrinsic temperature (T_{in}) is defined as the value where n_i equals the background doping of the N^-_{epi} layer (N_D in Fig.3.57) and its dependence on the N_D value is plotted in Fig.3.57. Assuming that the

V_{bd} value increases with the temperature, the region where the avalanche takes place will move to the coolest part of the power transistor. Afterwards, when the T_{in} is reached, the current filamentation and the subsequent device thermal destruction will occur provided a cooling mechanism is implemented[24]. On the other hand, the avalanche destruction (overvoltage) concerns the failures when a spike voltage due to stray inductance or the current from a load in switching operation exceeds the drain rated voltage[25]. A robust power MOSFET with high avalanche capability needs the breakdown to occur in the Silicon volume [26]. Another condition to avoid these failures is that negative differential resistance (NDR) branches have to be avoided[26].

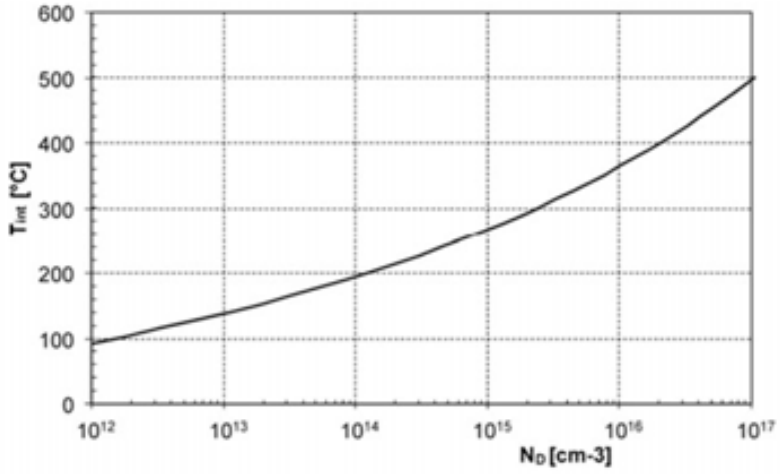

Fig. 3. 57: Evolution of T_{in} versus background doping concentration. Adapted from[26].

Two robustness tests are usually aplied to power MOSFETS: reverse recovery and UIS. The first is used to determine if a device can handle a fast switching under extreme conditions and it is described with T_{rr} (time that the device needs to recover from the current peak) and the Q_{rr} (charge to be removed before switching the device on again). Te reverse recovery is performed to ensure a good performance when a transient event takes place. The UIS test quantifies the energy that the device can handle. The results of both tests are normally detailed in the first page of the datasheet of a power MOSFET, hinting on their importance.

- **Reverse recovery**

The *I(t)* curve for a Reverse Recovery test performed in an UltiMOS transistor is plotted in Fig.3.59-(a) (test conditions detailed in Appendix B),where the *t1* and *t2* correspond to the fall time and the rise time, respectively. The total time (*t1+t2*) is known T_{rr}[9]. The I_{RRM} is the peak reverse current to be handled by the transistor during a reverse recovery test. The waveforms of the reverse recovery process for UltiMOS, ME/MI and Trench filled SJ MOSFETs are plotted in Fig.3.59-(b). The UltiMOS transistor exhibits the lower I_{RRM} value and the shortest *t1* time in comparison with the other SJ MOSFET counterparts. However, the UltiMOS *t2* time is slightly higher than

the Trench fill SJ MOSFET due to the low N^-_{epi} concentration. Anyway, the ME/MI technology leads to a high T_{rr} value (545 ns) in comparison with the T_{rr} values obtained for the trench fill SJ MOSFET (380 ns) and UltiMOS transistor (378 ns). Note that the Q_{rr} is lower in the UltiMOS, again due to the N^-_{epi} concentration (see Table.3.2 for the exact values). Normally, a steeper *di/dt* is not desired since it implies hard switching. The introduction of an N-type buffer layer can be used to have softer recovery characteristics. [27]. However, this leads to a slower switching performance with an increased *t2*.

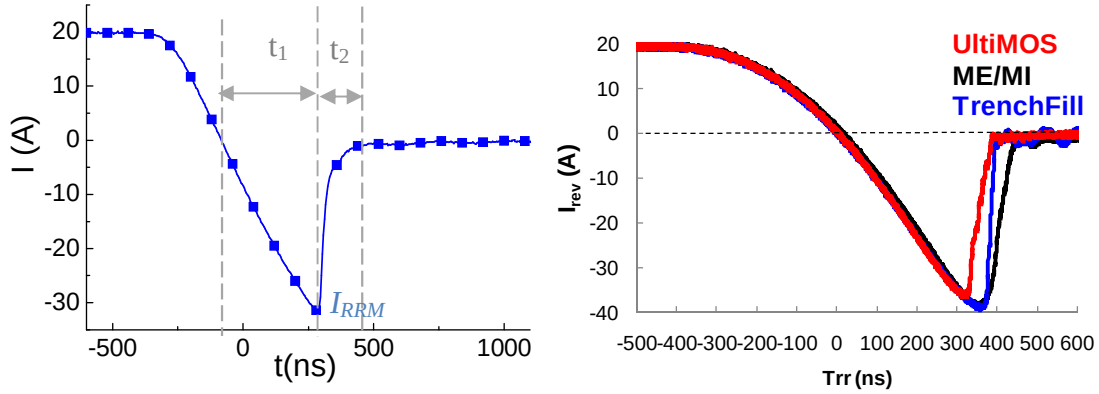

Fig.3.58. Measured reverse recovery for (a) UltiMOS and (b) for three different techniques, at I_d=20A, di/dt=100 A/µs and V_{ds} =480 V.

	On Semiconductor (*UltiMOS*)
T_{rr} (ns)	378
Q_{rr} (µC)	3.6
I_{RRM} (A)	35.7

Table.3.2. T_{rr}, Q_{rr} and I_{RRM} for UltiMOS. For the values of commercial SJ MOSFETs refer to Table.2.4.

- ## Unclamped Inductive Switching

The UIS test consists on the discharge of the energy stored in an inductor directly on the power transistor in the off-state. An typical *I-V* curve during an UIS test for an UltiMOS transistor is plotted in Fig.3.59. Notice that when the discharge of the inductor through the internal diode starts (current starts to decrease), the voltage increases up to a value even higher than the V_{bd} value due to self-heating effects[7], while the current is still high. At that moment, the power dissipated through the device can be in the range of 6-7 kW (depends on the UIS circuit set-up). With such high power values, if the current is not properly distributed in the whole area of the device, a thermal destruction will occur. It is worth to say that, due to the low doped N^-_{epi} layer[26], T_{in} is in the range of 200ºC for an UltiMOS transistor.

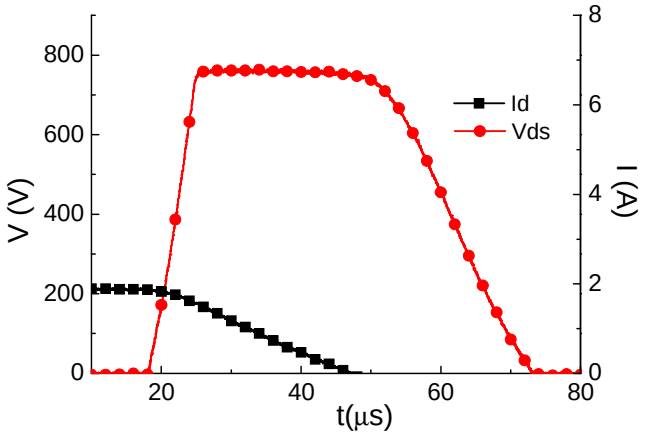

Fig.3.59. Measured UIS *I-V* curves for an UltiMOS transistor, with I_d=2 A, L=10mH and V_{dd}=50 V.

The results of the UIS test performed on the first UltiMOS transistors at wafer level with different CB conditions are plotted in Fig.3.60. The spread on the CB conditions is needed to ensure a good robustness for a wide enough CB window. The plotted V_{bd} and E_{AS} values are average data for 150 devices per wafer. The voltage capability obtained in the first UltiMOS layout was 550 V, with a maximum at 570 V for the optimum CB value. However, to get into the target, the V_{bd} value needs to be higher than 650 V. The energy capability was in the range of 400-450 mJ for P_{rich} devices, and it decreases to almost zero for Optimum CB and N_{rich} counterparts. Although the UIS test performed on P_{rich} devices exhibited an energy capability upon the minimum required value (350 mJ), it should be further increased to have enough margin to ensure the targeted value in all the fabricated devices. On the other hand, the robustness for the Optimum and N_{rich} CB conditions had to be definitely improved. **Thus, the cause of the low current capability for a quite significant CB range needs to be found and the maximum E_{AS} value must be increased.**

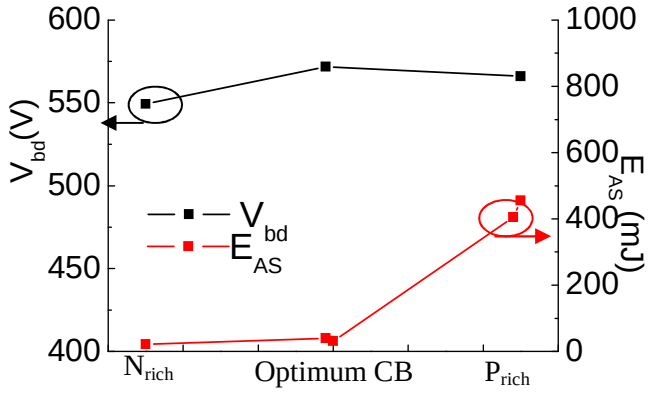

Fig.3.60. Measured V_{bd} and E_{AS} average data for different CB conditions

3.5. References

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CHAPTER 4

Edge Termination study

The edge termination of UltiMOS transistors is studied in detail in this section since failures were located in that region for certain CB condition. It is demonstrated that the avalanche process location and avalanche voltage can be varied with tuning different technological parameters of the implementation process of the transistors. Different measurement techniques and TCAD simulations are used to investigate the cause of failures on the edge termination region. Finally, a more robust termination is optimized for the UltiMOS transistors and the updated electrical performance for the optimized are presented.

4.1. Introduction

The failure spots captured on the first fabricated UltiMOS transistors during the UIS test were all located in the edge termination/periphery regions (see **Fig.4.1-(a)**) where the corner of the GR is blown up due to the heating effect. Therefore, a detailed analysis and optimisation of this region has to be performed to enhance the robustness of the UltiMOS transistor.

A first study to confirm the breakdown location was done using a new P_{ring} dose value (PringDose1), which is lower than the reference PringDose2 value. Different CB conditions are implemented with the PringDose1 and the comparison of the V_{bd} average values is shown in **Fig.4.1-(b)**. The maximum V_{bd} value for the P_{ring}Dose2 transistors is found at a more P_{rich} CB value than for the PringDose1, as indicated with the lines corresponding to the expected trend. These results clearly indicate that although the avalanche starts in the periphery of the device, there is a slight interaction between the implantation dose of the edge termination rings and the CB condition of each UltiMOS transistor[1]. The voltage capability of the edge termination has to be significantly increased to shift the initial avalanche point to the active area, avoiding a premature device failure at the corners of the edge termination. In fact, the active area is larger than the edge termination area, leading to a much higher energy capability when the

device is driven to avalanche. In this sense, the use of a thicker N^-_{epi} layer or an increase of its doping concentration will provide a higher voltage capability of the edge termination region. However, the electrical performance of the active area will change if a different N^-_{epi} layer is used. For instance, a thicker N^-_{epi} would increase the sR_{on} value, as it has been studied in Chapter 3 (see Fig.3.15-(b)). A second option to optimize the edge termination structure is the correct choice of the P_{ring} dose to reach the highest V_{bd} value. This was the selected option since it did not require any change in the active area properties, as detailed in section 4.3.

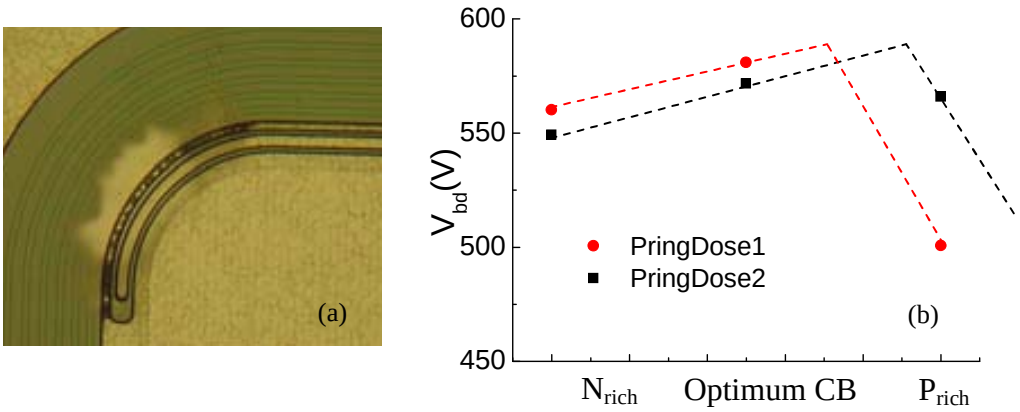

Fig.4.1. (a) Failure spot in the edge termination region. (b) Measured V_{bd} average value for different P_{ring} doses and different CB condition. The expected trend of the V_{bd} is indicated with the dashed lines.

The optimization of the main electrical characteristics of an UltiMOS transistor is difficult to be achieved by correlating experimental data on V_{bd}, sR_{on}, capacitances, etc. since a lot of geometrical and technological parameters are influencing these values. As a consequence, it was decided to implement a simple planar diode without the deep SJ trench to study the edge termination region (see Fig.4.2). Almost all the critical steps used in the standard UltiMOS process technology are not performed. The fabrication process starts with the N^-_{epi} growth and the Termination Module followed by the P_{body} and N_{link} implants. All steps until the Contacts Module are skipped, according to the process flow described in Appendix A. Contact, Metallization and Passivation Modules remain the same.

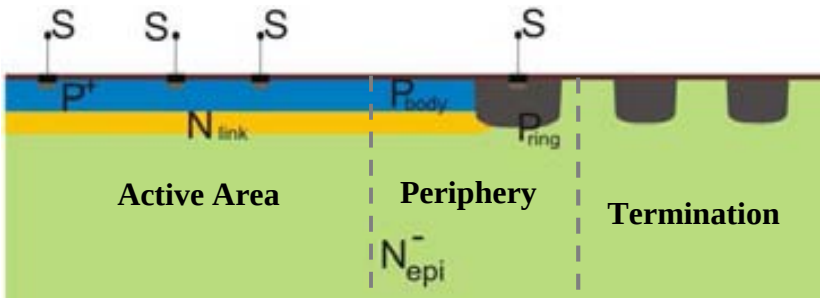

Fig.4.2. Cross section of the last microns of the active area, periphery and edge-termination of a planar diode

The fabricated device has two main regions that can be seen as two PiN diodes connected in parallel: the diode inherent to the periphery/edge termination, surrounding

the active area and formed by the P_{ring}/ N^-_{epi}/N^+_{sub} layers, and the diode of the active area, which is constituted by the $P_{body}/N_{link}/N^-_{epi}/N^+_{sub}$ layers. The avalanche will never start simultaneously in the P_{ring}/N_{epi} and P_{body}/N_{link} junctions since different doping concentration and depths are used to implement the P_{body} and P_{ring} diffusions. The architecture of the two PiN diodes leads to the possibility to force the breakdown to take place in one of two regions: periphery or edge termination. The device cannot break in the active area since the P_{body}/N_{link} junction is completely flat (ideal 1D breakdown) and its V_{bd} value will always be higher than that of the junction curvature at the periphery region. As a consequence, the E_F value in the periphery will always be higher than that of the active area due to the equipotential lines crowding at the junction curvature[2]. Therefore, the avalanche process can start in the corners of the active area (due to the curvature of the P_{body}/N_{link} junction) or in the periphery/edge termination area, depending on the N_{link} value. Small variations can make the avalanche fluctuate from one region to the other.

4.2. Breakdown location: Active area or Edge Termination

Two different N_{link} doses have been considered for this study, being $N_{link}1<N_{link}2$, while all the other parameters are kept constant in the fabricated planar diodes. The simulated *I-V* curves of the two planar diodes with different N_{link} doses are plotted in Fig.4.3-(a) and the E_F snapshots at different current levels for the simulated structures are plotted in Fig.4.4. The simulations are scaled to the area of the corners of the structure since the EMMI images performed on a planar diode show that this is the region where the avalanche starts (see Fig.4.3-(b)). When a low N_{link} value is used ($N_{link}1$), the avalanche process starts in the last ring of the edge termination, but it becomes higher in the GR when the current is increased since the current will flow from ground to the high voltage (drain) through the shortest and less resistive path. On the other hand, when a high N_{link} value is considered ($N_{link}2$), the avalanche process starts in the edge of the active area since the V_{bd} value of the active area (AAV_{bd}) is lower than that of the termination (TV_{bd}) (red curve in Fig.4.3). At a certain current level, the impact ionisation in the active area rises as a consequence of the generated heat. Therefore, the AAV_{bd} value becomes higher than the TV_{bd} one, leading to the shift of the avalanche location from the active area to the periphery, as shown on the E_F snapshots performed at 1.5×10^{-5} A to 5×10^{-3} A. The *I-V* curves for the two N_{link} values merge when the vertical E_F in the GR region dominates, as it can be deduced from the snapshot taken at 1.3 A. However, the NDR branch is differently induced, depending on the N_{link} dose, when the current is further increased. The active area takes the current for the $N_{link}2$ case, whereas for the $N_{link}1$ case the current remains in the periphery, as inferred on the snapshots taken at 5.3 A. As a consequence, the two *I-V* curves are slightly different at high current levels when the NDR is present. It is worth to notice that for the $N_{link}1$ case the electric field at low current is laterally distributed along the whole edge termination

width, but also a vertical electric field is created at the same time in the GR region. On the opposite, when $N_{link}2$ is used, the edge termination has lower electric field values than those of the active area at high current, meaning that the edge termination does not play any role when a high N_{link} is used.

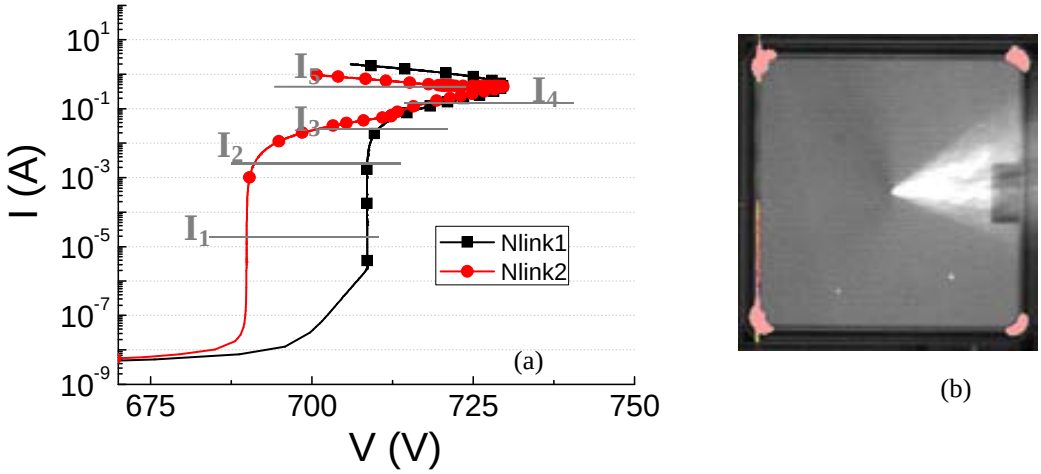

Fig.4.3. (a) Simulated *I-V* curves for different N_{link} dose values in an 8 ring edge termination structure, being $N_{link}1<N_{link}2$. (b) EMMI image taken at I_d=5 mA on a planar diode shows the avalanche at the corners. I_1 to I_5 in the *I-V* curve indicate the current levels at which the snapshots of Fig.4.4 are taken.

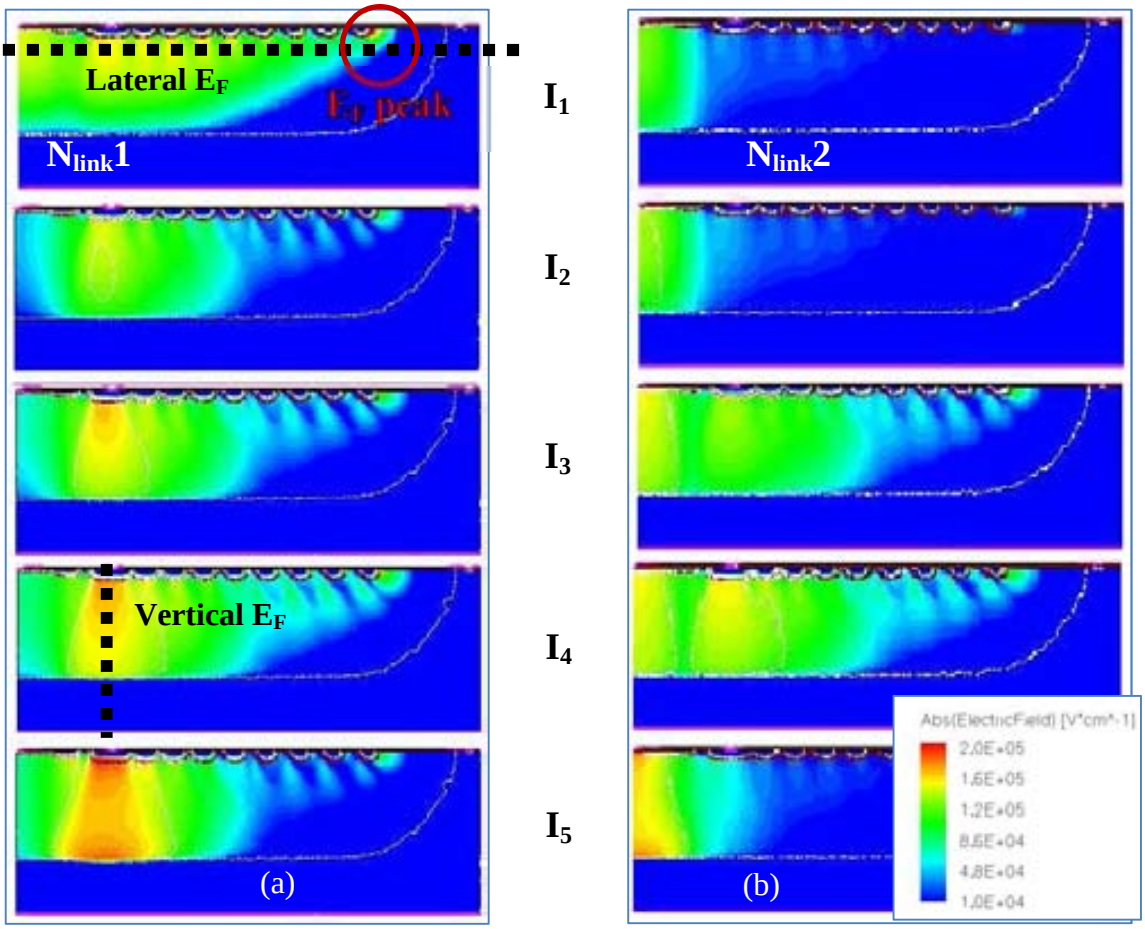

Fig.4.4. E_F snapshots for an 8 ring edge termination structure with (a) $N_{link}1$ and (b) $N_{link}2$, taken at different I_d: 1.5×10^{-5}, 5×10^{-3}, 6.4×10^{-2}, 1.6×10^{-1} and 1.3 A (top to bottom for both N_{link} doses).

EMMI measurements have been performed on fabricated diodes with the 8 ring edge termination to corroborate the dependence of the avalanche location on the N_{link} dose. The EMMI images at different current levels for devices with $AAV_{bd} < TV_{bd}$ ($N_{link}2$) are shown in Fig.4.5. The avalanche process clearly starts in the corner of the active area and the GR takes the current when the AAV_{bd} value becomes higher than the TV_{bd} one. Conversely to the simulation results, the last shift of the current to the active area is not visible since the real device will be destroyed since, at that current level, the NDR branch on the *I-V* characteristic is already present. On the other hand, the low current image for the device implemented with $N_{link}1$ shows the avalanche in the outer part of the last ring of the edge termination while at higher current the maximum avalanche is in the GR (see Fig.4.6). These results are in good agreement with the TCAD simulations.

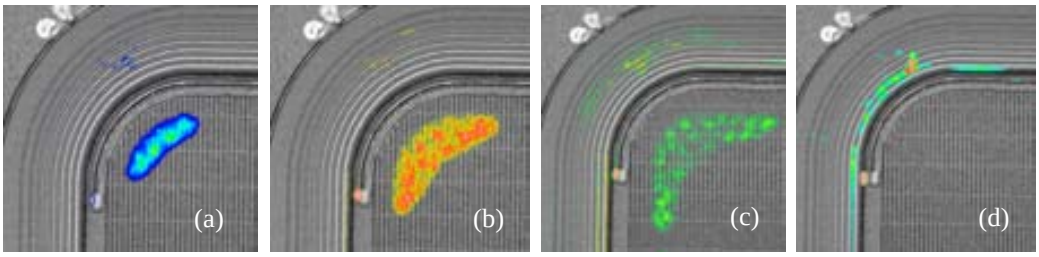

Fig.4.5. EMMI images of an 8 ring edge termination diode with $TV_{bd} > AAV_{bd}$ ($N_{link}2$). The current levels are (a) 8, (b) 18, (c) 24 and (d) 32 mA.

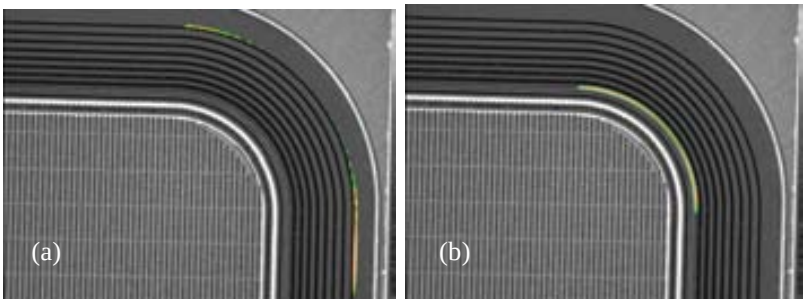

Fig.4.6. EMMI pictures for an 8 ring termination with $TV_{bd} > AAV_{bd}$ ($N_{link}1$), taken at (a) 13 µA and (b) 2 mA.

To find the cause of the failures in the edge termination (see section 4.3), simulations and measurements are performed using $N_{link}1$ dose to be sure that the critical E_F is located out of the active area. One could conclude that using $N_{link}2$ for the final UltiMOS transistor would force the impact ionisation to start in the active area, thus solving the problem. Unfortunately, this is not true since the impact ionisation starts at the edge of the active area, in the curvature of the N_{link}/P_{body} junction and the current is not properly distributed in the active area. Furthermore, the addition of the SJ trenches to the planar diode changes the electric field distribution in the active area[1].

4.3. Failures in the Edge Termination

Once the N_{link} value is already set in the planar diode to ensure the location of the initial avalanche point in the edge termination, the TV_{bd} value has to be increased to enhance the robustness of the final device. It has been reported in the literature that the design of the edge of the active area can influence on the destruction current limit of the PiN diode[3]. Anyhow, the P_{ring} dose has a direct effect on the V_{bd} value and its tuning does not require any layout variation. Thus different wafers of planar diodes were processed with different P_{ring} doses, while all other parameters are kept constant. Fig.4.7 shows the measured and simulated V_{bd} evolution as a function of P_{ring} dose together with the failure rate. The failure rate is an optimum FOM to correlate the robustness of the structure with the current level that the device can handle, which is calculated based on the device failures at 100 µA (during the V_{bd} test). This is a preliminary test at very low current, but the real device needs to handle much higher currents during the required UIS test. In our case, 14 devices identically processed on each P_{ring} split are measured to determine the failure rate. A high failure rate indicates that most of the structures were not able to handle large avalanche current values. The simulated values are plotted on the same graph to be able to validate the behaviour from the reported simulations. A P_{ring} dose in the range of 10 a.u. exhibits a high failure rate but the V_{bd} reaches its maximum at that dose, as expected from the simulated V_{bd} values. Unfortunately, the highest V_{bd} values were not statistically measured since most of the devices had already failed at the current level used to sense the voltage capability.

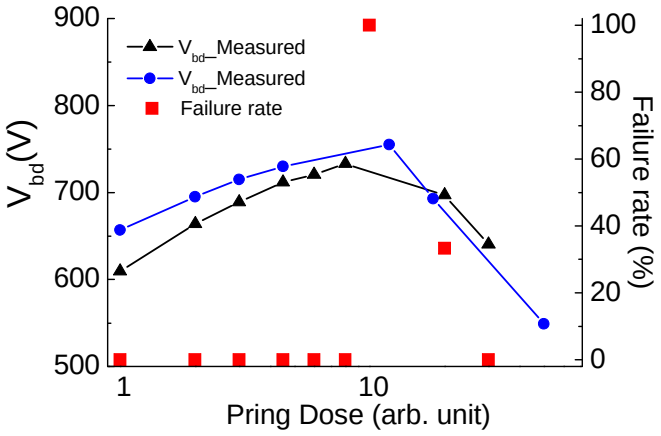

Fig.4.7. Simulated and measured dependence of the V_{bd} value on the P_{ring} dose. Measured values correspond to the V_{bd} average. Failure rate is based on the V_{bd} measurements.

Diode structures with different P_{ring} dose have been simulated to investigate the cause of the high failure rate for certain values. The simulated *I-V* curves for three different P_{ring} dose values are plotted in Fig.4.8, where the corresponding snapback current (I_{snap}) values are pointed with an arrow. Notice that the *I-V* curve with the highest V_{bd} value (optimal P_{ring} dose) corresponds to the lowest I_{snap} value, leading to a

reduction of the diode robustness. However, a non-optimal P_{ring} dose leads to a reduction of the voltage capability but to a much higher I_{snap} value, in correlation with experimental results shown in Fig.4.7. All the *I-V* curves are overlapped after the snapback since the maximum impact ionisation moves to the GR region at high current levels in all the cases. The lateral electric field distribution is uniform along the edge termination at the optimal P_{ring} dose value, as shown in Fig.4.9-(a), leading to the highest voltage capability at the cost of a premature snapback effect. As introduced in Chapter 3, the I_{snap} value is due to the Egawa effect when the N^-_{epi} concentration becomes lower than the charge induced by the avalanche process[4]. On the other hand, the lateral electric field distribution exhibits a peak at the last ring of the edge termination for higher P_{ring} doses while the peak is at the periphery for low P_{ring} doses. In both cases, the lateral electric field distribution becomes more balanced with the increase of the avalanche current level, leading to a more uniform distribution over the rings, as shown in Fig.4.9-(b). Therefore, the *I-V* curves for the non-optimal cases show a PDR branch at certain current level, before the last NDR branch. Anyway, in the non-optimal cases, the vertical electric field collapses and the negative resistance effect takes place before reaching a balanced lateral electric field distribution (see Fig.3.23-(b)).

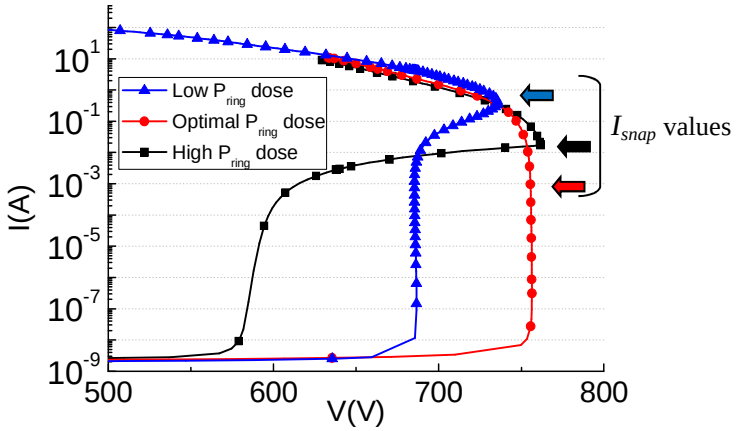

Fig.4.8. Simulated *I-V* curves for different P_{ring} doses.

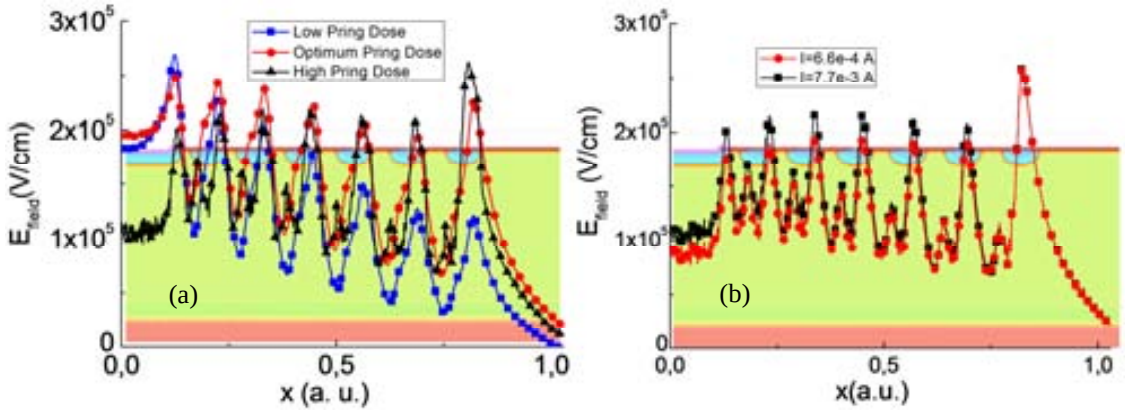

Fig.4.9. (a) Lateral electric field distribution at 7 mA for different P_{ring} doses. (b) Lateral electric field distribution for the high P_{ring} dose at different current levels.

In conclusion, a robust guard-ring edge termination structure can be achieved by optimising the trade-off between the voltage capability and the snapback current level. The maximum V_{bd} value is reached at the optimum P_{ring} dose, but a sharp decrease in the snapback current is found due to the Egawa effect in the edge termination area. As a consequence, **devices with optimal P_{ring} dose are not robust**. As deducted from Fig.4.8, the snapback current level can be increased by almost 4 decades when a lower P_{ring} dose is used. Thus, a robust edge termination can be implemented by using a non-optimal P_{ring} dose or by postponing the NDR branch (making the Egawa effect happen at higher current levels). A method to postpone the NDR branch could be to increase the N^-_{epi} concentration as shown in Fig.4.10. In this sense, the I_{snap} would increase with the N^-_{epi} concentration since more charge to be depleted would be available in the N^-_{epi} layer and the Egawa effect would happen at a higher current level. However, the V_{bd} would become too low for the device requirements since as the N^-_{epi} concentration increases, the V_{bd} decreases.

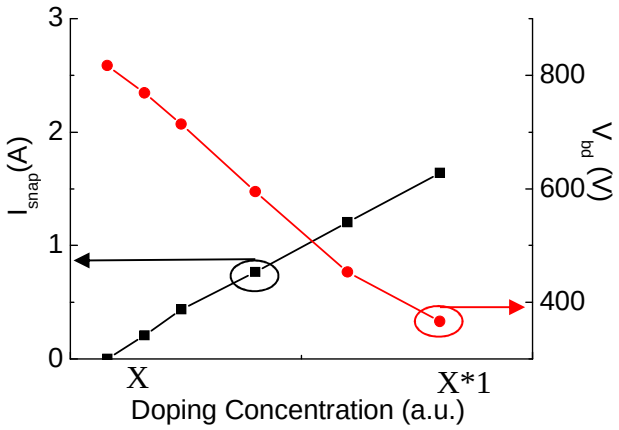

Fig.4.10. Dependence of the V_{bd} and I_{snap} on the N^-_{epi} doping concentration

4.4. How to avoid early failures in the edge termination: postpone the NDR branch

The early failure due to the low robustness of the edge termination needs to be solved by optimising the PiN diode of the edge termination (P_{ring}/ N^-_{epi}/N^{++}). The PiN diode of the active area is not relevant since the UltiMOS active area will be formed by the SJ pillars and, as a consequence, the off-state behaviour of the active area will not be based on the PiN diode approach (a triangular electric field distribution due to the avalanche of the N_{link}/P_{body} junction). A rectangular vertical electric field distribution will be created in the UltiMOS transistor with a higher voltage capability than the simple PiN diode.

The two main approaches to postpone the NDR branch to higher current levels are suggested in the literature to increase the robustness of planar high voltage diodes.

Assuming that the Egawa effect is the reason of the device failures at low current levels, a way to postpone the electric field collapse needs to be introduced. Chen proposed Boron islands implanted at the bottom of the N^-_{epi} region[5] (see Fig.4.11-(a)). The blocking capability it is no longer determined by the doping concentration but by the free carriers. Boron islands are implemented to inject as many holes as necessary to compensate the free electrons, which is the basics of the CIBH (controlled injection of backside holes) method[6]. As for the process flow, a few microns of the N^-_{epi} layer are grown on the N^+_{sub} followed by a photolithography step to locally implant the Boron. Then, the rest of the N^-_{epi} layer is grown. The diffusion of the Boron islands is carried out during the high temperature epitaxial layer growth step. On the other hand, Lutz suggested an intermediate N-type buffer (N_{buff}) layer to be grown in between the N^+_{sub} and the N^-_{epi} layers[7], as shown in Fig.4.11-(b). In a PiN diode, the E_F peak is located at the N^-_{epi}/N^+_{sub} interface but, when the N_{buff} layer is introduced, the E_F peak is shifted to the N^-_{epi}/N_{buff} interface. Therefore, the E_F can be further increased due to the charge introduced by the N_{buff} layer. In [8] there are 3D electrical field snapshots taken from the simulation of an edge termination structure, showing the different behaviour with or without N_{buff} layer.

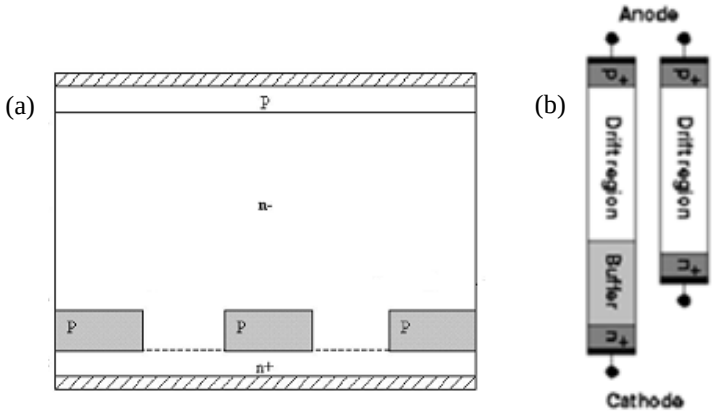

Fig.4.11. Schematic concepts on Planar PiN diodes from literature, being (a) CIBH and (b) N_{buff} layer.

The floating Boron islands are not compatible with the process technology of the UltiMOS transistor. Therefore, an N_{buff} layer is introduced in the planar diode under study to be able to assess the good performance of the PiN diode inherent to the UltiMOS edge termination[9]. The Nbuff layer is easy to be introduced in the UltiMOS process flow (see cross section in Fig.4.12). An extra epitaxial layer growth is required in between the N^+_{sub} and the N^-_{epi} layers, which can be done at the same process step as the N^-_{epi} growth (additional time and different doping concentration) with no additional mask and reduced extra cost. The simulated *I-V* curves for the termination with and without N_{buff} layer are plotted in Fig.4.13, which are scaled to the perimeter of the structure, since the device is supposed to have the highest impact ionisation in that region. The difference in the structures is the different N^-_{epi} layer characteristics. The N^-_{epi} of the structure without N_{buff} is different than the one used in combination with the N_{buff} layer. As a consequence, higher V_{bd} value is reached without N_{buff} layer. The

vertical electric field distributions taken at the edge of the GR (corresponding to the cut in Fig.4.12) at different current levels are plotted in Fig.4.14. As shown from 6.38×10^{-2} to 1.67×10^{-1} A in Fig.4.13, the *I-V* curve shows a PDR branch for the PiN diodes with N_{buff} layer, because the vertical electric field penetrates into this layer (see Fig.4.14-(b)). The NDR is present at high current levels even if the N_{buff} layer is introduced but the I_{snap} value increases 5 decades (more visible if the axis of the *I-V* curves is plotted in linear scale). The I_{snap} levels are indicated by the arrows in the same plot for both *I-V* curves.

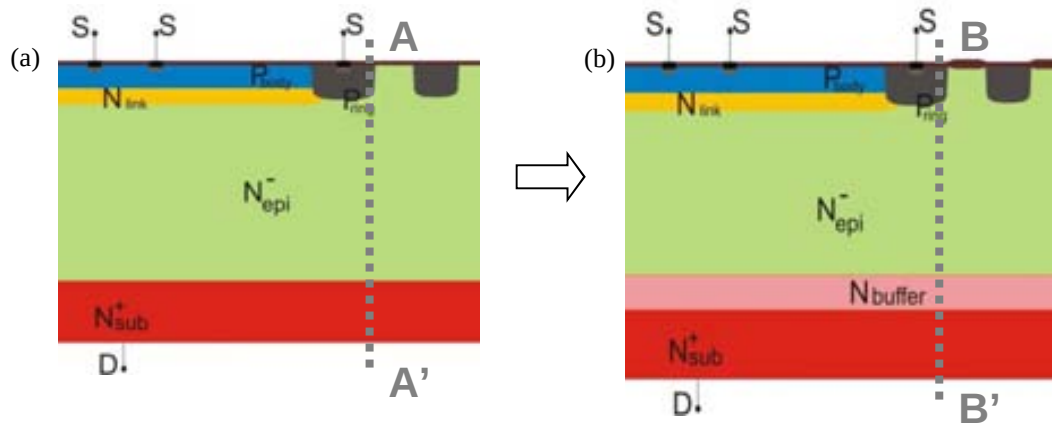

Fig.4.12. Cross-section of the edge of the active area, periphery and beginning of the edge termination for the studied planar diode (a) without and (b) with N_{buff} layer.

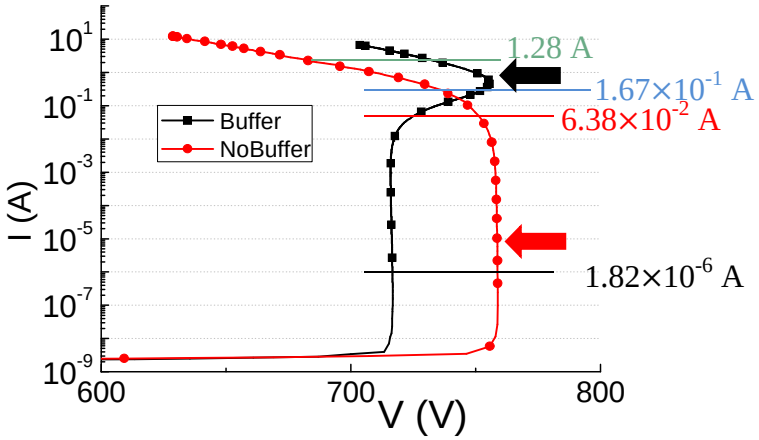

Fig.4.13. Simulated isothermal *I-V* curves showing the effect of an N_{buff} layer for identical P_{ring} dose.

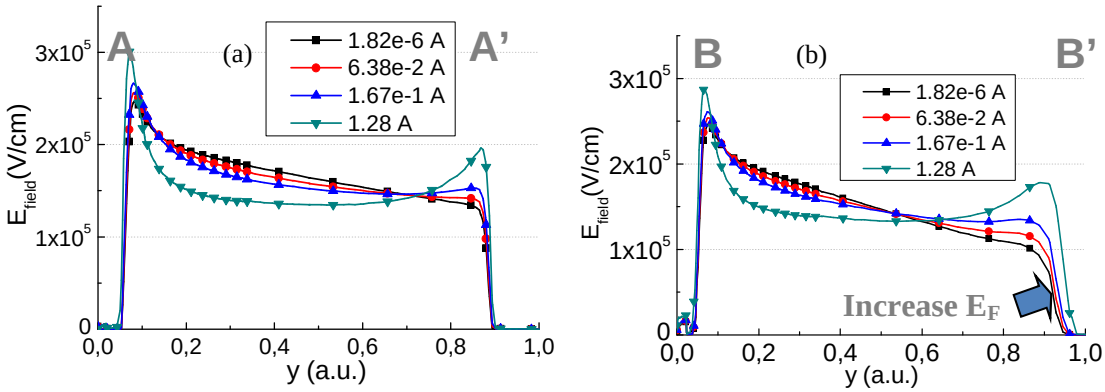

Fig.4.14. Vertical electric field distributions at different current levels indicated in Fig.4.13, at A and B locations according to Fig.4.12, (a) without N_{buff} layer and (b) with N_{buff} layer.

The N_{buff} layer layer is optimized to be able to get a high I_{snap} with no changes on the N^-_{epi} doping concentration to not degrade the voltage capability (see Fig.4.10). The thickness and the doping concentration of the N_{buff} layer layer have been tuned by using TCAD simulations and the results are shown in Fig.4.15. Three different N_{buff} layer concentrations were used to perform the study. The numbers in percentage denote the fraction of the N_{buff} layer thickness versus the complete N^-_{epi}/N_{buff} thickness. The total thickness (N^-_{epi} + N_{buff}) is kept constant in all cases since the final structure has to have the same electrical performance and no degradation of the sR_{on} or V_{bd} values are accepted (to be able to use the same SJ trench depth in all cases). As spotted from Fig.4.15, the V_{bd} value decreases when increasing the N_{buff} layer thickness, because the N^-_{epi} thickness is decreased and the N_{buff} concentration is in all cases higher than that of the N^-_{epi} layer. On the other hand, the I_{snap} value increases with the N_{buff} concentration, since more current is needed to completely deplete the N_{buff} layer[7]. When the N_{buff} thickness is decreased, neither the V_{bd} nor the I_{snap} values are depending anymore on the N_{buff} dose since the N_{buff} layer depletes faster in all cases.

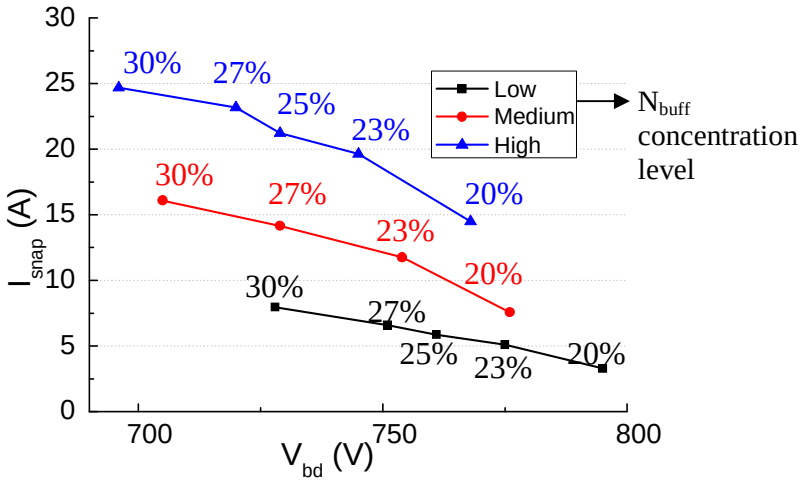

Fig.4.15. Simulated I_{snap} versus edge termination V_{bd} for three different N_{buff} concentrations. The percentages in the figure denote the N^-_{epi}/N_{buff} layer ratio.

The improvement on the failure current when the N_{buff} layer is introduced is corroborated with the TLP measurements performed on the planar diode structure with and without N_{buff} layer, as shown in Fig.4.16-(a). The failure current for the device with N_{buff} layer is considerably high, in the range of 6 A, and an NDR branch is visible in the *I-V* curve in the range of 4-5 A (Egawa effect), but the device failure is postponed by the N_{buff} layer. In the conventional PiN diode structure without N_{buff} layer almost no current is handled by the device when measured under TLP test. When the device fails at a current level in the range of the TLP noise, one can see the load of the line on the *I-V* curves (see Appendix B). All the PiN diodes with N_{buff} layer were able to handle the 100 µA of the V_{bd} measurement set-up without failing since the implemented P_{ring} dose was not the optimum one but 50% lower. The UIS test was performed on these devices (20 per split) and the results are reported in Fig.4.16-(b). In this case, $N_{buff}1$ and $N_{buff}2$ account for two N_{buff}/N^-_{epi} layer thicknesses. A huge increase on UIS current capability

due to the PDR branch is obtained in all the devices with N_{buff} layer, not failing until they are stressed at 10-11 A. On the other hand, devices without N_{buff} layer, can handle just 1-2 A. The difference between the TLP and UIS results can be attributed to the power limitation of the TLP system (Appendix B). Finally, simulations performed on the structure with N_{buff} layer show that the P_{ring} dose can be increased to reach a higher V_{bd} value with the same N^-_{epi} doping concentration and thickness when compared with the structure without N_{buff} layer. Anyhow, if the optimum P_{ring} dose is reached, early failures in the edge termination would be induced again due to the Egawa effect. The chosen edge termination parameters are those which give a V_{bd} value in the range of 750 V with a snapback current in the range of 9-10 A. These values are comparable with those obtained in the structures with N_{buff} layer measured under TLP and reported in Fig.4.16-(a). The $N_{buff}1$ case of the UIS measurements plotted in Fig.4.16-(b) provides a high enough V_{bd} value to accomplish the required specifications and a high I_{snap} value to avoid premature failures in the edge termination area.

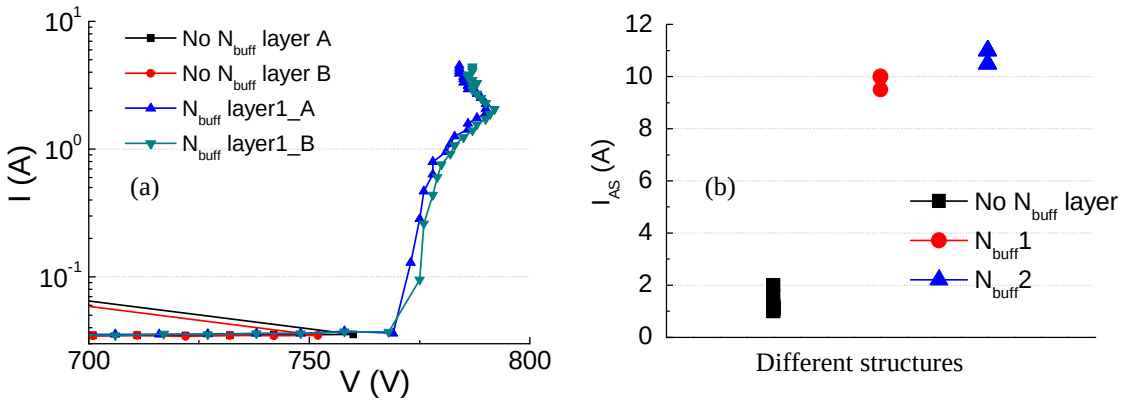

Fig.4.16. (a) TLP measurements on devices with and without N_{buff} layer at the optimum P_{ring} dose. A and B denote two different measured devices with the same characteristics. (b) Measured UIS data showing the boost in avalanche energy capability with the introduction of an N_{buff} layer. For devices with N_{buff} layer, two different N^-_{epi}/N_{buff} thicknesses are used ($N_{buff}1$ and $N_{buff}2$).

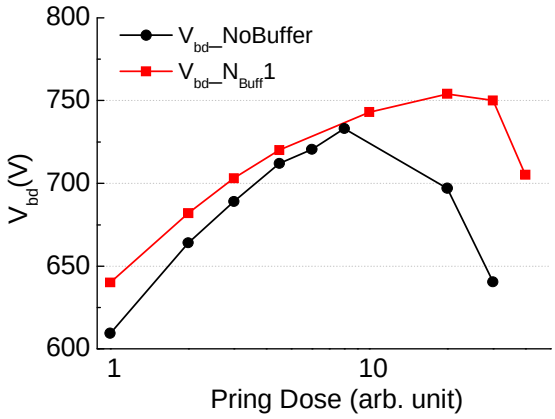

Fig.4.17. Simulated dependence of the V_{bd} on the P_{ring} dose for planar diodes with and without N_{buff} layer.

As a conclusion, **it is proven that the early failure is due to the non-robust edge termination. An optimized edge termination has been designed for the**

UltiMOS transistor, introducing an N_{buff} layer. Anyhow, it is necessary to see how the active area behaves after the introduction of the N_{buff} layer.

4.5. UltiMOS after edge termination optimization

The robustness of the UltiMOS transistor was checked through UIS test once the N_{buff} layer was introduced (see cross section in Fig.4.18-(a)). The measured E_{AS} and V_{bd} values for different CB conditions are shown in Fig.4.18-(b), where it can be observed how the UIS capability is still low for a wide range of CB conditions (Optimum CB and N_{rich}). The voltage capability when the CB condition of the UltiMOS transistor is close to the optimum is in the range of 750 V, higher than the value obtained without N_{buff} layer. In fact, the CB window where the V_{bd} value remains almost constant is wide (arrow in Fig.4.18-(b)), compared with the typical V_{bd}-CB curve of a SJ transistor where the V_{bd} values reach a maximum, and rapidly decrease at both sides of the Optimum CB. The maximum energy capability for P_{rich} UltiMOS transistors is now in the range of 700 mJ (limited by the system), 300 mJ higher than the UIS capability of the initial measurements performed on UltiMOS transistors without N_{buff} layer reported in Fig.3.63. It is worth to mention that the E_{AS} value remains low at the N_{rich} side of the E_{AS}-CB curve, even when the V_{bd} value is already decreasing (see circle in Fig.4.18-(b)). A slight increase of the measured E_{AS} value for UltiMOS transistors with a high N_{rich} value can be inferred in Fig.4.18-(b), being an indicator of the prominent increase of the E_{AS} value with the N_{rich} condition, although devices with high N_{rich} values were not processed on this first study.

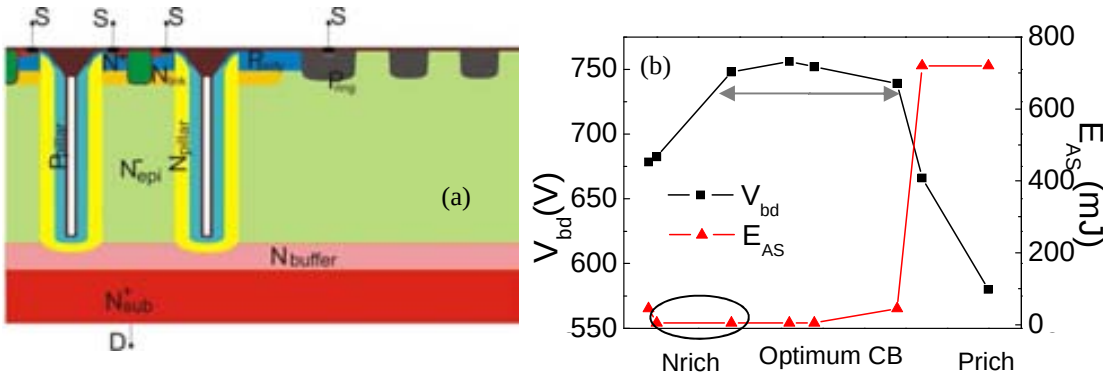

Fig.4.18. (a) Cross section of the UltiMOS active area/periphery/edge termination with the N_{buff} layer for the enhancement of the edge termination robustness. (b) Measured V_{bd} and E_{AS} average values for different CB conditions on the improved UltiMOS transistors with N_{buff} layer.

As already stated, the reverse recovery test is a complementary way to determine the robustness of a power MOSFET. In this sense, the test was performed on Optimum CB UltiMOS transistors to check the weak points of the layout, using as hard switching conditions I_d= 20 A and di/dt= 200 A/µs. The image after the failure is provided in Fig.4.19. Note that the failure spot is in the corner of the device, but further analysis is

needed to determine the exact location since the failure signature is too big to take premature conclusions; the failure could even be in the active area region.

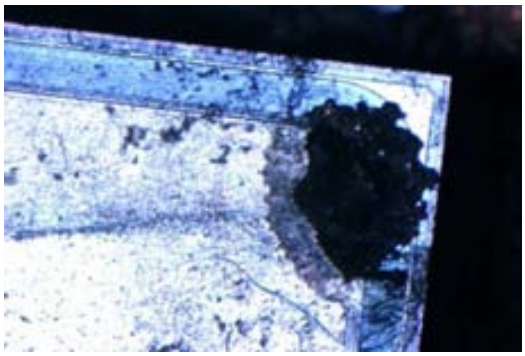

Fig.4.19. Failure spot after a T_{rr} test, located in the corner of the edge termination region.

The increase of the UIS capability in P_{rich} UltiMOS transistors clearly shows that the performance of the active area is also affected by the added N_{buff} layer. Therefore, a detailed analysis of the electrical performance of UltiMOS transistors when the N_{buff} layer is introduced has to be done before keep on the study of the failure causes.

- **Effect of the N_{buff} layer on the electrical performance of the Active Area**

The I_d-V_{ds} curves for UltiMOS transistors with different CB conditions (N_{rich} and P_{rich}), without and with N_{buff} layer are plotted in Fig.4.20-(a) and Fig.4.20-(b), respectively. See that, as in the edge termination structure, the introduction of the N_{buff} layer induces a PDR branch before the structure goes into the final NDR branch and the subsequent device failure. The final NDR branch appears independently of the N_{buff} layer implementation due to the activation of the parasitic bipolar (a more detailed explanation can be found in section 5.2).

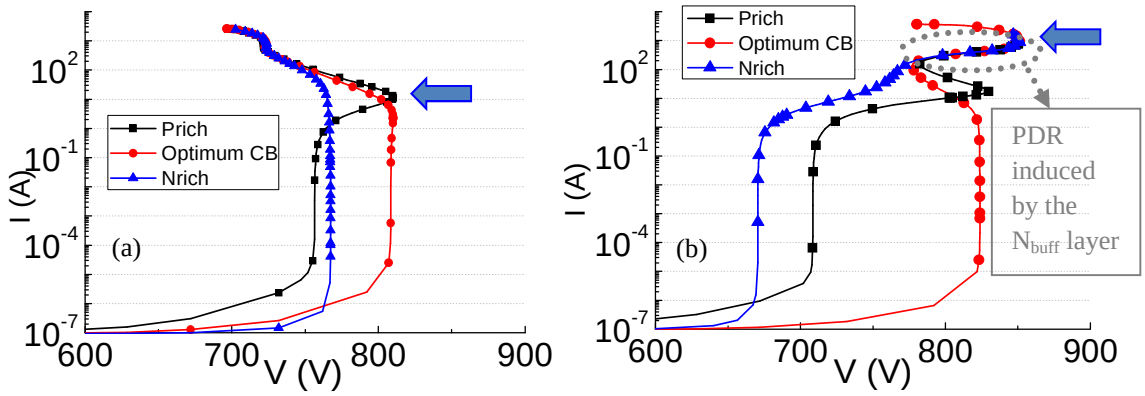

Fig.4.20. Simulated I_d-V_{ds} curves for N_{rich}, Optimum CB and P_{rich} UltiMOS transistors (a) without and (b) with N_{buff} layer.

From the performed simulations, it can be learned that the electrical performance of UltiMOS transistors with Optimum CB condition is a combination of the electrical

performance of N_{rich} and P_{rich} counterparts. The electric field distribution snapshots taken at 3×10^{-7} A for the three different CB conditions are shown in Fig.4.21. The E_F peak for N_{rich} and P_{rich} cases is at the top and bottom of the SJ pillars, respectively. In the case of Optimum CB transistors, the E_F peak appears simultaneously at the top and bottom of the SJ pillars. The vertical electric field cuts plotted in Fig.4.22 are taken in the middle of the SJ trench, in between the PN pillars for UltiMOS structures with and without N_{buff} layer (N_{rich} and P_{rich} CB conditions). In all cases, there is an E_F peak at the top of the structure caused by the P-type implant performed to connect the P_{body} diffusion and the P-pillar layer, which is further studied in Chapter 6. The Optimum CB case is not plotted since it is very difficult to achieve a perfect CB between the pillars and the vertical electric field distribution has to be perfectly flat. Therefore, the E_F is always balanced at the top or at the bottom of the structure.

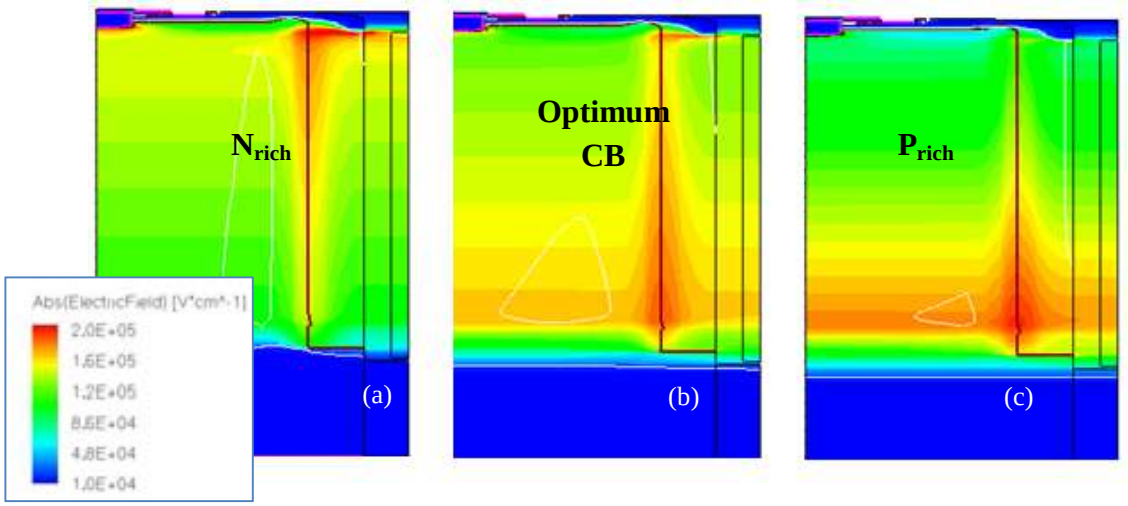

Fig.4.21. Simulated E_F distribution for (a) N_{rich}, (b) Optimum CB and (c) P_{rich} devices taken at 3×10^{-7} A.

As already stated in Chapter 3, the final NDR branch in the UltiMOS structures without N_{buff} layer is induced by the activation of the parasitic bipolar transistor. It is worth to remind that intermediate NDR branches can occur when the current is re-distributed in the structure. A decrease of the electric field in the middle of the N^-_{epi} layer can be observed at high current levels (from 10 to 200 A). On the other hand, when the N_{buff} layer is introduced, the electric field exhibits also a drop in the middle of the N^-_{epi} layer at high current levels, but it can be further increased due to the depletion of the N_{buff} layer, less doped than the N^+_{sub}, inducing the PDR branch. The simulated electric field cuts corroborate the E_F peak at the bottom of the **P_{rich}** structures, as expected from the SJ theory[10]. The small NDR branch exhibited in the I_d-V_{ds} curves corresponding to P_{rich} structures (Fig.4.20) is a direct consequence of the electric field increase at the bottom of the SJ trench before the N_{buff} layer is depleted and the current can be distributed over the bottom of the active area region. Thus, a NDR is induced when the drain current is increased, before the electric field penetrates into the N_{buff} layer. The simulated electric field cuts at different current levels for **N_{rich}** structures with and without N_{buff} layer show the E_F peak at the top of the structure. When a decrease of

the electric field appears in the middle of the N^-_{epi} layer, the maximum impact ionisation region moves from the top to the bottom of the structure. Thus, a PDR branch in the I_d-V_{ds} curve is possible due to the penetration of the electric field into the N_{buff} layer.

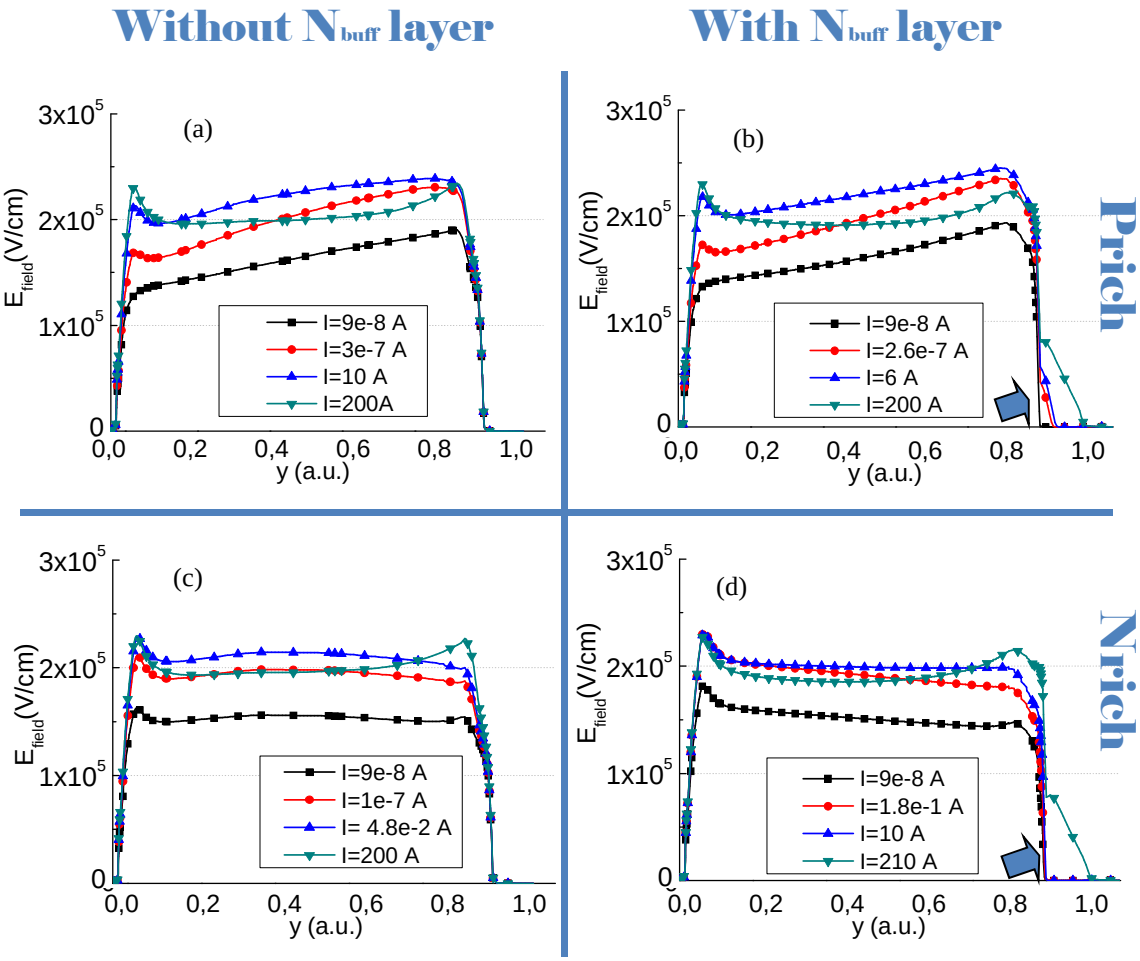

Fig.4.22. Vertical E_F distributions at different current levels according to Fig.4.20 at the active area of a P_{rich} UltiMOS transistor (a) without and (b) with N_{rich} UltiMOS transistor (c) without and (d) with N_{buff} layer.

- ***SRon* and *Vm* of the device with an N_{buff} layer**

As expected, the on-state characteristics of the UltiMOS transistor are affected by the addition of the N_{buff} layer. The sR_{on} value increases with the SJ trench depth. When the N_{buff} layer is added, the bottom of the SJ trench reaches the N_{buff} instead of penetrating directly into the N^+_{sub} (see cross section in Fig.4.23). As a consequence, the sR_{on} value will increase since the doping concentration of the N_{buff} layer is lower than that of the N^+_{sub}. The measured sR_{on} values at different current levels for UltiMOS transistors with and without N_{buff} layer are plotted in Fig.4.24-(a). The reported sR_{on} data is obtained at wafer level. The sR_{on} value measured on packaged devices with proper metals and soldering procedure at the back side of the device and several wires bonded on the drain pads is slightly decreased. The on-state performance could be enhanced by

increasing the doping concentration or decreasing the thickness of the N_{buff} layer. However, the N_{buff} layer characteristics are already fixed by the optimization of the edge termination. The small sR_{on} increase is the cost to be paid in order to have a robust edge termination. The V_{TH} value does not depend on the N_{buff} layer, as shown in the simulated I_d-V_g curves in Fig.4.24-(b). The V_{TH} value basically depends on the doping concentration and depth of the P_{body} diffusion.

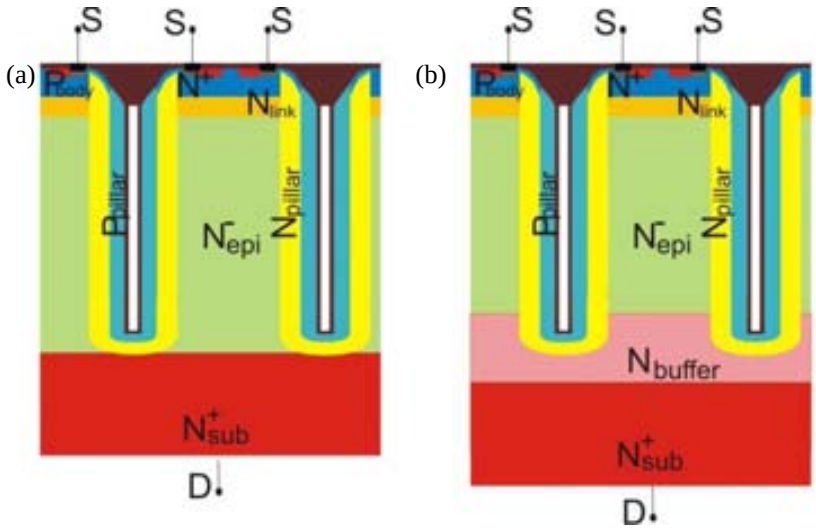

Fig.4.23. Cross section of the active area of an UltiMOS transistor (a) with and (b) without N_{buff} layer.

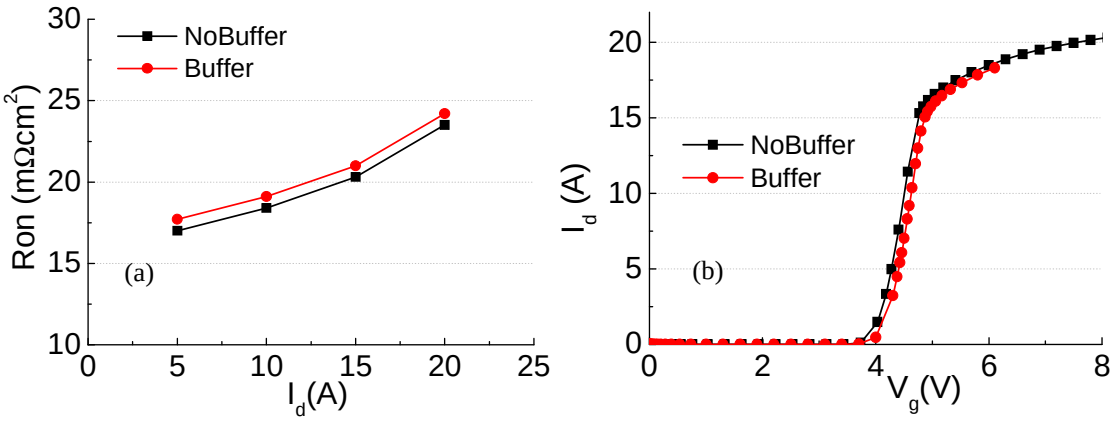

Fig.4.24. (a) Measured sR_{on} values at different current levels and (b) simulated I_d-V_g curves, for the UltiMOS transistors with and without N_{buff} layer.

The average V_{bd} and failure current during the UIS test values at different CB conditions are plotted in Fig.4.25, for UltiMOS transistors with and without N_{buff} layer. The structure with N_{buff} layer has some extra microns to increase the V_{bd} value by regulating the electric field distribution at the bottom of the SJ trench. Moreover, the N^-_{epi} dose is slightly lower than in the structure without N_{buff} layer, further increasing the V_{bd} value. The shift of the V_{bd} in both cases indicated that the amount of charges on the N^-_{epi} for the structure without N_{buff} layer is larger than the amount of charges of the N^-_{epi} plus the N_{buff} layer in the structure with the N_{buff} layer. Thus, more P-type charges are

needed in the epitaxial NIP grown in the structure without N_{buff} layer to be in the P_{rich} side of the CB window. It can be inferred that, unfortunately, the minimum E_{AS} value is not increased for Optimum CB devices even when the N_{buff} layer is introduced.

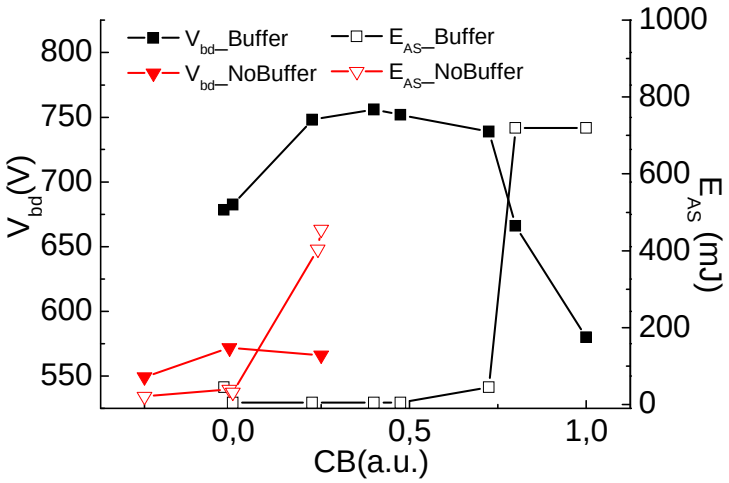

Fig.4.25. Comparison of measured V_{bd} and E_{AS} values under the UIS test values at different CB conditions for the enhanced UltiMOS transistors with and without N_{buff} layer.

4.6. Conclusions

The spot location of the failures after UIS tests lead to the improvement of the edge termination robustness with the introduction of the N_{buff} layer. The edge termination robustness has been improved as demonstrated by simulation and experimental results on planar diodes. New measurements were performed on UltiMOS transistors with the N_{buff} layer optimized for enhancing the I_{snap} value and the UIS capability of the edge termination. The results showed an improvement in the case of P_{rich} transistors (with a double E_{AS} value) but the energy capability is still low for Optimum CB and N_{rich} counterparts. Therefore, a further investigation is needed taking into account the electric field distribution inside the active area. In the next chapters, the structures under study always include the N_{buff} layer optimized to enhance the I_{snap} value of the edge termination.

4.7. References

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CHAPTER 5

Active Area study

The active area of the UltiMOS transistors is studied in depth to comprehend the current distribution over the device when a UIS test is performed. The aim of the work is to know which is the weakest region of the device, to avoid premature failures for a certain CB condition. Different structures derived from the UltiMOS are studied to understand the failures due to the parasitic bipolar activation, which depends on the CB condition.

5.1. Introduction

Although the robustness of the P_{rich} UltiMOS transistors is slightly improved with the addition of the N_{buff} layer optimized for the edge termination, as shown in Fig.4. 25, a further improvement is needed to have the wide enough CB manufacturability window to go into the market. The failure spot of an UltiMOS transistor with N_{buff} layer (Fig.4. 19) is located in the corner of the active area. On the contrary, the failure spot was placed in the edge termination when the N_{buff} layer was not yet introduced into the structure (Fig.4. 1). Thus, the periphery of the active area, the interface between the PiN diode of the edge termination and the active area SJ trenches, has to be carefully analysed to design a reliable UltiMOS transistor since the electric field distribution changes in that region from a 2D (edge termination PiN diode) to a 3D nature (the SJ structure). The layout of the structure has also been carefully checked, taking into account the possible activation of the parasitic bipolar transistor at certain regions of the structure. In the following subsections, the activation of the parasitic bipolar transistor is described and the different basic structures derived from the UltiMOS architecture are analysed, showing the electric field distribution over the active area and its impact on the device robustness. The different structures and the aim of their study are:

- UMOS (section 5.3.1):
    - Current distribution.
    - Bipolar transistor activation

    - Gate impact.
- SJ Diode (section 1.1.1):
    - Differences on electrical behaviour for different CB conditions.
    - Current distribution.
- SJ Diode with gate (section 1.1.1):
    - Differences on electrical behaviour for different CB conditions.
    - Current distribution.
    - Gate impact.
- SJ Bipolar (section 5.3.3):
    - Differences on electrical behaviour for different CB conditions.
    - Bipolar transistor activation.
    - Current distribution.
    - Impact of technological process steps on the parasitic bipolar transistor activation.

5.2. Parasitic Bipolar Transistor activation

The introduction of the N_{buff} layer in the UltiMOS structure causes a PDR branch in the I_d-V_{ds} curve at a drain current in the range of 100 A, as deducted from simulations. The basic effect is that the electric field distribution does not depend anymore on the CB condition at high current levels and the I_d-V_{ds} curves of all the implemented UltiMOS structures merge at that current range (see Fig.5.1). At very high current levels (600 A) the activation of the parasitic vertical bipolar transistor structure defined by the N^+ source (Emitter)/ P_{body} (Base)/N_{link}/N^-_{epi} (Collector) induces the final and destructive snapback in the I_d-V_{ds} curve (see schematic in Fig.5.2). However, the parasitic bipolar transistor activates at much lower current level when the N_{buff} layer is not implemented (10 A) (see difference on the I_{snap} value in the simulated I_d-V_{ds} curves from Fig.5.1). It is assumed in both cases that the whole active area is conducting the avalanche current as derived from the different thermal mappings.

To assess that the final snapback is due to the activation of the parasitic bipolar transistor, simulations with the source contact split into two independent contacts for P_{body} and N^+ diffusions are performed. The body and source simulated currents as a function of the drain current for the three different CB conditions are plotted in Fig.5.3. The simulation is performed to qualitative describe the bipolar activation. The drain voltage is set to 0.5 V and the body electrode is swept from 0 to 0.5 V, emulating a source of electrons on the P_{body} layer, close to the N^+ diffusion, that will activate the parasitic bipolar transistor. Notice that in Fig.5.3 there is a slope change in the body current at a certain current level. This change is a hint of the non-negligible current that flows through the source contact, meaning that the bipolar transistor is activated.

Afterwards, the source current (bipolar emitter) overcomes the base current (bipolar base), corroborating the activation of the parasitic bipolar at high current levels[1].

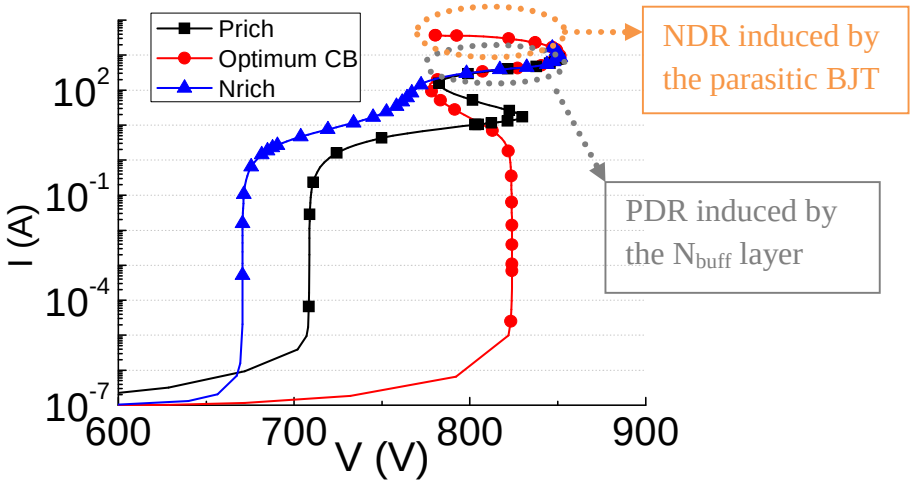

Fig.5.1. Simulated I_d-V_{ds} curves for N_{rich}, Optimum CB and P_{rich} UltiMOS basic cell structures. The curves are scaled by the total active area.

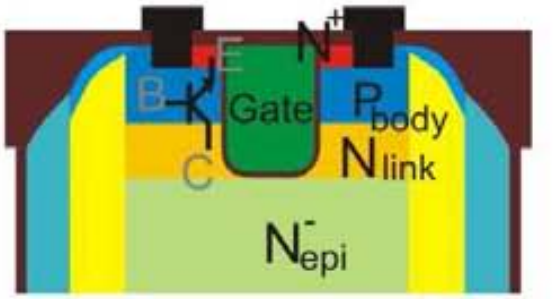

Fig.5.2. Cross section of the parasitic BJT inherent to the UltiMOS structure, formed by the N^+ source/ P_{body} /N_{link}/N^-_{epi} layers.

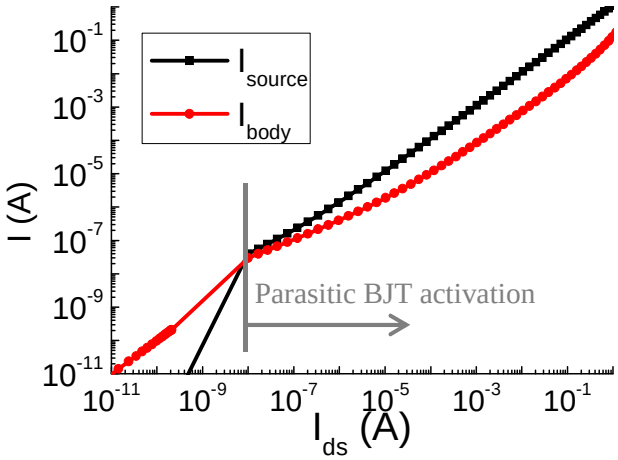

Fig.5.3. Body (I_{body}) and Source (I_{source}) currents as a function of the drain current level.

The parasitic bipolar activation does not depend on the CB condition of the UltiMOS structure (the I_{body}-I_{ds} and I_{source}-I_{ds} curves with different CB are overlapped).

In order to determine how prone to the parasitic bipolar transistor activation inherent to the UltiMOS transistor is, and how its activation can be avoided, different basic structures are analysed. It is important to remind that the drain current values used in the previous sections are directly derived from the I_d-V_{ds} simulated curves, assuming that the whole active area is carrying the current. A drain current of 100 A will never be possible since the device would be already destroyed, even assuming a conduction in the whole active area (see Chapter 3). However, when the current focalization is present, the simulated current levels decrease and become in accordance with the experimental results, as detailed in the next section.

5.3. Basic structures analysis

The first implemented structure is the conventional trench power MOS transistor (**UMOS** transistor) using the same technological process steps as in the UltiMOS transistor, except the formation of the SJ trenches. The resulting structure is similar to the planar diode described in section 4.1 with the inclusion of the trench gate and the N^+ source diffusion. The current distribution over the device and the activation of the parasitic bipolar transistor inherent to the UMOS structure are investigated. The electric field distribution in the active area and in the edge termination is identical with a triangular shape of the vertical electric field, being its maximum located at the top of the structure. The second studied structure includes the SJ pillars but not the gate trench nor the N^+ source diffusion (see Fig.5.4-(a)). The resulting **SJ Diode** is used to determine how the current distribution changes in the device when the SJ pillars are added. Since no N^+ diffusion is implemented, there is no possible bipolar transistor activation in the SJ Diode. Finally, the N^+ diffusion is added to the SJ Diode to emulate a **SJ Bipolar** transistor (see Fig.5.4-(b)), and the current distribution over the device is again investigated. From this structure, the parasitic bipolar transistor activation is easily studied by tuning the technological parameters at the top of the structure.

Automatic V_{bd} measurements and the failure current during the UIS test (I_{AS}) at a wafer level are first performed in all the fabricated basic structures. Experimental results are compared with the simulated values to be sure that the electrical behaviour of the basic structures can be properly described with TCAD simulations. Thermal Mapping is performed during the UIS test on the different basic structures to monitor the current distribution of the structure. EMMI images are also taken in all the studied structures to confirm the maximum impact ionisation location in each case. TIM measurements are performed on UltiMOS transistors to see the activation region of the devices under TLP pulses and prove the assessments derived from the analysis of the UMOS, SJ Diode and SJ Bipolar structures. Finally EMMI, thermal mapping and TLP measurements are also performed on the UltiMOS transistors with different CB conditions to confirm the statements on the electrical behaviour derived from the previous studied structures.

Thus, a large amount of experimental results are used to analyse the cause of the low current capability for certain CB conditions.

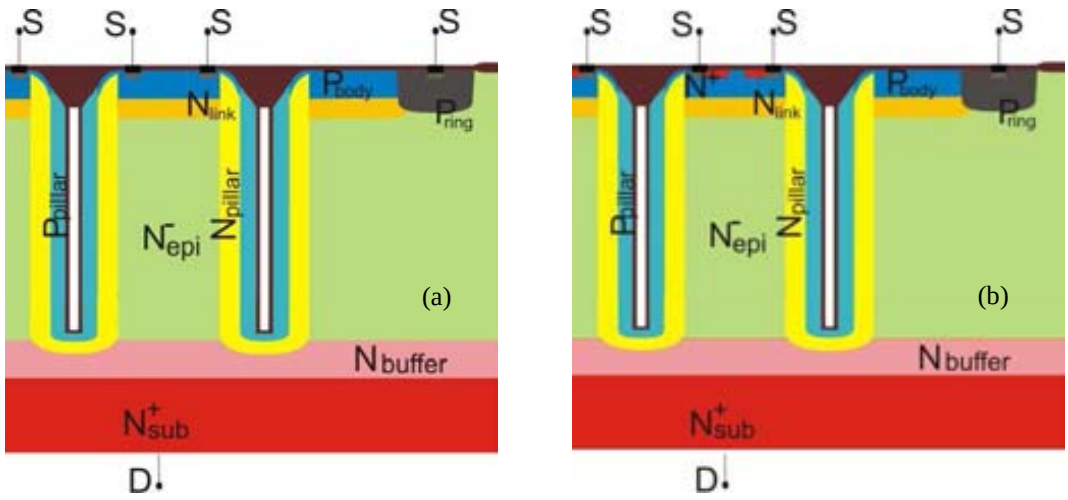

Fig.5.4. Cross sections of (a) SJ Diode and (b) SJ Bipolar transistor.

5.3.1. Trench MOSFET (UMOS)

As introduced, the UMOS transistor is similar to the planar diode studied in section 4.1, with the addition of the shallow N^+ source diffusion and the trench gate steps in the technological process (see schematic in Fig.5.6-(a)). The investigation on UMOS transistors is performed due to the similar electric field distribution in N_{rich} UltiMOS and UMOS transistors with the E_F peak located at the top of the structure: at the top of the SJ trench and at the corner of the gate trench for N_{rich} UltiMOS transistors and at the top of N^-_{epi} and in the gate trench corner for UMOS transistors. Thus, the fabricated UMOS transistors are used to check if the device weakness comes from the gate architecture, since the gate trench causes an electric field crowding at the trench bottom corners as confirmed from previous experiments (section 3.3.1). Moreover, the UMOS structure can also be used to investigate if the parasitic vertical bipolar transistor ($N^+/P_{body}/N_{link}/N^-_{epi}$ layers) is activated at low current values.

The simulated isothermal I_d-V_{ds} curve for an UMOS transistor is plotted in Fig.5.5. The automatically measured V_{bd} values at different current levels and the isothermal simulated I_d-V_{ds} curve of the edge termination are also plotted in the same figure. Note that the simulated I_d-V_{ds} curve of the UMOS active area is very close to the measured V_{bd} values at different current levels. From the behaviour of both isothermal I_d-V_{ds} curves, it can be inferred that the avalanche process starts in the active area of the device and, in the range of 20-30 A, the current shifts to the edge termination due to the presence of the NDR branch induced by the Egawa effect in that region. This behaviour can be demonstrated by TCAD simulations but no experiments have been performed at such high current range due to the power limitation of the measurement systems. No self-heating is considered on this structure since the simulations are 2D and it do not

properly emulate the real device due to the complexity of the current distribution on a 3D structure. Thus, the thermal impedance cannot be easily modelled on the studied structures.

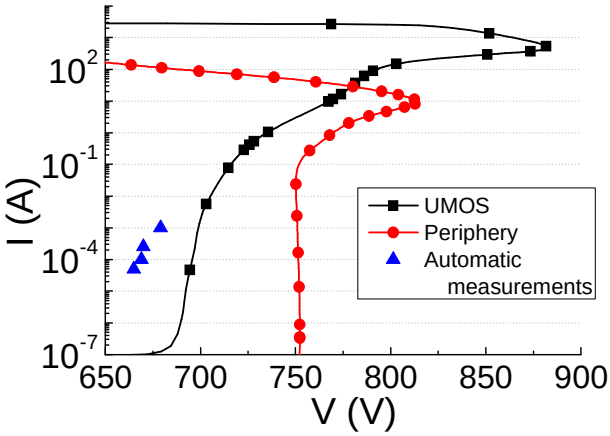

Fig.5.5. Simulated I_d-V_{ds} curves for the active area of the UMOS structure, a guard-ring edge termination and measured V_{bd} for an UMOS transistor. The simulated active area curves are scaled to the active area and the edge termination curves to the periphery area.

The vertical electric field at different current levels taken at the CC' cut of the active area (indicated in Fig.5.6-(a)), are plotted in Fig.5.6-(b). Notice that the E_F peak is located in the P_{body}/N_{link} junction, showing a triangular shape close to that region as expected in any vertical power MOSFET[1]. However, in the N^-_{epi} layer the electric field has a rectangular shape since there is no variation of the dopant type or doping concentration. The automatic V_{bd} and E_{AS} measurements performed along a wafer row are plotted in Fig.5.7-(b) to show the good uniformity across the wafer. The average V_{bd} value is 680 V and the E_{AS} obtained from the UIS test is in all cases 780 mJ, which is the limit of the UIS measurement set-up. The V_{bd} values are constant along the row on the different measured devices, even slight variations in the range of 5-10 V are captured, which can be induced by small variations on a specific technological process. The potential lines in the corners of the active area will crowd differently, leading to these small variations in the V_{bd} value.

The UIS test current can homogeneously spread through the whole active area of the device, as shown on the thermal mapping performed during a discharge of 8 A current pulse (see Fig.5.8-(a)). It is evidenced that the temperature is not higher than 45ºC, which is quite low for the amount of power that has to be dissipated in the device (in the range of 5.5 kW). The thermal mapping is taken at 150 µs (Fig.5.8-(b)), when the temperature is maximal[2].

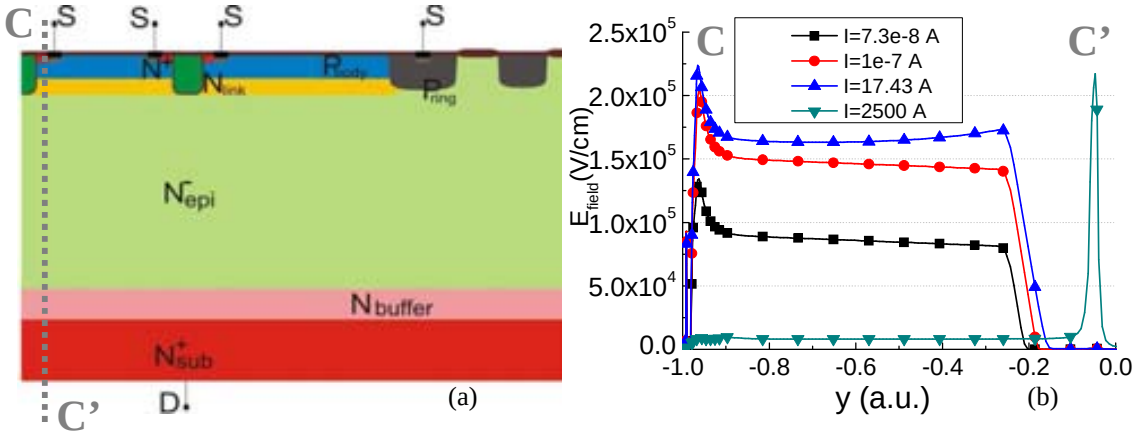

Fig.5.6. (a) Cross section of the active area-periphery regions. (b) Vertical E_F distributions at different current levels, taken at the CC' cut (-1 and 0 corresponds to the top and bottom of the structure, respectively).

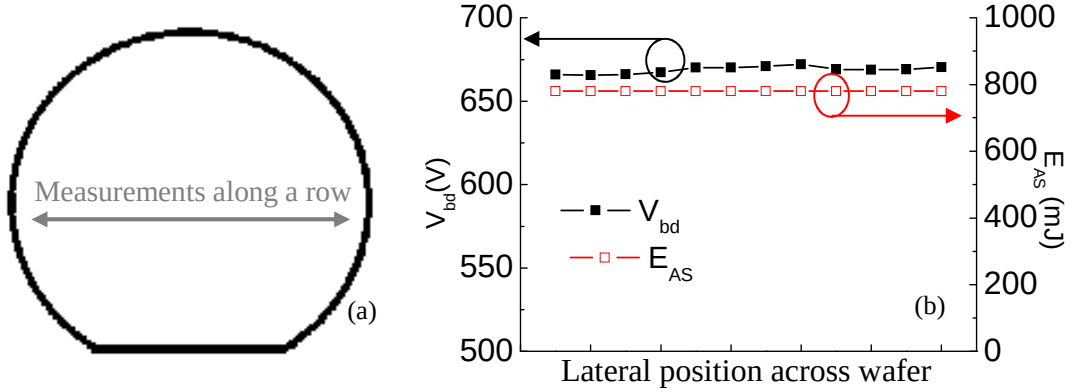

Fig.5.7. (a) Schematic of a wafer to indicate where measurements are performed. (b) Measured V_{bd} and E_{AS} average values along a UMOS wafer row for a single avalanche UIS test, done with a fixed inductor of 10 mH.

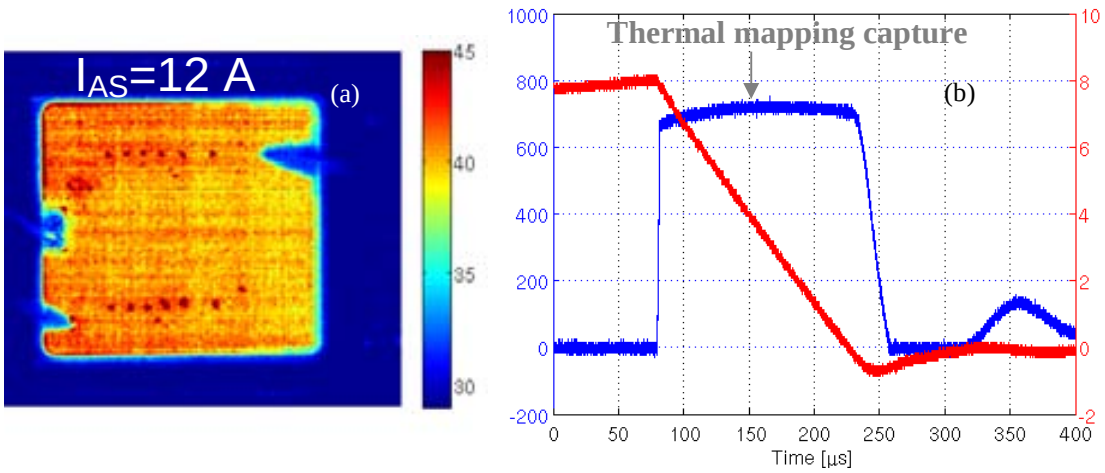

Fig.5.8. (a) Thermal mapping under the UIS pulse on an UMOS transistor and (b) corresponding *I-V* curves during the UIS test. Courtesy of Unina.

From the electron current density snapshots taken at different current levels for the UMOS structure (Fig.5.9), it is demonstrated that an NDR branch is forced by the parasitic bipolar transistor activation (see current density at I_d=2000 A, when the NDR is already present). Anyhow, the edge termination would take the current before the

bipolar activation starts as deduced from Fig.5.5. The shift of the current flow is due to the heating of the active area at high current levels leading to a higher impact ionisation at the termination region at certain current level, since this region is cooler than the active area. This effect is only possible since both I_d-V_{ds} curves merge at a certain current level.

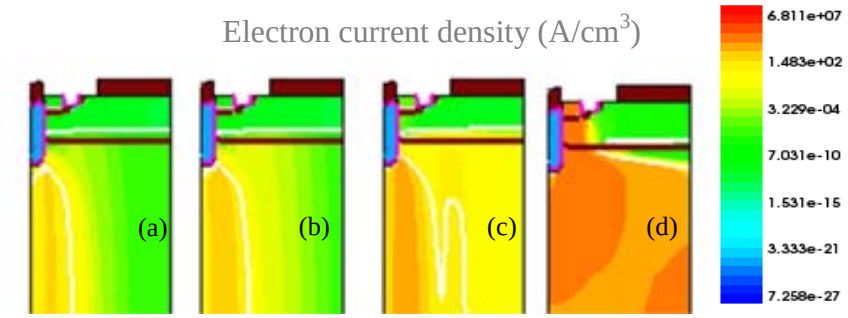

Fig.5.9. Simulated electron current density at different current levels in an UMOS structure. Current levels are (a) 7.3e-8, (b) 1e-7, (c) 17.43 and (d) 2000 A.

Finally, the UMOS structure has been simulated for different off-state gate voltages. This study is done to assess that the trench gate bottom is responsible for the dependence of the V_{bd} value on the gate bias. The obtained off-state I_d-V_{ds} curves are plotted in Fig.5.10, showing the decrease in V_{bd} values as the gate bias becomes more negative, as already observed in UltiMOS transistors (section 3.3.1). The same reasoning can be followed here: the negative gate voltage makes the potential lines crowd at the bottom corner of the trench gate a lower drain voltage values than the one needed to cause the avalanche on the N_{link}/P_{body} junction.

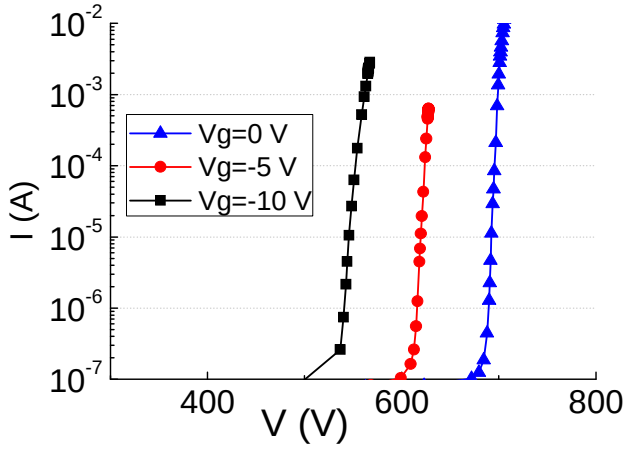

Fig.5.10. Simulated I_d-V_{ds} curves for an UMOS transistor with V_{gs} ranging from 0 to -10 V.

It can be concluded from the study of the UMOS transistors that the inherent parasitic bipolar does not trigger at low current levels since the applied current is perfectly distributed through the whole active area. At higher current levels the parasitic bipolar transistor is not activated since the higher impact ionisation is then located at the edge termination region. Therefore, the analysed devices handle an I_{AS}=11-12 A when a 10 mH inductor is used. Nevertheless, the electric field crowding at the trench gate

bottom could affect the electric field distribution over the UMOS active area, leading to a voltage capability degradation when variations on the potential distribution are present on the structure. Finally, it is important to remember that the vertical electric field distribution will change completely when the SJ trenches are implemented. Thus, SJ Diodes and SJ Bipolars are studied to go deeper in the electric field behaviour depending on the CB condition.

5.3.2. SJ Diode

SJ Diodes are fabricated with the same process flow as the UltiMOS transistor skipping the gate module and the shallow N^+ source implant (see Fig.5.11). The source electrode is then directly connected to the P_{body} diffusion, which is the anode of the SJ Diode. A P-type high doped implant is performed after the contact opening to ensure a good ohmic contact[1]. When a positive bias is applied to the drain electrode (cathode of the SJ Diode), the SJ structure becomes completely depleted at 15-20 V. The study starts with the failure location analysis and the interpretation of the results from the thermal mapping measurements under UIS tests for different CB conditions, to determine the current distribution over the device. The final goal is to identify which are the weakest regions of the device in an avalanche process[3].

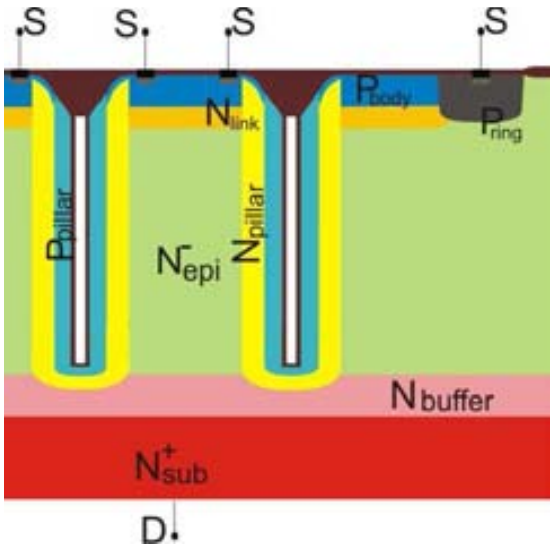

Fig.5.11. Cross section of SJ Diode structure.

The failure signature on SJ Diodes is typically located at the edge of the active area/periphery regions as observed in the Fig.5.12-(a) image, instead of being located at the edge-termination corner as for the first studied SJ UltiMOS transistors (Fig.4.1). The measured average V_{bd} and I_{AS} (using a 10 mH inductor) values in SJ Diode structures with different CB conditions are plotted in Fig.5.12-(b). As for the UltiMOS transistors, the breakdown voltage depends on the CB condition, reaching the maximum value for the Optimum CB case, and decreasing for both P_{rich} and N_{rich} counterparts. As exposed,

the I_{AS} value is in the 9-10 A range when the CB condition gets close to the Optimum CB value. On the contrary, unbalanced samples can sustain more than 12 A, which is the limit of the UIS system.

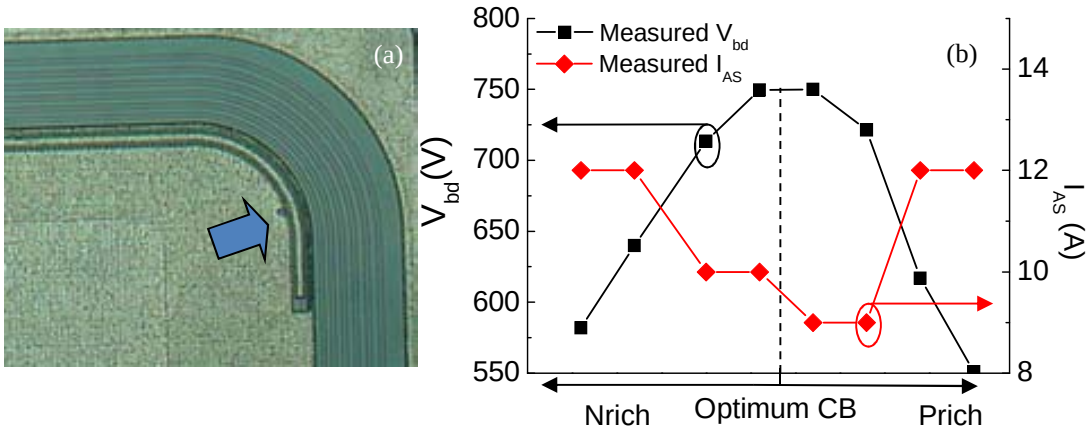

Fig.5.12. (a) Failure on the corner of the active area for a fabricated SJ Diode. (b) Experimental V_{bd} and I_{AS} values for different CB conditions. Plotted values correspond to the average value of 1150 devices.

IR Thermography Mapping has been performed on SJ Diodes with different CB conditions to monitor the current distribution during an UIS test. The voltage-current evolution for an 8 A UIS test is plotted in Fig.5.13-(b), Fig.5.13-(d) and Fig.5.13-(f). N_{rich} and P_{rich} SJ Diodes have lower V_{bd} at t=0 than the Optimum CB counterpart (as detailed in Table 5.1). The comparison at t=0 is done because heating at the beginning of the avalanche process can be disregarded. A calibration process has to be done after the thermal mapping to extract the maximum temperature (T_{max}) value in the device[2]. The temperature distribution in Fig.5.13-(a), Fig.5.13-(c) and Fig.5.13-(e) is an indicator of the current spreading through the SJ Diode. All the thermal mappings are taken at the T_{max}, corresponding to the maximum avalanche voltage during the UIS test[4].

For N_{rich} and P_{rich} SJ Diodes the heat generated during an UIS pulse spreads across the active area (see Fig.5.13-(a) and Fig.5.13-(e), respectively). The homogeneous current distribution in the whole active area for P_{rich} SJ Diodes is due to the avalanche located at the bottom of the SJ pillars[5]. Conversely, the maximum impact ionisation is located at the top of N_{rich} structures but, the current spreading in the active area is more difficult due to the SJ trench distribution on the device layout and the airgap into the SJ trenches. Hence, higher avalanche current will flow near the corners of an N_{rich} SJ Diode, where the potential lines are crowded and the current cannot easily spread inside the active area. It is worth to remember that this is not an optimum design for a conventional power diode. Notice that the maximum temperature for the measured N_{rich} and P_{rich} SJ Diodes is 70 and 47 ºC, respectively (see Table 5.1).

SJ Diodes with Optimum CB exhibit current focalisation in the periphery region, surrounding all the active area (Fig.5.13 (b)), with T_{max} =170ºC at 8 A, very close to the T_{in} value of the used N^-_{epi} layer. The EMMI image of an Optimum CB SJ Diode

reported in Fig.5.14 confirms the current focalisation in the periphery region. The Failure Analysis (FA) of an Optimum CB SJ Diode (failing in the periphery) is presented in Fig.5.15-(a). An image of the failure spot of an Optimum CB SJ Diode, obtained by lock-in thermography[6] is shown in Fig.5.15-(b), hinting to the current focalization on the device periphery. It has been proven in previous works that the avalanche capability is strongly depending on the initial impact ionization location[7].

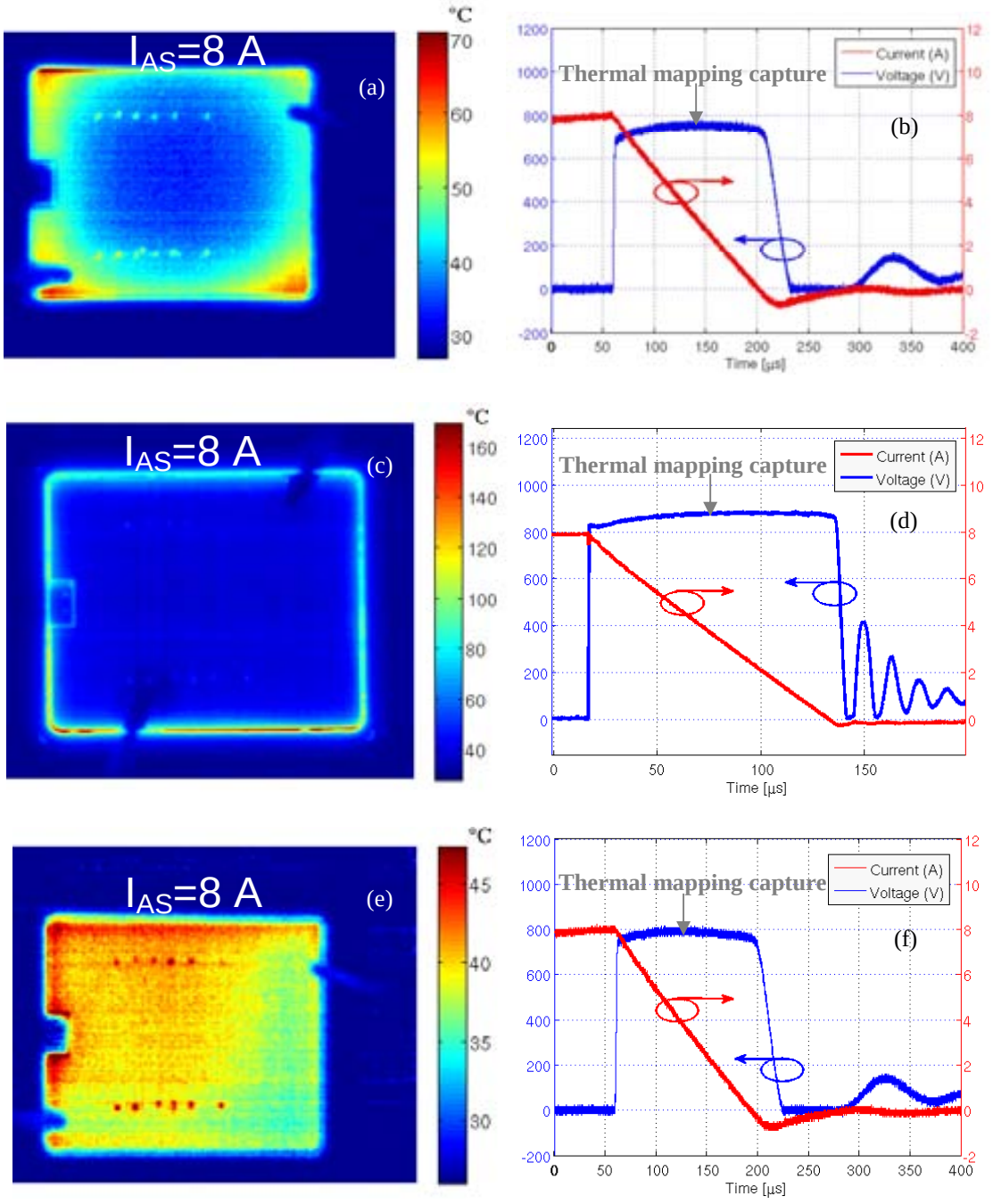

Fig.5.13. Thermal mappings during UIS pulses for (a) N_{rich}, (c) Optimum CB and (e) P_{rich} SJ Diodes. Mappings extracted at maximum temperature during the UIS pulse with the initial current fixed at 8 A. Corresponding *I-V* waveforms during UIS pulses for (b) N_{rich}, (d) Optimum CB and (f) P_{rich} devices. Courtesy of Unina.

	CB (%)	V(t=0) (V)	T_{max} @ 8A (ºC)
N_{rich}	-10	700	70
Optimum CB	0	820	170
P_{rich}	8	750	47

Table 5.1. V(t=0) and maximum temperature (T_{max}) values for the different CB conditions under the 8 A UIS test, according to Fig.5.13.

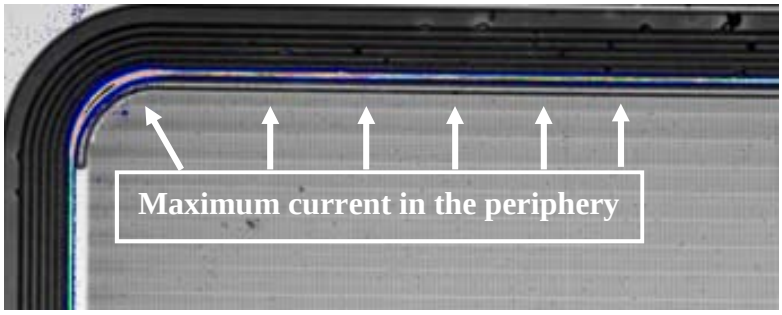

Fig.5.14. EMMI image of an Optimal CB SJ Diode, showing the periphery activation at 780 V-1.2 mA (using 5x lens and a 20 sec exposure).

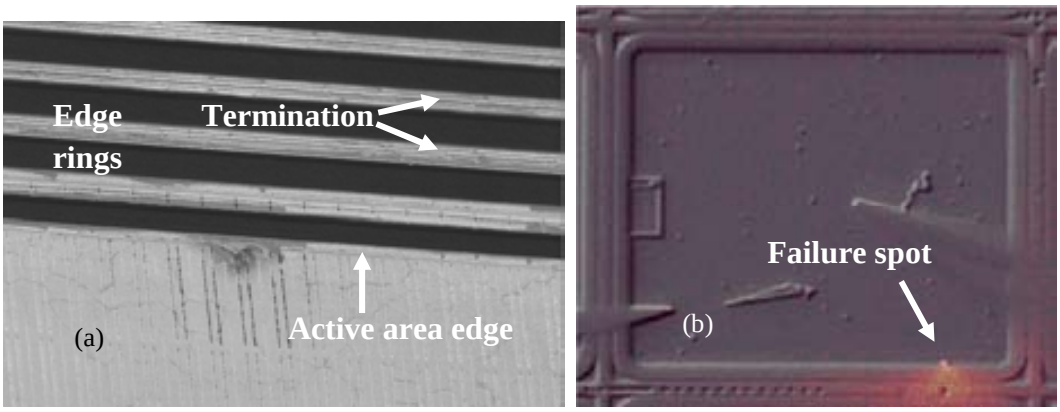

Fig.5.15. (a) FA on an Optimum CB SJ Diode, showing the failure at the periphery. (b) Failure spot obtained by lock-in thermography, courtesy of Unina.

2D TCAD simulations of the core cell are performed for N_{rich}, Optimum CB and P_{rich} SJ Diodes, and the corresponding I_d-V_{ds} curves are plotted in Fig.5.16-left, together with an *I-V* curve of the edge-termination/periphery structure simulated in section 4.4. All the curves are scaled according to the activated area derived from the thermal measurements reported in Fig.5.13, taking into account the whole active area (for N_{rich} and P_{rich}) or just the periphery region (Optimum CB). The Optimum CB SJ Diode exhibits a V_{bd} value higher than the one corresponding to the periphery (see Fig.5.16-(a)). A snapshot of the simulated electric field on the periphery region is captured in Fig.5.16-(b). As inferred, the peak is located at the edge of the active area, called periphery in this work and where the P_{ring} diffusion stops, in concordance with the experimental EMMI and thermal mapping results provided in Fig.5.13 and Fig.5.14, respectively. This means that when the CB is Optimum, the avalanche is dominated by the periphery instead of being ruled by the SJ trenches in the active area, as depicted in the schematic in Fig.5.17.

Thus, the current cannot be homogeneously distributed as required to be able to reach a high energy capability during an UIS test[8]. Optimum CB SJ Diodes can just handle the same E_{AS} value as the edge termination with the optimized buffer, studied on section 4.4 (see Fig.4.16).

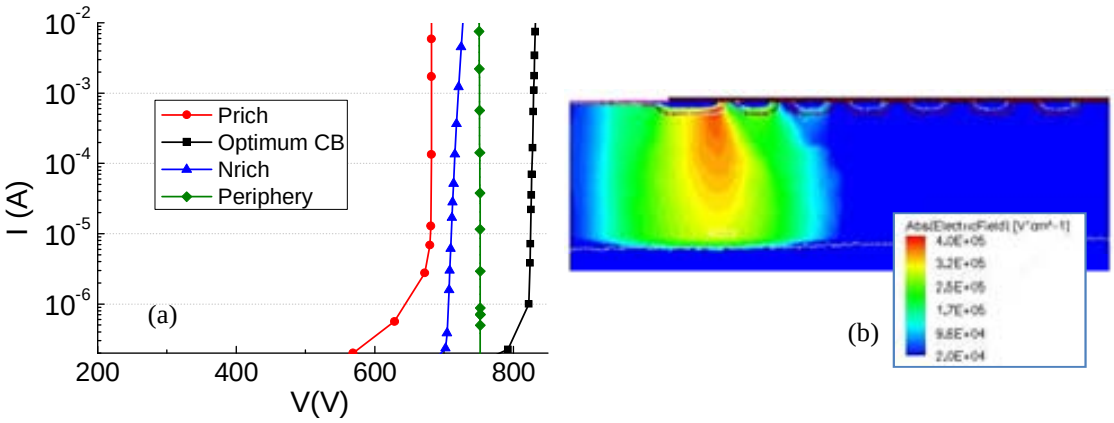

Fig.5.16 (a) Simulated isothermal I_d-V_{ds} curves for the active area of the SJ Diode with different CB conditions and for the periphery region. (b) Snapshot of the simulated electric field in the periphery region, showing the E_F peak in the edge of the active area.

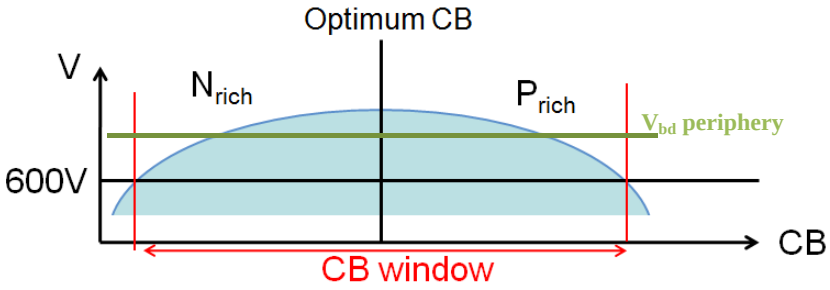

Fig.5.17. The V_{bd} value in the periphery region is lower than the V_{bd} value of the SJ structure when the CB is close to the Optimum.

To finish the study of the current focalization in the periphery of the SJ Diodes, the simulation results are compared with TLP measurements for different CB conditions. The simulated I_d-V_{ds} curves for the three possible cases (N_{rich}, P_{rich} and Optimum CB governed by avalanche in the periphery region) are plotted in Fig.5.18-(a). The early failure for the Optimum CB case is explained by considering that the periphery region, which dominates the avalanche process in the case of Optimum CB SJ Diodes, exhibits a lower I_{snap} value than that of the P_{rich} and N_{rich} cases. This low I_{snap} value is again related with the PiN diode effect[9] in the edge of the active area. The I_{snap} value for an Optimum CB SJ Diode can be observed in the TLP I_d-V_{ds} curve plotted in Fig.5.18-(b). The measurements show no failure, but no higher current capability was possible due to the power limitation of the system. Contrary, no NDR is visible neither on simulated nor measured I_d-V_{ds} curves for the P_{rich} and N_{rich} cases.

The simulated V_{bd} and I_{snap} values for different CB conditions for the edge termination and periphery regions are plotted in Fig.5.19, together with the experimental

UIS test results to demonstrate the good agreement with the performed automatic measurements. The measured V_{bd} values (Fig.5.19-(a)) are topped off by the simulated V_{bd} value of the device periphery, indicating that the voltage capability of the SJ Diode is finally limited by this region. The experimental I_{AS} drop on the Optimum CB devices coincides with the simulated I_{snap} current of the periphery (Fig.5.19-(b)). The experimental I_{snap} results are topped off at 12 A due to the UIS test set-up. Accordingly, the maximum simulated I_{snap} values are set at 12 A for comparison purposes, despite the currents were much higher. Therefore, the failure presented in Fig.5.12 can be explained by the current focalization on the periphery region of the SJ Diode.

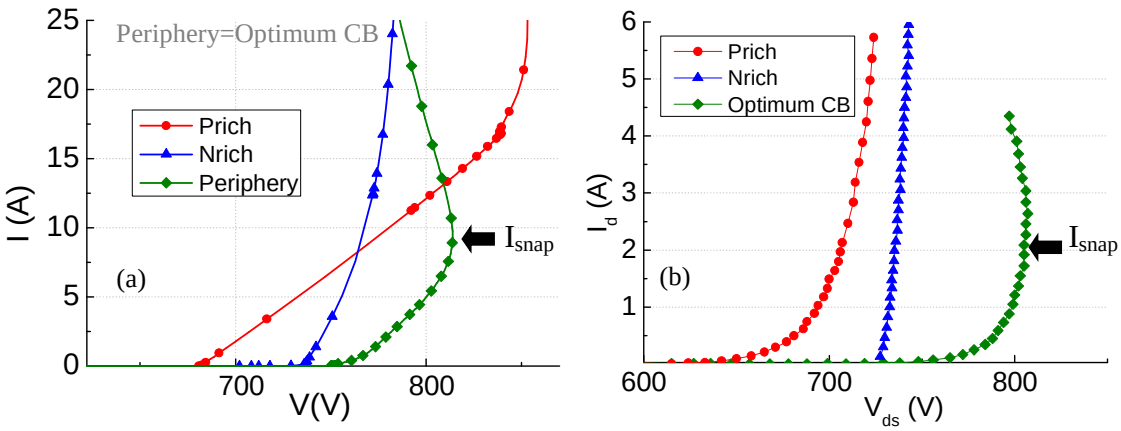

Fig.5.18. (a) Simulated isothermal I_d-V_{ds} curves for the edge termination and periphery regions and for N_{rich} and P_{rich} SJ Diodes. The scaling is done by the periphery area for the periphery case and by the active area for the P_{rich} and N_{rich} cases. (b) Experimental I_d-V_{ds} curves obtained with the TLP system SJ Diodes.

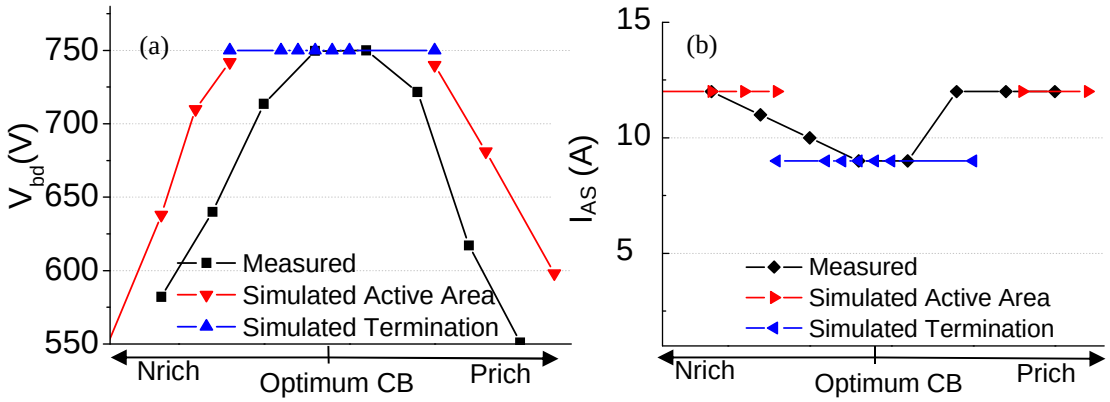

Fig.5.19. (a) Measured V_{bd} and (b) I_{AS} average values for the SJ Diodes with different CB conditions. The simulated V_{bd} and I_{snap} values for P_{rich} and N_{rich} CB SJ diodes are also plotted in (a) and (b), respectively. The simulated I_{snap} in the active area is topped off at 12 A to compare one to one with the measured values.

Taking advantage of the study on SJ Diodes, few wafers were implemented with the same process steps as the SJ Diode adding the gate trench. The aim is to demonstrate if the gate trench has any effect on the device robustness since the E_F peak for N_{rich} UltiMOS transistors is created at the top of the SJ trench and at the corner of the gate trench. The V_{bd} and E_{AS} average values for SJ Diodes with and without trench

gate and different CB conditions are plotted in Fig.5.20. The energy capabilities for N_{rich} SJ Diodes are slightly lower (see circle in Fig.5.20) since the E_F peak is also created at the gate trench region, which makes the device fail at lower current levels. This effect is due to the focalization of the avalanche current in the periphery of the device. The E_{AS} value is increased again as the voltage capability of the SJ Diodes decreases, since the avalanche is located in the whole active area and the maximum impact ionisation will be always at the top of the SJ trench for an N_{rich} SJ Diode. Conversely, the E_F peak is at the bottom of the SJ trench for P_{rich} devices, thus the gate trench does not cause any variation on the SJ Diode electrical performances.

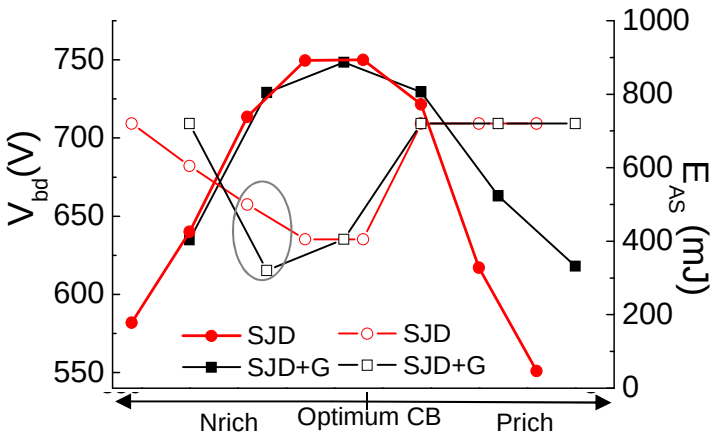

Fig.5.20. E_{AS} and V_{bd} average values for SJ Diodes with (SJD+G) and without (SJD) trench gate and different CB conditions. The average is taken from 655 devices per wafer, whereas each wafer has a different CB condition.

Summarising, the earlier failure observed in Optimum CB SJ diodes is linked to the high local current density in the periphery region. Since the Optimum CB devices are forced at a current level where the I_d-V_{ds} curve exhibits the NDR branch, current focalisation arises and failure may be triggered since no equalization mechanisms (electrical or thermal) can spread the current in a wider device area[8]. It has also been verified by 2D TCAD simulations and IR Thermography measurements that the current focalisation is the cause of failure. The gate trench slightly worsens the UIS current capability for N_{rich} SJ Diodes since the electric field is located at the top of the structure.

5.3.3. SJ Bipolar transistor

The SJ Bipolar transistor is implemented by following the same process steps as the UltiMOS transistor (detailed in appendix A), skipping the Gate Module (see cross section in Fig.5.21-(a)). The shallow N^+ diffusion is included in the structure to study if the parasitic bipolar transistor triggers at low current level, leading to the premature failure in the case of slightly N_{rich} and Optimum CB UltiMOS transistors. As concluded from the measured I_{AS} values for SJ Bipolar transistor with different CB conditions plotted in Fig.5.21-(b), the decrease of the energy capability as a function of the CB

condition follows a similar tendency as the one observed in SJ Diodes. However, the E_{AS} value of SJ Bipolar transistors is much lower (lower than 100 mJ) than that of SJ Diode counterparts (420 mJ), using a 10 mH inductor for the UIS test.

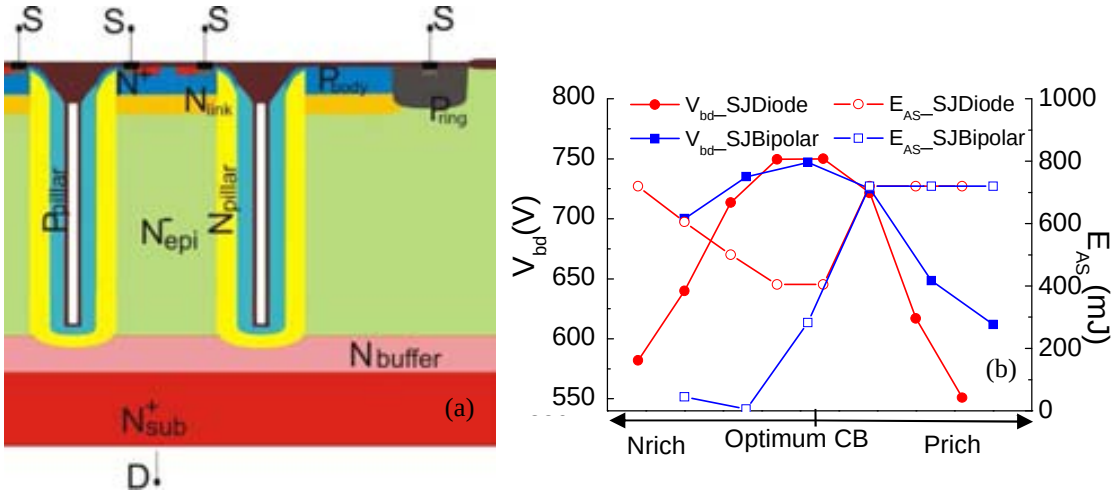

Fig.5.21. (a) Cross section of the SJ Bipolar transistor. (b) Comparison of the measured V_{bd} and E_{AS} values for SJ Diodes and SJ Bipolar transistors with different CB conditions. The plotted values are the average of 300 measured devices per split.

This difference in the experimental E_{AS} values can be explained in terms of the location of the impact ionisation process. The maximum electric field in N_{rich} devices is found at the top of the structure and, as a consequence, the parasitic bipolar transistor can be activated provided the P_{body}/N^+ junction reaches the V_{bi} value due to the hole flow under the shallow N^+ diffusion. On the other hand, the avalanche process in P_{rich} devices starts at the bottom of the structure, thus holes are not forced anymore to flow under the N^+ diffusion, creating the necessary voltage drop along the N^+/P_{body} junction to activate the parasitic bipolar transistor. This effect could explain the dependence of the energy capability with the CB condition. To confirm these statements, a first study is done to determine the region where the avalanche takes place, comparing the results with the ones obtained in SJ Diodes. Afterwards, the possibility to activate the parasitic bipolar transistor is studied by tuning the P_{body} and shallow N^+ diffusion properties.

The SJ Bipolar transistor has been measured under the same conditions as for the SJ Diodes reported in section 1.1.1 to see if the focalization also occurs in the periphery of the active area. The thermal mappings are taken at different current levels although the reported thermal images correspond always to the last measurement where the device survived the UIS test. The last captured thermal mapping for an optimum CB SJ Bipolar transistor, shown in Fig.5.22-(a), was taken before driving it into failure at 1.7 A. The current distribution is the same as for the Optimum CB SJ Diodes. The current is mainly flowing through the device periphery at the maximum avalanche driven voltage (see Fig.5.22-(b)) and the T_{max} is only 34 ºC, hinting the low current that is flowing through that region. Remember that on SJ Diodes the temperature was rising until 170 ºC for the Optimum CB case. Therefore, not only focalization is occurring on the periphery but another event makes the device to fail in that region. It is assumed from

the EMMI measurements performed on a SJ Bipolar transistor with Optimum CB condition that the highest impact ionisation is also located at the periphery of the active area (see Fig.5.23-(a)). The failure signature from the lock-in thermography is located at the same periphery region (see Fig.5.23-(b)). TLP measurements performed on P_{rich} and Optimum CB SJ Bipolar transistors are plotted in Fig.5.24. Notice that the Optimum CB device is failing before reaching 2 A. On the other hand, P_{rich} devices can handle 11 A with no failure.

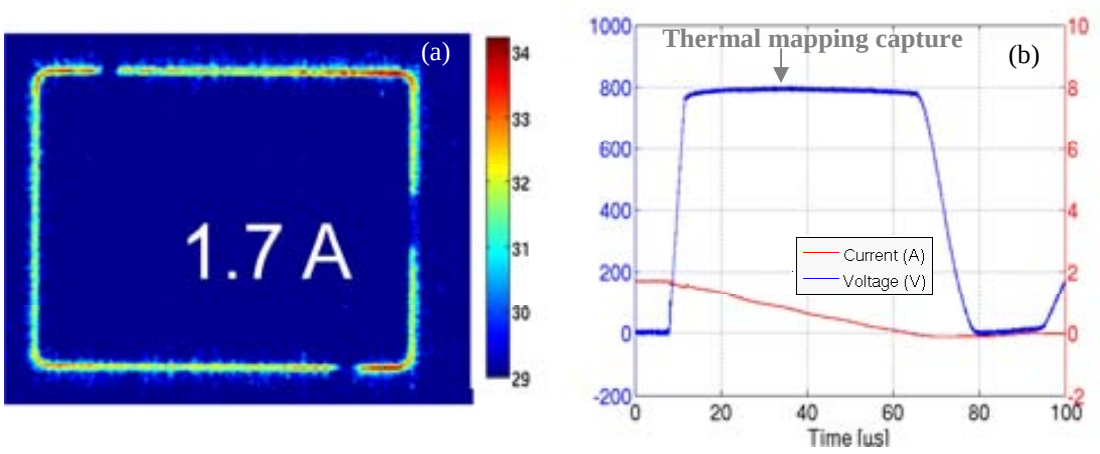

Fig.5.22. (a)Thermal mapping under an UIS pulse in an Optimum CB SJ Bipolar transistor, and (b) corresponding *I-V* waveforms during the UIS pulse. The snapshot is extracted at the maximum temperature during the 1.7A UIS pulse. Courtesy of Unina.

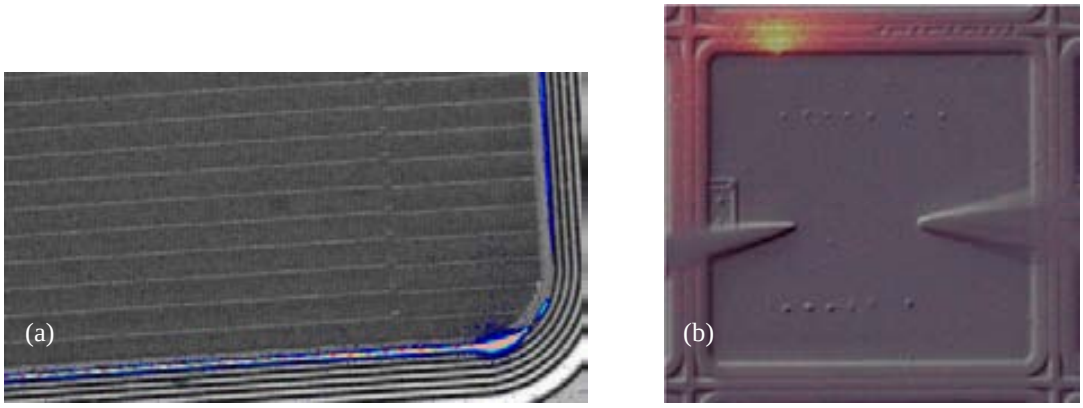

Fig.5.23. (a) Failure analysis of an Optimum CB SJ Bipolar transistor, showing the failure at the periphery. (b) Failure spot obtained by lock-in thermography, courtesy of Unina.

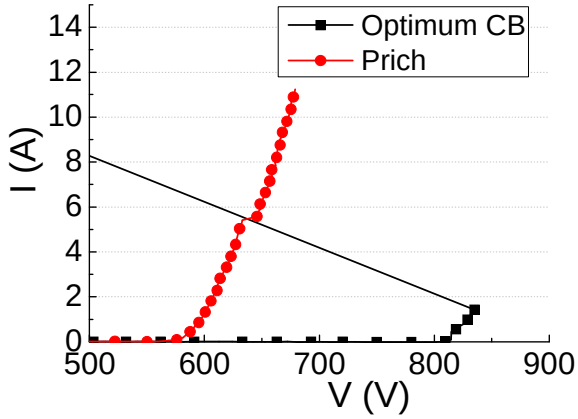

Fig.5.24. TLP measurements performed on SJ Bipolar transistors with different CB conditions.

5.4. Parasitic bipolar gain on UltiMOS transistors

The Gummel plot is a very useful tool to analyse the activation of the inherent bipolar transistor on a MOSFET device, which reflects the emitter-base (source-body) junction properties. The gain is defined as the ratio of the absolute collector current to the base current ($h_{fe}=I_c/I_b$), and it is plotted on the y axis, while the collector-emitter voltage (V_{ce}) is kept constant. The gain measures the proportion of electrons that are able to diffuse to the base and reach the collector[10]. On the x axis I_c or J_c are plotted in logarithmic scale, but in the performed study the I_c is preferred since the activation depends on the current forced by the avalanche in the MOSFET. The higher the gain, the easier is the bipolar transistor activation, thus the lower gain is preferred in the parasitic bipolar transistor inherent to the UltiMOS structure. Ideally, the gain should be loss than 1 to minimise the parasitic bipolar activation risk. The simulated Gummel confirm that the h_{fe} value is independent of the CB condition, as shown in Fig.5.26, with all the curves overlapped. However, the low E_{AS} values obtained for certain CB conditions in SJ bipolar transistors submitted to the UIS test indicate that the parasitic bipolar activation strongly depends on the impact ionisation location. On the other hand, the h_{fe} value is highly dependent on the P_{body} and N^+ implanted doses: the h_{fe} value can be reduced if the P_{body} dose is decreased and the N^+ dose is increased, as inferred from the Gummel plots in Fig.5.26 (a) and (b), respectively. However, if the P_{body} and N^+ implanted doses that give the minimum gain are selected leading to lowest h_{fe} value, the V_{TH} and the sR_{on} values would be increased, as inferred in Table 5.2. The increase of the N_{pillar}-N^-_{epi} concentration leads also to a decrease on the gain of the parasitic BJT transistor. However, it would lead in a voltage capability decrease[11].

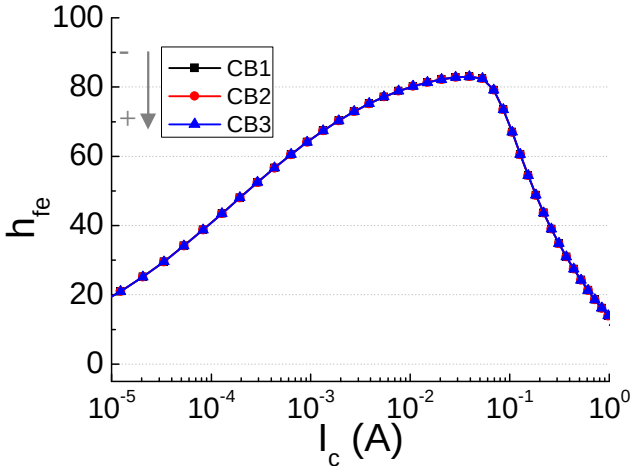

Fig.5.25. Simulated dependence of the current gain on the collector current for different CB condition (being CB1<CB2<CB3).

N^+	V_{TH} (V)	sR_{on} (mΩ)	Maximum h_{fe}
1	3.07	141	94.8
2	3.14	141.1	24.7
3	3.23	141.8	2.47
P_{body}	V_{TH} (V)	sR_{on} (mΩ)	Maximum h_{fe}
1	3.08	141	94.74
2	3.91	149.7	57.23
3	4.20	150	45.64

Table 5.2. V_{TH}, sR_{on} and maximum h_{fe} for different N^+ and P_{body} doses, being 1<2<3.

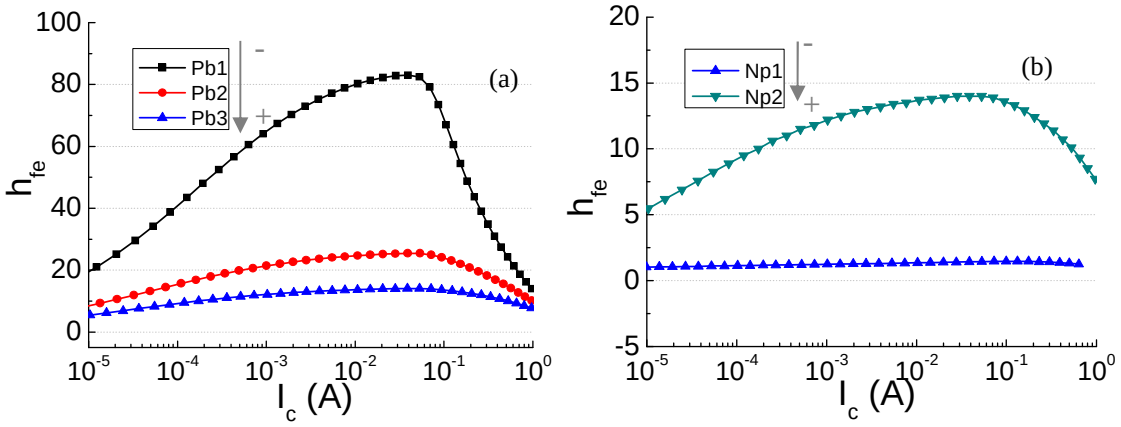

Fig.5.26. Simulated dependence of the current gain (h_{fe}) on the collector current (a) for different P_{body} doses (being Pb1<Pb2<Pb3) and (b) different N^+ doses (being Np1<Np2).

The impact of the P_{body} diffusion on the parasitic bipolar transistor activation of is studied by tuning the P_{body} dopant and dose and measuring the voltage and energy capabilities during the UIS test. The results on the UltiMOS transistors with different P_{body} doses are plotted in Fig.5.27. There are two different P_{body} dopants (Boron and BF_2). For each dopant type there are two different doses, being $P_{body}1$ dose lower than $P_{body}2$ dose. The correspondence for measured devices and doses/dopants are described in Table 5.3. When the P_{body} dose is decreased the base resistance of the bipolar transistor

increases and it is harder to be activated. As a consequence, the failure current under the UIS test shows a slight increase when higher P_{body} doses are used (cases 1 and 3) for both dopant types.

	Dopant	P_{body} dose	E_{AS} at Opt. CB(mJ)
STD	Boron	1	0
Case 1	Boron	2	150
Case 2	BF_2	1	0
Case 3	BF_2	2	0

Table 5.3. Correspondence of the P_{body} dopants and doses with the measurements plotted in Fig.5.27, and principal simulated on-state characteristics for the Boron cases.

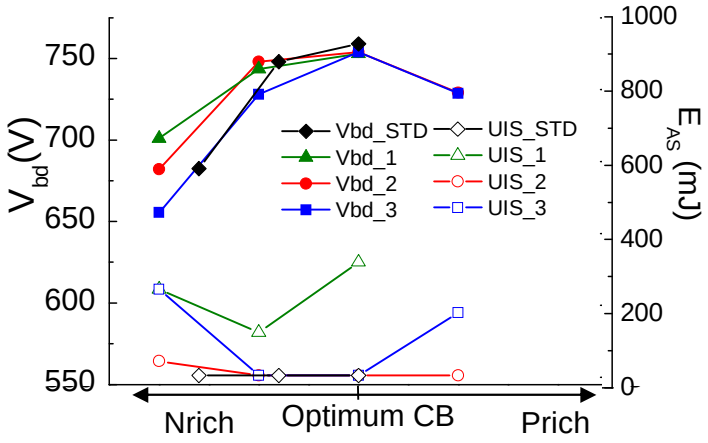

Fig.5.27. Measured V_{bd} and E_{AS} average values for different CB conditions as a function of the selected P_{body} dopants and doses. The plotted values are the average of 50 measured devices.

Finally, the shallow N^+ dose has been also tuned, using a lower dose than the reference one to decrease the gain of the parasitic bipolar transistor without degrading the V_{TH} value. Note how the energy capability improves when the lower N^+ dose is used (Fig.5.28). Therefore, a lower concentration is not feasible for the shallow N^+ diffusion to reduce the h_{fe} value.

The activation of the parasitic bipolar transistor has been proven in this section by the implementation of UltiMOS transistors with different P_{body} and N^+ implantation doping conditions. These transistors have a smaller h_{fe} as predicted from simulations, thus the activation is more difficult. The activation of the parasitic bipolar transistor happens at the edges of the active area (as deduced from the EMMI and the thermal mapping results), since the avalanche process starts at the periphery for a wide range of CB conditions. Moreover, the E_F peak for N_{rich} devices is located at the top of the structure, which in combination with the current focalization at the periphery, leads to the parasitic bipolar transistor activation. When the device is even more N_{rich}, the E_F peak is also at the top of the structure, but the current is not focalized at the periphery, thus the bipolar cannot be activated at low current levels.

Until now, the parasitic bipolar transistor formed by the $N^+/P_{body}/N_{link}$ layers has been analysed. However, the UltiMOS structure has another parasitic bipolar transistor, formed by the $N^+/P_{body}/P_{ring}/N_{epi}$, as detailed in Fig.5.29. The P_{ring} diffusion located at the edges of the device may enhance the parasitic bipolar activation since the base resistance in that region will be higher (larger current path). Therefore, less current is needed to activate the parasitic bipolar in that area. However, no study has been performed on this bipolar since the necessary layout variations were not implemented at the time of the mask set fabrication. Moreover, 3D simulations were not feasible due to the amount of computing resources needed.

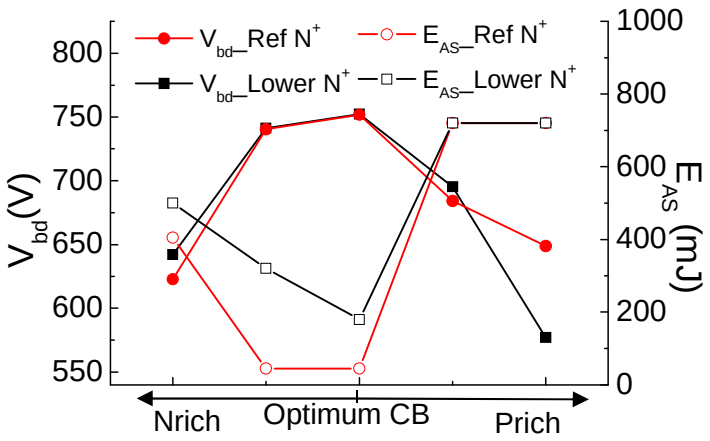

Fig.5.28. Measured V_{bd} and E_{AS} average values for different CB conditions as a function of the selected N^+ dose.

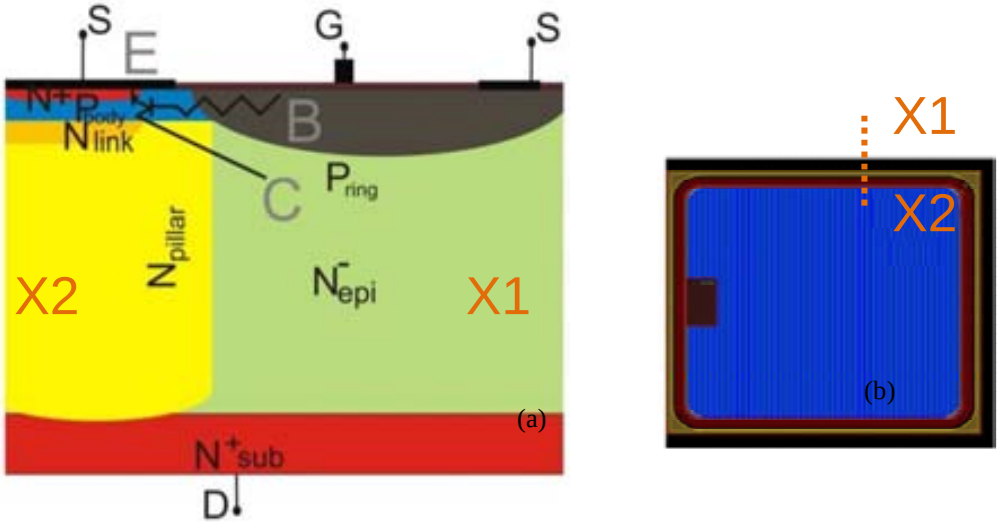

Fig.5.29. (a) Cross section of the edge of the active area and periphery regions showing the parasitic bipolar formed by the $N^+/P_{body}/P_{ring}/N^-_{epi}$ layers. (b) Top view of the layout to see where X1-X2 cross section is done.

5.5. UltiMOS transistor behaviour

The V_{bd} and the E_{AS} average values for UltiMOS transistors with different CB conditions are plotted in Fig.5.30-(a), to remind that devices with low E_{AS} values are in the range of the Optimum CB condition. The I_d-V_{ds} TLP curves are plotted in Fig.5.30-(b), where $N_{rich}1$ denotes an N_{rich} device and $P_{rich}1$ and $P_{rich}2$ denote a slightly P_{rich} and heavily P_{rich} devices, respectively. It can be observed that the V_{bd} value for the $P_{rich}1$ (775 V) and for the $P_{rich}2$ (594 V) are lower than that for the optimum CB condition (787). The current capability is determined by the CB condition, decreasing from 10 A (N_{rich} case) to 3 A (Optimum CB case). However, the current capability for $P_{rich}1$ is high (11 A although its V_{bd} value is very close to the Optimum CB case.

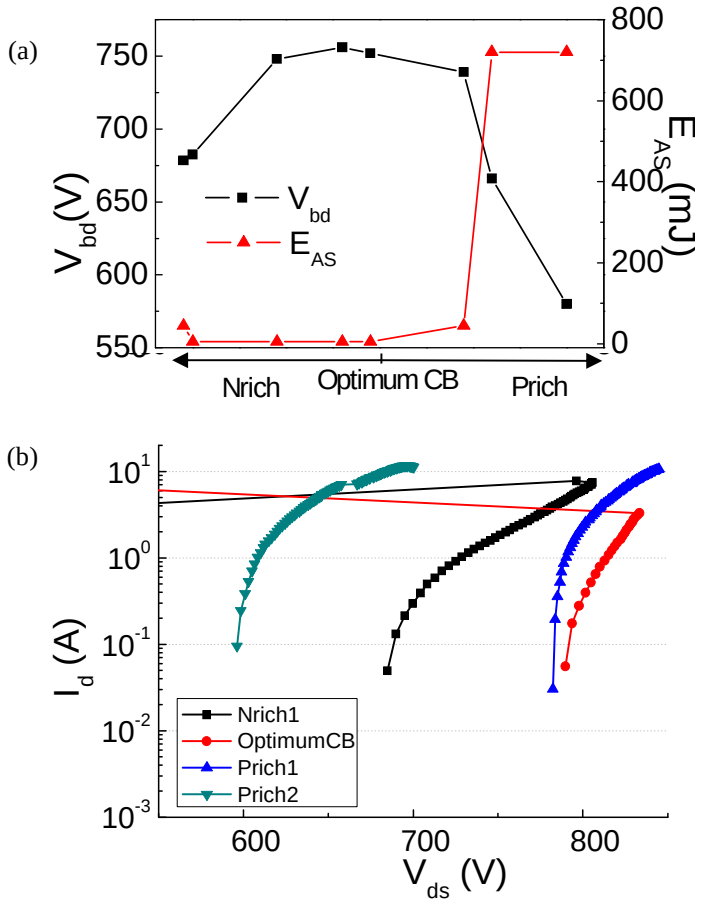

Fig.5.30. (a) Experimental V_{bd} and E_{AS} average values under the UIS test for different CB conditions. (b) TLP on UltiMOS transistors with different CB conditions.

The thermal mapping performed on UltiMOS transistors with different CB conditions and their respective *I-V* curves during the UIS pulse are plotted in Fig.5.31. All the captures are taken at 1 A lower than the failure I_{AS} value. The thermal mapping is taken at the maximum avalanche voltage in the *I-V* curve. As observed in Fig.5.31-(a), UltiMOS transistors with Optimum CB condition exhibit current focalization in the periphery region. A failure on the edge of the active area after the UIS test is shown in

Fig.5.32. Conversely, the current is spread over the active area for P_{rich} and N_{rich} counterparts, as shown in Fig.5.31-(c) and (e). The I_{AS} value indicated in the thermal images corresponds to the one obtained in the On Semiconductor facilities. However, the I_{AS} value of the UIS test *I-V* curves corresponding to the Optimum CB transistor is 6 A (Fig.5.31-(b)). This is because the gate was switched from 15 to -15 in the UIS test set-up of the University of Naples (where the thermal mapping were performed), leading to the undesired crowding of the potential lines at the bottom of the trench gate. As a consequence, the current is distributed at the trench gate bottom over the whole device, being more homogeneously distributed that if focalization in the periphery occurs, leading to a higher current capability.

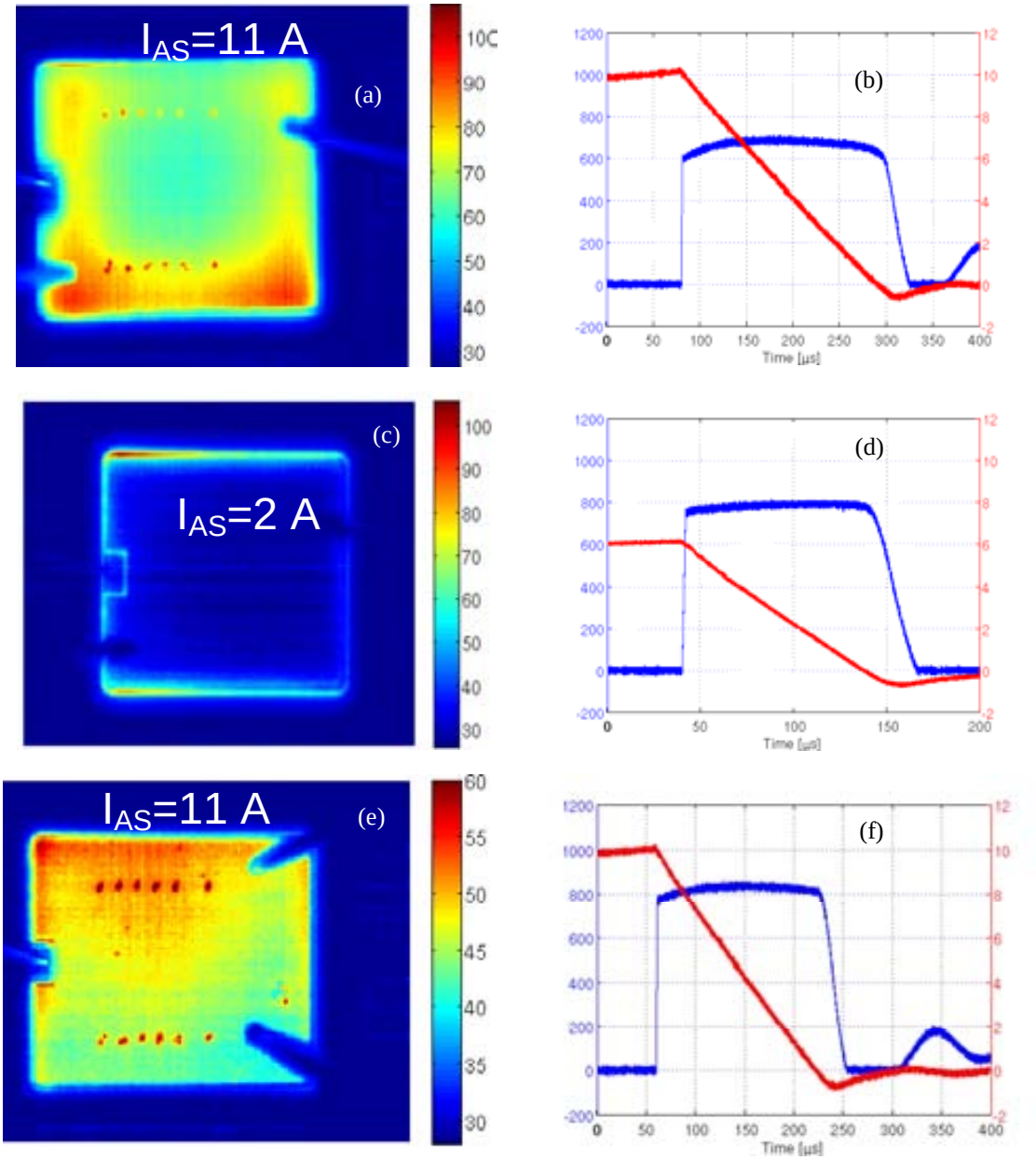

Fig.5.31. Thermal mapping of (a) N_{rich} under and 11 A UIS test, (b) Optimum CB and (c) P_{rich} SJ UltiMOS transistors. Courtesy of Unina. Indicated I_{AS} values correspond to measurements performed in the On Semiconductor facilities.

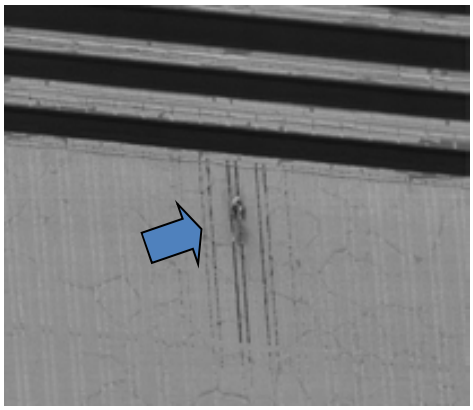

Fig.5.32. Failure on an Optimum CB UltiMOS transistor after an UIS test.

The thermal mapping for a P_{rich} device under a 13 A pulse is shown in Fig.5.33, with T_{max}= 180ºC before the thermal destruction (T_{max} corresponds to the T_{in} value of the UltiMOS transistor). Therefore, UltiMOS transistors have a limitation on the current capability given by the temperature increase when a high current pulse is applied.

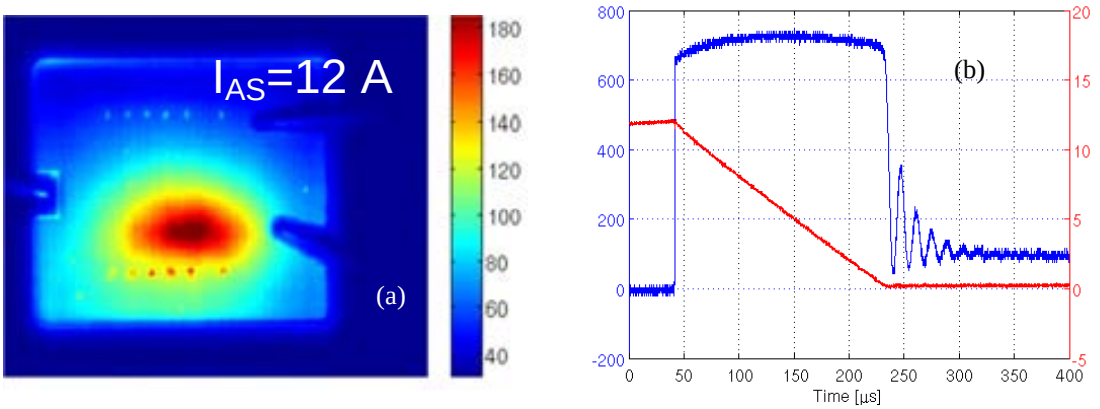

Fig.5.33. (a) Thermal mapping and (b) I-V curves during the UIS pulse for a P_{rich} device under a 12 A UIS test. Courtesy of Unina.

The temperature along the device during a 4 A TLP pulse for an Optimum CB UltiMOS transistor is plotted in Fig.5.34, with the temperature peaks located at the periphery region. TIM measures performed on a P_{rich} UltiMOS transistor are plotted in Fig.5.35, also performed under TLP stress. The measurements are taken in the active area/periphery/edge termination region and in the middle of the active area, referred as X1|X2 and X2|X3 in the layout provided in Fig.5.34-(b) (distances are not scaled). The TIM technique provides the phase shift distribution along a device, for different the pulse lengths. The negative values in the phase shift correspond to locations where the contacts are placed since the laser beam cannot be reflected in the regions where the conduction is high. Observe that the current is distributed over the active area and not over the termination (Fig.5.35-(a)), since the phase shift is zero at the edge termination region. However, the phase shift increases in the active area with the length of the applied current pulse, meaning that more current density is flowing through the device active area (Fig.5.35-(b)).

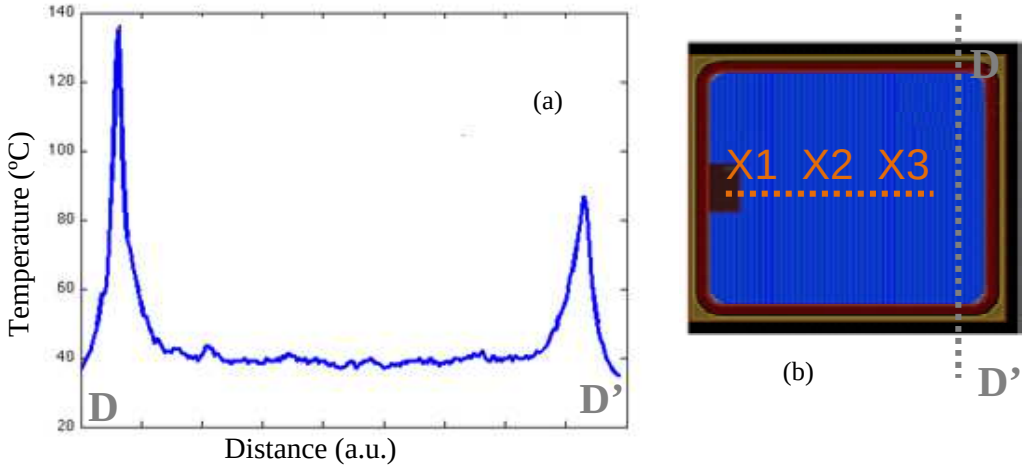

Fig.5.34. (a) Temperature distribution along an Optimum CB UltiMOS transistor on the DD' cut shown in the (b) UltiMOS layout. Courtesy of TUV.

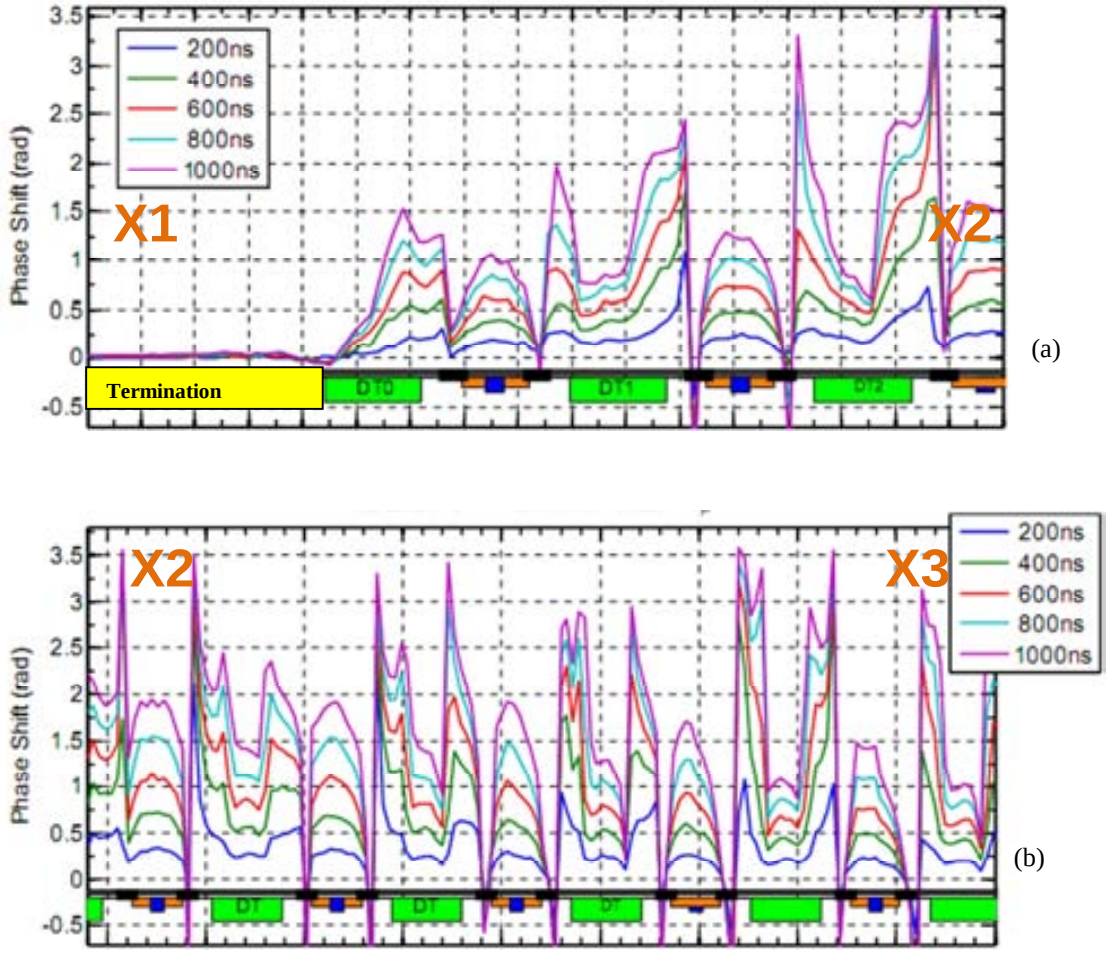

Fig.5.35. TIM measures for different 4 A TLP pulse lengths, on a P_{rich} UltiMOS transistor (a) at the edge of the active area and (b) at the center of the active area. Courtesy of TUV.

Simulated and experimental results lead to the conclusion that the poor robustness for certain CB conditions comes from the higher voltage capability of the active area compared to the edge termination one. The avalanche process starts at the

edge termination at a voltage of 750 V (section 4.4), leading to current focalization in that area. Notice the UltiMOS V_{bd} value taken at 100 µA is lower than 750 V for any CB condition, as derived from the experimental data plotted in Fig.5.30-(a). The simulated I_d-V_{ds} curves of UltiMOS transistors for different CB conditions, taking into account that all the active area is conducting, are plotted in Fig.5.36-(a). However, different scaling is considered in Fig.5.36-(b), depending on the conducting area observed in the corresponding thermal mappings. On these figures, Opt-1, Opt-2 and Opt-3 are referred as negative CB conditions (N_{rich}), whereas Opt+1, Opt+2 and Opt+3 are used for the positive CB conditions (P_{rich}). The ±1 denotes a slightly CB variation, increasing when going to ±2 and ±3. Therefore the electrical performance of UltiMOS transistors depending on the CB condition is:

- In the case of P_{rich} transistors, as the Op+1, Op+2 and Op+3 cases plotted in Fig.5.36, the current is homogeneously distributed over the whole active area, as predicted by the thermal mappings. The high E_{AS} values (even for the slight P_{rich} devices) are due to the location of impact ionisation at the bottom of the SJ trenches. As a consequence, the current can be properly spread and the focalization at the edge of the active area/periphery is avoided. In the case where the TV_{bd} value is lower than the AAV_{bd}, the self-heating on the termination decreases the impact ionisation process in that region, with the subsequent voltage capability increase with the avalanche current. Therefore, the **whole active area** is taken into account for the I_d-V_{ds} scaling for all P_{rich} devices.

- When the transistors are N_{rich} and $AAV_{bd} < TV_{bd}$, as the Op-3 case plotted in Fig.5.36, the current focalization problem is avoided. From the thermal mapping images it can be deducted that the whole active area is conducting, although the edges show a slightly higher current density due to the difficult current spread over the device (airgap inside the SJ trenches). However, as an approximation, the **whole active area** is taken into account for the I_d-V_{ds} scaling.

- Finally, when the transistors are Optimum CB or slightly N_{rich}, as in the Opt CB, Op-1 and Op-2 cases plotted in Fig.5.36, the I_d-V_{ds} curves have to be scaled by the periphery of the active area but just considering the **top and bottom regions of the active area layout** (see thermal mappings for Optimum CB condition). The sides parallel to the SJ trenches are not taken into account (low current density in the thermal mappings) since no transistor is formed on the last SJ trench of the active area. When the scaling is introduced, the NDR corresponding to the parasitic bipolar activation occurs at much lower current tan that for N_{rich} or P_{rich} CB conditions (see Fig.5.36).

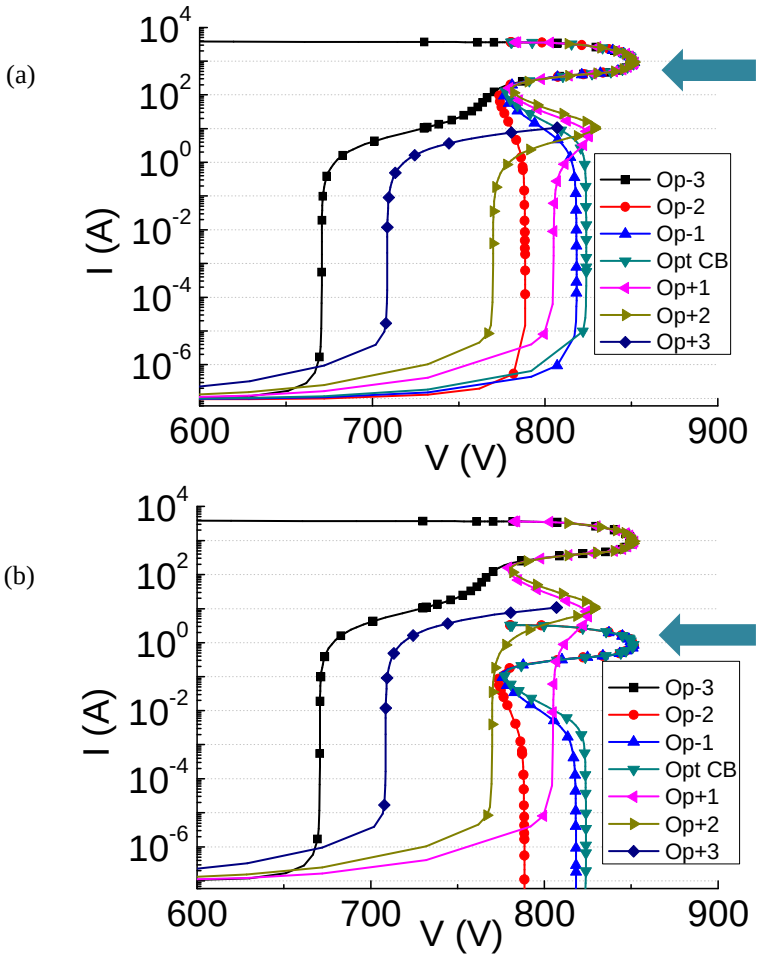

Fig.5.36. Simulated isothermal I_d-V_{ds} curves for the UltiMOS active area with different CB conditions, n (a) scaled by the whole active area and (b) scaled by the area where the current is distribute.

5.6. Summary and conclusions

The robustness of the UltiMOS transistors depends on the CB condition, as it has been demonstrated through the current capability study performed on different structures (SJ diode, UMOS transistor and SJ Bipolar). The energy capability is low for Optimum CB and N_{rich} UltiMOS transistors. When the gate is not implemented, creating a SJ Bipolar transistor, the energy capability remains low, as reported in Fig.5.37. On the other hand, when the shallow N^+ implant is skipped (implementing a SJ Diode) the energy capability is significantly improved for the Optimum CB and N_{rich} conditions. The study on SJ Diodes and SJ Bipolar transistors has demonstrated that the energy capability decrease depends on the E_F peak location. Measurements have been performed on UltiMOS transistors with different CB conditions to confirm the assessments derived from the SJ Diode and SJ Bipolar in sections 1.1.1 and 5.3.3 show that the current flows in the periphery region for the SJ Diode, SJ Bipolar and UltiMOS

transistor (see comparison in Fig.5.38). However, the current capability decreases from 9 A (SJ Diode) to 1.7-2 A (SJ Bipolar and UltiMOS transistor).

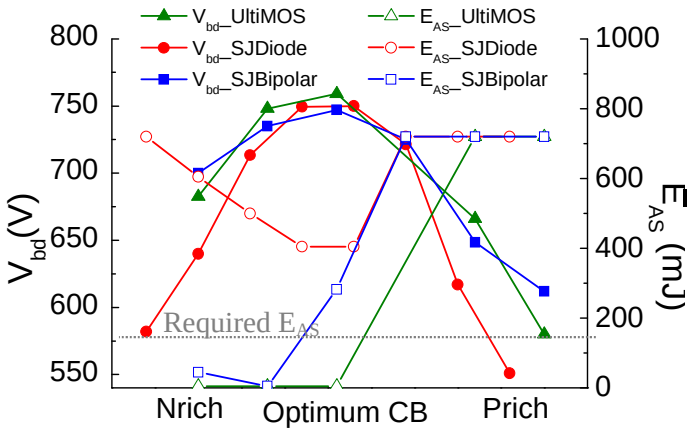

Fig.5.37. Measured V_{bd} and E_{AS} values under the UIS test for SJ MOSFET, SJ Diode and SJ Bipolar transistors with different CB conditions.

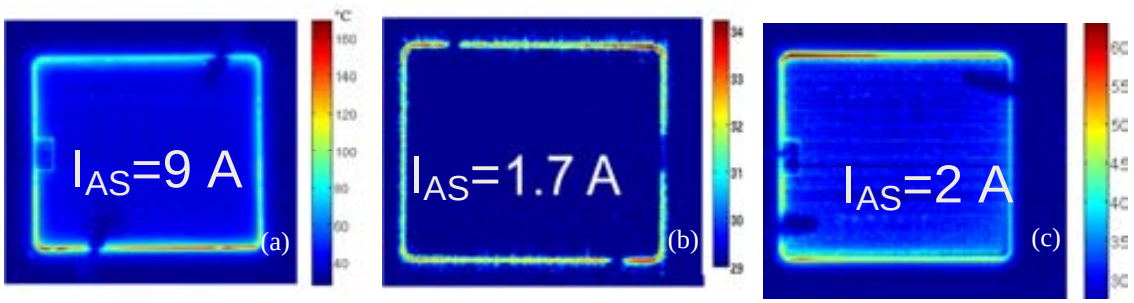

Fig.5.38. Thermal mappings on a (a) SJ Diode, (b) a SJ Bipolar transistor and (c) an UltiMOS transistor with Optimum CB condition, captured at the maximum V_{bd} value during the UIS pulse. The I_{AS} values are taken from the measurements in the On Semiconductors facilities. Courtesy of Unina.

As a conclusion, the early failure for UltiMOS transistors with N_{rich} and Optimum CB conditions has been proven to **be caused by the triggering of the parasitic bipolar transistor, enhanced by the current focalization on the periphery/edge of the active area region**. N_{rich} devices are prone to the bipolar transistor activation because the impact ionisation is located at the top of the structure, while for P_{rich} devices it is located at the bottom, far enough of the P_{body}/N_{link} junction. Therefore, different proposals to enhance the UltiMOS transistor robustness are presented on next chapter.

5.7. References

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CHAPTER 6

Robustness enhancement of UltiMOS

Two ways to improve the robustness of the UltiMOS devices are studied in this chapter, based in the electric field engineering to avoid or postpone the NDR branch in the I-V characteristics of the transistor for certain CB conditions. The first approach demonstrates that the interaction between the active area and the edge termination is crucial to handle high current levels. The second technique creates a PDR branch in the active area to sustain high avalanche current.

6.1. Introduction

It has been demonstrated in Chapter 5 that the edge termination region exhibits a lower avalanche voltage capability than the active area for certain CB conditions, leading to current focalization and device failure. Therefore, the energy capability of these particular transistors has to be enhanced to obtain a wide enough manufacturability window. In this sense, a new structure needs to be defined without degrading the target values of the main electrical characteristics as sR_{on}, V_{bd}, V_{TH}, T_{rr} or Q_g. Minimum variations on the process technology and no layout modification or new mask introduction are desirable.

This chapter is divided into three main sections:

- The study of the electrical interaction between the active area and the edge termination.
- The investigation on two different ways to enhance the robustness of the UltiMOS transistors.
- The definition of a final UltiMOS structure with all the electrical requirements fulfilled.

6.2. Interaction between Active Area and Edge Termination

The goal of this section is to understand why the current redistribution is not possible in UltiMOS transistors with certain CB conditions, leading to device failure at low current range. To this purpose, Optimum CB (with low energy capability) and P_{rich} (high energy capability) UltiMOS transistors are studied in detail to analyse the current distribution at different current levels, under different electrical stress conditions. The performance of both UltiMOS structures is compared to investigate how the current distribution should be in the Optimum CB case. The interaction between the active area and the edge termination regions is studied in each case by comparing simulated and experimental results.

Optimum CB condition

The simulated and measured results for an Optimum CB UltiMOS transistor in the off-state are plotted in Fig.6.1. This figure includes the I_d-V_{ds} isothermal simulations for the active area and the isothermal and non-isothermal *I-V* simulations for the edge termination. The edge termination *I-V* curves are scaled assuming that the current is mainly distributed in the corners, as concluded from the PiN diodes studied on Chapter 4. If self-heating in the edge termination is considered, the voltage starts to increase at certain current level (around 20 mA, red line in Fig.6.1) due to the lattice scattering that the temperature increase carries. Therefore, a higher electric field is needed to have the same current flowing through the device. Conversely, the I_d-V_{ds} curve for the active area is scaled approximately with the half of the periphery region, as was deducted from the thermal mappings reported in Fig.6.3. The first NDR on the I_d-V_{ds} active area curve is due to small variations of the electric field distribution (as described in Chapter 3). Nevertheless, 2D simulation results cannot be directly used to describe the real behaviour since the UltiMOS structure is very complex and 3D simulations should be used to provide a more accurate and qualitative results (see Appendix B). The automatic measurements plotted in Fig.6.1 show that the I_d-V_{ds} curve for a real UltiMOS transistor (750 V) has a V_{bd} value close to the simulated TV_{bd} value (721 V). Automatic and TLP measurements exhibit an increase of the voltage with the avalanche current due to the heating of the edge termination region. Notice that the slope of the TLP measurement follows the slope of the edge termination simulated isothermal *I-V* curve, corroborating that the current mainly flows through the edge termination at that range.

It can be qualitatively concluded from the TLP and the automatic measurements that the current starts flowing through the edge termination and, at a given current level, the current moves from the edge termination to the active area/periphery. However, the active area I_d-V_{ds} curve shows an NDR branch at that current level. As a consequence, although the I_{snap} is increased in the edge termination region and a PDR branch is

present, the Optimum CB UltiMOS transistors fail at a maximum current of 2 A under the TLP test. Therefore the current cannot be redistributed, leading to a current focalisation on the periphery and to the subsequent parasitic bipolar activation and device destruction.

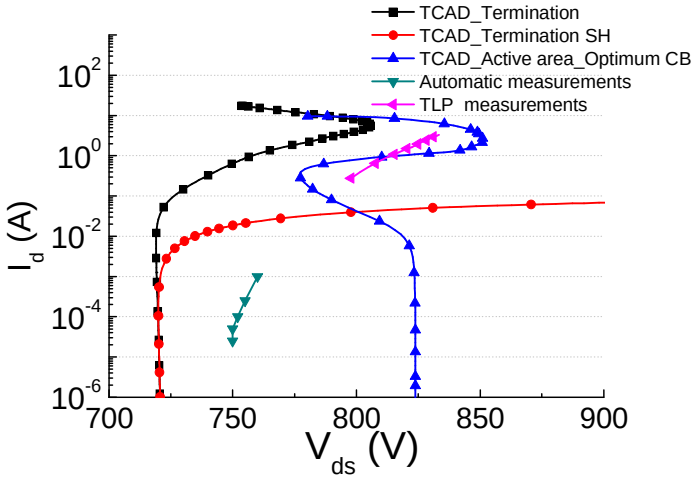

Fig.6.1. Simulated I_d-V_{ds} curves for the active area and edge termination with and without self-heating and measured I_d-V_{ds} curves, for an Optimum CB UltiMOS transistor. The device measured under TLP failed at 2 A. TCAD simulations are scaled by the periphery of the device.

P_{rich} condition

The simulated and measured I_d-V_{ds} curves for a slightly P_{rich} UltiMOS transistor are plotted in Fig.6.2, where the AAV_{bd} value is still higher than the TV_{bd} value. This CB condition should lead into current focalization at the periphery of the UltiMOS transistors. However, these devices can handle more than 780 mJ under a single avalanche UIS test. Notice that the V_{bd} value for the automatic measurements for the P_{rich} transistor in Fig.6.2 is lower (737 V) than that of the Optimum CB counterpart (750 V). The active area I_d-V_{ds} curve is scaled taking into account that the whole active area is conducting, as deducted from the thermal mappings reported in Fig.5.30. The NDR branch observed in the active area I_d-V_{ds} curve at 10 A is related with the current redistribution on the active area. However, the exact current value cannot be extracted from 2D simulations since the scaling is just approximated. The avalanche process starts in the edge termination since automatic measurements are very close to the TV_{bd} value. With increasing avalanche current, the voltage capability increases due to the heating of the edge termination region. Then, the main current path shifts to the active area with no redistribution problems since the impact ionization is placed at the bottom of the SJ trenches for P_{rich} UltiMOS transistors. Therefore, the current can be easily redistributed since the airgap in the SJ trenches does not stop the current distribution since this is done through the N_{buff} layer. P_{rich} UltiMOS transistors can handle up to 10 A under the TLP test, which is the limit of the power capability of the system.

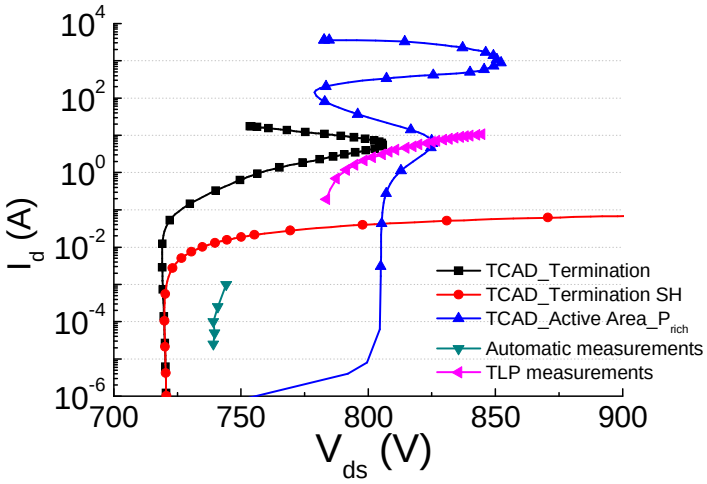

Fig.6.2. Simulated I_d-V_{ds} curves for the active area and termination with and without self-heating and measured I_d-V_{ds} curves, for a P_{rich} UltiMOS transistor. The device measured under TLP failed at 10 A. The termination curves are scaled just by the periphery whereas the active area is scaled by the whole active area.

Thermal mappings on both P_{rich} and Optimum CB devices

The thermal mappings for an Optimum CB UltiMOS transistor captured at different times during an UIS test are shown in Fig.6.3. It can be inferred that the device periphery heats up when the pulse is applied and the temperature further increases in the middle of the pulse. See that the *I-V* curve (Fig.6.5-(a)) exhibits a continuous increase of the voltage capability during the whole current decay, indicating that no transfer of the current to the active area is present. Conversely, in the thermal mappings for a P_{rich} UltiMOS transistor plotted in Fig.6.4, the current spreads in the active area with the time. See on the *I-V* curve of Fig.6.5-(b) that the voltage capability increases during the UIS test until a maximum value corresponding to 150 µs and afterwards it decreases due to the current redistribution in the active area and the subsequent device cooling. Although the current is finally spread in the active area, the avalanche process starts at the periphery since the voltage capability at the begging of the UIS test is close to the TV_{bd} value.

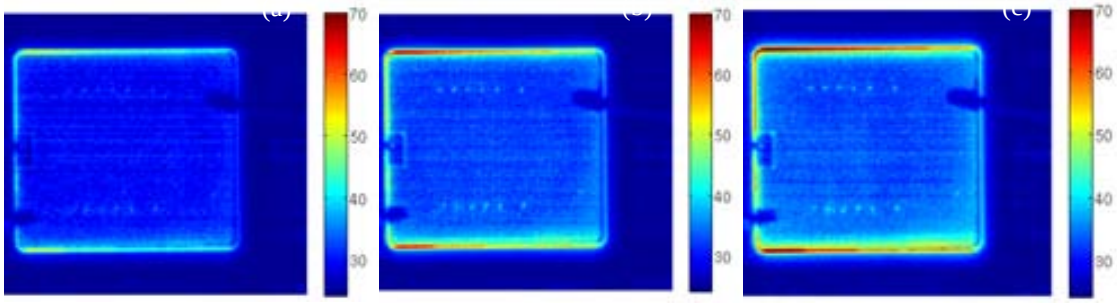

Fig.6.3. Thermal mappings for an Optimum CB UltiMOS transistor taken at (a) 50, (b) 100 and (c) 150 µs (see Fig.6.5). Courtesy of Unina.

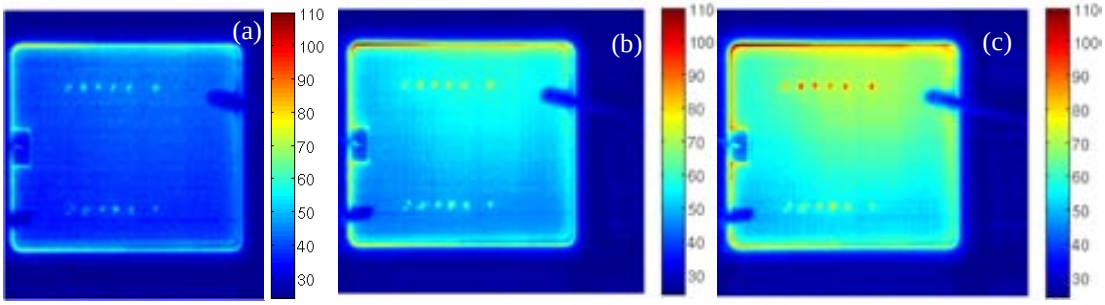

Fig.6.4. Thermal mapping for a slightly P_{rich} UltiMOS transistor taken at (a) 100, (b) 150 and (c) 200 µs (see Fig.6.5). Courtesy of Unina.

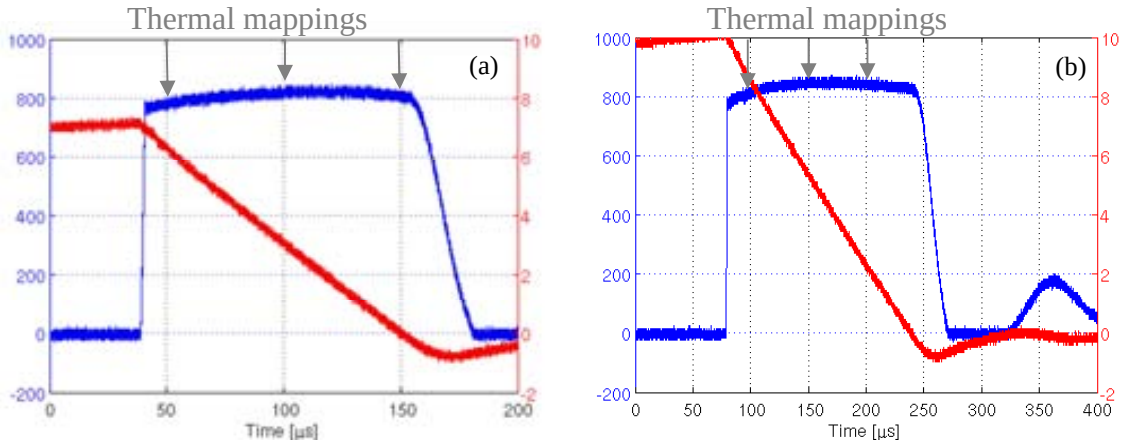

Fig.6.5. *I-V* curves during an UIS test for an (a) Optimum CB UltiMOS transistor and (b) a slightly P_{rich} counterpart. Courtesy of Unina.

The avalanche process starts at the periphery region for both CB conditions, but the current capability of P_{rich} UltiMOS transistors is much higher than that of the Optimum CB counterparts since the current can be properly redistributed in the active area. Therefore, in the Optimum CB case the active area does not play any role in the current distribution at high current range.

It can be concluded from the off-state behavior that the I_{snap} in the active area must be increased for Optimum CB UltiMOS transistors and that the current has to shift from the edge termination to the active area to flow through a larger area. Otherwise, even the I_{snap} in the active area happened at a higher current level, the current would also be focalized in the edge termination and the parasitic bipolar would activate again at 1-2 A. Therefore, the edge termination has to be designed in a way that the shift of the current is feasible, thus enlarging the PDR branch. Another possibility is the increase of the TV_{bd} value to avoid current focalization in the periphery of the UltiMOS transistors. New solutions to enhance the robustness of UltiMOS transistors are proposed and analyzed in the next section.

6.3. Proposals to enhance the robustness of UltiMOS transistors

In the previous sections, the I_{snap} value of both active area and edge termination *I-V* curves was used to quantify the improvement or degradation of the device robustness. It was correctly assumed that the higher the I_{snap} value, the later the NDR branch occurs. However, in section 6.2 it has been demonstrated that if a higher energy capability is required, a current redistribution is needed across the whole active area. It has also been determined that the active area and the edge termination cannot be treated as separated regions to optimize the energy capability of the device. However, the performed studies have been very useful for the comprehension of the electrical behaviour of the UltiMOS structure. Unfortunately, the complete 3D simulation merging the edge termination area with several active area trenches has not been performed due to the large amount of required computational resources. The interface between the two regions will modify the equipotential lines distribution on the periphery region[1]. Therefore, the measured I_d-V_{ds} curves cannot easily fit the simulated behaviour on UltiMOS transistors when the avalanche process starts in the edge termination region.

There are some requirements for the design of active area and edge termination regions that need to be taken into account:

- Active area:
  - Have a PDR branch when the shift of current is produced to let the current increase. This is equivalent of having a higher I_{snap} value on the active area.
  - Do not degrade the main electrical characteristics of the device (increase of the R_{on} or decrease of the V_{bd} values).
- Edge termination:
  - Force a larger PDR branch to be able to shift the current to the active area, even if the I_{snap} value is slightly decreased. The current should be redistributed in the active area before reaching the I_{snap} value in the edge termination.
  - Do not degrade the V_{bd} value.

In this section, the main techniques to increase the avalanche current capability on SJ MOS transistors already in production are described. Afterwards, two different techniques to enhance the energy capability of the UltiMOS transistors are proposed and implemented by using the same UltiMOS process technology, without any layout or masks modifications. The solutions are:

1. **Enlargement of the length of the PDR branch in the edge termination** in combination with the **increase of the I_{snap} on the active area**. This is feasible by tuning the N_{buff} layer properties.
2. Force a **larger PDR branch in the active area**, which is achieved by the engineering of the electric field in the structure.

6.3.1. Proposals in literature to enhance the robustness of SJ MOSFET transistors

Different solutions have been proposed to enhance the energy capability of power SJ MOSFET devices. Miyasaka[2] (from Fuji Electric Co.) studied long time ago the strong decrease of the avalanche current (from 63 A to 7 A) when the Optimum CB condition is implemented in a power SJ MOS transistor (see Fig.6.6). However, the same P_{conc} and N_{conc} is preferable for the sake of Silicon efficiency. In this section, different techniques to engineer the electric field into the Silicon volume are described and discussed.

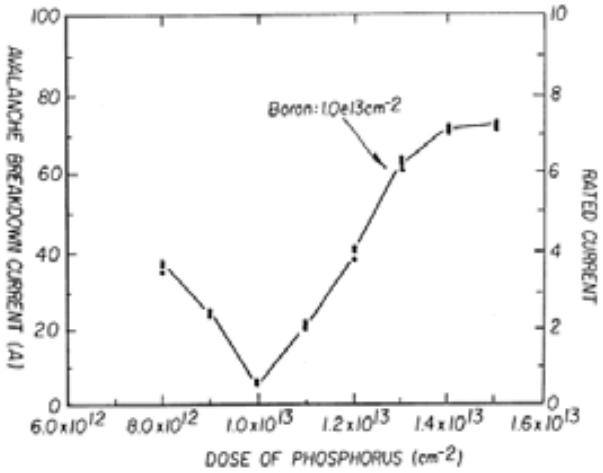

Fig.6.6. Avalanche breakdown current evolution with the Phosphorous and Boron dose of the P-N-type pillars for a power SJ transistor. Adapted from [2].

Auerbach et al.[3] (from Infineon) claims that the maximum electric field peak has to be found at the centre of the compensation regions (P-N pillars), between the top and bottom electrodes. The cross-section of the proposed solution is plotted in Fig.6.7. The goal is to keep the same CB condition along the vertical direction, but the higher doping concentration will lead in lower V_{bd} in that region (as demonstrated in section 3).

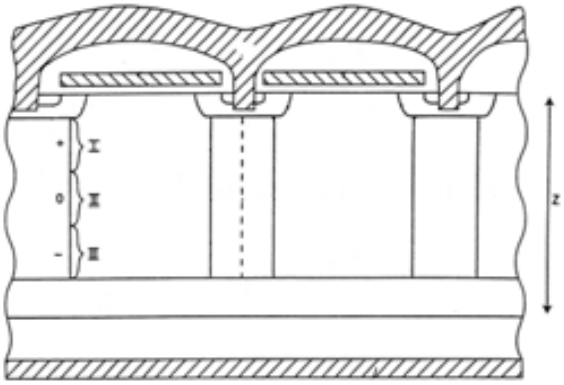

Fig.6.7. Cross section of the Auerbach solution (unbalance of both N and P pillars). Adapted from [3].

In several patents from Infineon, Deboy et al.[4,5] (from Infineon) claim that a non-uniform electric field distribution in the structure is required to have a high current capability. The different Boron implants performed during the multi-epitaxial layer growth need to have different doses to reach a non-uniform CB conditions in the structure, as inferred from **Fig.6.8-(a)**. Notice that the CB goes from a -20% to a 30% from bottom to top of the device, creating a vertical CB variation. This would be basically done to make sure that the top of the structure is not N_{rich} and the parasitic bipolar would never activate. Moreover, the current distribution in the device would be better. In the same way, Ono et al.[6] (from Toshiba) presented a power SJ structure that comprises a P-pillar where the diffused layers have lateral widths varied at certain periods along the depth (see **Fig.6.8-(b)**). Sridevan[7] (from International Rectifier) proposed a similar technique, having a thicker P-type diffusion at the top of the P-type pillar (see **Fig.6.9**). Therefore, the charge imbalance at the top of the structure is ensured, leading to a device less prone to manufacturability variations with good voltage capability and improved ruggedness.

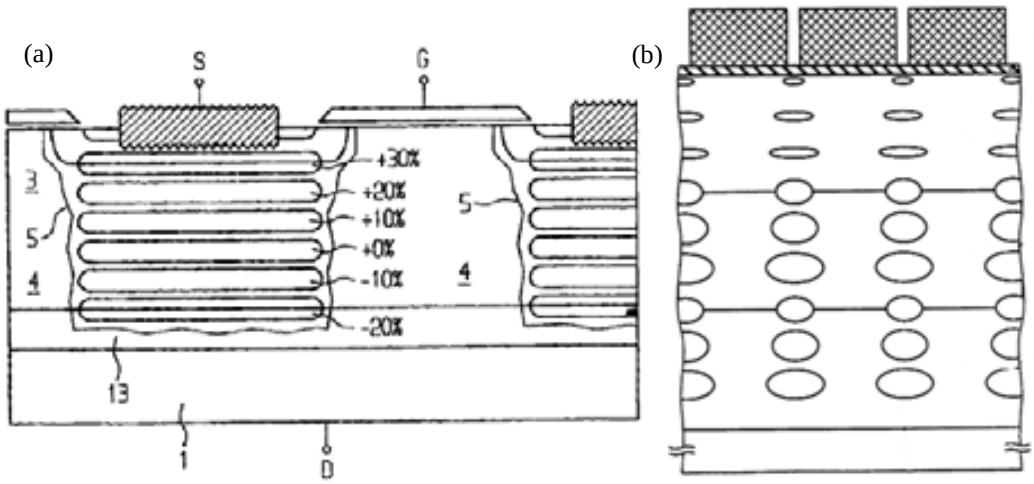

Fig.6.8. Cross section of the (a) Deboy's and (b) Ono's solutions to unbalance the P pillar. Adapted from [5] and [6], respectively.

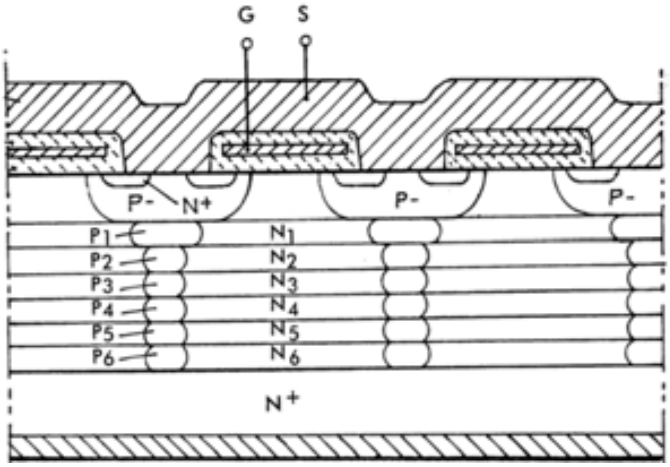

Fig.6.9. Cross section of the Sridevan's technique to implement a wider P-type diffusion at the top of the P-type pillar. Adapted from [7].

A similar solution was presented by T. Tamaki et al. [8], where tapered trenches were implemented to decrease the sR_{on} and the Q_g values. However, even there is no data on the device robustness of the device; it is similar to the previous techniques, since the top of the device will be P_{rich} and the bottom N_{rich}, re-locating the maximum electric field.

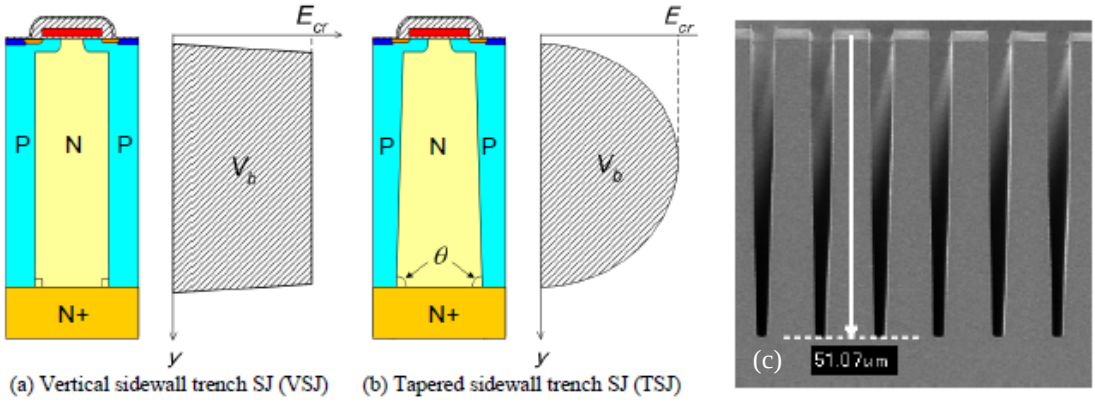

Fig.6.10. Cross section of the (a) vertical and (b) tapered trench SJ structures. (c) SEM image of the fabricated tapered trenches (right). Adapted from [8].

Finally, Saito[9] and Ono[10] presented a solution that involves an N-type buffer layer at the bottom of the P and N-type pillars that increments the E_{AS} of the SJ transistor by tuning the N_{buff} layer dose (n-$_{BAL}$) and thickness (t_{BAL}), as detailed in Fig.6.11. They present experimental UIS data with improved avalanche current capability values for an optimized N_{buff} layer.

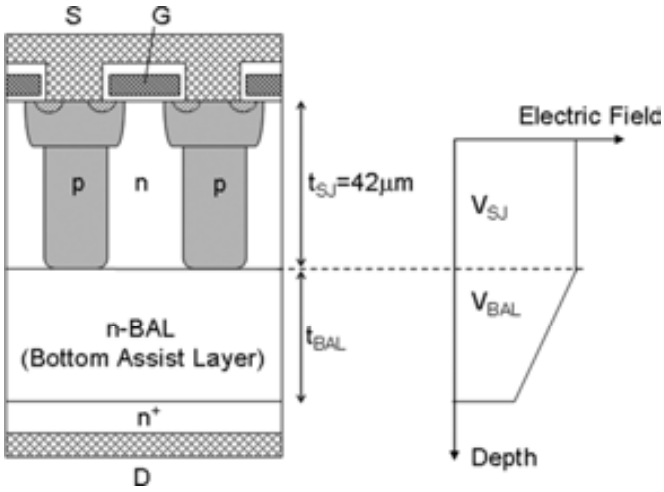

Fig.6.11. Cross section structure and schematic electric field distributions of the Saito's and Ono's technique.Adapted from [9].

Concluding, the SJ MOSFET devices in the market enhanced their robustness by engineering the electric field position in the structure, avoiding the E_F peak at the top of the structure, which would lead to the parasitic bipolar activation for certain CB conditions.

6.3.2. N_{buff} layer optimized for the Active Area and Edge Termination

As introduced, the optimized N_{buff} layer for the robustness enhancement in power devices is already reported in the literature. An N_{buff} layer with specific dose and thickness is implemented to postpone the NDR branch in power MOSFET devices[10]. It is important to remember that an N_{buff} layer has been already optimized in section 4.2 to have the highest I_{snap} value, increasing the I_{AS} of the PiN diode formed in the edge termination region. However, the N_{buff} layer needs to be re-optimized to enlarge the PDR branch to allow the current redistribution on the active area before the NDR branch on the edge termination starts. The re-optimization of the N_{buff} layer will lead to the decrease of the I_{snap} value in the edge termination. Fortunately, the I_{snap} level in the edge termination can be decreased since the current will shift to the active area at high current levels. The re-optimization can be achieved by:

- Increasing N^-_{epi} layer concentration.
- Reducing the thickness of the N_{buff} layer.
- Decreasing the N_{buff} layer concentration.

However, all these options are invasive for the electrical parameters ruled by the active area. Therefore, another way to increase the E_{AS} value for all the CB conditions has to be introduced on the UltiMOS structure.

The influence of the N_{buff} layer on the electrical performance of the active area of the reference UltiMOS transistor introduced at the end of Chapter 5 is analysed in this section. TCAD simulations are performed to optimize the concentration and thickness of the N_{buff} layer to enhance the transfer of the current from the edge termination to the active area. Finally, a new N_{buff} layer is defined, which enhances the I_{snap} level of the active area and the length of the edge termination PDR branch. The devices with the new N_{buff} layer are experimentally tested and analysed.

6.3.2.1. Simulation and experimental results

Technological and electrical TCAD simulations have been done for different CB conditions to study how the N_{buff} layer changes the device behaviour. This is done with the examination of the simulated results for N_{rich} transistors. Afterwards, the analysis of the electric field distribution in the active area for the reference N_{buff} layer and for an optimized N_{buff} layer that provides a larger PDR branch is done for Optimum CB devices.

- **Technological variations analysis**

The I_d-V_{ds} curves for the active area of two N_{rich} UltiMOS structures with different N_{buff} and N^-_{epi} layer properties are plotted in Fig.6.12. The first case (Thicker N_{buff}) corresponds to a 10% thicker N_{buff} layer than the reference. The N_{buff} layer of the second case has the same thickness as the reference but its doping concentration has been reduced by 44.4% (see Table 6.1).

- When the N_{buff} layer doping concentration decreases:
  - the V_{bd} value remains almost the same
  - PDR slope is different with a slightly lower I_{snap} value.
- When the N_{buff} layer thickness is increased:
  - the V_{bd} value increases around 70 V.
  - exactly the same PDR slope.

Therefore, the V_{bd} value is more dependent on the N_{buff} layer thickness than on its doping concentration. However, when the doping concentration of the N_{buff} layer is varied, the slope of the PDR branch changes accordingly to the new resistance, as can be spotted from the TCAD simulations.

	Reference(B1)	Thicker N_{buff}	Lower N_{buff} conc.	B2 N_{buff}	B3 N_{buff}
N_{buff} thickness	NT	NT+10%	NT	NT+10%	NT+10%
N_{buff} conc.	NB	NB	NB-44%	NB-44%	NB-66%

Table 6.1. Summary of the simulated I_d-V_{ds} curves plotted in Fig.6.12.

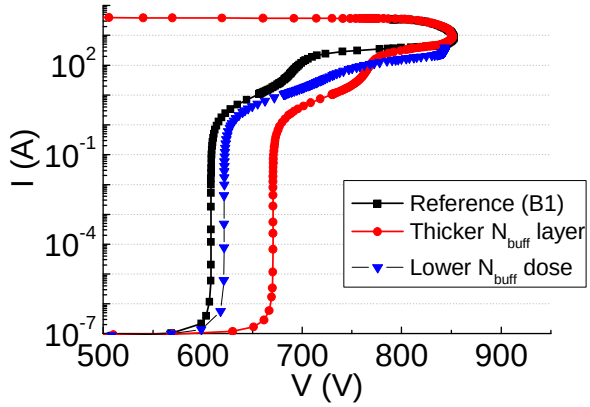

Fig.6.12. Simulated I_d-V_{ds} curves for N_{rich} UltiMOS transistors with a thicker N_{buff} and with a lower N_{buff} layer doping concentration.

- ## Electrical behaviour in Optimum CB devices with different N_{buff} layer

The simulated isothermal I_d-V_{ds} curves for the reference N_{buff} layer (B1) and for an N_{buff} layer that provides a larger PDR branch in the edge termination (B2) are plotted in Fig.6.13-(a) and Fig.6.13-(b) (edge termination and active area curves for Optimum CB structures, respectively). All the curves are scaled by the periphery of the device. The B2 N_{buff} layer has a lower doping concentration and a higher thickness (see Table 6.1) than the reference one (B1), leading to an increase of TV_{bd} value, as deducted from Fig.6.13-(a). Accordingly, the AAV_{bd} value is also slightly increased, but the PDR branch in the active area is shorter when the B2 N_{buff} layer is implemented (Fig.6.13-(b)).

The vertical electric field cuts in the active area of an Optimum CB UltiMOS transistor when B1 and B2 N_{buff} layers are used, taken in the middle of the SJ pillars, are plotted in Fig.6.14-(a) and Fig.6.14-(b), respectively. The current levels are the same for both structures, which are indicated in Fig.6.13-(b). Note that there is always an electric field peak at the N^-_{epi}/N_{buff} interface. The E_F distribution is almost the same for both N_{buff} cases at low current levels, where the slight NDR branch when the current is increased from I_1 to I_2 corresponds to the small decrease on the E_F values through the N^-_{epi} layer. The PDR branch induced by the N_{buff} layer starts at lower current level for the B2 N_{buff} layer than for B1 (60 A instead of 200 A), which is beneficial for having a PDR branch when the current is shifted to the active area. For both cases, the electric field is increased at the bottom of the N_{buff} layer (at I_3 current level for the B2 N_{buff} layer but not visible yet for the B1 N_{buff} layer). This means that the current can further increase because the N_{buff} layer can afford the expansion of electric field. For the B1 it would be visible in the range of 1000 A, since it depends on the N_{buff} concentration and thickness. See that both electric field distribution are similar at I_4, penetrating on the N^+_{sub} when the final NDR is already present, because the amount of charges induced by the impact ionization are higher than that on the active area. Therefore, even both electric fields

have a similar behaviour; the point is to have a large PDR branch in the edge termination and a small first NDR branch on the active area, to allow the movement of the current form one region to the other.

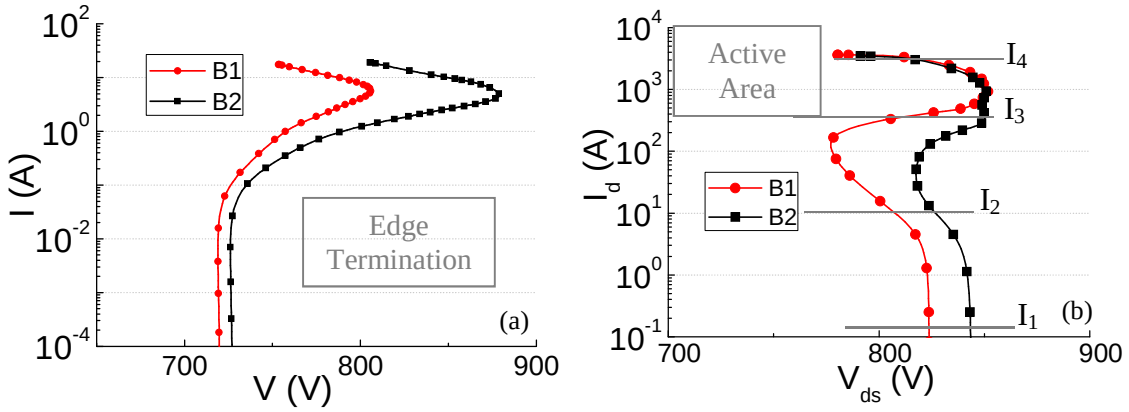

Fig.6.13. Simulated I_d-V_{ds} curves for (a) the edge termination and (b) the active area of Optimum CB UltiMOS transistors, when B1 and B2 N_{buff} layers are used (see Table.6.1 for the definition of B1 and B2 N_{buff} layers). The scaling is done for the periphery area for both (a) and (b).

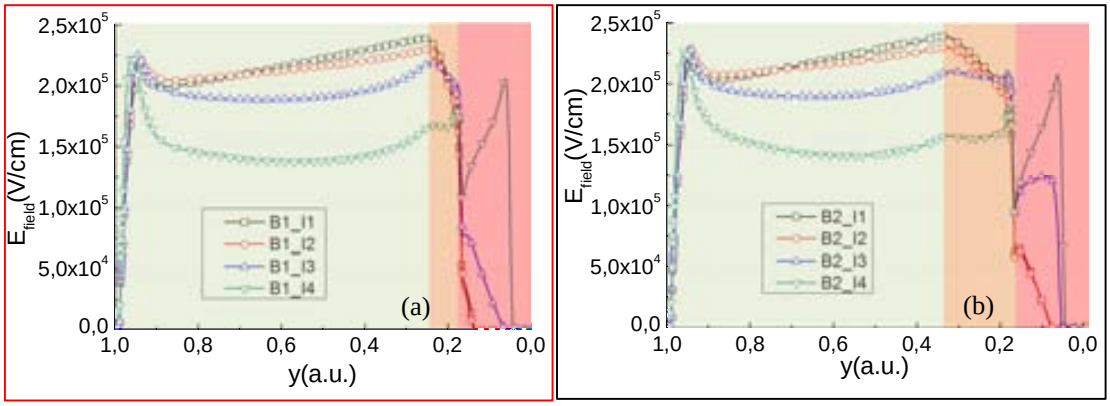

Fig.6.14. Electric field cuts for Optimum CB UltiMOS structures with (a) B1 and (b) B2, N_{buff} layers. The cuts are taken in between the SJ pillars at 1×10^{-1}, 10, 200 and 2000 A from the I_d-V_{ds} curves plotted in Fig.6.13-(b).

The isothermal I_d-V_{ds} simulated curves of the active area of an Optimum CB UltiMOS structure with the new N_{buff} layer (B2) are plotted in Fig.6.15 (see properties of the B2 N_{buff} layer in Table 6.1). The simulations of the edge termination (isothermal and including self-heating) are added in the figure. The avalanche process starts in the edge termination as in the B1 case (TV_{bd}<AAV_{bd}), following a PDR branch at high current levels. The real edge termination I-V curve will exhibit an intermediate shape between the isothermal and the non-isothermal curves. Observe that the active area can handle the hopping of the current since the I-V curves for the edge termination and active area merge at a certain current level (compare with Fig.6.1). The thermal mapping captured in Fig.6.16-(a) corresponds to an Optimum CB UltiMOS transistor with the B2 N_{buff} layer, stressed under the UIS test, captured at the maximum voltage (see curve in Fig.6.16-(b)). The avalanche process takes place mainly on the device periphery. The captured thermal mapping image is the last one before the device failed at 6 A, using a 10 mH

inductor. As a result, the current capability when the B2 N_{buff} layer is used is 3 times higher than the value obtained in the reference UltiMOS transistor.

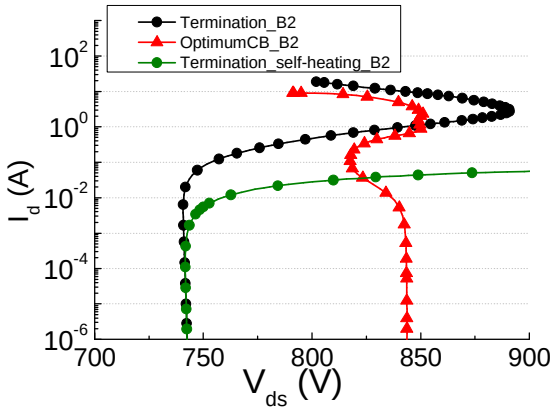

Fig.6.15. Simulated I_d-V_{ds} curves of the active area and edge termination regions, with and without self-heating, for an Optimum CB UltiMOS transistor with the new N_{buff} layer (B2).

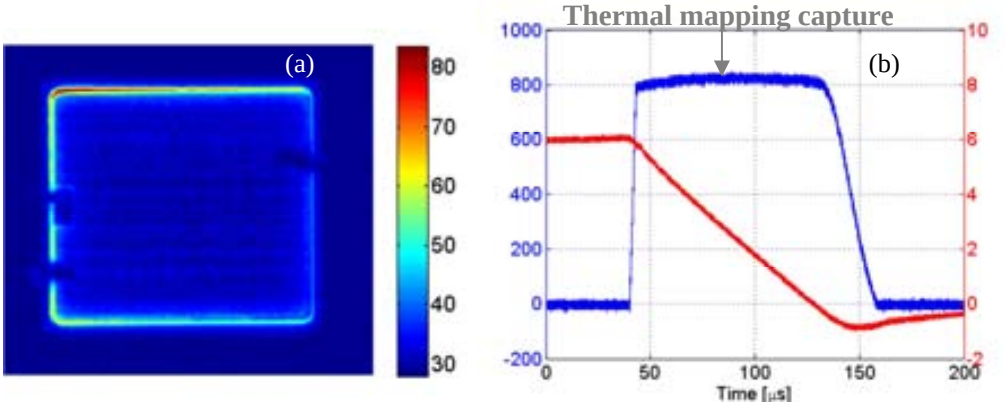

Fig.6.16. (a) Thermal mapping under the UIS pulse on an Optimum CB UltiMOS transistor where B2 is used and (b) *I-V* curves during the UIS test. Courtesy of Unina.

As already introduced, the sR_{on} value increases when the concentration of the N_{buff} layer is decreased and its thickness is increased. The measured sR_{on} values from fabricated SJ transistors with different CB conditions and N_{buff} layer characteristics are plotted in Fig.6.17. The characteristics of the three implemented N_{buff} layers are reported in Table 6.2. The average sR_{on} value is reduced by 15 %, whereas the peak V_{bd} value is reduced just a 4% when the Medium N_{buff} is used. The Higher N_{buff} case leads to a 30% reduction of the sR_{on} value and no significant degradation of the maximum V_{bd} value (1.3%) since the N^-_{epi} layer thickness has been increased a 9% and the N_{buff} layer has been decreased a 25%, compared with the lower N_{buff} case.

	Lower N_{buff}	Medium N_{buff}	Higher N_{buff}
N_{buff} conc.	a	a+50%	a+44%
N^-_{epi} thickness	b	B	b+9%
N_{buff} thickness	c	C	c-25%
sR_{on}	***d***	***d-15%***	***d-30%***

In all cases the N^-_{epi}+N_{buff} thickness remains constant

Table 6.2. Properties of the N_{buff} layers used in Fig.6.17.

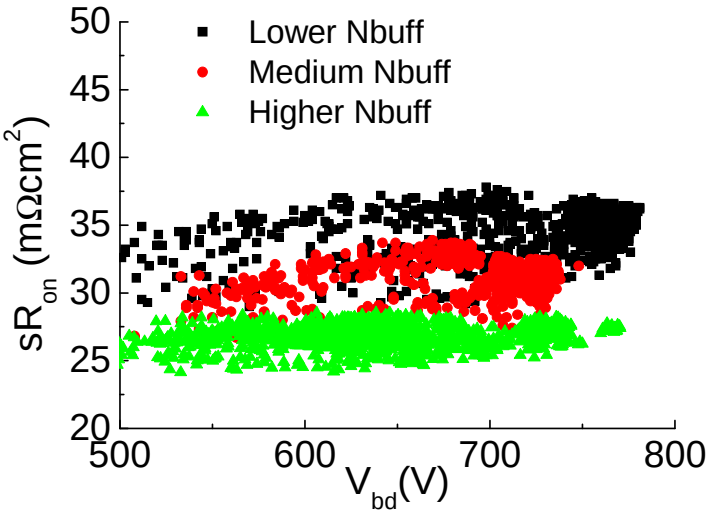

Fig.6.17. Measured sR_{on} and V_{bd} values for UltiMOS transistors with different N_{buff} layers. The high Ron values are linked to the fact that no backside metal is present for the measurement.

Concluding, the optimization of the N_{buff} layer has to be done taking into account the interaction between the edge termination and the active area of the device. It has been demonstrated that the avalanche process starts in the edge termination area for Optimum CB transistors. The current shift from the edge termination to the active area has to occur before the edge termination enters the NDR branch. Therefore, a PDR branch enlargement in the edge termination is needed. Moreover, it is required that the active area exhibits a PDR branch when the current is transferred to avoid the failure. The new N_{buff} layer needs to be designed to have a minimal degradation of the sR_{on} value.

6.3.2.2. Optimized N_{buff} layer

Finally, the N_{buff} layer has been optimized for the UltiMOS requirements. The new N_{buff} layer (B3) has a lower doping concentration than the reference N_{buff} layer, whereas the thicknesses of both N_{buff} and N^-_{epi} layers have been increased. A comparison between experimental results obtained with the optimized N_{buff} layer (B3) and those corresponding to the reference N_{buff} layer (B1) is provided in this section. The *I-V* curves corresponding to edge terminations structures implemented with B3 and B1 N_{buff} layers are plotted in Fig.6.18-(a). On the other hand, the I_d-V_{ds} curves for the active area of an Optimum CB UltiMOS structure implemented with both N_{buff} layers are plotted in Fig.6.18-(b). See that both TV_{bd} and AAV_{bd} values are higher when the B3 is used. The edge termination *I-V* curve for B3 exhibits a larger PDR branch, even the I_{snap} level has been reduced a 50% (see values in Table 6.3). On the other hand, the I_{snap} value in the active area has increased from 0.28 mA to 2.25 A. Moreover, the simulated sR_{on} value exhibits just a slightly increase from 20.4 to 22.1 $m\Omega \cdot cm^2$ with the B3 N_{buff} layer, (Fig.6.19).

	AA B1	AA B3
V_{bd} (V)	824	873
I_{snap} (A)	0.28	2.25
sR_{on} (mΩ·cm^2)	20.4	22.1

	Term B1	Term B3
V_{bd} (V)	718	740
I_{snap} (A)	16.57	8.53
PDR (V)	87	150

Table 6.3. Summary of the main electrical characteristics of the simulated I_d-V_{ds} curves plotted in Fig.6.18. The scaling is done for the periphery region for both active area and edge termination simulations.

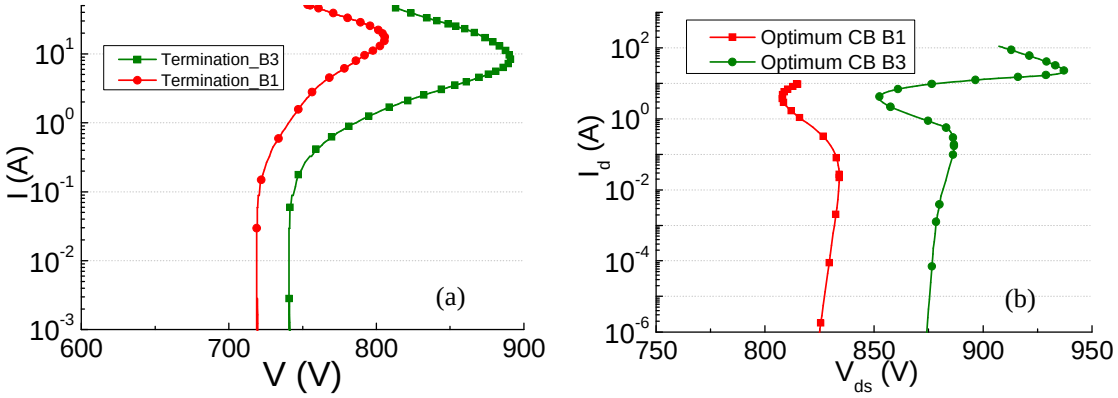

Fig.6.18. Simulated *I-V* curves for the edge termination and simulated I_d-V_{ds} curves for the active area of Optimum CB UltiMOS transistors, when B1 and B3 are implemented. The scaling is done for the periphery region for both active area and edge termination simulations.

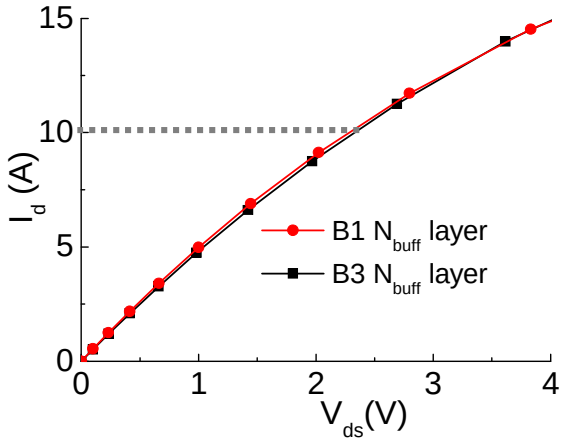

Fig.6.19. Simulated I_d-V_{ds} curves for the Optimum CB UltiMOS transistor with B1 and B3, when V_g=10 V.

The improvement of the energy capability under the UIS test can be deducted from Fig.6.20, where the E_{AS} values for Optimum CB and N_{rich} UltiMOS transistors increases from 0 to 400 mJ when the B3 N_{buff} layer is used. Notice that the E_{AS} value is above the requirements for all the CB conditions and the V_{bd} value is also increased, enhancing the margin with respect the target value defined in the device specifications (600 V). However, the optimized N_{buff} layer increases the sR_{on} value compared to that of the reference structure, as inferred from the experiments plotted in Fig.6.21.

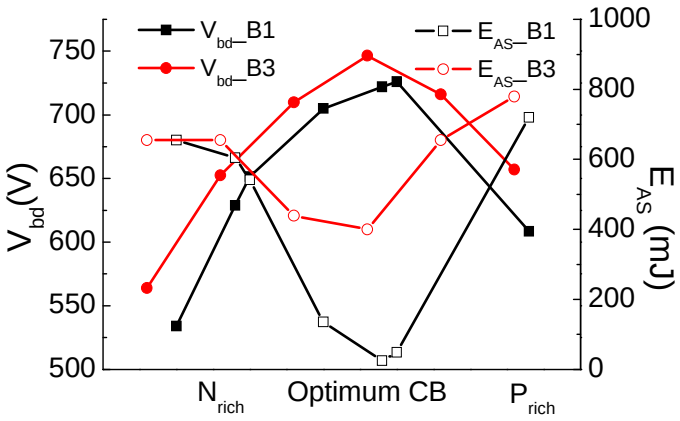

Fig.6.20. Average of measured V_{bd} and E_{AS} values for different CB conditions

	V_{bd} (V)	R_{on} (Ω)
Ref N_{buff}	667,62	0,131
Opt N_{buff}	670,78	0,158

Fig.6.21. Measured average sR_{on} and V_{bd} values for the Optimum CB UltiMOS transistor implemented with the reference and the optimized N_{buff} layers.

The thermal mappings for Optimum CB and P_{rich} UltiMOS transistors implemented with the B3 N_{buff} layer are plotted in Fig.6.22-(a) and Fig.6.22-(b), respectively. Both images are taken at a current value just before failure when a 10 mH inductor was used (6 and 11 A, respectively). Note that the heat distribution is basically focalised at the device periphery in both cases, but a current spread in the active area is observed for the P_{rich} case where the AAV_{bd} value is very close to the TV_{bd} one. This is because the maximum E_F is located at the bottom of the structure for P_{rich} UltiMOS transistors, leading to a good distribution of the current is possible even if focalization occurs. The PDR branch in the edge termination *I-V* curve for the B3 N_{buff} layer is larger than that obtained with B1, which allows the avalanche current further increase before the shift to active area takes place. However, a current redistribution for the Optimum CB UltiMOS transistor cannot be achieved since the NDR branch in the active area is present when the transfer of the current occurs.

Optimized N_{buff} layer (B3)

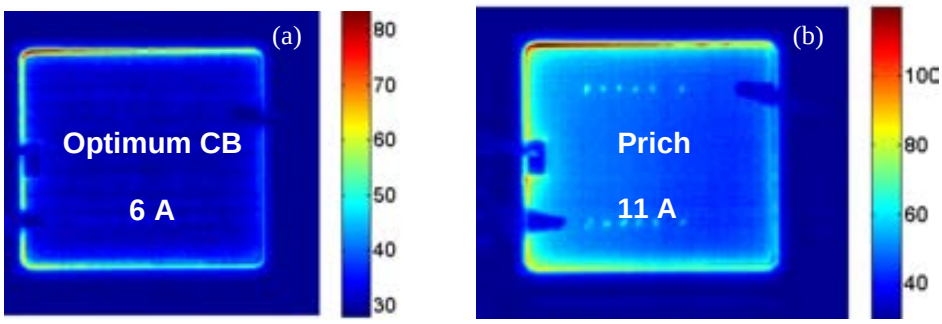

Fig.6.22. Thermal mappings on (a) Optimum CB and (b) P_{rich} UltiMOS transistors implemented with the optimized N_{buff} layer. Captures are taken at 6 and 11 A, respectively. Courtesy of Unina.

The experimental I_d-V_{ds} curves for an Optimum CB UltiMOS transistor with the reference (B1) and the optimized (B3) N_{buff} layers, measured automatically and with the TLP technique, are plotted in Fig.6.23. The isothermal simulated I_d-V_{ds} curves for the Optimum CB active area are also plotted in the same figure. The simulated curves are scaled to graphically see the effect that makes the device fail (a scale factor larger than when just the periphery is taken into account). Both experimental I_d-V_{ds} curves show an increase of the voltage with the current due to the heating of the edge termination, whereas the maximum avalanche takes place at low current levels. The last TLP captured value corresponds to the current level before the device failure. Notice that both devices failed when the current shift to the active area is imminent and the active area shows an NDR branch at that current level. The failure signature after a 6 A UIS test pulse with a 10 mH inductor is shown in Fig.6.24. The failure signature is located at the GR, at the periphery of the device, as it used to happen with the reference CB UltiMOS transistors. This supports the theory that the current is still flowing through the edge termination even the N_{buff} layer has been optimized. Therefore, next step would be to further increase the I_{snap} value for the active area to avoid the failures at this current range.

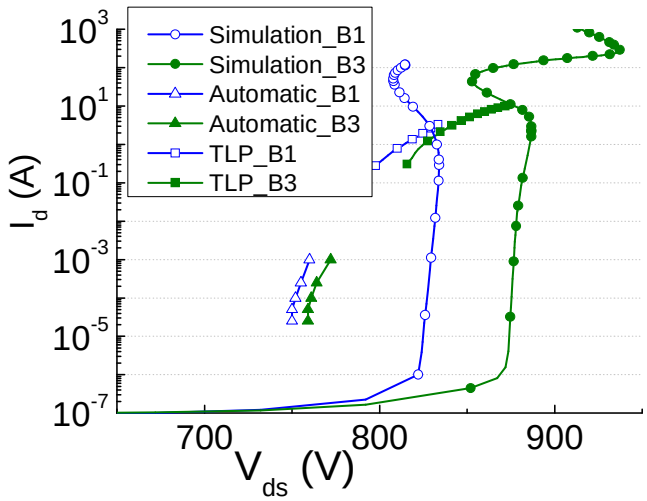

Fig.6.23. Simulated I_d-V_{ds} curves for the active area of Optimum CB UltiMOS transistors and the corresponding experimental data (automatic and TLP) for both B1 and B3 N_{buff} layers.

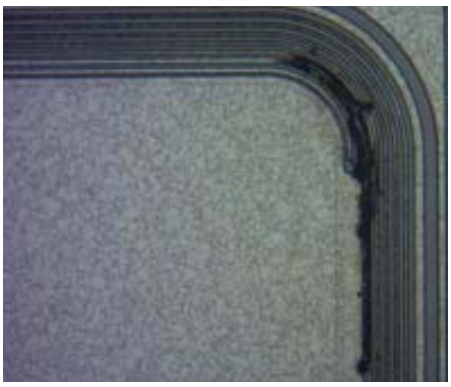

Fig.6.24. Failure image of an Optimum CB UltiMOS transistor with the B3 N_{buff} layer.

As a conclusion, even if the TV_{bd} value is still lower than the AAV_{bd} for certain CB conditions, the PDR branch in the edge termination region allows the shift of the current to the active area. However, the NDR branch in the active area has to be further postponed to higher current levels to be able to increase the energy capability of UltiMOS transistor with Optimum CB and slightly N_{rich} conditions. Even with the optimized N_{buff} layer (B3), the avalanche process starts in the edge termination region and focalization in the periphery would occur, which could activate the parasitic bipolar transistor. However, this happens at higher current levels than for the reference N_{buff} layer (B1). Variations on the P_{body} or N^+ regions should be introduced to completely asses this statement. However, the fabrication of those devices was not performed during the PhD investigation. It can be finally concluded that for this device, a larger PDR branch is more beneficial than a higher I_{snap} value in the edge termination for the device robustness point of view.

6.3.3. Forcing a PDR branch in the Active area

Up to now it has been observed that the avalanche process for Optimum CB transistors is always focalized in the periphery of the device, even if the energy capability of that region is increased, with the failure signature located at the GR area. The goal of this new study is to move the E_F peak far away from the P_{body}-N_{link} junction to avoid the activation of the parasitic bipolar transistor when the current shifts from the edge termination to the active area. It has been demonstrated that the E_F peak is placed right at the bottom of the $P_{connection}$ diffusion (**Fig.6.25-(b)**) performed to avoid a floating P-type pillar layer, in the case of Optimum CB and N_{rich} transistors where the E_F peak is at the top of the SJ trench. Moreover, the E_F peak can move to another region in the Silicon when different technological parameters of the $P_{connection}$ Module (see Appendix A) are varied. Therefore, a re-location of the E_F peak is feasible by tuning the $P_{connection}$ Module parameters (liner oxidation thicknesses, implant angle, etc.). In this section, the physical principle of the E_F peak relocation and the impact on the electrical performance of the SJ power transistors are first presented. It is confirmed how the E_F peak location can be moved to different regions at the top of the Silicon with just tuning the $P_{connection}$ Module characteristics. At the end of the section, an optimized $P_{connection}$ Module is presented to implement UltiMOS transistors with higher energy capability. Finally, an additional section is included to discuss on the ways to improve the robustness of the SJ MOSFET transistors reported in literature since the robustness was a weakness for all SJ MOSFETs in the market.

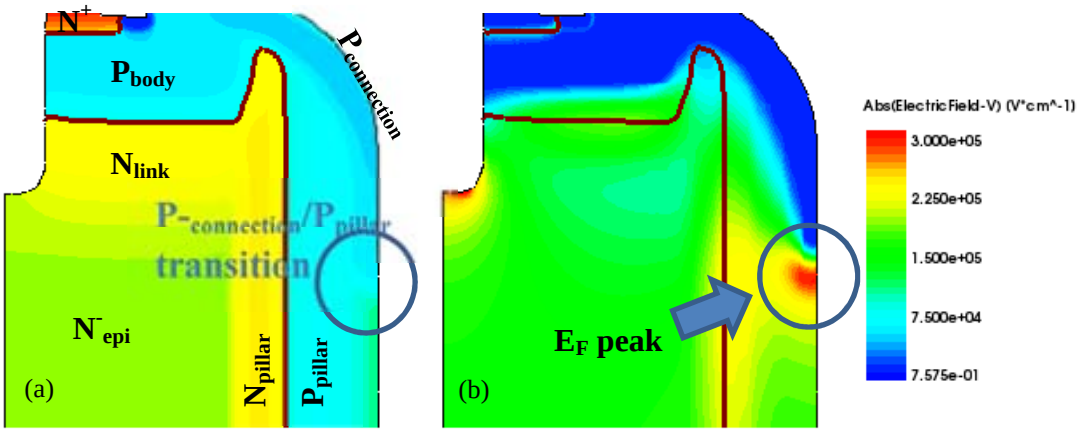

Fig.6.25. (a) Cross section of the top of the UltiMOS transistor and (b) electric field distribution at the same region, when the device is in avalanche.

6.3.3.1. Simulation results

The simulated I_d-V_{ds} isothermal curves for different CB conditions in UltiMOS transistors implemented with the standard $P_{connection}$ Module (reference UltiMOS) are plotted in Fig.6.26-(a). Notice that the I_d-V_{ds} curves show a first NDR branch before entering the PDR branch induced by the N_{buff} layer (Fig.6.26-(a)), as it has been described in section 6.3.1. In that section it was stated that the electric field increase at high current levels in some region of the structure (like in the N_{buff} layer) is beneficial for the energy capability. A similar idea can be applied to the optimization of the $P_{connection}$ Module. Observe that the E_F exhibits a maximum at the $P_{connection}/P_{pillar}$ transition is in the range of $2.3x10^5$ V/cm for a current level of 0.18 A (Fig.6.27-(b), Fig.6.28-(b) and Fig.6.29-(b)). The electric field could be further increased at the top of the structure if the $P_{connection}$/P-type pillar transition is modified by tuning the $P_{connection}$ Module and if the E_F peak is moved to a deeper region in the Silicon.

The simulated I_d-V_{ds} isothermal curves for different CB conditions when the modified $P_{connection}$ Module is used are plotted in Fig.6.26-(b). Notice that, in contrast with the reference counterparts, no NDR branch is visible for any of the different CB conditions. The small bump present on the PDR branch at the 100 A range is related to extension of the electric field into the N_{buff} layer. The vertical electric field cuts taken at the junction between the P and the N-type pillars for reference and modified $P_{conection}$ UltiMOS transistors are plotted in Fig.6.27-Fig.6.29. Note that the electric field in the N_{buff} layer (R3 region in Fig.6.27) increases with the avalanche current, as described in 6.3.1. However, there is also an increase of the electric field at the top of the structure, between the top of the device and the point where the E_F peak is reached (R1 region). It is important to note that the E_F peak at I_{ds}=9× 10^{-8} A (close to 2× 10^5 V/cm), placed at the interface between R1 and R2 regions (where R2 is the region between the E_F peak and the N_{buff} layer), in the case of modified $P_{connection}$ transistors, is similar than that of the reference counterparts at the same current range. However, the electric field

increases with the current in the R2 and R1 regions when the $P_{connection}$ Module is modified, for any CB condition. The electric field increase at the top region of the structure induces a PRD branch at the current range where an NDR branch was present for the reference UltiMOS, although the NDR branch is not visible for the plotted I_d-V_{ds} curve. However, if a slightly N_{rich} CB condition is selected, the I_d-V_{ds} curve will also show the first NDR branch. Thus, the relevance of the $P_{connection}$ implant relies on the possibility to determine the position where there is a balance of the E_F distribution along the y direction (R1/R2 interface). Moreover, the modification of the $P_{connection}$ Module does not degrade the sR_{on} value, conversely to the N_{buff} layer optimization case.

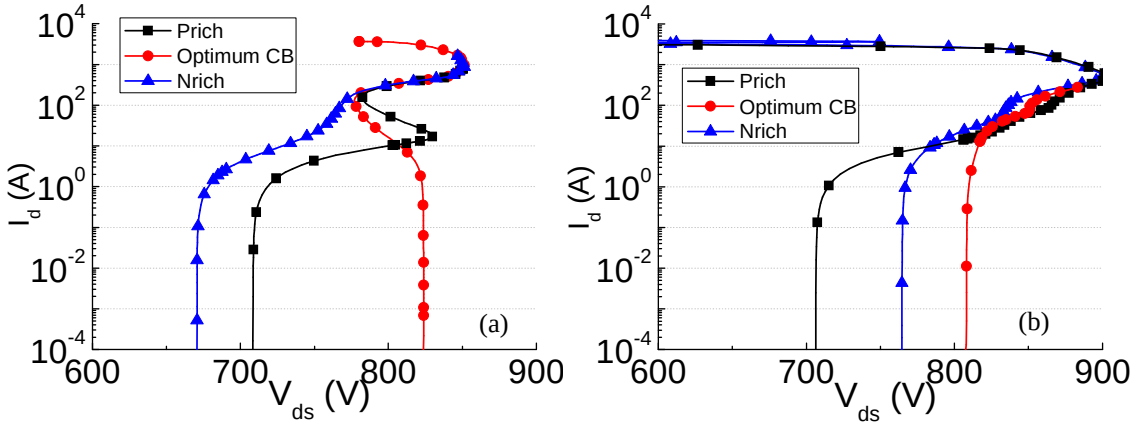

Fig.6.26. Simulated I_d-V_{ds} curves for the active area for (a) the reference UltiMOS transistors and (b) with the modified $P_{connection}$ Module.

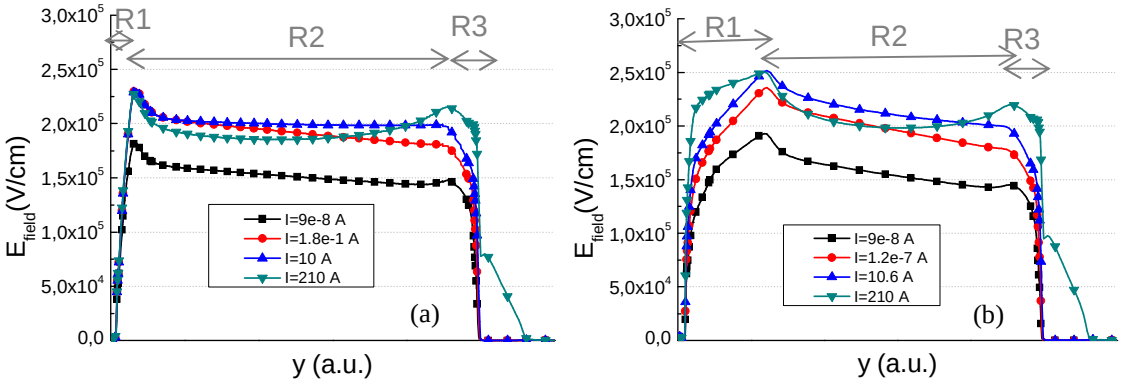

Fig.6.27. Vertical electric field cuts in the region between the P and the N-type pillars for N_{rich} (a) reference UltiMOS transistors and (b) with the modified $P_{connection}$ Module.

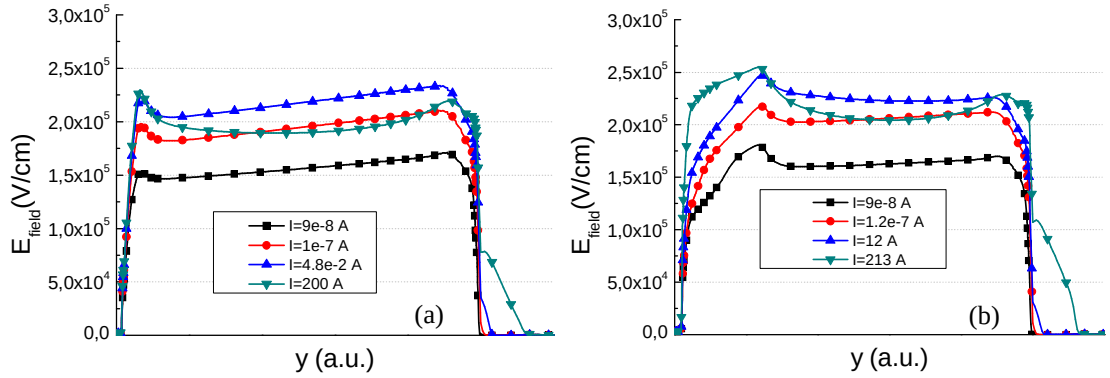

Fig.6.28. Vertical electric field cuts in the region between the P and the N-type pillars for Optimum CB (a) reference UltiMOS transistors and (b) with the modified $P_{connection}$ Module.

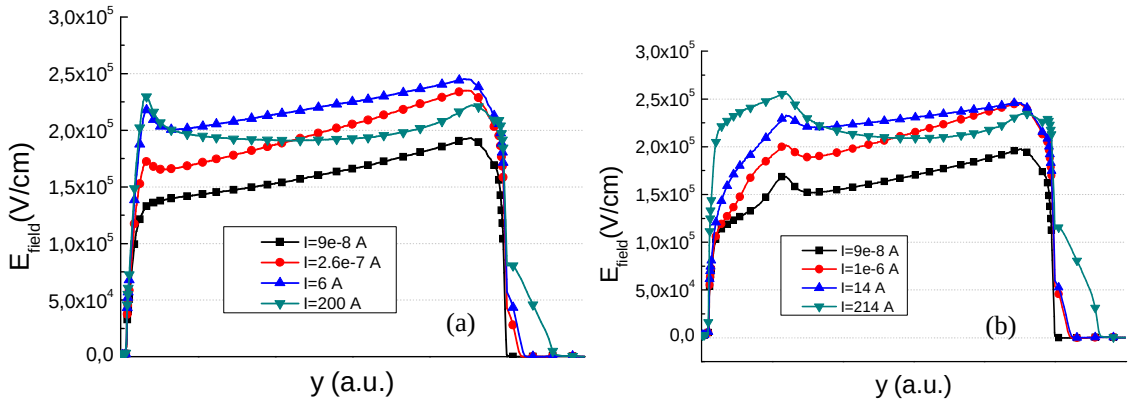

Fig.6.29. Vertical electric field cuts in the region between the P and the N-type pillars for P_{rich} (a) reference UltiMOS transistors and (b) with the modified $P_{connection}$ Module.

As studied in previous sections, the NDR branch observed in the *I-V* characteristics of the edge termination corresponding to the reference UltiMOS transistors starts before the current can be spread on the active area. However, since the active area shows a larger PDR branch when the $P_{connection}$ Module is modified, the current can be shifted to the active area without device destruction.

6.3.3.2. Technological variations

Different studies have been carried out during the optimization of the $P_{connection}$ implant, focussed on the implantation and diffusion of the P-type dopant at the top of the SJ trenches.

- **Pconnection implant angle**

The P-type implant angle is a very sensible parameter for the robustness of the UltiMOS transistor since it determines how deep in the Silicon the implant will penetrate. The evolution of the vertical CB condition at the top of the structure (referred to the vertical axis) for different implant angles is plotted in Fig.6.30-(a), being A1<A2<A3<A4. The lower the angle, the deeper in the vertical direction the implant goes, and the smoother is the transition between the $P_{connection}$ layer and the P-type pillar. Notice that when the angle is increased from A2 to A3 (A3/A2=1.43) the diffusion reaches almost the double of the depth (see also Fig.6.30-(b)). The implant depth in the horizontal direction (indicated as x axis in Fig.6.30-(b)) is just slighty modified with the angle, but it can be easily tuned with the implantation energy, as detailed in next sections.

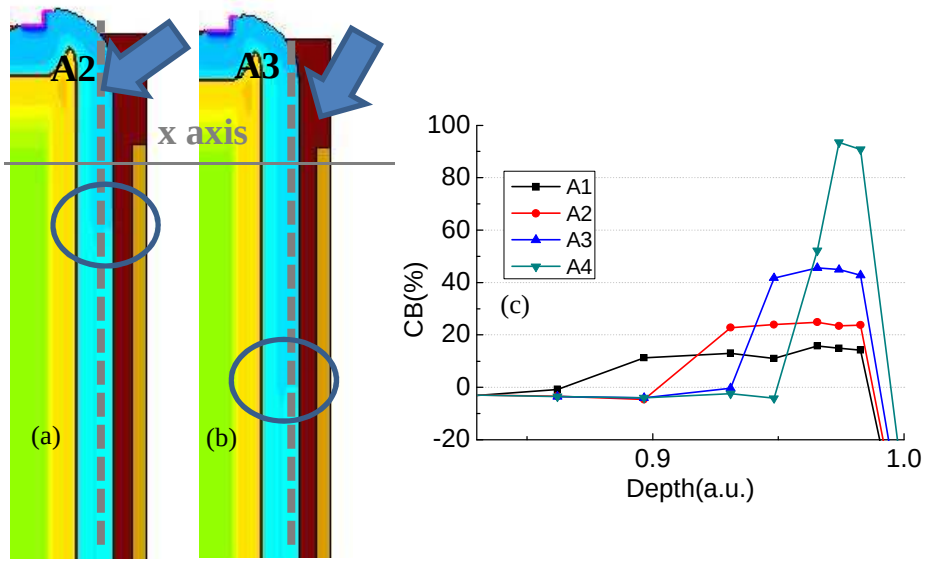

Fig.6.30. Cross-section of the UltiMOS transistors with (a) A2 and (b) A3 implantation angles, with A2>A3. The circles in the cross-section indicate the end of the $P_{connection}$ diffusion, which varies with the implantation angle. (c) Simulated vertical CB condition with A1>A2>A3>A4. The dashed lines in (a) and (b) indicate where the CB condition is extracted.

- ## Pconnection implant dose

The simulated vertical CB evolution for different P-type implanted doses is plotted in Fig.6.31-(a). The CB condition increases to positive values (P_{rich}) with the dose, but the P-type pillar/$P_{connection}$ transition is in the same location. Therefore, when the implanted dose is increased, the E_F peak will not move deeper into the Silicon, but the transition between the two P-type regions will be sharper and the critical E_F value will be reached at a lower current level. Therefore, the V_{bd} increases for N_{rich} devices with the dose (see Fig.6.31-(b)). This effect is because the D4 dose level is closer to the optimum dose to get the optimum R1 region where the electric field can further increase.

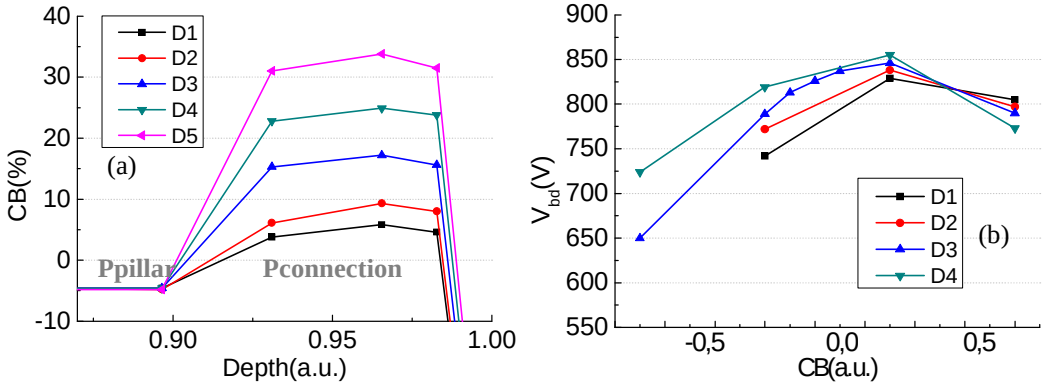

Fig.6.31. Simulated (a) vertical CB evolution and (b) V_{bd}-CB evolution for different P-type implant doses, being D1<D2<D3<D4<D5.

- **Pconnection implant energy**

The P-type doping concentration in the structure for different energy values (*E1*, *E2* and *E3* keV, being *E2* and *E3* the double and triple of *E1*, respectively) is plotted in Fig.6.32. See that the penetration of the P-type dopant into the protection oxide at the top of the N^+ and P_{body} diffusions increases with the implantation energy. This effect is also present in the top corner of the SJ trench, where the P-type implant connects the P_{body} to the P-type pillar. The increased penetration of the implanted P-type dopant at high energy levels can be inferred from the vertical CB evolution at the top of the device (see Fig.6.33-(a)). It is observed that the CB is also higher when the *E3* energy is used, but it is worth to say that if the cut in the x axis is done more close to the oxide, the *E2* energy would have the higher CB. From previous sections, it was already demonstrated that the increase of CB is due to the increase of implant dose or the variation of the implant angle. A higher energy leads to a lower maximum V_{bd}, as shown in the V_{bd}-CB curve plotted in Fig.6.33-(b), since the $P_{connection}$ implant goes deeper in the Silicon, moving the electric field peak location. Therefore, when the energy is varied, the dose and the angle of the $P_{connection}$ implant should be tuned again.

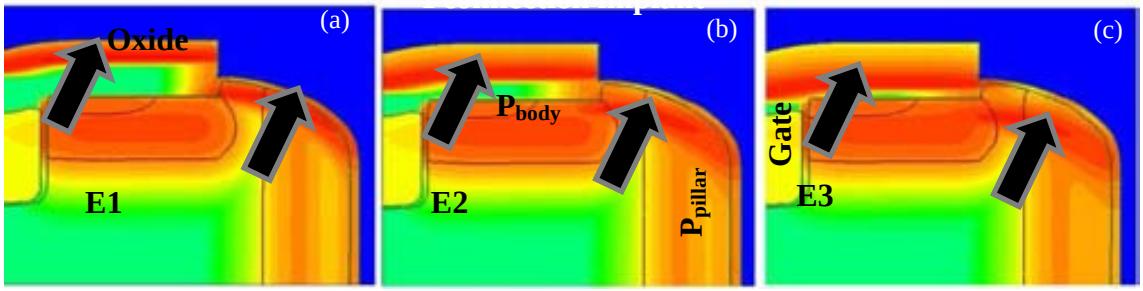

Fig.6.32. P-type doping concentration at the top of the UltiMOS structure when (a) E1, (b) E2 and (c) E3, implantation energies are used, being E1<E2<E3.

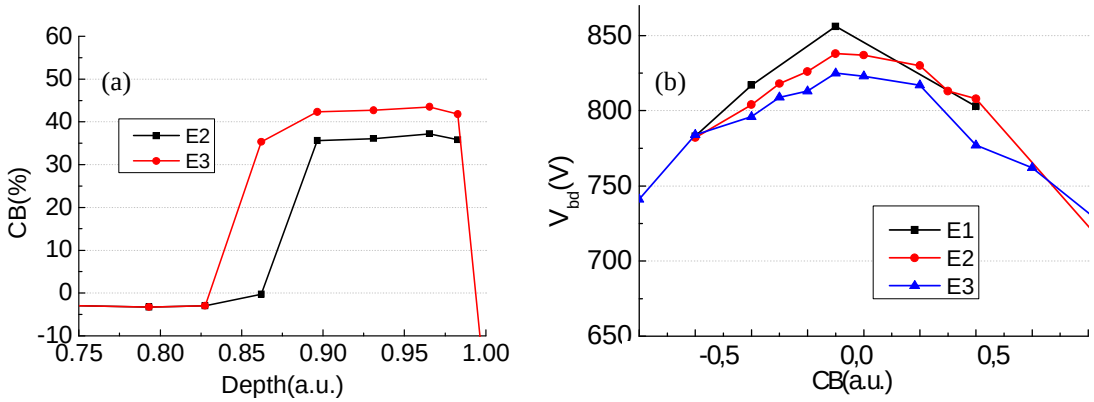

Fig.6.33 Simulated (a) vertical evolution of the CB condition and (b) V_{bd}-CB trade-off, for different implantation energies.

As a final remark it can be stated that although the main function of the $P_{connection}$ implant is the electrical connection between the P_{body} diffusion and the P_{pillar} layer, the

definition of the $P_{connection}$ dose, angle and energy values has to be accurately done to tune the E_F peak location in order to enhance the robustness of the UltiMOS transistor.

6.3.3.3. Optimized Pconnection implant

As it has been introduced, the key to improve the device robustness is to engineer the electric field peak location to be able to reach a high avalanche current capability. A possible way is to spread the current over the whole active area, with the inherent PDR branch in the I_d-V_{ds} MOSFET characteristic. As deducted from the previous I_d-V_{ds} curves plotted in Fig.6.26, when the $P_{connection}$ Module is modified, the current can be transferred to the active area, avoiding the device destruction. The $P_{connection}$ Module has to be optimized by tuning the energy, dose and angle of the $P_{connection}$ implant. The optimized $P_{connection}$ implant (*Opt*) has the same dose as the reference (*Ref*), but a 0.23x angle and a double implantation energy is used. Therefore, the implanted Boron goes deeper in the Silicon, in both vertical and horizontal directions. The same reference N_{buff} layer is used in both *Opt* and *Ref* cases.

The simulated V_{bd} and I_{snap} values for different CB conditions are plotted in Fig.6.34. The I_{snap} values are taken when the first decrease in avalanche voltage is observed. However, if the simulated voltage decrease in the NDR branch is very small (less than 10-20 V), the NDR will not be visible at all in the measurements and the device will survive since an increase on the electric field will be possible in the device after the small NDR. Thus, an I_{snap} value lower than 1 A is not taken into account in the simulations since the avalanche process for the Optimum CB condition will start in the edge termination. Moreover, self-heating needs to be taken into account when the device is carried to high current levels to measure its energy capability. Notice that the I_{snap} value (when the very first NDR branch starts in the I_d-V_{ds} curve) is in the range of 10 A in the *Opt* case, 5 decades higher than the *Ref* case.

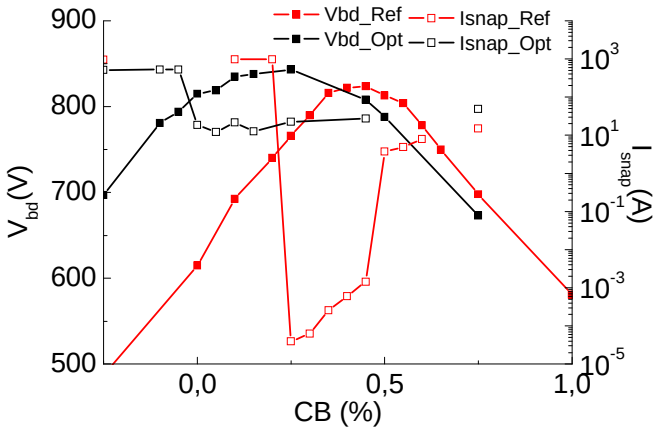

Fig.6.34. Simulated V_{bd} and I_{snap} values for different CB conditions for the reference UltiMOS (*Ref*) and the condition with the optimized $P_{connection}$ Module (*Opt*).

The experimental and simulated I_d-V_{ds} curves for Optimum CB *Opt* and *Ref* UltiMOS transistors are compared in Fig.6.35. Taking into account that the I_d-V_{ds} curve depends on the system set-up, note that the automatic measurements gives a lower V_{bd} value than the one corresponding to the simulated active area, being close to the TV_{bd} value. The TLP measurements exhibit an increase of the voltage with the current in both cases. However, the *Ref* transistor failed at lower current range during the TLP since the active area exhibits an NDR branch at lower current level, as observed in the simulated I_d-V_{ds} curve of the *Ref* active area. On the contrary, the *Opt* transistor did not fail since the active area shows a large PDR branch at high current level.

An UIS test with a 10 mH inductor, charged with the energy equivalent to 12 A (in the range of 700 mJ) has been performed on an Optimum CB *Opt* transistor. The *I-V* curves are plotted in Fig.6.36, and the thermal mappings at different times are shown in Fig.6.37. Observe that at the beginning of the pulse, some current flows already through the active area but the higher current is observed at the periphery/edge termination region. However, the current can be spread in the active area, as deducted from the Fig.6.37-(b) and (c) images, where 100 ºC are captured in the active area of the device.

The EMMI measurements presented in Fig.6.38 are performed at 647 and 698 V, using different lenses to capture the images of Optimum CB UltiMOS transistors with the optimised $P_{connection}$ Module. The pictures show that the avalanche process takes place at the edge termination area of the device at a current level in the range of 20 mA. The failure signatures once Optimum CB *Opt* transistors are destroyed, under a 12 A UIS pulse, are captured in Fig.6.39. As inferred, all the failures are located at the corner of the active area. This is a clear indicator that the current flows through the active area during the UIS test, with no focalization in the GR region.

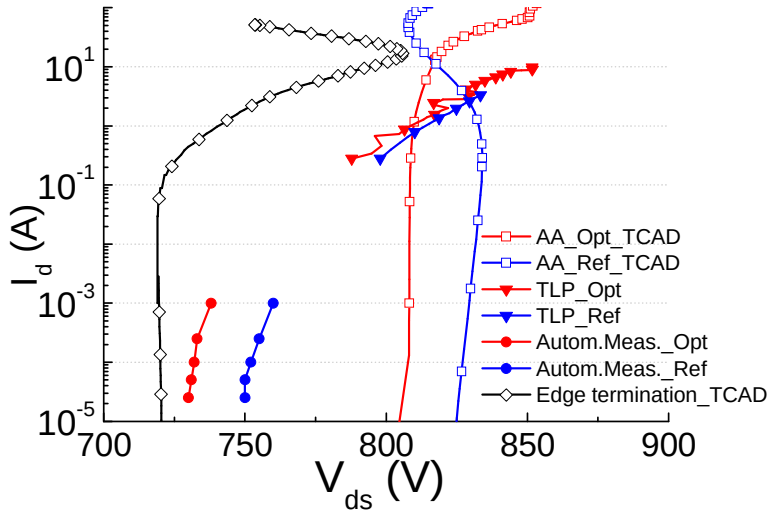

Fig.6.35. Simulated I_d-V_{ds} curves for the active area and edge termination and measured I_d-V_{ds} curves (TLP and automatic measurements) for Optimum CB *Ref* and *Opt* UltiMOS transistors.

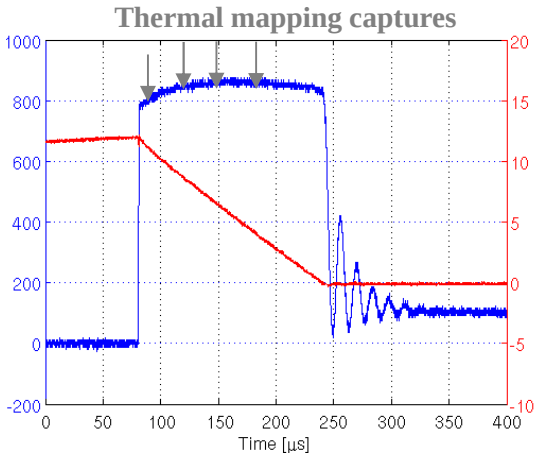

Fig.6.36 *I-V* curves during an UIS test for an Optimum CB UltiMOS transistor with the optimized $P_{connection}$ Module. Courtesy of Unina.

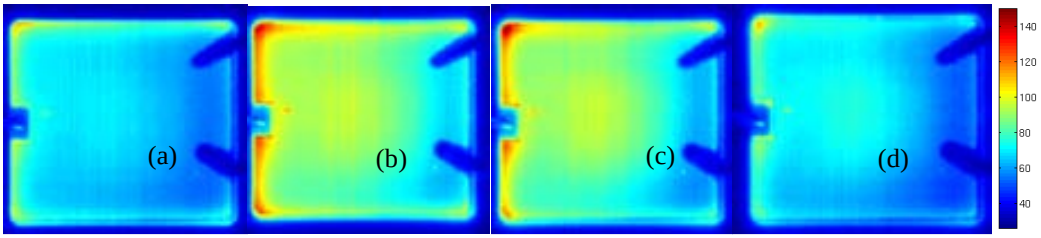

Fig.6.37 Thermal mapping for an UltiMOS transistor with the optimized $P_{connection}$ Module, taken at (a) 80, (b) 120, (c) 160, (d) 200 and (e) 240 µs (from *I-V* curve in Fig.6.36), for a 12 A UIS pulse, using a 10 mH inductor. Courtesy of Unina.

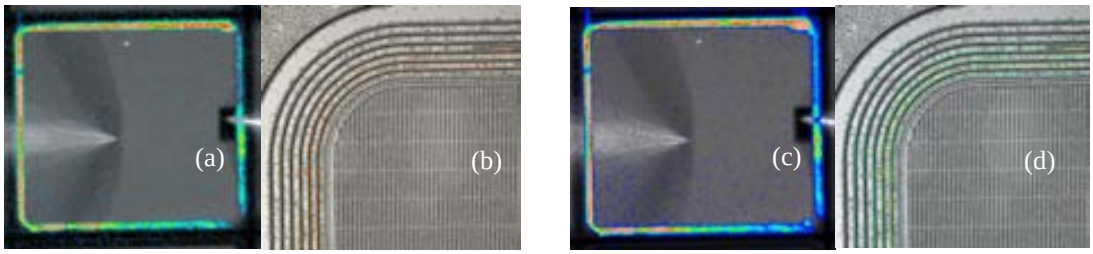

Fig.6.38. EMMI measurements on the UltiMOS transistor with the optimized $P_{connection}$ Module, taken at 647 V/15mA ((a) and (b), with 0x8 and 20x lenses, respectively) and at 698/22.3 mA ((c) and (d), with 0x8 and 20x lenses, respectively). For the measurements with 0x8 lens, a 2 sec exposure is done. However, when the 20x lens is used, a larger time is needed to capture the emission due to the different sensitivity of the camera.

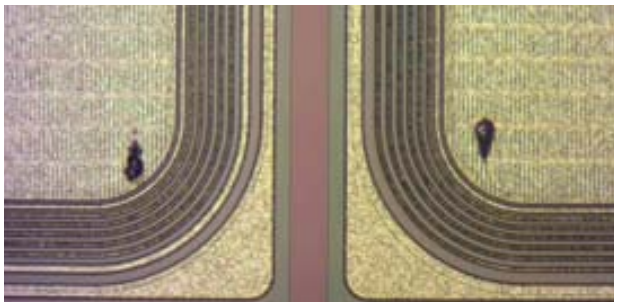

Fig.6.39. Failure signature at the corner of the active area for two Optimum CB Opt UltiMOS transistors, taken after the failure under UIS test.

The use of an optimised $P_{connection}$ Module allows significantly improves the robustness of the UltiMOS transistors, as shown in Fig.6.40, where the average V_{bd}-E_{AS} values for different CB conditions are plotted for two different processed lots (A and B). Notice that the E_{AS} in both cases has increased from zero values to values in the range of 600 mJ. The Lot B (Fig.6.40-(b)) has a wider CB range, with transistors for both N_{rich} and P_{rich} CB conditions. However, in this lot, the average V_{bd} value is lower in the *Opt* case in comparison with the *Ref* one since the N^-_{epi} layer is slightly thinner than the standard one (also the SJ trenches depth was reduced). The low V_{bd} average value in the CB-V_{bd} curves is just because the V_{bd} value is taken at low current levels, where the V_{bd} is determined by the termination. The electric field peak in the active area is placed deeper in the silicon, and at the edges of the active area will interfere with the edge termination avalanche location. However, as inferred in the *I-V* curve from the UIS measurement (Fig.6.36), the voltage at t=0 is in the range of 800 V. Therefore, if the V_{bd} value at lower current level needs to be higher, the edge termination should be re-designed accordingly to the new electric field peak location.

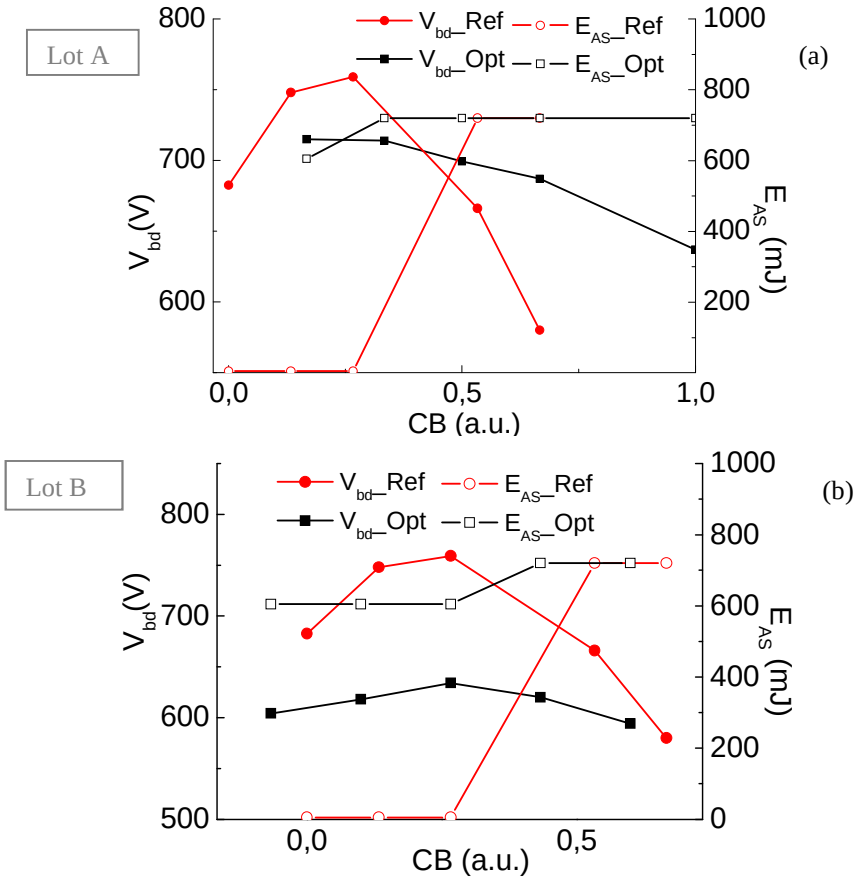

Fig.6.40. Measured V_{bd} and E_{AS} average values for different CB condition in the case of (a) the reference UltiMOS (*Ref*) and (b) the one with the optimized $P_{connection}$ Module (*Opt*). Data for two different processed lots.

The different on-state behaviour has been checked from the experimental measurements. No impact is observed from the experimental V_{TH} and R_{on} values for *Opt* and *Ref* devices with different CB conditions.

6.4. New N_{buff} layer and new $P_{connection}$ implant together

As already described, the use of the optimized N_{buff} layer and the $P_{connection}$ leads to an enhancement of the UltiMOS transistors robustness, whatever the CB condition is implemented. As a final structure, both solutions are merged to get the best possible UltiMOS transistor. The three different cases are labelled as *Opt* (Optimum $P_{connection}$ Module), *Buf* (Optimized N_{buff} layer) and *Opt+Buf* (merge of both optimized $P_{connection}$ Module and N_{buff} layer). The V_{bd} and E_{AS} average values for different CB conditions are plotted in **Fig.6.41-left** and **Fig.6.41-right**, respectively. Note that the V_{bd} value is higher for the *Buf* case since the optimized N_{buff} layer leads to an increase on V_{bd} as concluded in section 6.3. Therefore, the V_{bd} value in the *Opt+Buf* case is higher than that of the *Opt* case, increasing the manufacturability window from the point of view of amount of CB conditions that lead to V_{bd} values higher than 650 V. On the other hand, the E_{AS} average values slightly decrease when the optimized N_{buff} layer is used. Note that for the *Opt+Buf* case the E_{AS} further decreases for Optimum CB devices, although it increases again when the CB condition is P_{rich} or N_{rich}. This decrease is related to the fact that the optimization of the $P_{connection}$ implant was done for the reference N_{buff} layer. Therefore, a new set of parameters needs to be established to have E_{AS} values above 600 mJ. Note that in all cases the E_{AS} average values are higher for P_{rich} than for N_{rich} UltiMOS transistors since it will be always easier for the current to spread at the bottom of the SJ trench than at the top. However, when the Optimized N_{buff} layer is used, the R_{on} is degraded, as demonstrated in section 6.3.2.

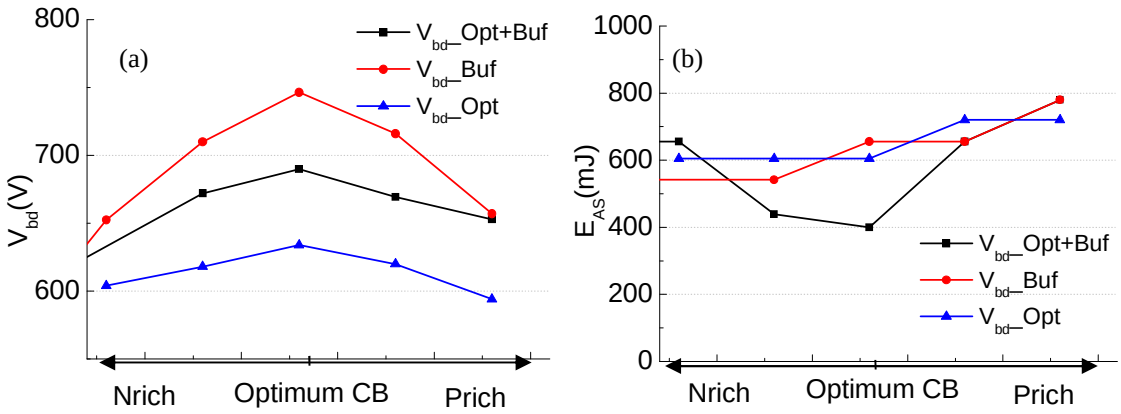

Fig.6.41. Measured (a) V_{bd} and (b) E_{AS} median values for different CB condition for the *Opt*, *Buf* and *Opt+Buf* cases.

6.5. Conclusions

In this Chapter, the electrical behaviour of the Optimum CB and Prich UltiMOS transistors has been compared to determine how the Optimum CB device should behave. It has been demonstrated that the UltiMOS structure avalanche energy capability can be improved by engineering the electric field distribution in the structure. In this way, the parasitic bipolar activation can be avoided since the current will not crowd at the top of the structure, near the P_{body}-N_{link} junction. It has been proven that:

- The optimization of the N_{buff} layer to increase the length of the PDR branch in the edge termination is crucial for the transfer of the current from the periphery of the device to the active area. In this way, the current can be spread in a larger area, increasing its capability. On the other hand, the same N_{buff} layer needs to not degrade the current capability of the active area and, if possible, increase the current level at which the NDR for the active area starts. The optimization has to be done taking into account that the R_{on} can be degraded, which is a key parameter for the conduction losses when the device is in circuit operation.
- The optimization of the $P_{connection}$ implant that is used to connect the P_{body} with the P-type pillar is a key process step for the avalanche current capability of certain CB conditions. The electric field peak location can be varied by tuning the $P_{connection}$ implant parameters (angle, dose and energy). In the reported measurements, the V_{bd} is decreased since the termination-active area interaction has an electric field at deeper in the Silicon volume. Therefore, the termination should be re-designed accordingly. It has been demonstrated that with this technique, the R_{on} value is not degraded.
- The use of both approaches together is a feasible way to increase the E_{AS}, without degrading the voltage capability of the device, since the termination V_{bd} is increased with the optimized N_{buff} layer. However, it leads to a slight reduction of the R_{on} value.

6.6. References

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CHAPTER 7

7.1. General conclusions

The research work carried out in the framework of this Ph. D. thesis deals with the robustness improvement of a SJ power MOSFET designed and fabricated by ON Semiconductor, known as UltiMOS transistor and based on deep trench technology for local charge balance. The final goal is to fulfill all the electrical requirements including the avalanche capability to define the final process technology to go into the market. The main results raised from the present work are summarized as follows.

- The initial failures located at the edge termination led to the study of the avalanche capability of the edge termination/periphery PiN. Those failures were induced by the NDR branch of the *I-V* characteristics, caused by the Egawa effect.

    - The edge termination robustness was improved with the introduction of an N_{buff} layer. Other techniques could be used, as CIBH, but more process steps should be added into the UltiMOS process flow.

    - UltiMOS transistors with the N_{buff} layer optimized for postponing the NDR branch in the edge termination region exhibit a higher energy capability for P_{rich} CB conditions. However, UltiMOS transistors with optimum and slightly N_{rich} CB conditions show almost null E_{AS} values. The implementation of the N_{buff} layer slightly increases the sR_{on} value from 21 to 24 $m\Omega cm^2$.

- Once the robustness of the edge termination was improved, devices derived from the UltiMOS (UMOS, SJ Diode and Sj Bipolar) were implemented and investigated for better understanding the failures causes. Isothermal *I-V* simulations were performed to compare with the experimental data. Thermal

mapping, TLP and EMMI measurements were performed on all the fabricated devices to determine the current distribution.

  - The E_{AS} values were found to be strongly dependent on the CB conditions in all the implemented structures.
  - The relevance of the current distribution over the device was demonstrated.
  - It was demonstrated that current focalization in the periphery region occurs for Optimum CB (both in SJ Diode and SJ Bipolar devices) conditions since the TV_{bd} value is lower than the corresponding AAV_{bd}.
  - The location of the maximum impact ionization is crucial for the activation of the parasitic bipolar transistor at the top of the structure. The Impact Ionization is located at the top of the SJ trenches for N_{rich} and Optimum CB devices, close to the N_{link}-P_{body} junction. Hence, the current focalization at the edge termination enhances the parasitic BJT activation.

- UltiMOS transistors with different CB conditions were analyzed to assess the conclusions coming from the different fabricated devices derived from the UltiMOS architecture:
  - The cause of the low E_{AS} values for certain CB conditions was investigated. It was concluded that the current focalization in the periphery region of the UltiMOS for Optimum and slightly N_{rich} CB conditions enhances the parasitic BJT activation. Different technological parameters were varied to decrease the risk of the parasitic BJT activation. However, the variation on those parameters leads to the undesired degradation of R_{on} and V_{TH}.

- The need of a higher energy capability in the whole CB range has led to the re-design of the UltiMOS transistor:

  - The N_{buff} layer has been optimized to enlarge the PDR branch to be able to re-distribute the current from the edge termination to the active area for Optimum CB transistors. However, the energy capability is still topped off by the edge termination robustness and the R_{on} value is increased again.
  - A new technique to increase the robustness of SJ MOSFETs is presented in this thesis. It consists on the engineering of the electric field in the active area of the device to push the electric field peak to a deeper region in the Silicon, far from the N_{link}/P_{body} junction (to avoid the parasitic BJT activation). The good experimental results confirm the feasibility of modifying the $P_{connection}$ Module in the final process technology of the UltiMOS transistor. However, the V_{bd} value is decreased.

- The two implemented solutions for the robustness enhancement are compatible with the UltiMOS process technology with any layout or masks modifications.

7.2. Future work

- The on-state resistance can be further reduced by shrinking the cell pitch of the UltiMOS active area. Notice that the region in between SJ trenches has to be wide enough for the gate trench and the source contact implementation. In this sense, a strong effort has to be made to reduce the gate trench width to enhance the sR_{on} performance.
- The edge termination region has to be optimized by exploiting the benefit of the charge balance using deep trenches. The final goal is to increase the voltage capability of the edge termination region to avoid current focalization problems. However, the edge termination could be already enhanced by re-optimizing the actual Guard Ring edge termination.
- The doping concentration of the N^-_{epi} layer has to be increased to enhance the current capability of the UltiMOS transistor with a reduced area and no thermal destruction.

7.3. Publication List

Proceedings in International Conferences

1. S. Díez, M. Ullán, M. Ruat, P. Fernández-Martínez, A. Villamor, G. Pellegrini, M. Lozano, R. Sorge, D. Knoll
   "Radiation studies of power LDMOS devices for High Energy Physics applications"

   IEEE Nuclear and Space Radiation Effects Conference, Denver, July 2010.

2. A. Villamor-Baliarda, P. Vanmeerbeek, J. Roig, P. Moens, D. Flores
   "Electric Field Unbalance for Robust Floating Ring Termination"

   European Symposium Reliability on Electron Devices, Failure Physics and Analysis (ESREF*), Bourdeaux (France), October 2011.

3. J. Rhayem, A. Wieers, A. Vrbicky, P. Moens, A. Villamor-Baliarda, J. Roig, P. Vanmeerbeek, A. Irace, M. Riccio, M. Tack
   "*Novel 3D Electro-Thermal Robustness Optimization Approach of Super Junction Power MOSFETs under Unclamped Inductive Switching"*

   Semiconductor Thermal Measurement Modeling an-d Management Synopsium (SEMI-THERM), 28th Annual IEEE, San Jose (CA) USA, pp 69-73 (2012)

4. P.Vanmeerbeek, A.Villamor-Baliarda, J. Roig, F. Bogman, P. Moens, D. Flores
   "Enhancing the robustness of multiple floating field-limiting ring termination by introduction of a buffer layer"
   ISPSD, Brugge (Belgium), June 2012.

5. A. Villamor-Baliarda, P. Vanmeerbeek, M. Riccio, V. d Alessandro, A. Irace, J. Roig, P. Moens, D. Flores
   "Influence of Charge Balance on the Robustness of Trench-Based Super Junction Diodes "

   European Symposium Reliability on Electron Devices, Failure Physics and Analysis (ESREF*), Sardenya (Italy), October 2012.

6. A. Villamor-Baliarda, F. Bogman, P. Moens, D. Flores
   "Breakdown location for different Charge Balance on Super Junction Trench-Based MOSFET devices"

   International Synopsis Power Semiconductors (ISPS), Prague (Check Republic), August 2012.

   * ESREF papers are published in Microelectronics Reliability

Proceedings in National Conferences (Spain)

1. A. Villamor, I. Cortés, F. Bogman, J. Roig, P. Vanmeerbeek, P. Moens, D. Flores
   "Capacitive behaviour in Super Junction Trench MOSFET devices"

   Spanish Conference on Electron Devices (CDE), February 2011

2. D. Flores, S. Hidalgo, A. Villamor, S. Mcquaid, I. Mazarredo
   "Improving the firing mechanisms in thyristors for lighting applications"

   Spanish Conference on Electron Devices (CDE), February 2011

3. J. Urresti, S. Hidalgo, A. Villamor, D. Flores and I. Cortés
   "Lateral Punch-Through TVS Devices in Ultra-Thin SOI Technology"

   Spanish Conference on Electron Devices (CDE), February 2011

Patent submitted

1. P. Moens, A. Villamor, P. Vanmeerbek, J. Roig, F. Bogman,
   "Method for improved robustness of Local Charge Balanced Semiconductor Devices"
   Submitted on November 2012

No further publications were allowed due to the high confidentiality of the project.

Appendix A: Technology requirements and building blocks

The UltiMOS structure is implemented on an N^+ substrate (N^+_{sub}) in which an epitaxial N-type layer is grown (N^-_{epi}). The N^-_{epi} layer should be as thick as the trench depth would be, including the necessary safety microns to ensure good contact between the trench bottom and the high conductive N^+ substrate. An additional intermediate N-type buffer layer (N_{buff}) is grown between the substrate and the epilayer in some of the analysed devices to enhance their electrical performance. The process technology includes around 10 photolithographic steps, deep trench etch and selective epitaxial growth.

The first module to be implemented after the N^-_{epi} layer and the eventual N_{buff} layer growth is the **Termination Module**, based on the conventional guard ring edge termination technique[1]. A first thin oxide layer is grown followed by a deposition of a Si_3N_4 layer, which is used as the hard mask for the LOCOS field oxide formation[2] (see Fig.A.1-(a)). Then, a first photolithography step is done to be able to selectively etch the Si_3N_4 layer where the field oxide will be present (see Fig.A.1-(b)). During the oxidation process, the typical bird's beak will appear at the edges of the Si_3N_4 mask, leading to a soft transition between active and non-active areas. The sacrificial Si_3N_4 layer is removed by performing an initial oxide wet etch to eliminate the thin oxide layer grown on top of the Si_3N_4 layer followed by the Si_3N_4 wet etch. Then, a second photolithographic step for the implantation of the P-type rings is performed by covering the whole active area with resist to avoid boron penetration into the Silicon surface (see Fig.A.1-(c)). The activation and diffusion of the implanted Boron will be carried out during the subsequent thermal steps.

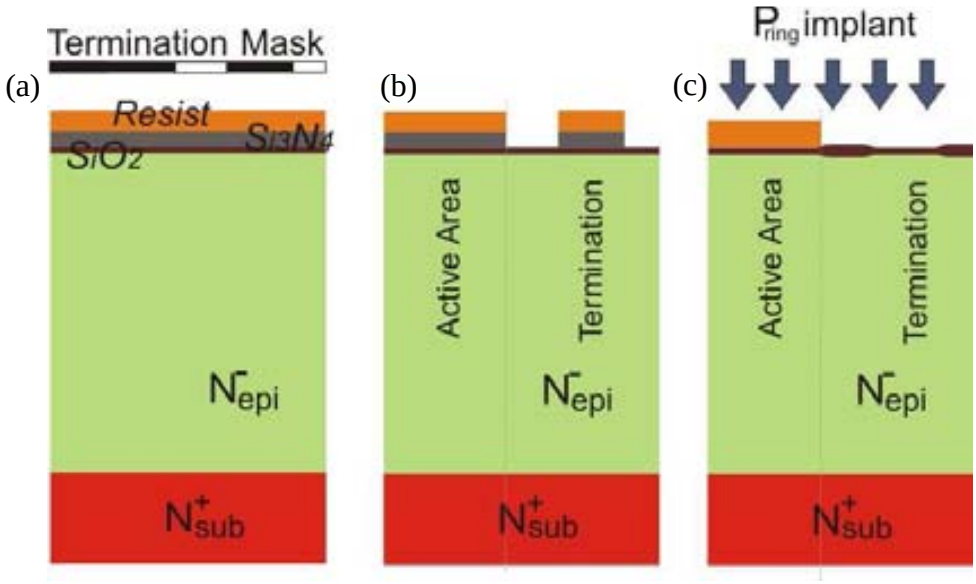

Fig.A.1. Sequence of the Termination Module. (a) SiO2 growth and deposition of Si_3N_4 and resist, (b) photolithography for the LOCOS field oxide growth and (c) Boron implant.

The second module to be implemented is the **Implants Module**, where the P_{body}, N_{link} and N^+ diffusions are formed. The N_{link} implant is performed through a thick resist layer due to the very high energy used to ensure that the N_{link} diffusion is deeper than the P_{body} after all the process steps. Both P_{body} and N_{link} implants are performed on the complete active area (Fig.A.2-(a)) , whereas the N^+ is done stripe alike exactly where the gate trench will be located, but using a wide mask that overlaps the gate trench to have N^+ diffusion on both sides (Fig.A.2-(b) and (c)). The diffusion of the P_{body}, N_{link} and N^+ implants is performed with the subsequent thermal steps of the process.

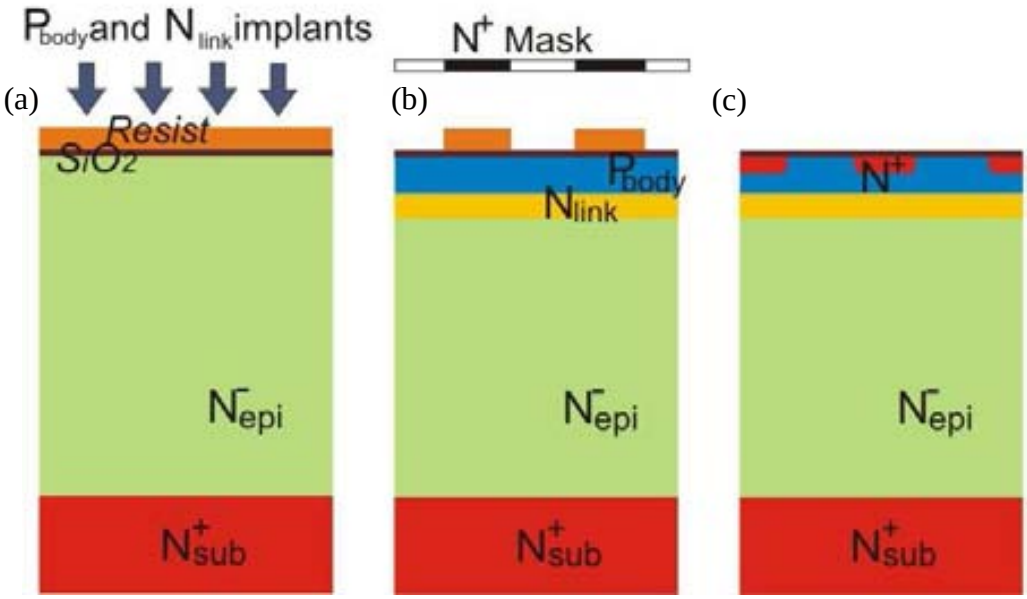

Fig.A.2. Sequence of the Implants Module. (a) Boron and Phosphorous implants to form the P_{body} and the N_{link} diffusions respectively, (b) photolithography for the N^+ mask and (c) structure after the diffusion step.

The **Gate Module** starts with a tetraethylorthosilicate (TEOS) oxide deposition and densification to create the hard mask for the gate trench etch. After the photolithography step (Fig.A.3-(a)) with the subsequent TEOS etch where the gate has to be located, the silicon dry etch is performed to create the shallow gate trench (Fig.A.3-(b)). Then, the gate oxide is grown and, since the oxide growth rate depends on the doping concentration[3,4], the oxide layer will be slightly thicker at the top of the trench gate where the N^+ diffusion is located than on the rest of the trench walls. Finally, the polysilicon is deposited and flattened until the silicon surface, using the thin oxide as stop layer for the polysilicon etching (Fig.A.3-(c)). The polysilicon gate is contacted at the end of the trench with the inherent trench mask widening in that region. Therefore, the gate trench will be deeper in the polysilicon contact region since the dry etching rate depends on the mask window[4]. The deposited polysilicon has to be thick enough to completely fill the gate ending.

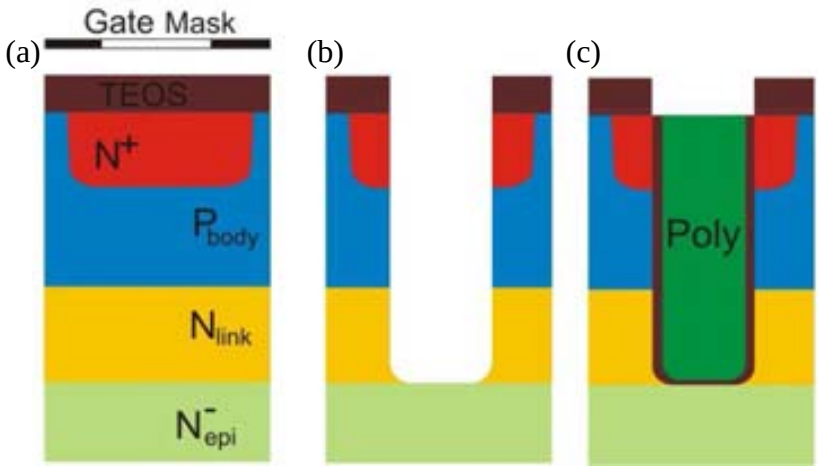

Fig.A.3. Sequence of the Gate Module. (a) Photolithography after the TEOS deposition, (b) after the trench etch and (b) the polysilicon deposition and planarization.

The most critical steps of the technological process come after the Gate Module and involve the deep trench formation and the epitaxial growth, called **NIP Module**. A TEOS layer is used to mask the silicon (Fig.A.4-(a)) and a Deep Reactive Ion Etching (DRIE) process is performed to create a deep silicon trench (Fig.A.4-(b)). The etching block is defined as the polymer deposition and selective etch of the bottom of the trench to mask the already formed trench sidewalls[5,6]. Thus, just the silicon from the bottom of the trench is etched away obtaining a completely vertical profile. The number of iterations of the etch block is determined by the depth of the trenches and the desired verticality of the trench sidewalls. The silicon etch has to be stopped before going deep into the N^{+}_{sub} and the walls need to be completely vertical and as smooth as possible.

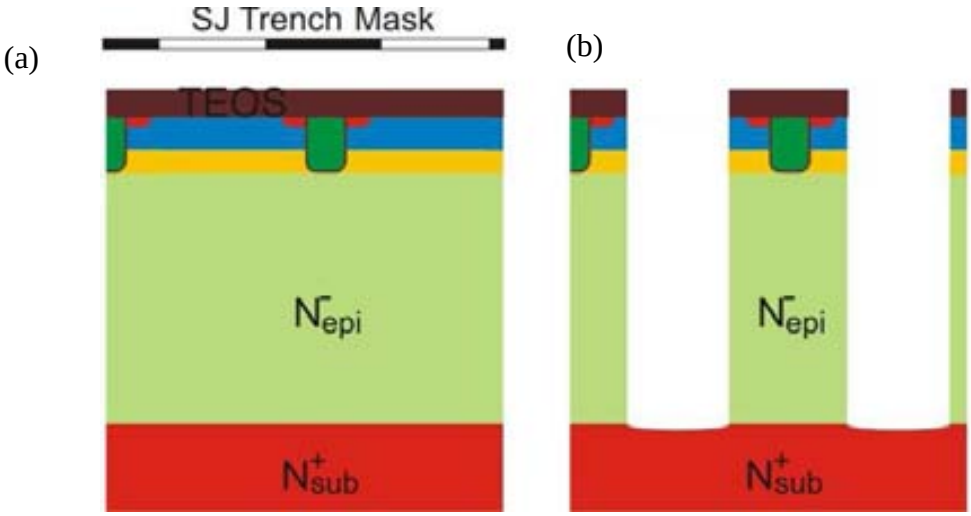

Fig.A.4. Sequence of the trench etch for the NIP Module. (a) Photolithography after the TEOS deposition and (b) deep trench etch.

Afterwards, the NIP (N-type/Intrinsic/P-type) layers are implemented (Fig.A.5-(a)). The three layers are consecutively grown in the epitaxial reactor to avoid native oxides in the interfaces. The purpose of the intrinsic layer growth is to separate both pillars for having a soft doping transition. If the intrinsic layer is skipped, the N-P pillars

will compensate their charges in the interface, loosing charges that contribute on the CB[7]. On the UltiMOS cross sections the intrinsic layer is not drawn since it will take charges from the N and P pillars during diffusion steps, thus it just smoothens the transition between the two N and P-type epi layers and it will not remain intrinsic any more at the end of the complete fabrication process. This module is also critical in the sense that the selective epitaxial N and P growth has to be done with the exact doping concentration and thickness. If the thickness is more than the target value, the trench will be closed before the complete fabrication steps and the absence of the void will mechanically stress the structure. On the contrary, if the epitaxial thicknesses are less than the target values the trench will not be properly sealed. The concentration is also a critical parameter since small variations will produce a shift in the CB curve and, as a consequence, the V_{bd} value can eventually be lower than the target[8]. After the NIP growth, a silicon recess is done to remove the silicon grown on the top of the structure, leading to a smooth V shape on top of the trench for better sealing (Fig.A.5-(b)).

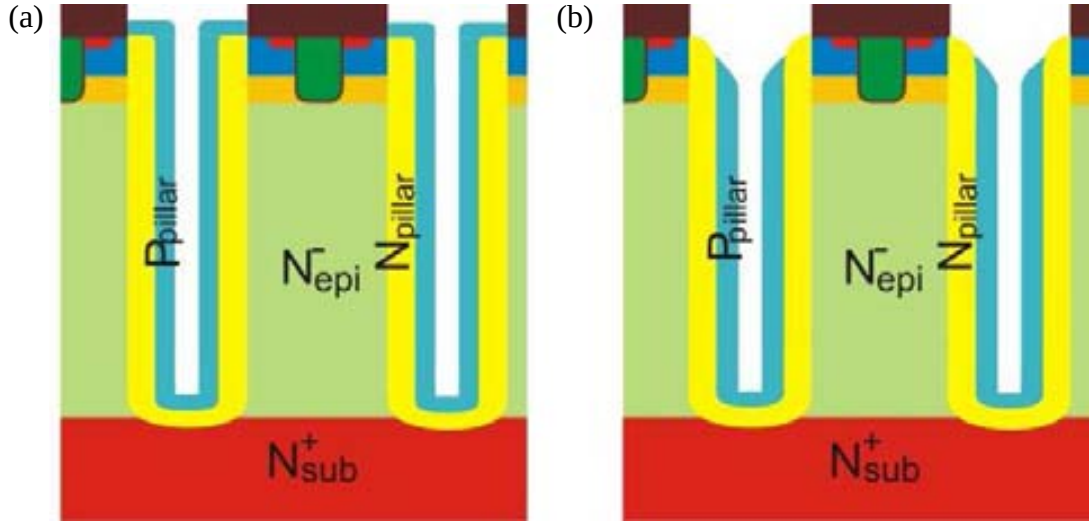

Fig.A.5. Sequence of the NIP growth for the NIP Module. (a) N-type, Intrinsic and P-type layers are growth and (b) silicon recess. The intrinsic layer will take charges from both N-type and P-type epitaxial layers during thermal steps.

A tricky module of a strong relevance for this thesis is needed before the trench sealing: the **Pconnection Module**. A Boron implant is performed through a pre-implant oxide to be able to electrically connect the P_{body} and P pillar regions (Fig.A.6). The energy, dose and tilt angle of the implant can be tuned to reach the required depth in the silicon and in the trench vertical direction, where the P_{pillar} is located. A more detailed study on the impact of different process parameters of the $P_{connection}$ Module on the electrical behaviour of UltiMOS is provided in Chapter 6.

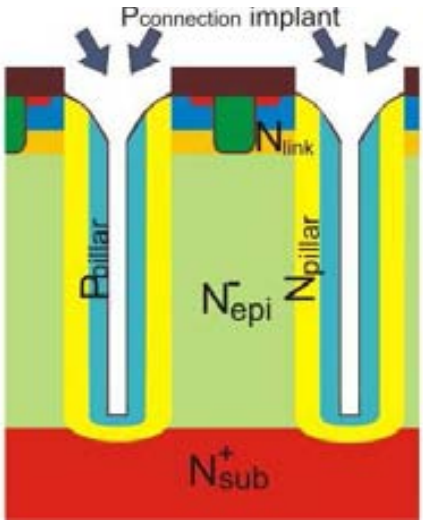

Fig.A.6. Boron implant to connect the P_{body} and P pillar regions.

Afterwards, the trench is sealed with a Borophosphosilicate glass (BPSG) deposition, leaving an air gap in the middle of the trench to avoid the stress that would make the complete fill of the trench by the oxide[7] and finally the surface is planarised by a Chemical Mechanical Polishing (CMP) process. The whole sequence is referred as **Sealing Module** (Fig.A.7-(a)).

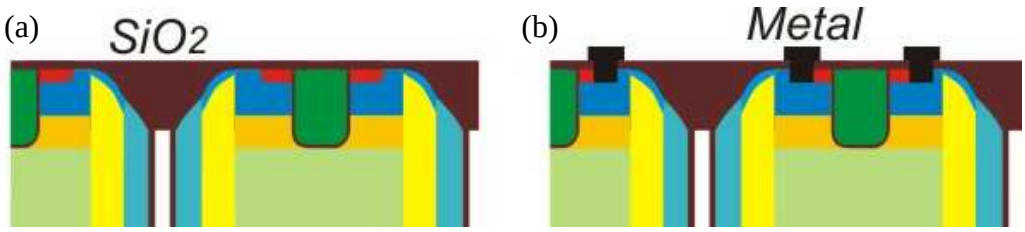

Fig.A.7. Cross sections of the (a) Sealing and (b) Contact Modules.

Finally, the **Contacts and Passivation Module** is implemented. The contact mask is used to open the regions where the oxide is etched away to make the metal-Silicon contact. A first thin metal is deposited and sintered to form a silicide to enhance the contact resistance (Fig.A.7-(b)). Afterwards, a second thick metal is deposited to handle the high source current. A mask is used to etch away the metal of the regions where it is not needed (basically, outside of the active area and in between the edge termination rings). Then the passivation is deposited and the last mask is applied to remove the passivation from the active area where the wire bonds will be placed.

A SEM image of the active area of an UltiMOS transistor is shown in Fig.A.8. The void in between trenches is marked as airgap. On the top part of the airgap there is the oxide plug, with the small V shape on the interface with the metal. The gate trench can be observed between the deep trenches. On both sides of the gate, the Source contacts are placed, which contacts both N^+ and P_{body} diffusions.

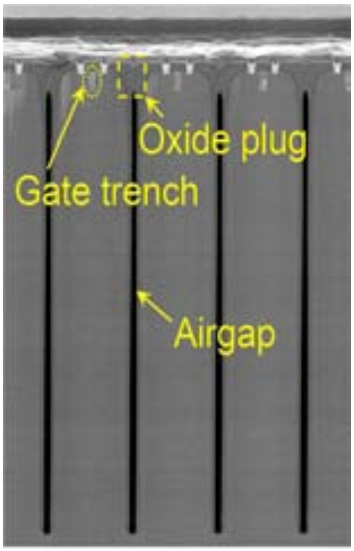

Fig.A.8. SEM image of the active area of an UltiMOS transistor.

References

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Appendix B: Experimental techniques and TCAD simulations

Processed devices

Almost all the measurements reported in this thesis are done at wafer level on a high voltage probe station. The only measurements performed on packaged devices are the Reverse Recovery test and the measurements on real applications since both tests are done with the device integrated in a circuit. Also the capacitive measurements in Phoenix are performed on packaged devices.

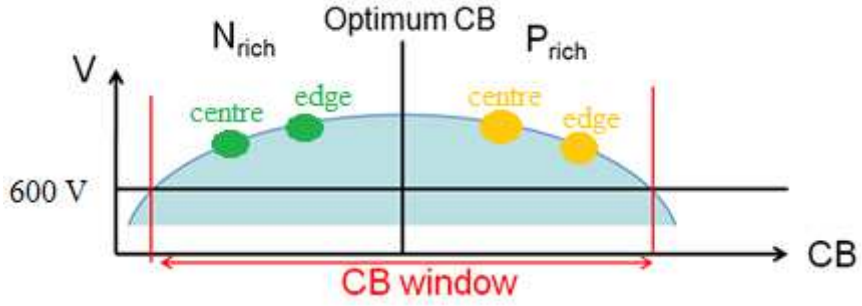

Fig.B.1. V_{bd} dependence on the CB condition.

Devices with different CB condition are present within the same wafer in order to get a large amount of devices of each CB value for measuring purposes. This is needed to make sure that all devices will fulfil the target specifications, even if there are small doping concentration variations during the epitaxial NIP Module implementation. As a result, the wafer edge is more P_{rich} than the wafer centre, which is achieved by tuning the selective epitaxial growth during the NIP Module. According to Fig.B.1, N_{rich} wafers have the edge devices more close to the Optimum CB, while the P_{rich} target wafers have the edge devices even more P_{rich}. Therefore there is some variability in the experimental results on a given wafer, and this is why an average value is taken to plot some experimental data in the thesis manuscript. Furthermore, some measurements are done in different areas on the wafer, normally edges, middle and centre. Middle means a reticle field in between the edge and centre of the wafer.

Experimental techniques

A large amount of different measurement techniques are used during this investigation. Some of the techniques are used to have the results detailed in the datasheet of the device, as the current capability under the UIS test (repetitive or single avalanche pulse), the reverse recovery test (to get T_{rr} and Q_{rr}) or the *C-V* measurements

to get C_{rss}, C_{oss} and C_{iss}. The other type of measurements are the ones performed to investigate the behaviour of the device under different conditions, as the Transmission Line Pulse (TLP), Transient Interferrometric Mapping (TIM), Emission Microscopy (EMMI), Thermal Mapping, etc. The real importance of the measurements comes when all of them are merged to dig for the device behaviour during operation, since each measurement is done under different conditions, or shows a different aspect of the electrical behaviour. This is what is done in the studies in Chapter 4, 5 and 6, where the studied structures are tested under different test conditions and techniques. Some of the measurements are performed in other research institutions during different collaborations. The relation of techniques and centres where they have been performed is on Table B.1.

Centre	Technique	Packaged Devices	Wafer Level
ON Semiconductor (Oudenaarde)	Automatic measurements (V_{bd}, V_{TH}, R_{on}, etc.) UIS test TLP EMMI *C-V* measurements		X
ON Semiconductor (Phoenix)	*C-V* measurements	X	
DIBET (Department of Biomedical, Electronics, and Telecommunications Engineering from University of Naples Federico II)	Thermal Mapping under UIS test Lock-in thermography		X X
TUV (Vienna University of Technology)	TIM		X
KUL (University of Leuven)	Application tests	X	
CNM (Centro Nacional de Microelectrónica, Barcelona)	Reverse Recovery test	X	
STUBA (Slovenská Technická Univerzita V Bratislave)	Repetitive UIS pulse		X

Table.B.1. Relation of techniques used during the thesis and the centres where they were performed.

- ## Transmission Line Pulse (TLP)

Transmission Line Pulse (TLP) is a technique for measuring devices and circuits under the influence of short-time pulses. Test is usually used to emulate Electrostatic Discharge (ESD) events in the Device Under Test (DUT). The introduced self-heating

during TLP measurements is so small that the experimental results can be directly compared with the isothermal TCAD simulations. The TLP setup consists on a transmission line that is charged and discharged, leading to a rectangular pulses sequence (see circuit on Fig.B.2-(a)). The oscilloscope measures the current and the voltage, making an average value obtained from the 70 to the 90% of the pulse[1]. Once the DUT is already measured, a tester is used to check for the damage on the DUT by measuring the leakage current. Example of I_d-V_{ds} curves measured by TLP are plotted in Fig.B.2-(b). At low voltage levels, the measured current is just noise from the system, and it is in the range of 10-100 mA. At high voltage levels the real I_d is measured showing the typical current increase with the drain voltage. The "snapback" shows the impedance of the line, meaning that the device is in short circuit. Some of the measurements do not show this device failure signature because the system is limited in power to 2.5 kW and the applied pulses are not able to destroy the devices[2].

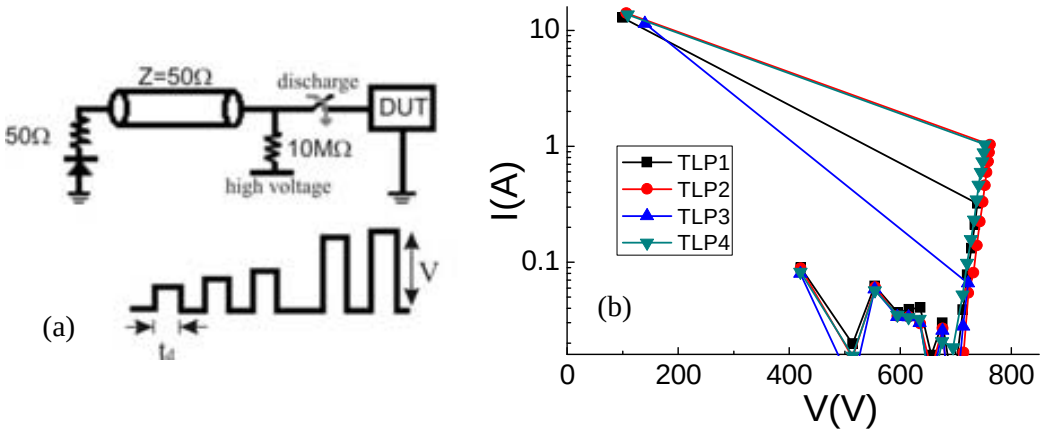

Fig.B.2. (a) Schematic of a basic TLP system and (b) example of I_d-V_{ds} curves obtained from TLP measurements.

The first UltiMOS TLP measurements were done under 500 and 100 ns long pulses. A comparison between both pulses is reported on Fig.B.3. In this case, the device is not destroyed and reaches the maximum available power for the measurement setup for both measurements. Although an NDR branch is present on the 500 ns I_d-V_{ds} curve, the device is not destroyed due to the very short applied pulses. On the other hand, the 100 ns pulse curve reaches higher voltage levels without showing the NDR branch. Therefore, the thermic effects could be disgraded if the 100 ns pulses are used, postponing the snapback. However, if the system would permit higher power levels, the NDR would be also present in the 100 ns pulse curve with identical shape than that of the 500 ns curve[3]. Thus all the measurements reported on this thesis are done on 100 ns pulse to be able to compare with the performed isothermal simulations.

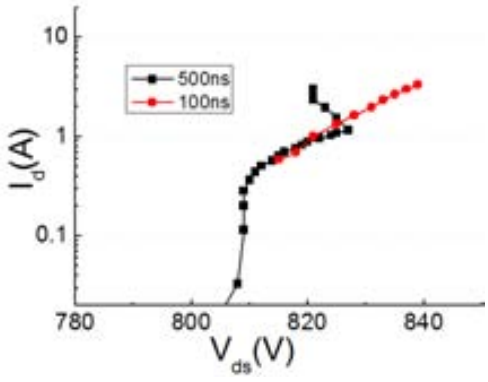

Fig.B.3. I_d-V_{ds} TLP curves with 100 and 500 ns pulses performed on PiN diodes.

- ## Unclamped Inductive Switching (UIS)

The UIS test is a standard test used to quantify the robustness of power devices, and it yields a measure for the ability of a power device to absorb a high amount of energy in a short time without being damaged[4]. The device is driven into breakdown to dissipate the energy; therefore the device needs to be able to sustain the avalanche even when high currents are flowing through it. The test consists on the discharge of the energy stored in an inductor directly through the DUT (see the circuit in Fig.B.4-(a)). The dumping of the energy starts when the gate is switched off (see curves in Fig.B.4-(b)). Then the current starts to decrease at the same time that the voltage rises very fast to voltages higher than the nominal V_{bd} of the device. In the case of UltiMOS transistors, the device has to sustain power in the range of 100 kW/cm^2. Finally, when the inductor is totally discharged, the V_{ds} value corresponds to the nominal V_{dd} value[5,6].

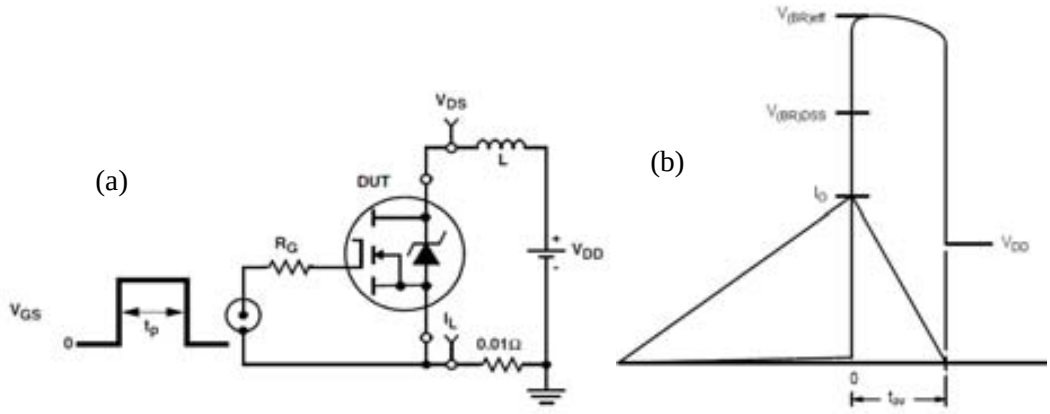

Fig.B.4. (a) UIS test circuit and (b) typical switching waveforms.

The current capability (I_{AS}) of the device is defined as the maximum of the UIS current discharge that is successfully sustained by the device. On the other hand, E_{AS} is defined as the energy capability of the device. The conversion I_{AS}-E_{AS} can be done with:

$$E_{AS} = \frac{1}{2} L I_{AS}^{2} \qquad \text{(Eq. 1)}$$

being L the inductor value. There are two basic ways to perform the UIS test: the single avalanche or the repetitive avalanche setups. In data sheets the results under these tests are quantified as E_{AS} (energy capability) or I_{AS} (current capability) for the single pulse and E_{AR} (energy capability) for the repetitive pulse[7]. Notice that the E_{AR} value will be always lower than the E_{AS} value due to the enhanced self-heating effect when UIS pulses are repetitively applied to the device. There are two failure modes when the MOSFET is subjected to UIS. The first (active mode) results when the avalanche current forces the parasitic bipolar activation. The second (passive mode) results when the instantaneous chip temperature reaches a critical value. Depending on the inductor value and the avalanche current the failure mode can be deducted[8]. The I_{AS} values for different inductances as increasing the temperature for a Vishay[8] and UltiMOS transistors are plotted on Fig.B.5-(a) and (b), respectively. It the same reference, it is stated that low inductances limits the instantaneous temperature excursion since they provide little energy, leading to active mode failures. On the other hand, higher inductances extends the decay time for the avalanche, increasing the temperature in the chip resulting into a passive mode failure. All the measurements performed in the ON Semiconductor laboratories are single avalanche pulses.

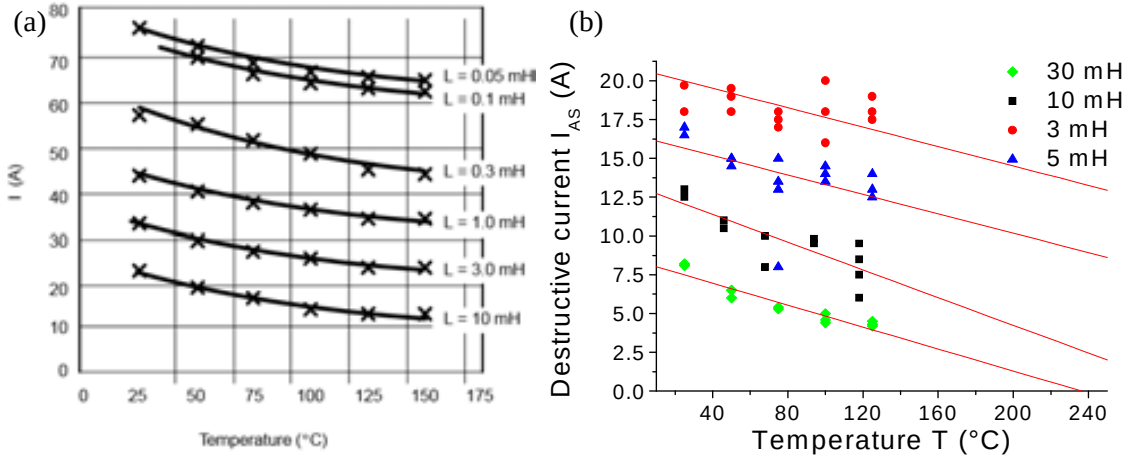

Fig.B.5. Avalanche failure current with the temperature for a (a) Vishay and (b) UltiMOS counterparts, when the inductor value is modified. Courtesy of Vishay[8] and STUBA, respectively.

When the PhD research started in 2009, the fabricated SJ transistors were packaged and tested under UIS pulses at the Phoenix site of ON Semiconductor with the subsequent extra time for shipping the devices, packaging them and one by one measuring. The results of the UIS test on packaged parts were the same as the ones previously measured on wafer level. Thus, an automatic UIS test system to be used at wafer level was acquired at the Oudenaarde site. In this way, a faster and much economic way to test the robustness of the SJ power transistors has been used to perform the studies reported on Chapter 4, 5 and 6. The measurement set-up used in ON Semiconductor is an ITC 5510F UIS inductive tester (Fig.B.6), where the user can select

the inductor value, the applied V_{dd} and the current that is going to be dumped on the DUT. The test can be done by varying the inductor or the current values. However, all the experimental data reported in this work has been obtained by modifying the inductor discharge current for better comparison with the UIS performance on competitor devices with V_{dd} and inductor values set to 50 V and 10 mH, respectively. The UltiMOS gate voltage is set from 10 to 0 V when switching. In the first UIS measures performed at the DIBET laboratories the gate was biased at +15 and -15 V in the on and off states, respectively, due to the available system set-up (see waveforms on **Fig.B.7-(a)** and **(b)**). This is how the study reported on Chapter 3 on the CB dependence on the off-state gate voltage started: differences in the experimental results on N_{rich} devices were found when measured at DIBET or ON Semiconductor sites. In order to use identical setup in both sites, the DIBET gate drive was changed to switching from 10 to 0 V. Typical UIS waveforms performed in ON Semiconductor are plotted in **Fig.B.8**, where the V_{ds}, I_d and V_g curves can be discerned. Notice that the V_{ds} value when the inductor is totally discharged (I_d=0 A) is twice the applied V_{dd} value. This is inherent to the measurement system. The UIS waveforms corresponding to UIS measures performed at the STUBA laboratories are plotted in **Fig.B.9**. These single shot measurements were performed before the repetitive avalanche ones to check if the STUBA system provides identical results than those obtained in On Semiconductor. See that the voltage peak in **Fig.B.9** increases with the current due to the DUT self-heating. In that case, the device failed when an 11.6 A pulse was dumped into the device. When the device fails during the discharge of the inductor (4-5 A), the V_{ds} value drops to 0 V since the UltiMOS behaves as a short circuit between the drain and source electrodes.

Fig.B.6. Detail of the UIS measurement system used in ON Semiconductor laboratories.

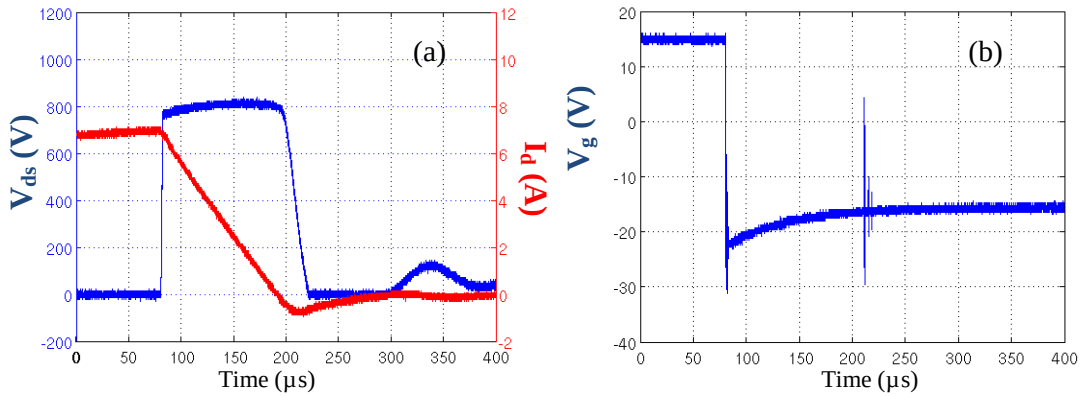

Fig.B.7. Measured UIS waveforms of an UltiMOS transistors, for I_d=7 A and V_{gs} switching from 15 to -15 V. Measurement performed in DIBET.

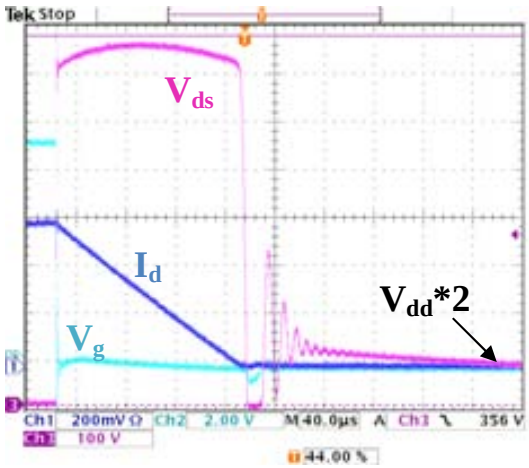

Fig.B.8. Measured UIS waveforms of an UltiMOS transistor, for I_d = 6 A. Measurement performed in ON Semiconductor.

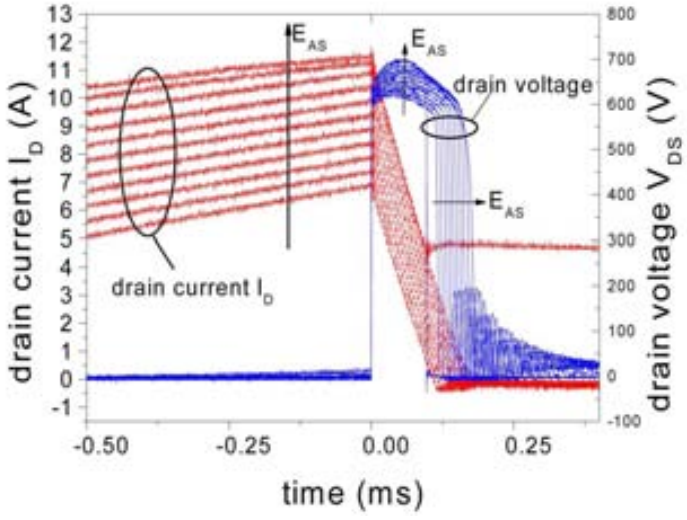

Fig.B.9. Measured UIS waveforms of an UltiMOS transistor, as the current is being increased. Courtesy of STUBA.

- **C-V measurements**

The system used in ON Semiconductor laboratories to measure the *C-V* characteristics is the Agilent 4284A. The voltage sweep applied to the device to extract the C_{ds}-V_{ds} curve ranges from 0 to 25 V with 0.5 V steps. Some *C-V* measurements were performed in Phoenix on packaged devices, sweeping from 0 to 200 V. This is basically due to the Agilent 4284 voltage range limitation available in the laboratory located in Oudenaarde (a maximum of 40 V is available). The added AC small signal has a level of 0.26 V with a 10 kHz frequency for both capacitance measurements. The two system connectors are for high and low voltages. Concretely, the drain electrode, in contact with the chuck, has to be connected to the high electrode. Otherwise, the measurement would not be accurate since the needle is directly connected to the chuck of the probe station, and this area is much bigger than the one used for the source needle. The source of the device has to be connected to the ground of the system to measure the C_{gd} capacitance, as shown in Fig.B.10. For the C_{ds} capacitance, the gate electrode has to be connected to the ground of the system. If the gate is grounded with the source, the measured capacitance is C_{oss}, even no significant variations will this introduce to the *C-V* curve since C_{gd} is very small compared to C_{ds}. An initial calibration has to be always done before starting a sequence of measurements[9].

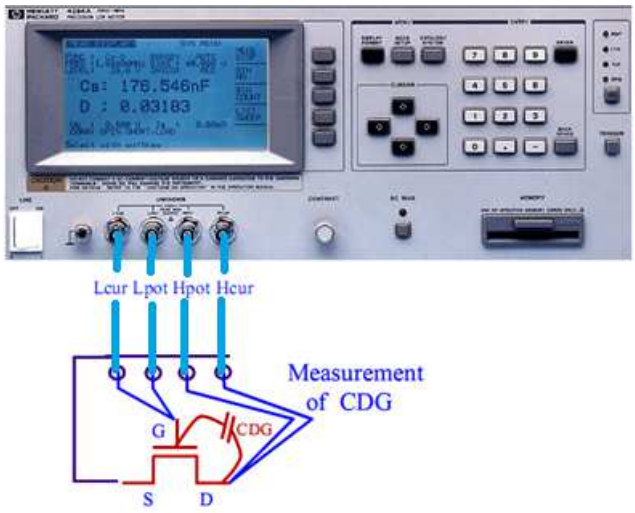

Fig.B.10. Detail of the *C-V* measurement system with the output connections (low-high ports for current and voltage).

Automatic measurements are performed on the engineering system of the lab of ON Semiconductor (Oudenaarde) to capture a capacitive value at different predefined drain-source voltages and it is basically used to measure C_{ds} and C_{gd}. The capacitive results are summarized in section 3.3.2, where the automatically extracted values from the *C-V* curves are the C_{ds} at 0V (C_{ds}@0 V), at 25 V (C_{ds}@25V) and V_{pinch}.

- **Automatic measurements**

Automatic measurements on a FET Tester are performed just after the processed wafers are out of the Fab to check the main electrical characteristics as V_{TH}, V_{bd}, sR_{on}, I_{ds}, I_g, etc. The system is a FET Tester E3600E and an Electroglas 2001cx automatic wafer prober (see detail of the wafer prober in Fig.B.11-(b)). The wafer is automatically loaded on the chuck, where it is properly biased depending on the test to be performed. A cassette with up to 25 wafers can be automatically loaded. The control software is especially developed based on the type of device to be tested and its layout. Between 9 and 12 reticle fields (around 150-200 devices) on different regions of the wafer are tested in 20 minutes to check uniformity of the wafer. In the case of V_{bd} measurement, the system takes the voltage at different predefined I_{ds} values as 1µA, 10 µA, 100 µA and 250 µA. The V_{bd} results reported in this work are taken at 100uA, the V_{TH} value is taken at 250 µA when drain and gate electrodes are swept together from 0 to 10 V. The R_{on} is extracted at I_d =10 A when the drain bias is increased, with V_g= 10V. All this values are the standards to be able to compare with competitor device datasheets.

Fig.B.11. (a) Automatic measurement bench and (b) detail of the microscope and the needle on the bench.

The FET Tester can be hooked up to different measurement systems, as to the UIS tester for instance. In this way, UIS test software was developed to perform around 150 measurements per wafer, which takes around 1 hour. The UIS automatic test performs 10 measurements per device with currents from 1 to 12 A, skipping 3 and 5 A. The inductor is set to 10 mH inductance as reference. As a result, the software gives the last current at which the device has passed the test. If it is 12 A, it means that the device survived even the last test.

- **Curve Tracer**

The curve tracer, a Tektronix 370A, is basically used to perform the EMMI measurements with a power limitation of 50 W[10]. The EMMI measurements using the curve tracer can be compared to a constant DC voltage applied to the device with the subsequent temperature increase. Devices under current stress in the curve tracer were

destroyed before reaching 50 mA due to the heating, as shown in the I_d-V_{ds} curves plotted in Fig.B.22. However, the curve tracer system was used to check if the snapback on the I_d-V_{ds} curve was visible, but the device failed before. An example of curve-tracer measurement where a device fails can be found on Fig.B.12 where the current is increased until the device was destroyed, at 140 mA-850 V.

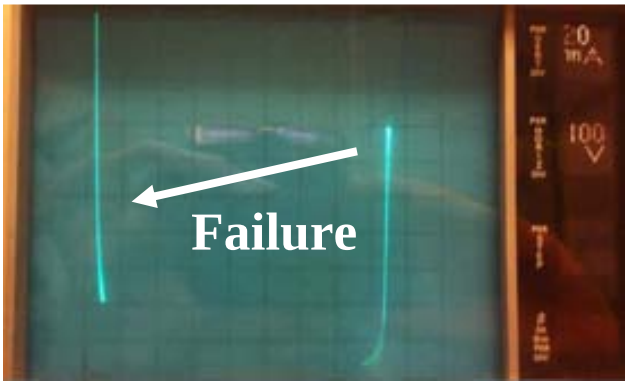

Fig.B.12. Example of I_d-V_{ds} measurement on the curve tracer.

- ## Emission Microscopy (EMMI)

The Emission Microscopy (EMMI) is a technique that allows detecting photonic radiation coming from the device due to the recombination process. Thus, the location of failure spots can be determined. The system is based on a cooled CCD camera with high sensitivity (in the 3-5 µm wavelength region) since the photoemission cannot be seen by the naked eye due to its very low intensity. A first image from the device is taken to be able to later overlay the emission picture to know the concrete region where the highest recombination takes place. For the emission image, the camera captures the photons that are emitting while the device is biased for a certain time. Thus, the longer the exposure time the highest photon capture. If the emission is uniformly over the complete exposure region, no exposure image will be possible since there will be no contrast in the image[11,12].

The EMMI measurement system[13] (PHEMOS1000, see Fig.B.13) consists on a bench with a camera on top, both inside a dark box to be able to capture the photons generated in the recombination process, when the device is biased with the curve tracer. When the avalanche process takes part, more current density is flowing through the device, thus more recombination leading to more emitted photons. The high voltage is at the drain (chuck) and the source and gate are shortened to ground. If the measurement is done on a diode, there is obviously no Gate connector. The current is increased and images are taken at the desired current level. Normally it is difficult to have a good emission picture at a current lower than 1 mA since too long exposure times are needed. The maximum current at which the device can be forced is around 50-60 mA, according to the power limitation of the curve tracer at 50W (55 mA*850 V= 46.75 W). It is

sometimes difficult to have an emission capture at high current level since the device is heating up due to the DC current applied to the device for several seconds (to set it up and take the image takes around 5-6 seconds for higher currents and even minutes for low currents). The device under these extreme conditions may break easily. The EMMI measurements are basically used to detect which region of the UltiMOS transistor is first activated when the device is in the off-state and try to correlate with the eventual CB non-uniformities on the device, leading to current focalisation

Fig.B.13. PHEMOS 1000 system.

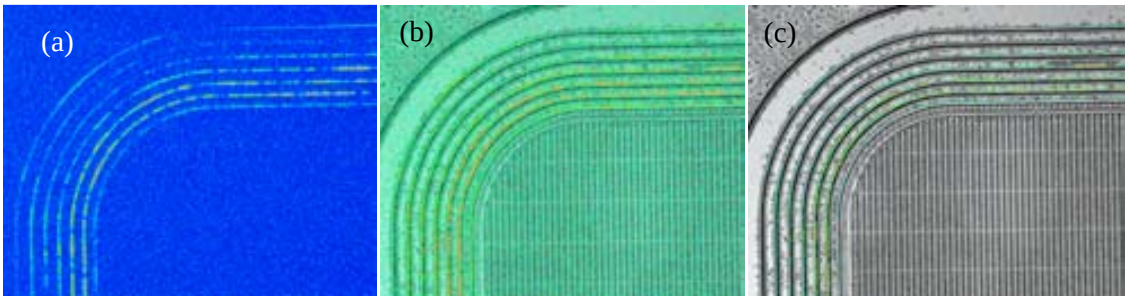

Fig.B.14. Example of EMMI measurements: (a) emission image and (b)-(c) overlap of the emission image with the device picture with different contrast.

It is worth to remark that the EMMI test is performed on wafers after Passivation and Metal layers are removed. Passivation is removed just to make sure that metal is perfectly removed all over the device since the majority of EMMI are done to see the behaviour of the device edge termination. The thin metal that is used to form the UltiMOS silicide is extremely difficult to remove. Therefore, in a typical EMMI image, the visible rectangles are the source contacts with this thin metal on top (see small rectangles in Fig.B.14-(c)). In between the rectangles there is oxide.

- ## Thermal mapping

Thermal mappings have been performed in the DIBET department of the University of Naples. Samples are tested under UIS conditions, ramping up the current until the device is destroyed. The UIS test is performed several times on the same

device (like a repetitive avalanche UIS test) and a picture is captured at different times. Then a calibration is needed and the final image looks like the ones shown in Fig.B.15. The pictures are taken at the maximum temperature (maximum power, thus, the top of the voltage curve)[14]. Two needles are used to contact the source and it has been proved that there is no influence on the needle position on the thermal mapping result. On the right of each picture there is the temperature scale. Due to the fact that the temperature increases with the current, the different temperature in the device gives an idea of the current distribution. See that the current is more or less homogeneously distributed in Fig.B.15-(a), although it is focalized at the top and bottom of the device on Fig.B.15-(b). Due to the resolution of the IR camera, no more accuracy can be obtained.

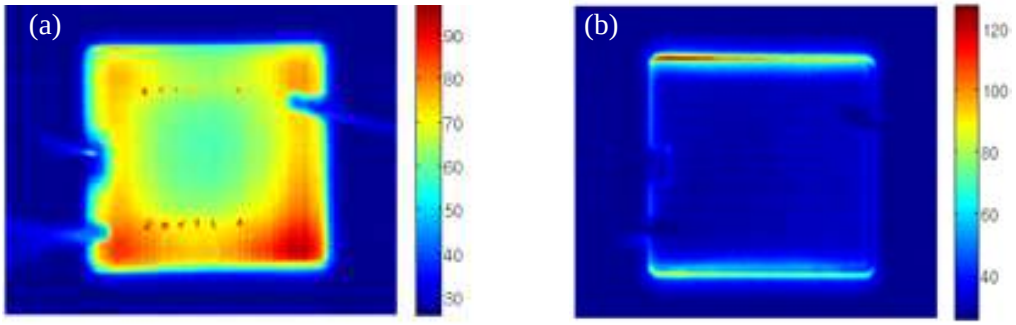

Fig.B.15. Examples of thermal mapping captures. Courtesy of Unina.

- ## Transient Interferrometric Mapping (TIM)

Transient Interferometric Mapping (TIM) is a method to detect temperature and carrier concentration variations with a laser beam. The refractive index changes with the variation of the current and, as a consequence, it can be measured by the optical phase shift between the measurement signal and the reference signal. The TIM method provides a micrometer space resolution and nanosecond time resolution and access to the device from the backside[15,16]. To be able to measure, a dainty preparation of the DUT is needed: the wafer is cut into small pieces and the drain is contacted with silver-glue, where a window for the TIM is kept open. The laser beam wavelength is 1.3 µm, which is transparent for Silicon, to sweep laterally in the silicon from the backside. A positive phase shift indicates heating/power dissipation. The pulse time is increased to see the temperature distribution when the power is increased. An example of TIM measurement is plotted in Fig.B.17, where it is shown how the phase shift varies depending on the position and how the phase shift (temperature) increases with the length of the pulse.

The applied pulse comes from a 500 ns TLP system, as the one already described, with a load-line of 1 kΩ. Higher load-lines allow better resolving of steep *I-V* curves, because this is close to a constant current regime[17]. The TLP circuit used to stress the device is shown on Fig.B.18-(a). The R1 and R2 values are 1 kΩ and 50 Ω,

respectively. The voltage and current curves measured on the device under stress are plotted in Fig.B.18-(b). The positive applied pulses on the drain are 4 A with a length of 1µs, while the source and the gate are grounded. After each stress the leakage current is measured to identify failure of the DUT, with K237 SMU and 400 ms delay for each voltage step. The current probe is a Tektronix CT1 and the voltage probe is a Philips 1:100.

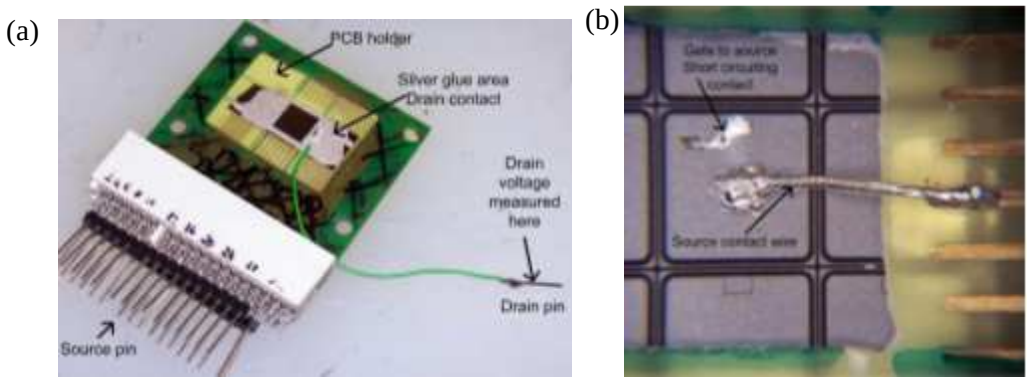

Fig.B.16. Picture of the PCB used to perform TIM measurements (a) from the drain side and (b) from the source side. Courtesy of TUV.

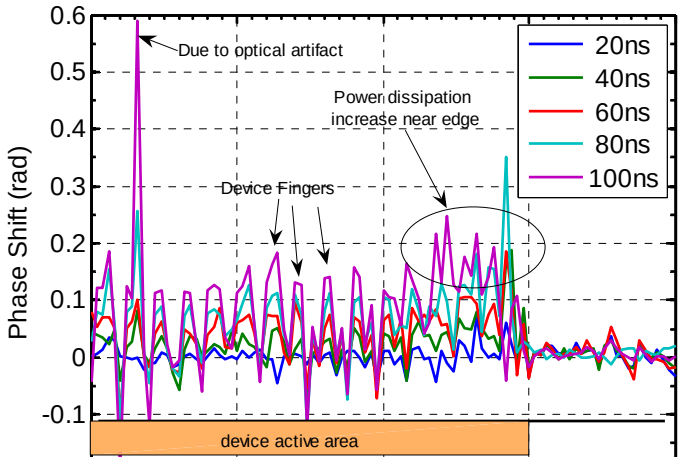

Fig.B.17. Example of TIM measurement on the edge of the active area of an UltiMOS transistor where the phase distribution for a certain region, when different pulses length are used. Courtesy of TUV.

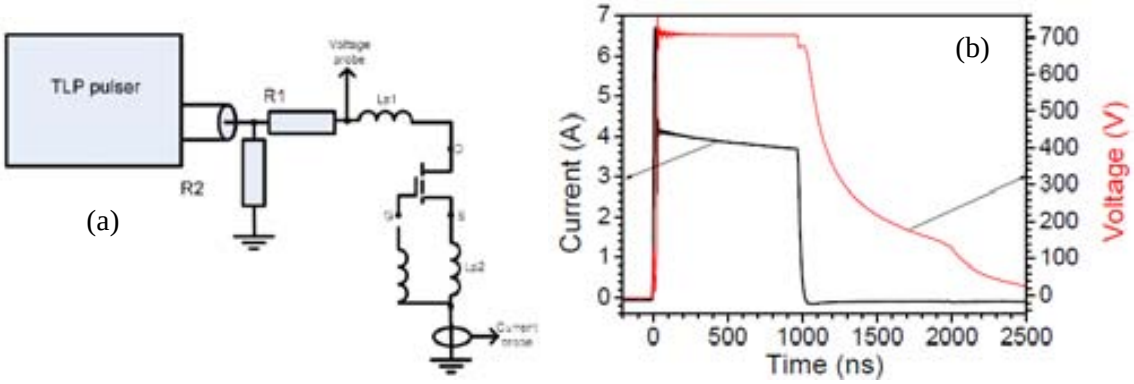

Fig.B.18. (a) TLP stressing scheme. (b) I-V measured curves for a device stressed under TLP. Courtesy of TUV.

- ## Reverse Recovery test

The parasitic body diode reverse recovery occurs in hard switching conditions when the device goes from on-state to off-state, since the storage minority charges need to be removed via negative current or via recombination inside the device. The parameters listed in a datasheet are: T_{rr} (body diode reverse recovery time), Q_{rr} (body diode charge) and I_{RRM} (body diode reverse peak current). These parameters are typically measured with the circuit plotted in Fig.B.19, where the gate of the IGBT is pulsed from +15 to -15 V. The DUT is subjected to a double pulse: the first is used to charge the device and when the second starts, the DUT body diode needs to recover before the MOSFET voltage can drop. Notice that the different parameters are measured from the beginning of the second pulse. For the measurements included in the thesis, the drive MOSFET is substituted by an IGBT (IXSH40N60), with an R_g= 10Ω and L=1 mH.

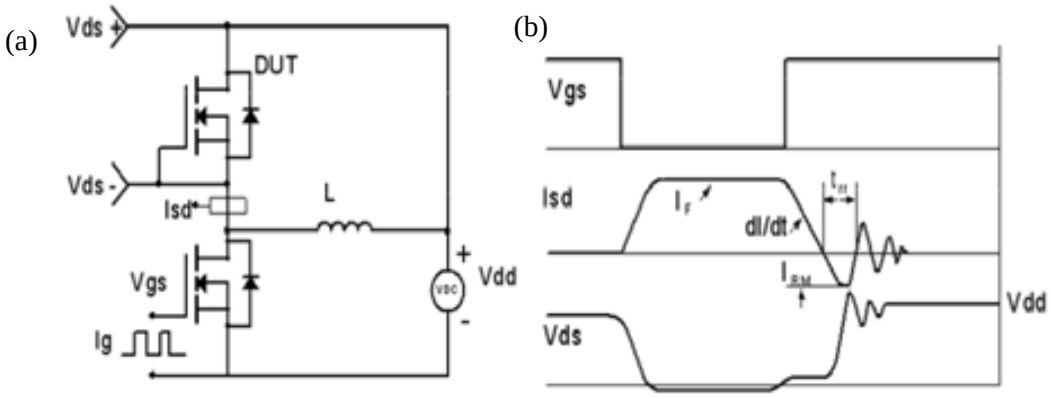

Fig.B.19. Reverse recovery (a) test circuit and (b) typical waveforms.

- ## Application test

The application circuit that has been chosen to measure the lost energy during the switching of the UltiMOS transistor and to make the comparison between performances with the other competitor devices is an inverted Buck converter, working at 1MHz and 6kW. The gate driver works at 2MHz with a V_{gs} varying between -10V and 15V, being the low and high, respectively. The measured E_{on} and E_{off} for the different devices are reported in Chapter 3, which are a good parameter to quantify the losses during switching.

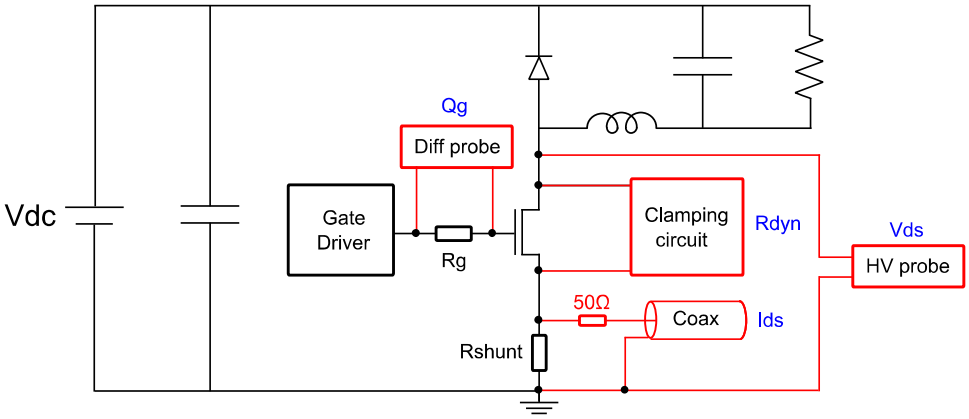

Fig.B.20. Buck converter circuit where the E_{on} and E_{off} for the UltiMOS are tested. Courtesy of KUL.

- ### Failure analysis

The failure analysis (FA) basically consists on a visual inspection of the device surface to check where the failure spot is located after a failure. It is worth to say that it might not be the same failure signature if a device fails under UIS or TLP measurement. A huge amount of energy has to be dissipated in the device during a UIS test; while for the TLP it will be much lower even for the same current level since the TLP pulse is very short (ns) and almost no self-heating will occur in the device. For the EMMI measurements, the usage of the curve tracer makes the device handle large amount of power for several seconds during the capture of the image with the subsequent self-heating.

TCAD Simulations

TCAD simulations are performed with Sentaurus[18], from the Synopsys platform. When the investigation started, the Dios, Mesh and SDevice were the current available tools. The Dios tool is used to perform technological simulations of the fabrication process. Thus, all the steps are processed according the region of the device that is being simulated and the real fabrication process. For instance, the P_{ring} implants will not be implemented in the simulation of the active area region since the implant is masked and do not apply to the active area. The Mesh tool is used to re-mesh the structure coming from the Dios simulator. This has to be done because the technological process meshing is more accurate in the junctions, whereas for the electrical simulation, the conducting regions need more meshing. Finally, the SDevice tool input file has the instructions for the electrical simulation, which are in accordance with the measurements performed to do a comparison one to one. When snapshots need to be captured, it is specified in the SDevice input file, and the structures are visualized with the Tecplot tool, where the electric field, potential lines, electron current density, etc. can be plotted. *C-V*

simulations and voltage capability termination simulations were performed in this way. Afterwards, the Dios was miscataloged and the process had to be changed to the SProcess tool, which functionalities were exactly the same, but different commands were used. The rest of simulations performed on this thesis, are done with Sprocess.

2D TCAD simulations of the edge termination and active area have been performed separately during the investigation, because the amount of computer resources needed to simulate both structures together is too big. 3D simulations of the first active cell, periphery and edge termination of the UltiMOS structure were performed in DIBET. 2D simulations are done with W=1 µm as default parameter. Therefore, all the curves have to be scaled afterwards, taking into account the area that is activated from EMMI measurements for instance.

Edge termination

The edge termination 2D simulations have been performed including the last microns of the active area for the sake of accuracy (see example in Fig.B.22-(a)). The active area is basically implemented with a P and N implant on the N^-_{epi} layer (forming the P_{body} and N_{link} diffusions, respectively). The edge termination is implemented with a certain number of floating rings, with differences in the width of rings and distance between them depending on the layout of the processed devices to be compared with. Snapshot of the electrical field for certain current level is plotted in Fig.B.22-(b). 1D simulations have been performed in the edge termination to determine the maximum voltage that the edge termination can handle, since no curvatures are present in the simulated structure.

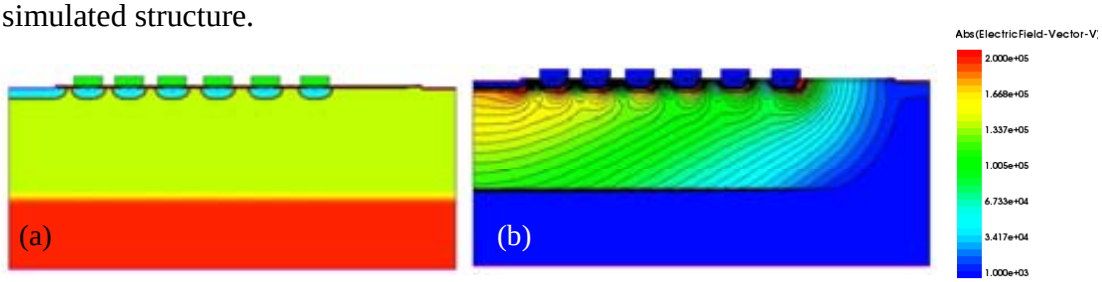

Fig.B.21. Simulated edge termination structure showing (a) the doping concentration after Dios simulation and (b) the electric field after SDevice simulation when the device is in the off-state.

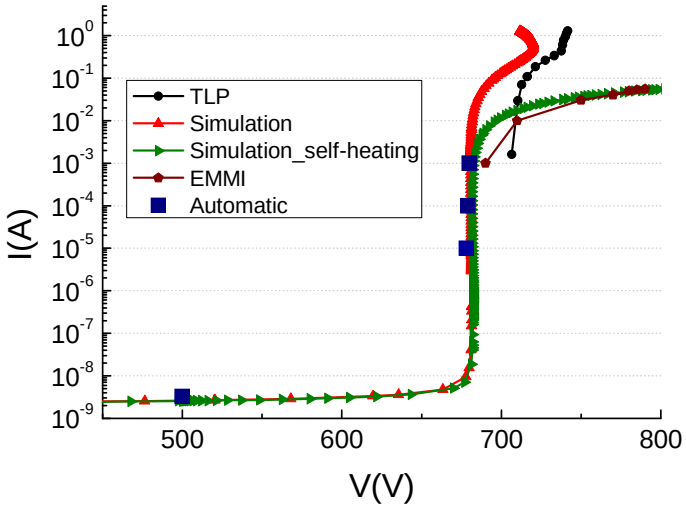

Fig.B.22. Simulated (Isothermal and Non-Isothermal) and measured (TLP, EMMI, FET tester) I_d-V_{ds} curves corresponding to a PiN diode with an 8 ring edge termination structure.

The I_d-V_{ds} curves coming from the electrical simulation altogether with some experimental results are plotted in Fig.B.22. A good agreement between simulated and measured performances can be observed. Since just the corners of the device are activated (derived from the EMMI results, see example in Fig.4.3-(b)), the curves are scaled by the perimeter of the four corners. If the EMMI would show activation in the whole periphery of the device, the I_d-V_{ds} curves should be scaled by the whole perimeter of the active area. Notice that the isothermal simulation results (not taking into account the self-heating of the device) can be compared with the TLP measurements, due to the short duration on the applied pulses. Automatic data is also plotted, showing good accuracy from simulations on the leakage current. On the other hand, the electrical simulation has been also done taking into account the self-heating of the device, which result can be compared one to one with the curve tracer measurements.

Active Area

The 2D simulations of the active area are performed on half of an UltiMOS cell due its symmetry. The structure with the doping concentrations and different materials, coming from the SProcess is plotted in Fig.B.23-(a) and the electric field snapshot from an SDevice simulation, including the flow lines at certain current level, is plotted in Fig.B.23-(b). The void in the middle of the SJ trenches is simulated as a nitride for better simulation convergence. When the I_d-V_{ds} curves are scaled, the perimeter of all the SJ trenches in the active area is taken into account.

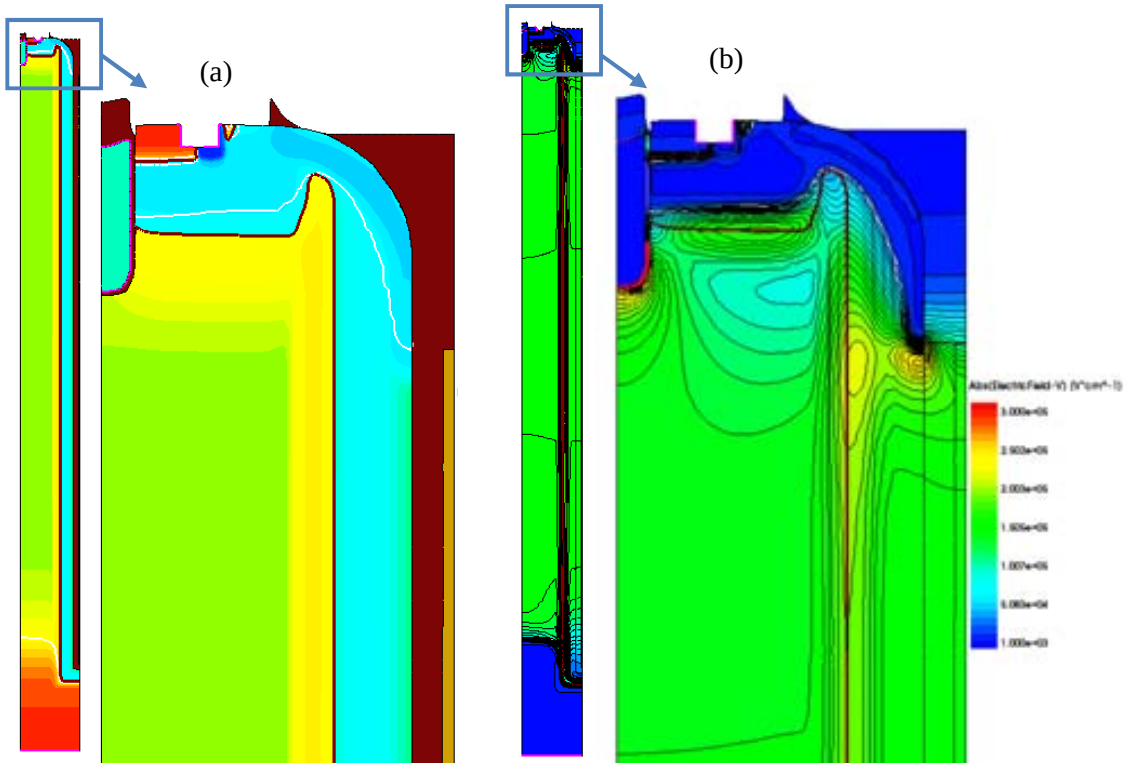

Fig.B.23. Simulated half-cell in the active area of an UltiMOS structure: (a) doping concentration and (b) electric field when the device is in the off-state.

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