

UNIVERSIDAD AUTONOMA DE BARCELONA

# NEMS/MEMS integration in submicron CMOS Technologies

by

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HEREBY CERTIFIES THAT

the thesis entitled **NEMS/MEMS integration in submicron CMOS Technologies** submitted by Jose Luis Muñoz Gamarra to fulfill part of the requirements to achieve the degree of Doctor of Philosophy in Electronic Engineering, has been performed under his supervision.

Bellaterra, September the 19<sup>th</sup>, 2014

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*“Appreciation is born through struggle”*

Anonymous





# *Abstract*

The reduction of MEMS devices dimensions to the nano scale (NEMS) has allowed them to access a host of new physics and promise to revolutionize sensing applications. However this miniaturization has been obtained at an expense of dedicated, difficult and non reproducible fabrication processes.

This thesis deals with the miniaturization of MEMS structures following a CMOS–MEMS approach. In order to it a small pitch CMOS technology (ST 65nm) is studied in depth, NEMS structures are defined using its available layers (width= 60 nm, thickness= 100nm in polysilicon and width= 90nm, thickness= 180nm in metal 1 based on copper) and a post-CMOS releasing process is developed in order to release them. Successful integration of NEMS devices is demonstrated with the added value of a robust, reproducible fabrication and an easy integration with additional circuitry. However this aggressive scaling has a main drawback, small output signals.

As an alternative to capacitive read-out, the implementation of a resonant gate transduction, based on the idea of modulate the charge of a transistor by the movement of a mechanical structure, is studied and implemented. The frequency response of a polysilicon resonator implemented in AMS 0.35um CMOS technology (24 MHz) has been successfully characterized and its operation as a low voltage switch (2.25 V pull-in) is demonstrated.

In addition, we propose the use of mechanical switches not only as memory or logic devices (due to its energy efficiency), but also as the building blocks of a ring oscillator configuration composed exclusively by mechanical switches. This new approach extends their use to other application as mass sensing but with the added value of a digital output signal. In order to implement this new configuration a model to simulate its behavior is developed and mechanical switches are built using different CMOS technologies, trying always to reduce their dimensions. Low operating voltages (5 V, MIM approach), abrupt response (4.3 mV/decade, ST Metal 1) and good  $I_{ON}/I_{OFF}$  ratio ( $1.10^4$ , MIM approach) are obtained.



# *Resumen*

La reducción de los dispositivos MEMS hasta la nano escala (NEMS) ha permitido el acceso a nuevos dominios de la física y promete revolucionar las aplicaciones de sensado. Sin embargo esta miniaturización ha sido conseguida a costa de procesos de fabricación complicados y no reproducibles.

Es por ello que esta tesis trata de obtener dichos dispositivos NEMS a partir de una tecnología CMOS comercial (ST 65nm). Con este objetivo un estudio en detalle de la tecnología ST 65nm es llevado a cabo para posteriormente definir en ella estructuras NEMS en sus diferentes capas (en polysilicio con un grosor y ancho de 60 nm x 100 nm y en metal 1, cobre , con unas dimensiones de 90nm x 100nm). Un nuevo post proceso de liberación es presentado que nos permite liberar las estructuras, demostrando así su correcta fabricación. Sin embargo, fruto de esta miniaturización las señales eléctricas usadas para sensar su movimiento se reducen también.

Como alternativa a un sensado capacitivo estudiamos la viabilidad de adaptar a nuestro proceso de fabricación CMOS–MEMS a un método de transducción basado en un transistor cuyo puerta resuena, su movimiento modula las cargas del canal y dicho desplazamiento puede ser leído en la corriente del puerta del transistor. Mediante dicho método de transducción la respuesta en frecuencia de un resonador de polysilicio a 24 MHz fue leída y su funcionamiento como interruptor a bajos voltajes (2.25 V pull-in) fue validado.

Además, proponemos el uso de interruptores mecánicos no solo como memorias o en aplicaciones lógicas (gracias a su eficiencia energética) sino como el elemento base para la implementación de un oscilador en anillo, completamente mecánico. Con este oscilador ampliamos el rango de aplicación de los interruptores N/MEMS a nuevos campos como el sensado de masa pero con el valor añadido de tener una señal digital. Para implementar esta nueva configuración presentamos un modelo y desarrollamos interruptores mecánicos en diferentes tecnologías CMOS intentando siempre reducir sus dimensiones. Con estos interruptores mecánicos CMOS hemos conseguido voltajes de operación bajos (5V), respuestas abruptas (4.3 mV/decada) y una buena relación  $I_{ON}/I_{OFF}$  ( $1.10^4$ ).



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# Abbreviations

<b>MEMS</b>	<b>M</b> icro <b>E</b> lectro- <b>M</b> echanical <b>S</b> ystem
<b>NEMS</b>	<b>N</b> ano <b>E</b> lectro- <b>M</b> echanical <b>S</b> ystem
<b>ECAS</b>	<b>E</b> lectronica <b>C</b> ircuits <b>A</b> nd <b>S</b> ystems group (UAB)
<b>MiCs</b>	<b>M</b> icro <b>C</b> hemical systems
<b>MiBs</b>	<b>M</b> icro <b>B</b> iological systems
<b>IC</b>	<b>I</b> ntegrated <b>C</b> ircuit
<b>CMOS</b>	<b>C</b> omplementary <b>M</b> etal <b>O</b> xide <b>S</b> emiconductor
<b>RF</b>	<b>R</b> adio <b>F</b> requency
<b>CNT</b>	<b>C</b> arbon <b>N</b> ano <b>T</b> ube
<b>SoC</b>	<b>S</b> ystem <b>o</b> n <b>C</b> hip
<b>FEM</b>	<b>F</b> inite <b>E</b> lement <b>M</b> ethod
<b>BEOL</b>	<b>B</b> ack <b>E</b> nd <b>O</b> f <b>L</b> ine
<b>FEOL</b>	<b>F</b> ront <b>E</b> nd <b>O</b> f <b>L</b> ine
<b>ROM</b>	<b>R</b> educe <b>O</b> rders <b>M</b> ethod
<b>PDE</b>	<b>P</b> artial <b>D</b> ifferential <b>E</b> quation
<b>ODE</b>	<b>O</b> rdinary <b>D</b> ifferential <b>E</b> quation
<b>DRIE</b>	<b>D</b> eep <b>R</b> eactive <b>I</b> on <b>E</b> tching
<b>SOI</b>	<b>S</b> ilicon <b>O</b> n <b>I</b> nsulator
<b>FET</b>	<b>F</b> ield <b>E</b> ffect <b>T</b> ransistor
<b>MIM</b>	<b>M</b> etal <b>I</b> nsulator <b>M</b> etal
<b>RIE</b>	<b>R</b> eactive <b>I</b> on <b>E</b> tching
<b>FIB</b>	<b>F</b> ocused <b>I</b> on <b>B</b> eam
<b>SEM</b>	<b>S</b> canning <b>E</b> lectron <b>M</b> icroscope
<b>VHF</b>	<b>V</b> ery <b>H</b> igh <b>F</b> requency



# Chapter 1

## Introduction

### 1.1 Introduction

Microelectromechanicals systems (MEMS) have extended the benefits of Moore's law [1] beyond the electrical domain, producing a (r)evolution in sensing applications. The measurement of femtometer displacement [2], forces in the atto scale [3], mass sensors with single atom resolution [4] [5] or sub-single charge [6] is now a reality. All these achievements come from the miniaturization of MEMS dimensions to the nanoscale (NEMS) and it have had a deep impact in chemical, biomedical or environment field since many physical and chemical processes can now be monitored with an unprecedented resolution.

MEMS can be defined as a micro scale or smaller device that operates mainly via a mechanical or electromechanical means. In these devices a transduction method between mechanical magnitudes and electrical magnitudes (electromechanical transduction) is always presented (figure 1.1 [7]) in order to induce and/or the detect the motion of its moving parts. They are used in a very wide range of applications (inkjet, microphones, optical devices, inertial sensors, pressure sensors, radio frequency (RF) resonators, RF switch, Lab on Chip, drug delivery systems, optical switches or microspectrometers [8]) thanks to its:

- **Batch fabrication capability.** Process originally developed for the integrated circuit technology can be used to create and process thousand of identical MEMS devices in a single wafer, making them economical. The parallelism between IC industry and MEMS is so deep that foundries that can not afford the latest CMOS technology nodes are converted to MEMS fabrication centers.
- The possibility to add **new functionalities** to integrated circuits thanks to the integration of sensors (vibration [9], temperature [10], pressure [11], liquids [12], gases [13]) or actuator (acting upon a sensed signal) on the same substrate. This suppose an added value to integrated circuit industry.
- The **reduction of systems size** where the use of macroscopic devices like oscillators or accelerometers (piezoelectric devices and quartz oscillators, respectively) prevented further systems miniaturization [14] [15].

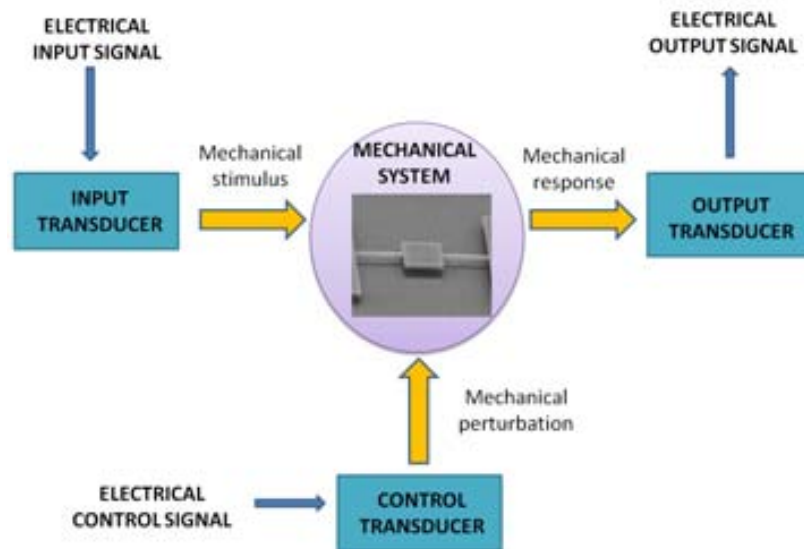


FIGURE 1.1: Schematic representation of an electromechanical system (extracted from [7]).

As transistors, MEMS devices also benefits of scaling but extend the benefits of size reduction in terms of: **speed** as higher frequencies can be reached if the dimensions of the resonator are reduced or faster response sensor can be developed. **Power consumption** and the actuation energy is reduced too and small quantities of energy can be sensed. More **complex** systems and bigger integration density

can be reached adding more functionalities in a given area. But it is in the field of **sensing**, that MEMS devices are playing a 'crucial role'. In fact, and due to new properties emerging at the nanoscale, nanomechanical resonators allow to access a host of new physics and promise to revolutionize many sensor applications. For instance as mass sensor, where the miniaturization of the NEMS devices has made possible to reach atomic mass resolution. Resonant mass sensors operate by providing a frequency shift that is directly proportional to the inertial mass of the molecules accreted upon them. As it can be observed in expression 1.1 the ultimate limit on these sensors mass resolution ( $\Delta M$ ) is fixed by the structure effective mass ( $m_{eff}$ ) and resonant frequency ( $f_n$ ) [16](assuming that an accreted mass on the beam does not produce any change in the spring constant):

$$\Delta M = S_m \Delta f_n \approx - \left[ \frac{2m_{eff}}{f_n} \right] \Delta f_n \quad (1.1)$$

Reducing the resonators dimensions, higher resonant frequencies are reached ( $f_n$ ) and a lower effective masses ( $m_{eff}$ ) are obtained, as a consequence better mass resolution is obtained. In table 1.1 some of the state of the art mass sensors based on resonant structures are shown. Their sensitivity ( $S_m$ ) is specified as it is the parameter that indicates the amount of mass necessary to shift the resonant frequency 1 Hz. Therefore as lower is the sensitivity better is the sensor

Material	Dimensions	Sensitivity ( $S_m$ )
Carbon Nanotube [Jensen08] [4]	l=205 nm, d=1.78 nm	0.01 yg/Hz
Carbon Nanotube [Lassagne08] [17]	l=900 nm, d=1 nm	0.09 yg/Hz
Silicon Nanowire [He08] [18]	l=1.8 $\mu$ m, d=30 nm	0.06 zg/Hz
Silicon Carbide Nanowire [Naik09] [19]	l=1.7 $\mu$ m, t= 100 nm	0.08 zg/Hz
Aluminum [Verd07] [20]	l=10 $\mu$ m, t=750 nm	0.90 ag/Hz

TABLE 1.1: Mass sensors summary (l=length of the beam, d= nanowire diameter and t is the structure thickness).

It can be easily appreciated how the mass sensitivity is improved as long as the structures are scaled. Carbon Nanotubes (CNT) are the devices with the smallest dimensions (and better sensitivity), followed by silicon nanowires and finally a mass sensor developed using a CMOS–MEMS approach.

These minimum dimensions structures, with lower  $S_m$  value, are obtained at an expense of a difficult, dedicated and non-reproducible fabrication process. Moreover, all these advantages due to size reduction have one main drawback: displacement detection. As the dimensions are reduced smaller displacement is produced under movement and the output signals generated by the different transduction methods are lower, being easily masked by parasitic effects.

The aim of this thesis is contribute to obtain the smaller NEMS resonator using a CMOS–MEMS approach, in order to reach the sensing limits that nanoscale shows. CMOS–MEMS has the added value of a robust fabrication process, reduction of parasitic capacitances and allows its integration with additional circuitry without any additional effort.

The present Ph. D dissertation has been written in the core of the Department of Electronic Engineering of the Universidad Autonoma de Barcelona at the ECAS (Electronic Circuits and Systems) group. The group is led by Prof. Nuria Barniol and their research framework is based on the development of MEMS systems for sensing and signal processing. The know-how acquired in the integration of MEMS resonator in CMOS technologies by the ECAS group has been taking as the starting point of this PhD thesis work.

## 1.2 Scope of the Thesis

The objective of this thesis is to **develop the smallest NEMS** structures following an **intra CMOS–MEMS approach**, that ensures an easy integration of the new NEMS devices with CMOS circuitry and providing competitive performance



as mass sensor. The fabricated devices could be used, in a future application, as the basis of a mass-sensor. In order to obtain this nano scaled structures:

- A small pitch CMOS technology, **ST 65 nm**, will be studied and different structures will be defines using its available layers. Two are the challenges to be solved:
  - A) A **new post CMOS releasing process** will have to be developed in order to release the structure defined in this new CMOS technology node.
  - B) As it was mentioned in the introduction, the miniaturization of the devices will have a deep impact on the generated output signals. The **feasibility of a capacitive transduction** will be studied in these minimum dimensions devices. As an alternative to this transduction, the implementation of a **resonant gate transduction** scheme following a CMOS–MEMS approach will be studied and implemented.

The mass sensing principle of mass sensor based on MEMS consists in measuring the resonance frequency shift of the MEMS device due to an accreted mass, as it was mentioned before. In system-on-chip application not only the integration of the signal conditioning circuitry (pre-amplifier) is necessary, also the electronics for driving the resonator at resonance and continuously tracking its resonant frequency need to be integrated. As a result analog active feed back loop circuitry need to be designed [21].

- As an alternative to the analog frequency tracking scheme configuration, we study the **feasibility** to implement an **oscillator composed exclusively by mechanical switches** based on the well known ring oscillator configuration. It will consist in an inverter configuration based on mechanical switches with a passive feedback loop. For an accurate  $V_{DD}$  voltage value, the system will be driven to auto-oscillate. Every time that one of the mechanical switches are brought into contact with the output a falling or rising

edge is obtained and as a consequence a digital output signal (a periodic square voltage) is obtained. Note that using this configuration a successful transduction is guaranteed (the output signal will be  $V_{DD}$  or zero) at a fixed oscillation frequency. In order to implement this new configuration:

- C) A **model** to simulate the **mechanical ring oscillator** behavior will be developed in order to study the conditions to obtain a stable periodic response.
- D) Different **mechanical switches** will be implemented in different CMOS technologies using an intra-CMOS MEMS approach to check if the conditions to implement a mechanical ring oscillator are satisfied. Again its dimensions will try to be minimized in order to obtain **low operating voltages** and high sensitivity in its future application as mass sensor.

## 1.3 Research Framework

In the development of this PhD thesis I have been involved in two national projects:

- 'NEMS/MEMS in submicrometric CMOS technologies for RF SYSTEMS and novel applications (NEMESYS)' (Ref:TEC2009-9008)
- 'Dispositivos nanoelectromecánicos (NEMS) integrados en CMOS: exploración de las propiedades no lineales de los resonadores NEMS en aplicaciones lógicas y sensores (NEMS-in-CMOS)' (Ref:TEC2012-32677)

Additionally the work developed during the PhD was granted with one GICSERV project (2010–2012) developed at the Institut de Microelectronica de Barcelona–Centro Nacional de Microelectronica (IMB–CNM) called 'Fabricación de elementos resonantes NEMS en tecnología CMOS de 65nm' whose aim was to develop a post-CMOS releasing process in ST 65nm CMOS technology.

## 1.4 Thesis outline

After this introduction chapter, the thesis has six additional chapters and 2 appendixes:

**Chapter 2** describes the main theory of beam resonators with electrostatic transduction and capacitive read-out.

**Chapter 3** is focused on the mechanical switches theory. In addition the ring oscillator theory and simulations are presented. The conditions to obtain a stable periodic response will be established.

**Chapter 4** is focused on the fabrication process of N/MEMS structures in ST 65nm commercial CMOS technology. In this chapter the state of the art of CMOS–MEMS will be establish. Then ST Microelectronics 65nm commercial CMOS technologies will be described and a detailed description of the post-CMOS releasing process of STM 65nm technology will be exposed. Additionally resonator developed in the different available layers will be described.

**Chapter 5** shows the experimental results of the mechanical switches developed using three different approaches: Switches based on AMS 0.35  $\mu\text{m}$  back-end metal layer, switches based on AMS 0.35  $\mu\text{m}$  capacitive MIM module and ST 65nm copper back-end metal layer.

**Chapter 6** is dedicated to resonant gate transistor transduction method. First of all, a model based on mass spring dash model and EKV transistor model will be presented. Next polysilicon resonators using AMS 0.35  $\mu\text{m}$  will be designed and electrically characterized. Its application as switch and resonator will be studied.

**Chapter 7** is a summary of the scientific contributions of this work. It is intended to recapitulate the achievements of this thesis, as well as to give some perspectives on the continuation of this work.

**Annex A** shows the semi-analytical limit cycle calculation of the ring oscillator configuration.

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**Annex B** presents the different chips that have been designed during this thesis.

# Chapter 2

## CMOS-MEMS resonators basis

---

*In this chapter the theoretical basis of beam resonators with electrostatic actuation and capacitive read-out will be presented. In addition the working principle of mass sensors based on resonators will be presented.*

---

### 2.1 MEMS resonators mechanical model

In this section Euler–Bernoulli equation, that models the dynamic response of MEMS devices, will be presented and solved in order to obtain the natural frequencies of the beam. Right after, a lumped model will be presented (mass–spring–dash) to model the position of a single point of the beam.

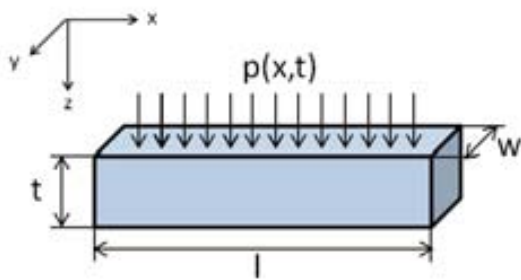
#### 2.1.1 Euler–Bernoulli equation

The dynamic response of MEMS devices under movement can be modeled by the theory of elasticity. It will be assumed that the MEMS are built of an homogeneous and isotropic elastic material that elastically deforms when a force is applied to

it, recovering its original shape. We will assume that this condition is satisfied for small displacement.

With these conditions, and under the assumptions enumerated below, the movement of a cross-section beam can be modeled by Euler-Bernoulli equation 2.1 [22]:

- The beam is subject to pure deflection only (no additional shear or axial force is considered). Transverse deflections do not result in axial torsion or rotational shear forces.
- There is no friction and losses at movement.
- Under bending, cross section remains planar.
- The bending moment is constant or varies slowly.



Parameter	Symbol
Length	$l$
Width	$w$
Thickness	$t$
Cross-section Area	$A=w.t$
Density	$\rho$
Mass	$M$
Moment of Inertia	$I$
Young's coefficient	$E$
Distributed load	$p(x,t)$
Deflection	$u(x,t)$

FIGURE 2.1: Geometry of a squared cross-section beam under consideration.  
In the table the cantilever main parameters are shown.

$$EI(x) \frac{\partial^4 u(x,t)}{\partial x^4} + \rho A(x) \frac{\partial^2 u(x,t)}{\partial t^2} = 0 \quad (2.1)$$

To find the eigenfunctions or natural modes together with the corresponding eigenvalues or natural frequencies, the homogeneous equation 2.1 is solved by employing a separation of variables approach. Assuming that  $u(x,t) = \phi(x)z(t)$ :

$$\frac{\phi^{iv}(x)}{\phi(x)} = -\frac{\rho A}{EI} \frac{\ddot{z}(t)}{z(t)} \quad (2.2)$$

with  $\phi^{iv}(x) = \frac{d^4\phi}{dx^4}$ . Note that each side of the equation depends on a different independent variable. Consequently, they must both be equal to a constant,  $\beta^4$ , which allows to split the partial differential equation into two ordinary differential equations

$$\begin{cases} \phi^{iv}(x) - \beta^4\phi(x) = 0 \\ \ddot{z}(t) + \omega^2 z(t) = 0 \end{cases} \quad (2.3)$$

where  $\omega^2$ , angular frequency, is given by:

$$\omega^2 = \frac{\beta^4 EI}{\rho A} \quad (2.4)$$

Note that the top equation in 2.3 determines the shape that the cantilever takes while is vibrating, while the bottom equation determines the time-varying amplitude of the vibrations. Six initial conditions are required to solve 2.3. Two of them,  $z(0)$  and  $\dot{z}(0)$ , can be arbitrary chosen. However, a simple analysis shows that

$$z(t) = a \cos(\omega t + \varphi) \quad (2.5)$$

where  $\varphi = \arccos(z(0)/a)$  and  $a = \sqrt{(z(0))^2 + (\dot{z}(0)/\omega)^2}$ . Clearly,  $\omega$  (see equation 2.4) determines the natural frequency of oscillation associated with the shape  $\phi(x)$ . The general solution of  $\phi(x)$  can be expressed as a sum of trigonometric functions:

$$\phi(x) = A_n \sin(\beta x) + B_n \cos(\beta x) + C_n \sinh(\beta x) + D_n \cosh(\beta x) \quad (2.6)$$

In order to obtain the values of  $A_n, B_n, C_n$  and  $D_n$  the Dirichlet boundary conditions need to be established, depending on the beam configuration. In table 2.1, the Dirichet boundary conditions and the values of these parameters are shown for a cantilever and C.C.Beam configuration.



	Cantilever	C.C. Beam
Schematic		
Dirichlet boundary conditions	$\phi(0) = 0$ $\frac{\partial \phi(0)}{\partial x} = 0$ $\frac{\partial^2 \phi(l)}{\partial x^2} = 0$ $\frac{\partial^3 \phi(l)}{\partial x^3} = 0$	$\phi(0) = 0$ $\frac{\partial \phi(0)}{\partial x} = 0$ $\phi(l) = 0$ $\frac{\partial \phi(l)}{\partial x} = 0$
$A_n \ B_n \ C_n \ D_n$	$A_n = -C_n$ $B_n = -D_n$ $\frac{A_n}{B_n} = -\frac{\cosh(\beta l) + \cos(\beta l)}{\sinh(\beta l) + \sin(\beta l)}$ $\frac{A_n}{B_n} = -\frac{\sinh(\beta l) - \sin(\beta l)}{\cosh(\beta l) + \cos(\beta l)}$	$A_n = -C_n$ $B_n = -D_n$ $\frac{A_n}{B_n} = -\frac{\sin(\beta l) + \sinh(\beta l)}{\cos(\beta l) - \cosh(\beta l)}$ $\frac{A_n}{B_n} = -\frac{\cos(\beta l) - \cosh(\beta l)}{\sin(\beta l) - \sinh(\beta l)}$
Frequency eq.	$\cosh(\beta l) \cdot \cos(\beta l) = -1$	$\cosh(\beta l) \cdot \cos(\beta l) = 1$
$\beta_n$ values	$\beta_1 l = 1.87$ $\beta_2 l = 4.69$ $\beta_2 l = 7.85$ ...	$\beta_1 l = 4.73$ $\beta_2 l = 7.85$ $\beta_2 l = 10.99$ ...

TABLE 2.1: Dirichlet boundary conditions, coefficients, frequency equations and  $\beta_n$  values for a cantilever and c.c. beam configuration.

In both cases, the two equations, that fixes the ration  $A_n/B_n$  can be combined (frequency equation row in table 2.1), obtaining a transcendental equation whose numerical solutions will fix the natural modes of the beam (last row of table 2.1 shows the first three values for both configurations). Consequently expression 2.3 has countably many solutions of the form (assuming  $D_n = 1$ ,  $B_n = 1$ ):

$$z_n(t) = a_n \cdot \cos(\omega_n t + \varphi_n) \quad (2.7)$$



$$\phi_n(x) = \cosh(\beta_n x) - \cos(\beta_n x) - \frac{\cosh(\beta_n l) + \cos(\beta_n l)}{\sinh(\beta_n l) + \sin(\beta_n l)} (\sinh(\beta_n x) - \sin(\beta_n x)) \quad (2.8)$$

$$\phi_n(x) = \cos(\beta_n x) - \cosh(\beta_n x) - \frac{\sin(\beta_n l) + \sinh(\beta_n l)}{\cos(\beta_n l) - \cosh(\beta_n l)} (\sin(\beta_n x) - \sinh(\beta_n x)) \quad (2.9)$$

(2.8 for a cantilever and 2.9 for a c.c. beam) where  $\omega_n$ ,  $\beta_n$ ,  $a_n$  and  $\varphi_n$  are related as equations 2.5 and 2.4 show. The first three modes shape functions for both configurations are shown in figure 2.2.

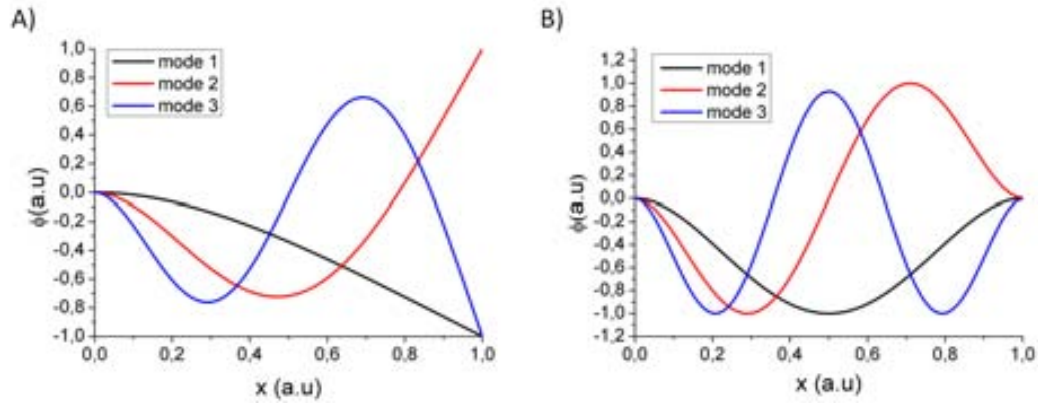


FIGURE 2.2: First three modes shapes for a A)cantilever and B) C.C. Beam.

Note from the linearity of the differential operator that the complete solution of equation 2.1,  $u(x, t)$ , is given by

$$u(x, t) = \sum_{n=0}^{\infty} \phi_n(x) z_n(t) \quad (2.10)$$

The mode shape functions satisfy the next two conditions:

$$\int_0^l \phi_i(x) \phi_j(x) dx = 0 \quad (2.11)$$

$$\int_0^l [\phi_i(x)]^2 dx = l \quad (2.12)$$

The second property (2.12) is imposed in order to have a solution uniquely determined. These properties are the basis of the Galerkin method. Galerkin method is a reduced order method (ROM) (based on domain [23]), that basically consists on approximate a coupled sets of partial differential equations (PDEs) by a small set of ordinary differential equations (ODEs). In order to do it [24]:

- The solution of the original problem can be expressed as a linear combination of a limited set of basis functions (normally the eigenmodes of the structure).
- Projecting the PDEs on this set of basis functions (Galerkin projection) a set of ODEs are obtained whose unknowns are the coefficients of the linear combination.

The dynamic behavior of a mechanical switch will be studied using this method in section 3.6.

Finally, knowing that the moment of inertia of a rectangular cross section beam is given by equation 2.13, a general expression can be obtained for the natural resonant frequencies of beams (equation 2.14), substituting 2.13 in expression 2.4.

$$I = (tw^3)/12 \quad (2.13)$$

$$f_n = \frac{(\beta_n l)^2 w}{2\pi l^2} \sqrt{\frac{E}{12\rho}} \quad (2.14)$$

### 2.1.2 Mass–spring–dash model

A lumped model can be developed if just the movement of the maximum displacement point is modeled (in a cantilever, the free extreme point and the central point

in a c.c.beam configuraton). An effective mass is associated to this point that is attached to a spring fixed in the other extreme (see figure 2.3). A non conservative system is supposed and losses are modeled by a damping factor.

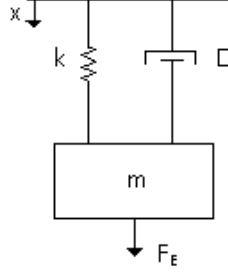


FIGURE 2.3: Mass-spring model with damping.

In this system, the equation of motion is given by:

$$m_{eff}\ddot{x} + D\dot{x} + kx = F_E \quad (2.15)$$

where  $m_{eff}$  is the effective mass associated to the beam,  $k$  the effective spring constant,  $D$  is the damping coefficient and  $F_E$  is the external force acting on the mass.

The value of the effective mass and spring constant depend on the resonant mode. It seems intuitively that in a c.c. beam configuration the second mode spring constant value is bigger than the value of the first mode, as the structures moves less than in the fundamental mode. This argument can be applied to effective mass too. The effective mass can be smaller than the physical mass of a given structure if just a small portion of it is moving.

The effective mass value of a structure resonating in one of its mode shapes is given by [8]:

$$m_{eff} = \int \rho |\phi_n^2(x)| dx \quad (2.16)$$

where  $\rho$  is the mass density and  $\phi_n$  the mode shape (see equations 2.8, 2.9 and table 2.1 for cantilever and c.c. beam configurations). For example, in the case of a cantilever resonating at one of its modes:

$$m_{eff}^c = \int \rho |\phi_n^2(x)| dx = \rho w t \int_0^l \left[ \frac{\phi_n(x)}{\phi_n(l)} \right]^2 dx = \frac{3\rho w l t}{(\beta_n l)^4} \quad (2.17)$$

where  $\phi_n(x)$  is given by equation 2.8 (note how its value has been normalized requiring that the maximum of the mode shape is one). Note how its value depends on the eigenvalues of each resonant mode.

Following this procedure the effective mass of a c.c. beam can be obtained:

$$m_{eff}^{cc} = \frac{192\rho w l t}{(\beta_n l)^4} \quad (2.18)$$

With the effective mass and the resonance frequency known, the effective spring constant is obtained from (where  $\omega_n = 2\pi f_n$ ,  $f_n$  given by expression 2.14 ):

$$\omega_n^2 = \frac{k}{m_{eff}} \quad (2.19)$$

The values of the effective spring constant for a cantilever (equation 2.20) and c.c. beam (equation 2.21) configuration with a constant cross section (in-plane movement):

$$k = \frac{3EI}{l^3} = \frac{E}{4} t \left( \frac{w}{l} \right)^3 \quad (2.20)$$

$$k = \frac{192EI}{l^3} = 16Et \left( \frac{w}{l} \right)^3 \quad (2.21)$$

where  $I$  is the moment of inertia of a rectangular cross section beam (expression 2.13).

The damped equation 2.15 can be expressed in terms of the resonant frequency:

$$\ddot{x} + 2\zeta\omega_o\dot{x} + \omega_o^2x = 0 \quad (2.22)$$

where  $\zeta = D/2m_{eff}\omega_o$ .

For  $0 \leq \zeta < 1$  the system is underdamped and its response to a perturbation will be an oscillation at the natural damped frequency  $w_d$ , which is a function of the natural frequency and the damping ratio (expression 2.24). Note how the amplitude of the oscillation is fixed by the losses of the system ( $\zeta$ ).

$$x(t) = e^{-\zeta\omega_o t} (A\cos(\omega_d t) + B\sin(\omega_d t)) \quad (2.23)$$

where

$$\omega_d = \omega_o \sqrt{1 - \zeta^2} \quad (2.24)$$

For an underdamped system the damping factor can be approximated to:

$$\zeta = \frac{1}{2Q} \quad (2.25)$$

being Q the quality factor (ratio between the total system energy and the average energy loss in one radian at resonance frequency).

Taking the Laplace transform of equation 2.22, we can obtain the transfer function of the system.

$$H(s) = \frac{1/m_{eff}}{s^2 + (\omega_o/Q)s + \omega_o^2} \quad (2.26)$$

In figure 2.4 its frequency response is represented. It can be observed how a resonant peak appears at  $\omega_d$  (which is  $\omega_d \cong \omega_o$  due to the small values of  $\zeta$ ) and how its amplitude increase as  $Q$  has a bigger value.

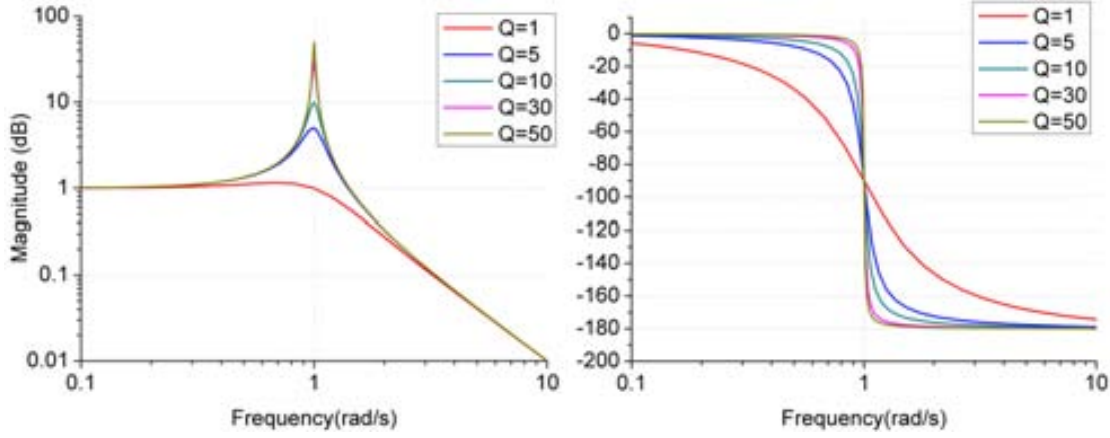


FIGURE 2.4: Frequency response for different quality factors ( $Q$ ) ( $m_{eff} = \omega_o = 1$ ).

The quality factor of the system can be obtained experimentally from the magnitude and phase frequency response. In the magnitude response, the quality factor is the ratio between the center frequency of the peak ( $f_o$ ) and the bandwidth (BW) which is the frequency interval at which the output power has dropped to half of its mid-band value (see expression 2.27)

$$Q = \frac{f_o}{BW_{3dB}} \quad (2.27)$$

The  $Q$  can be obtained from the phase magnitude too:

$$Q = f_o \frac{\pi}{360} \frac{\partial \phi}{\partial f} \quad (2.28)$$

being  $\frac{\partial \phi}{\partial f}$  the phase slope of the graph at the resonance frequency.

The response of the system (equation 2.15) (in a steady state) when it is excited with a sinusoidal force  $F_E = A_c \sin(\omega t)$  is given by expression:

$$x(t) = \frac{A_c/m_{eff}}{\sqrt{(\omega_o^2 - \omega^2)^2 + \frac{\omega\omega_o}{Q}}} \sin(\omega t + \theta) \quad (2.29)$$

It shows how a sinusoidal solution will be found whose amplitude will be maximum for an excitation signal equal to the structure resonant frequency ( $\omega = \omega_o$ ). In addition, it can be observed how the Q factor will fix the maximum amplitude.

## 2.2 Transduction between mechanical and electrical domain

### 2.2.1 Introduction

A key element on MEMS design is how to transform a voltage or current into a force in order to induce movement in the micromechanical structure and how to turn its movement into an electrical output signal that can be processed by the circuitry. This coupling between the electrical and mechanical domain is performed by the transduction methods used in the readout and excitation schemes (figure 1.1).

Excitation schemes based on electrothermal [25], magnetive [26], piezoelectric [27] or electrostatic [28] schemes have been successfully implemented. On the other hand, the movement of the structures has also been detected thanks to optical [29], piezoresistive [30], piezoelectric [31], capacitive [27] or based on solid state devices [32] [33] transduction methods.

However as the dimensions of the MEMS structures are scaled to nanometer range the actuation and detection of their sub-nanometer displacements at high frequencies is becoming one of the most important challenges.

In this section we will focus on the electrostatic excitation and capacitive readout, as they show an easy simple principle, fabrication and implementation using a CMOS approach.

### 2.2.2 Electrostatic actuation

In order to apply an electrostatic force to excite the structure ( $F_E$ ) (see equation 2.15) and induce its movement, a fixed electrode (driver) is placed at one side of the resonator (for an in-plane movement) at a distance  $s$  (actuation gap).

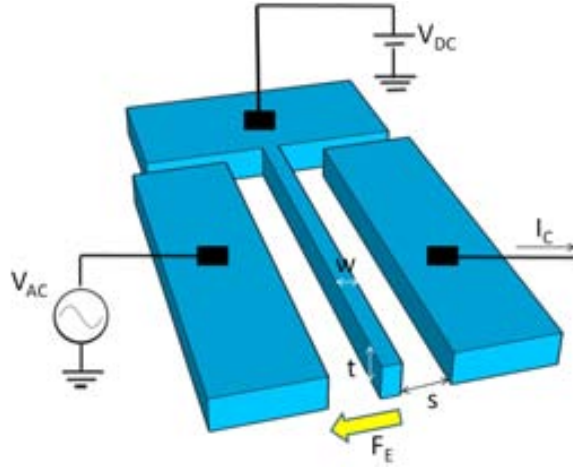


FIGURE 2.5: Schematic view of a two ports c.c beam configuration with electrostatic actuation and capacitive readout.

At movement the driver and the beam forms a variable capacitor that depends on the gap and the position of the beam:

$$C = \frac{\epsilon l t}{s - x} = C_o \frac{s}{s - x} \quad (2.30)$$

where  $C_o = \epsilon A/s$  is the capacitance with zero displacement, being  $A$  the coupling area ( $A=l \cdot w$ , for an in-plane configuration and  $A=l \cdot t$  for an out-of-plane configuration) and  $\epsilon$  the permittivity of the medium. Applying a time-varying voltage difference  $\Delta V_{in}$  across this variable capacitor  $C$ , generates an input electrostatic force  $F_E$  that can be obtained from the energy stored in the capacitor:

$$\begin{aligned} F_E &= -\frac{dW}{dx} = -\frac{\partial}{\partial x} \left( \frac{1}{2} C \Delta V_{in}^2 \right) = \\ &= -\frac{1}{2} \Delta V_{in}^2 \frac{\partial C}{\partial x} = -\frac{1}{2} \Delta V_{in}^2 \frac{\partial}{\partial x} \left( \frac{\epsilon l t}{s - x} \right) = -\frac{1}{2} \Delta V_{in}^2 \frac{\epsilon A}{(s - x)^2} \end{aligned} \quad (2.31)$$



The negative sign indicates that the force is always attractive. For sufficiently large nominal gaps and small forces, the displacement is much smaller than the gap ( $x \ll s$ ) and thus  $\partial C/\partial x$  can be approximated as a constant whose value is determined by the capacitor dimensions. Doing so yields

$$\frac{\partial C}{\partial x} \approx \frac{\varepsilon A}{s^2} = \frac{C_o}{s} \quad (2.32)$$

Taking into account this assumption the excitation force 2.31 when a  $V_{DC}$  voltage is applied to the beam and an AC driving voltage ( $V_{AC}$ ) is applied to the electrode ( $\Delta V_{in} = V_{DC} + V_{AC}\cos(\omega t)$ ) is given by:

$$\begin{aligned} F_E &= -\frac{1}{2}\Delta V_{in}^2 \frac{C_o}{s} = -\frac{1}{2}\frac{C_o}{s}(V_{DC} + V_{AC}\cos(\omega t))^2 = \\ &= -\frac{1}{2}\frac{C_o}{s} \left( V_{DC}^2 + 2V_{DC}V_{AC}\cos(\omega t) + \frac{1}{2}V_{AC}^2 + \frac{1}{2}V_{AC}^2\cos(2\omega t) \right) \end{aligned} \quad (2.33)$$

As it can be observed, the electrostatic excitation force is composed by three component at different frequencies; 0,  $\omega$  and  $2\omega$ . In order to excite movement at  $\omega$  (dominant term) the DC voltage has to be much bigger than the AC voltage  $V_{DC} \gg V_{AC}$ .

When the condition ( $x \ll s$ ) is not satisfied the capacitance variation at movement can not be considered constant (equation 2.32). For small displacement variation  $\frac{\partial C}{\partial x}$  can be obtained using Taylor's series approximation as:

$$\begin{aligned} F_E &= -\frac{1}{2}\Delta V_{in}^2 \frac{\partial}{\partial x} \left( C_o \frac{s}{s-x} \right) = \\ &\approx -\frac{1}{2}\Delta V_{in}^2 \frac{C_o}{s} \left[ 1 + 2\left(\frac{x}{s}\right) + 3\left(\frac{x}{s}\right)^2 + \dots + (n+1)\left(\frac{x}{s}\right)^n \right] \approx \\ &\approx -\frac{1}{2}\Delta V_{in}^2 \frac{C_o}{2s} \left[ 1 + 2\left(\frac{x}{s}\right) \right] \end{aligned} \quad (2.34)$$

For small displacement, just the first two terms can be considered. As it can be observed, there is constant value that just depend on the voltage (in fact is the electrostatic force under the assumption than  $x \ll s$  (equation 2.33) and other term than depend on the cantilever position ( $x$ ). The electrostatic force acts like a spring in the opposite direction to the elastic recovering force of the beam. This effect, called spring softening, can be modeled defining an effective spring constant  $k_{eff}$  [32]:

$$k_{eff} = k - \frac{C_o \langle \Delta V_{in}^2 \rangle}{s^2} \quad (2.35)$$

Looking at the expression 2.19 it is clear that the spring softening will affect to the resonant frequency too.

$$f_{o-eff} = \sqrt{\frac{k_{eff}}{m_{eff}}} = f_o \sqrt{1 - \frac{\langle \Delta V_{in}^2 \rangle C_o}{k s^2}} \quad (2.36)$$

A lower resonant frequency will be obtained as the voltage is increased.

### 2.2.3 Capacitive Read-out

In order to detect the movement of the resonator capacitive read-out is an attractive solution due to its easy implementation, low noise and zero power consumption. In figure 2.6 the polarization of the beam and the two electrodes are shown, together with the capacitances formed by the different conductive layers.

As it can be observed, the read-out electrode forms two different capacitances: one with the beam ( $C_R$ ) and another with the excitation electrode ( $C_P$ ). The capacitance that forms with the beam varies when it is oscillating, generating a current ( $I_M$ ):

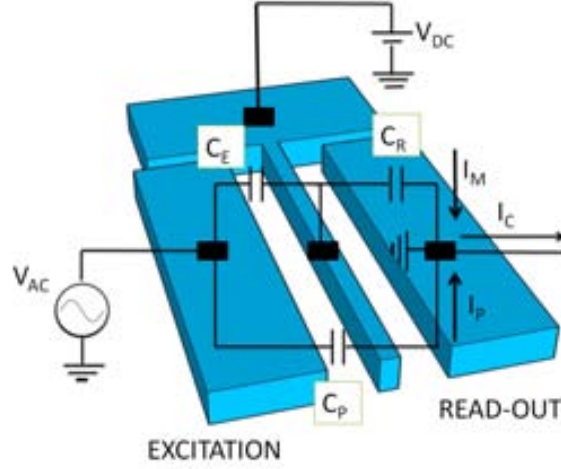


FIGURE 2.6: Schematic view of a two ports c.c beam configuration with electrostatic actuation and capacitive readout.

$$\begin{aligned}
 I_M &= \frac{\partial}{\partial t} (C \cdot V) = V_{DC} \frac{\partial C}{\partial t} = V_{DC} \frac{\partial C}{\partial x} \frac{\partial x}{\partial t} \approx \\
 V_{DC} \frac{\partial C}{\partial x} \frac{\partial x_o \sin(\omega t)}{\partial t} &= V_{DC} \frac{\partial C}{\partial x} \omega x_o \cos(\omega t)
 \end{aligned} \tag{2.37}$$

The motional current depends on the resonance amplitude ( $x_o$ ), oscillation frequency ( $\omega$ ), DC voltage ( $V_{DC}$ ) and the gradient of the capacitance between the driver and the resonator. In order to estimate the motional current at resonance, the next relations have to be establish first, the amplitude of motion for a given force and the force for a given  $V_{AC}$  polarization. This last relation was obtained in equation 2.33 and it is called electromechanical coupling ( $\eta$ ):

$$\frac{F_E(\omega)}{V_{AC}} = V_{DC} \frac{\partial C}{\partial x} \approx V_{DC} \frac{C_o}{s} = \eta \tag{2.38}$$

Electromechanical coupling fixes how good is the transduction between the mechanical and electrical domain and its value depend on the gap ( $s$ ), coupling capacitance ( $C_o$ ) and polarization voltage ( $V_{DC}$ ). Now, the relation between the force and the movement need to be established. As a first approximation and at resonance it can be assumed that the displacement is fixed by the quality factor and the spring constant:

$$x = \frac{QF}{k} \quad (2.39)$$

The motional current at resonance frequency ( $\omega_o$ ) can be now estimated from equations 2.37, 2.38 and 2.39 :

$$I_M \approx Q \frac{V_{DC}^2 V_{AC} \omega_o C_o^2}{k s^2} \quad (2.40)$$

However, the current at the read-out current is not composed exclusively by the motional current, as it can be observed on figure 2.6. A parasitic current will appear due to the variation of voltage  $V_{AC}$  with time:

$$I_P = \frac{\partial}{\partial t}(C_P \cdot V) = C_P \frac{\partial V_{AC}}{\partial t} \quad (2.41)$$

where  $C_p$  is mainly produced by the fringe capacitance between drivers. Note that total current at the read-out electrode is the sum of the motional and parasitic current:

$$I_C = I_M + I_P \quad (2.42)$$

That is why is so important to reduce the parasitic current, as it could mask the motional current and the movement of the beam could not be detected. That is the reason for using two drivers instead of just one to excite and read the beam movement. In a one port configuration the parasitic capacitance between the driver and the beam will be the coupling capacitance ( $C_o$ ) which is much bigger than the parasitic capacitances caused by fringing field.

## 2.3 Electrical model

In order to simulate the MEMS response with the electrical setup (taking into consideration the impedances at its input/output ports) or even with the additional circuitry that can be integrated at its output, an electrical model will be useful. The equivalent circuit using lumped constant element ( $R_m$   $L_m$   $C_m$ ) is show in figure 2.7. The RLC branch models the resonator operating in linear regime and  $C_p$  the parasitic capacitance that can mask the motional current, as it was showed in the previous section.

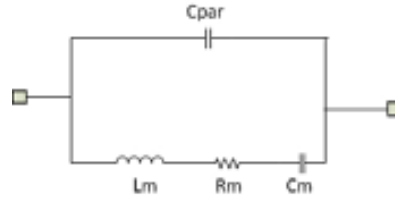


FIGURE 2.7: MEMS Resonator Electrical Model.

To obtain the values of  $R_m$ ,  $C_m$  and  $L_m$  the electromechanical coupling (expression 2.38) relates the current with the velocity when it is used in expression 2.37

$$I_M = \eta \frac{\partial x}{\partial t} \quad (2.43)$$

Substituting in the motion equation 2.15 the electromechanical coupling expressions 2.43:

$$m_{eff} \frac{d}{dt} \left( \frac{I_M}{\eta} \right) + \frac{D}{\eta} I_o + \frac{k}{\eta} \int I_M dt = \eta V_{AC} \quad (2.44)$$

$$\frac{m_{eff}}{\eta^2} \frac{dI_M}{dt} + \frac{D}{\eta^2} I_M + \frac{k}{\eta^2} \int I_M dt = V_{AC} \quad (2.45)$$

Note that this equation is the one that would be obtained from a RLC circuit doing:

$$L_m = \frac{m_{eff}}{\eta^2} \quad (2.46)$$

$$C_m = \frac{\eta^2}{k} \quad (2.47)$$

$$R_m = \frac{\sqrt{km}}{Q\eta^2} \quad (2.48)$$

At resonance frequency ( $\omega = \sqrt{1/L_m C_m}$ ), the effect of  $L_m$  and  $C_m$  are canceled and the branch is reduced to the motional resistance  $R_m$  which accounts for resonator energy losses.

Once the resonator model has been presented, a deeper study of the final resonator configuration is needed to find the parasitic capacitance value. In figure 2.8 the capacitances of a released beam developed in a commercial CMOS technology (AMS 0.35 $\mu$ m) are showed, where each capacitance is specified in table 2.2.

$C_{pp}$	Fringe capacitance between PADS
$C_{pc}$	Fringe capacitance between the cantilever and PADS
$C_{dri}$	Fringe capacitance between drivers
$C_{dc}$	Capacitance between driver and cantilever ( $C_o$ )
$C_{ds}$	Capacitance between drivers and substrate
$C_{cs}$	Capacitance between cantilever and substrate

TABLE 2.2: Schematic of the parasitic capacitances in a 2 Port configuration.

It is important to compute their values trying to make sure that they are not going to be big enough to make impossible the electrical read-out ( $I_M < I_P$ ) and to know their relative position respect the RLC branch, that will fix the motional current. For a two port system in which the resonator is excited through one driver and the readout is performed in another driver electrode, a linear double RLC branch models its electrical response, see figure 2.9 A) [34].

It can be simplified to one simple RLC assuming that the electromechanical coupling coefficients for both drivers are the same  $\eta_n = \eta_m$ , as it is shown in figure

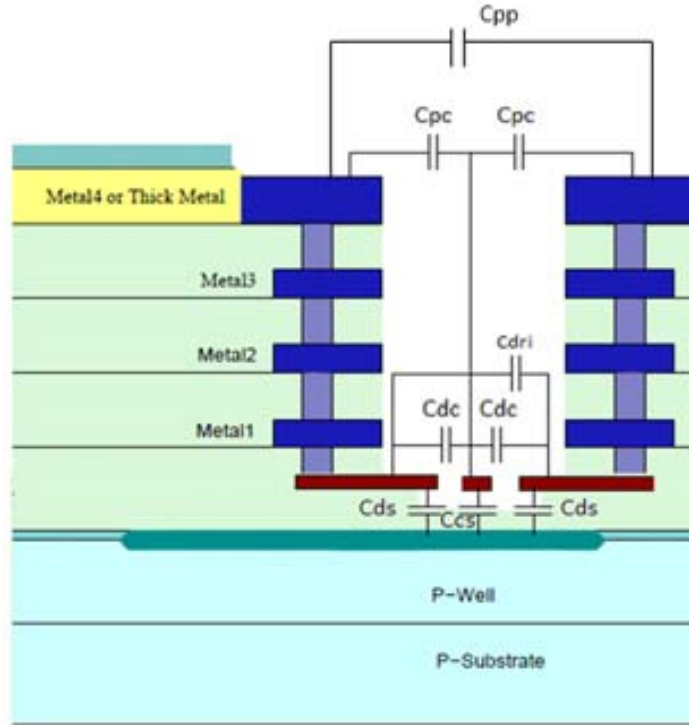


FIGURE 2.8: Parasitic capacitances schematic of a beam implemented in the polysilicon layer of AMS  $0.35\mu\text{m}$  CMOS technology.

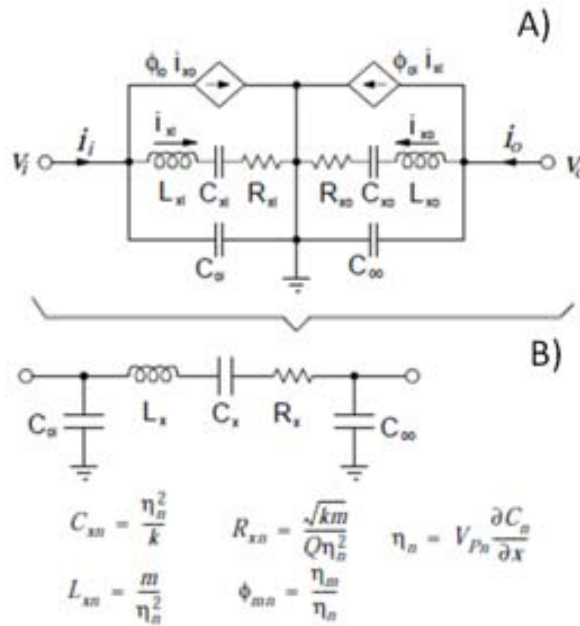


FIGURE 2.9: Equivalent circuit for a two-port micromechanical resonator showing the transformation to the convenient RLC form. Figure extracted from [34].

2.9 B). The series RLC tank represents the resonator electrical model. Then it is necessary to find the relative position of each of the parasitic capacitances to the RLC Branch. As it is a small signal model the conductive layer with a constant DC Bias are grounded. So finally the model is presented in figure 2.10.

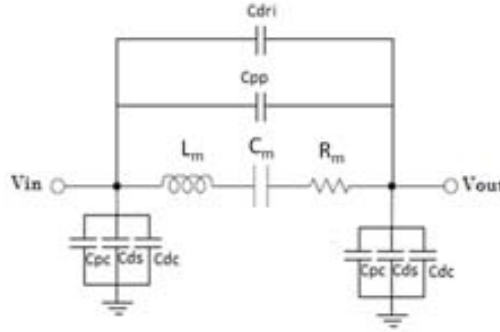


FIGURE 2.10: Complete electrical model for a 2 terminal resonator.

As the model shows the motional current due to the resonator movement can be masked by the capacitances in parallel with the RLC branch. At resonance  $L_m$  and  $C_m$  cancel each other so if the impedance due to the parallel capacitances  $Z_{C||} = 1/j \cdot \omega(C_{dri} + C_{pp})$  is lower than the motional resistance  $R_m$  the resonance response could be masked. It can be clearly observed how for a given  $R_m$  value  $C_{dri}$  and  $C_{pp}$  need to be minimized in order to obtain a good  $I_m/I_p$  ratio. Again it is highlighted in figure 2.11 , which shows the frequency response of the equivalent electrical circuit (figure 2.10) for increasing values of  $C_{PAR} = C_{dri} + C_{pp}$

$$\frac{I_m}{I_p} = \frac{\frac{V_{in}}{R_m}}{\frac{V_{in}}{Z_{C||}}} = \frac{1}{R_m \omega_o (C_{dri} + C_{pp})} \quad (2.49)$$

In addition it can be observed how the anti-resonance peak becomes closer to the resonance frequency,  $f_o$  (see equation 2.50), lowering the resonance peak and masking the intrinsic mechanical quality factor of the resonator (Q).

$$f_p = f_o \sqrt{1 + \frac{C_m}{C_p}} \quad (2.50)$$



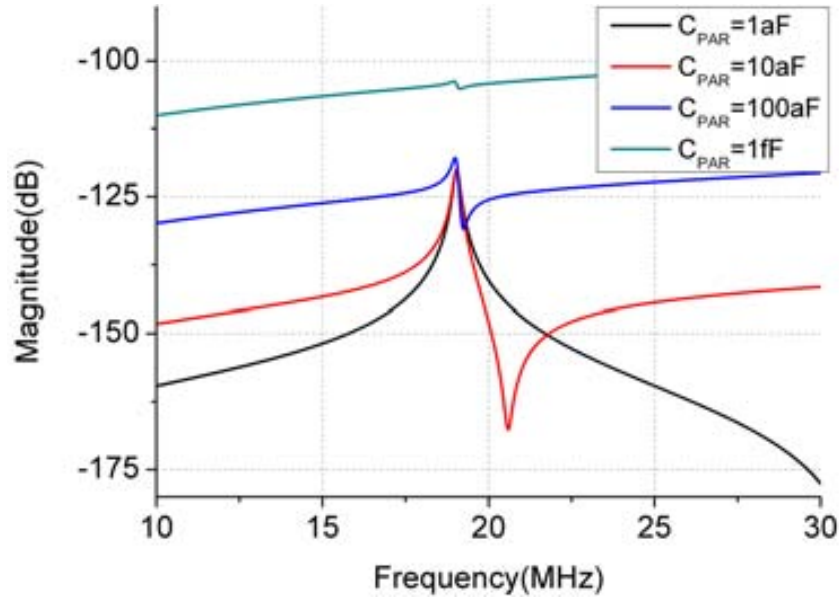


FIGURE 2.11: Effect of the parasitic capacitance on the frequency response of a MEMS resonator with  $R_m = 49.8M\Omega$ ,  $L_m = 41.35H$  and  $C_m = 1.69aF$ .

To calculate these parasitic capacitances the fringing field effect will be considered. Similarly to the parasitic capacitances in CMOS metal adjacent lines. Coventor simulator is capable to evaluate it and also, it can be determinate using an analytical fringe capacitance model [35].

It is important to remark that using additional circuitry at the MEMS output, the parallel capacitance between PADS  $C_{pp}$  is eliminated. Furthermore, the output signal can be processed, amplified and input and output impedance can be matched. In this sense and in order to get a better output signal additional circuitry at the MEMS output could be included, integrated directly from the CMOS technology used [21].

## 2.4 MEMS resonator as a mass sensor

MEMS devices offer many possible principles for the detection of a physical quantity which enables their application as a sensor with often unprecedented sensitivities. Gas sensors, pressure sensors, accelerometers or gyroscopes based on MEMS have become a reality [8].

In our particular case we will take special attention to its application as a mass sensors. Its working principle is not new as it is based on the observed dependence of quartz oscillation frequency on the change in surface mass. It implies that a small change in the resonator mass induces a linear change in the resonance frequency, that can be measured:

$$\Delta m = C f_n \quad (2.51)$$

We assume that the added mass on the beam does not produce any change in the spring constant (for a mass much lower than the mass of the resonator, the stiffness effects can be neglected, and the main contribution corresponds to the deposited mass), so under this assumption, when a punctual mass is added ( $\Delta m$ ) a down shift on the resonance frequency ( $\Delta f_n$ ) is produced according to equation:

$$f_n - \Delta f_n = \frac{1}{2\pi} \sqrt{\frac{k}{\Delta m + m_{eff}}} \quad (2.52)$$

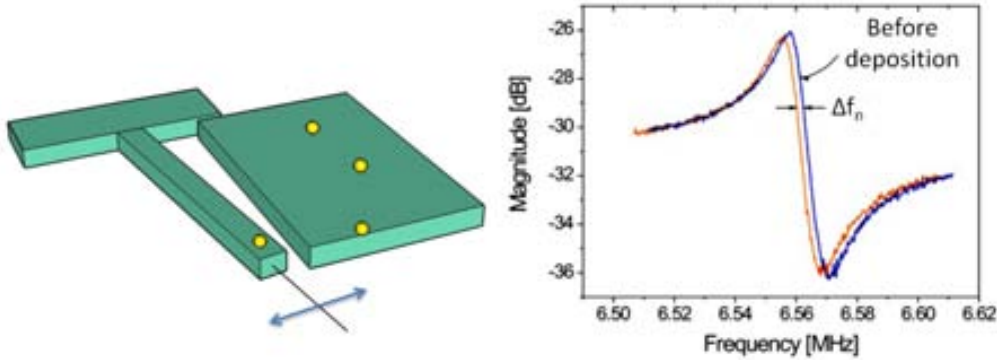


FIGURE 2.12: Schematic diagram of MEMS resonator mass sensing working principle. The added mass down shift the MEMS resonant response.

Looking at equation 2.52, it can be easily appreciated the deep impact that will have in the performance of the sensor the miniaturization of MEMS devices. The reduction of MEMS dimensions translate into a smaller effective mass value (see equations 2.17 and 2.18) and the lower the mass of the resonator, the higher the relative change of mass provoked by the deposition of a determinate mass, and therefore the higher the change in the resonance frequency. In addition, higher

operating frequencies are reached as the MEMS devices are scaled so their resulting absolute frequency shift is larger. The minuscule mass, high operating frequencies and high quality factors (high frequency stability) of NEMS have pushed the limits of detection down to yoctograms range [5].

The most important parameters to characterize the performance of a sensor are its sensitivity and resolution. The IEEE standard dictionary of electrical and electronics defines the sensitivity of any sensor as the ratio of the magnitude of its response to the magnitude of the quantity measured [21]:

$$S_m = \frac{\Delta m}{\Delta f_n} \approx -\frac{2m_{eff}}{f_n} \quad [kg/Hz] \quad (2.53)$$

Additionally, the inverse of the mass sensitivity is called responsivity ( $R_m$ ):

$$R_m = \left| \frac{\partial f_n}{\partial m} \right| \quad [Hz/kg] \quad (2.54)$$

These equations are valid for punctual mass depositions, where the mass is added at the free-end of a cantilever or at the center of a c.c. beam. If the sensitivity is expressed in terms of the resonator dimensions and material properties (substituting effective mass, equations 2.17 and 2.18, and resonant frequency equation (2.14, in expression 2.54):

$$S_m^c \approx 3\rho \sqrt{\frac{\rho}{E}} l^3 t \quad (2.55)$$

$$S_m^{cc} \approx 0.75\rho \sqrt{\frac{\rho}{E}} l^3 t \quad (2.56)$$

(where  $S_m^c$  is the mass sensitivity of a cantilever and  $S_m^{cc}$  for a c.c. beam). Mass sensitivity shows which amount of mass produce a frequency shift of 1 Hz so the lower is its value better is the device as mass sensor. As it can be appreciated in mass sensitivity expressions, if the length of the structure is scaled by a factor  $\lambda$

( $l_S=1/\lambda$ , being  $\lambda > 1$ ), the mass sensitivity value is reduced by a factor of ( $\lambda^3$ ), that is why miniaturization of MEMS devices has improve mass detection significantly, as it was mentioned before. In fact the best mass sensors have been developed using a bottom-up approach thanks to its intrinsic small dimensions.

The mass sensor resolution is the minimum detectable mass  $\Delta m_{min}$ . In mass sensors based on nanomechanical resonators, this parameter is determined by the mass sensitivity and the minimum detectable shift of the resonance frequency  $\Delta f_{min}$ :

$$\Delta m_{min} = S_m \Delta f_{min} \quad (2.57)$$

Ideally the limit of  $\Delta f_{min}$  is imposed by the resonator thermal noise [16]:

$$\Delta f_{min} = \sqrt{\frac{k_B T}{E_C} \frac{f_o BW}{2\pi Q}} \quad (2.58)$$

where  $k_B$  is the Boltzmann constant,  $T$  the temperature,  $E_C = m_{eff} \omega_o^2 < x^2 >$  is the kinetic energy of the beam at movement,  $BW$  is the readout bandwidth,  $f_o$  the resonant frequency and  $Q$  is the quality factor. However in most cases, the readout system noise limits the mass resolution of the sensor system avoiding to achieve the mass resolution set by equation 2.58.

# Chapter 3

## Micromechanical switches and ring oscillator theory

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*Micromechanical switches not only has raised as a solution to the slowing down of CMOS scaling pace according to Moore's law, they are the key element to introduce MEMS device into digital applications, and extrapolate to this domain some of their applications as mass sensing. In this chapter its operation principles and its state of the art of MEMS switches will be established in a first stage. Then a novel oscillator approach built exclusively with mechanical switches will be presented.*

---

### 3.1 Introduction

As it was mentioned in the introduction chapter, to develop an on chip mass sensing system, besides a MEMS device an additional integrated circuitry is necessary to drive the resonator at resonance and continuously track its resonant frequency.

As an alternative, we propose a novel ring oscillator configuration composed exclusively of mechanical switches (see figure 3.1). For large enough  $V_{DD}$  bias, the system may start to auto-oscillate, delivering a periodic square voltage at its output, each falling or rising edge corresponding to an impact of one of the switches.

The switches being driven in a dynamic bouncing mode, the oscillation frequency can be shown to be a function of the natural resonance frequency of the mechanical part, as opposed to CMOS ring oscillators where the period of oscillation is governed by electrical delay in the loop. This property of the oscillation frequency can be used for resonant sensing applications. In particular, M/NEMS Ring oscillator may be used as CMOS-less, autonomous resonant sensors, without all the drawbacks associated with the traditional resonant sensing approach relying on an active electronic feedback loop (loop design, MEMS/electronics co-integration, power consumption).

Beside the benefits that the use of mechanical switches as sensing elements provides, there is a growing interest in MEMS switches as an alternative to switches based on transistors, thanks to their energy efficiency. In this next section this point is analyzed.

### 3.1.1 CMOS scaling and power crisis.

Continuous scaling of complementary metal oxide semiconductor (CMOS) devices to the nano scale has been successfully achieved in last decades according to Moore's law (figure 3.2) [1]. The more an integrated circuit (IC) is scaled the higher is its circuit speed, lower is its power dissipation and higher becomes its integration density [36] (see table 3.1). This is translated into a superior performance and cost reduction per chip.

However the transistor size reduction has been attained at an expense of more complex designs and extremely high level performance requirements. New challenges have come out as technology nodes reach the nanometer scale: lithography limitations, short-channels effects, increasing variability.

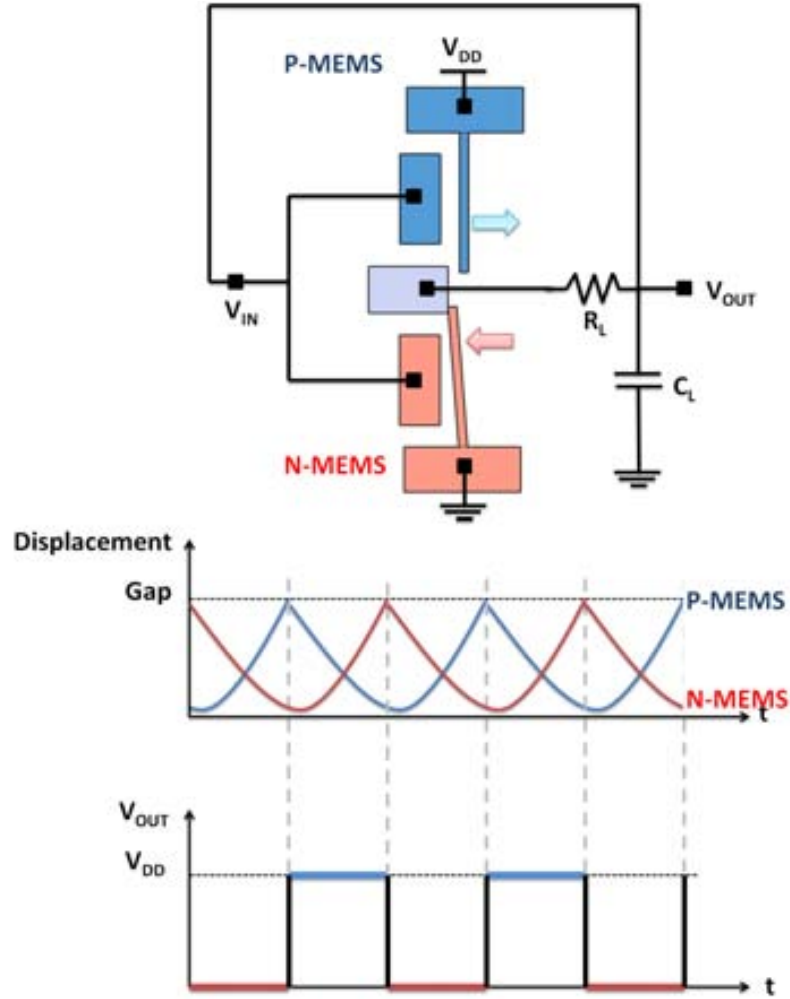


FIGURE 3.1: Schematic representation of a MEMS ring oscillator configuration.

Additionally, as the technology nodes reach the nano scale, the increase in gate and subthreshold leakage current is making almost impossible to continue the same scaling pace than in the past decade and to get energy efficient designs. With each technology node the CMOS supply voltage ( $V_{DD}$ ) and threshold voltage ( $V_{TH}$ ) have been reduced in order to reduce the power consumption, keep the gate overdrive ( $V_{DD}-V_{TH}$ ) and therefore keep performance. However the drain to source current in the OFF state ( $V_{GS} < V_{TH}$ ), increases exponentially decreasing  $V_{TH}$  (see figure 3.3).

In the OFF state the drain to source current,  $I_{DS}$ , is mainly produced by the diffusion of carriers (drift component is almost negligible) [37]. This transport mechanism follows a Boltzmann distribution and therefore the current follows an exponential dependence as equation 3.1 shows [38]:

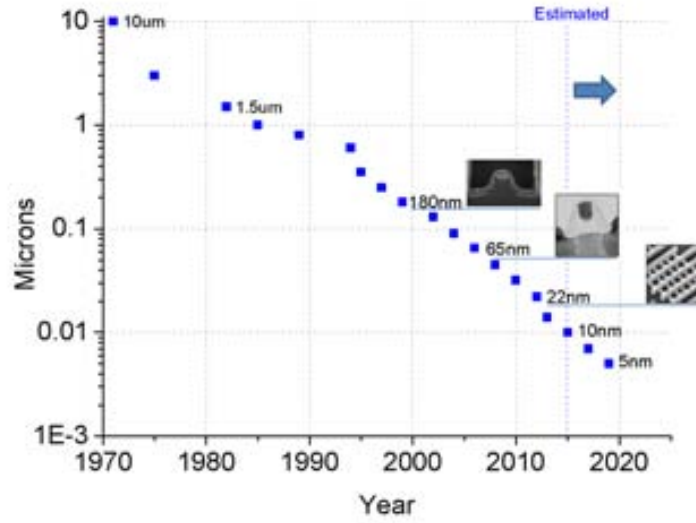


FIGURE 3.2: CMOS Half pitch evolution. Data extracted from [1].

Device and Circuit Parameters	Scaling Factor
Device dimension ( $t_{ox}, L, W$ )	$1/\kappa$
Doping concentration ( $N_B$ )	$\kappa$
Supply Voltage ( $V_{DD}$ )	$1/\kappa$
Electric field (E)	1
Transistor Current	$1/\kappa$
Area(A)	$1/\kappa^2$
Capacitance $\epsilon A/t_{ox}$	$1/\kappa$
Intrinsic delay ( $\tau \sim CV_{DD}/I$ )	$1/\kappa$
Power dissipation ( $P \sim IV_{DD}$ )	$1/\kappa^2$
Power density P/A	1

TABLE 3.1: Rules and results for circuit performance in scaling MOSFET by a factor  $\kappa$  ( $\kappa > 1$ ) keeping a constant electric field. Reproduced from [36].

$$I_{DS} \propto e^{(\psi_s - 2\phi_F)/U_T} \quad (3.1)$$

where  $U_T$  is the thermal voltage ( $(k_B T/q)$ ),  $\phi_F$  the fermi level and  $\psi_s$  the surfaca potential.

In this state,  $V_{GS}$  fixes the value of the surface potential by the capacitor divider formed by the depletion ( $C_d$ ) and oxide capacitance ( $C_{ox}$ )(expression 3.2 ).



$$\frac{d\psi_s}{dV_{GS}} = \frac{C_{ox}}{C_{dep} + C_{ox}} \quad (3.2)$$

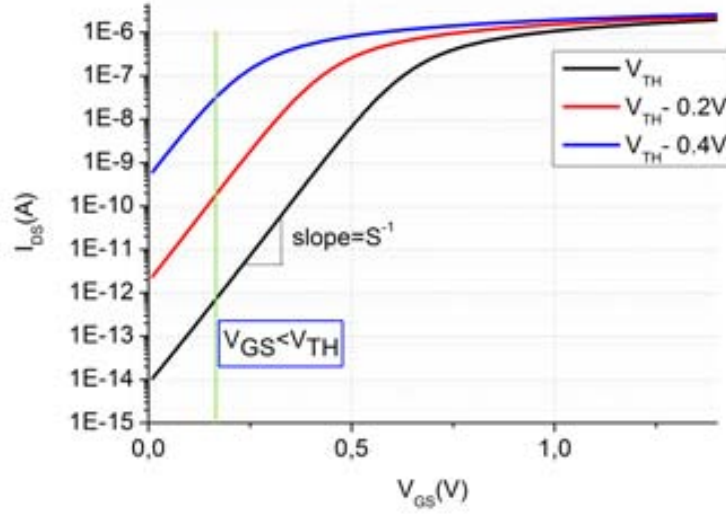


FIGURE 3.3:  $I_{DS}$ - $V_{GS}$  characteristics of a MOSFET. It can be observed how reducing the  $V_{TH}$  voltage higher subthreshold currents are obtained

The inverse of the slope in this region is defined as the subthreshold swing ( $S$ ) and it can be obtained from equation 3.2 and 3.1:

$$S \equiv \left( \frac{d \log_{10} I_{DS}}{dV_{GS}} \right)^{-1} = \left( \frac{d \log_{10} I_{DS}}{d\psi_s} \frac{d\psi_s}{dV_{GS}} \right)^{-1} = \ln(10) \frac{k_B T}{q} \left( 1 + \frac{C_d}{C_{ox}} \right) \quad (3.3)$$

Ideally an infinite slope ( $S=0$ ) would be desired, as it would indicate an abrupt change between ON and OFF state and the possibility to reduce the passive power consumption. However this slope is fundamentally limited to be no less than 60mV/decade ( $(k_B T/q) \ln(10)$ , at 25°C) in the ideal case of  $C_d/C_{ox} = 0$  (not satisfied in practice, sub-threshold swing values are typically around 90 mV/decade for bulk CMOS devices [39]).

With the intention of stop the increasing of  $I_{OFF}$  current the  $V_{TH}$  scaling has slowed down dramatically below 0.3 V [36]. In order to reduce the dynamic energy (proportional to  $V_{DD}^2$ , see equation 3.4)  $V_{DD}$  values are scaled too. However, the

leakage energy also imposes a limit in the reduction of  $V_{DD}$ . Scaling  $V_{DD}$  value,  $I_{ON}$  is reduced too, as it depends on the overdrive  $|V_{DD} - V_{TH}|$ . As a consequence slower response times are got ( $t_{delay} \propto \frac{1}{I_{ON}}$ ) [40]. Moreover the  $t_{delay}$  also affects to the leakage energy (see equation 3.5). So  $V_{DD}$  has an optimal value that minimize total energy. Its value has saturated around 1 V from the 130 nm technology node [36].

$$E_D \propto CV_{DD}^2 \quad (3.4)$$

$$P_S \propto I_{OFF}V_{DD}t_{delay} \quad (3.5)$$

In figure 3.4 the evolution in active and passive power consumption is shown and it can be observed how in the 45nm technology node the leakage power is bigger than the active power for the first time. Additionally, in the right axis, the subthreshold current per micron is shown (at 40°C). In bigger nodes (0.25um) the leakage current per transistor was 2nA/ $\mu m$ . One chip of this node could have ten million transistors per chip, this suppose 20mA/ $\mu m$ . In the new generation nodes like 45nm the leakage current has grown exponentially. In 45nm nanometers the leakage current is 3 $\mu$ A/ $\mu m$ , in these nodes a common chip could have a thousand million of transistors ( $1.10^9$  transistors). This means 3.10<sup>3</sup> A/ $\mu m$ . So it clearly shows the need to solve this problem.

In this direction alternative transistor designs with steeper subthreshold swing have been proposed [1] as double-gate tunnel FET [42] and impact ionization MOSFET [43]. However they still present nonzero  $I_{OFF}$ . At this point, the use of mechanical switches appears. This is not a novel idea. Mechanical elements have been used historically for computing. From the simple abacus to the first numerical wheel developed by Pascal in 1642. Its zenith appeared during the second world war when complex mechanical devices were used to codex information [44]. This renewed interest in mechanical elements is due to the advancements in

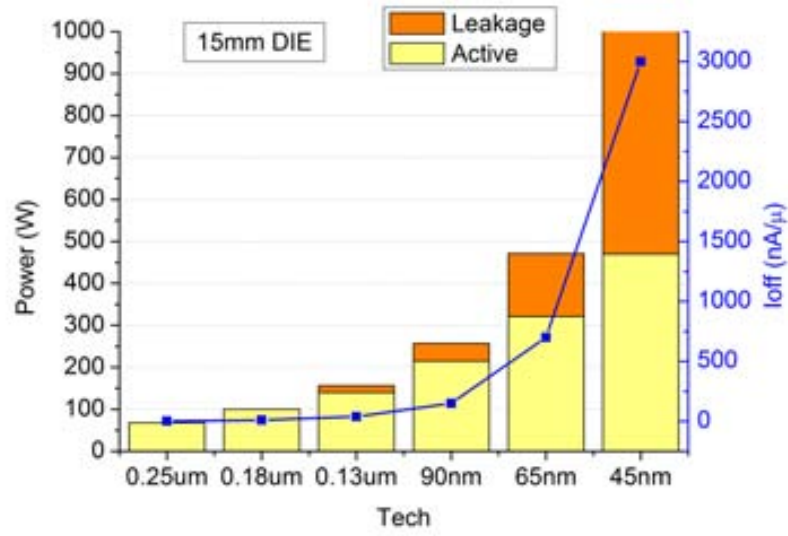


FIGURE 3.4: CMOS Half pitch active and leakage power consumption in a 15mm DIE and Sub-threshold current per micro for different technologies. Data extracted from [41]

planar processing technology over the last decades, particularly the development of surface micromachining processes for microelectromechanical systems (MEMS).

The ideal mechanical switch electrical response is showed in figure 3.5. An abrupt response (ideally infinite slope) between a high current ( $I_{ON}$ ) in the ON state and ideally zero current in the OFF state ( $I_{OFF}$ ) is obtained. This makes the leakage power consumption equals to zero and total power consumption consists only on the active power, so  $V_{DD}$  can be further scaled without any effect on the total energy.

## 3.2 Microelectromechanical contact switches

Microelectromechanical contact switches are composed by a mobile structure that is deflected until it reaches physical contact with an electrode, forming a path for the current to flow and changing the state of the devices. So we have two different states: no contact (OFF state) or contact (ON state).

In the OFF state, the current is limited to vacuum tunneling and Brownian motion displacement currents that appear in the physical gap that separates the mobile

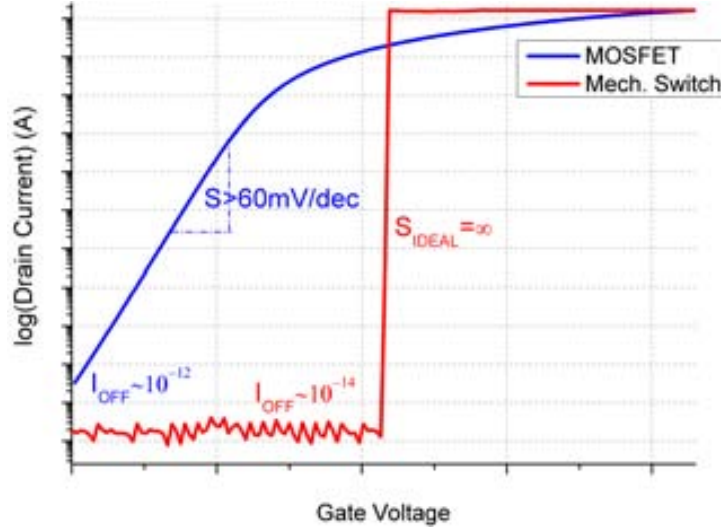


FIGURE 3.5: Solid State transistor and ideal switch electrical response.

structure and the electrode [45]. These currents have low values solving the problem of passive power consumption that traditional CMOS transistors present.

In order to actuate the switches numerous solutions have been proposed in order to generate a force that will be able to close the device. Magnetic, thermal, piezoelectric and electrostatic solutions have been proposed [36]. The main drawback in magnetic actuation is that magnetic and ferromagnetic layers are not compatible with Si micromachining processing. Thermal actuation is dismissed because large quantities of power are needed to actuate the switches. On the other hand piezoelectric and electrostatic actuation have raised as promising alternatives. Piezoelectric materials can achieve large displacement and forces with at low energy and its integration for IC applications has been demonstrated [46]. However, to be an alternative to CMOS devices they would need to be scaled down to smaller dimensions and improvement in material and manufacturing processes. Due to its compatibility with IC industry (materials and processing techniques), scalability and power consumption, electrostatic actuation has raised as the better solution and numerous works have appeared [47][48][49][50]. Our work will focus in this actuation method. Respect the contact mechanism more details will be given on the next section.

### 3.2.1 Operational principles

In figure 3.6 a two terminals (2-T) mechanical switch is shown. The mobile structure is a cantilever and the electrode is placed to a distance ( $s$ ) that will be used to read and excite the contact with the active element. Using this device, the study of the basic operational principles of mechanical switches will be done.

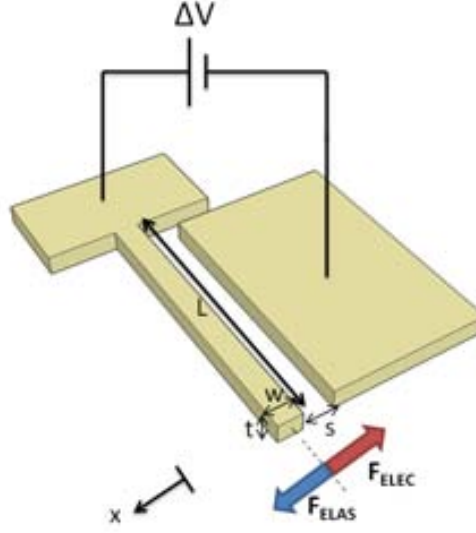


FIGURE 3.6: Two Terminals Switch Schematic.

In order to deflect the active element into physical contact with the opposing electrode a voltage difference between them is applied. As a consequence of this voltage difference an attractive electrostatic force appears (equation 2.31, assuming small displacement around the equilibrium point). On the other hand, an elastic restoring force will oppose to the displacement of the cantilever in the driver direction ( $F_{ELAS} = k \cdot x$ , where  $k$  is given by equation 2.20) as it is shown in Figure 3.6. The total force on the mobile structure at voltage  $\Delta V$  and gap  $s$  using a sign convention that assigns a positive sign for forces that increase the gap, is:

$$F_{TOT} = -\frac{\varepsilon A \Delta V^2}{2(s-x)^2} + k(s-x) \quad (3.6)$$

At a point of equilibrium  $F_{TOT} = 0$  (we assume that the actuation voltage  $\Delta V$  is changing slowly in comparison to mechanical resonance frequency. This allow

for ignoring the inertial effects in the analysis). As the voltage applied across the active element and the electrode is increased, the resulting electrostatic forces are balanced by elastic restoring forces in the active element. While there is not contact between the conductors just a small current due to tunneling effect and brownian motion is observed (state A in Figure 3.7)

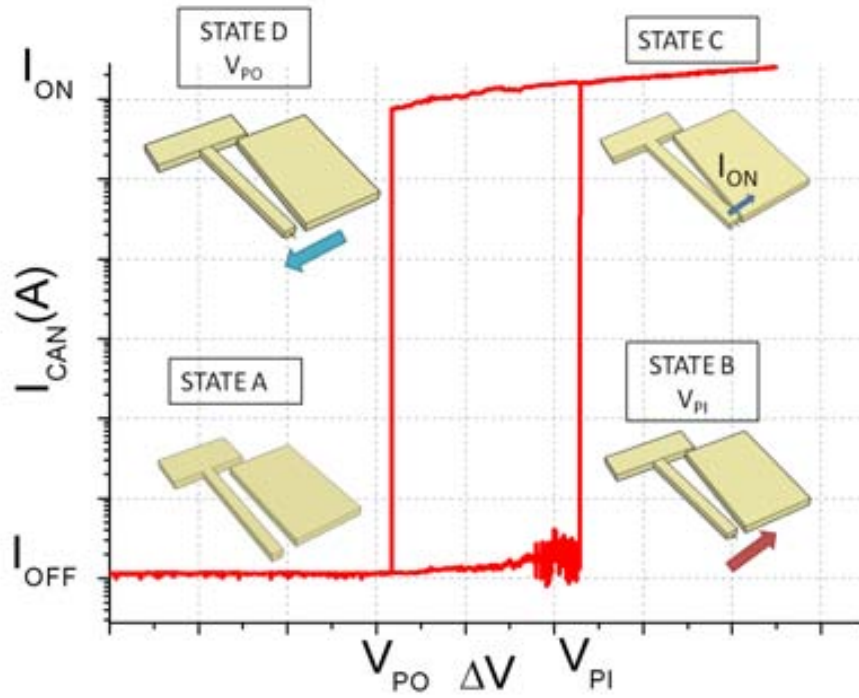


FIGURE 3.7: Schematic of a mechanical switch working principle and electrical response.

As the voltage difference is increased the electrostatic force is balanced by the restoring force until a voltage is reached (Pull-in Voltage  $V_{PI}$ ) in which the system become unstable, collapsing the beam with the electrode. In order to determine this point a stability analysis is required. Stability analysis involves perturbing the position slightly and asking whether or not the net force tends to return to the equilibrium position:

$$\delta F_{TOT} = \left. \frac{\partial F_{TOT}}{\partial x} \right|_{\Delta V} \delta x \quad \delta F_{TOT} = \left( \frac{-\epsilon A \Delta V^2}{(s-x)^3} - k \right) \delta x \quad (3.7)$$

If  $\delta F_{TOT}$  is positive for positive  $\delta x$  then is an unstable equilibrium point, because a small increase creates a force tending to increase it further. If  $\delta F_{TOT}$  is negative, then is a stable equilibrium point. So in order to have a stable equilibrium:

$$k > \frac{-\varepsilon A \Delta V^2}{(s-x)^3} \quad (3.8)$$

Clearly, since the equilibrium gap decreases with increasing voltage, there will be a specific voltage at which the stability of the equilibrium is lost. This is called the pull-in voltage,  $V_{PI}$ . At pull-in, there are two equations that must be satisfied:

$$\sum F = 0 \quad \frac{dF}{dx} = 0 \quad (3.9)$$

$$-\frac{\varepsilon A \Delta V^2}{2(s-x)^2} + k(s-x) = 0 \quad k = \frac{-\varepsilon A \Delta V^2}{(s-x)^3} \quad (3.10)$$

Both conditions are satisfied when  $x=s/3$  [22] and the snap-in voltage can be obtained substituting the pull-in displacement in equation 3.7 and isolating the voltage:

$$V_{PI} = \sqrt{\frac{8ks^3}{27\varepsilon A}} \quad (3.11)$$

A more accurate result is obtained, in the case of cantilever resonator, when it is assumed that the beam sustains a linear deformation shape deflection when it bends to the the driver electrode instead of assume parallel bend toward the electrode. Under this assumption, the snap-in voltage is given by the next expression [51], and in this case the cantilever collapses when its displacement  $x = 0.44 \cdot s$ :

$$V_{PI} = \sqrt{\frac{0.88ks^3}{\varepsilon A}} \quad (3.12)$$

At this point an abrupt current between the two terminal ( $I_{ON}$ ) will appear due to the voltage difference (state B in Figure 3.7). Its value will be fixed by the contact Resistance ( $R_{CO}$ ) between the two conductors (see Contact Resistance section 3.2.2). In this configuration, an increase in the voltage difference will be translate into a bigger current (ohmic behavior will be got (state C in figure 3.7), although it is important to note that this voltage increase will mean a bigger attractive force between the conductors and the value of the contact resistance could vary due to this extra force).

Additionally, It is important to take into account the adhesive contact forces  $F_{Ads}$  that will appear (mainly Van der Waals forces  $F_{VDW}$ ) trying to hold the beam stuck. In order to release the structure the voltage difference is reduced until a voltage is reached (Pull out voltage  $V_{PO}$  in which the elastic recovery forces overcome the electrostatic and adhesive forces reopening the switch ,breaking the contact between the conductor and reducing the current to  $I_{OFF}$  again (State D 3.7).

On the other hand, there are devices whose elastic restoring forces are not big enough to overcome the adhesive forces although the electrical bias is fully removed. These devices operates in a non-volatile way [52], in contrast with other devices that are able to remove the contact (volatile devices [50]). In order to ensure volatile operation high Young modulus materials and large gaps are necessary to obtain large restoring forces ( $F_{ELAS} = k \cdot x$  where k is given by equation 2.20 for a cantilever beam). In contrast these configurations have large snapin voltages (equation 3.12).

The voltage current response got due to the balance of forces shows an hysteretic behavior, in volatile and non-volatile operation (see figure 3.7), that makes this devices accurate for memory [53] and logic applications [54].

An expanded configuration adds an extra electrode in order to excite and read the electrical contact at different voltages (three terminal switches, 3-T) (see figure 3.8). One electrode (gate) is used to push the beam (source) into contact with the



read electrode (drain). In this way current at contact is fixed by the voltage difference between the beam and the read electrode, preventing the structure damage by high currents. No contact between the excitation electrode (gate) and beam is desired so two different gaps need to be defined ( $s_D < s_G$ ) and the condition  $s_D < s_G/3$  need to be satisfied, to prevent the pull-in of the beam with the actuation electrode (gate) when the mobile structures is brought into contact with the read electrode (drain). In addition, in this non-pull-in mode, only surface adhesive force causes the hysteretic switching behavior, so the pull-out voltages are expected to be smaller.

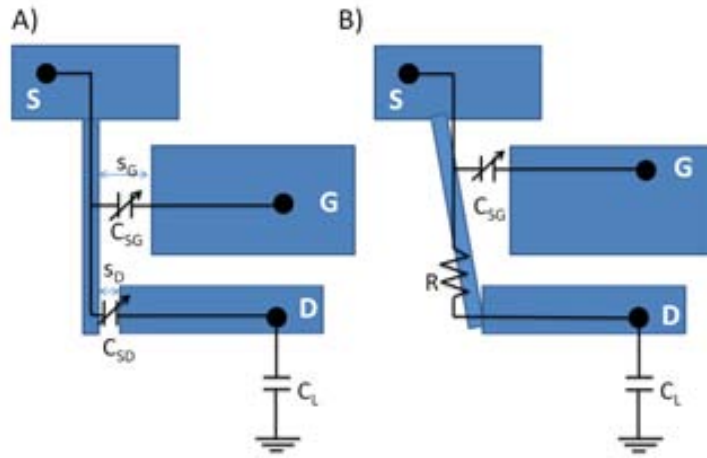


FIGURE 3.8: 3-T switch configuration in equilibrium (A) and at pull-in (B)

Note how using mechanical switches, the trade-off between dynamic and leakage energy as  $V_{DD}$  is scaled, disappear. As the zero OFF-state leakage current can be neglected, the energy per operation just depend on the dynamic component, given by the expression [36]:

$$E_{TOT} = E_{DYN} = \frac{\epsilon_o A}{s_G - s_D} V_{DD}^2 \quad (3.13)$$

A reduction of the value of  $V_{DD}$  will now be translated into a lower total energy.

Mechanical switches voltage time response is represented in figure 3.9 when a voltage ramp is applied to the device gate and a capacitance load is connected to the drain (assuming no charge in the initial moment). As it can be seen the

drain voltage ( $V_{DRAIN}$ ) is null until the pull-in voltage (6 V in this particular case) is reached at the input (gate). Then the beam contacts with the read electrode charging the load capacitance to the beam voltage. It is produced after a certain delay composed by two component: switching time ( $t_S$ ) and the time necessary to charge the capacitance ( $t_{CH}$ ). The switching time is the time that takes the beam to travel from its equilibrium position to the read electrode. Its value for inertial limited systems (small damping) is showed in equation 3.14 [8].

$$t_S = \sqrt{\frac{27}{2}} \frac{V_{PI}}{V_{ACT}} \frac{1}{\omega_o} \quad (3.14)$$

where  $\omega_o$  is the fundamental flexural mode angular frequency 2.19 and  $V_{ACT}$  the actuation voltage. Equation 3.14 shows how short switching times requires high resonant frequency and high actuation voltages in comparison to the pull-in voltage. Once at contact, the time required to charge the load capacitance is added ( $t_{CH}$ ). Its value is given by the RC time constant formed by the load capacitance and the resistance when the contact is produced (expression 3.15 [55] approximation of the rising time of a low pass filter with a single time response constant)

$$t_{CH} \cong 2.2\tau = 2.2RC_L \quad (3.15)$$

$$R = R_{CO} + R_{ANCHOR} + R_{CHANNEL} + R_{DRAIN} \quad (3.16)$$

The resistance value is mainly fixed by the contact resistance ( $R_{CO}$ ) as it has the biggest value. Usually the electrical delay is shorter than the switching time (electrical delay is in the picosecond range while the shortest switching time measured to date its 2.8 ns [56]). The switch keep on in contact until the pull-out voltage is reached in the sweep-down. At this point the beam will be unstuck again, recovering its initial position. The voltage value at the capacitance will be hold if there is no path for the current to discharge it.

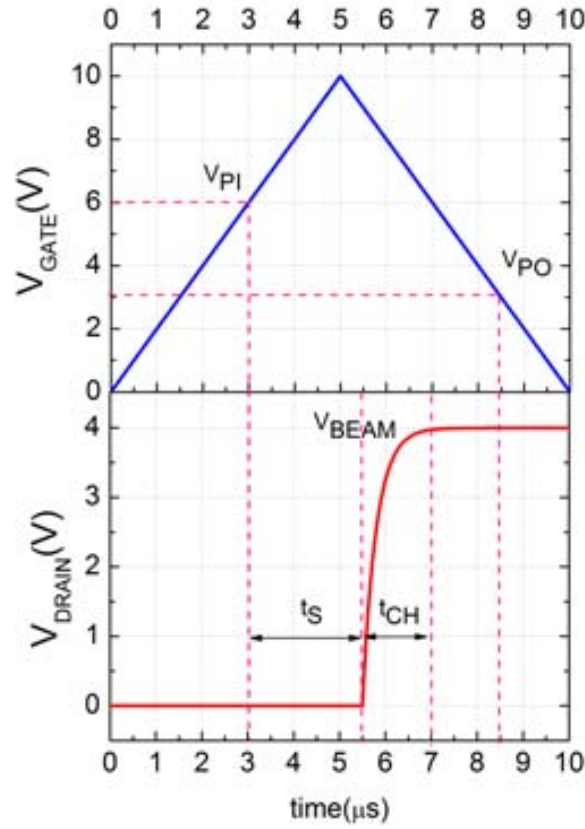


FIGURE 3.9: Mechanical switch voltage time response

### 3.2.2 Contact Resistance

As it was mentioned before, the contact resistance is an important parameter as it fixes the  $I_{ON}/I_{OFF}$  ratio, subthreshold swing and switch time response. It is the core of the switch performance and the main drawback of mechanical switches together with reliability issues, at the moment. In fact, the use of mechanical switches in RF application has been hampered by the difficulty to obtain small contact resistance values ( $< 1\Omega$ ) [36]. On the other hand, switches designed for memory and logic operation can tolerate higher values.

The contact resistance is defined as the constriction resistance between two conductors at contact (with no contamination film presented in the contact area) and it indicates the facility of the current to flow from the structure to the electrode when the contact is made. It depends on:

- contact force

- surface topology
- electrical resistivity
- hardness
- material properties of the surface at contact

Although the electromechanical switches are designed with a fixed contact area, just a fraction of it is in physical contact when the pull-in is produced. Contact is made by local asperities [36] (see figure 3.10). Each of these asperities will have an associated contact resistance and the total contact resistance will be given by the expression:

$$\frac{1}{R_{CO}} = \Sigma \frac{1}{R_i} \quad (3.17)$$

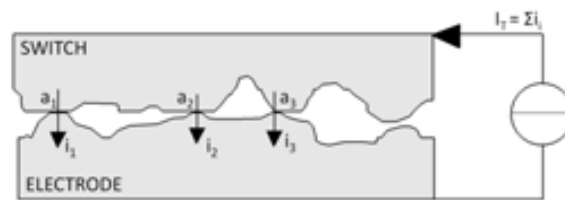


FIGURE 3.10: Cross-section of an electromechanical contact. Reproduced from [36]

As it can be easily seen, it will be difficult to predict the asperities present in a given area (surface topology) and how they will interact with the other surface (material properties of surface at contact, and contact forces). That is why, contact resistance is a parameter difficult to predict. Its calculation details are shown in figure 3.11

### 3.3 Applications

Due to the energy advantages that mechanical switches present, its use has been extended to fields which have been traditionally dominated by CMOS circuits.

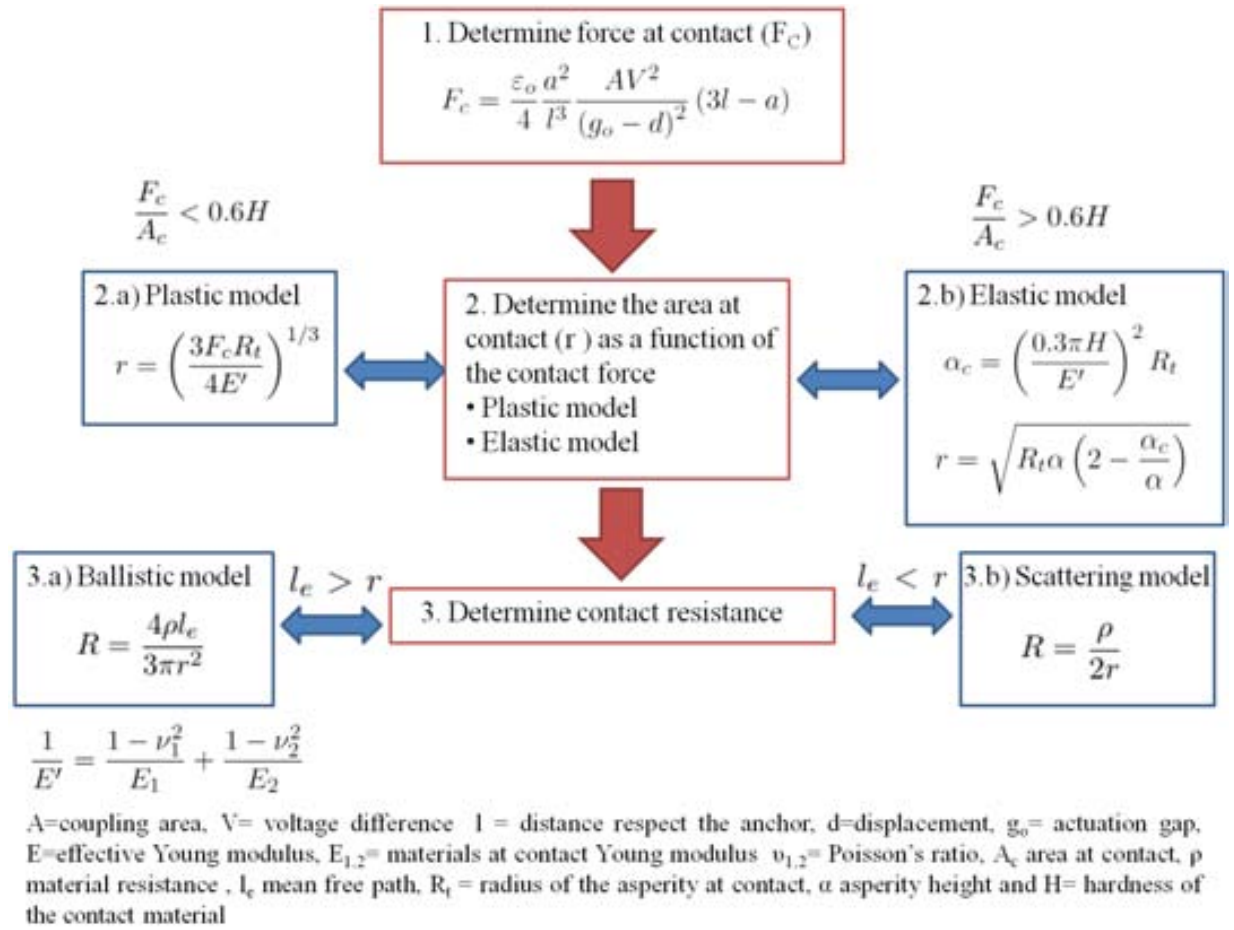


FIGURE 3.11: Contact resistance calculation diagram

### a) Logic applications

Since the electrostatic force is quadratic, the switch can be turned on if a sufficiently large positive or negative voltage is applied between source and gate. This allow the same switch structure to be operated equivalently as an NMOS transistor or a PMOS transistor by appropriately biasing the source terminal (0V for NMOS operation and VDD for PMOS operation) and be able to get the invensor configuration (figure 3.12).

In CNEM gates, the pull-in voltage of the NEM relays is required to satisfy the condition  $|V_{PI}| > V_{DD}/2$  in order to prevent the simultaneous connection of both relays to the output electrode. Using this configuration the basic building block of logic applications (the inverter) is got. In addition, numerous configurations have been proposed that imitate other logic gates

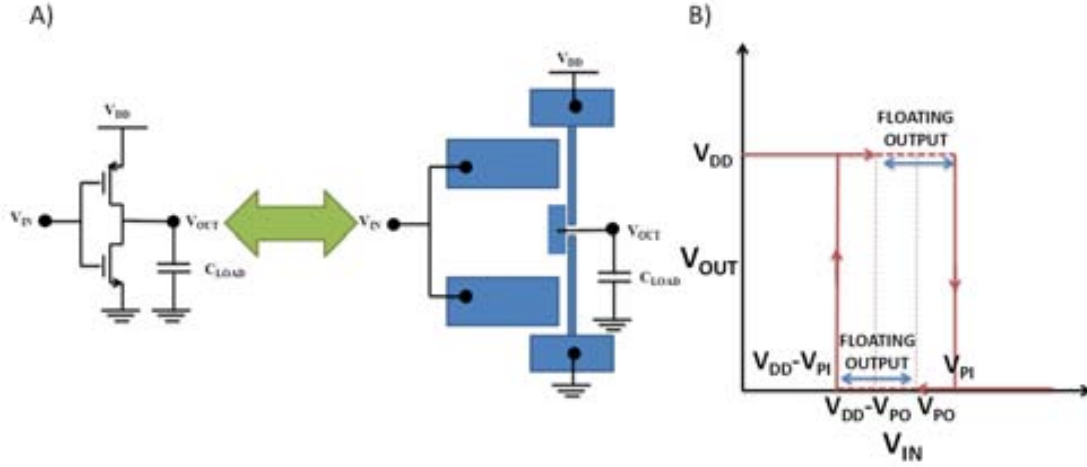


FIGURE 3.12: A) Complementary NEMS (CNEMS) inverter schematic configuration. B) DC transfer characteristic.

as AND, OR or NAND [36][39][57]. The design of FPGA using these new relays has been proposed too [58].

Their main advantages are:

- In optimized designs, the electrical delay due to several stages can be replaced by a single mechanical delay [59] and more energy efficient designs are obtained. Due to the large ratio between the mechanical and electrical delay, an optimized mechanical switch-based IC design would arrange for all mechanical movement to happen simultaneously. Relay based circuits should consist of single-stage complex gates so the delay per operation is essentially one mechanical delay [60]. Additionally, the reduction of energy per operation allows mechanical switches to obtain a good energy-delay trade-off compared with CMOS transistors. In figure 3.13 a comparison between a CMOS inverter chain and a mechanical switches relay chain is established.

It can be observed how in the mechanical chain the  $N$  input signal arrive at the same time, so all the delays switch simultaneously and the total delay of the chain is equal to just one mechanical delay ( $t_{TOTAL} = t_{mech-delay}$ ). The maximum working frequency will be fixed by the mechanical delay ( $f_{max} = 1/t_{switch}$ ). In the MOSFET chain the propagation delay is  $N$  times the electrical delay of a single stage

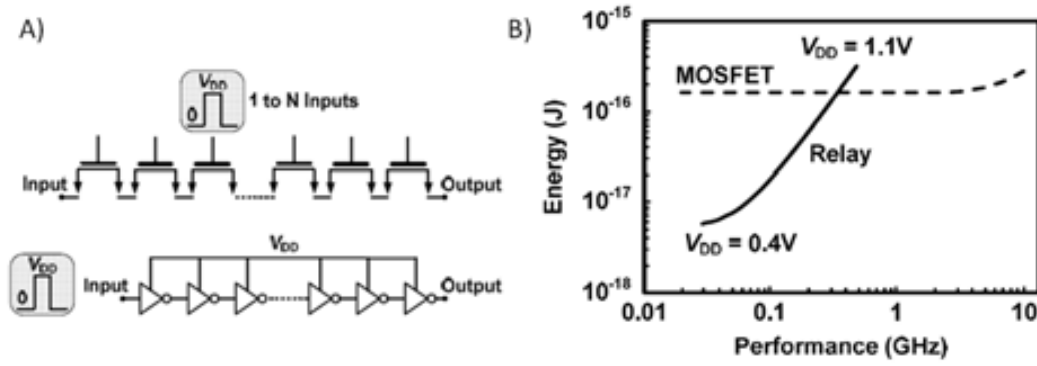


FIGURE 3.13: A) In top image a chain consisting of  $N$  mechanical switches in series is shown. In the image at the bottom a CMOS inverter consisting of  $N$  inverter stages. B) Simulated energy-performance comparison of MOSFET inverter chain versus relay chain circuits. Reproduced from [60].

( $t_{TOTAL} = N \cdot t_{elec-delay}$ ) and its working frequency will be fixed by ( $f=1/(t_d \cdot l_d)$ , where  $l_d$  is the logic depth of the critical path, that in a inverter chain configuration will be equal to number of stages  $f=1/(N \cdot t_d)$ ). In figure B) it is shown a energy-performance comparison between the mechanical switches and CMOS chain and how a N/MEMS switch technology is more energy efficient than CMOS technology for applications working up to 400 MHz, thanks to the null leakage power that they present.

- Although the individual devices are larger, fewer devices are needed to implement the same logic function getting a significant area reduced. (XOR/XNOR gates can be implemented using only two NEMS transistors)[61].

Its main disadvantage is the reliability that electromechanical switches present. A deep study has to be done in order to ensure that the device can stand enough cycles of operation. Another disadvantage is that the mechanical switches can not be so easily integrated with CMOS circuits, except in the case of CMOS-NEMS.

#### b) Memory applications

As we have indicated before, the presence of the hysteresis shows the possibility of using the CNEM inverter as a memory cell. The use of electromechanical switches solves the problem between scaling and cell stability that traditional CMOS cell presents [62], apart from the energy advantages. Furthermore, the write and read delay can be reduced thanks to an intelligent design where one mechanical delay can substitute several electrical delay stages, as was indicated in logic circuits point. Besides, dielectric layers have been added in some switches design to trap charges in order to induce a voltage difference and obtain nonvolatile operation [63].

### 3.4 Benefits of Mechanical switches scaling

As it has been shown, mechanical switches solve the power consumption problem that CMOS devices present when they are scaled. The motivation of this scaling is to get a higher devices density, increase the number of devices per chip and thus decrease cost. These points can be applied to mechanical switches with additional benefits. Extrapolating the concept of scaling the device under constant electric field, scaling all the dimensions of the structure by a factor  $\kappa$  ( $\kappa > 1$ ) table 3.2 has been developed [36], showing how the main parameters of a mechanical switch are affected:

Variables	Scaling Factor
Mechanical switch dimension (l,w,t,s)	$1/\kappa$
Actuation Area A	$1/\kappa^2$
Density	$\kappa^2$
Spring constant k	$1/\kappa$
Effective mass $m_{eff}$	$1/\kappa^3$
Pull-in voltage $V_{PI}$	$1/\kappa$
Switching time	$1/\kappa$
Switching energy	$1/\kappa^3$
Power	$1/\kappa^2$
Power density	1

TABLE 3.2: Constant field scaling of electrostatic relays ( $\kappa > 1$ ). Reproduced from [36]



As it can be observed

- A bigger integration density is obtained and as a consequence, the cost is reduced.
- Switches operating voltage is reduced. Snap-in voltages need to be reduced to make it compatible with CMOS. In order to do it the dimensions of the operating device can be scaled, (as was shown in table 3.2). However reach sub 5 V operating voltages requires small gaps and mechanical switch dimensions (as can be appreciated in the state of the art table 3.3) that are limited by the fabrication process. As an alternative bigger structures are defined with a low spring constant value (see equation 3.11). However, this solution implies a cost in terms of space,
- Faster devices. As it can be observed in equation 3.14 scaling the beam length and width shorter time responses are obtained ( $1/\kappa$ ). As it was mentioned before, one of the main drawback of mechanical switches is that they are slower than CMOS transistor switching time (the faster switch in the state of the art has a 2.8 ns switching time [56] while pico-second time response are got in CMOS transistor). The only way to keep on reducing their time response (for a given material) is an aggressive scaling.
- Lower energy and power consumption. As CMOS devices power consumption is reduced due to the scaling. But what is remarkable is that the energy per operation does not depend on the leakage current so the total energy per operation can be scaled with scaling dimensions,  $1/\kappa^3$  (see equation 3.13).

On the other hand some disadvantages appears due to the scaling:

- Reliability. It can be observed in the state of the art (next section) how the best reliability performance is obtained in big dimensions devices (several tens of microns). As the dimensions are reduced common failure modes increase (damaged caused by electrical discharges, stiction or melting at

contact). Meanwhile damages due to field effect emission are substantially reduced, due to the definition of small gaps and thus low operating voltages, other failure mechanisms as stiction are increased. It can be explained observing equation 3.18 where the elastic restoring force and the elastic constant of an in-plane cantilever is shown [8]:

$$F_{ELAS} = -k\Delta x \quad k = 0.25Et \left(\frac{w}{l}\right)^3 \quad (3.18)$$

It can be observed how scaling all the dimensions by a factor  $\kappa$   $k$  is scaled too (table 3.2) and therefore the elastic restoring force is reduced. As a consequence adhesive forces, that appears at contact, would be hardly overcome and the structure could remain stuck. Adhesive forces can be reduced defining a smaller contact area, but at an expense of a bigger contact resistance in the ON state.

### 3.5 State of the Art N/MEMS switches

Numerous M/NEMS switches devices have been reported in the last decade using top-down and bottom-up approaches [47].

The major contributions to microelectromechanical switches have been summarized in tables 3.3, 3.4, where they have been arranged in decreased order of pull-in voltage. In addition their dimensions,  $I_{ON}/I_{OFF}$  ratio, subthreshold swing and their reliability are shown. In the dimensions row, the coupling area (A) has been defined as the product of the length of the device by its thickness in an in-plane movement and by its width in an out-plane configuration. It will give us some insight into the scaling of the devices. Figure 3.14 represents the miniaturization of the devices together with switches main parameters, in order to show how switch behavior degrades as it is scaled.

Mechanical switches have broken the limits of CMOS devices, presenting a subthreshold swing of 0.1 mV/decade [50] [64], higher  $I_{ON}/I_{OFF}$  ratios ( $10^{11}$ ) [50]

and energy efficiency devices scaling down their operating voltages below 1 V (0.4V)[48]. It can be observed in the state of the art tables how the reliability is still the main drawback of these devices (the best yield correspond to [65], with 21 billion of cycles).

In order to reduce the snap-in values without reducing the gap, big coupling areas have been defined [50] or, as an alternative, novel switches configurations have appeared that try to maximize the coupling area in order to decrease the operating voltages: U-shaped [66], Curved Shape [67], Seesaw [64] or 3D-Torsionals [68][69]. However, their integration capability is seriously reduced.

In figure 3.14 the main parameters of the state of the art switches are represented as a function of its coupling area. As it can be observed in the top figure the lowest operating voltage and miniaturization has been reached by kaul06 ([56]) whose device is based on a small dimensions CNT ( $l=130\text{nm}$ ,  $d=3\text{nm}$ ). However its reliability need to be improved. Respect the  $I_{ON}/I_{OFF}$  ratio (figure in the middle) there is not a device with small dimensions that beats the limit imposed by professor Liu devices (Nathanael09 [50] and jeon10 [64]). However these devices present a large coupling area. Finally, in the figure at the bottom, it can be observed how as the dimensions are reduced the reliability is lower. This can be observed in figure 3.14 which clearly shows two different groups well defined: devices with a coupling area smaller than  $1\text{ }\mu\text{m}^2$  that work less than 100 cycles and other group form by 5 devices which present a better reliability (all operates more than  $10^7$ ) and have a bigger coupling area. Besides the coupling area, some of these devices have a decoupling of the electrical and mechanical domain (attaching a conductive layer to the mechanical structure [50][64]) or their contact resistance has been improved depositing an additional layer (platinum[70]) (the other two approaches are based on SiC that has been regarded as the most viable technology for high-temperature applications [65] [71]). As a consequence of this good contact resistance these works present a good  $I_{ON}/I_{OFF}$  ratio.




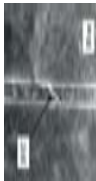
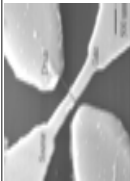


Material	Device	Structure Description	Dimensions	Pull-in Voltage (V)	$I_{ON}/I_{OFF}$	mV/decade	Reliability (cycles)	Comments
TiW/W [48] [lee13]		Pipe clip C.C.Beam 2-Terminal	$l=1.4\mu m$ $w=300nm$ $s=4nm$ $A=0.42\mu m^2$	0.4	$10^6$	10	20	Top-down. Lowest snap-in voltage
Silicon carbide nanowires [49] [feng10]		2-Terminal	$l=8\mu m$ $t=25nm$ $s=27nm$ $A=0.2\mu m^2$	1.5	$10^2$		Several tens	Top-down.
Poly-silicon-SiGe, Tungsten and ultra thin $TiO_2$ coating [50] [nathanael09]		4-Terminal	$l=30\mu m$ $w=30\mu m$ $s=100nm$ $A=900\mu m^2$	2	$10^{11}$	0.1	$10^9$	Top-Down. 100ns switching time. Highest $I_{ON}/I_{OFF}$ ratio.
Carbon nanotubes [56] [kaul06]		2-Terminal	$l=130nm$ $d=3nm$ $s=20nm$ $A=3.9 \times 10^{-4}\mu m^2$	3.5	$10^4$		10	Bottom-up. Niobium electrode. Fastest switch (2.8ns switching time)
Carbon Nanotube [72] [cha05]		3-Terminal	$l=800nm$ $d=40nm$ , $s=40-60nm$ $A=0.032\mu m^2$	3.5	$10^4$		1	Bottom-up.
Carbon nanotubes [73] [jang08]		3-Terminal	$l=2\mu m$ $d=50nm$ $s=30nm$ $A=0.1\mu m^2$	4.15	$10^5$		1	Bottom-up. Snap-in by repulsive forces
Platinum [74] [chong11]		3-Terminal	$l=3.5\mu m$ $t=60nm$ $s=100nm$ $A=0.21\mu m^2$	4.3	$10^4$	0.8		Top-down. NEMS on CMOS

TABLE 3.3: MEMS switches state of art 1


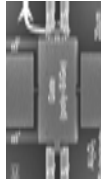






Material	Device	Structure Description	Dimensions	Pull-in Voltage	$I_{ON}/I_{OFF}$	mV/decade	Reliability (cycles)	Comments
Silicon Carbide [65] [lee10]		3-Terminal	$l=8\mu\text{m}$ $t=400\text{nm}$ $s=150\text{nm}$ $A=3.2\mu\text{m}^2$	6			21 billion	Best Reliability. Computing at 500°
poly-SiGe [64] [jeon10]		3-Terminal Torsional	$l=12\mu\text{m}$ $w=42\mu\text{m}$ $s=100\text{nm}$ $A=504\mu\text{m}^2$	7.14	$10^{10}$	0.1	$10^9$	Top-down.
AlSi [75] [abele05]		2-Terminal Resonant Gate Transistor approach	$l=80\mu\text{m}$ $w=4\mu\text{m}$ $s=220\text{nm}$ $A=320\mu\text{m}^2$	9	100	2		Top-Down. Gate of a transistor acting as a switch
Si/PtSi [67] [grogg13]		Curved shape device 3-Terminal	$l=29.5\mu\text{m}$ $t=800\text{nm}$ $s=50\text{nm}$ $A=23.6\mu\text{m}^2$	9	$10^6$			Top-down. Avoids non-uniform electric field
Polysilicon-Platinum [70] [Parsa13]		5-Terminal	$l=16\mu\text{m}$ $t=1.2\mu\text{m}$ , $s=500\text{--}400\text{nm}$ , $A=19.2\mu\text{m}^2$	10	$10^5$		$10^8$	Top-down. Improve poly contact resistance with platinum ( $R_{CO} = 3k\Omega$ )
TiN [76] [jang08TiN]		2-Terminal	$l=300\text{nm}$ $w=200\text{nm}$ $s=15\text{nm}$ $A=0.06\mu\text{m}^2$	14	$10^5$	3	hundreds	Top-down. CMOS compatible
Germanium nanowires [77] [andzane09]		2-Terminal	$l=3\mu\text{m}$ $d=30\text{nm}$ $s=500\text{nm}$ $A=0.09\mu\text{m}^2$	19	100		tens	Bottom-up
Silicon Carbide [71] [he13]		3-Terminal	$l=8\mu\text{m}$ $t=200\text{nm}$ $s=200\text{nm}$ $A=1.6\mu\text{m}^2$	22.5V	$10^4$		$10^7$	Top-down

TABLE 3.4: MEMS switches state of art 2

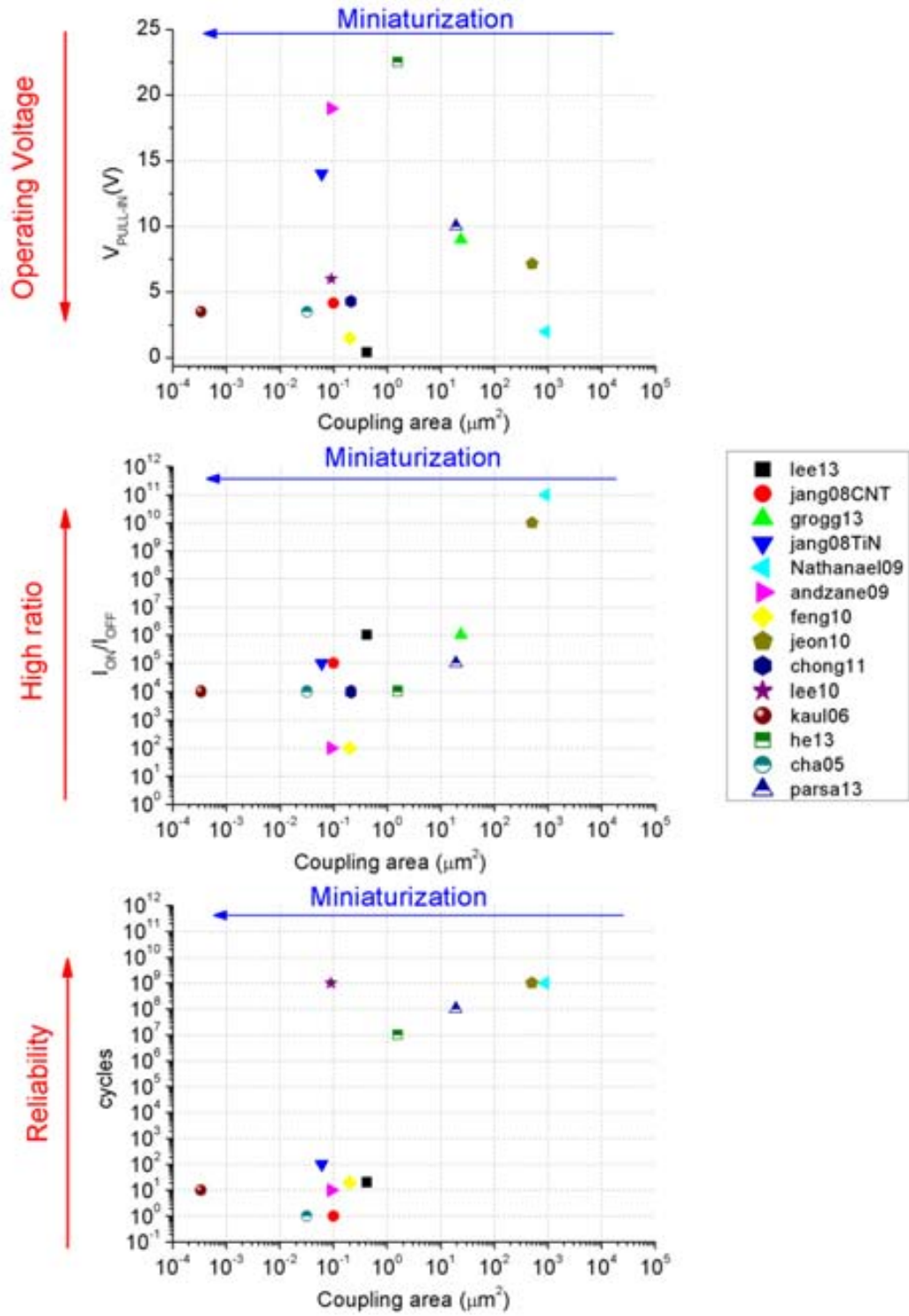


FIGURE 3.14: Mechanical switches State of the Art

## 3.6 Ring Oscillator

As it was shown in the applications section the parallelism that exists between electromechanical switches and CMOS devices has extended its use to fields which are traditionally dominated by the CMOS technology, such as logic circuits [36] or memory cells [63]. With logic circuits in mind, one may wonder whether a purely MEMS-based synchronous logic can be achieved, i.e. can a digital clock signal be generated using only MEMS switches? And can this clock signal be used to drive other MEMS-based logic components? The aim of this section is to show how such a classical concept as the CMOS ring oscillator (a loop consisting of an odd number of inverters in series, see figure 3.15 ) may be extended into the MEMS domain and in which respect we may answer positively to the first of these two questions. In order to simulated the response of a ring oscillator configuration composed by mechanical switches the next mechanical and electrical model is proposed:

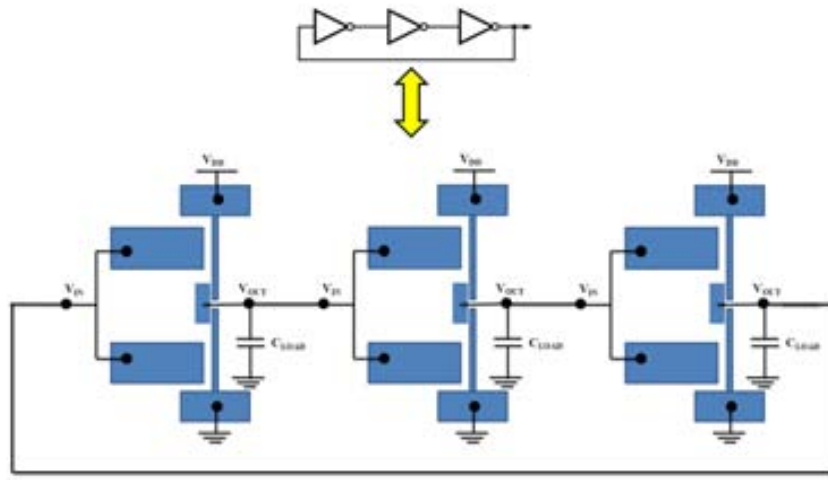


FIGURE 3.15: Ring oscillator schematic.

### 3.6.1 Switch electrical model

Figure 3.16 A) represents the studied out of plane cantilever switch configuration. When a sufficient voltage is applied across gate and source, the flexible part of the source bends as a result of electrostatic forces until its tip touches the drain

and an electrical contact is established. The simplest MEMS inverter consists of two switches, PMEMS and NMEMS, respectively with source voltages  $V_{dd}$  and  $V_{ss}$ , having a common drain and a common gate (Figure 3.16 B)). With correct design, the drain (output) voltage is when the gate (input) voltage is and vice-versa. Putting an odd number of such inverters in series and closing the loop results in an intrinsically unstable system, known as a ring oscillator, a simplified model of which is established in the next sub-sections.

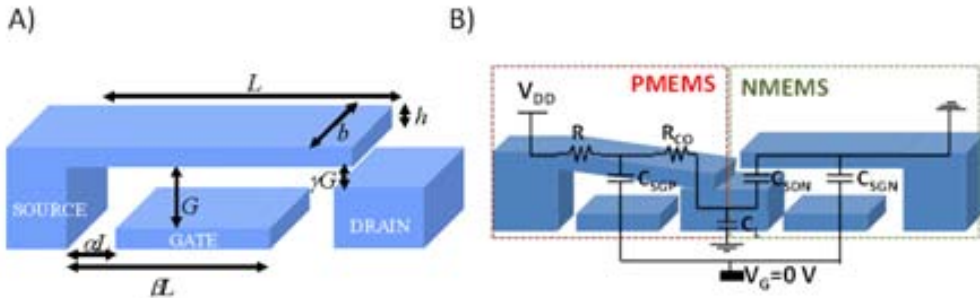


FIGURE 3.16: A) Schematic of a MEMS cantilever switch and notations. B) Figure 2. MEMS inverter and its electrical model when  $V_G=0V$ .

In a ring oscillator, the switches are either in the free mode, such as NMEMS in Fig 3.16 B) which is moving toward or away from the drain, or in the contact mode, such as PMEMS in Fig.3.16 B). In the contact mode, a resistive path between source and drain is established. As long as mechanical contact is maintained, is governed by:

$$R_{ON}C_{ON}\frac{dV_D}{dt} + V_D = V_S \quad (3.19)$$

where  $R_{ON}$  is the resistance of the path between source and drain and  $C_{ON}$  is the total capacitance when contact is established.  $R_{ON}$  can be assimilated to the contact resistance ( $R_{CO}$  in figure 3.16 B) between source and drain, which is typically several orders of magnitude greater than the intrinsic resistance of the drain or of the source ( $R$  in figure 3.16 B). If  $\tau_{ON} = R_{ON}C_{ON}$  is small compared to the mechanical contact duration  $V_D$  goes to  $V_S$ . It will be assumed a contact resistance in the range  $1-10k\Omega$  and a gate to source capacitance in the  $0.1-10$  fF range [62]. In the free mode, provided the change in  $C_{SGP}$  or  $C_{SGN}$  is not



too large compared to  $C_L$ , the gate/drain voltages can be considered as constant. Note that the behaviour of our oscillator is considerably different from that of the one proposed in [78], where the mechanical and electrical time constants have the same order of magnitude. It is assumed throughout the rest of the section that  $V_{ss} = 0$

### 3.6.2 Mechanical model

The beams in the ring oscillator can be modelled with the Euler-Bernoulli equation (expression 2.1), in which we have account squeezed-film damping (second term) as the dominant damping phenomenon (it governs the gas flow between two surfaces moving towards each other), electrostatic actuation and the contact applied at the beam tip ( $F_c$ ) when it is brought into contact with the readout electrode:

$$E \frac{bh^3}{12L^4} \frac{\partial^4 w}{\partial x^4} + \mu_{eff} \frac{b^3}{G^3} \frac{\chi(\alpha, \beta)}{(1-w)^3} \frac{\partial w}{\partial t} + \rho b h \frac{\partial^2 w}{\partial t^2} = \varepsilon_o \frac{b}{2G^3} V^2 \frac{\chi(\alpha, \beta)}{(1-w)^2} + F_c(w) \delta(1) \quad (3.20)$$

where  $\chi \in [0,1]$  is the normalized coordinate along the length of the beam ( $x=1$  corresponding to the tip), displacement  $w(x, t)$  is normalized with respect to the gap  $G$ ,  $V$  is the voltage applied to the beam and  $\chi(\alpha, \beta)$  is the characteristic function of the actuation electrode (equal to 1 if  $x \in [\alpha, \beta]$  and 0 otherwise).  $E$  and  $\rho$  are the Young modulus and mass density of the structural material,  $\mu_{eff}$  the effective viscosity of the surrounding medium and  $\varepsilon_o$  the permittivity of vacuum. The solution of 3.20 can be approximated as:

$$w(x, t) = a_1(t)W_1(x) + a_2(t)W_2(x) \quad (3.21)$$

where

$$W_1 = \frac{1}{2}(U_1 + U_2) \quad W_2 = \frac{1}{2}(U_1 - U_2) \quad (3.22)$$

and  $U_1(x)$  and  $U_2(x)$  are the first two eigenmodes of the cantilever, with eigenvalues  $\lambda_1^4$  and  $\lambda_2^4$ , normalized so that  $U_1(1) = U_2(1) = 1$ . Consequently,  $W_1(1) = 1$  and  $W_2(1) = 0$ . Mechanical contact between source and drain then takes place when  $a_1 \geq \gamma$ , regardless of  $a_2$ . We use the Galerkin method to derive the following nonlinear mechanical model of the beam:

$$\mathbf{K}\mathbf{a} + \mathbf{B}(\mathbf{a})\dot{\mathbf{a}} + \ddot{\mathbf{a}} = \mathbf{f}_e(\mathbf{a})V^2 + \mathbf{f}_c(\mathbf{a}) \quad (3.23)$$

where  $\mathbf{a}^T = [a_1, a_2]$  and

$$\mathbf{K} = \frac{Eh^2}{192\rho L^4} \begin{bmatrix} (\lambda_1^4 + \lambda_2^4) & (\lambda_1^4 - \lambda_2^4) \\ (\lambda_1^4 - \lambda_2^4) & (\lambda_1^4 + \lambda_2^4) \end{bmatrix} \quad (3.24)$$

$$\mathbf{B} = (B_{ij})_{\substack{1 \leq i \leq 2 \\ 1 \leq j \leq 2}} \quad B_{ij}(\mathbf{a}) = \frac{\mu_{eff}b^2}{\rho h G^3} \int_{\alpha}^{\beta} \frac{W_i W_j}{(1-w)^3} dx \quad (3.25)$$

$$\mathbf{f}_e = (f_i)_{1 \leq i \leq 2} \quad B_{ij}(\mathbf{a}) = \frac{\varepsilon_o}{2\rho h G^3} \int_{\alpha}^{\beta} \frac{W_i}{(1-w)^2} dx \quad (3.26)$$

$$f_c = \begin{cases} \begin{bmatrix} K_c(a_1 - \gamma) + B_c \dot{a}_1 \\ 0 \end{bmatrix} & \text{if } a_1 \geq \gamma \\ 0 & \text{Otherwise} \end{cases} \quad (3.27)$$

Note that the contact force 3.27 is not necessarily conservative. Using 3.21 , 3.23 3.24, 3.25 , 3.26, 3.27, a MEMS-based ring oscillator with an arbitrary number of stages can be simulated and several of its characteristics can be explored (influence of contact stiffness and damping, influence of supply voltage on the existence of periodic solutions, etc.). However, the model developed in this section, in spite of its apparent simplicity, is difficult to simulate because of (i) the existence of discontinuities, and of (ii) the coexistence of several phenomena with very different

time scales (ideally, the transition from a high to a low state should be very short compared to the mechanical contact duration, and even shorter compared to the period of oscillation). In the annex A, we propose a semi-analytical tool based on simplifying assumptions which will allow us to predict the existence of periodic regimes without resorting to computationally-intensive simulation tools.

### 3.6.3 Simulation results

We have represented in 3.17 the starting transient of  $a_1(t)$ , obtained by simulating 3.19 and 3.23 with Matlab/Simulink. The device is a 1-stage MEMS ring oscillator consisting of two identical beams arranged as in Figure 3.16 B), with shorted gate and drain, with the following geometry:  $\alpha = 0.1$ ,  $\beta = 0.9$ ,  $\gamma = 0.15$ ,  $L=25 \mu\text{m}$ ,  $b=1 \mu\text{m}$ ,  $h=0.25 \mu\text{m}$  and  $G=0.3 \mu\text{m}$  ( $1/f_o = 1.88 \mu\text{s}$ ,  $Q_{squeezed}=15.2$ ,  $V_{snap}=2.07 \text{ V}$ ). The material is assumed to be polysilicon and the surrounding medium air at ambient pressure. The actuation voltage is  $V_{dd}=1.4 \text{ V}$  and we set  $R_{on}=10 \text{ k}\Omega$  and  $C_{on}=10 \text{ fF}$ . In these conditions, the oscillator reaches a periodic regime after a short time, with a period of  $T=1.15 \mu\text{s}$ . We also show in 3.18 the steady-state behavior of  $a_1(t)$  as predicted by the method presented in annex A. There is an excellent match between the simulated response and the predicted one.

In figure 3.18, we compare the results obtained by slowly sweeping the actuation voltage in the transient nonlinear model to the "T versus  $V_{on}$ " curve obtained with our semi-analytical method - for the transient simulations, T is the fact the "apparent" period, i.e. the time between two successive rising edges of  $V(t)$ . As expected [79] [78] depending on the value of  $V_{on}$ , the simulated behavior is not always periodic, even though our semi-analytical method predicts one or more possible periodic limit cycles. For example, transient simulation shows that the system exhibits chaotic behaviour when  $V_{on}$  is between 1.5 V and 1.75 V, whereas our semi-analytical method predicts the existence of one or two periodic solutions. This illustrates the fact that the stability of the predicted limit cycles is not guaranteed a priori and should be the object of careful study. This situation is even more pronounced for structures with small damping factors (larger Q).

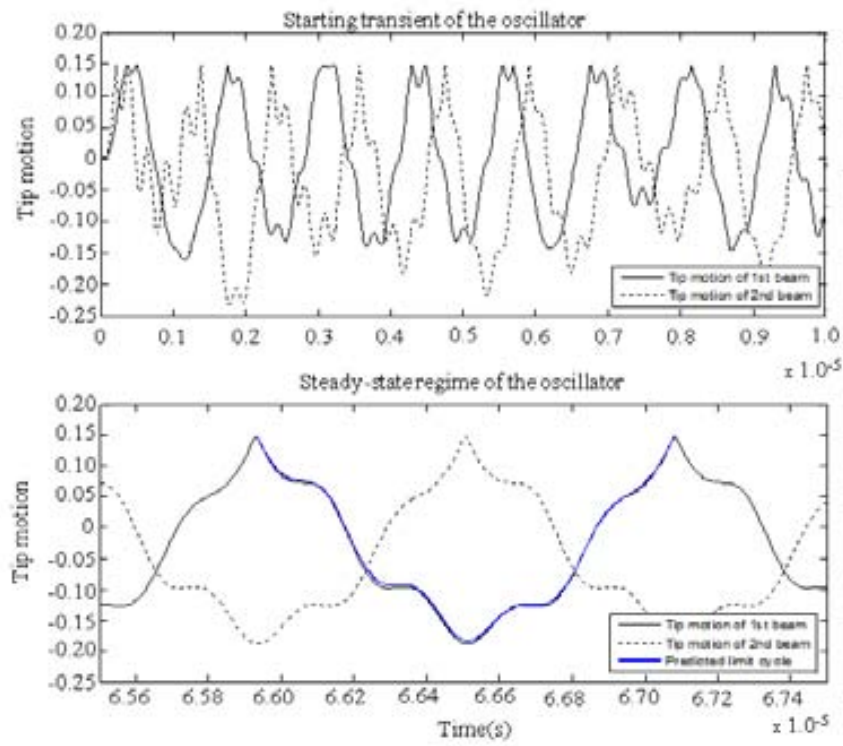


FIGURE 3.17: Simulated transient response of  $a_1(t)$  (normalized beam tip position) for the two beams composing the switch (top) and simulated and predicted steady-state response (bottom).

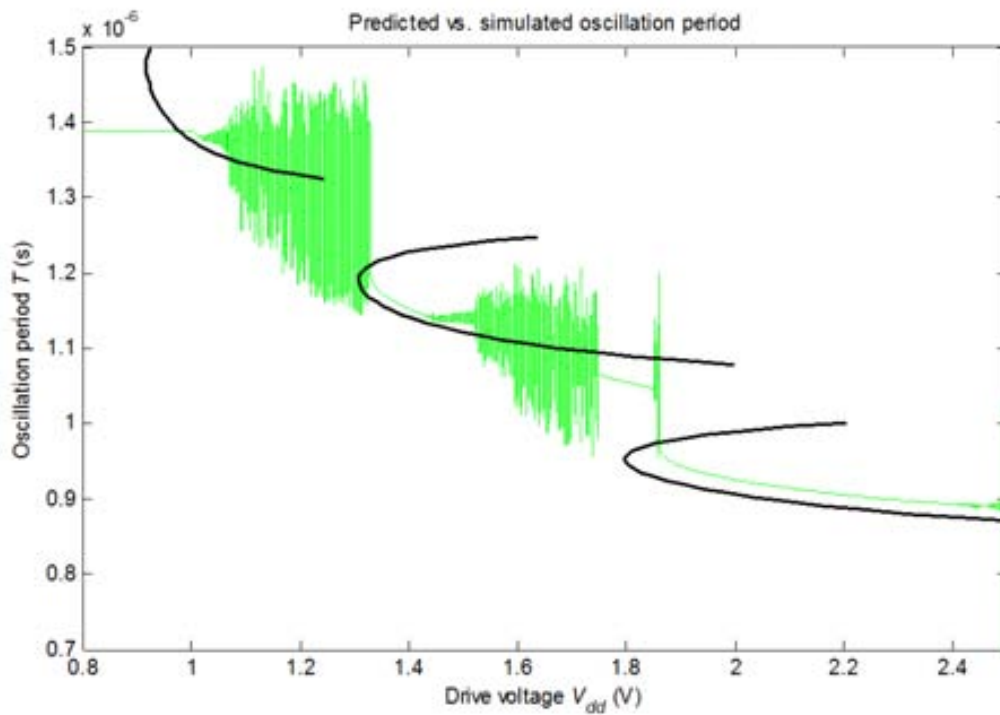


FIGURE 3.18: Figure 4. Comparison of predicted "T versus  $V_{on}$ " curve (black line) and results obtained by transient simulation (green line), starting from  $V_{dd} = 2.5$  V.

From these simulations, we have shown that under certain conditions, one may contrive to generate a periodic square signal using an odd number of MEMS inverters in a ring oscillator configuration. The governing equations of such a system were established and a semi-analytical method for predicting the existence of simple limit cycles was proposed. Comparison of the results obtained by our method and by simulation incite us to develop tools to study the stability of these limit cycles, for example following [80]. Qualitatively, we have found that too large a quality factor is detrimental to the stability of the system. Also, a possible reason for non-periodic behaviour is that the two natural resonance frequencies of the system (those of the first two eigenmodes of the beam) are not harmonically related. The beam profile could then be carefully designed, for example to tune the beam for periodic behaviour in a given voltage range. Several questions remain open, e.g. heating, friction and wear, etc. which are the subject of ongoing work.



## Chapter 4

# CMOS-MEMS based on ST 65nm technology

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*The reduction of MEMS devices to the nano scale (NEMS) devices promises to revolutionize measurements of extremely small displacements and extremely weak forces. In order to obtain smaller structures using a CMOS approach, ST 65nm commercial CMOS technology will be used to define NEMS structures and a post-CMOS releasing process will be developed in order to release the NEMS devices. This chapter contents include: the state of the art of CMOS-MEMS devices, ST 65 nm technology description, post-CMOS NEMS releasing process and physical characterization of the fabricated devices. Additionally the electrical characterization of the resonator developed using the different available layers are presented.*

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## 4.1 Micro and nanosystems technology

The fabrication of MEMS devices can be divided in two well distinguished approaches: top-down and bottom-up [22].

**Bottom-up** techniques: build or grow structures atom by atom or molecule by molecule [81] [82]. These techniques include chemical synthesis, self-assembly and positional assembly. A commonly use approach is based on using growing crystals methods to make the resonant structures as it is done with carbon nanotubes or Silicon nanowires (Figure 4.1)

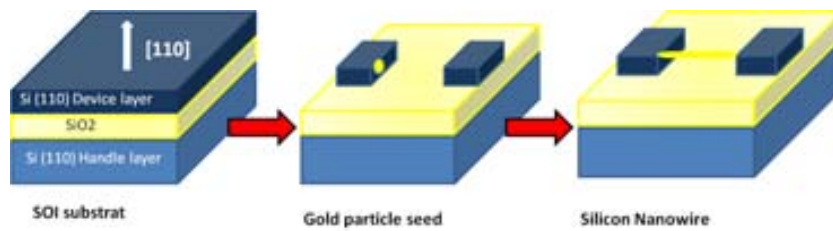


FIGURE 4.1: Silicon Nanowires fabrication process.

**Top-Down** approach: the resonant structure is made removing material from a homogeneous layer (as a sculpture is carved [83]). In order to do it, the fabrication processes developed by the IC industry are used, as batch processing, lithography or layers deposition. In this way, MEMS fabrication benefit of the robustness of microfabrication standard processes and thousand of devices can be processed simultaneously, reducing the production cost. Top-down approach can be subdivided in two different subcategories: Bulk micromachining and surface micromachining (see figure 4.2). Surface micromachining is based on patterning thin films on top of a substrate wafer. In figure 4.2 A) a typical surface micromachining process is shown. It starts with a substrate where a sacrificial layer has been deposited (A.1). Then a hole is made by lithography and etching (A.2) and a new layer, that will act as structural, is deposited (A.3). Finally the sacrificial layer is etched remaining the released structure. On the other side bulk micromachining defines free structures by selectively etching the substrate [8]. Figure 4.2 B) shows a bulk micromachining process. It starts with a Silicon on Insulator (SOI) wafer (B.1). Then a etch process define the movable structure (B.2) and finish with a



the definition of trenches, by a deep reaction ion etching (DRIE) in the back of the wafer (B.3).

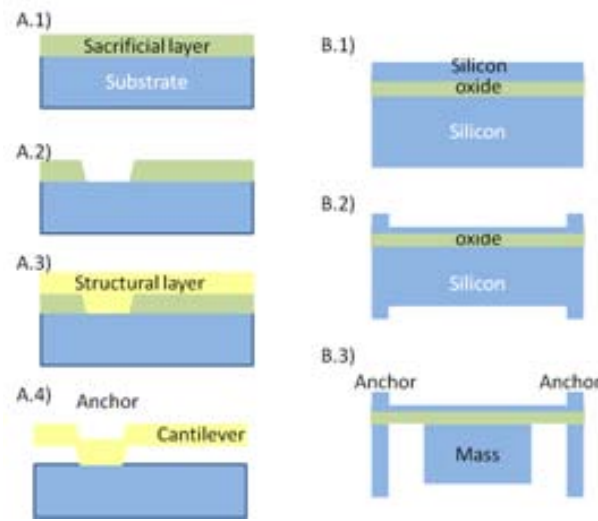


FIGURE 4.2: Top-Down fabrication approaches: A) Surface micromachining and B) Bulk micromachining.

So it can be easily appreciated how IC industry and top-down MEMS share the main fabrication processes. Additionally, if new market demands are taken into account, like integrate all the components of a system (RF components or sensors) in a single chip system on chip (SoC) solution, the integration of circuitry and MEMS devices in the same chip seems straight forward. The advantages of this approach are a reduction of cost due to batch fabrication capability, size reduction, faster time responses due to the reduction of parasitic capacitances as no external interconnections are needed and a reliability and robustness improvement. As CMOS has become the predominant technology for integrated circuits, we will focus on the integration of MEMS with CMOS.

#### 4.1.1 CMOS-MEMS

There are three different approaches to integrate MEMS devices with CMOS technology and its classification depend on the moment when they are integrated in the CMOS sequence [84]. In that way, CMOS-MEMS are divided in: pre-CMOS, intra-CMOS or post-CMOS.

- **Pre-CMOS.** MEMS device are defined before the CMOS sequence starts. Typically, in a first step the MEMS are defined and then are buried to protect them for the next fabrication steps. Then the wafer with the buried structures are planarized and it is used as starting material for the subsequent CMOS process. Once the CMOS circuitry has been defined in areas adjacent to the MEMS areas, the mechanical structures need to be released (wet or dry etching) in a post-CMOS process. Examples of this approach are: the *M<sup>3</sup>EMS* (Modular, Monolithic MicroElectroMechanical Systems) technology developed at Sandia National Laboratories [85] and Mod MEMS Technology developed by Analog Devices [86].
- **Intra-CMOS.** In this approach the micromachining process to define the MEMS structure are inserted between the front-end and the back-end interconnect metallizations. One way to fabricate the MEMS structures using this approach consist on buried in oxide the mobile structure after the front end process and released after finishing the back-end fabrication processes. Commonly, polysilicon structures are implemented using this fabrication process. Examples of this fabrication process are the polysilicon gyroscopes [87] and accelerometers [88] developed by Analog devices or Infineon pressure sensor [89]. The other fabrication process consist on using the front-end and back-end layers as structural material [90] [91] [28] [92] to develop the micromechanical structures. Its main advantage is that commercial CMOS technologies can be used to define the structures getting benefit of the robustness and reproducibility that standard CMOS fabrication process offers. Moreover, thanks to the continuous scaling of the CMOS nodes, smaller structures could be designed without any additional effort. On the other side, the material to build the mechanical structures are limited to the CMOS layers, in addition to a stringent thermal budget, as high temperature could modified the transistor behavior. We will focus on this fabrication process later.
- **Post-CMOS.** After completion of the regular CMOS process sequence, which can, in principle, be performed at any CMOS foundry, the post-CMOS

micromachining steps can be done at a dedicated MEMS foundry. In order to do it, two different fabrication processes are distinguished. The first one consists on define the structure on top of a finished CMOS substrate, micromachining of add-on layers. Examples of this fabrication process are a nickel gyroscope developed by General Motors [93] or Texas Instrument Digital Micromirror [94]. In the other approach, microstructures are released by micromachining the CMOS substrate wafer itself after the completion of the regular CMOS process sequence. By far the majority of demonstrated devices rely on bulk micromachining processes, such as wet and dry anisotropic and isotropic silicon etching. Using this fabrication method different companies as Motorola or Bosch have developed pressure sensors [84].

In this thesis a intra-CMOS approach will be used as the MEMS devices are defined using the polysilicon layer or the metal layers of the BEOL. No modification of the CMOS sequence is required. Just an in house post-CMOS releasing process is used to release the resonators. The MEMS devices are defined in commercial CMOS technologies using the conductive layers as structural layers and silicon oxide as sacrificial layer. A post-CMOS wet etching based on a buffered HF bath, without any additional mask, is used to remove the silicon oxide that surrounds the mobile structure, releasing it. This technological approach has been proven in 2 different CMOS technologies: AMS 0.35um [91] and UMC 0.180um [28].

In the design process the first step is to fix the resonator dimensions. To do that, some theoretical study based on the analytical expression and FEM (Finite Element Method) simulations are needed to obtain the target MEMS resonator.

Once the design is done the resonators are drawn in a standard IC CAD environment (Cadence) and sent to a foundry. In this workflow, no modification of the CMOS process is required, even though some violations of the design rules will be needed. The CMOS fabrication is completely transparent to the designer as it is entirely developed on the standard CMOS process of the selected foundry. Moreover, the total amount of masks required in this MEMS fabrication is the same of the CMOS process selected.

To allow the etchant to reach the resonators, the passivation layer deposition above the resonator is prevented by using the PAD window layer available in the technology, whereas the remaining area of the chip is protected by this passivation layer, as it is shown in Figure 4.3. The use of this PAD window is one of the main responsible of the simplicity of the overall process. If the definition of this PAD window is not possible, an additional step will be needed (for example a RIE could be use to cut this passivation layer and allows the etchant to reach the structure [95]). Moreover, to make easier the structures release, the minimum amount of oxide above the resonator is wanted. In order to get this point, in the design process, we define the contact VIAS between metals above the resonator without any metal above, obtaining in this way 'empty VIAS'. This point is particularly contentious and permission from the foundry is required as multiple design rules are violated.

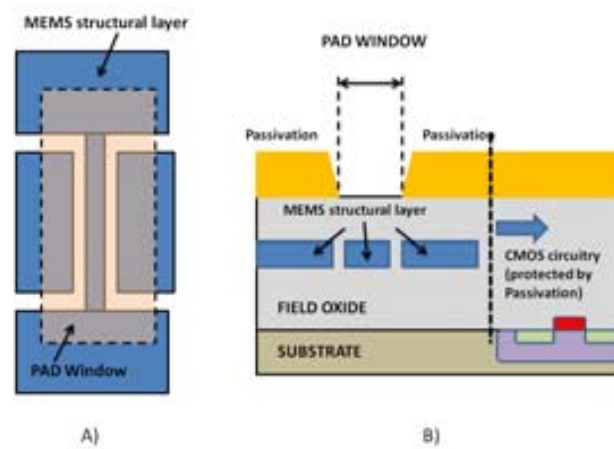


FIGURE 4.3: A) Schematic layout of the MEMS resonator, structural layer and pad window is shown. B) Schematic cross-section of the chip. Passivation layer protect the CMOS circuitry whereas the PAD window allows the etching of field oxide.

#### 4.1.2 CMOS–MEMS State of the Art

As one of the aims of this thesis is developed the smallest CMOS-NEMS device following a intra-CMOS approach), the state of the art of CMOS–MEMS resonators is showed in table 4.1 and 4.2. It is focused in all the devices that have been developed using the available layers of different standard CMOS technologies.

Pre-CMOS approaches [85] [86] [96] and post-CMOS [94] [97] [98] fabrication process that define the MEMS resonator without using the back end of line (BEOL) or the front end of line (FEOL) layers are excluded of the table as the minimum dimensions in these approaches do not depend on the technology design rules.

In the state of the art tables, the devices are arranged in decreased order of cross section (thickness by width  $A = w \cdot t$ ), in order to compare the miniaturization of the devices. The lowest coupling value correspond to devices developed in IBM 32nm SOI Tech [99] [100]. However it is an unreleased device, operating in the GHz range and not valid as a sensor device.

As it can be observed four different materials and stacks configurations are mainly used in order to develop the mechanical structures: polysilicon, aluminum, stacks composed of aluminum, silicon oxide, tungsten and finally silicon.

Polysilicon is the layer that presents the smaller thickness of the available layers of a CMOS technology (for example in AMS 0.35  $\mu\text{m}$  polysilicon thickness is 282 nm [28]), and as a consequence it allows the definition of the smaller structures. However due to its small value a capacitive read-out is difficult to perform (in in-plane resonators), as its coupling area is low and hence the capacitive output current can be easily masked. This problem is solved reducing the gap. The smallest gap obtained using a intra CMOS-MEMS is 40 nm (ECAS) thanks to the spacer technique [28].

Back end metal lines allows the definition of structures with small thickness too (in UMC 0.18  $\mu\text{m}$  the top metal presents a thickness of 580 nm [28]). In 0.18  $\mu\text{m}$  and bigger technology nodes, metal lines are mainly based on aluminum, in smaller CMOS technology nodes it is substituted by copper that presents a lower resistivity. As its thickness is bigger then polysilicon, capacitive detection can be performed with bigger gaps, but at an expense of bigger operating voltages (21 V for the polysilicon devices while 80 V are used in the aluminum structure).

So it can be observed how the definition of a small gap has a deep impact on the miniaturization of the devices. A small gap ensures a successful capacitive

transduction. The bigger miniaturization in intra CMOS–MEMS released devices has been reached in the designs with the smaller gaps (aluminum ECAS [28], poly ECAS [101]). As the technology imposes a limit in the minimum gap that can be defined, some efforts have been made in order to reduce its value dynamically making the mobile structure collapses with a stopper (in [102] a gap of 970 nm without pull-in is reduced to 270 nm with pull-in). However high operating voltages are reached using this approach.

Another way to ensure capacitive readout without reducing the gap between the structure and driver is to define a big coupling area. With this aim, stack of Al-SiO<sub>2</sub> and Al-SiO<sub>2</sub>-W are used. However this solution forbids the structures miniaturization. Note that the use of oxide as structural material can improve the temperature coefficient of frequency compared with mere-metal CMOS-MEMS counterparts [103].

Finally, silicon has been used as structure material too [104]. Its main advantage is that it is a monocrystalline material so it can present high quality factor. However its fabrication process is not reproducible.


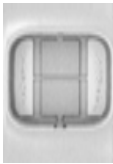



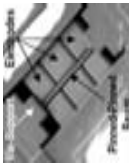
Inst.	Material	CMOS Tech.	Configurations	Device	Ref. Year	Minimum Dimensions Cross section (A=w·t) length (l), width (w), thickness (t), gap (s)	Features (fo and Q)	MEMS Bias Voltage
MIT	Silicon	IBM 32nm SOI Tech [99] [100]	unreleased resonator		[100] 2013	w=360 nm, t<100 nm l=2.5 $\mu\text{m}$	11.1 GHz 30	<1 V
UAB	Polysilicon	CMOS 2.5 $\mu\text{m}$ [105] AMS 0.35 $\mu\text{m}$ [106] [101] [107] [108]	resonators (bulk, DETF, c.c. beams) and filters		[108] 2009	A=0.098 $\mu\text{m}^2$ l=13 $\mu\text{m}$ , w=350 nm t=282 nm, s= 40 nm	22 MHz 4400 (Vac)	5 V
UAB	Aluminum	AMS 0.35 $\mu\text{m}$ [109] [91] [20] UMC 0.18 $\mu\text{m}$ [28]	resonators (c.c. beam and cantilevers)([91] [20] mass sensor)		[28] 2009	A=0.162 $\mu\text{m}^2$ l=2.7 $\mu\text{m}$ , w=280 nm t=580 nm, s=280 nm	228 MHz 145	80V
Cornell	Polysilicon	ON Semiconductors 1.5 $\mu\text{m}$ [95]	Dome and arch bridges resonators (piezoresistive)		[95] 2010	A=0.30 $\mu\text{m}^2$ l=10.5 $\mu\text{m}$ , w=1.5 $\mu\text{m}$ t=200 nm, s=50 nm	36.85 MHz 800 (Vac)	1.5 V
NTHU	Aluminum	TSMC 0.35 $\mu\text{m}$ [110]	Resonators (F.F. Beam Res)		[110] 2011	A=3.7 $\mu\text{m}^2$ l=40 $\mu\text{m}$ , w=4 $\mu\text{m}$ t=0.925 $\mu\text{m}$ s=1 $\mu\text{m}$	3.64 MHz 1770 (Vac)	100 V
NTHU	Al-SiO <sub>2</sub> -W Stack	TSMC 0.35 $\mu\text{m}$ [110] [111] [92] [102] TSMC 0.18 $\mu\text{m}$ [112]	Resonator (F.F. Beam, DETF,P.P. Beam, C.C. Beam)		[110] 2011	A=3.945 $\mu\text{m}^2$ l=40 $\mu\text{m}$ , t=3.945 $\mu\text{m}$ , w= 1 $\mu\text{m}$ s=500 nm	1.46 MHz 714 (Vac)	25 V

TABLE 4.1: CMOS-MEMS resonators state of the art.



Inst.	Material	CMOS Tech.	Configurations	Smaller Device	Ref. Year	Minimum Dimensions Coupling area (A) length (l), width (w), thickness (t), gap (s)	Features (fo and Q )	MEMS Bias Voltage
CMU	Silicon	TSMC 0.35 $\mu\text{m}$ , Jazz SiGe 0.35 $\mu\text{m}$ [104]	Vertical Resonators		[104] 2007	$\frac{A=5 \mu\text{m}^2}{l=28.5 \mu\text{m}, w=5 \mu\text{m}, s=1.45 \mu\text{m}}$	8.04 MHz, 3589 (Vac)	46 V
NTHU	$\text{SiO}_2\text{-Al}$ Stack	TSMC 0.35 $\mu\text{m}$ [103] TSMC 0.18 $\mu\text{m}$ [113]	Resonator (Lame and C.C. Beam)		[103] 2011	$\frac{A=6.56 \mu\text{m}^2}{l=55 \mu\text{m}, w=4 \mu\text{m}, t=1.64 \mu\text{m}, s=640 \text{ nm}}$	2.58 MHz 1212 (Vac)	120 V
CMU	Al- $\text{SiO}_2$ Stack	HP 0.8 $\mu\text{m}$ [90] HP 0.5 $\mu\text{m}$ [114] TSMC 0.35 $\mu\text{m}$ , Jazz SiGe 0.35 $\mu\text{m}$ [115] [116]	Resonator (Square Frame, Cantilever, Paddle)		[116] 2005	$\frac{A=20 \mu\text{m}^2}{l=63 \mu\text{m}, w=4 \mu\text{m}, t=5 \mu\text{m}, s_o=0.9 \mu\text{m}, s=25 \text{ nm}}$	6.18 MHz 996 (Vac)	20 V

TABLE 4.2: CMOS-MEMS resonators state of the art.



## 4.2 CMOS–MEMS scaling

Recently some contributions have appeared that present CMOS-compatible NEMS resonators for very high performance sensing [117] [118]. In these systems top-down approaches with mass production capability are used, obtaining NEMS devices with higher dimensions than CNT [17] and nanowires [18] but with very promising mass sensing capabilities. In order to keep on profiting the robustness of the CMOS standard process and decrease the dimensions of the top-down fabricated resonators we try to extrapolate our technological approach, previously used in AMS 0.35  $\mu\text{m}$  and UMC 0.18  $\mu\text{m}$  to ST 65 nm CMOS technology [119] where sub-100 nm dimensions can be defined.

The first consideration choosing the CMOS technology constitutes the available layers in the technology and how they affect to the resonator performance. In our particular case we will take special attention to its future application as a mass sensor based on resonant beams in its first flexural mode. In addition minimum dimensions mechanical switches will be developed using the back end metal layers with the aim to develop alternative transduced MEMS-based sensor with a mechanical ring oscillator configuration.

According to equation 4.1 (mass sensitivity of an in-plane C.C. Beam, as it was explained in section 2.4) the best mass sensitivity (the lower value of  $S_m$ , means that a variation of 1 Hz is obtained by a smaller amount of added mass) will be offered by a material with the highest Young modulus and the lowest mass density.

$$S_m \approx 0.74tl^3\rho\sqrt{\frac{\rho}{E}} \quad [kg/Hz] \quad (4.1)$$

Taking Table 4.3 into consideration, it can be easily appreciated how carbon nanotube is the best option. Respect the layers available in CMOS technologies, it is clear that polysilicon as a structural layer will be better than any metal layer (aluminum or copper) available in CMOS technologies, due to its mass density Young modulus ratio, as we can see on column 3 in Table 4.3. In this sense we chose ST

Material	Young modulus E[GPa]	Mass density $\rho$ [kg/m <sup>3</sup> ]	$\rho\sqrt{\frac{\rho}{E}}$ [ $\frac{kg}{m^3}\sqrt{\frac{kg}{m^3Pa}}$ ]	$S_m$ [g/Hz]
Polysilicon [120]	160	2230	0.263	$2.92 \cdot 10^{-23}$
Aluminum [91]	131	3000	0.454	$5.03 \cdot 10^{-23}$
Copper [121]	117	8920	2.462	$2.73 \cdot 10^{-22}$
Silicon Nanowire [122]	160	2230	0.263	$2.92 \cdot 10^{-23}$
Carbon Nanotube [123]	1000	2200	0.103	$1.14 \cdot 10^{-23}$

TABLE 4.3: C.C. beam mass sensitivity for different materials considering equal dimensions ( $l = 1 \mu\text{m}$ ,  $t = 150 \text{ nm}$ ).

(ST Microelectronics [119]) 65 nm CMOS technology, which at the date of starting the project (2010) it constituted the smaller technological node available in Europe practice [124] or *CMP*<sup>®</sup> (circuit multi-project, France) [125] in which polysilicon acts as transistor gate. In fact a polysilicon C.C. beam resonator with a length of  $1.5 \mu\text{m}$ , 60 nm width and 100 nm thickness will reach a mass sensitivity of 66 yg/Hz at 232 MHz resonant frequency matching the experimental mass sensitivity of a bottom up silicon nanowire [18].

In contrast, this reduction of the resonator size has the disadvantage of a difficult signal transduction due to a degradation of the signal to noise ratio and the increase of parasitic and not desired effects.

### 4.3 ST 65nm CMOS technology

Along this section the main characteristics of ST 65nm CMOS technology will be presented. A good technology knowledge will be necessary to get the maximum performance designs and adapt the post-CMOS process to release the structures.

The key technology features are:

- **Front-end key main features**

- Shallow trench isolation, isolated P–Well twin–tub, single poly CMOS process using a type (100) P– substrate in  $\langle 100 \rangle$  orientation.
- Nickel silicide on junctions and polysilicon gates and lines.
- Dual  $V_t$  transistors.
- IOs using 2.8nm or 5.0nm gate oxide for 1.8V or 2.5V respectively.
- Spacer technique.

- **Back–end key main features**

- Back–End with 6 or 7 metal layers.
- Damascene Copper for metal 1 to last metal.
- Low K ( $\sim 3.0$ ) inter – metal dielectrics for thin metal layers to reduce parasitic capacitance.

Damascene process is used in order to build the Back-end-of-line layers (BEOL) because they can not be defined by etching, as in aluminum layer, since copper can not be easily etched as it does not form a volatile by product. Moreover, between each BEOL layer an etch stopper is deposited. It is a thin layer normally based on SiN that controls the depth of an etching process as the etch rate on SiN is slower than in  $SiO_2$  or almost null. In figure 4.4 the process sequence that allows the definition of VIA1 and the deposition of Metal 2 is detailed in order to have a deeper understanding of the CMOS technology.

In figure 4.4 A) [126] M1 has been previously defined together with a low K dielectric. It can be observed how a thin etch stopper layer (SiN or SiCN) is defined on the top, bottom and in the middle of the dielectric. Moreover M1 has a dielectric barrier on top that avoids the diffusion of the copper into the dielectric. The process starts with a deposition of a hard mask that will define the M2. The photoresist is lithography patterned to fix M2 layer layout (4.4 B)). The etch stopper layer and the low–K inter layer dielectric (ILD) are etched using an anisotropic dry etch (figure 4.4 C)). Then the hard mask is etched and the surface is cleaned. Next a photoresist is applied again, and it is lithography

patterned to define the VIAS. Again a dry etch step erase the dielectric until the bottom Silicon Nitride etch stopper (figure 4.4 E) that it is opened with a special etch (figure 4.4 F)). Then, copper deposition is done, using an electro-chemical process: electroplating [127]. Once the Copper has been deposited a planarization step called chemical mechanical planarization (CMP) polishes the wafer until it has reached the bottom of the barrier layer. Then again a barrier layer is deposited to cover the top of the copper inlays, such that copper is fully encapsulated within the barrier material. This process is repeated in each metal layer level.

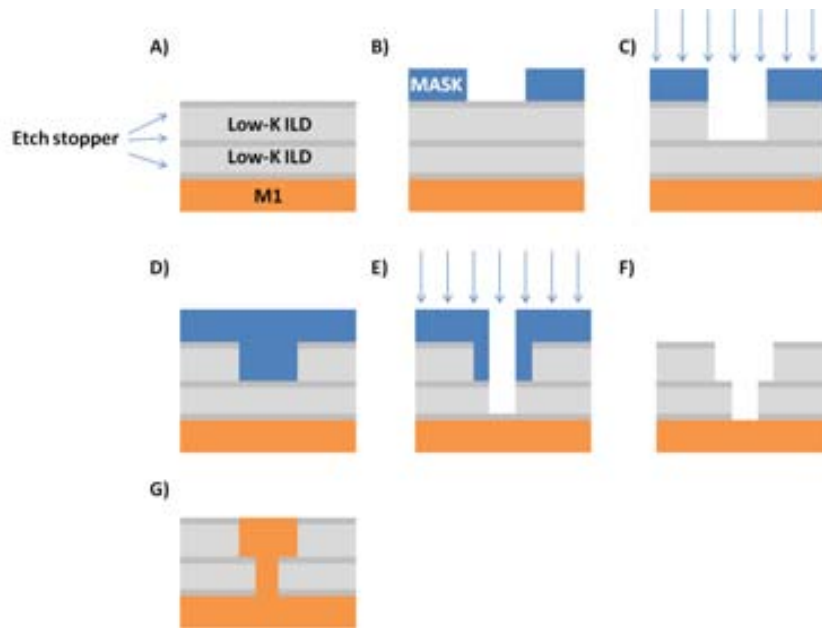


FIGURE 4.4: Schematic of dual damascene process (reproduced from [126]).

As it will be shown in section 4.4.2, damascene process and etch stoppers will have a deep impact in the post-CMOS NEMS releasing process.

ST 65nm presents 3 different technology options depending on the number and configurations of BEOL (see 4.4). The back-end metal layers are divided depending on its thickness: M1 (180 nm), MX (220 nm), Intermediate layer (MY 500 nm) and thick metal (MZ 900 nm). The technology option offered by Circuit Multi-Project (*CMP*<sup>®</sup>, France) was 7M-4X-0Y-2Z.

A schematic cross section of ST 65nm technology is showed in figure 4.6. Note that it is a simplified model because the fabrication process is not completely known (as the composition of etch stopper or copper barrier material) due to ST data

Configuration	Nº of metals	Metal 1	Thin Metal	Inter. Metal	Thick Metal
6M-4X-0Y-1Z	6	1	4	0	1
7M-4X-0Y-2Z	7	1	4	0	2
7M-4X-1Y-1Z	7	1	4	1	1

TABLE 4.4: ST 65nm technology options.

protection policy and some details (as the etch stopper necessary to define the ViAX) has not been included for simplification reasons.

The distance and minimum dimensions in any of these layers is given by the technology design rules, specified in table 4.5. Unlike the other CMOS technologies used to develop MEMS (AMS 0.35  $\mu\text{m}$  and UMC 0.18 $\mu\text{m}$ , the gap between a given layer (s) depend on the width ( $w_1$ ,  $w_2$ ) of the layers and length in parallel ( $l_c$ ) between them, as larger is the structure, bigger is the gap (see figure 4.5 ). This makes more challenging a capacitive read-out. In table 4.6, the minimum dimensions for M7, M5, M1 and poly beams are shown.

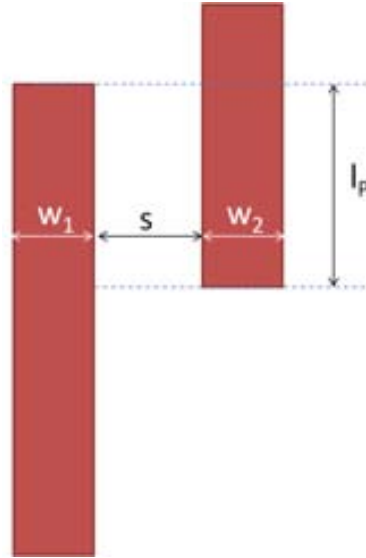


FIGURE 4.5: Design rules schematic

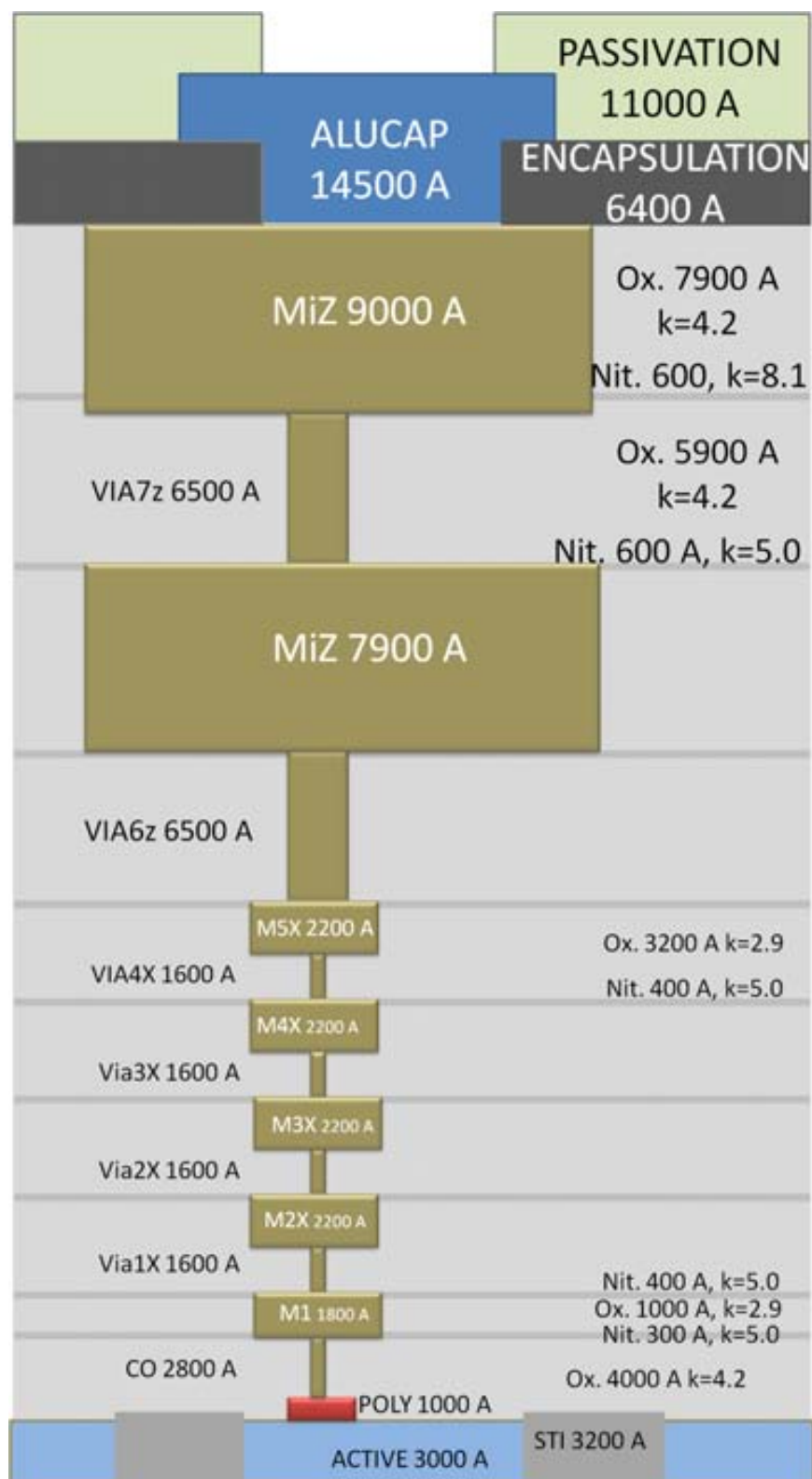


FIGURE 4.6: ST 65nm CMOS technology cross section (Note that in order to simplify the figure, the oxide and nitride thickness have been specified just for one of the MZ and MX layers.)

Layer	Design Rule	nm
PO	minimum width (w)	60
PO	minimum space on field oxide (s)	120
PO	space (s) if at least one PO width is $> 0.13 \mu\text{m}$ and if the parallel PO run length is $> 0.18 \mu\text{m}$	180
M1	minimum width (w)	90
M1	minimum space (s)	90
M1	space (s) if at least one metal line width is $> 0.20 \mu\text{m}$ and if the parallel metal run length is $> 0.38 \mu\text{m}$	110
M1	space (s) if at least one metal line width is $> 0.42 \mu\text{m}$ and if the parallel metal run length is $> 0.42 \mu\text{m}$	160
M1	space (s) if at least one metal line width is $> 1.5 \mu\text{m}$ and if the parallel metal run length is $> 1.5 \mu\text{m}$	500
MiX	minimum width (w)	100
MiX	minimum space (s)	100
MiX	space (s) if at least one metal line width is $> 0.20 \mu\text{m}$ and if the parallel metal run length is $> 0.38 \mu\text{m}$	120
MiX	space (s) if at least one metal line width is $> 0.40 \mu\text{m}$ and if the parallel metal run length is $> 0.40 \mu\text{m}$	160
MiX	space (s) if at least one metal line width is $> 1.5 \mu\text{m}$ and if the parallel metal run length is $> 1.5 \mu\text{m}$	500
MiZ	minimum width (w)	400
MiZ	minimum space (s)	400
MiZ	space (s) if at least one metal line width is $> 1.50 \mu\text{m}$ and if the parallel metal run length is $> 1.50 \mu\text{m}$	500

TABLE 4.5: ST 65nm design rules

Layer	Width (nm)	Thickness (nm)	Gap (nm)
M7	400	900	400
M5	100	220	100
M1	90	180	90
poly	60	100	120

TABLE 4.6: Metals and poly minimum dimensions (Note that the minimum gap cannot be always defined as it depends on the width of the driver and beam. More details are given in table 4.5).

## 4.4 MEMS fabrication in ST–65nm CMOS technology

### 4.4.1 CMOS–MEMS design

Once the technology has been presented, its different layers (M7, M6, M5 and poly) will be used to develop M/NEMS structures. In order to release the resonators just a consideration has to be taken into account, in the layout design, a window in the encapsulation enables a direct path for the etchants to reach the sacrificial layers and release the MEMS structures. It is defined just above the M/NEMS area. In this way the encapsulation and passivation layer will protect the rest of the chip during the post-CMOS process.

In order to define this window, some design rules need to be violated. To define a common PAD, layer CB define a hole in the encapsulation layer and CB2 another one in the nitride layer above it. Then this area is filled by the PAD (ALUCAP layer, a composite of aluminum and copper). To release the structures CB and CB2 layers are defined in a window called OPENPAD, as in the last case, but the ALUCAP layer is not included, see figure 4.7. On that way the oxide is exposed and the post-CMOS process can be done.

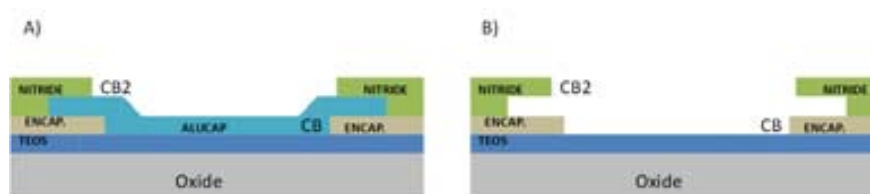


FIGURE 4.7: OpenPAD Configuration

The main different with the designs previously developed by ECAS group in other CMOS technologies (AMS and UMC) is that in addition to the OPENPAD in the encapsulation, VIAS were defined without filled them with metal [28]. Using this approach big amounts of oxide was not deposited and the releasing process was successfully achieved with short etching times. In ST 65nm technology, the foundry is very strict with the design rules and it did not allow the definition of



VIAS without metal. As a consequence, the releasing process will have to erase a lot of oxide to reach the depth of the buried devices as it is shown in figure 4.8 where the distance to M7, M6, M5, M1 and poly devices are shown.

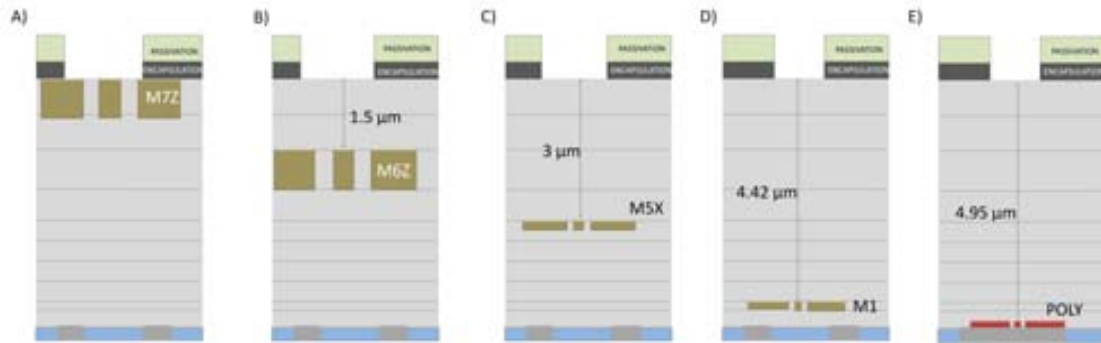


FIGURE 4.8: Schematic view of the buried devices (two drivers in plane resonators) before the post-CMOS releasing process. A) Metal 7, B) Metal 6, C) Metal 5, D) Metal 1 and E) polysilicon device.

In addition, a free dummies area was defined on top of all the resonator, in order to avoid the deposition of small metal pieces on top of the resonator after the releasing process. These metal dummies are needed to guarantee homogeneity density over all the metal layers of the CMOS process.

#### 4.4.2 CMOS-MEMS post-fabrication process

In addition to the big amount of oxide that has to be erased to reach M1 and poly devices, another important factor need to be taken into account. The etch stoppers (based on nitride), prevent the use of a releasing process based exclusively on a buffered fluorhydric acid (BHF) wet etching process [91], as its etch rate on nitride is much lower than in oxides [128]. Therefore, a post-CMOS releasing process based on a dry etching and buffered wet HF bath is used to remove the silicon oxide that surrounds the mobile structure.

A Reactive Ion Etching (RIE) using the Alcatel AMS-110DE has been established for the dry etching ( see table 4.7) . The etching time has to be adjusted to remove all the oxide that cover the resonator but not to damage the MEMS structures. After achieving an optimal etching time the oxide and Etch Stoppers above the

resonator were removed. A  $\text{SiO}_2$  etch rate of 5300 Å/min has been obtained. Only the oxide below the structure remains as it was expected, see figure 4.9 B).

Gas	Percentage	Parameters	Value
$\text{C}_4\text{F}_8$ (sccm)	30	Pressure (Pa)	0.33
$\text{CH}_4$ (sccm)	20	Power (Source, RF1 (W))	2500
He (sccm)	20	Power (Chuck, RF2 (W))	150

TABLE 4.7: Reactive Ion Etching specifications.

In order to release the resonator (etching the remaining oxide), the BHF wet etching is done after the RIE process, see figure 4.9 C). Again the etching time has to be adjusted to prevent the MEMS structure damage. We have found that once the dry etching time has been adjusted to eliminate all the etch Stopper layers above the MEMS structure, the releasing process is quite reproducible because the subsequent wet etching is very selective to copper.

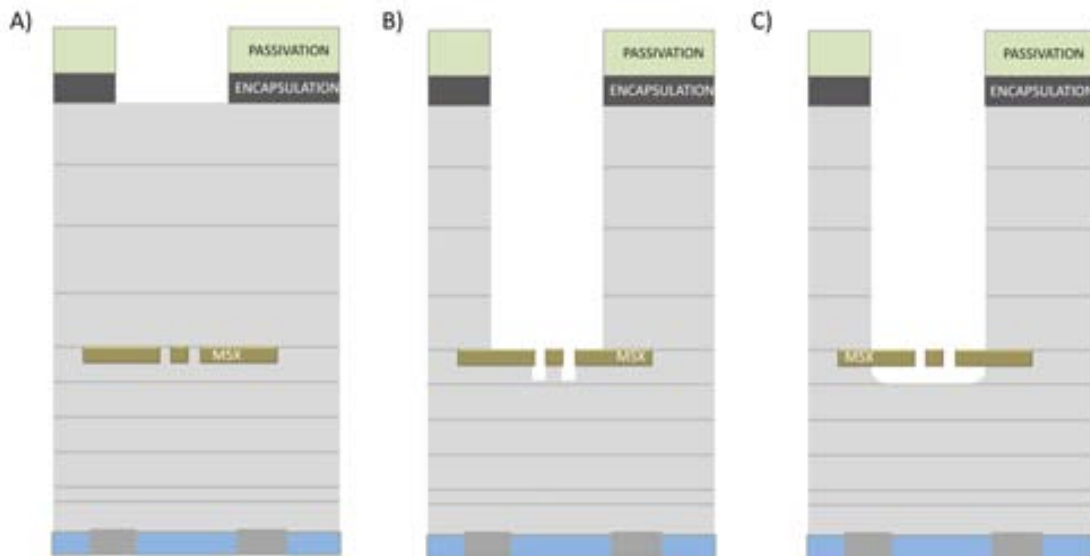


FIGURE 4.9: A) Schematic view of a M5 device before the post-CMOS releasing process (as received from the CMOS foundry). B) Structure after the dry etching. C) Device released after the Wet etching process.

## 4.5 Fabricated devices

Two different CMOS processes CHIPS (NEMSTRANS1 RUN (July 2011) and NEMSTRANS2 RUN (May 2013)) were designed trying to define the minimum dimensions allowed by the technology in order to develop high performance resonators and mechanical switches. M7, M6, M5, M1 and poly layers were used as structural layers. The CHIPS presented an approximated area of  $1\text{mm}^2$  (see figure 4.10).

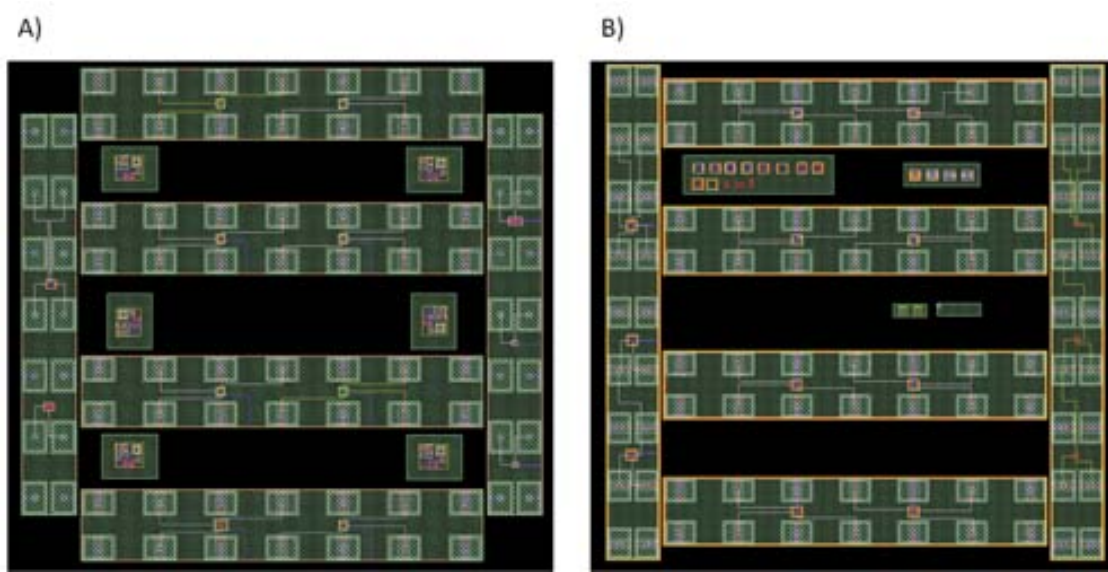


FIGURE 4.10: CHIP's layouts of A) NEMSTRANS1 RUN and B) NEMSTRANS2 RUN (Chips area =  $1\text{mm}^2$ )

In figure 4.11 an optical image of one CHIP can be observed. It can be appreciated how the chip is divided in two lateral columns and four rows of electrical PADS. The area between PADS row is compulsory to follow density design rules from the technology.

In figure 4.12 a scanning electron microscopy (SEM) image of two rows of PADS is shown. Two OPENPADS are highlighted in the middle of the rows that denote that a resonator is defined below them. In addition, it can be appreciated how dummies area is visible after the dry etching process. That shows that the encapsulation and passivation layers were damaged during the dry etching process. In order to avoid it, an additional process will have to be implemented to prevent

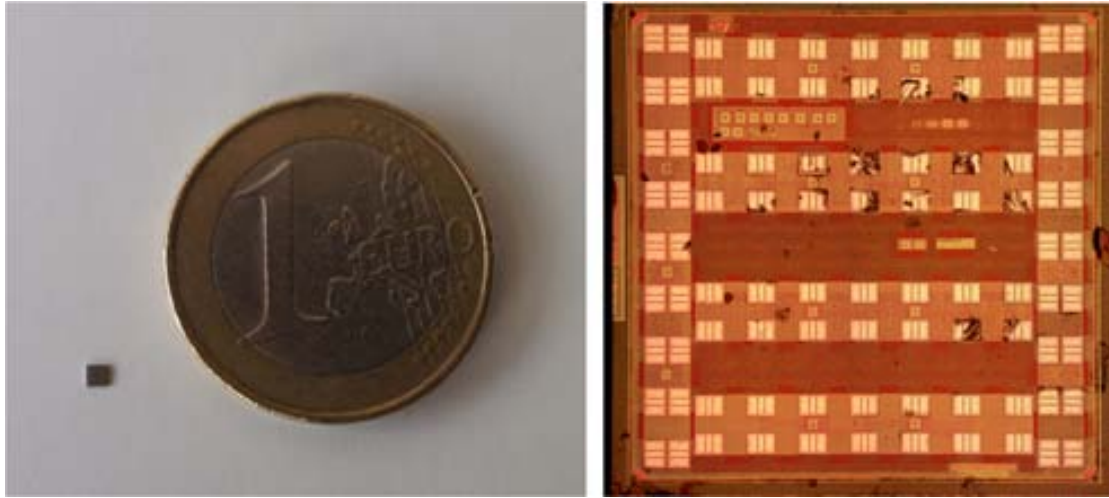


FIGURE 4.11: Photograph of a chip near an Euro coin and optical microscope image of the same chip.

the erase of these layers and allow the etch of the oxide above the MEMS structures without damage them. It will consist on the deposition and pattern of an additional layer resistant to the dry etching (as Aluminum) on top of the encapsulation. This new layer will cover all the CHIP except PADS and OPENPADS area. Different techniques can be used with this purpose at wafer level (ultra violet lithography, laser lithography, electron beam lithography, SOI stencil [129][22]). As the damage of the encapsulation and passivation layers do not prevent the releasing of the structures and their electrical characterization using PADS, which is our main goal, we will continue the characterization without adding this new step. Obviously this protection step will be a priority for the successful implementation of the MEMS with additional circuitry.

To characterize the technology properly, some focus ion beam (FIB) cuts were performed on a CHIP before the releasing process. In figure 4.13 A) and B) SEM images of FIB cuts in a M1 and poly resonators are showed. The different etch stoppers between layers have been highlighted with arrows. In order to check the effect of the wet etching on these layers a short etching was performed. As it can be appreciated in figure 4.13 C) the wet etching erases the silicon oxide but it is not able to remove the etch stopper layers.

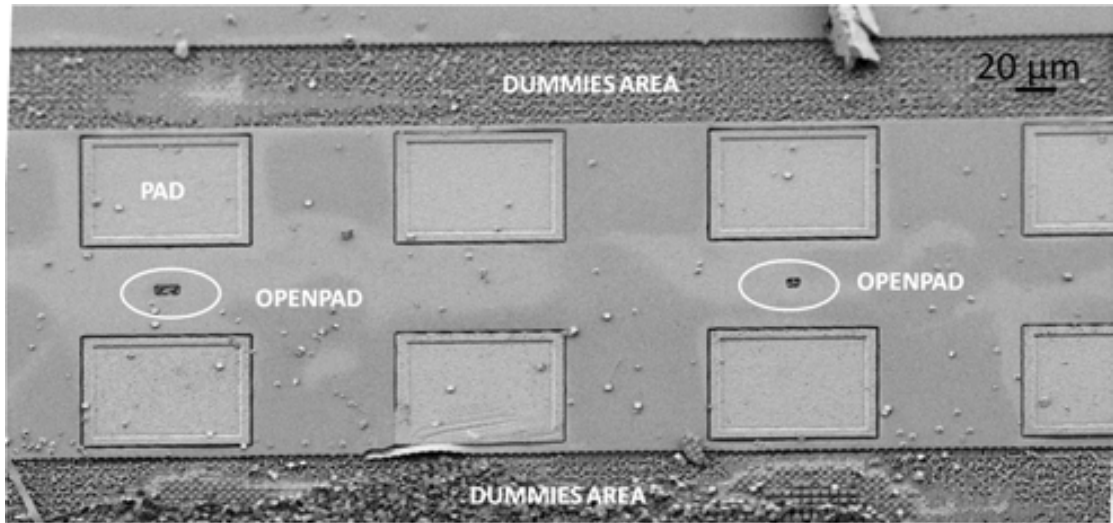


FIGURE 4.12: SEM images of a NEMSTRANS1 CHIP after a dry etching process.

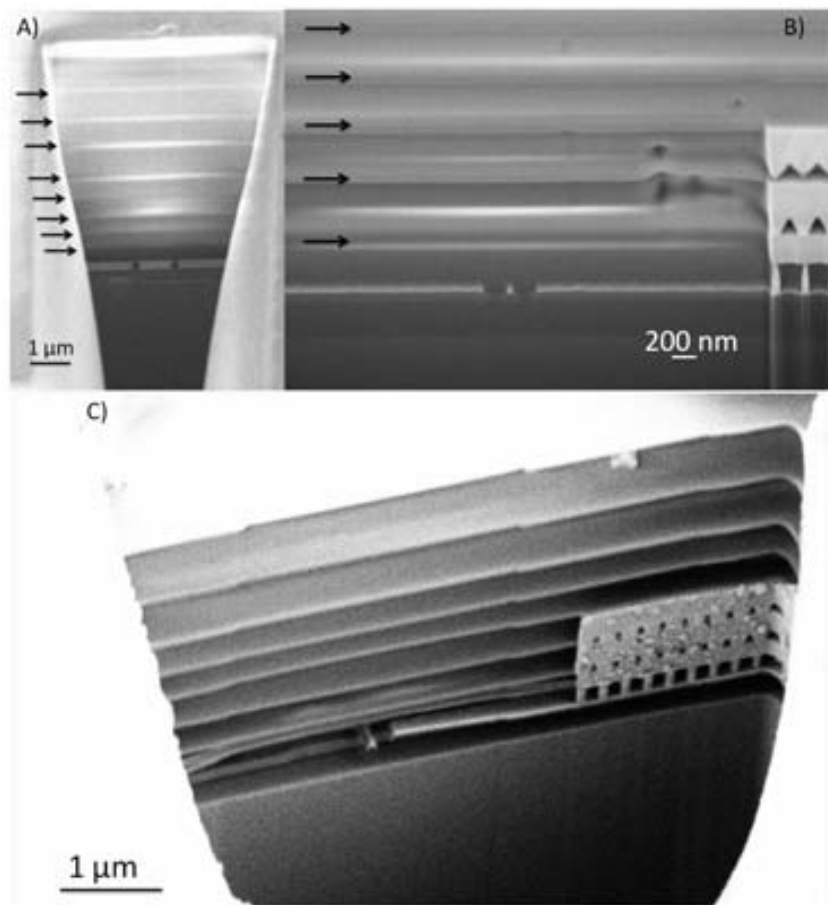


FIGURE 4.13: A) SEM image of a focus ion beam cut of the CHIP over a metal M1 resonator area as it is received from the foundry. The different silicon oxide and etch stopper layers are clearly appreciated and are indicated with an arrow. B) SEM image of a FIB cut of the CHIP over a poly resonator. C) SEM image of the poly resonator showed in figure B) after wet etching.

### 4.5.1 M7 and M6 metal MEMS devices

Devices fabricated in M7 and M6 are introduced together as they have the same thickness and design rules. The main difference between M7 and M6 devices is that M7 structures are not buried in oxide, they are visible in the OPENPAD window. It can be observed on figure 4.14 A) and B) how some residues appear on top of the fabricated M7 resonators. Taking into account that the encapsulation and passivation layers are deposited after the definition of M7 (although they are not defined on top of the resonator), some residues could be produced when they are deposited over the rest of the chip area. In figure 4.14 C) a FIB cut have been done in a M7 device in an area protected by the encapsulation. As it can be seen, the thickness and minimum gap agree with the theoretical value predicted by the design rules. In addition, it can be observed how the structure is not damage in this area as it is protected with the encapsulation and passivation layer. However, if the FIB cut is done in a M7 OPENPAD area, some residues appears that damage the structure as it has been highlighted in figure 4.14 D).

M6 resonators are buried in oxide, preventing the damage of the structure during the passivation and encapsulation formation. In figure 4.15, a M6 C.C. beam resonator is showed after a releasing process of 4.5 min RIE+ 3.5min wet etching. The resonator has been correctly defined and released (see table 4.8 for the drawn dimensions and finally obtained values). Note that the size of the OPENPAD has increased after the releasing process. The original size of the window is marked by the residues on top of the resonator.

	Length ( $\mu\text{m}$ )	Width (nm)	Gap (nm)
Layout	10	400	500
Measured	10.1	420	480

TABLE 4.8: M6 C.C. Beam dimensions (see figure 4.15)

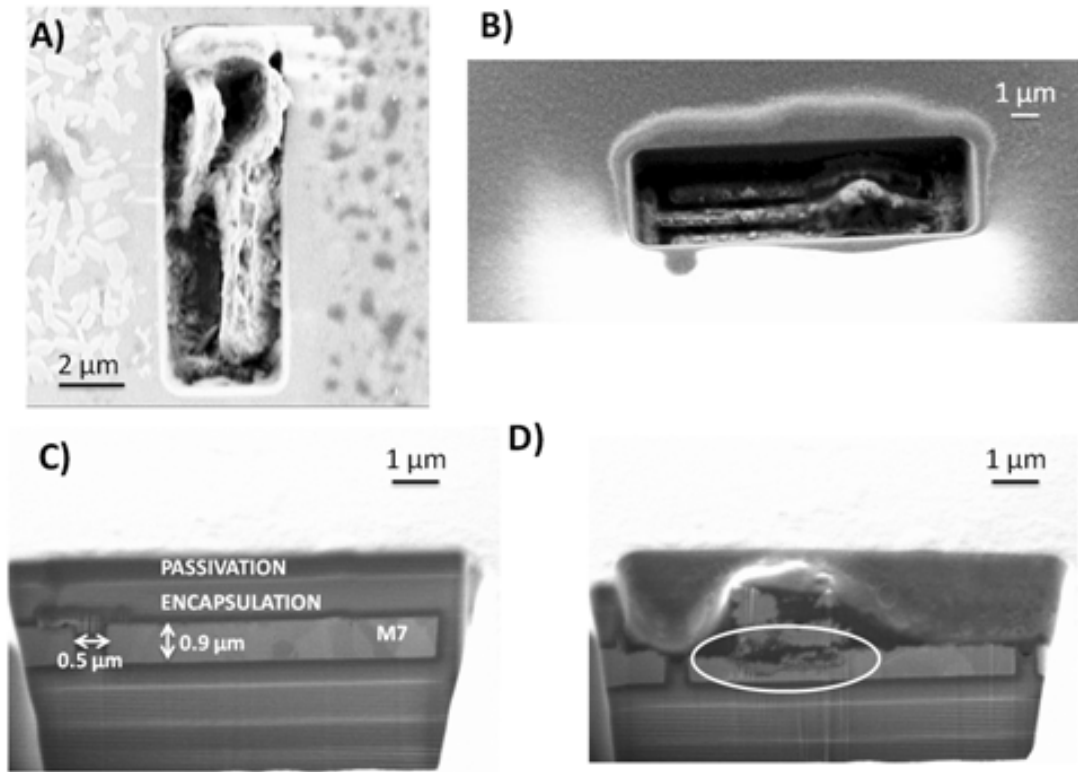


FIGURE 4.14: A) and B) SEM image of M7 devices before the post-processing (as received from the foundry). C) and D) SEM images of FIB cuts. Image C) in an area protected by encapsulation and D) in the OPENPAD.

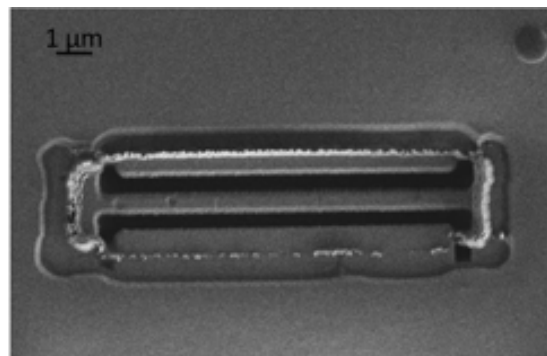


FIGURE 4.15: SEM images of a released M6 C.C beam (length= 10.1  $\mu\text{m}$ , width 420 nm and gap 480nm).



### 4.5.2 M5 Metal MEMS devices

M5 layer was chosen to develop MEMS devices as it is the first layer that exhibits MiX properties: a thickness of 220 nm, and design rules that allow the definition of a minimum layer width of 100 nm and a minimum gap of 100 nm. Additionally it is close to the CHIP surface, allowing a shorter post releasing process time and hence a less aggressive process for electrical PADS and encapsulation. In figure 4.16 SEM images of a FIB cut in a M5 resonator before the releasing process are shown. Again it can be observed how the experimental dimensions are slightly different than the values defined on layout (table 4.9). In addition, the structure presents a trapezoidal cross section.

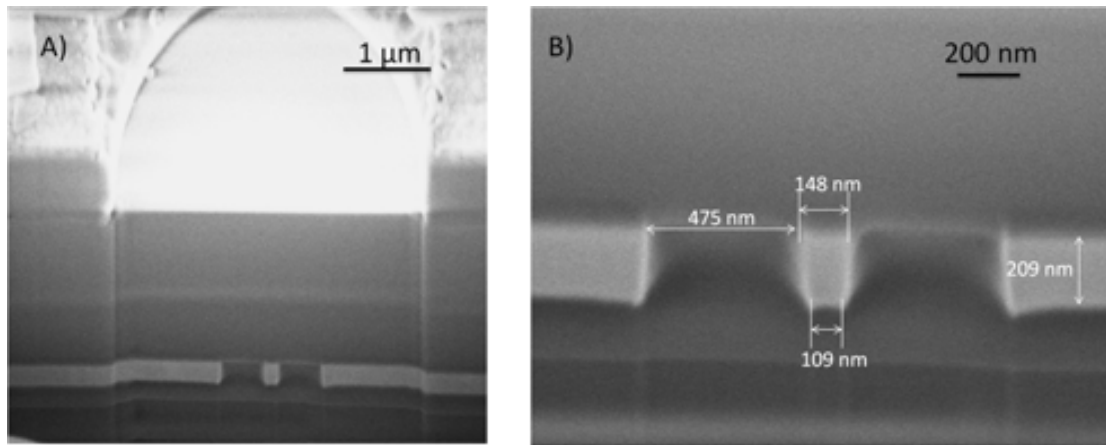


FIGURE 4.16: SEM images of a FIB cut in a M5 device.

	Width (nm)	Gap (nm)
Layout	100	500
Measured	148–109	475

TABLE 4.9: M6 C.C. Beam dimensions

M5 devices were released using a 5 min 30 sec RIE and a wet etching of 5 min. From figure 4.17 A) the MEMS resonator is released. However in figure 4.17 B) a tilted SEM image of the same resonator is showed and it can be seen how an oxide wall is formed below the resonator. A FIB cut in the resonator was performed (Figure 4.18) observing that although the resonator seems released a stack of copper and oxide has been formed. Moreover the trapezoidal shape has changed to a square cross section.



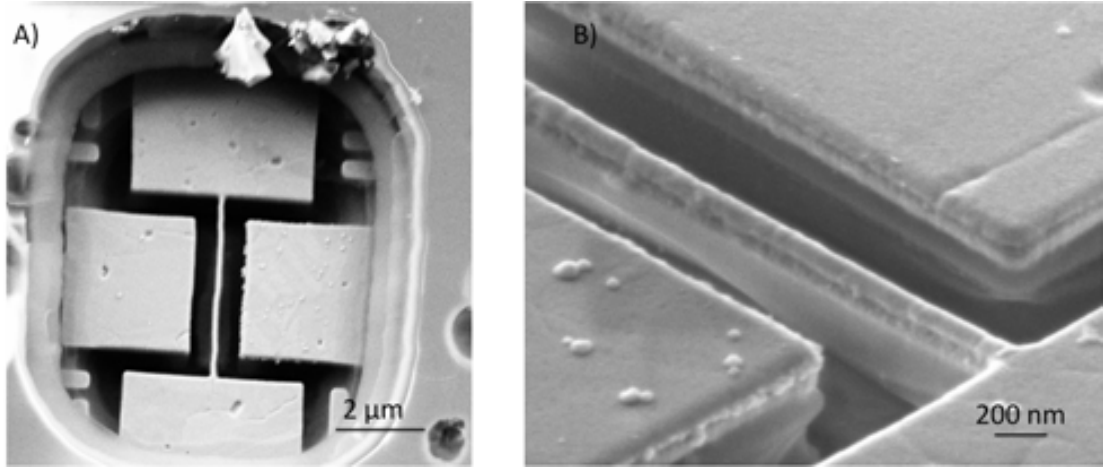


FIGURE 4.17: A) Top SEM image of a M5 C.C. Beam resonator ( $l= 4.32 \mu\text{m}$ ,  $w=117 \text{ nm}$ ,  $\text{gap}= 412 \text{ nm}$ ). B) Tilted view of the resonator.

The cross section shape change suggests that the copper structure is damaged in the RIE process. The extremes of the trapeze long side forms a copper wall (figure 4.19 B)) that in combination with the etch stopper below the structure forms a copper oxide stack that is not released after the wet etching process (figure 4.19 C) and figure 4.17 B)).

As it can be observed in figure 4.7 M6 devices have the etch stopper below them at a greater distance, 590 nm instead of 160 nm as in the M5 configuration. This greater distance could prevent the wall formation. In addition this phenomenon will not be observed in M1 Metal devices as they have the etch stopper in contact with their bottom side, so there is no oxide gap between the copper and the etch stopper to form a stack.

### 4.5.3 M1 devices

The main advantage of M1 layer is that it allows the definition of a minimum gap of 90 nm and structures with a width of 90 nm. But in order to do it, the parallel metal line (driver) needs to have a width smaller than 200 nm. If the driver is so narrow, it could be released in the post CMOS process and it could affect to the correct operation of the device. In order to fix the position of the driver and get a 90 nm gap, the configuration proposed in figure 4.20 is presented. It consist on

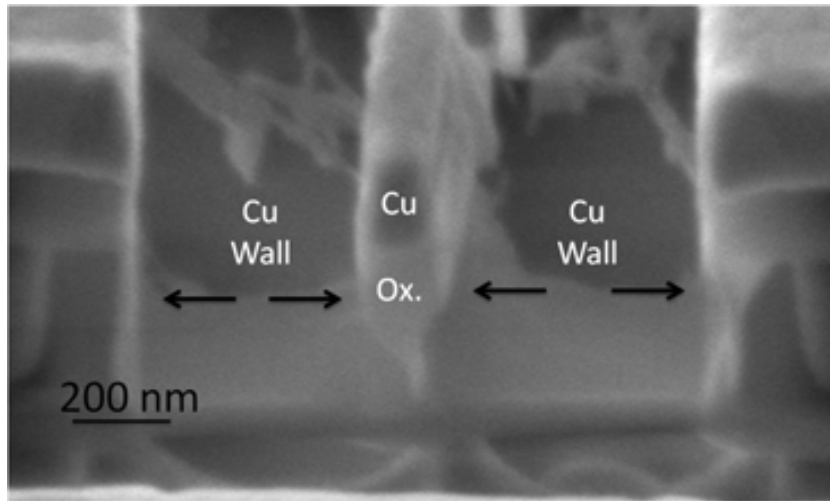


FIGURE 4.18: SEM images of a FIB cut in a M5 device after the releasing process.



FIGURE 4.19: Schematic view of the releasing process in a M5 devices. A) M5 structure before the releasing stage. B) Structure after 5 min 30 sec RIE. C) Devices after the RIE + 5 min WH.

define a driver with a width smaller than 200 nm, that allows the definition of a 90 nm gap, and anchored it with the upper metal.

Using this technique, minimum dimensions 2-T switches (section 5.3) and two drivers resonator (figure 4.21) has been defined. Again it can be observed in the FIB cut SEM images (figure 4.21) how the M1 structures present a slight trapezoidal shape and the value of width and gap vary due to this fact. The structures were released after a three steps RIE etching (4 min 30 sec + 3 min + 3 min) and the subsequent wet etching to erase the oxide below the structure.

Bigger gap resonators were also fabricated following the standard in-plane driver-resonator-driver structure. Figure 4.22 shows a released M1 resonator following this approach. Unlike M5 devices, where a stack was formed below the structure, the M1 structures are completely released. As it was shown in the previous section

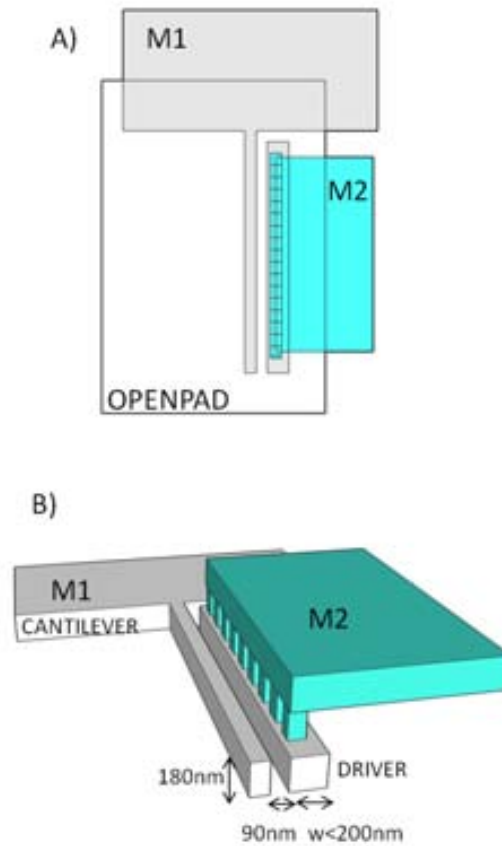


FIGURE 4.20: Schematic view of M1 configuration in order to get a 90nm gap.

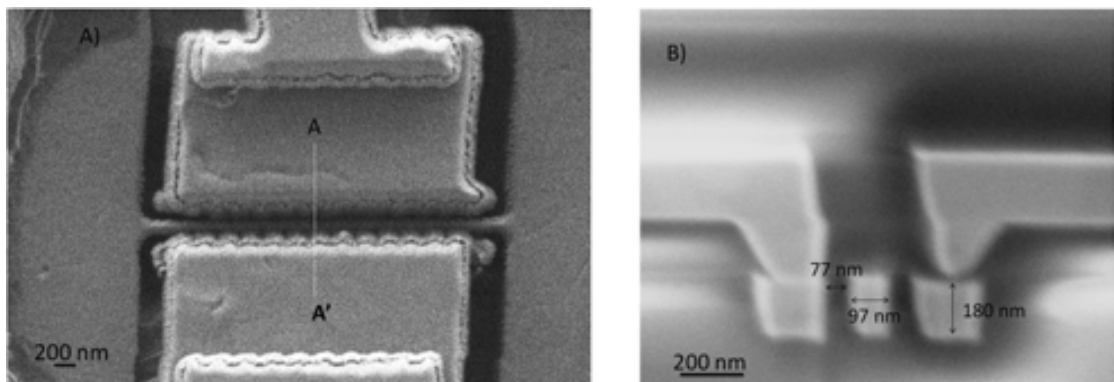


FIGURE 4.21: A) M1 2 drivers resonator ( $l=3.17\text{ }\mu\text{m}$ ,  $w=90\text{nm}$ ,  $s=90\text{nm}$ , defined on layout.) B) SEM image of a FIB cut before the releasing process.

the main differences between the two approaches is that M1 has the etch stopper in touch with its bottom side so no oxide gap exists between the metal and the etch stopper.

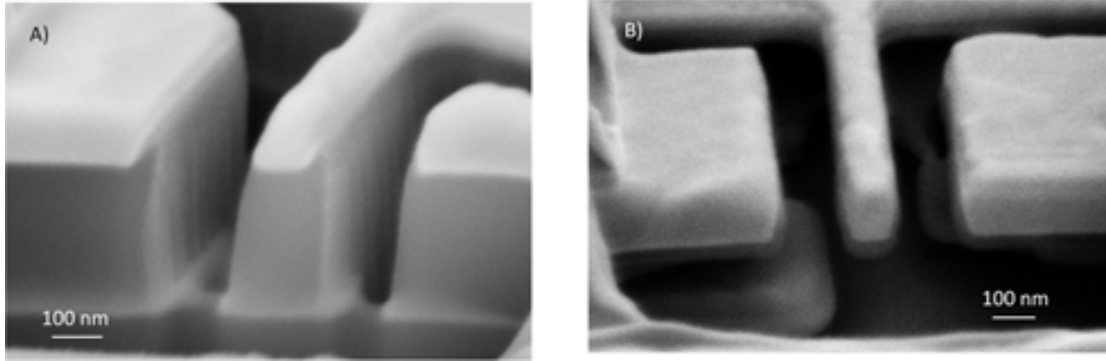


FIGURE 4.22: A) SEM image of a M1 resonator FIB cut after the RIE etching.  
B) SEM image of a M1 resonator FIB cut after the WH process.

#### 4.5.4 Polysilicon devices

Polysilicon devices show attractive features thanks to its mechanical properties, as it was shown in the introduction of the chapter, and in addition, the smaller dimensions which can be defined using this layer (width 60 nm and thickness 100 nm), see figure 4.23 that shows a SEM image of an unreleased poly c.c. beam cross section. On the other side, the minimum gap is bigger than M1 approach (120 nm instead of 90 nm).

In this case, cantilever and c.c. beam resonator were designed and released (figure 4.24). Polysilicon was not used as structure layer in order to design mechanical switches due to the poor contact resistance previously shown [130].

Again some differences between the layout dimensions and the fabricated devices were observed (table 4.10).

The structures were released after a three steps RIE etching (4 min 30 sec + 3 min + 3 min) and the subsequent wet etching to erase the oxide below the structure. Figure 4.25 shows two polysilicon c.c. beam structures after the releasing process. In figure 4.25 a FIB cut is performed in the middle of the released structure in

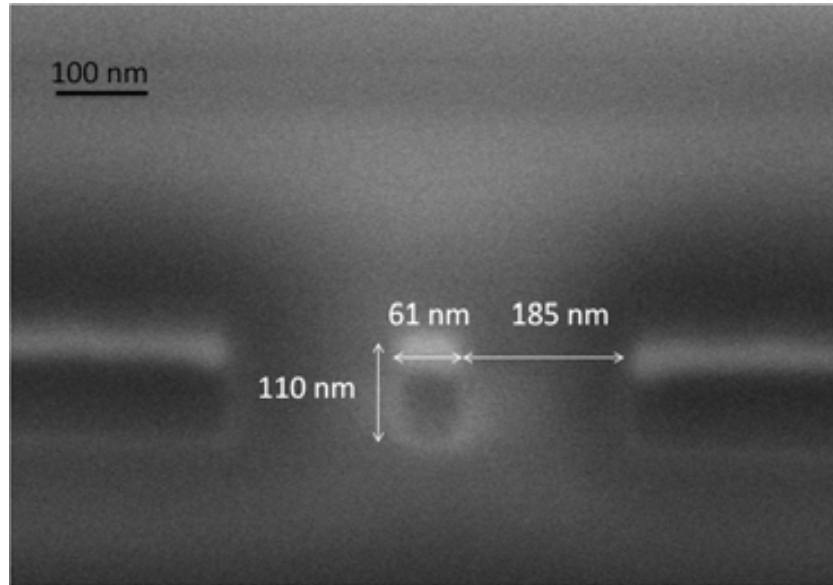


FIGURE 4.23: SEM image of a FIB cut in an unreleased two driver poly resonator. Theoretical dimensions  $w=60$  nm,  $t=100$  nm,  $s=185$ nm.

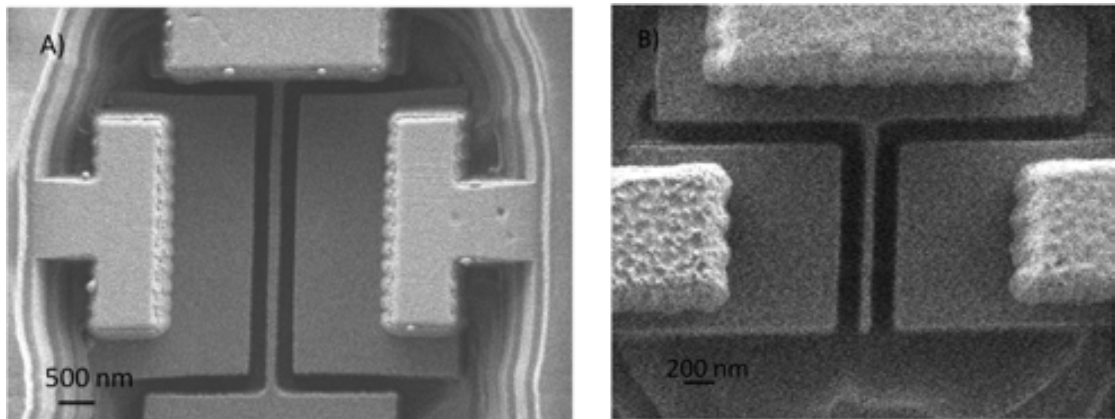


FIGURE 4.24: A) Polysilicon c.c. beam resonator. B) Polysilicon cantilever resonator. Dimensions details in table 4.10.

	Length ( $\mu\text{m}$ )	Width (nm)	Gap (nm)
C.C. Beam Layout	4	150	180
C.C. Beam measured	4.05	154	190
Cantilever Layout	1.5	60	180
Cantilever measured	1.58	68	175

TABLE 4.10: Layout and experimental polysilicon devices dimensions of the designs showed in figure 4.24 A) and B).

order to check that there is not oxide under it, as it can be observed (the structure bends upward due to residual stress).

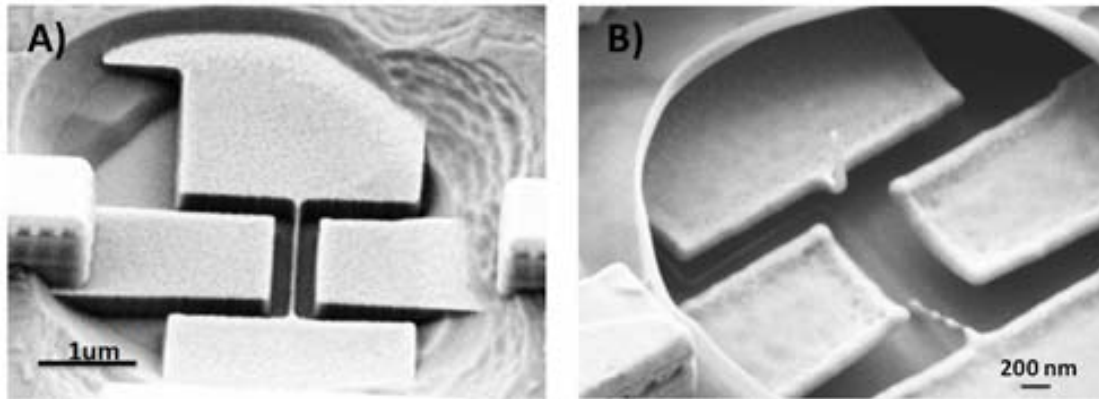


FIGURE 4.25: A) SEM image of a released poly resonator B) SEM image of a released resonator that presents a FIB cut in its central area.

In order to summarize all the devices presented in this section table 4.11 shows the different designed devices with main fabrication results.

## 4.6 Electrical characterization

In this section the electrical characterization of the resonators exposed in previous section will be shown. The electrical setup to characterize the resonators frequency response is showed in figure 4.26. The beam is biased at a fixed voltage (using the DC source Keithley 230), while an AC signal is applied to one of the electrodes (Network Analyzer Agilent E5100A output) to induce the beam movement and the generated capacitive output signal is measured in the other electrode connected to the input of the network analyzer. The frequency response of the transmission parameter ( $S_{21}$  parameter) is acquired.

The electrical characterization of the mechanical switches developed in metal M1 will be presented in section 5.3.








Layer	Device	Dimensions	Theoretical Features	Fabrication (Comments)
M7	Resonators			 Encapsulation and passivation residues appears on the M7 devices
M6	C.C. Beam Resonator	$l=10\ \mu\text{m}, w=400\ \text{nm}, t=900\ \text{nm}, s=500\ \text{nm}$	$f_o=14.9\ \text{MHz}, V_{snap}=200\ \text{V}$	
M5	Resonators			 Devices not released
M1	C.C. Beam Resonator	$l=3.17\ \mu\text{m}, t=180\ \text{nm}, w=90\ \text{nm}, s=90\ \text{nm}.$	$f_o=34\ \text{MHz}, V_{snap}=18\ \text{V}$	
M1	2-T switch (seccion 5.3)	$l=3.5\ \mu\text{m}, t=180\ \text{nm}, w=100\ \text{nm}, s=90\ \text{nm}.$	$V_{snap}=4\ \text{V}$	
poly	C.C. Beam Resonator	$l=4\ \mu\text{m}, t=100\ \text{nm}, w=150\ \text{nm}, s=180\ \text{nm}.$	$f_o=81\ \text{MHz}, V_{snap}=80\ \text{V}$	
poly	Cantilever Resonator	$l=1.5\ \mu\text{m}, t=100\ \text{nm}, w=60\ \text{nm}, s=180\ \text{nm}.$	$f_o=36\ \text{MHz}, V_{snap}=31\ \text{V}$	

TABLE 4.11: Fabricated devices using ST 65nm CMOS technology.

#### 4.6.1 M6 resonator

Figure 4.27 presents the M6 C.C. beam frequency response, in magnitude and phase, for different polarization voltages. The characterization was performed in ambient condition (room temperature and atmospheric pressure) using an excitation voltage of  $V_{AC}=0\ \text{dBm}$  and varying resonator bias voltage  $V_{DC}$ . High operating voltages are necessary due to the big gap between the resonator and driver (500 nm). However robust behavior was demonstrated despite the high operating voltage.



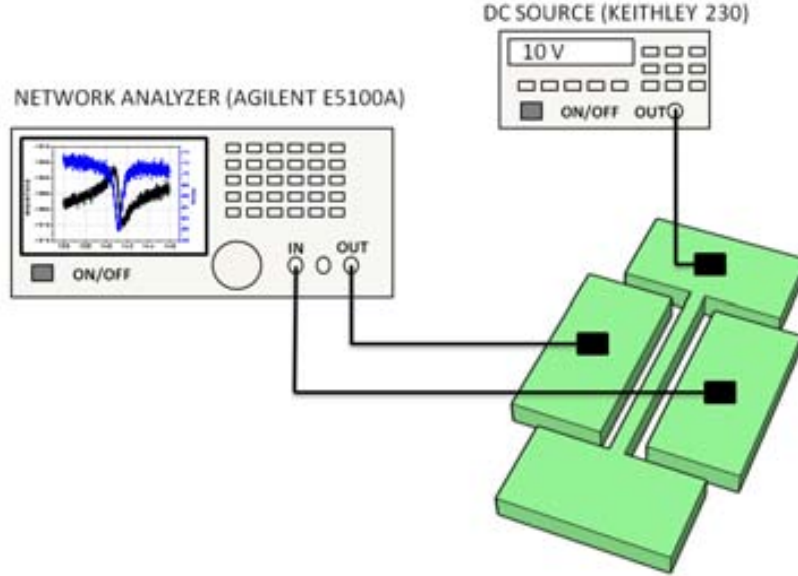


FIGURE 4.26: Test setup for two port frequency characterization measurement.

The resonance frequency is at 14.1 MHz approximately (at 80 V), near the theoretical value (14.9 MHz computed with  $E=117$  GPa and  $\rho=8820$  kg/m<sup>3</sup>).

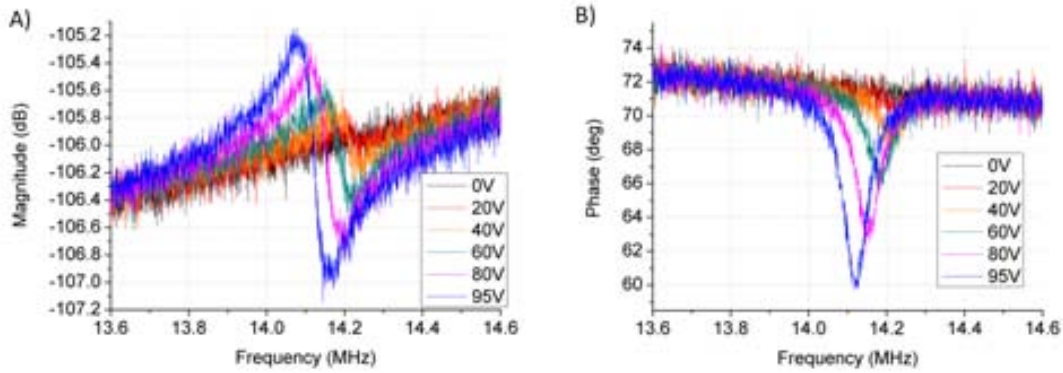


FIGURE 4.27: Frequency response A) magnitude and B) phase of the M6 c.c. beam ( $l=10$   $\mu$ ,  $w=400$  nm,  $t=900$  nm,  $s=500$  nm) for different DC bias ( $V_{AC}=0$  dBm) in air conditions.

Figure 4.28 shows how the resonant frequency varies with  $V_{DC}$ . It shows a linear dependence between the resonance frequency and the square of the effective driving voltage due to the spring-softening effect. The measured slope  $-15.4$  Hz/V<sup>2</sup> is smaller than the theoretical approximated value,  $-88.5$  Hz/V<sup>2</sup>, given by the expression 2.36. Note that the theoretical value is overestimated as it is calculated considering that at movement the beam and driver acts as a parallel plate capacitor and the beam profile is not taken into account.



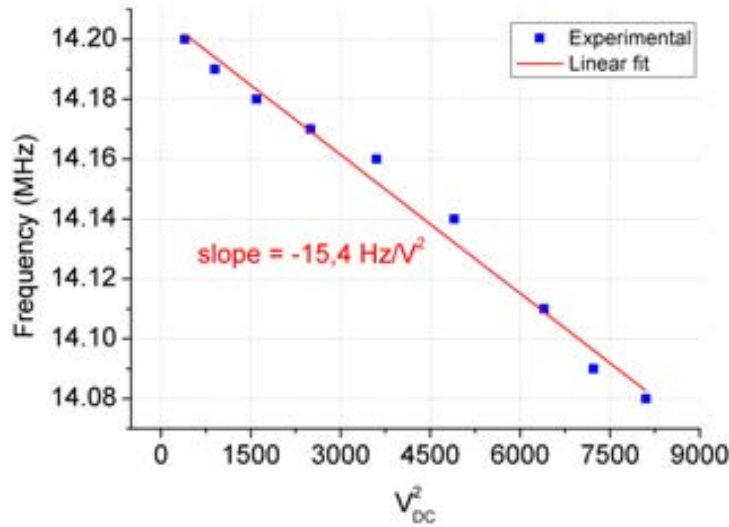


FIGURE 4.28: Plot of the resonance frequency versus squared effective DC-Bias for the M6 C.C. Beam ( $V_{AC} = 0dBm$ ) .

The Q value of the resonator has to be calculated from the phase measurements, as no 3dB peak is obtained in air measurements (see expression 2.28). The obtained value at  $V_{DC}=95$  V is 25. The low value of the quality factor could be caused by the reduction of the Q due to air damping or can be caused by the electrical characterization as the parasitic feedthrough capacitor between PADS that can mask the resonance peak, obtaining a lower value. To calculate its value expression 2.50 is used with the anti-resonance and resonance values obtained from the characterization at 95V ( $f_o=14.07$  MHz,  $f_p= 14.15$  MHz), getting a parasitic capacitance of 0.74 fF.

#### 4.6.2 M1 and Polysilicon resonators

Although M1 and Polysilicon devices were released, as it is shown in figures 4.25 and 4.22, resonance was not measured using a capacitive readout.

As it was shown in section 2.3, the ratio between the parasitic impedance and the motional resistance indicates if the motional current is masked by the parasitic capacitances (see equation 2.49).  $R_m$  is obtained from expression 2.48, while the parasitic capacitance ( $C_{PAR}$ ), mainly produced by fringe capacitance between

PADS ( $C_{pp}$ ) and excitation and readout electrodes ( $C_{dri}$ ) (see figure 2.8), can be estimated using Coventor simulations ( $C_{PAR}=C_{dri} + C_{pp}$ ).

In addition the value of the motional current has to be taken into account in order to check if our equipment is able to measure its output level. The value of the motional current under capacitive detection can be estimated using expression 2.40.

Parasitic capacitance values and motional resistance of M1 and poly resonator are summarized in table 4.12 :

Design	Dimensions	$R_m$ (M $\Omega$ )	$C_{PAR}$ $Z_p(\omega = \omega_o)$	$I_m/I_p$	$I_m$
Poly Cantilever	l=1.5 $\mu$ m, w=60 nm, s=180 nm, t= 100 nm	16.79	$C_{pp}=0.25$ fF $C_{dri}=26.1$ aF $C_{PAR}=0.27$ fF $Z_p(36$ MHz)= 16.37 M $\Omega$	0.97	13 nA
Metal 1 (M1)	l=3.17 $\mu$ m, w=90 nm, s=90 nm, t=180 nm	4.20	$C_{pp}=0.25$ fF $C_{dri}=105$ aF $C_{PAR}=0.35$ fF $Z_p(34$ MHz)= 13.37 M $\Omega$	3.18	54 nA

TABLE 4.12: Electrical model parameter for poly and M1 resonator. ( $V_{AC}=0$  dBm,  $V_{DC-poly}=20$  V,  $V_{DC-M1}=15$  V and  $Q=100$ ).

As it can be observed a  $I_m/I_p$  ratio near 1 is obtained for the poly resonator while a higher value (3.18 ) is obtained for the M1 device thanks to its smaller gap (a lower motional resistance,  $R_m$  , is obtained). In addition the value of the motional currents are in the nano-Amps range, currents that can be measured using the Network Analyzer (Agilent E5100A).

The value of the parasitic capacitance was measured experimentally measuring the background level of the magnitude frequency response for excitation frequencies much higher than the resonant frequency ( $\omega \gg \omega_o$ ), where the current at the output is mainly given by the parasitic branch due to the high impedance of the RLC, and biasing the beam to  $V_{DC} = 0V$ . Under this conditions, the experimental values obtained were bigger than the theoretical (3.61 fF for poly and 12 fF for

M1 resonator) preventing capacitive read-out. In fact with this larger parasitic capacitances the ratio  $I_m/I_p$  is 0.07 for poly and 0.09 for M1 device.

In order to overcome this problem, an amplifier stage could be integrated at the output of the resonator to decrease parasitic capacitance [20]. The readout circuitry has to be integrated on-chip along with the mechanical transducer in order to eliminate the parasitic capacitance introduced by the bonding pads and external wires. This is the one of the main advantages of CMOS-MEMS, the possibility of co-integrated MEMS and circuitry in the same fabrication process.

Another possible solution is to change the transduction method. It has to be easily implemented using a CMOS-MEMS approach and as a consequence it has to be based on CMOS-compatible material. In addition the provided output signal should be high enough to be detected without any additional circuitry despite the device size reduction. A good candidate to substitute capacitive readout in these minimum dimensions devices could be resonant gate transduction that get benefit of the gain of a transistor to produce high motional currents. It is based on the modulation of the charges on a transistor by the movement of a mechanical structure. This transduction method will be studied and implemented in a CMOS technology (AMS 0.35  $\mu\text{m}$ ) in chapter 6.

Meanwhile, further efforts using mixing technique [131] or optical transduction [132] can be performed in order to obtain the device resonant response and study the mechanical properties of the fabricated devices.

## 4.7 Conclusions

MEMS devices were successfully integrated on ST 65nm technology, the smallest node where released MEMS devices has been fabricated (see tables 4.1 and 4.2 ).

A combination of wet and dry etching processes has been established to release minute resonators monolithically integrated in this CMOS process. It has been

successfully demonstrated that it is possible to fabricate devices based on polysilicon layer and M1 copper layer with dimensions down to 60 nm x 100 nm and 90 x 180 nm respectively. The resonators size is similar than bottom-up nanowires, but with the advantages of a fully CMOS integrated process, which overcome the problem of further mass-production. They are the smallest devices fabricated following a CMOS-MEMS approach as it can be observed in table 4.13 that compares the fabricated devices with the previous smallest CMOS-MEMS reported in tables 4.1 and 4.2 .

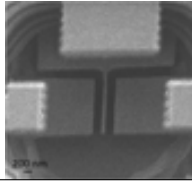
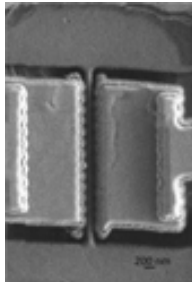


Material	Device	Cross section	length( $\mu\text{m}$ ) gap (nm)
		( $A=w \cdot t$ ) Thickness Width	
Polysilicon		$A= 0.006\mu\text{m}^2$ $t=100\text{ nm}$ $w= 60\text{ nm}$	$l=1.5\ \mu\text{m}$ $s=180\text{ nm}$
Copper		$A= 0.0162\ \mu\text{m}^2$ $t=180\text{ nm}$ $w=90\text{ nm}$	$l=3.17\ \mu\text{m}$ $s=90\text{ nm}$
Polysilicon [108]		$A= 0.0987\ \mu\text{m}^2$ $t=282\text{ nm}$ $w=350\text{ nm}$	$l=13\ \mu\text{m}$ $s=150\text{ nm}$ $s=40\text{ nm}$
Aluminum [28]		$A=0.1624\ \mu\text{m}^2$ $t=580\text{ nm}$ $w=280\text{ nm}$	$l=2.7\ \mu\text{m}$ $s=280\text{ nm}$

TABLE 4.13: Minimum dimension CMOS-MEMS State of the Art.

# Chapter 5

## CMOS–MEMS switches

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*In this section MEMS switches fabricated using an intra-CMOS approach in AMS 0.35  $\mu\text{m}$  and ST 65 nm commercial CMOS technologies will be presented. They can be divided in three different groups: MEMS switches implemented in AMS 0.35  $\mu\text{m}$  BEOL metal layers or stack of BEOL metal materials, mechanical switches based on AMS 0.35  $\mu\text{m}$  Metal–Insulator–Metal capacitive module and finally copper switches implemented in Metal 1 of ST 65 nm technology.*

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### 5.1 Switches based on AMS 0.35 $\mu\text{m}$ back-end metal layers

This section presents 0.35  $\mu\text{m}$  CMOS AMS metal MEMS switches monolithically integrated using the fabrication process previously reported in section 4.1.1. In this way advantages in terms of CMOS mass production capability, fabrication process robustness and the possibility of M/NEMS integration with an additional circuitry without any additional effort are demonstrated.

### 5.1.1 MEMS devices

Three Terminals (3T) MEMS switches were designed (figure 5.1 A) and B)). The main advantage of 3T configuration is that actuation and read-out can be done at different voltages as the movable structure (BEAM) will contact only with the read-out electrode (READ) thanks to a smaller gap, in comparison with the actuation electrode (ACTUATOR).

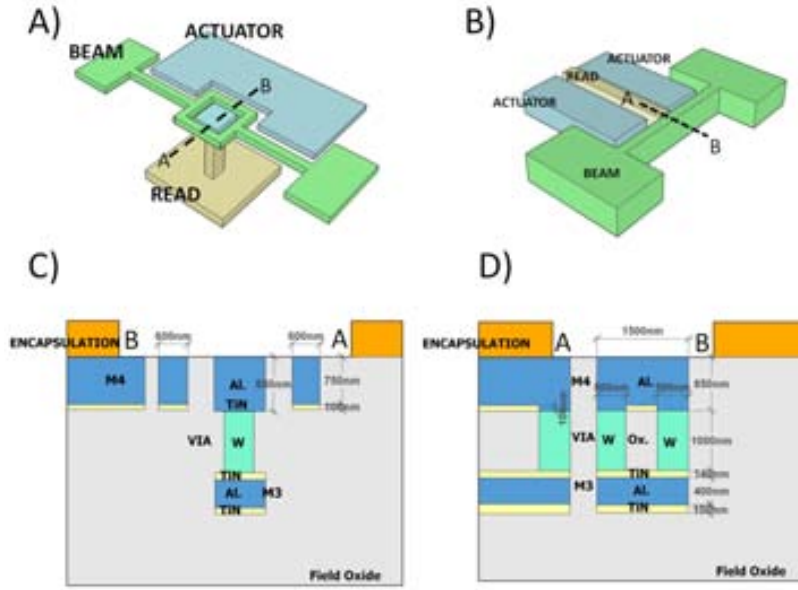


FIGURE 5.1: A) M4 configuration where it can be appreciated how the readout electrode is composed of a pillar formed by M4–VIA3–M3. B) Stack configuration switch composed by a clamped beam where we have defined two actuator electrodes (blue) and a read-out electrode (light brown) with a smaller gap. C) M4 Switch cross section. D) M4–VIA3–M3 stack configuration cross section.

For an in-plane c.c. beam configuration, the snap-in voltage value is given by (equation 3.11 and 2.21):

$$V_{PI} \propto \sqrt{\frac{E w^3 s^3}{\varepsilon l^4}} \quad (5.1)$$

As it can be observed from equation 5.1, small gaps and widths are necessary in order to get low snap-in voltages. Respect the length, there is a trade-off between the snap-in voltage and the overall rigidity of the structure which can

be stuck to the electrode if very long structures and thus low  $k$  structures are defined. In relation with the material for the MEMS switch we are limited by the different layers that AMS 0.35 $\mu\text{m}$  CMOS technology offers: aluminum (metal layers), tungsten (VIAS) and polysilicon (transistor gate). The smallest width and gap are achieved using polysilicon. However it was found [130] that it shows low  $I_{ON}/I_{OFF}$  current ratio (due to a big contact resistance value) and poor reliability, despite its small gaps (length=13 $\mu\text{m}$ , length coupling=9 $\mu\text{m}$ , width=0.35 $\mu\text{m}$  and gap=40nm). In this section we present two different approaches using the back-end of line (BEOL) metal layers of the CMOS technology: aluminum switches (using the top metal layer, M4) and aluminum-tungsten stack (using the M4-VIA-M3 layers as a stack), see cross sections in figure 5.1.

The M4 aluminum switches configuration tries to maximize the actuation coupling area with a novel structure based on a modified clamped clamped beam. In this configuration the read electrode is placed in the middle of the clamped-clamped beam, through a squared cavity which is electrically contacted and mechanically anchored using vias to the M3 layer in a 3D design (figure 5.1 A and figure 5.2). In this way all the beam length is active for actuation. The advantage of the second approach, based on a thick metal stack, is that it can support higher currents and eventually it will present smaller ON resistance due to a bigger contact area in comparison with the M4 approach. The stack approach is composed of Al, thin layers of TiN and tungsten W, with an overall thickness of 2.39  $\mu\text{m}$  (see figure 5.1 D). This latter material has high melting point that makes it suitable to stand high temperatures that appears in the snap-in event due to the Joule effect, increasing the switch yield. We have observed that during the releasing process the aluminum at the edges is etched so we expect that tungsten will be the contact material on this stack configuration (see figure 5.3 B).

The fabricated 3T switches are shown in the scanning electron microscope (SEM) images in figure 5.2 and 5.3. Due to the length of the beams a clamped-clamped configuration has been used instead of a cantilever in order to avoid stress and sticking problems, despite higher snap-in voltages will be obtained. In both configurations (M4 and M4–VIA–M3) the gap between the actuator electrode and

the beam is designed in the layout at 500 nm while the gap between the read electrode and beam is defined at 400 nm. These are the minimum distances which have been proven to be attained from the used CMOS technology (according to the technology rules the minimum allowable distance between M4 layers is 600 nm). Note from these SEM images that the experimental gaps are a bit smaller than the defined layout gaps: 460nm for the actuation and 310nm for the readout gap in the M4 Switch (see figure 5.2) and 420nm/300nm respectively in the stack approach (see figure 5.3).

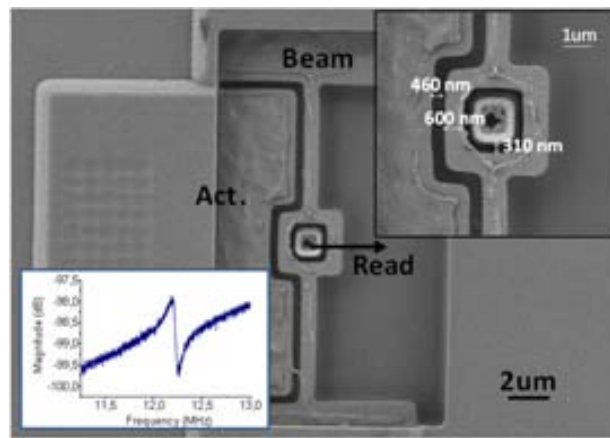


FIGURE 5.2: SEM images of a M4 clamped-clamped beam switch (length=19μm, width=600nm) and frequency response (inset).

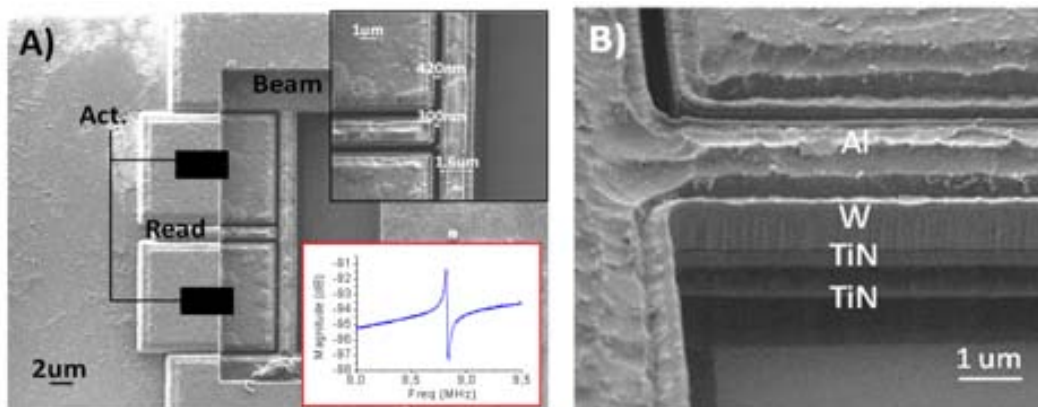


FIGURE 5.3: A) Stack configuration clamped-clamped beam SEM images (length=30μm, width=1.5μm,) and frequency response (inset). B) Lateral tilted SEM image where the different stack material after MEMS releasing can be observed.

In the insets of both figures 5.2 and 5.3 the clamped-clamped beam frequency response in ambient conditions is provided in order to demonstrate that the MEMS



structures are fully released. The experimental resonant frequency for the M4 configuration is 12MHz which is coherent with the computed in-plane fundamental frequency ( $f=11.9\text{MHz}$ ) considering a simple clamped-clamped beam (not real structure) composed exclusively of TiN ( $l=19\mu\text{m}$  and  $w=600\text{nm}$ ). We are assuming that almost all the Aluminum has been erased during the releasing process as it is clearly seen in the SEM image of figure 5.2, thus only TiN has been used as material for the computation. For the stack configuration we have used finite element simulation due to the different materials layers, obtaining a fundamental resonance frequency at 9.1 MHz which is in accordance to the experimental one.

### 5.1.2 Electrical characterization

The electrical characterization of the switching behavior was done using a parametric semiconductor analyzer (B1500A from Agilent). A voltage sweep is applied to the actuator electrode while the beam is polarized to a fixed voltage and the current is measured in the three terminals. Figure 5.4 shows the electrical response of the M4 switch. As it can be seen snap-in phenomenon appears at 18.8 V (21.8 V at the actuator minus 3 V at the beam) showing an  $I_{ON}/I_{OFF}$  ratio of 300, with a computed slope of 24 mV/decade. The gradual pull-out behavior found in figure 5.4 A), is due to a weak elastic force of the CC beam to overcome the adhesion forces between the driver and the beam. Similar behavior has been reported in [133]. The switch was operated over 20 cycles (see figure 5.4 B)). It can be seen how the  $I_{ON}$  current is reduced in the last cycle, due to an increase in the contact resistance value.

Figure 5.5 shows the electrical response of the stack configuration switch during a voltage sweep. As it can be observed, the snap-in event is detected in the actuator and beam electrode when 51 V are applied in the actuator terminal. In the read-out electrode this phenomenon can be detected at a smaller voltage (47.9 V) thanks to its smaller gap, although its poor contact resistance produces a small current variation (see current in figure 5.5 top). In this way a 3T switching behavior is demonstrated for the stack configuration although the current level is too low for

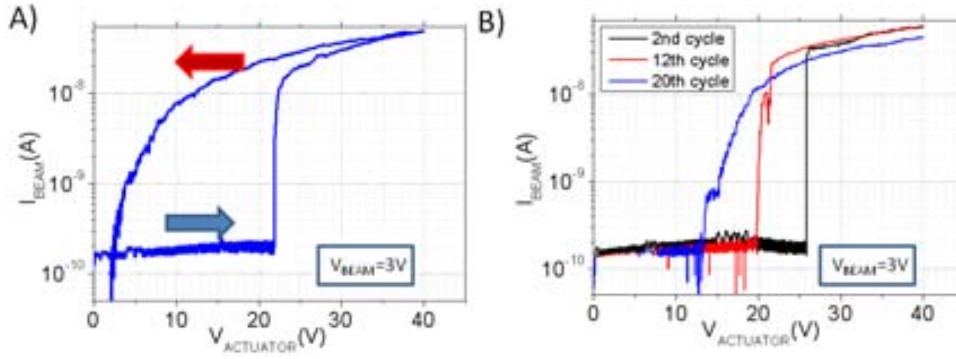


FIGURE 5.4: A) M4 Switch (device figure 2a, length=19  $\mu\text{m}$ , width=600nm,  $s_0$ =500nm,  $s_1$ =400nm) electrical characterization showing snap-in when the actuator reached 21.8 V. B) Different cycles of switching events are shown (only sweep up) . Note the degradation on the  $I_{ON}$  current level of last cycles (20th).

a proper operation. Considering snap-in with the actuation electrode (as a 2T switch) this stack configuration presents a bigger  $I_{ON}/I_{OFF}$  ratio ( $1.10^3$ ) than M4 approach. This stack switch worked for several tens of cycles with a computed slope of 5 mV/decade which is comparable with the ones reported in [76] [74] in which a non monolithical CMOS integration approach is used.

In both cases the switching behavior, with a clear difference between ON and OFF current levels, occurs when the beam is contacting directly with the actuator electrode instead of contacting only with the read electrode. In order to avoid this effect (catastrophic pull-in) the read-out gap ( $s_{READ}$ ) should be smaller than 0.44 the actuation gap ( $s_{ACT}$ ),  $s_{READ} < 0.44 \cdot s_{ACT}$ . As the minimum gap defined in this layer is 400 nm, the actuation gap should be bigger than 909  $\mu\text{m}$  obtaining very high snap-in voltages. In the stack configuration the current at the readout electrode shows a low value due to a poor constant resistance. It has also been found that some of the tested devices required very high snap-in voltages which irreversibly damage the switch due to field emission. Although we have reported switching behavior, new designs and approaches must be developed in order to decrease the snap-in voltages and obtain real 3-T operating switches using the BEOL metal layers of the CMOS technologies. Among them, we will consider new structures based on cantilevers and the use of the capacitive modules available in analog CMOS technologies based on MIM (metal insulator metal) modules which offer gaps smaller than 50 nm.

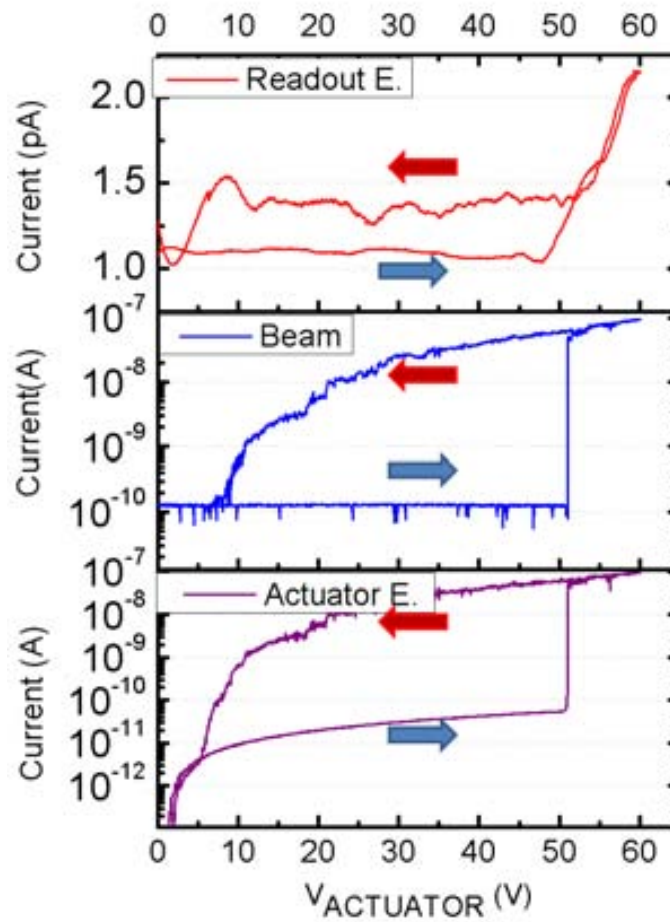


FIGURE 5.5: Stack Switch electrical characterization showing the hysteresis cycle due to snap-in (blue arrow) and snap out (red arrow) . Current level at the actuator (Bottom) and Beam (middle) is almost the same after the snap-in event. However, at the read out electrode (top curve) the snap-in event is detected for a smaller voltages being the current change almost negligible.

## 5.2 Switches based on capacitive MIM module

In the previous section, MEMS switches were fabricated using the back-end metal layers of AMS 0.35 $\mu$ m CMOS technology. However their large gaps translated into high pull-in voltages. With the aim of getting small gaps the Metal-Insulator-Metal (MIM) module, available in analog CMOS technologies, has been used to define the mechanical structures. A schematic view of the MIM module is presented in figure 5.6. It is formed by a metal insulator metal sandwich whose insulator layer (based on nitride) presents a small thickness (27 nm). Thanks to this feature, big capacitances can be fabricated using small areas and makes it attractive to

define out of plane mechanical switches. Once we have defined a structure using the METCAP layer, it will be released using a wet etching process based on a buffered HF solution previously reported [91]. Metal 2 layer will act as the bottom excitation electrode and METCAP (Titanium Nitride with a Young Modulus,  $E=600$  GPa [76]) will be the mobile structure. The main problem in order to use this novel approach is that MIM module design rules fix the minimum dimensions to  $4\text{ }\mu\text{m} \times 4\text{ }\mu\text{m}$  area. In order to make the releasing process easier, dummies structures with a minimum dimension of  $500\text{ nm}$  (figure 5.6 B) will be used as the mechanical movable structure. A METCAP dummy structure is placed besides a regular MIM capacitance that will act as the anchor of the cantilever movable switch, figure 5.6 C).

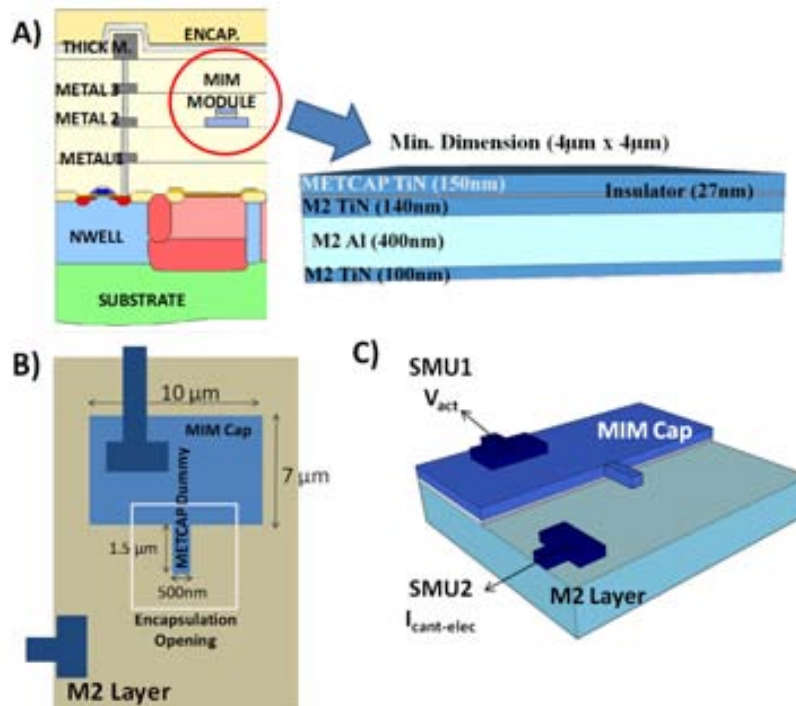


FIGURE 5.6: . A) MIM module schematic view. B) METCAP dummy element for implement NEMS cantilever. It can be observed how to release just the cantilever an opening in the encapsulation is defined above it (white square), preventing the releasing of the anchor. C) Electrical characterization SET-UP of the cantilever switch. SMU1 and 2 are the two Source-Measurement-Units corresponding to B1500A semiconductor analyzer used for the electrical characterization.

### 5.2.1 Devices design

Using this approach two terminals (2-T) out of plane switches have been developed, using two different structures: cantilever beams (figure 5.7) and semi-paddle structures (figure 5.8). It can be seen in figure 5.7 C) how the 27 nm gap has been obtained without any complex fabrication process, just taking advantage of the high performance that commercial CMOS technologies offer.

The semi-paddle structure has been designed in order to have three different states. The first one is the equilibrium position (state A in figure 5.8) when no voltage is applied and an air gap separates the structure and the electrode. In the second state (state B in figure 5.8) the tip of the switch makes contact as a consequence of the torsional movement produced in the paddle anchors. In the third state (state C in figure 5.8) the snap of the whole paddle structure is produced. In order to have these three states, it is important to have special careful on the paddle anchors design, in our particular case simple beams with  $l_a$ ,  $w_a$  and  $t_a$  dimensions.

Once the torsional pull-in has been produced the semi-paddle has a configuration in which one side is in contact with the electrode and the other side is supported by the anchors (Fig. 5.8 state B). If the contact resistance were low, ideally zero, it can be supposed that the semi-paddle and electrode would be at the same voltage, disappearing the electrostatic force. However, as the contact resistance is high (due to a small contact area) the voltage difference is kept and this second configuration can have a second pull-in, collapsing the whole semi-paddle structure. This behavior will depend on the value of the anchors spring constant. In order to have this two step pull-in processes, the voltage difference necessary to make pull-in of the whole structure in the out-of-plane mode, (state C in Fig. 5.8) has to be larger than the torsional pull-in (state B in Fig. 5.8).

The pull-in voltage due to torsional movement is given by the expression 5.2 [134]

$$V_{SNAP-TOR} = 0.6432k_o\beta^{-3/2} \quad (5.2)$$

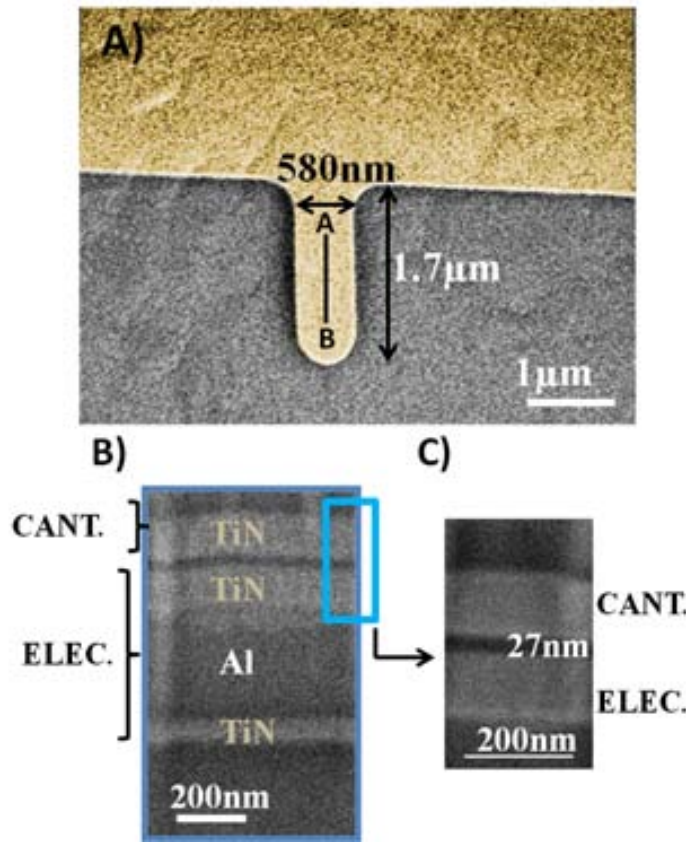


FIGURE 5.7: A) SEM Image of a cantilever Switch. (METCAP layer has been coloured for easy recognition). B) SEM Image of A-B FIB Cross section. C) Zoom to show the 27nm gap.

(in our particular case  $\beta=1$  because our actuation driver covers all the semi-paddle area).  $k_o$  is given by the expression 5.3 where  $S_o$  (equation 5.4) is the stiffness and  $I_p$  (equation 5.5) is the moment of inertia of a cross section beam whose width  $w_a$  is bigger than the thickness  $t$ ,  $s$  is the gap,  $\varepsilon$  is the permittivity of air ( $8.85 \cdot 10^{-12}$  F/m) and  $G$  is the TiN shear modulus ( $G=300$  GPa) [135]).

$$k_o = \left[ \frac{2S_o s^3}{\varepsilon L W^3} \right]^{1/2} \quad (5.3)$$

$$S_o = \frac{2GI_p}{l_a} \quad (5.4)$$

$$I_p = \left[ t^3 w_a \left( \frac{1}{3} - 0.21 \frac{t}{w_a} \left( 1 - \frac{t^4}{12w_a^4} \right) \right) \right] \quad (5.5)$$



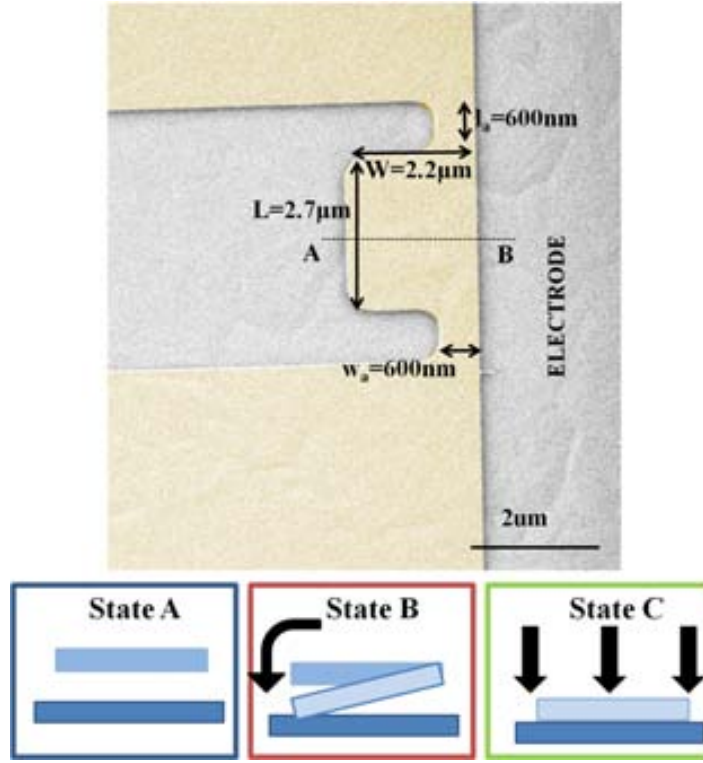


FIGURE 5.8: SEM Image of a Semi-Paddle Switch and a schematic of its operation modes at the cross section A-B defined in the SEM image: State A: without actuation voltage, State B: pull-in due to the torsional movement of the paddle anchors, State C: pull-in due to the flexural movement of the paddle anchors.

In order to calculate the pull-in value of configuration C (figure 5.8) some assumption will be taken to obtain a simple analytical expression. It will be assumed that the anchors act as two cantilevers connected in series ( $k_T = 2k_C$ , equation 5.7) , fixing the spring constant value in equation 5.6 [8] and the gap  $s=27$  nm constant along the structure despite the tilt. Moreover, as the angle between the structure and the electrode is small at contact ( $\Phi = \arcsin(s/W) = \arcsin(27 \cdot 10^{-9}/2, 2 \cdot 10^{-6}) = 0,7^\circ$ ) parallel plate capacitance will be assumed to calculate the coupling capacitance  $C_o$  (equation 5.8).  $E$  is the TiN Young modulus (600GPa [76]).

$$V_{SNAP\_VER} = \sqrt{\frac{8}{27} \frac{s^2 k_T}{C_o}} = \sqrt{\frac{4}{27} \frac{s^2 (2k_C)}{C_o}} \quad (5.6)$$

$$k_C = 0.25 E w_a \left( \frac{t_a}{l_a} \right)^3 \quad (5.7)$$

$$C_o = \frac{\varepsilon LW}{s} \quad (5.8)$$

In Figure 5.4 the two magnitudes are represented for a given coupling area ( $L=2.7$   $\mu\text{m}$  and  $W=2.2$   $\mu\text{m}$ ) supposing a 600 nm anchors width and their length is varied in order to get the value that satisfies this condition. As it is shown for length values shorter than (1.2  $\mu\text{m}$ ) a Tri-state switch can be obtained. In addition, it is interesting to highlight that the length of the anchors would fix the voltage difference between states.

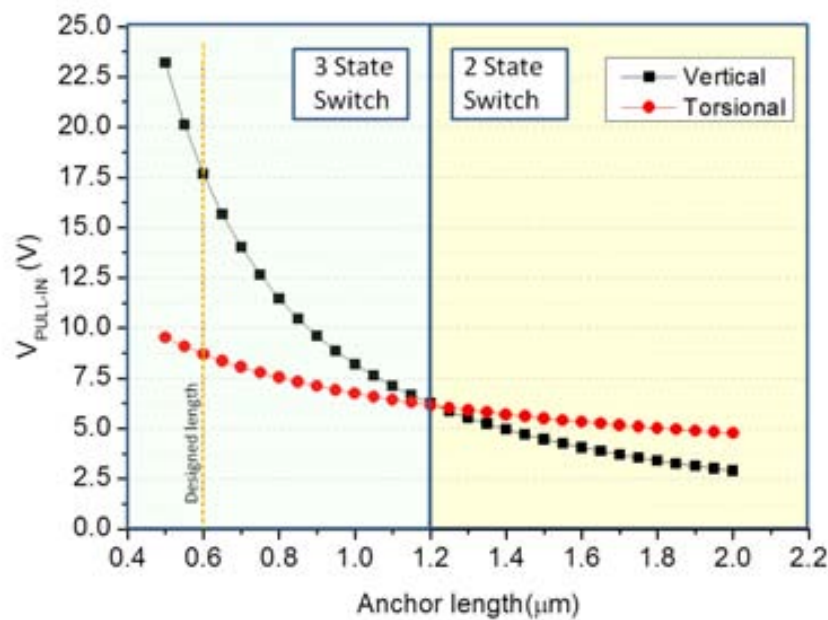


FIGURE 5.9: Analytical prediction of the pull-in voltages for 600 nm wide anchor. It can be observed how the voltage difference between states can be fixed choosing a given length

### 5.2.2 Electrical characterization

Once the chips were post-processed to release the structures, we carefully characterized the devices and measure the two-terminal switching behavior using a semiconductor Devices Analyzer (Agilent B1500A).



### 5.2.2.1 Cantilever switch

Cantilever beams with different lengths (2.5  $\mu\text{m}$ , 2.0  $\mu\text{m}$  and 1.5  $\mu\text{m}$ ) and the same width, 580 nm, were characterized, presenting the responses showed in figure 5.10. The pull-in events take places at 11,6 V, 16,7 V and 19 V (respectively) and the pull-out at 2 V, 4 V and 18 V approximately. Pull-in voltages increase as the beam length is reduced since the beam spring constant is higher. Thanks to this spring constant increase, higher pull-out values are obtained, since the elastic restoring forces are bigger and attractive forces like Van der Waals forces can be more easily overcome. Its hysteresis behavior makes these devices suitable for memory applications. The switches worked for a few cycle, remaining them stuck, as it is shown in figure 5.11.

In order to improve the reliability of the MIM switch an atomic layer deposition (ALD) was done [76] depositing 8 nm  $\text{Al}_2\text{O}_3$  oxide. Figure 5.12 shows its electrical characterization showing a lower pull-in voltage (compared with the same device without ALD). Moreover, a good  $I_{ON}/I_{OFF}$  ratio ( $10^4$ ) was obtained, where the  $I_{OFF}$  value is given by the experimental set-up and  $I_{ON}$  value is fixed by the semiconductor analyzer compliance and an additional resistance of 500 M $\Omega$  to avoid abrupt current peaks. Abrupt behavior (at least 5 mV/decade) during switch-on transition can be observed (see figure 5.12 inset). It was found that the reliability was improved, making the switch works for ten cycles, remaining then stuck (see 9th response in figure 5.12). It can also be appreciated, how the pull-in voltages are reduced as the number of operating cycles is increased. This effect could be explained by an accumulation of charges in the dielectric deposited by ALD [136] [137]. Charges can be stored in these layers, adding an electrostatic force that could reduce the initial gap, as it was observed in some devices (Figure 5.13) that presented lower pull-in values (5 V was the minimum value observed).

In table 5.1 a summary of the main attributes of the designed MIM switches is presented and compared with the state of the art of minimum dimensions top down switches. It can be observed how using a fabrication process based on a commercial CMOS technology similar features have been obtained in terms of

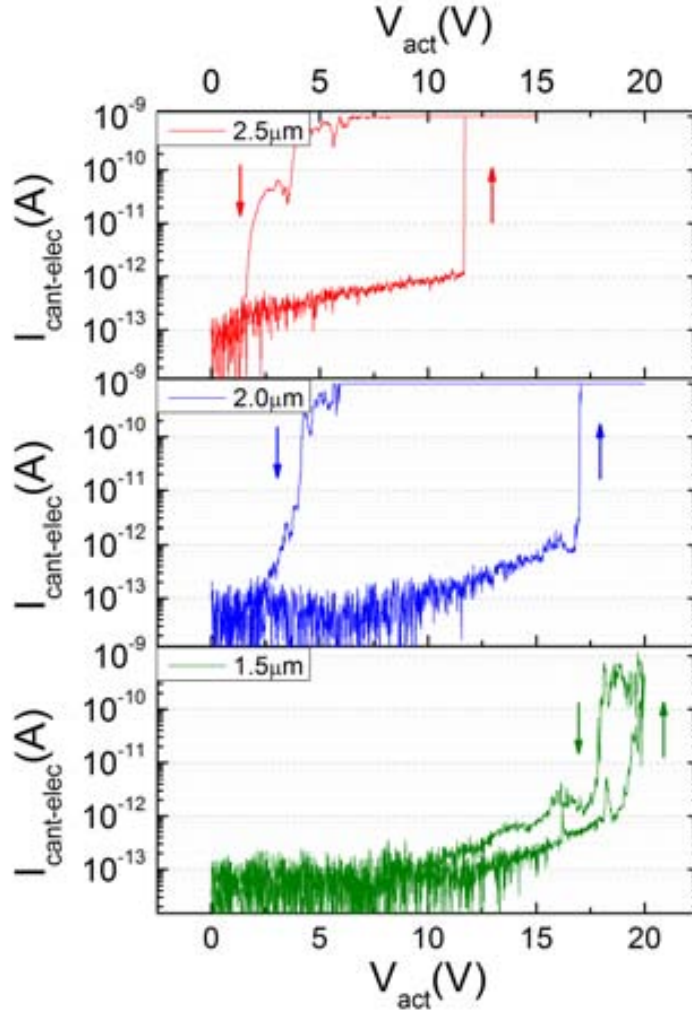


FIGURE 5.10: Electrical measurement for different cantilever lengths (width=580nm, thickness 120nm).

abrupt behavior (at least 5 mV/decade),  $I_{ON}/I_{OFF}$  ratio ( $10^4$ ) and low pull-in voltages (5 V) making our approach competitive with the state of the art switches.

### 5.2.2.2 Semi-paddle switch

Semi-Paddle switches electrical characterization with the two different pull-in events is presented in Fig. 5.14. The first pull-in, corresponding to the torsional mode, occurs at 10.7 V while the vertical pull-in takes place at 15 V. Both experimental voltages slightly differ from the theoretical values found in Fig. 5.9.

To our knowledge this is the first time that in a 2-T switch three different states are presented, making this device appropriate for three-state logic in digital circuits as

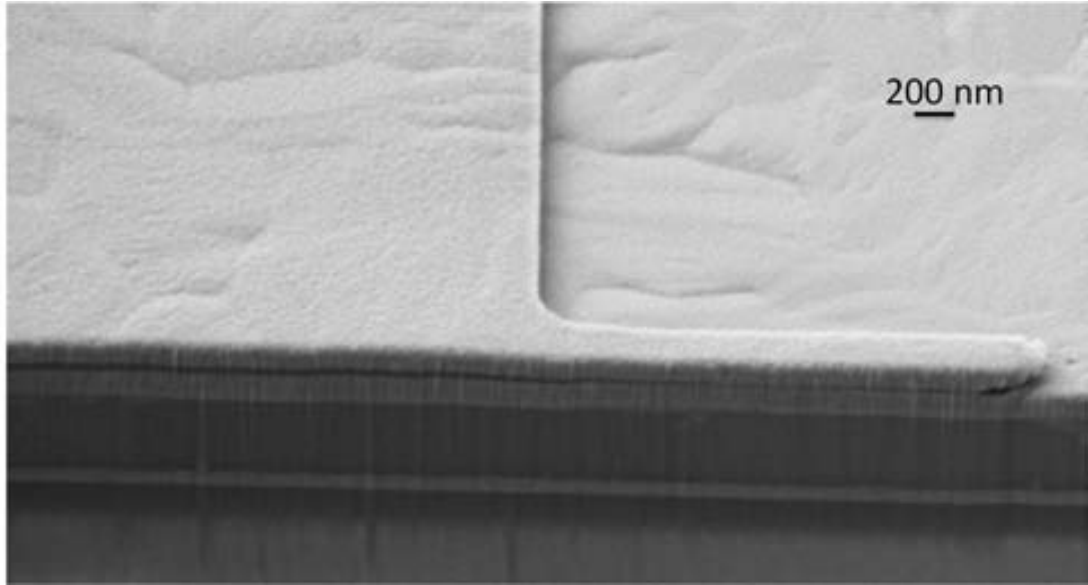


FIGURE 5.11: Cross section SEM image of a released and stuck 2  $\mu\text{m}$  cantilever after a FIB cut.

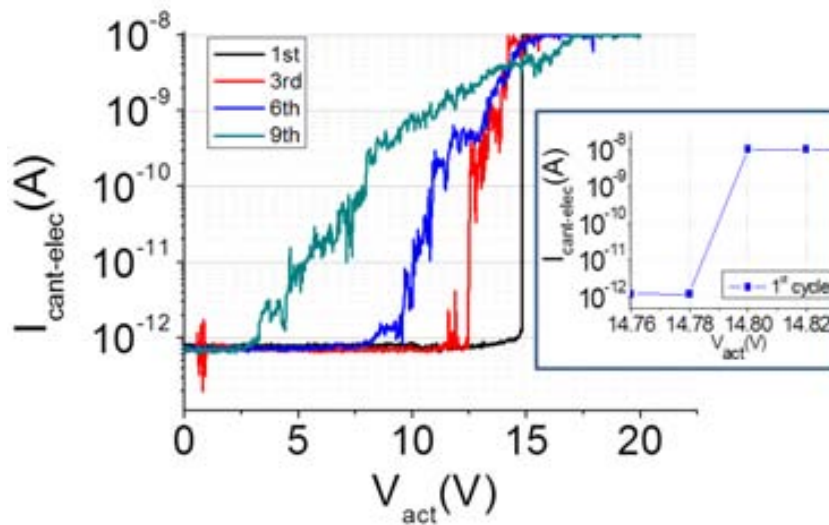


FIGURE 5.12: Electrical measurement after ALD (1.5  $\mu\text{m}$  length and 580 nm width) (Just the sweep-up cycles are represented).

registers, bus drivers and flip-flops. It shows a high impedance state when it is not making contact with the electrode and two different states (torsional or flexural) depending on the voltage applied between the structure and driver. Therefore, using this switch the number of bits could be reduced in memory and logic applications, as 3 different states are obtained just applying one voltage difference (actuation voltage), in contrast to common memories where two different bits (voltages) are necessary in order to obtain 3 different states (00,01,10).

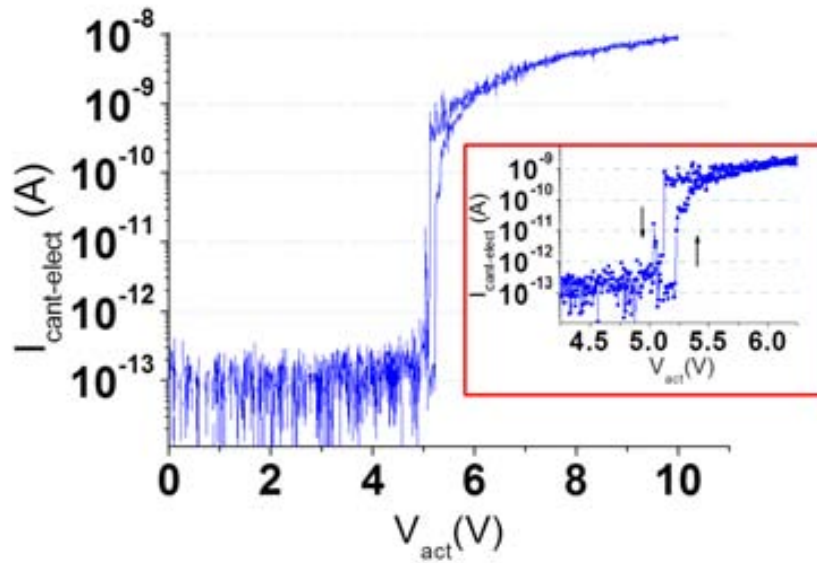


FIGURE 5.13: Cantilever switch ( $1.5\mu\text{m}$  length and  $580\text{nm}$  width) electrical characterization after ALD process ( $8\text{ nm } \text{Al}_2\text{O}_3$  oxide). The variation in the pull-in and pull-out voltages respect other measured designs is attributed to charge accumulation on the dielectric.

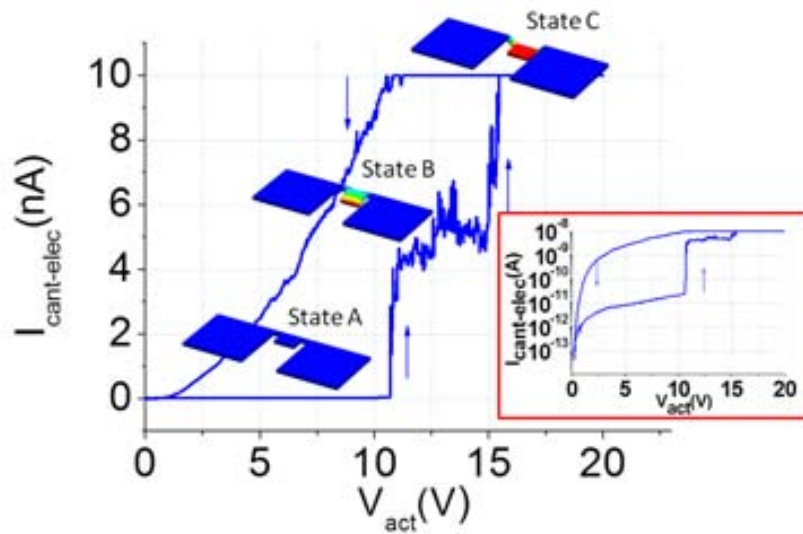


FIGURE 5.14: Semi-paddle switch electrical characterization where two different pull-in events can be observed. For each state, finite element simulation is shown.

Material	length (l) gap (s)	$V_{PI}$	$I_{ON}/I_{OFF}$	mV/decade	CMOS
SiC [49]	l=6–20 $\mu\text{m}$ s=27–90 nm	1–8 V	$10^3$		NO
TiW/W [48]	l=1.5 $\mu\text{m}$ s=4 nm	0.4 V	$10^6$	10	Suited for NEMS–CMOS hybrid I.C.
Pt [74]	l=3.5 $\mu\text{m}$ s=100 nm	4.3 V	$10^4$	0.8	NEMS on CMOS
TiN [76]	l=0.3 $\mu\text{m}$ s=15 nm	14 V	$10^5$	3	CMOS compatible
TiN [This work]	l=2.5–1.5 $\mu\text{m}$ s=27 nm	5 V	$10^4$	5*	Monolithically integrated / MIM configuration

TABLE 5.1: Top down switches state of the art. Special attention has been taken to those works that try to minimize switches area and co-integrate them with CMOS (\* limit of the experimental set-up).

### 5.3 ST 65nm M1 switches

In this section the electrical characterization of the electromechanical switches developed using ST 65nm technology will be shown.

In figure 5.15, the SEM image of a 2–T switch developed using Metal 1 is presented. In order to be able to define the smallest gap (90 nm) the driver is anchored using M2 layer (as it was shown in section 4.5.3).

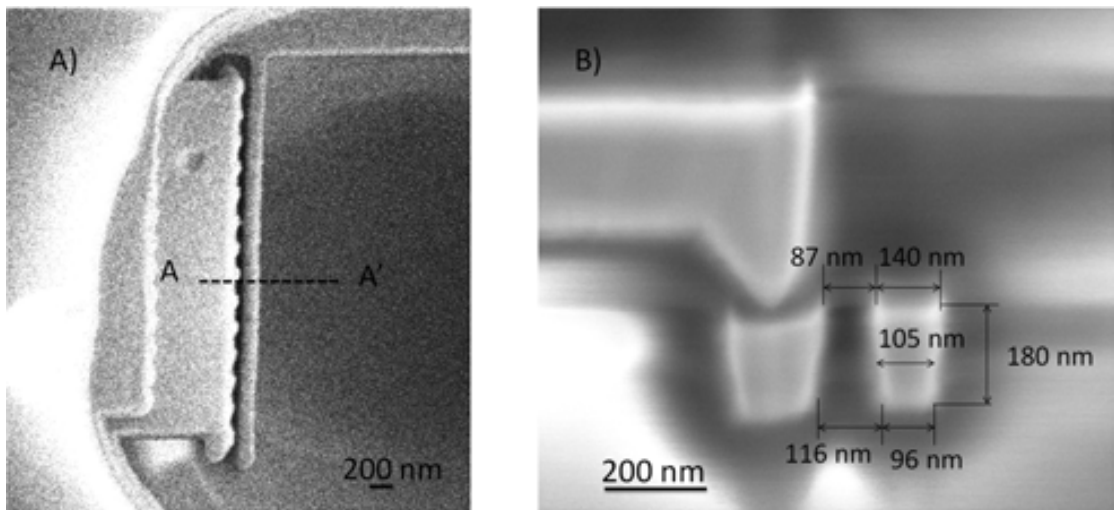


FIGURE 5.15: A) Released 2-T M1 switch (l=3.5  $\mu\text{m}$ , w=100 nm, s=90nm, defined on layout.) B) SEM image of a FIB cut before the releasing process.

Again, it can be observed in the FIB cut (figure 5.15 B)) how the beam presents a trapezoidal cross section. This fact will have to be taken into account in order to determine its snap-in voltage. The moment of inertia for a trapezoidal cross section beam is given by expression [8] :

$$I = \frac{1}{48}(b_1 + b_2)(b_1^2 + b_2^2)t \quad (5.9)$$

where  $b_1, b_2$  are the width of the top and bottom side and  $t$  is the thickness of the beam. Therefore the spring constant of the cantilever can be calculated using equation 2.20:

$$k = \frac{3EI}{l^3} = \frac{3E}{l^3} \frac{1}{48}(b_1 + b_2)(b_1^2 + b_2^2)t \quad (5.10)$$

In our particular case ( $b_1=140$  nm,  $b_2= 96$  nm,  $l= 3.5$   $\mu$ m,  $t=180$  nm and  $E=117$  GPa) the spring constant has a value of 0.20 N/m, almost twice the value of the spring constant supposing a square cross section with a width of 100 nm (0.122 N/m). Additionally the gap is not constant along the beam thickness. It has a minimum value of 87 nm in the top side and 116 nm at the bottom. So an upper and lower bounds can be fixed for the pull-in voltage using these values and equation 3.12:

$$V_{PI} = \begin{cases} s = 87nm \rightarrow V_{PI} = 4.71V \\ s = 116nm \rightarrow V_{PI} = 7.29V \end{cases} \quad (5.11)$$

So, theoretically the beam should collapse with the electrode when the voltage difference reach a value ranged from 4.71 V to 7.29 V. Next, the 2-T switches were characterized using the parametric semiconductor analyzer B1500A from Agilent (as, in the previous sections). A voltage sweep is applied on the electrode, the beam is polarized to a fixed voltage (GND) and the current is measured in the two terminals. In addition a 25  $M\Omega$  resistance was connected in series with the

cantilever to prevent its damage during hot switching. Figure 5.16 shows its electrical response.

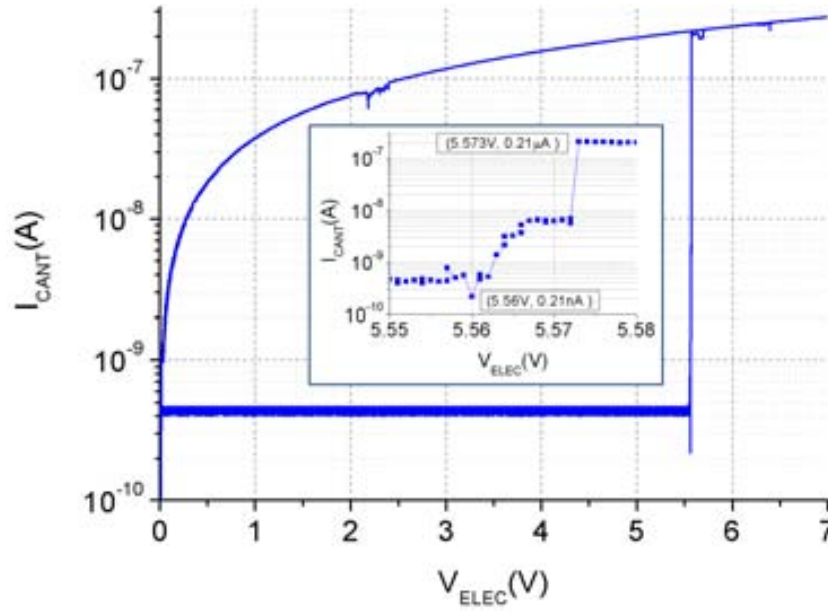


FIGURE 5.16: Switch electrical response with a protection resistance of 25 MΩ.

Snap-in event takes place at 5.5 V, inside the theoretical range previously fixed, an  $I_{ON}/I_{OFF}$  ratio of  $1 \cdot 10^3$  was measured with a subthreshold swing of 4.3 mV/decade, beating again the MOSFET limit. However the switch just worked for one cycle remaining then stuck. It could be irreversibly damaged by microwelding. The maximum current that M1 stands (specified by the technology design rules) is 90 nA for a minimum width (90 nm) metal line. In the ON state the current that runs through the M1 layer is bigger than 100 nA (see figure 5.16), exceeding the current limit. To protect the device of high current the value of the protection resistance was increased to 500 MΩ ( $I_{limit}=5/500 \text{ M}\Omega=0.01 \text{ }\mu\text{A}=10 \text{ nA}$ ). The electrical characterization of a new devices using this protection resistance is showed in figure 5.17:

In figure A) the first working cycle is represented. The snap-in event takes place at 6.5 V. A  $I_{ON}/I_{OFF}$  ratio of  $10^2$  and abrupt transition around 10 mV/decade between the ON and the OFF state is also demonstrated. Note how the subthreshold swing is reduced due to a lower value of  $I_{ON}$  current, that at the same time, improves the reliability of the device avoiding melting. In Fig B its response for



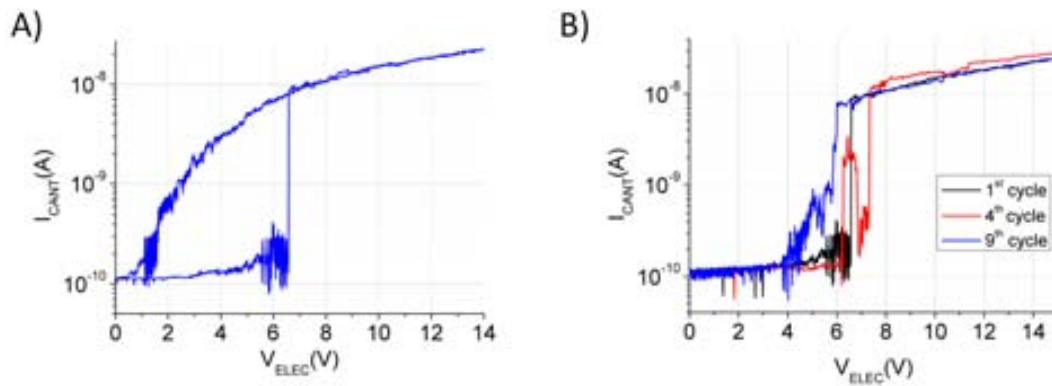


FIGURE 5.17: A) Switch electrical response. B) Switch electrical characterization in different successive cycles.

different cycles is represented, showing how the snap-in event varies slightly in the different cycles and its response degrades a bit as long as the cycles are performed. In ambient conditions, the copper oxides [138] degrading the operation of the switch in two different aspect:

- Charges can be trapped on the native oxide formed in its surface modifying its snap-in voltage [137].
- Native oxide will increase the contact resistance value and will make it more unstable.

In order to improve the device features, hermetic sealing packaged could be used [139] or the devices could be coated with an additional layer that will be used as contact material. Ruthenium [36], is a good candidate as it forms conductive oxide ( $RuO_2$ ) in air, and its hardness is high.

## 5.4 Conclusions

In this chapter successful integration of microelectromechanical switches in commercial CMOS technology has been shown, improving the subthreshold swing that switches based on transistors presents, relieving power consumption problem.



Switches designed in the back end metal layers of a standard CMOS technology have been fabricated and electrical characterized. M4 switches based on Al present a snap-in voltage around 20 V, with two decades  $I_{ON}/I_{OFF}$  ratio and 24 mV/decade slope. The stack configuration based on Al/TiN/W has shown bigger  $I_{ON}/I_{OFF}$  ratios ( $1 \cdot 10^3$ ) with smaller subthreshold slopes (5mV/decade). Both configuration switches have been ramped for several decades with almost non-functional degradation. From the presented results we can conclude that metal BEOL layers of the CMOS technology are promising candidates to develop MEMS switches with, good reliability and easy and reproducible fabrication process.

Respect switches based on the MIM capacitive module, the small dimensions of the structures (length 1.5  $\mu\text{m}$ , 580nm width and 27nm gap) ensure a high integration density and consequently a cost reduction. MIM switches presented the lowest snap-in value (see table 5.2) of the CMOS–MEMS switches developed in this thesis, thanks to its small gap (27 nm). Although lower pull-in voltages have been reported using top-down approaches (table 3.3, 3.4) they are not totally CMOS fabricated as our approach, which requires only one additional post-processing step to release the structures. Moreover, the switches present abrupt behavior and a good  $I_{ON}/I_{OFF}$  ratio. Further efforts are need in order to improve the reliability. In addition we have presented a 2-Terminal 3 states switch with promising applications in memory and logic applications.

Copper NEMS switches developed in ST 65 nm CMOS technology presented the most abrupt subthreshold swing (4.3 mV/decade) and a good  $I_{ON}/I_{OFF}$  ratio ( $10^3$ ). The devices, as the developed in AMS 0.35  $\mu\text{m}$  worked for a few decades.

In table 5.2 all the properties of the switches developed in this thesis are summarized.






Material	Device	Structure Description	Dimensions	Pull-in Voltage	$I_{ON}/I_{OFF}$	mV/decade	Reliability
TiN		2-T cantilever	l=1.5 $\mu\text{m}$ , t=150 nm, w=580 nm, s=27 nm, A=0.58 $\mu\text{m}^2$	5 V	$10^4$	5*	10 cycle
Copper		2-Terminal Cantilever	l=3.5 $\mu\text{m}$ , w=100 nm, t=180 nm, s=90 nm, A=0.63 $\mu\text{m}^2$	5.5 V	$10^3$	4.3	20 cycles
TiN		3 State 2-Terminal device	l=2.7 $\mu\text{m}$ , w= 2.2 $\mu\text{m}$ , $l_a = 600\text{nm}$ , $w_a = 600\text{nm}$ , s=27 nm, A= 5.94 $\mu\text{m}^2$	10.7 V 15 V	$10^2$	20	1 cycle
Al, TiN		C.C.Beam 3-Terminal	l=19 $\mu\text{m}$ , w=600nm, t=850nm, s=460nm, A=16.15 $\mu\text{m}^2$	18.8 V	$3 \cdot 10^2$	24	20 cycles
Al, Oxide, TiN, W Stack		C.C. Beam 3-Terminal	l=30 $\mu\text{m}$ w=1.5 $\mu\text{m}$ , t=2.39 $\mu\text{m}$ , s=500 nm, A=71.7 $\mu\text{m}^2$	51 V	$10^3$	5	20 cycle

TABLE 5.2: Summary of the CMOS-N/MEMS switches sorted by increasing pull-in voltages (\* limit of the experimental set-up).

# Chapter 6

## Resonant gate transistor

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*Resonant Gate Transistor (RGT) has emerged as a smart and alternative solution to detect the movement of small structures that produce low level output signal under capacitive read-out. This chapter starts with a brief introduction to the resonant gate transistor configuration followed by its state of the art. Next a theoretical model will be developed using the spring-mass lumped model in order to simulate the MEMS movement and the EKV model to obtain the transistor response. Finally a RGT device will be developed using a commercial CMOS technology (AMS 0.35  $\mu\text{m}$ ). It will be characterized as resonator and mechanical switch.*

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### 6.1 Introduction

The miniaturization of MEMS devices to the nano scale (NEMS) has allowed the emergence of flexural mechanical resonator operating in the very high frequency range (VHF) [122] [140] [141], bulk resonators operating at GHz frequencies with

high quality factors [142] [143], development of high sensitivity sensor [17] [4] and the definition of low voltage operating switches [56] [48]. For these reasons, N/MEMS have positioned as a emerging technology in RF front-end modules, sensors and memory and logic applications [1].

In order to induce movement on the devices and detect it, electrostatic actuation and capacitive read-out are widely used due to its simple principle, fabrication and implementation. However, as the dimensions are reduced stiffer resonators are obtained and as a consequence smaller displacement is produced, making more difficult to detect its motion if gaps between the structures and drivers can not further be reduced, normally limited by technology. Lower output signal are produced, higher DC voltages are needed to excite movement and a higher motional resistance is obtained (in the  $M\Omega$  range). In order to overcome this problem read-out schemes based on piezoresistive [143], piezoelectric [31], magnetomotive [144] and high-K materials have been used [145]. However a successful detection is got at an expense of higher power consumption, difficult measurement set-up, the use of not CMOS compatible materials and complex fabrication processes, respectively.

As an alternative to these transduction methods, some solutions have emerged based on the idea of modulate the charge on a transistor by the movement of a mechanical structure. The variation of the position of a structure biased to a fixed potential is equivalent to change the value of the potential in the fixed gate of a common transistor. It was first proposed by Nathanson in 1967 [32] (figure 6.1), in fact some authors consider its work as the born of MEMS, as for the first time mechanical and electrical domains were combined in a single operating device.

In its device configuration a metal beam electrode, clamped on one end to an insulating oxide, is fabricated parallel to and suspended over the surface of a silicon slice. Underneath the tip of the beam there is an insulated input force plate. Voltages applied to this plate exert electrostatic forces on the beam electrode causing it to vibrate. Only at the mechanical resonance frequency of the beam the vibration is appreciable. Vibrations of the beam are detected as variations of field effect inducing charge modulation in the channel region of a normally ON MOS

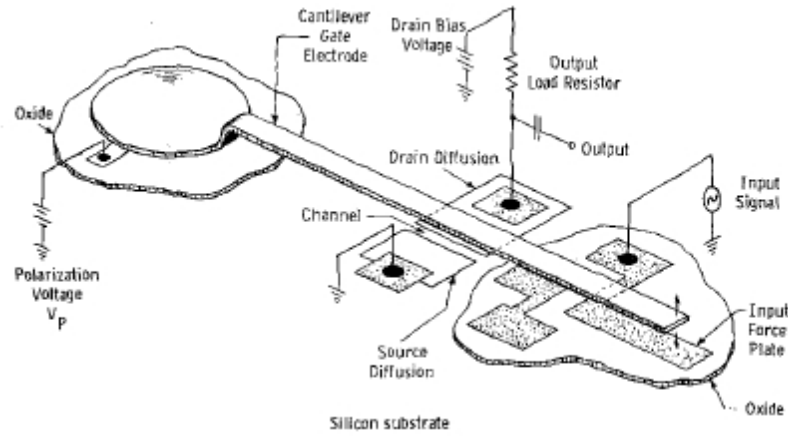


FIGURE 6.1: Nathanson resonant gate device. Image extracted from [32].

transistor underneath the middle of the beam. An output voltage amplified by the transistor gain is extracted at the drain of the device. It is this amplification effect that makes RGT attractive in NEMS sensing. As it is known, the transistor output current increases with the reciprocal of the beam width, i.e. the MOSFET drain current is higher for a smaller channel length, due to the MOS amplification effect. Just the opposite effect is observed using a capacitive readout when the dimensions of the beam are reduced, lower coupling area are obtained and as a consequence lower output current are produced (see figure 6.2).

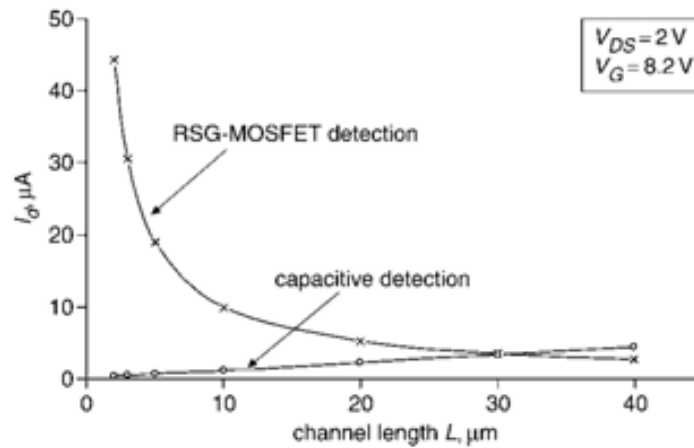


FIGURE 6.2: Comparison of simulated peak current associated with capacitive and MOSFET detections for various beam widths. Image extracted from [146]



Insulator (SOI) technology using the upper silicon layer as structural layer and defining gaps using E-beam lithography [149]. Transistor and beam are built in the same layer. The transistor is defined with an implantation of phosphorous to define gate, source and gate. The gate resonates in plane with the channel (in the same horizontal plane)(Figure 6.3 B)).

Respect the transistor types, partially depleted SOI [147] and enhancement mode transistor [148] [149] have been used, although it has been found that during the RGT implementation charges trapped on the oxide varies its original behavior [149].

- Resonant Channel/Body Transistor

A different approach is to define the channel on the resonant structure as it is shown in figure 6.4. Numerous works has appeared using this read out scheme ([150],[151] [33]) and although the channel is defined on the beam in all of them, different working principle are used. If the active area on the structure does not present a high stress while it is resonating (figure 6.4 A)) the channel is modulated by the proximity to the gate, as in the previous section [150]. However, if the active area is stressed at movement not only the modulation of charge is exploited, the silicon resistance is also modulated [151] (figure 6.4 B)). The contribution of these two effects will depend on the dimensions of the structure. Additionally, active areas has been defined on small bulk resonators [33]. In this configurations the elastic waves produces on the structure modulate the output current changing the carrier mobility by piezoresistive modulation [100] [33] (figure 6.4 C)).

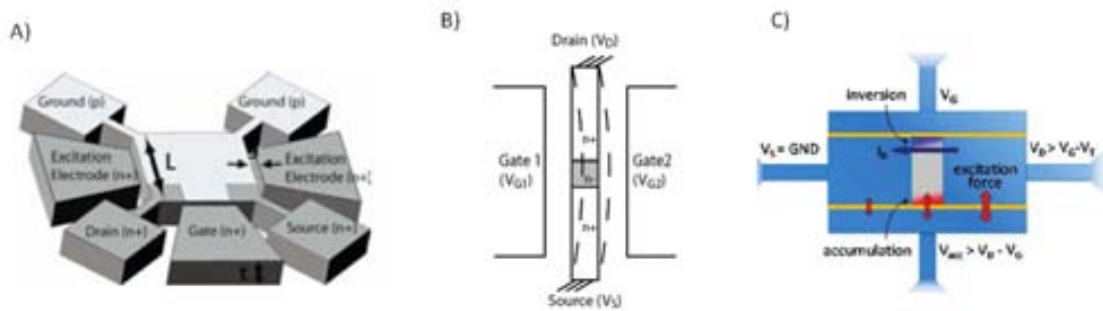


FIGURE 6.4: Resonant body transistor configurations extracted from [150],[151] [33], respectively.

Although it is not a transduction method properly based on a transistor, it is worthy to mention read-out and actuation schemes based on P-N junction [152] [153] [154], whose operating principle is similar to the resonant gate: the modulation of the current in the P-N junction is produced by the variation of an electric field induced by a resonant beam.

In table 6.1, the most representative works of the different approaches mentioned before are shown.

All these devices can also be divided into two different groups depending on the coupling between excitation and readout schemes:

- approaches that decouple the excitation and readout [32][33][150][151][155]. Based on Nathanson original configuration an electrode is used to excite the movement on the beam but the polarization of the transistor that detect the movement can be fixed independently.
- approaches whose electrostatic force is produce by the charges in the channel and the polarization of the beam [147][148]. So the DC voltage applied to the beam fixed the electrostatic force and the state of the transistor.

Once all the different approaches have been shown, we will focus on the out of plane resonant gate transistor configuration (first approach) because its fabrication process is more easily reproduced on CMOS-MEMS. The impossibility of having different dopant concentration in a same layer using maskless post-CMOS process makes the second configuration not suitable to our approach.



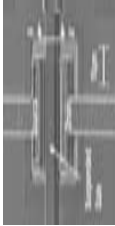


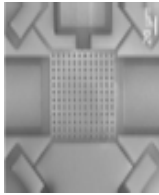


Approach (Year)	Device	Operation principle	Material	Dimensions length (l), width (w), thickness (t), gap (g)	$f_o$	Q (Vacuum)	Operating Voltage
Gate resonating (out of plane) (2006) [147]		Position of the gate modulates the charges in the channel	Aluminum Silicon alloy (1%)	l=34-10 $\mu\text{m}$ , w=6-8 $\mu\text{m}$ , t=1.9 $\mu\text{m}$ , g=300nm	16-91 MHz	641	$V_{DC}=0.61-1\text{ V}$ $V_{AC}=200\text{mV}$
Double gate: one at resonance (out of plane) the other floating (2013) [148]		Position of gate at resonance modulates the charges in the channel	Stack of Alu- minum and $\text{SiO}_2$	g=175nm	3.72 MHz	1700	$V_{DC}=41\text{V}$ $V_{AC}=-38\text{dBm}$
Gate resonating (In plane) (2008) [155]		Position of the gate modulates the charges in the channel	Silicon	l=16.1 $\mu\text{m}$ , w=490nm, t=200nm, g=107nm	14.5 MHz	700	$V_{DC}=10\text{ V}$ , $V_{AC}=-41\text{dBm}$
Channel resonating (in plane) (2007) [150]		Position of the gate modulates the charges in the channel	Silicon	D1 l=30 $\mu\text{m}$ w=1.7 $\mu\text{m}$ t=1.35 $\mu\text{m}$ g=100nm D2 (Bulk) l=90 $\mu\text{m}$ w=90 $\mu\text{m}$	D1 13MHz D2 32MHz	D2 4000	$V_{DC}=30\text{V}$ , $V_{AC}=0\text{dBm}$
Channel resonating (in plane) (2008) [151]		Exploits accumula- tion/inversion channel charge and piezoresis- itivity modulation	Silicon	D1 l=100 $\mu\text{m}$ , w=3 $\mu\text{m}$ , t=1.25 $\mu\text{m}$ $\mu\text{m}$ , s=200nm D2 (Bulk) l=50 $\mu\text{m}$ , w=50 $\mu\text{m}$	D1 2.3MHz D2 71MHz	D1 6970 D2 15400	D1 12V D2 40V
Channel resonating (Bulk) (2010) [100] [33]		Mobility of charges at channel are modulated by acoustic waves	Silicon	l=1.1 $\mu\text{m}$ w=500nm s=15nm (Bulk)	11.76 GHz	1831	$V_{DC}=5\text{V}$ $V_{AC}=0.5\text{V}$

TABLE 6.1: Resonant Gate Transistor State of the Art

### 6.3 RGT theoretical model

The resonant gate transistor fundamental schematic model for a standard CMOS technology is showed in figure 6.5:

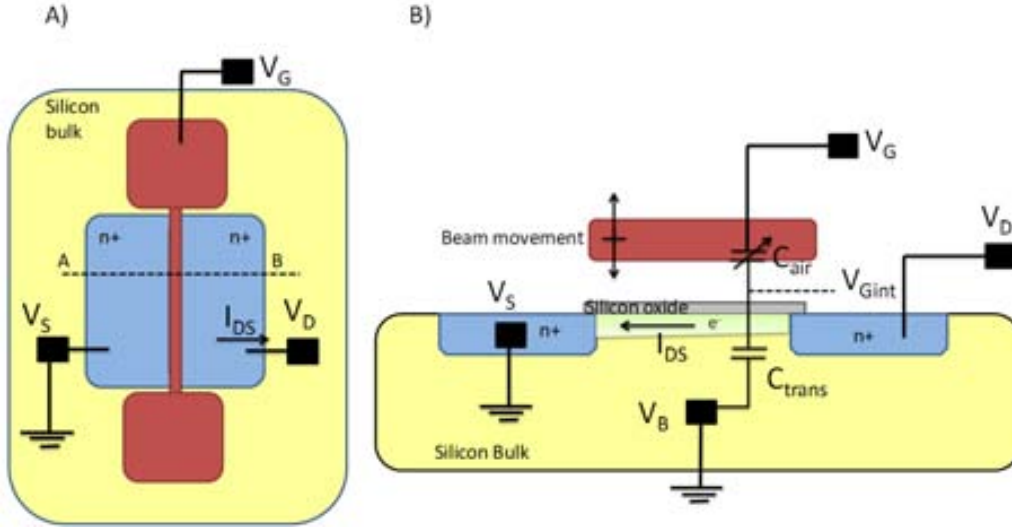


FIGURE 6.5: A) Top view of a Resonant Gate Transistor based on an polysilicon C.C. Beam configuration. B) A-B RGT Cross section

This RGT-CMOS approach is composed of a polysilicon beam defined parallel to a silicon substrate area where a transistor has been defined. The polysilicon, that is used as structural material, is at the same time the gate of a transistor whose dielectric is composed of an air gap and silicon oxide, as it can be observed in figure 6.5 B).

When a voltage  $V_G$  is applied to the gate, it is tuned according to a capacitor divider (see equation 6.1 and figure 6.6 A)) formed by the air gap and the transistor intrinsic capacitance. In this way, the effective voltage operating in the transistor is  $V_{Gint}$ :

$$V_{Gint} = \frac{V_G}{1 + \frac{C_{trans}}{C_{air}}} \quad (6.1)$$

where  $C_{air}$  is the air gap capacitance and  $C_{trans}$  is the intrinsic capacitance of the transistor (whose value depend on the intrinsic voltage  $V_{Gint}$ ). As it will be shown in section 6.5,  $C_{trans}$  acts like a series combination of a fixed, voltage-independent

gate oxide capacitance ( $C_{ox}$ ), and a voltage-dependent semiconductor capacitance (mainly due by the depletion region), such that the overall CMOS capacitance becomes voltage dependent, see figure 6.6.

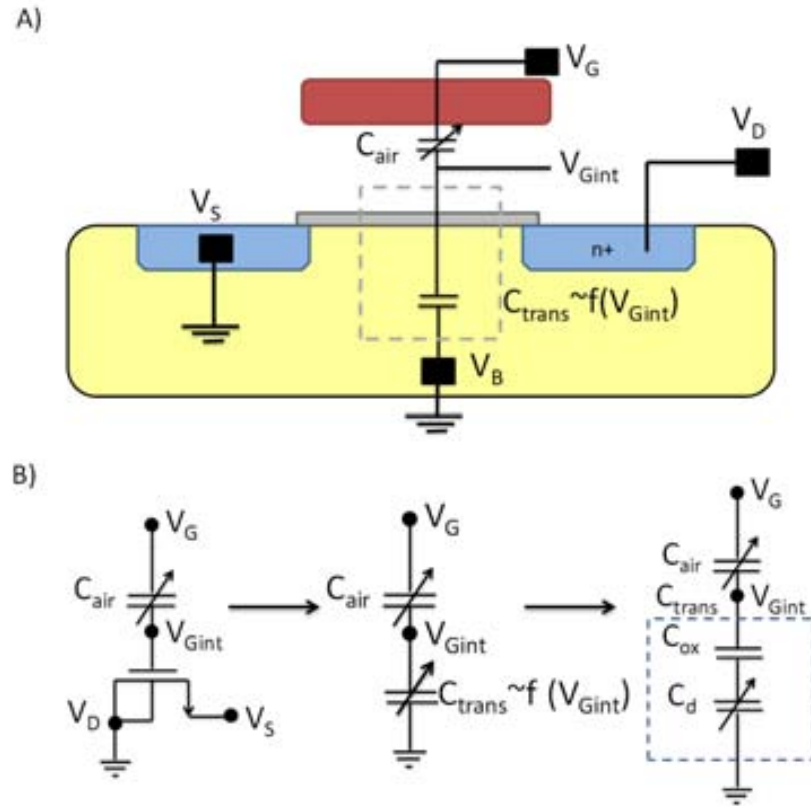


FIGURE 6.6: A) Schematic of the capacitor voltage divider composed of the air gap ( $C_{air}$ ) capacitance and the intrinsic capacitances of the transistor ( $C_{trans}$ ). B) simplified electrical equivalent schematic.

The  $V_{Gint}$  voltage has the same effect on this configuration as the gate voltage in a common transistor (see figure 6.6 B)). As  $V_{Gint}$  is increased inversion charge layer will be formed and a channel between the source and drain terminals will be created for high enough voltages ( $V_{Gint} > V_{TO}$  being  $V_{TO}$  the threshold voltage). At the same time the voltage difference on the beam ( $V_G - V_{Gint}$ ) will form an electric field that will tend to displace the beam to the transistor surface varying the air gap, see figure 6.7 A). As a consequence of this movement, the air gap will be reduced, the air gap capacitance will be increased and  $V_{Gint}$  will have a higher value (see equation 6.1). That will be translated into a bigger amount of charges in the inversion charge and hence a bigger drain current. When the electrostatic force due to the voltage difference  $V_G - V_{Gint}$  is bigger than the elastic recovering

forces, the pull-in phenomenon will take place, and the beam will collapse with the gate oxide (see figure 6.7 B)). When it is produced  $V_G = V_{Gint}$  and an abrupt change on the drain current will be measured. In this way, it has been proved, how the movement of the structure can be detected with this configuration measuring the current at the output.

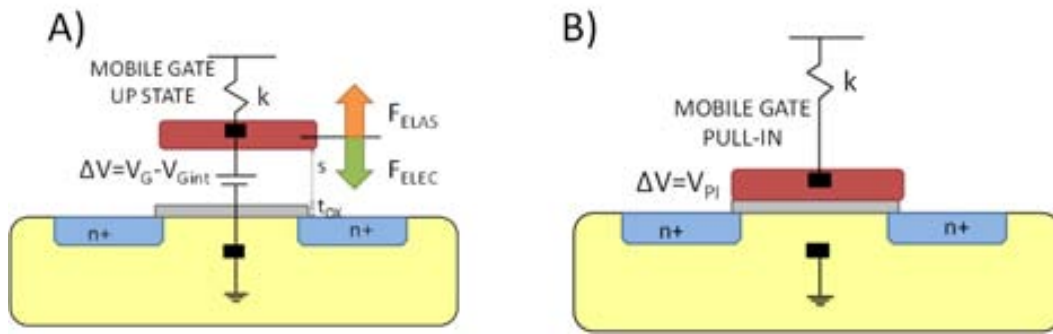


FIGURE 6.7: Schematic of the RSG-MOSFET in the up-state (A) and pulled-in (B)

Moreover, this configuration can be used to detect a dynamic movement of the beam as well. If an AC signal is applied to the gate (plus a  $V_{DC}$  voltage that fixes the polarization point and hence the inversion channel) the charges at the channel can be seen as an electrode, the variation on the electric field between them will induce a movement on the structure. As it has been shown before, this movement on the structure will produce a variation on the current at the drain. The value of this variation will depend on the operation region of the transistor ( $V_{DC}$ ). As it can be expected on weak inversion lower current values will be obtained but the movement of the beam will produce a big current variation respect the current fixed by the DC value (note that in weak inversion the drain current has an exponential behavior). In strong inversion higher currents will be obtained but smaller current variation will be produced by the beam movement (more details will be given in section 6.3.4). In this way the resonant gate transistor will provided an amplified signal current proportional to its transconductance gain multiplied by the beam position. Measuring the drain current, the displacement of the beam can be detected again.

As it can be seen, there is a clear coupling between the mechanical domain, position of the beam, and the electrical domain, that will fix the electrostatic force with the structure and the read-out current. It will be necessary to develop a model for the transistor (in all its regions of operation) and another for the beam position. They need to be related, as the voltage difference between resonator and the intrinsic voltage at the transistor will fix the beam position, and the beam position will fix the operation region of the transistor and the obtained output current. These models will be presented in the next section, along with an electrical model in order to simulate its frequency response.

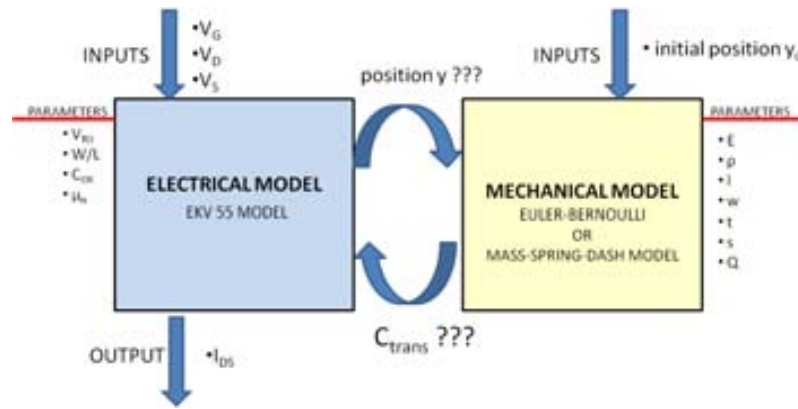


FIGURE 6.8: Schematic of the coupling between the mechanical and electrical domain coupling in a RGT simulation.

### 6.3.1 MOSFET Model

In order to simulate the transistor response the EKV model has been used [156] [157]. It provides a fully analytical MOS transistor model whose expressions are continuous in all the regions of operation. In this way the current through the transistor and its equivalent capacitance could be determined.

Note that this model is for a standard MOS transistor so there is no air gap ( $C_{air} = 0$ ) and  $V_G = V_{Gint}$ .

The drain to source current is calculated on the pinch-off voltage  $V_P$  (difference between the quasi-Fermi potential of the carriers forming the channel ( $\phi_n$ ) and the quasi-Fermi potential of the majority carriers ( $\phi_p$ ) that becomes the inversion

charge zero for a given gate voltage (defined in equation 6.7)) and drain  $V_D$  and source  $V_S$  polarization.

$$I_{DS} = I_F - I_R \quad (6.2)$$

$$I_F = I_S \left[ \ln \left( 1 + \exp \left( \frac{V_P - V_S}{2U_T} \right) \right) \right]^2 \quad (6.3)$$

$$I_R = I_S \left[ \ln \left( 1 + \exp \left( \frac{V_P - V_D}{2U_T} \right) \right) \right]^2 \quad (6.4)$$

$U_T$  is the thermodynamic voltage  $U_T = k_B T / q$ ,  $I_S$  is a normalization factor called specific current and it depends essentially on the  $W/L$  of the device, the carriers mobility  $\mu_n$  and the oxide capacitance  $C_{ox}$  as it can be observed on 6.5. The pinch-off voltage can be directly related to the gate voltage  $V_G$  using the expressions 6.6 and 6.7.

$$I_S = 2n\mu_n C_{ox} \frac{W}{L} U_T^2 \quad (6.5)$$

$$V'_G = V_G - V_{TO} + PHI + GAMMA \cdot \sqrt{PHI} \quad (6.6)$$

$$V_P = V'_G - PHI - \gamma' \left[ \sqrt{V'_G + \left( \frac{\gamma'}{2} \right)^2} \right] - \frac{\gamma'}{2} \quad (6.7)$$

where the parameter GAMMA is the body effect factor (equation 6.8) and the parameter PHI is the approximation of the surface potential in strong inversion (equation 6.9).  $V_{TO}$  is the threshold voltage (6.10)

$$GAMMA = \frac{\sqrt{2qN_{sub}\epsilon_{Si}}}{C_{ox}} \quad (6.8)$$

$$PHI = 2\phi_F = 2\frac{KT}{q}\ln\left(\frac{N_{sub}}{n_i}\right) \quad (6.9)$$

$$V_{TO} = V_{FB} + PHI + GAMMA\sqrt{PHI} \quad (6.10)$$

$$V_{FB} = \Phi - \frac{Q_{ox}}{C_{ox}} \quad (6.11)$$

where  $N_{sub}$  is the doping concentration of substrate,  $V_{FB}$  is the flat-band voltage, that depends on the work function of the polysilicon ( $\Phi$ ) and the charges trapped ( $Q_{ox}$ ) on the gate oxide capacitance ( $C_{ox} = \epsilon_r\epsilon_o/t_{ox}$ ).

The corrected body effect factor  $\gamma'$  accounts for small geometry effects. For large devices geometries it can be assumed  $\gamma' = GAMMA$ .

The weak inversion slope factor  $n$  is defined as the inverse of the partial derivative of the pinch-off voltage with respect to the gate voltage:

$$n = \frac{dV_G}{dV_P} = 1 + \frac{GAMMA}{2\sqrt{V_P + PHI}} \quad (6.12)$$

The EKV model also provide a model for the intrinsic capacitances assuming quasi-static operation and medium frequency operation (figure 6.9 A)) that will be used to obtain  $C_{tans}$  value. In figure 6.9  $g_{mg}$ ,  $g_{ms}$ ,  $g_{md}$  are respectively the gate, source and drain transconductances (see equations 6.13) and the gate to bulk ( $C_{gb}$ ), gate to source ( $C_{gs}$ ), gate to drain ( $C_{gd}$ ), bulk to source ( $C_{bs}$ ) and bulk to drain ( $C_{bd}$ ) capacitances.

$$g_{mg} = \left| \frac{\partial I_{DS}}{\partial V_G} \right|_{V_D, V_S} \quad g_{ms} = \left| \frac{\partial I_{DS}}{\partial V_S} \right|_{V_G, V_D} \quad g_{md} = \left| \frac{\partial I_{DS}}{\partial V_D} \right|_{V_G, V_S} \quad (6.13)$$

In our particular case a variation in the gate voltage will be applied, while keeping the other voltages fixed (drain, source and bulk). The equivalent circuit is showed

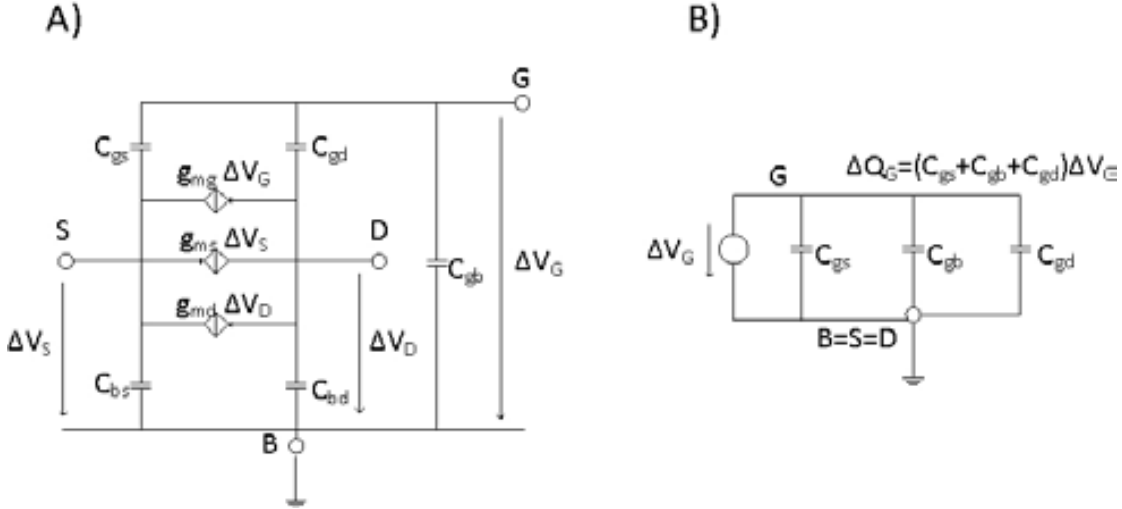


FIGURE 6.9: A) Medium frequency small-signal equivalent circuit. B) Effect of a gate potential variation.

in Figure 6.9 B). It can be observed how the transistor capacitance ( $C_{trans}$ ) defined on figure 6.6 is the equivalent of the gate to source, gate to bulk and gate to drain capacitances in parallel (equation 6.14). The EKV model provides an expression for each of these capacitances as a function of the forward and reverse normalized currents:

$$C_{trans} = C_{gs} || C_{gb} || C_{gd} = C_{gs} + C_{gb} + C_{gd} \quad (6.14)$$

$$i_f = I_F / I_S \quad (6.15)$$

$$i_r = I_R / I_S \quad (6.16)$$

$$C_{gs} = C_{ox} \left[ \frac{1}{c_{gss}(if, ir)} + \frac{1}{c_{gsw}(if)} \right]^{-1} \quad (6.17)$$

$$C_{gd} = C_{ox} \left[ \frac{1}{c_{gss}(if, ir)} + \frac{1}{c_{gsw}(ir)} \right]^{-1} \quad (6.18)$$



$$C_{gb} = C_{ox} \left( \frac{n-1}{n} \right) \left[ 1 - \frac{c_{gbs}(i_f, i_r) c_{gbw}(i_f, i_r)}{c_{gbs}(i_f, i_r) + c_{gbw}(i_f, i_r)} \right] \quad (6.19)$$

$$c_{gss}(i_f, i_r) = \frac{2}{3} \left[ 1 - \frac{i_r}{(\sqrt{i_f} + \sqrt{i_r})^2} \right] \quad (6.20)$$

$$c_{gsw}(i_f) = i_f G(i_f) \quad (6.21)$$

$$c_{gsw}(i_r) = i_r G(i_r) \quad (6.22)$$

$$c_{gbs}(i_f, i_r) = \frac{2}{3} \left[ 1 + 2 \frac{\sqrt{i_f i_r}}{(\sqrt{i_f} + \sqrt{i_r})^2} \right] \quad (6.23)$$

$$c_{gbw}(i_f, i_r) = i_f G(i_f) + i_r G(i_r) \quad (6.24)$$

$$G(i) = \frac{1}{\sqrt{i + \frac{1}{2}\sqrt{i} + 1}} \quad (6.25)$$

### 6.3.2 Beam Movement: Mass–spring–dash model

The beam maximum displacement position will be determined solving the mass–spring–dash equation (section 2.1.2) using the Runge-Kutta method.

The movement equation is given by the expression( see section 2.1.2 in chapter 2):

$$\ddot{y} + \frac{b}{m} \dot{y} + \frac{k}{m} y = \frac{F_E(y, t)}{m} \quad (6.26)$$

where the electrostatic force  $F_E$  is given by :

$$F_E = \frac{1}{2} \frac{C_{air}}{(s-y)} \Delta V^2 = \frac{1}{2} \frac{\varepsilon_o l w}{(s-y)^2} \Delta V^2 \quad (6.27)$$

$$C_{air} = \frac{\varepsilon_o l w}{s-y} \quad (6.28)$$

being  $s$  the air gap,  $y$  the beam displacement,  $\varepsilon_o$  the dielectric constant of air,  $l$  and  $w$  the length and width of the beam and  $\Delta V = V_G - V_{Gint}$  the voltage difference acting on the beam as it can be observed in figure 6.10:

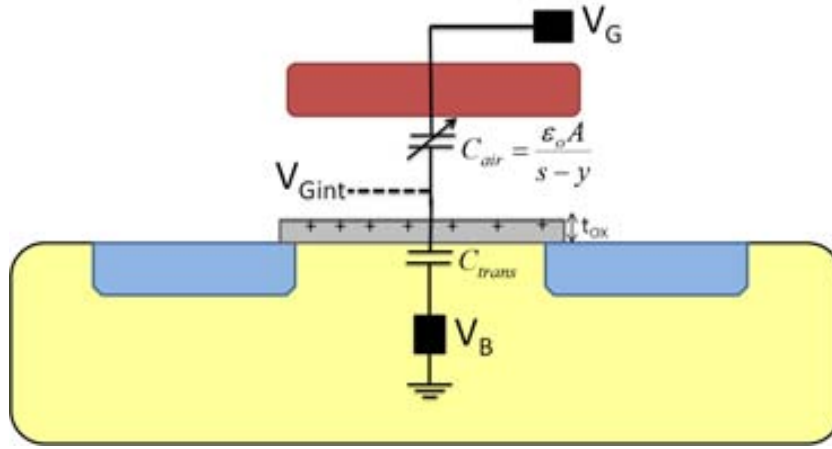


FIGURE 6.10: Voltage difference acting on the beam. Trapped charges on the oxide have been added.

However some charges can be trapped on the gate oxide (we will suppose that charges are trapped on top of the dielectric [137]) varying the voltage difference. Note that an accumulation of positive charges on the oxide will have the same effect on the charges at the channel that an increase in the  $V_{Gint}$  value, while negative charges will have the opposite effect. So the voltage difference consequence of these trapped charges can be modeled as  $\Delta V_{ox} = Q_d / C_{trans}$ , where  $Q_d$  is the charge trapped on the dielectric and  $C_{trans}$  the intrinsic transistor capacitance. In this way the voltage difference finally takes the next expression:

$$\Delta V = V_G - \left( V_{Gint} + \frac{Q_d}{C_{trans}} \right) \quad (6.29)$$

In order to fix the air gap capacitance value to calculate the electrostatic force the notion of electrical air-gap is introduced [158]. As it was mentioned before the charges at the channel, when it is formed, acts like an electrode, in order to establish an analogy with electrostatic actuation. The electrical air gap (EGT) represents the electric field between the gate and the channel, more relevant than the physical air gap. Its value is bigger than the air gap as it includes poly-depletion and also the gate oxide thickness, see equation

$$EGT = s + \frac{t_{ox}}{\varepsilon_{ox}} + \frac{d_{poly}}{\varepsilon_{Si}} \quad (6.30)$$

where  $s$  is the air gap,  $t_{ox}$  the oxide thickness,  $d_{poly}$  is the poly depletion depth and  $\varepsilon_{ox}$ ,  $\varepsilon_{Si}$  the oxide and silicon permittivity. Poly depletion depth is strongly dependant on the silicon doping level and on the surface electrode potential. Typical values for sub-micron CMOS technologies are around around 1–4 nm [159]. So in order to calculate the electrostatic force,  $s=EGT$  in equation equation 6.27.

Now that the electrostatic force has been obtained mass-spring-dash model can be solved using Runge-Kutta method, that transforms the differential equation into an equivalent first order equation system:

$$\frac{dy}{dt} = v \quad \frac{dv}{dt} = f(y, v, t) = -\frac{k}{m}y - \frac{b}{m}v + \frac{F_E}{m} \quad (6.31)$$

$$k_1 = hv \quad l_1 = hf(y, v, t) \quad (6.32)$$

$$k_2 = h \left( v + \frac{1}{2}l_1 \right) \quad l_2 = hf \left( y + \frac{k_1}{2}, v + \frac{l_1}{2}, t + \frac{h}{2} \right) \quad (6.33)$$

$$k_3 = h \left( v + \frac{1}{2}l_2 \right) \quad l_3 = hf \left( y + \frac{k_2}{2}, v + \frac{l_2}{2}, t + \frac{h}{2} \right) \quad (6.34)$$

$$k_4 = h \left( v + \frac{1}{2} l_3 \right) \quad l_4 = hf(y + k_3, v + l_3, t + h) \quad (6.35)$$

$$y(t + h) = y(t) + \frac{1}{6} (k_1 + 2k_2 + 2k_3 + k_4) \quad (6.36)$$

$$v(t + h) = v(t) + \frac{1}{6} (l_1 + 2l_2 + 2l_3 + l_4) \quad (6.37)$$

In order to obtain a stable solution, the pull-in condition ( $y \leq s/3$ ) is established (in the case of a cantilever this condition will be  $y \leq 0.44s$ ). When the c.c. beam displacement is bigger than  $s/3$  we force the beam position to be equal to  $s$  ( $y=s$ ) and hence the air gap disappears and the device operate as a common transistor.

### 6.3.3 Equivalent Circuit Model

In this section an electrical model of the Resonant Gate Transistor device will be developed in order to be able to simulate its frequency response.

The resonance of the structure will be obtained applying a DC voltage to the gate ( $V_{DC}$ ) (that will create the channel at the transistor) and an AC voltage ( $V_{AC}$ ), that will induce the movement of the structure near the equilibrium position fixed by  $V_{DC}$ .

So the model can be divided in two different block

- Resonator Model (already seen in section 2.3)
- MOSFET small signal model (for a given  $V_{DC}$  polarization)

The complete model is showed in figure 6.11. The vibrating gate and the air-gap capacitance can be modeled by a RLC series branch (that models the modulation of charges at resonance) in parallel with the electrical air-gap capacitance ( $C_{par}$ )

(blue color), coupled with the small signal MOSFET analysis [55] to account for the transistor gain ( $g_m = \partial I_{DS} / \partial V_{Gint}$ ) (green color). A load resistance has been added to the drain output (normally  $50\Omega$  for a network analyzer).

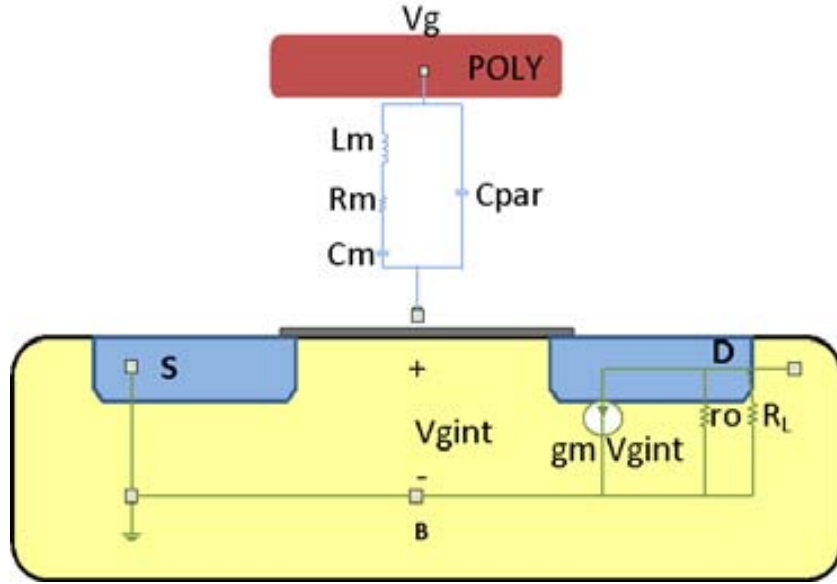


FIGURE 6.11: Small signal equivalent model of a RSG-MOSFET(low frequency).

The transfer function of the small signal equivalent MOSFET, taking into account the load resistance  $R_L$  is:

$$\frac{V_{out}}{V_{Gint}} = -g_m(r_o || R_L) \quad (6.38)$$

$r_o$  is the mosfet output resistance that models the effect of channel length modulation. Note how all the parameters have a fixed value for a given DC polarization: the resonator parameters  $R_m, C_m, L_m$  and the transistor parameter  $g_m, r_o$ .

The values of  $R_m, L_m$  and  $C_m$  are given by expressions 2.48, 2.46, 2.47 respectively and the electrical air gap capacitance by expression 6.28 where  $s=EGT$ . The values of  $g_m$  are obtained from the static simulations of the EKV-mass spring dash developed model. Once the  $I_{DS} - V_G$  and  $V_{Gint} - V_G$  curves has been obtained  $g_m$  can be fixed for a given DC voltage. The variation of  $V_{Gint}$  is obtained for a given  $V_{DC} + V_{AC}$  polarization.

### 6.3.4 RGT simulations

The developed models will be used in order to study the response of the resonant gate transistor device as a switch or in order to detect the movement of a resonant structure. The mechanical and electrical models need to be coupled as the position of the beam will fix the current at the output and the intrinsic voltage of the transistor ( $V_{Gint}$ ) will fix the electrostatic force in the beam and thus its position.

In figure 6.12 a simplified diagram of the procedure followed in order to model the resonant gate response is showed. A initial point ( $t_o$ ) is assumed, in which the position of the beam ( $y$ ) and the state of the transistor ( $V_{Gint}, C_{trans}$ ) are known, for a given gate voltage  $V_G$ . When a variation on the gate value is produced ( $V_G^{t_o} + \Delta V$ ), the position of the beam and the current at the drain will vary. In order to know both variables  $V_{Gint}$  has to be determined, as it will fix the electrostatic force between the beam and the transistor, and its polarization. However its value depend on the intrinsic transistor capacitance value  $C_{trans}$  that at the same time depend on  $V_{Gint}$  (the EKV model fixes the dependence of  $C_{trans}$  with  $V_{Gint}$ , section 6.3.1). The voltage divider equation and EKV expressions will form a nonlinear systems of equation that has to be solved numerically. Once it has been solved, the variables  $V_{Gint}$ ,  $C_{trans}$  and  $I_{DS}$  are known. Now the voltage difference  $\Delta V = V_G - V_{Gint}$  is established, so the position of the beam can be calculated with the mechanical model of the beam (showed in section 6.3.2). The values obtained ( $y, V_{Gint}, C_{trans}$ ) will be used as initial condition for a new iteration ( $t = t_o + h$ ). This procedure will be repeated until the beam reaches the stationary state (approximately a time equal to Q times the period ( $T = 1/f_o$ ) of the beam). When the displacement of the beam is bigger than  $s/3$  (for a c.c. beam structure) pull-in is produced and the displacement is fixed to the whole air gap ( $y=s$ ), acting now the device as a common MOSFET with a gate oxide of  $t_{ox}$ .

Using this procedure the response of a RGT device can be obtained when a voltage sweep is applied to its gate. In figure 6.13 the response of a common MOSFET ( $W = 8.7 \mu\text{m}$ ,  $L = 0.35 \mu\text{m}$ ,  $t_{ox} = 7.6 \text{ nm}$ ,  $V_{TO} = 0.58 \text{ V}$ ,  $\text{PHI} = 0.84 \text{ V}$ ,  $\text{GAMMA} = 0.58 \sqrt{\text{V}}$ ,  $I_S = 4.72 \mu\text{A}$ ), a FET with a fixed air gap (the transistor has

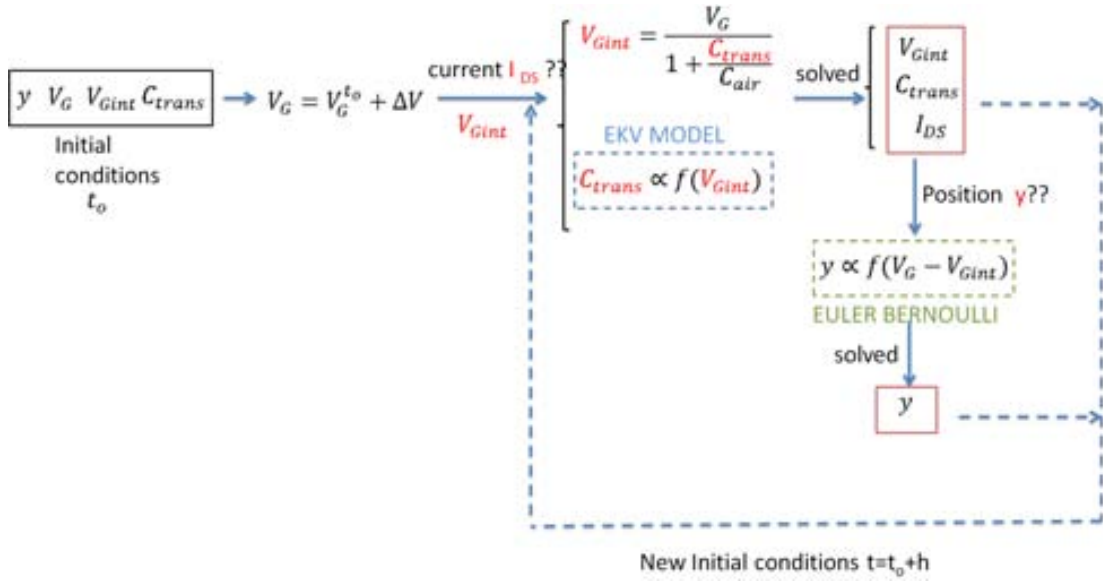


FIGURE 6.12: Diagram of the procedure to obtain beam position and current at the transistor drain (words in red are unknown variables).

the same parameters that the MOSFET but its dielectric is composed of an air gap of 12 nm ( $s=12$  nm) and a gate oxide of 7.6 nm) and a resonant gate transistor (it has the same characteristics than the fix air gap FET but in this case the air gap can vary as the gate can move) are represented.

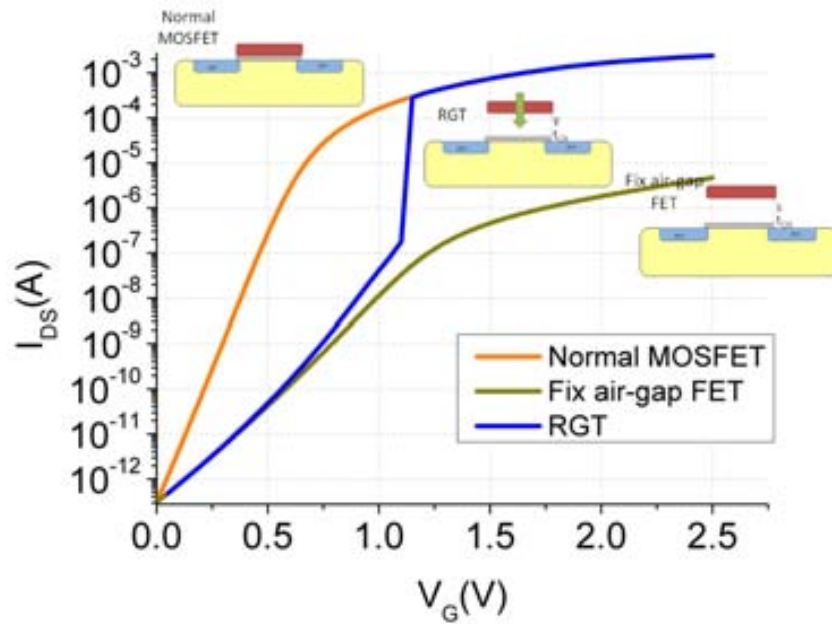


FIGURE 6.13: Common MOSFET, fix air gap FET and resonant gate transistor responses when a voltage sweep is applied to the gate.

As it can be observed, for low voltages the RGT device acts like a fix air gap

FET. As the electrostatic forces are weak no movement is produced in the gate and the voltage in the transistor ( $V_{Gint}$ ) is fixed by the air and transistor capacitances voltage divider. However when the voltage difference ( $\Delta V = V_G - V_{Gint}$ ) is increased, the beam starts moving, reducing the air gap and hence obtained bigger drain current. When the beam displacement reaches one third of the gap ( $y=s/3$ , for a c.c. beam) the structure collapses and the device starts to act as a common MOSFET. The pull-in event will be fixed by the elastic constant of the beam (see equation 3.11) and the operation point of the transistor as it fixes the ( $C_{trans}$ ) value and hence  $V_{Gint}$  (equation 6.1) that determines the electrostatic force (equation 6.27).

If the beam is brought into resonance, the drain current can be used to detect its movement too. In figure 6.14 the  $I_{DS} - V_G$  response of a RGT device ( $k=110$  N/m,  $s=12$ nm and a transistor with  $t_{ox}=7.6$  nm,  $W= 8.7$   $\mu$ m,  $L= 0.35$   $\mu$ m,  $V_{TO}=0.58$  V,  $\Phi=0.84$  V,  $\text{GAMMA}=0.58 \sqrt{V}$ ,  $I_S=4.72$   $\mu$ A) is represented. There are highlighted two possible operating points: one in weak inversion (blue), where the drain current shows an exponential dependence with gate voltage, and other in strong inversion (red). In order to detect the beam movement the transistor in weak inversion presents a maximum of drain current sensitivity for gate voltage variation but the signal level will be lower than in strong inversion.

## 6.4 Fabrication approaches for a RGT on AMS

### 0.35 $\mu$ m CMOS technology

In order to implement RGT scheme on AMS 0.35  $\mu$ m CMOS commercial technology we have considered two possible approaches using poly1 or poly2 as the structural layer for the MEMS resonator.



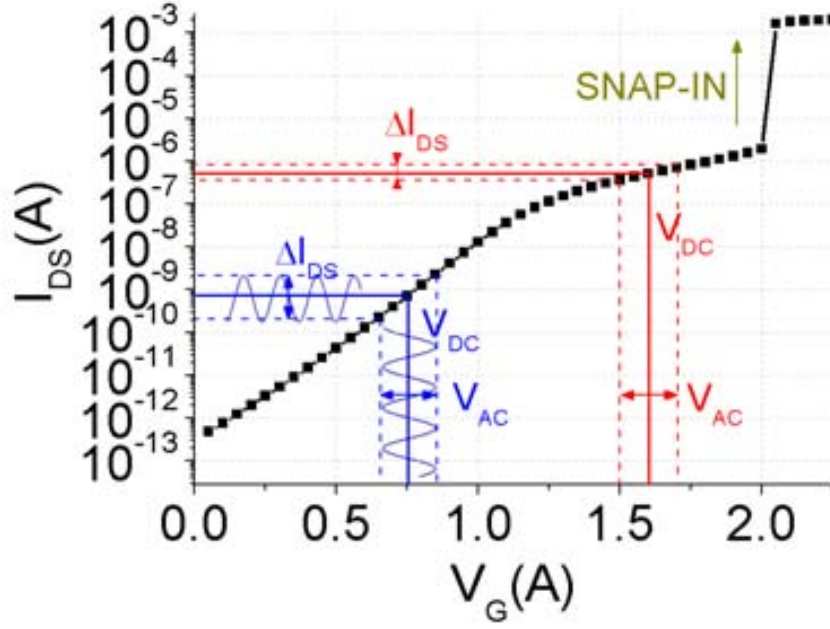


FIGURE 6.14: A)  $I_{DS} - V_{GS}$  RGT response showing two polarization points in order to detect resonance.

#### 6.4.1 Poly1 as structural layer.

In this approach poly1 is used as structural layer and at the same time it acts as the gate of a transistor that is defined on the maximum displacement point of the structure (center position in a C.C. Beam or in one extreme in the cantilever configuration, see figure 6.15 that show the configuration for a C.C. Beam). The structure is released with a post-CMOS wet etching (section 4.1.1) to remove the silicon oxide that surrounds the mobile structure and to partially erase the gate oxide (7.6nm) (figure 6.15 C)).

In this technological approach there is an important drawback because the high quality gate oxide will be partially or fully etched away during the releasing of the resonator. In addition, a low quality native oxide will grow on the active area after the releasing, changing the transistor parameters ((i.e. threshold voltage due to trapped charges [160]) (see equation 6.10 and figure 6.15 D)). However the small thickness of the gate oxide (7.6nm) ensures a small air gap and then small operating voltages.

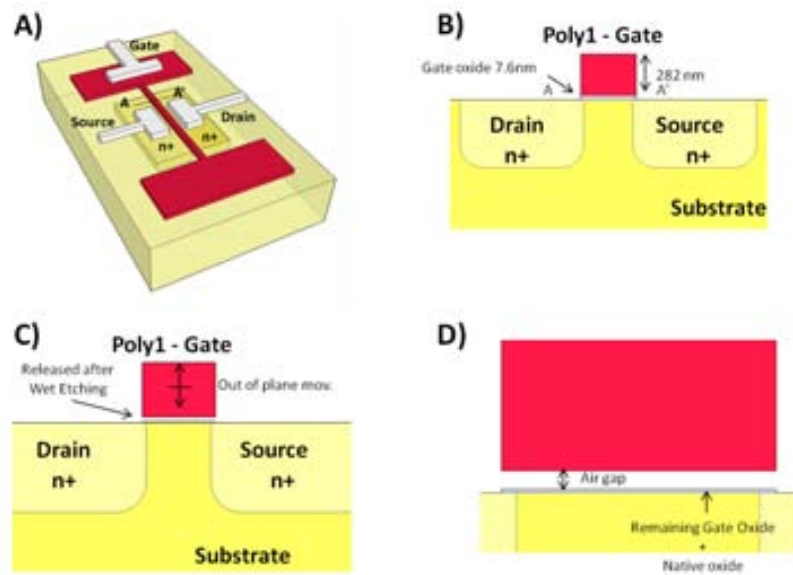


FIGURE 6.15: A) Schematic of a Resonant gate transistor device using poly1 gate as structural layer. B) A-A' cross-section C) Cross-section of the released beam. D) Zoom of the air gap after the releasing process.

Using this approach a C.C. beam structure was defined using polysilicon layer which at the same time acts as the gate of a transistor defined on its central area (the anchors were not designed above active area)(dimension details on table 6.2). Note that the transistor dimensions are:  $W/L=8.5 \mu\text{m}/0.35 \mu\text{m}$ . In figure 6.16 the layout and a SEM image of the released device are shown. In its inset the characteristic curvature of the bird's beak (BB) effect can be observed, consequence of defining the poly layer between active and passive area. It is defined by the encroachment of the oxide underneath the silicon nitride mask during the thermal oxidation step [161]. Additionally it has been demonstrated how precurved polysilicon layer can project it upward during the release, due to compressive stress, enhancing the gap [95]. This compressive stress can reduce the resonant frequency of the structure [162].

In order to check how the bird's beak affect the resonant frequency Coventor simulations were performed. In the first mode, a resonant frequency of 28.5 MHz was found, bigger than the theoretical value obtained using expression 2.14 (24.6 MHz). As it can be observed on figure 6.17 B) the portion of the beam between the anchor and bird's beak does not move significantly in the first vertical mode.

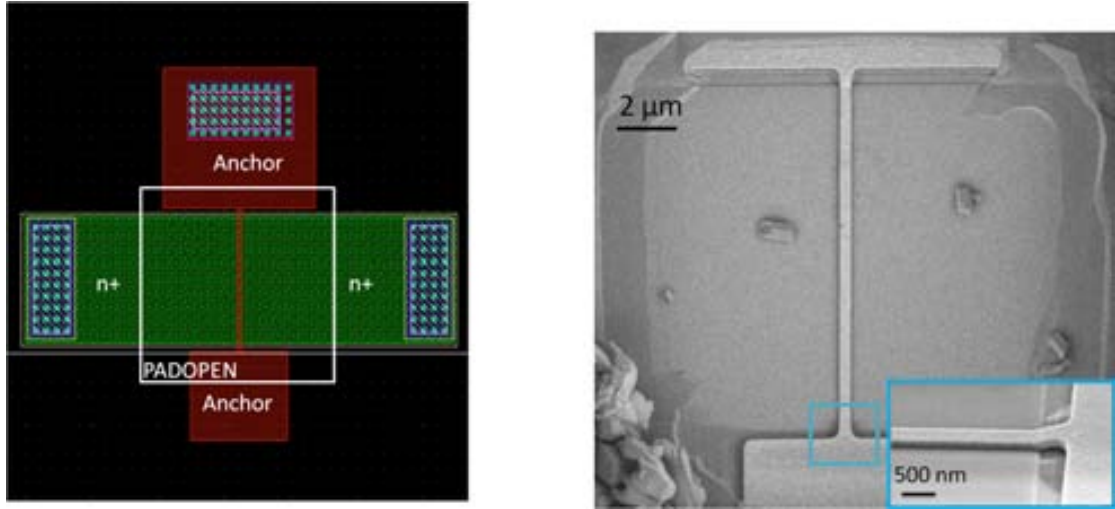


FIGURE 6.16: A) Layout of a poly 1 RGT device. B) SEM image of the released device. In the inset a lateral view of the anchor area shows beam curvature due to different height between active and non-active transistor area.

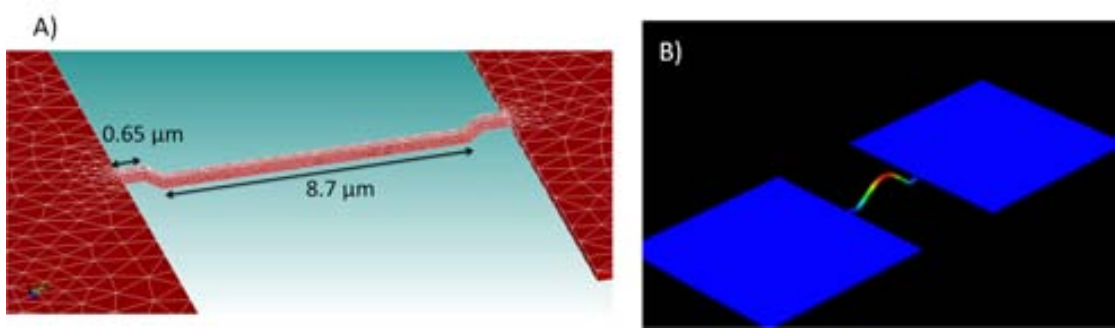


FIGURE 6.17: A) Bird's beak in the Coventor model B) First mode shape.

Beam Length (μm)	Width (nm)	Thickness (nm)	Transistor length (nm)	Transistor width (μm)	gap (nm)	$f_o$ (MHz)
10	350	282	350	8.7	7.6	28.5

TABLE 6.2: Poly1 resonant gate transistor dimensions.

The snap-in voltage depends on the beam dimensions and on the state of the transistor, as the voltage applied to the gate is divided by the air and transistor capacitance (see equation 6.1). Supposing that the gate oxide is completely erased ( $s=7.6$  nm), the voltage difference ( $\Delta V = V_G - V_{Gint}$ ) necessary to produce snap-in, can be obtained using the expression 3.11, assuming that the coupling area ( $A$ ) is fixed by the active area and an effective length of  $8.7 \mu m$  is used to calculate the spring constant value (based on the Coventor simulations). Under this assumption

$$V_{PI} = \Delta V = 0.39V.$$

### 6.4.2 Poly2 as structural layer.

In this case is not the gate of the transistor which is resonating, a structure is defined just above the gate to ensure that its polarization will modulate the charges of the channel. It is like a multi-gate device but instead of vary the voltage of the second gate, it is its position which modulates the charges. In a CMOS-MEMS approach the role of the resonant structure can be played by poly2 or a metal layer or even a stack of silicon oxide and metal layer as it has already been reported in [148].

In order to implement Poly2 approach, Poly2 of Poly2-Insulator-Poly1 (PIP) capacitances can be used as the structural layer (see figure 6.18). The insulator of the capacitance (40nm silicon oxide) is etched, releasing the poly2 structure while the oxide below Poly1 is preserved guaranteeing the transistor performance. The movement of this Poly2 structure modulates the charge on the transistor that will be fixed by the polarization on poly1.

The main advantage of this approach is the sub-100nm gap obtained (40 nm) that will ensure an operation at low voltages.

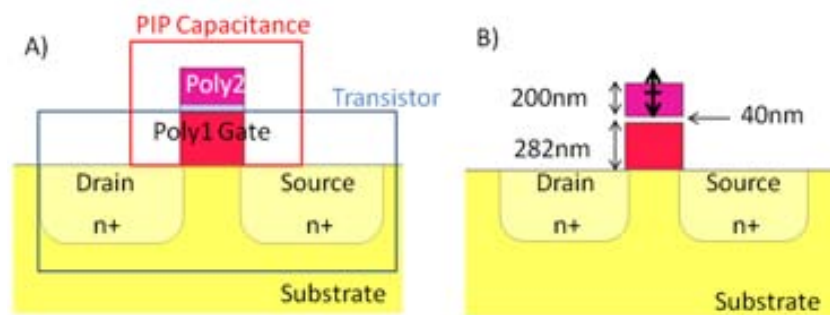


FIGURE 6.18: Resonant gate transistor using poly 2 as structural layer. A) Before the releasing process and B) after been released.

The main problem of this approach comes from the fabrication process. Define a PIP capacitance using poly1 that is simultaneously acting as the gate of a transistor violates technology design rules and as a consequence the correct fabrication of the device can not be guaranteed.

A poly2 C.C Beam was defined above a polysilicon transistor as it is shown in the layout of figure 6.19 A). Its dimensions are showed in table 6.3. In figure B) a SEM image of the fabricated device is shown. It can be easily appreciated how the poly2 C.C. Beam was not successfully fabricated.

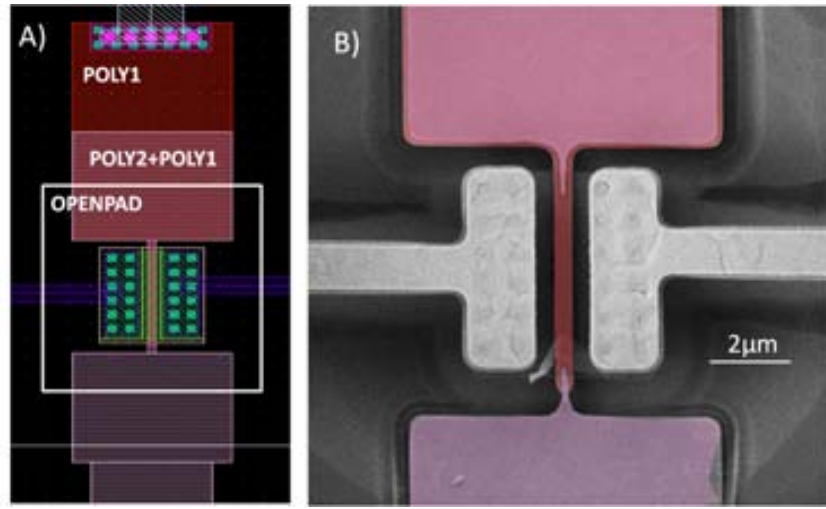


FIGURE 6.19: A) Layout of a poly 2 RGT device. B) SEM image of the fabricated device (the images have been coloured for an easy recognition).

Poly2 length ( $\mu\text{m}$ )	poly2 width (nm)	Poly1 length (nm)	poly1 width (nm)	Transistor width ( $\mu\text{m}$ )	Transistor length ( $\mu\text{m}$ )
6.4	350	6	350	5	0.350

TABLE 6.3: Poly2 RGT Dimensions

## 6.5 Electrical characterization of the unreleased RGT CMOS-MEMS

In this section the I/V curves of the MOS transistors with unreleased poly gates are presented. Figure 6.20 A) shows its  $I_{DS} - V_{GS}$  and B)  $I_{DS} - V_{DS}$  responses

using the semiconductor analyzer Agilent B1500A. The transistor parameters need to be extracted to model the transistor response in the simulations.

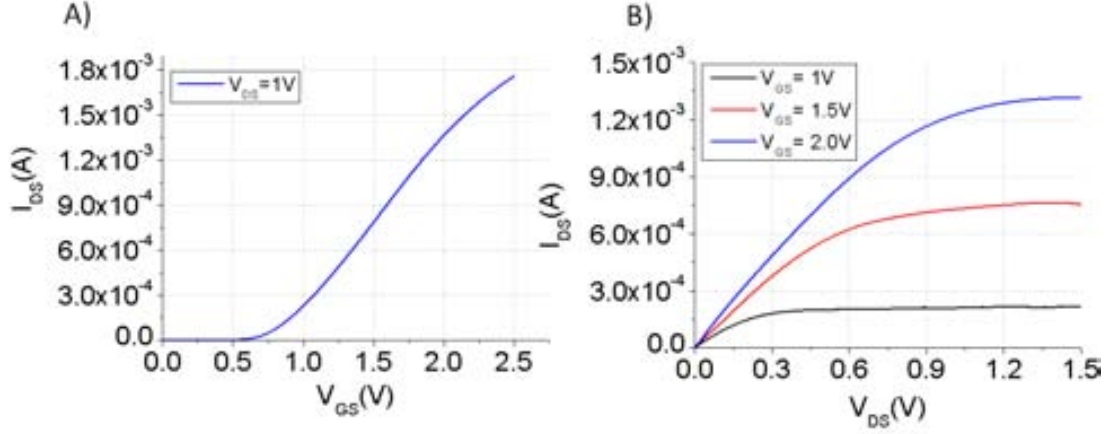


FIGURE 6.20: Electrical characterization of the unreleased poly 1 transistor ( $W=8.7 \mu\text{m}$ ,  $L=0.35 \mu\text{m}$ ). A)  $I_{DS} - V_{GS}$  response and B)  $I_{DS} - V_{DS}$  response.

The EKV parameters (GAMMA, PHI, VTO and  $I_s$ ) are extracted following the next procedure indicated in [157]:

- $I_s$  is extracted from the square root of the  $I_{DS}$  current when the transistor is polarized in strong inversion (SI). According to [163], in this region the reverse current (equation 6.4) can be neglected and the drain current (eqn. 6.2) is exclusively composed of the forward current (eqn 6.3), that in this region, presents a quadratic asymptotic behavior:

$$I_D = \frac{I_s}{(2U_T)^2} (V_P - V_S)^2 \quad (6.39)$$

For a given gate voltage (i.e. a fixed pinch-off voltage), it is thus simple to determine  $I_s$  from the strong inversion slope of the  $\sqrt{I_s}$  vs.  $V_S$  characteristic (see equation 6.40 and figure 6.22 A)), derived from the drain current expression in SI saturation:

$$\sqrt{I_D} = \frac{\sqrt{I_s}}{2U_T} (V_P - V_S) \quad (6.40)$$

In this particular case  $I_s=4.72 \mu\text{A}$ .

- Once  $I_s$  value has been determined, pinch-off voltage can be obtained. According to equation 6.3, the pinch-off voltage can be measured at the source in saturation (reverse current can be neglected again), for a particular value of the drain current approximately equal to half the specific current  $I_s$  (assuming  $(\ln(2))^2 \cong 1/2$ ) and drain and gate shortcut, see figure 6.21. The  $V_P$ - $V_G$  characteristic is simply obtained by sweeping the gate voltage and measuring the source voltage  $V_S \simeq V_P$  (see figure 6.22 B)).

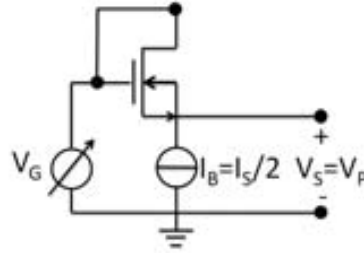


FIGURE 6.21: Set-up used for the measurement of the pinch-off voltage  $V_P$  vs.  $V_G$  characteristic (extracted from [157]).

- $V_{TO}$  is determined from  $V_P$ - $V_G$  response as the particular value of  $V_G$  corresponding to the  $V_P = 0$  cross point ( $V_{TO}=0.58$  V).
- GAMMA and PHI are extracted by fitting equations 6.7 and 6.6 to the measured characteristic (see figure 6.22 B)). In our particular case PHI=0.84 V and GAMMA=0.58  $\sqrt{V}$  (which is equivalent to say that the doping level on the transistor is  $2.12 \cdot 10^{17} \text{ donors/cm}^3$ )

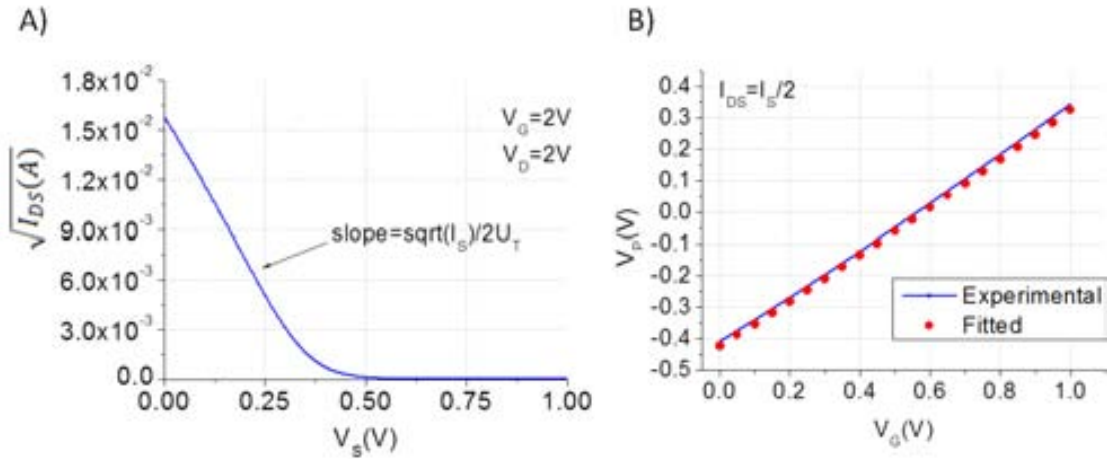


FIGURE 6.22: Electrical  $\sqrt{I_{DS}}-V_S$  and  $V_P-V_G$  curves for parameter extraction procedure from a RGT transistor as received from the foundry.



Using these parameters and the dimensions specified in table 6.2 (poly 1 approach), the drain to source current was simulated in a gate voltage sweep. Figures 6.23, 6.24 show the experimental and simulated results. It can be observed how the simulated values are in good agreement with the experimental results (in the  $I_{DS}$ - $V_{GS}$  curve, the measured experimental data for low polarization  $V_{GS} < 0.25$  V is affected by noise floor of the experimental set-up that prevents us from measuring the real transistor response). The subthreshold swing has been measured (83.68 mV/decade) in order to check if this value is improved in the RGT device acting as a switch.

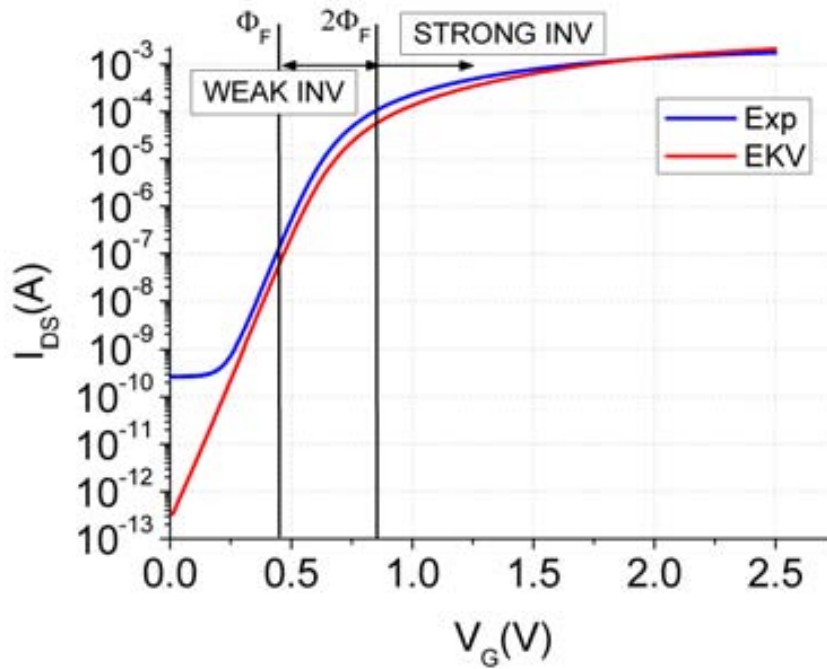
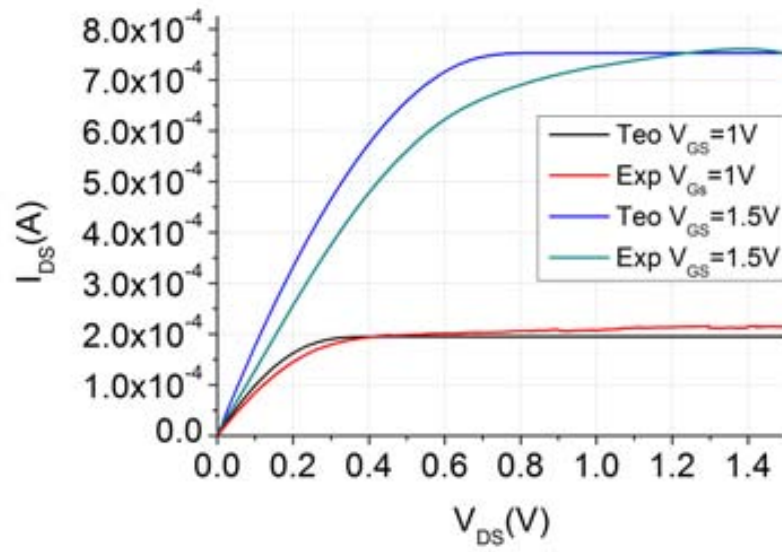
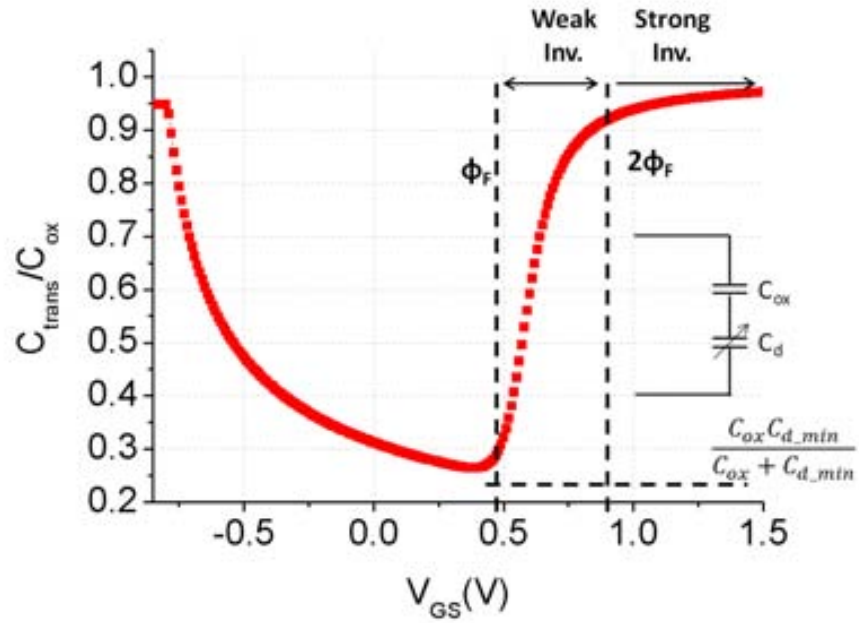


FIGURE 6.23: Experimental and simulated  $I_{DS} - V_{GS}$  curve ( $V_{DS} = 1$ ).

In addition the  $C_{trans}$  capacitance has been calculated using equation 6.14 and it is represented in figure 6.25 with the obtained parameters. As it can be observed the intrinsic capacitance of a MOS transistor acts like a series combination of a fixed, voltage-independent gate oxide ( $C_{ox}$ ) capacitance, and a voltage-dependent semiconductor capacitance (mainly due to the depletion region  $C_d$ ), such that the overall MOS capacitance becomes voltage dependent [37].

$C_{trans}$  plays an important role determining the electrostatic force on the resonator (as it fixes the  $V_{Gint}$  value together with  $C_{air}$ , equation 6.1) and hence its snap-in



FIGURE 6.24: Experimental and simulated  $I_{DS} - V_{DS}$  curves.FIGURE 6.25:  $C_{trans}/C_{ox}$ - $V_G$  voltage

voltage. A bigger snap-in value will be observed if the transistor is forced to be in strong inversion ( $C_{trans} \approx C_{ox}$ ) instead of weak inversion ( $C_{trans} < C_{ox}$ ).

## 6.6 Poly1 RGT simulations

Once the transistor was characterized, the behavior as a resonant gate device was simulated supposing different transistor conditions. Note that the releasing process consist on partially or totally erase the gate oxide so the transistor behavior can not be predicted after the etching. For that reason different simulations will be performed supposing different conditions, in order to gain some insight into the experimental results.

In all the simulations performed in this section it has been supposed an effective beam length of  $8.7 \mu\text{m}$  that corresponds to the MOS transistor width (section of the c.c. beam defined in active area). This assumption has been adopted, as it was observed in the Coventor simulations that the portion of the beam between anchors and Bird's Beak did not move significantly in the first vertical mode (figure 6.17). In addition note that in order to calculate the electrostatic force the electrical air gap has been used 6.30, as it was commented in section 6.3.2.

- Different gate oxide thickness

The transistor has a fixed gate oxide thickness of 7.6 nm (specify by AMS 0.35  $\mu\text{m}$  technology) before the etching. After the releasing process, an air gap and the remaining oxide will form the dielectric of the transistor, but the thickness of each of them are unknown. The value of the gate thickness after the releasing process is difficult to predict as the exact composition of the gate oxide is unknown, and therefore its etch rate can not be determined. Moreover, the thickness of the native oxide that will grown after the etching when the device is in ambient condition can not be predicted.

In figure 6.26 the RGT response is shown for two different gate oxide thickness ( $t_{ox} = 1 \text{ nm}$  and  $t_{ox} = 6 \text{ nm}$ ). Although the air gap is bigger in the RGT device with  $t_{ox} = 1 \text{ nm}$ , its snap-voltage is lower. This is due to its bigger transistor capacitance ( $C_{trans}$ ) that reduce the  $V_{gint}$  values (equation 6.1) and as a consequence increase the voltage difference ( $\Delta V = V_G - V_{Gint}$ ), reaching the pull-in voltage at lower gate voltage value.

Bigger currents are obtained when  $t_{ox}$  is reduced as  $I_s$  parameter scale proportionally to  $C_{ox}$  (see equation 6.5).

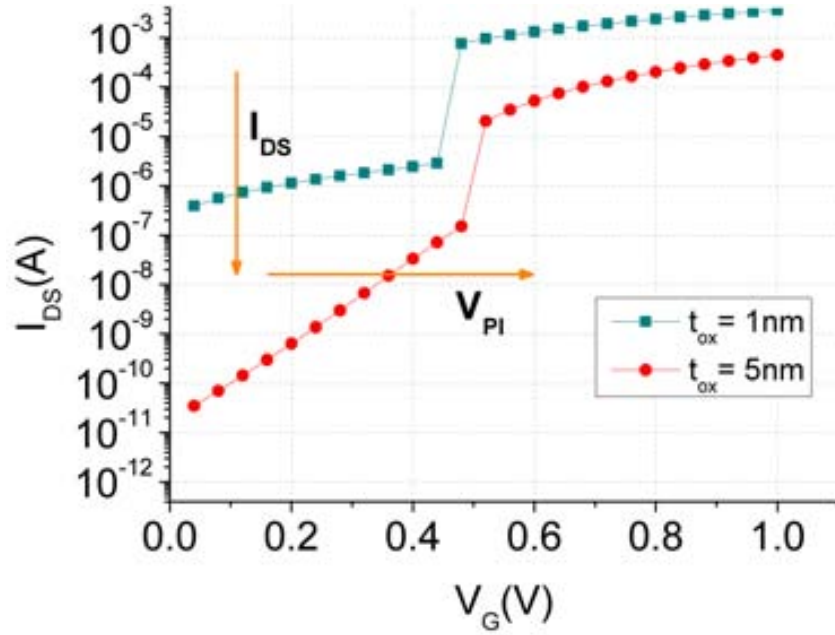


FIGURE 6.26: Comparison of the RGT response for various gate oxide thickness ( $t_{ox} = 1nm$  and  $t_{ox} = 6nm$ ) ( $V_{DS} = 1V$ ).

- $C_{ox}$  variation

In the previous section, different simulations were performed taking attention to  $t_{ox}$  value that fixes the  $C_{ox}$  capacitance and therefore  $C_{trans}$ . However, the gate oxide dielectric constant will vary too after the etching as a worse quality oxide will be obtained. It will affect to the current value (as  $I_s$  scales proportionally to its value 6.5) and VTO value too (equation 6.10). In figure 6.27 the  $I_{DS}$ - $V_G$  response is showed supposing a  $t_{ox} = 6$  nm ( $s = 1.6$  nm) and different dielectric constants ( $\epsilon_{ox} = 3.45 \cdot 10^{-11}$  F/m).

As it can be observed the  $I_{DS}$  current is reduced (as  $I_s$  scale proportional to  $C_{ox}$ , equation 6.5) and the  $C_{trans}$  capacitance is reduced too obtaining bigger  $V_{Gint}$  (equation 6.1) and as a consequence lower electrostatic forces and a bigger pull-in voltage.

- Air gap variation

Another issue to take into account is that the air gap can be enhanced if the polysilicon presents compressive stress, as it was shown in [95].

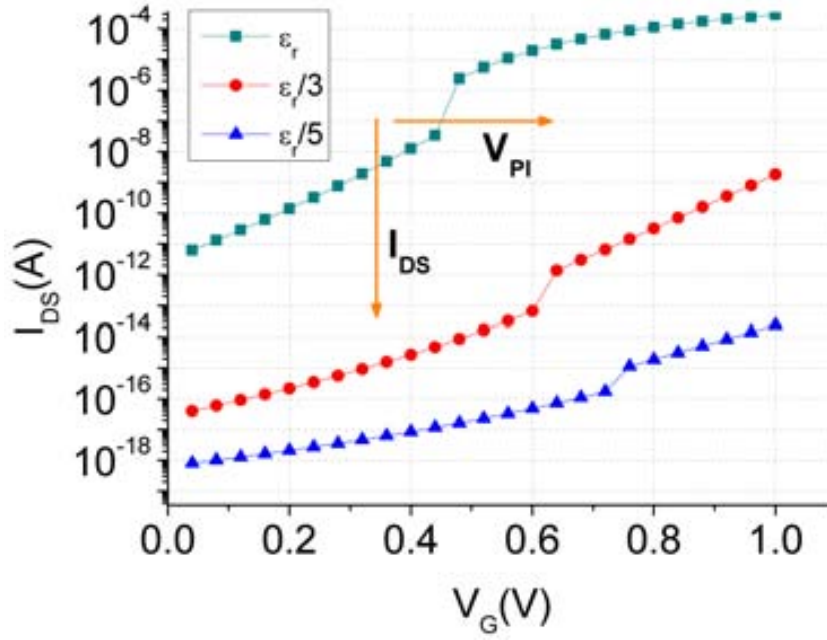


FIGURE 6.27: Comparison of the RGT response for various gate oxide dielectric constants ( $V_{DS} = 1V$ ).

In figure 6.28 the current at the drain A) is shown for different air gaps (after the releasing process), when a voltage sweep is applied to the gate. An oxide thickness of 6 nm has been supposed ( $V_{TO}=0.47$  V,  $\text{PHI}=0.84$  V and  $\text{GAMMA}=0.46 \sqrt{V}$ , values obtained supposing  $t_{ox}= 6\text{nm}$  and  $\epsilon_{ox} = 3.45 \cdot 10^{-11}$  F/m ).

As it can be observed, as bigger is the air gap bigger snap-in values are found. In figure 6.28 B) the voltage difference acting on the MOSFET is represented. Additionally, in table 6.4 the voltage difference in order to produce snap-in in one structure with our same dimensions and gap has been calculated using expression 3.11. On the same table the simulated voltage difference when the snap-in is produced is shown too. As it can be observed in the table the simulated results are agree with the theoretical values.

- Oxide trapped charges.

Charge can be trapped in the oxide that remains once the releasing process has been done. This will affect to the threshold voltage (as it was shown in expression 6.10, 6.11) and to the electrostatic force (equation 6.29). Both effects will be present. In recent works it has been demonstrated how the

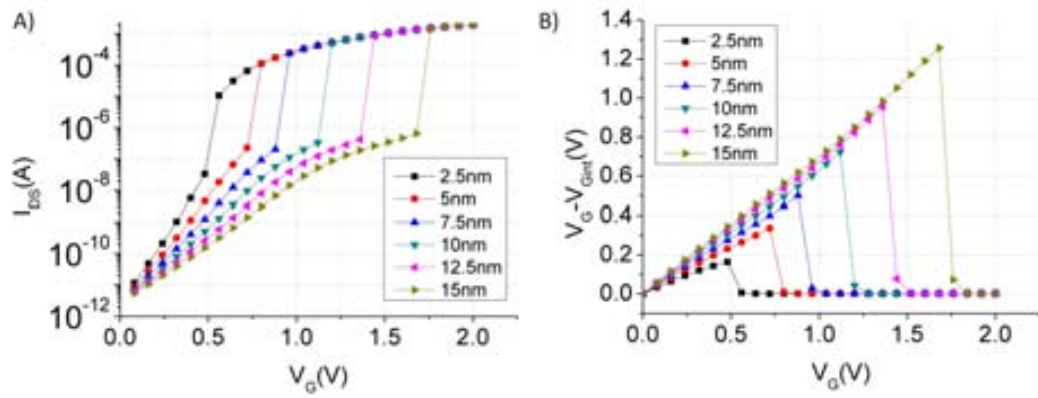


FIGURE 6.28: RGT switch A)  $I_{DS}$ - $V_G$  and B)  $\Delta V$  simulation for various air gaps ( $V_{DS} = 1$ ).

Air gap (nm)	$V_{snap}$ (V) exp 3.11	Simulated max $\Delta V = V_G - V_{Gint}$
2.5	0.17	0.16
5	0.33	0.33
7.5	0.53	0.50
10	0.76	0.72
12.5	1.01	0.96
15	1.28	1.25

TABLE 6.4: Poly1 resonant gate transistor snap-in voltages for different air gaps.

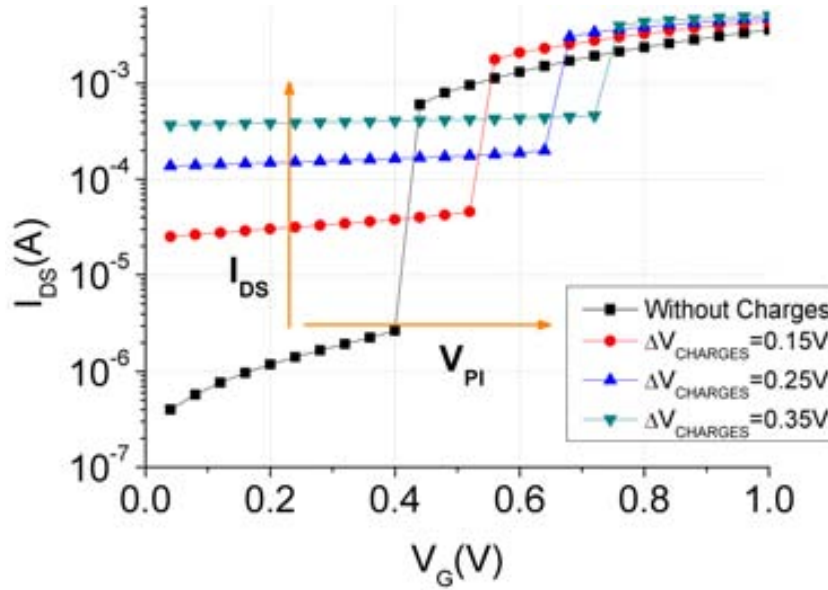
trapped charge can vary the pull-in voltage in more than 1 V and the threshold voltage value in 7-8 V range [137]. It will depend on the oxide and air gap capacitance.

In a NMOS transistor, an accumulation of positive charges on the gate oxide will reduce threshold voltage while negative trapped charge will increase its value (expression 6.10, 6.11). At the same time, positive charges will decrease the electrostatic force between the gate and the intrinsic voltage while negative charges will increase it (see expression 6.29). Additionally, it can be observed how the variation of the electrostatic force will depend on the state of the transistor as the charge trapped on the oxide is divided by  $C_{trans}$ . This means that a bigger  $\Delta V$  will be produced while the transistor is operating in strong inversion, where  $C_{trans}$  has its bigger value (see figure 6.25). In table 6.5 this effects are summarized.

	$V_{TO}$	Elect. Force
negative charges	$\uparrow\uparrow$	$\uparrow\uparrow$
positive charges	$\downarrow\downarrow$	$\downarrow\downarrow$

TABLE 6.5: Effect of gate oxide trapped charges in a NMOS transistor.

Several simulation were performed supposing an air gap of 5.6 nm, an oxide thickness of 2 nm with  $V_{TO}=0.11$  V , $\Phi=0.84$  V GAMMA=  $0.1 \sqrt{V}$ . Accumulation of positive charges was supposed based on previous works [137], varying its concentration. Simulations were performed in order to check how the electrical response of the device changes (as it can be seen on the simulation without charges the snap-in event takes place when the transistor is in strong inversion, in this region  $C_{trans} = C_{ox}$ , so it can be supposed that the threshold voltage variation and the variation in the electrostatic force is the same)

FIGURE 6.29:  $I_{DS} - V_G$  simulation when positive charges are trapped on the gate oxide ( $V_{TO}=0.11$  V,  $V_{DS} = 1$  V).

As it can be appreciated in the simulations, the trapped charges produce two main effects in the device behavior. The first effect is the variation on the snap-in voltage, produced by the change in the electrostatic force that the trapped charges produce. The second effect is due to the threshold voltage

variation. As its value is reduced ( $V_{TO}=0.11-\Delta V_{CHARGES}$  V) the transistor operates in strong inversion at lower  $V_G$  values and the current values are higher.

In table 6.6 the consequences of the listed effects in the drain to source current and pull-in voltage are summarized:

Effect	$I_{DS}$	$V_{PI}$
$\uparrow\uparrow$ gate oxide thickness ( $t_{ox}$ )	$\downarrow\downarrow$	$\uparrow\uparrow$
$\uparrow\uparrow$ air gap (s)	$\downarrow\downarrow$ (OFF state)	$\uparrow\uparrow$
$\downarrow\downarrow$ oxide dielectric constant ( $\varepsilon_{ox}$ )	$\downarrow\downarrow$	$\uparrow\uparrow$
positive trapped charge	$\uparrow\uparrow$	$\uparrow\uparrow$

TABLE 6.6: Simulation results summary.

## 6.7 Poly1 RGT experimental results

In this section the experimental response of the poly 1 RGT device will be presented as a switch and as a resonator.

### 6.7.1 Poly1 RGT as a switch

Poly 1 resonant gate device (showed in section 6.4.1) was released using the post CMOS fabrication process previously reported (section 6.4.1) and characterized as a switch using a semiconductor Devices Analyzer (Agilent B1500A) and the proposed set-up shown in figure 6.30. The current in all the terminal was acquired.

Its electrical response is represented in figure 6.31 where the current in the drain is showed (no change in the gate current, pico-Amps range, was observed). A switching effect due to pull-in at low voltages occurs and is directly measured on the drain current, which validates the actuation and detection principle of the RGT-MOSFET. As it can be seen, the snap-in event appears at 2.25 V (being the

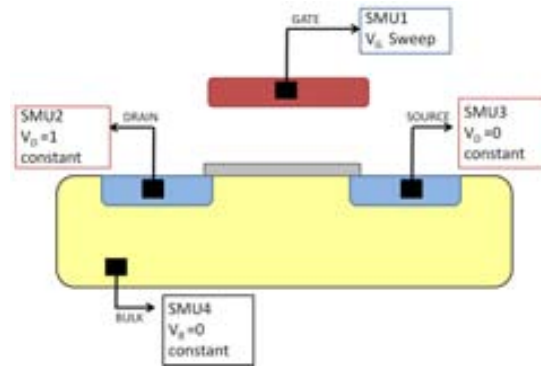


FIGURE 6.30: Schematic of the experimental Setup to characterize the device as a switch

transistor is in strong inversion) with a  $I_{ON}/I_{OFF} = 1.7 \cdot 10^2$  and a slope of at least 10 mV/decade beating the subthreshold swing of the unreleased transistor (83.68 mV/decade).

Moreover, the current in the ON state, once the pull-in has been produced is lower than in the unreleased device. It is produced by a degradation of the  $I_S$  value (equation 6.5). It can be explained as a consequence of a reduction of the dielectric constant of the oxide (oxide  $\epsilon_r$ ) or a reduction of the mobility of the electrons in the channel. Since carriers in the channel are very close to the semiconductor-oxide interface, they are scattered by surface roughness and by coulombic interaction with fixed charges in the gate oxide [160].

Additionally the transition between the weak and strong inversion can be observed in the OFF state. That indicates that the  $V_{TO}$  has not reached very low value (due to trapped charges or  $C_{ox}$  variations) after the releasing.

### 6.7.2 RGT frequency response

Once the releasing of the device was demonstrated by its experimental characterization as a switch, frequency characterization was performed following the characterization set-up shown in figure 6.32.

Its frequency response is shown in figures 6.33, 6.34 where it can be appreciated how for a gate polarization of 1.65 V the frequency peak appears. Its resonant



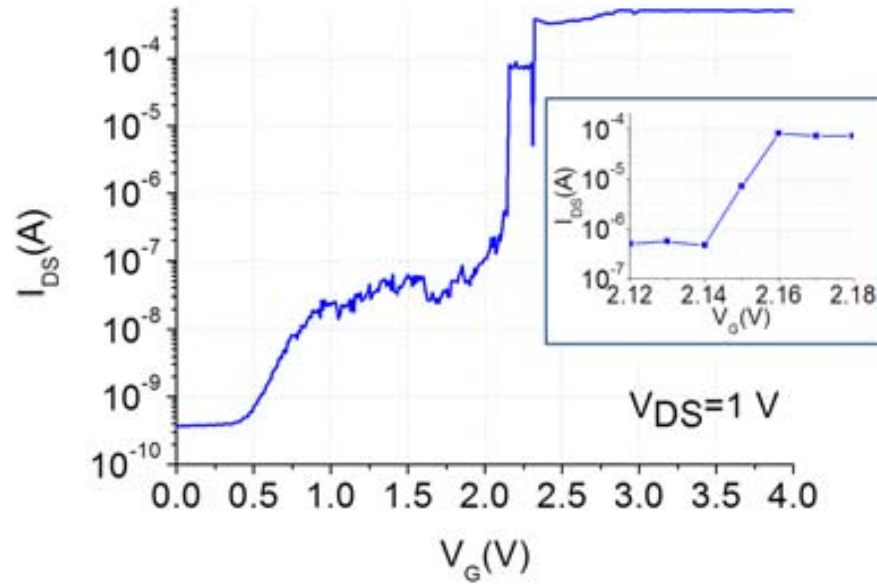


FIGURE 6.31: A)  $I_{DS} - V_G$  experimental response and inset of the electrical response between ON and OFF state.

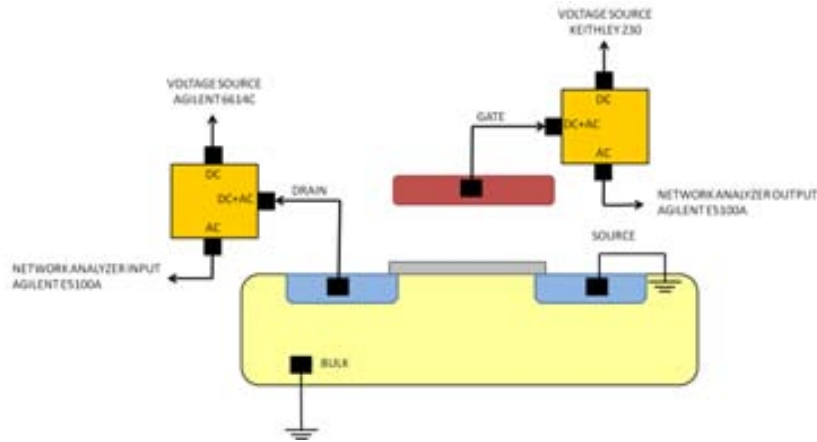


FIGURE 6.32: RGT frequency characterization experimental set-up.

frequency is slightly lower than the obtained in the Convector simulation (28.5 MHz). Compressive stress reduce the frequency response of mechanical structures [162]. As it can be appreciated the beam was polarized until 3V, so a bigger snap-in voltage value is reached in this device.

The quality factor of the resonator was calculated using Q phase formula 2.28 obtaining a value of 25 V. This low value could be caused by a high air damping due to the small gap. Using its value the motional resistance  $R_m$  can be estimated using the expression 2.48 and assuming an effective voltage of 1 V ( $\Delta V = V_G - V_{Gint}$ ),

1.3 M $\Omega$  is obtained. The parasitic capacitance  $C_{air}$  can be estimated too, from the anti-resonance frequency, using the expression 2.50). The value obtained is 3.25 fF ( $C_m = 0.14$  fF with  $Q=25$ ) that is equivalent to an air gap capacitance of 8.29 nm (note that this gap is obtained when a DC voltage is applied to the beam and it is closer to the transistor surface, so a bigger physical gap will be obtained in practice). Again this gap enhancement could be explained supposing compressive stress.

In addition the increase in the signal level thanks to the transistor gain can be observed.

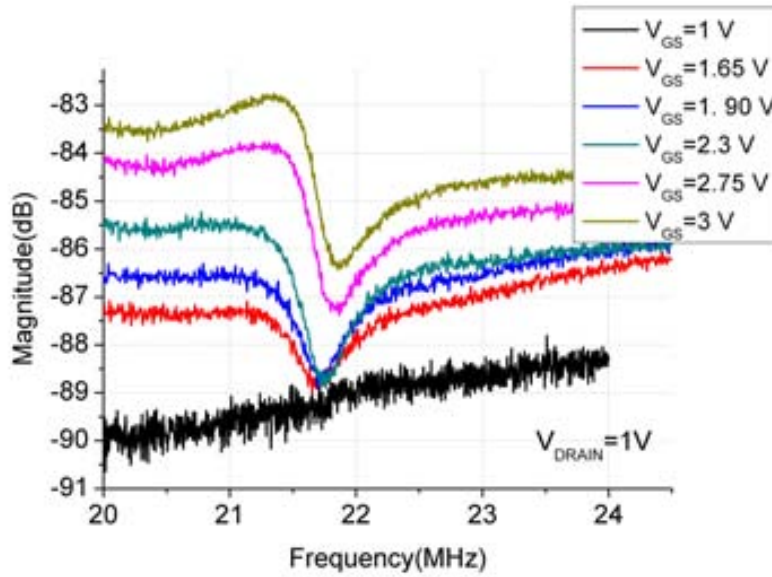


FIGURE 6.33: Poly 1 device electrical characterization for different gate voltages ( $V_{AC}=10$ dBm).

The drain current can be estimated using the frequency response (see table 6.7), knowing that (being the load resistance  $R_L = 50\Omega$ ):

$$S_{21} = 20 \cdot \log\left(\frac{V_{out}}{V_{in}}\right) = 20 \cdot \log\left(\frac{g_m V_{Gint} R_L}{V_{in}}\right) = 20 \cdot \log\left(\frac{I_D R_L}{V_{in}}\right) \quad (6.41)$$

As it can be observed the drain current changes linearly with the gate voltage, indicating that the RGT device is working in strong inversion. In weak inversion the response is masked by the parasitic capacitance.

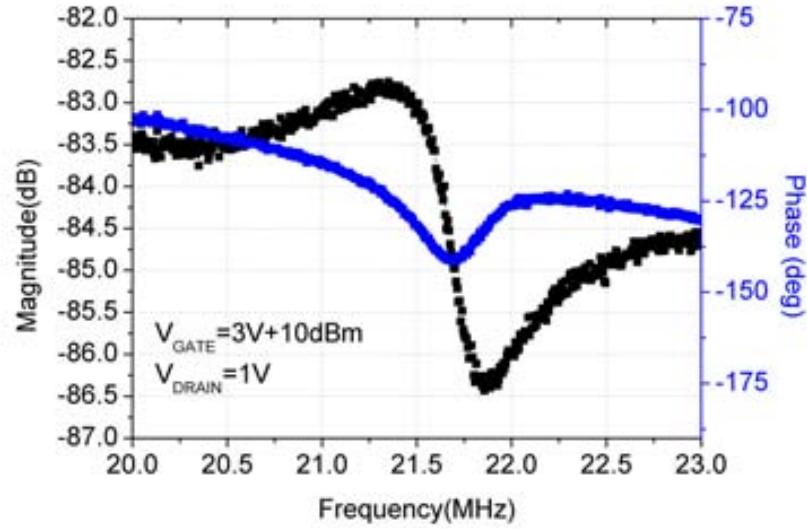


FIGURE 6.34: Magnitude and phase frequency response of poly1 RGT device, with  $V_G=3$  V+10 dBm.

$V_{DC}$	$S_{21}(20MHz)$	$I_{DS}$
1.65 V	-87.5	0.59 $\mu$ A
1.90	-86.5	0.67 $\mu$ A
2.30	-85.5	0.75 $\mu$ A
2.75	-84	0.89 $\mu$ m
3	-83.5	0.93 $\mu$ m

TABLE 6.7: Calculated  $I_{DS}$  current values, using the measured frequency response.

## 6.8 Conclusions

In this chapter, it has been proven how resonant gate transduction can be easily implemented on commercial CMOS technologies using a maskless post CMOS releasing process. Moreover, small operating voltages have been got, (the second lowest in the state of the art, just beat by [147] and much lower than the other reported CMOS approaches [148] (41V)), thanks to the small gap obtained, which makes its operating voltages totally compatible with CMOS technology. In addition, it is also important to remark the small dimensions of our device (just beat by [33]) and that at low voltages, high operating frequencies has been reached.



# Chapter 7

## Conclusions

### 7.1 Conclusions

This main contributions of this thesis are:

- **The development of NEMS structures in sub-micron CMOS technologies.** After the successful integration of MEMS structures in UMC 0.18  $\mu\text{m}$  and AMS 0.35  $\mu\text{m}$  commercial CMOS technology, our intra CMOS-MEMS approach has been applied to ST 65nm Technology trying to scale MEMS devices to nanoscale.
  - Successful integration of NEMS structures has been demonstrated in ST 65nm (the smallest CMOS node in which released structures has been developed). NEMS devices have been fabricated using copper and poly with a cross sections of 60 nm x 100 nm and 90 nm x 180 nm respectively.
  - A post-CMOS releasing process based on dry and wet etching has been developed, showing the capability of erase big amounts of oxide (designs buried 4.95  $\mu\text{m}$  were released).
  - A copper clamped clamped beam resonator was characterized using ST metal 6 layer, showing robust behavior.

- **A new oscillator configuration composed exclusively of mechanical structures was proposed**

A model was developed to simulate the dynamic response of the mechanical switches inverter in a ring oscillator configuration finding that under certain conditions, one may contrive to generate a periodic square signal using an odd number of MEMS inverters in a ring oscillator configuration.

- **Study and implementation of nano–micro mechanical switches in CMOS technologies.**

N/MEMS switches were successfully fabricated using a CMOS–MEMS fabrication process. Three different approaches were proposed:

- Microelectromechanical switches based on BEOL metal layers (based on Aluminum in AMS 0.35  $\mu\text{m}$  CMOS technology and Copper in ST 65nm technology).
- N/Microelectromechanical switches developed using the MIM capacitive module that allow us to obtain small gaps (27 nm). The structural material was based on TiN.
- Stack switches. Different AMS 0.35  $\mu\text{m}$  metal layers (M4 and M3) were joined using VIAS layer in order to obtain a MEMS switch with big contact area in order to obtain better reliability.

Using a CMOS–MEMS fabrication process low snap–in voltages values were obtained (5 V in the MIM configuration and 5.5 V in ST 65nm), abrupt behavior (4.3 mV/decade in ST) and a good  $I_{ON}/I_{OFF}$  ratio ( $10^4$  in the MIM approach). As it can be observed in figure 7.1 where the state of the art switches are represented according to its coupling area (length by thickness in an in plane movement and length by width in an out of plane movement) and snap–in values, the switches developed in this thesis, demonstrated the integration of minimum dimensions switches using a CMOS approach and operating at low voltages. It can be observed in the figure how MIM and ST switches, present a low coupling area, that ensures a good integration capability, and low

operating voltages, just beat by bottom-up approaches and other three top-down devices with similar performance but without the added value of a CMOS fabrication process.

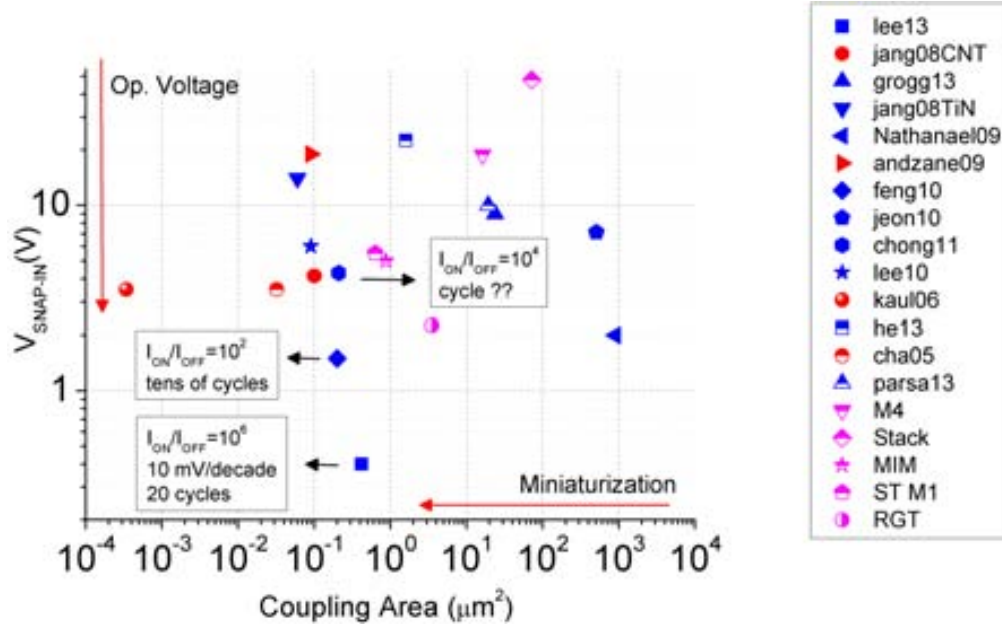


FIGURE 7.1: Mechanical switches state of the art (the devices that have a blue color are developed using a top-down approach and the ones in red a bottom-up approach. Our devices have been represented in pink color (the references of the different works are specified in tables 3.3 and 3.3.)

- **Implementation of resonant gate transduction in CMOS-MEMS.**

Due to the sensing problems found to detect the movement of NEMS structures using capacitive read-out, Resonant gate transduction has been implemented and studied in a commercial CMOS technology.

A polysilicon campled beam with resonant gate transduction method was successfully implemented in AMS  $0.35 \mu\text{m}$ . As a switch a low snap-in voltage (2.25 V) was obtained (the fourth in the switches state of the art, see figure 7.1, but with the added value of being completely CMOS) and subthreshold slope of 10 mV/decade. In addition, the resonant gate transduction method was also used to detect its resonance at 24 MHz, operating at voltages lower than 3 V.

## 7.2 Future work

Based on the achievements of this work, some promising directions for future research and development in the field of NEMS are identified

- **CMOS–NEMS integration on ST 65nm**

Although the fabrication of CMOS–NEMS devices in ST 65nm CMOS technology has been validated, the read–out of the smaller M1 and poly structures has not yet been demonstrated. The measurement of the stand–alone NEMS was obscured by the parasitic capacitances. In order to overcome this problem, besides the resonant gate approach, an amplifier stage could be integrated at the output of the resonator [20].

Additionally, it was observed how the encapsulation and passivation layers of the chip were damaged during the dry etching stage of the post–CMOS releasing process. As a solution, it is proposed to develop an additional fabrication step (lithography, deposition and lift–off), at wafer level, to protect the encapsulation and passivation layer during the releasing. This additional step is proposed to be performed at wafer level as working with wafer makes the alignment easier and the samples are handled more easily, especially in this case, that CHIPS have  $1\text{ mm}^2$  area. As an alternative to this solution, and working at CHIP level, we propose the use of the top metal layer as ‘buried mask’. It consists on using the top metal layer (M7) as a mask. It is defined on the places that we want to protect, as the circuitry, and an open window is defined above the resonator, as can be appreciated in figure 7.2 A). After the dry etching, even in the worst case, with the passivation and encapsulation completely erased, the M7 layer will stay as it will not be etched by the RIE (figure 7.2 B)). Then the wet etching is performed and due to a short etching time requirements the ‘buried mask’ will not be released, unlike the resonator (see figure 7.2).

- **CMOS–MEMS switches.**



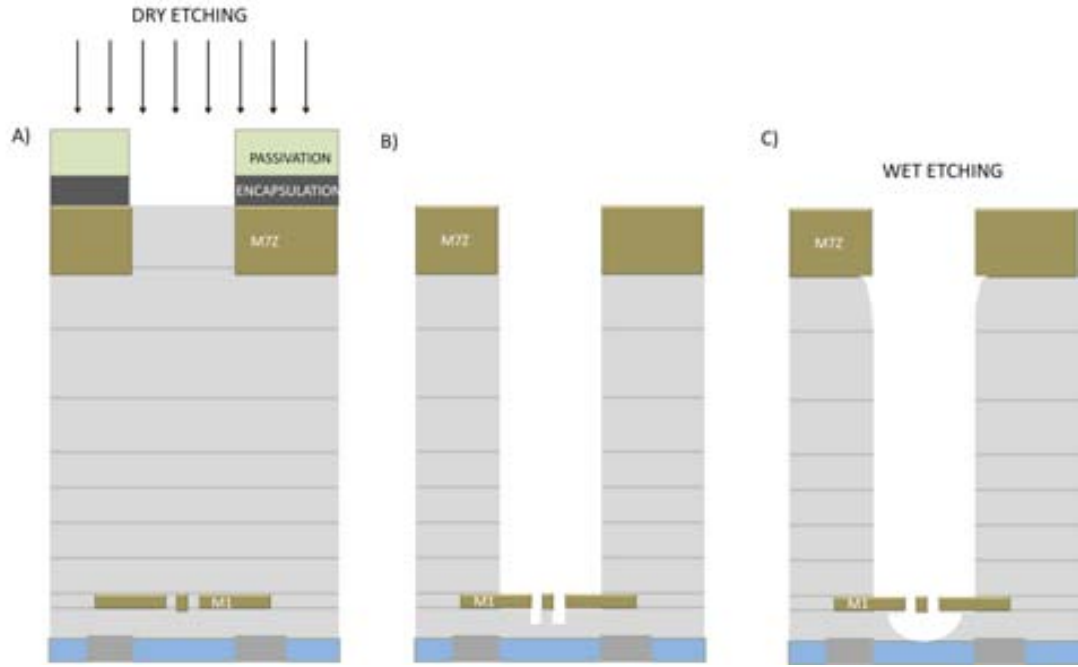


FIGURE 7.2: ST releasing process with the proposed 'buried mask'

The mechanical switches developed in this work were designed with the main aim to obtain low operating voltage, thanks to small gaps, and trying to minimize their dimension in order to obtain a good integration density capability. This was successfully obtained at an expense of 3-T operation. The main drawback of the N/MEMS switches were its low reliability. Note that for a relay-based embedded sensor application operating for 10 years at 100 MHz clock the mechanical switches should operate  $\approx 10^{14}$  cycles [60]. As it can be observed in the state of the art tables 3.3, 3.3 and in figure 3.14, we are still far from this yield, specially when the devices are scaled. However, the main reason for this poor yield is due to the electromechanical contact when the movable part is brought into contact with the electrode. In fact, some groups have bet for a decoupling between the mechanical and electrical domains, attaching a conductive layer to the movable structures [50], [64] obtaining promising results ( $10^9$  cycles). With this decoupling, materials with good mechanical properties can be chosen in order to obtain low operating voltages (Young modulus low) and hard materials are used to make the electrical contact. However, it is needed a dedicated difficult fabrication process and it has not been proven yet that minimum dimensions devices can be fabricated

using it. However, in our particular case, we are limited to the materials and fabrication process that the selected commercial CMOS technology offers. So in order to improve the contact an additional layer can be coated on the switch once the releasing process has been done. A reliable MEMS switch technology employing titanium oxide ( $TiO_2$ ) coated tungsten (W) electrodes has been developed [164]. The  $TiO_2$  coating improves contact stability and relay endurance because it acts as an oxidation barrier and also serves to limit current conduction to mitigate micro-welding issues. Another option is to coat materials that do not form insulating native oxide, that degrades the contact. Ruthenium is a good candidate as it forms a conductive oxide ( $RuO_2$ ) in air, and in addition it has a high hardness (the limit current at contact should be limited externally in this case)[36].

- Resonant gate transistor has been successfully implemented using a CMOS–MEMS approach in AMS 0.35  $\mu m$ . This technology was chosen instead of ST 65nm due to its cheaper prize and faster time response between design and chips delivery. So, as future work, it should be implemented in ST 65nm CMOS technology using minimum dimensions polysilicon layer as mechanical material.

### 7.3 Author contributions

In this section, the contributions of this thesis work as articles published in international journals are listed as well as a selection of the most relevant contributions to international conferences with peer review process.

Articles in preparation:

- J.L. Muñoz-Gamarra, A. Uranga, N. Barniol, *Polysilicon Resonant gate approach on AMS 0.35  $\mu m$  commercial CMOS technology* . In preparation.
- J.L. Muñoz-Gamarra, A. Uranga, N. Barniol, *Nanomechanical switch based on ST 65nm commercial CMOS technology*. In preparation.

## Articles in international journals

- J.L. Muñoz-Gamarra, A. Uranga, N. Barniol, *Nanomechanical switches based on metal-insulator-metal capacitors from a standard complementary-metal-oxide semiconductor technology*, Applied Physics Letters. vol. 104, p. 243105, 2014
- J.L. Muñoz-Gamarra, G. Vidal-Alvarez, F. Torres, A. Uranga, N. Barniol, *CMOS-MEMS switches based on back-end metal layers*, Microelectronic Engineering, Volume 119, 1 May 2014, Pages 127-130, ISSN 0167-9317
- J.L. Muñoz-Gamarra, P. Alcaine, E. Marigo, J. Giner, A. Uranga, J. Esteve, N. Barniol, *Integration of NEMS resonators in a 65nm CMOS technology*, Microelectronic Engineering, Volume 110, October 2013, Pages 246-249, ISSN 0167-9317
- A. Uranga, J. Verd, E. Marigo, J. Giner, J.L. Muñoz-Gamarra, N. Barniol (2013). *Exploitation of non-linearities in CMOS-NEMS electrostatic resonators for mechanical memories*, Sensors and Actuators A: Physical, 197, 88-95.
- J. Giner, A. Uranga, E. Marigo, J.L. Muñoz-Gamarra, E. Colinet, N. Barniol, J. Arcamone (2012). *Cancellation of the parasitic feedthrough current in an integrated CMOS-MEMS clamped-clamped beam resonator*, Microelectronic Engineering, 98, 599-602.
- J. Giner, A. Uranga, J.L. Muñoz-Gamarra, E. Marigo, N. Barniol (2012). *A fully integrated programmable dual-band RF filter based on electrically and mechanically coupled CMOS-MEMS resonators*, Journal of Micromechanics and Microengineering, 22(5), 055020.
- J. Giner, A. Uranga, J.L. Muñoz-Gamarra, E. Marigo, N. Barniol (2012). *VHF monolithically integrated CMOS-MEMS longitudinal bulk acoustic resonator*, Electronics letters, 48(9), 514-516.

- E. Marigo, J.L. Muñoz-Gamarra, J. Giner, A. Uranga, N. Barniol, *A 230 MHz CMOS-MEMS bulk acoustic wave resonator*, Microelectronic Engineering, Volume 98, October 2012, Pages 458-462, ISSN 0167-9317
- E. Marigo, J.L. Muñoz-Gamarra, G. Vidal, J. Giner, F. Torres, A. Uranga, N. Barniol, *Cross coupled beams CMOS-MEMS resonator for VHF range with enhanced electrostatic detection*, Microelectronic Engineering, Volume 88, Issue 8, August 2011, Pages 2325-2329, ISSN 0167-9317

Abstract in peer reviewed proceedings of relevant conferences:

- J.L. Muñoz-Gamarra, A. Uranga, N. Barniol, *Nanomechanical switch based on ST 65nm commercial CMOS technology*, 40th International Conference on Micro and Nano Engineering (MNE), 2014, Lausanne, Switzerland, 22-26 September 2014
- J.L. Muñoz-Gamarra, A. Uranga, N. Barniol, *NEMS switches monolithically fabricated on CMOS MIM capacitors*, 27th Eurosensors Conference, 2014, Brescia, Italy, 7-10 September 2014
- J.L. Muñoz-Gamarra, G. Vidal-Alvarez, F. Torres, A. Uranga, N. Barniol, *Characterization of aluminum CMOS-MEMS switches*, 39th International Conference on Micro and Nano Engineering (MNE), 2013, London, England, 16-19 september 2013
- J.L. Muñoz-Gamarra, N. Barniol, J. Juillard, *Analysis of a MEMS-based ring oscillator* Circuits and Systems (ISCAS), 2012 IEEE International Symposium on , pp.2103-2106, 20-23 May 2012 doi: 10.1109/ISCAS.2012.6271700
- J. L. Muñoz-Gamarra, P. Alcaine, E. Marigo, J. Giner, A. Uranga , N. Barniol, *Implementation of NEMS resonator in a 65nm CMOS technology* , 38th International Conference on Micro and Nano Engineering (MNE), 2012, Toulouse, France, 16-20 september 2012

- J.L. Muñoz-Gamarra, E. Marigo, J. Giner, A. Uranga, N. Barniol, *Mass sensor limits of resonant beams monolithically integrated in a 65nm industrial CMOS technology*, BCN-b Barcelona nanotechnology cluster, Bellaterra (Spain) 2 June 2011
- J.L. Muñoz-Gamarra, E. Marigo, J. Giner, A. Uranga, N. Barniol, *Mass sensor limits of resonant beams monolithically integrated in a 65nm industrial CMOS technology*, 8th International Workshop on Nanomechanical Sensing 2011, NMC 2011 Dublin (Ireland), 11-13 May 2011
- J. Giner, A. Uranga, J. L. Muñoz-Gamarra, E. Marigó, E. Colinet, J. Arcamone, and N. Barniol, *Cancellation of the Parasitic Current in an Integrated CMOS-MEMS Clamped-Clamped Beam Resonator*, 37th International Conference on Micro and Nano Engineering 11-13 September 2011
- E. Marigo, J.L. Muñoz-Gamarra, J. Giner, A. Uranga and N. Barniol, *CMOS-MEMS Dogbone resonator with capacitive and piezoresistive sensing capabilities Participation*, 37th International Conference on Micro and Nano Engineering (MNE) 11-13 September 2011
- J. Giner, A. Uranga, E. Marigo, J. L. Muñoz-Gamarra, and N. Barniol, *UHF CMOS-MEMS bulk acoustic wave resonator*, in Frequency Control and the European Frequency and Time Forum (IFCS), 2011 Joint Conference of the IEEE International, 2011, pp. 1-4. 2011
- J.L. Muñoz-Gamarra, E. Marigo, J. Giner, A. Uranga, N. Barniol, *Characterization of CMOS-MEMS resonator by pulsed mode electrostatic actuation*, Frequency Control Symposium (IFCS), 2010 IEEE International Newport Beach, California, USA, 2-4 June 2010
- J. Giner, A. Uranga, F. Torres, E. Marigo, J. L. Muñoz Gamarra, and N. Barniol, *A CMOS-MEMS filter using a V-coupler and electrical phase inversion*, in Frequency Control Symposium (IFCS), 2010 IEEE International, pp. 344-348, , 2010,

- E. Marigo, J. L. Muñoz-Gamarra, J. Giner, J. L. Lopez, F. Torres, A. Uranga, N. Barniol, and J. Verd, *Linear operation of a 11MHz CMOS-MEMS resonator*, in Frequency Control Symposium (IFCS), 2010 IEEE International, 2010, pp. 158-161.
- E. Marigo, J.L. Muñoz-Gamarra, G. Vidal, J. Giner, F. Torres, A. Uranga, N. Barniol, *Cross Coupled Beams CMOS-MEMS Resonator for VHF Range with Enhanced Electrostatic Detection*, 36th International Conference on Micro and Nano Engineering (MNE) 2010
- J.L. Lopez, E. Marigo, J. Giner, J.L. Muñoz-Gamarra, F. Torres, A. Uranga, N. Barniol, *CMOS-MEMS free-free beam resonators*, 40th European Solid-State Device Research Conference (ESSDERC) 2010

# Appendix A

## Ring Oscillator semi-analytical limit cycle prediction

In this annex the semi-analytical limit cycle for the ring oscillator configuration is calculated.

The following set of assumptions is made. First of all, only small amplitude motion of the beam is considered, so that  $\mathbf{B}(\mathbf{a}) \rightarrow \mathbf{B}(\mathbf{0})$  and  $\mathbf{f}_c(\mathbf{a}) \rightarrow \mathbf{f}_c(\mathbf{0})$  in equation 3.23. This allows us to recast 3.23 in the following state-space form:

$$\dot{\mathbf{z}} = \mathbf{A}\mathbf{z} + \mathbf{b}_e V^2 + \mathbf{b}_e(z) \quad (\text{A.1})$$

with

$$\mathbf{z} = \begin{bmatrix} \mathbf{a} \\ \dot{\mathbf{a}} \end{bmatrix} \quad \mathbf{b}_e = \begin{bmatrix} \mathbf{0} \\ \mathbf{f}_e(\mathbf{0}) \end{bmatrix} \quad (\text{A.2})$$

$$\mathbf{A} = \begin{bmatrix} \mathbf{0}_2 & \mathbf{I}_2 \\ -\mathbf{K} & -\mathbf{B}(\mathbf{0}) \end{bmatrix} \quad (\text{A.3})$$

It is also assumed that mechanical contact is instantaneous and governed by:

$$\mathbf{z}(t_c^+) = \mathbf{S}\mathbf{z}(t_c^-) \quad \mathbf{S} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & -\kappa & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad (\text{A.4})$$

where  $t_c$  designates the instant at which contact occurs. Equation A.4 implies that, when a contact takes place, the state of the system is unchanged, except for the first modal velocity coefficient, governed by:

$$\dot{a}_1(t_c^+) = -\kappa \dot{a}_1(t_c^-) \quad (\text{A.5})$$

Coefficient  $\kappa < 1$  then represents the mechanical losses during contact. Between impacts, a beam is then governed by:

$$\dot{\mathbf{z}} = \mathbf{A}\mathbf{z} + \mathbf{b}_e V^2 \quad (\text{A.6})$$

Finally,  $V^2$  in A.6 can take either of two values, ideally equal to  $V_{off}^2 = 0$  and  $V_{on}^2 = V_{dd}^2$ , provided the electrical time constant is small (otherwise, the load capacitance is only partially charged or discharged. This, however, does not affect very much the rest of the analysis. The commutation from one value to the other takes place when the output of the previous inverter in the ring oscillator loop changes.

From this set of hypotheses, the existence of simple limit cycles can be predicted. In particular, let us assume that a limit cycle with period  $T$ , half-period  $T/2$  and delay  $\tau$  can take place in the system, meaning that:

$$V(t) = \begin{cases} V_{on} & t \in ]0, \tau] \\ 0 & t \in ]\tau, \tau + \frac{T}{2}] \\ V_{on} & t \in ]\tau + \frac{T}{2}, T] \end{cases} \quad (\text{A.7})$$



where the origin of time is taken at the moment when the mechanical contact occurs. Note that  $\tau$  depends on the number of stages in the ring oscillator:  $\tau = 0$  for a one-stage oscillator,  $\tau = T/3$  for a three-stage oscillator, etc. The analytical solution of A.6 A.7 is straightforward, provided the beam does not come into contact with the drain for  $t \in ]0, T[$ . Under this hypothesis, we find:

$$\mathbf{z}_f - \mathbf{e}^{AT} \mathbf{z}_o = \left( \mathbf{I}_4 - \mathbf{e}^{A(\frac{T}{2}-\tau)} + \mathbf{e}^{A(T-\tau)-e^{AT}} \right) \mathbf{z}_e V_{on}^2 \quad (\text{A.8})$$

where  $\mathbf{z}_f = \mathbf{z}(T^-)$ ,  $\mathbf{z}_o = \mathbf{z}(0^+)$ ,  $\mathbf{z}_e = -\mathbf{A}^{-1} \mathbf{b}_e$  and  $\mathbf{e}^M$  designates the matrix exponential of  $\mathbf{M}$ . If the motion is periodic, we should have  $\mathbf{z}(T^-) = \mathbf{z}(0^-)$ , so that, using A.4, A.8 becomes:

$$\mathbf{z}_o(V_{on}^2) = (\mathbf{S}^{-1} - \mathbf{e}^{AT})^{-1} \left( \mathbf{I}_4 - \mathbf{e}^{A(\frac{T}{2}-\tau)} + \mathbf{e}^{A(T-\tau)} - \mathbf{e}^{AT} \right) \mathbf{z}_e V_{on}^2 \quad (\text{A.9})$$

For a given value of  $\gamma$ ,  $V_{on}^2$  should then be adjusted so that:

$$\begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} \mathbf{z}_o = \gamma \quad (\text{A.10})$$

Since  $\gamma$  and  $V_{on}^2$  are positive, this is only possible if, for instance,

$$\begin{bmatrix} 1 & 0 & 0 & 0 \end{bmatrix} \mathbf{z}_o > 0 \quad (\text{A.11})$$

Furthermore, at time  $0^+$ , the beam should be bouncing away from the drain (and not into it), i.e.:

$$\begin{bmatrix} 0 & 0 & 1 & 0 \end{bmatrix} \mathbf{z}_o(1) > 0 \quad (\text{A.12})$$

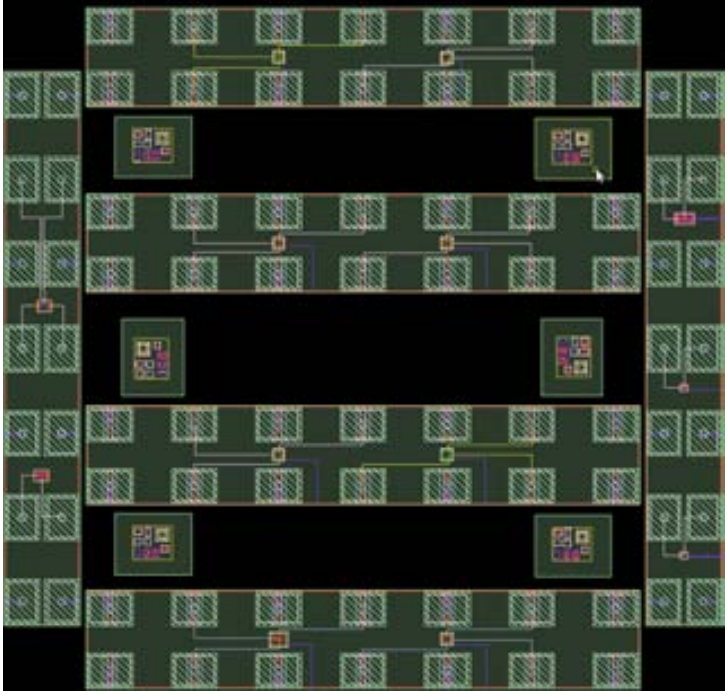
Finally A.9 is valid only if there are no spurious contacts for  $t \in ]0, T[$ . There is no analytical way of verifying this, although the analytical expression of  $\mathbf{z}(t)$  exists. One should then tabulate  $\mathbf{z}(t_i)$  for  $t_i \in ]0, T[$  and verify that,  $\forall i$ , the first

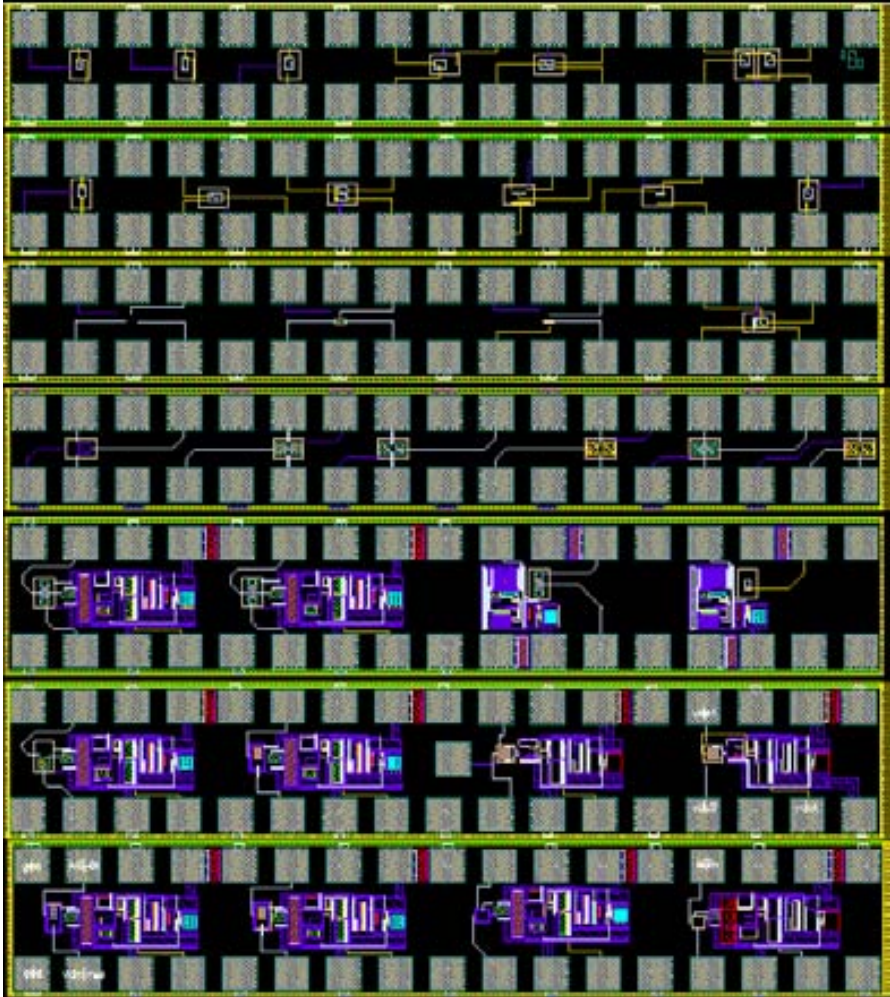
component of  $\mathbf{z}(t_i)$  (corresponding to  $a_1(t_i)$ ) is smaller than  $\gamma$ . If the condition is met, and [A.11](#) and [A.12](#) as well, then a limit cycle with period  $T$ , half period  $T/2$ , delay  $\tau$  and no supplementary impacts between 0 and  $T$  may take place in the system. By setting  $\gamma$  and sweeping a range of values of  $T$ , it is then possible to plot curves giving  $T$  versus  $V_{on}$ . Note that the procedure described above can be extended to the case when several impacts take place during a period. However, this requires solving a nonlinear set of equations and quickly becomes impractical when the number of impacts is more than a few.

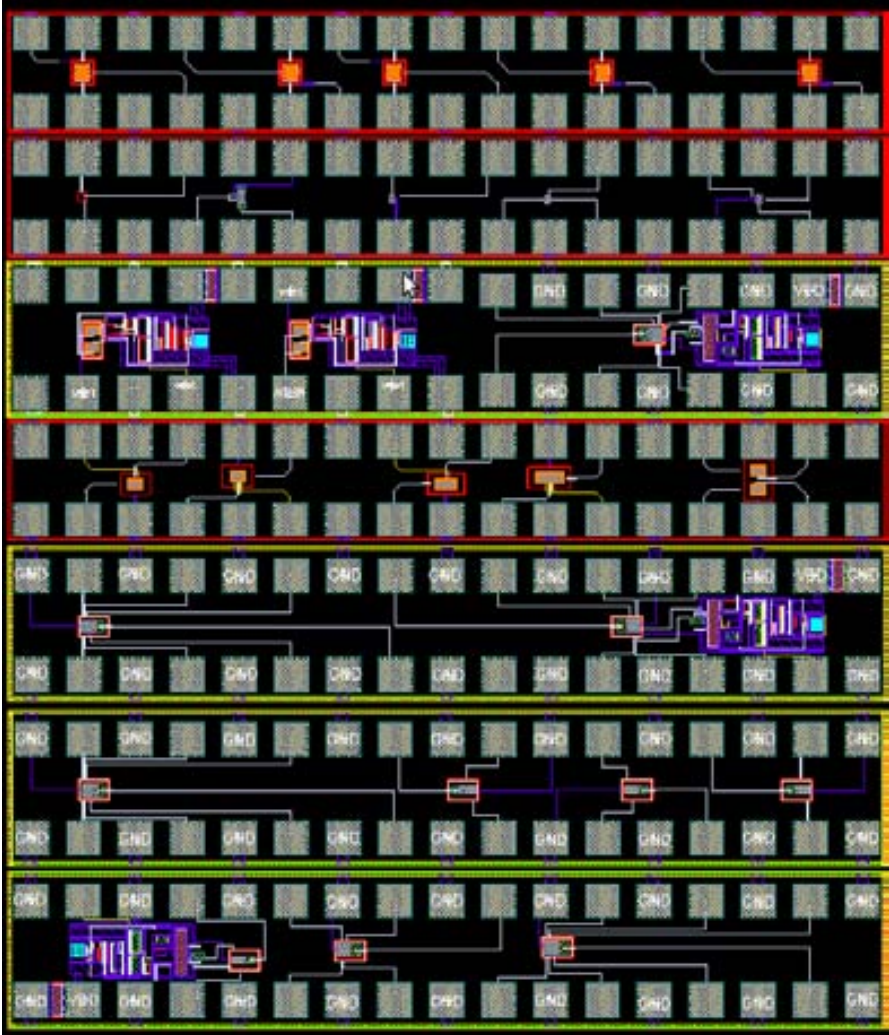
# Appendix B

## RUNs description

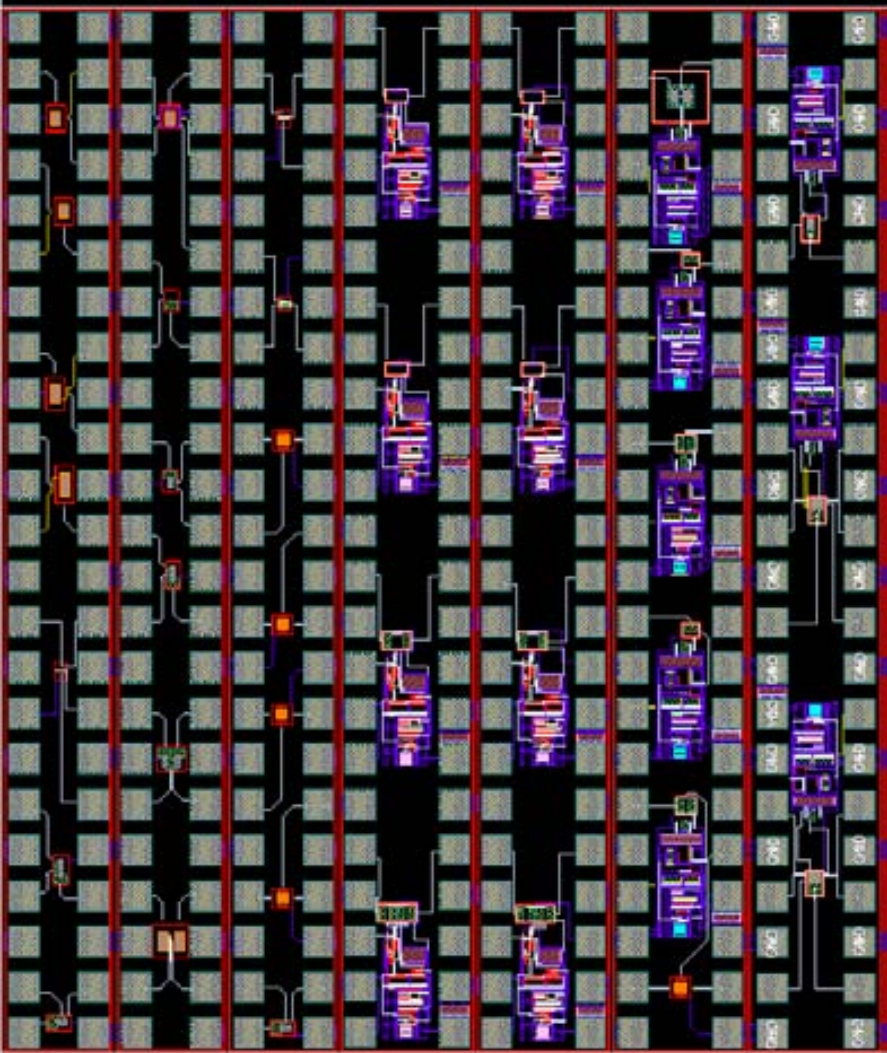
In this annex all the chips submitted during this thesis are summarized:

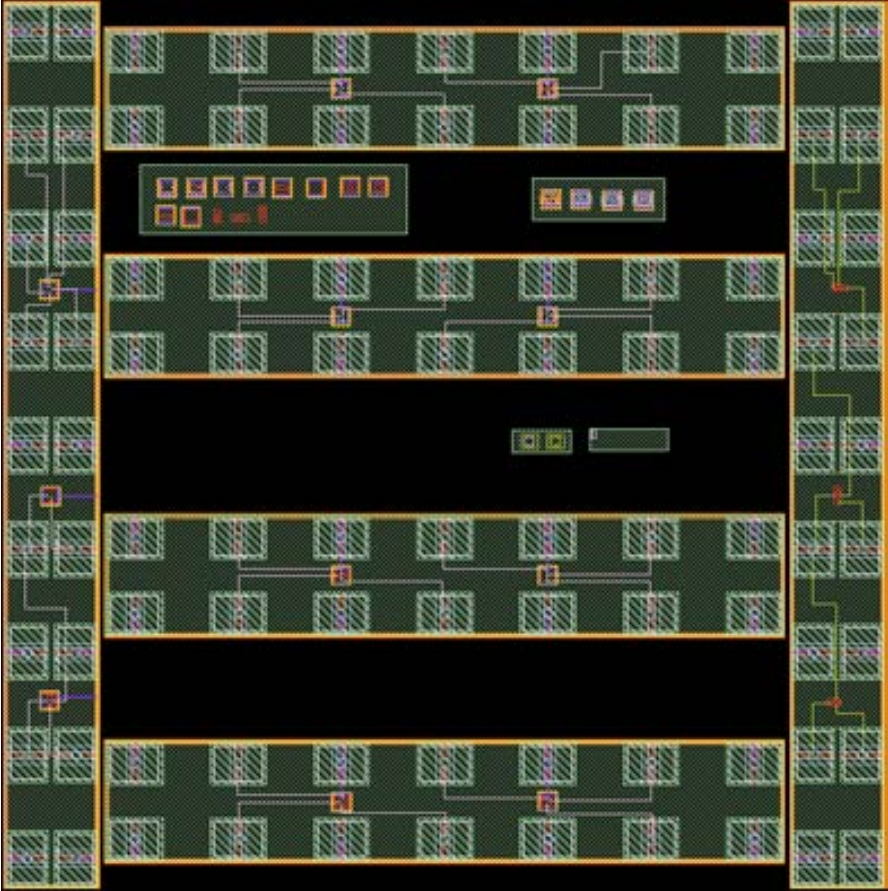
RUN July 2011	
<b>Technology:</b> ST CMOS065:6M-4X-0Y-2Z	<b>Area:</b> 1270 $\mu\text{m}$ x 1203 $\mu\text{m}$
<b>Objective:</b> (First design in ST 65nm) Study the feasibility to develop CMOS-MEMS devices in ST 65nm. Resonator were implemented in M7,M5,M1 and poly, with minimum dimensions. A deep study of the releasing process was performed using this RUN CHIPS.	
	

RUN September 2012	
<b>Technology:</b> AMSS35D4M2	<b>Area:</b> 2470 $\mu\text{m}$ x 2785 $\mu\text{m}$
<b>Objective:</b> Develop low operating switches using the MIM module of this AMS technology. Cantilevers and torsional designs were implemented	
	

RUN December 2012	
<b>Technology:</b> AMSC35B4C3	<b>Area:</b> 2500 $\mu\text{m}$ x 2940 $\mu\text{m}$
<b>Objective:</b> Develop MEMS switches using the BEOL metal layer of AMS 0.35 CMOS technology. Two different approaches were followed: M4 as structural layer or M4-VIA3-M3 stack.	
	



RUN March 2013	
Technology: AMSC35B4C3	Area: 2795 $\mu\text{m}$ x 3320 $\mu\text{m}$
Objective: Develop RGT devices using a CMOS-MEMS approach.	
	

RUN May 2013	
<b>Technology:</b> ST CMOS065:6M-4X-0Y-2Z	<b>Area:</b> 1275 $\mu\text{m}$ x 1280 $\mu\text{m}$
<b>Objective:</b> Develop NEMS structures using a CMOS-MEMS approach. After develop a post-CMOS releasing process in the previous ST RUN, in this design we focus on the design of minimum dimensions and gaps (anchoring the drivers with the top layer) switches and resonators in M1 and poly layers.	
	





# Bibliography

- [1] International technology roadmap of semiconductors. Technical report, 2011.
- [2] Robert G Knobel and Andrew N Cleland. Nanometre-scale displacement sensing using a single electron transistor. *Nature*, 424(6946):291–293, 2003.
- [3] JL Arlett, JR Maloney, B Gudlewski, M Muluneh, and ML Roukes. Self-sensing micro-and nanocantilevers with attonewton-scale force resolution. *Nano Letters*, 6(5):1000–1006, 2006.
- [4] K Jensen, Kwanpyo Kim, and A Zettl. An atomic-resolution nanomechanical mass sensor. *Nature nanotechnology*, 3(9):533–537, 2008.
- [5] Julien Chaste, A Eichler, J Moser, G Ceballos, R Rurali, and A Bachtold. A nanomechanical mass sensor with yoctogram resolution. *Nature nanotechnology*, 7(5):301–304, 2012.
- [6] Andrew N Cleland and Michael L Roukes. A nanometre-scale mechanical electrometer. *Nature*, 392(6672):160–162, 1998.
- [7] KL Ekinci and ML Roukes. Nanoelectromechanical systems. *Review of scientific instruments*, 76(6):061101, 2005.
- [8] V. Kaajakari. *Practical MEMS*. Small Gear Publishing, 2009. ISBN 9780982299104.
- [9] Jonathan Bernstein, Raanan Miller, William Kelley, and Paul Ward. Low-noise MEMS vibration sensor for geophysical applications. *Microelectromechanical Systems, Journal of*, 8(4):433–438, 1999.

- [10] CM Jha, G Bahl, R Melamud, SA Chandorkar, MA Hopcroft, B Kim, M Agarwal, J Salvia, H Mehta, and TW Kenny. CMOS-compatible dual-resonator MEMS temperature sensor with milli-degree accuracy. In *Proceedings of the Solid-State Sensors, Actuators and Microsystems Conference*, pages 229–232, 2007.
- [11] Liwei Lin and Weijie Yun. MEMS pressure sensors for aerospace applications. In *Aerospace Conference, 1998 IEEE*, volume 1, pages 429–436. IEEE, 1998.
- [12] Chih-Ming Ho and Yu-Chong Tai. Micro-electro-mechanical-systems (MEMS) and fluid flows. *Annual Review of Fluid Mechanics*, 30(1):579–612, 1998.
- [13] Qing Wan, QH Li, YJ Chen, Ta-Hung Wang, XL He, JP Li, and CL Lin. Fabrication and ethanol sensing characteristics of zno nanowire gas sensors. *Applied Physics Letters*, 84(18):3654–3656, 2004.
- [14] CS Lam. A review of the recent development of MEMS and crystal oscillators and their impacts on the frequency control products industry. In *Ultrasonics Symposium, 2008. IUS 2008. IEEE*, pages 694–704. IEEE, 2008.
- [15] Jiangfeng Wu, Gary K Fedder, and L Richard Carley. A low-noise low-offset capacitive sensing amplifier for a  $50\text{-}\mu\text{g}/\sqrt{\text{Hz}}$  monolithic cmos mems accelerometer. *Solid-State Circuits, IEEE Journal of*, 39(5):722–730, 2004.
- [16] KL Ekinici, YT Yang, and ML Roukes. Ultimate limits to inertial mass sensing based upon nanoelectromechanical systems. *Journal of applied physics*, 95(5):2682–2689, 2004.
- [17] B Lassagne, D Garcia-Sanchez, A Aguasca, and A Bachtold. Ultrasensitive mass sensing with a nanotube electromechanical resonator. *Nano letters*, 8(11):3735–3738, 2008.

- [18] Rongrui He, XL Feng, ML Roukes, and Peidong Yang. Self-transducing silicon nanowire electromechanical systems at room temperature. *Nano Letters*, 8(6):1756–1761, 2008.
- [19] AK Naik, MS Hanay, WK Hiebert, XL Feng, and ML Roukes. Towards single-molecule nanomechanical mass spectrometry. *Nature nanotechnology*, 4(7):445–450, 2009.
- [20] J Verd, A Uranga, G Abadal, J Teva, F Torres, Francesc Pérez-Murano, J Fraxedas, J Esteve, and N Barniol. Monolithic mass sensor fabricated using a conventional technology with attogram resolution in air conditions. *Applied physics letters*, 91(1):013501, 2007.
- [21] J. Verd. *Monolithic CMOS–MEMS resonant beams for ultrasensitive mass detection*. PhD thesis, 2008.
- [22] Stephen D. Senturia. *Microsystem Design*. Springer, New York, NY, USA, 1st edition, 2000. ISBN 0792372468, 9780792372462.
- [23] Ali H Nayfeh, Mohammad I Younis, and Eihab M Abdel-Rahman. Reduced-order models for MEMS applications. *Nonlinear dynamics*, 41(1-3):211–236, 2005.
- [24] Jerome Juillard, Grégory Arndt, and Eric Colinet. Modeling of micromachined beams subject to nonlinear restoring or damping forces. *Microelectromechanical Systems, Journal of*, 20(1):165–177, 2011.
- [25] RRA Syms, H Zou, J Yao, D Uttamchandani, and J Stagg. Scalable electrothermal MEMS actuator for optical fibre alignment. *Journal of Micromechanics and Microengineering*, 14(12):1633, 2004.
- [26] H Guckel. High-aspect-ratio micromachining via deep x-ray lithography. *Proceedings of the IEEE*, 86(8):1586–1593, 1998.
- [27] Hee-Chul Lee, Jae-Yeong Park, and Jong-Uk Bu. Piezoelectrically actuated RF MEMS DC contact switches with low voltage operation. *Microwave and Wireless Components Letters, IEEE*, 15(4):202–204, 2005.

- [28] JL Lopez, J Verd, J Teva, G Murillo, J Giner, F Torres, A Uranga, G Abadal, and N Barniol. Integration of RF-MEMS resonators on submicrometric commercial CMOS technologies. *Journal of Micromechanics and Microengineering*, 19(1):015002, 2009.
- [29] U Krishnamoorthy, RH Olsson III, Gregory R Bogart, MS Baker, DW Carr, TP Swiler, and PJ Clews. In-plane MEMS-based nano-g accelerometer with sub-wavelength optical resonant sensor. *Sensors and Actuators A: Physical*, 145:283–290, 2008.
- [30] Mo Li, Hong X Tang, and Michael L Roukes. Ultra-sensitive NEMS-based cantilevers for sensing, scanned probe and very high-frequency applications. *Nature nanotechnology*, 2(2):114–120, 2007.
- [31] Gianluca Piazza, Philip J Stephanou, and Albert P Pisano. Piezoelectric aluminum nitride vibrating contour-mode MEMS resonators. *Microelectromechanical Systems, Journal of*, 15(6):1406–1418, 2006.
- [32] H.C. Nathanson, W.E. Newell, R.A. Wickstrom, and Jr. Davis, J.R. The resonant gate transistor. *Electron Devices, IEEE Transactions on*, 14(3): 117–133, Mar 1967. ISSN 0018-9383. doi: 10.1109/T-ED.1967.15912.
- [33] Dana Weinstein and Sunil A Bhawe. The resonant body transistor. *Nano letters*, 10(4):1234–1237, 2010.
- [34] CT-C Nguyen. Micromechanical resonators for oscillators and filters. In *Ultrasonics Symposium, 1995. Proceedings., 1995 IEEE*, volume 1, pages 489–499. IEEE, 1995.
- [35] Aditya Bansal, Bipul Chandra Paul, and Kaushik Roy. An analytical fringe capacitance model for interconnects using conformal mapping. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 25(12):2765–2774, 2006.

- [36] Vincent Pott, Hei Kam, Rhesa Nathanael, Jaeseok Jeon, Elad Alon, and Tsu-Jae King Liu. Mechanical computing redux: relays for integrated circuit applications. *Proceedings of the IEEE*, 98(12):2076–2094, 2010.
- [37] Ben G Streetman and Sanjay Banerjee. *Solid state electronic devices*, volume 4. Prentice Hall Englewood Cliffs, NJ, 1995.
- [38] Yannis Tsividis. *Operation and Modeling of the MOS Transistor*. McGraw-Hill, Inc., New York, NY, USA, 1987. ISBN 007065381X.
- [39] Hamed F Dadgour and Kaustav Banerjee. Hybrid NEMS-CMOS integrated circuits: A novel strategy for energy-efficient designs. *Computers & Digital Techniques, IET*, 3(6):593–608, 2009.
- [40] Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic. *Digital integrated circuits- A design perspective*. Prentice Hall, 2ed edition, 2004.
- [41] George Sery, Shekhar Borkar, and Vivek De. Life is CMOS: why chase the life after? In *Proceedings of the 39th annual Design Automation Conference*, pages 78–83. ACM, 2002.
- [42] Kathy Boucart and Adrian Mihai Ionescu. Double-gate tunnel FET with high- $\kappa$  gate dielectric. *Electron Devices, IEEE Transactions on*, 54(7):1725–1733, 2007.
- [43] Kailash Gopalakrishnan, Peter B Griffin, and James D Plummer. I-MOS: A novel semiconductor device with a subthreshold slope lower than  $kt/q$ . In *Electron Devices Meeting, 2002. IEDM'02. International*, pages 289–292. IEEE, 2002.
- [44] George C Chase. History of mechanical computing machinery. In *Proceedings of the ACM National Meeting*, pages 1–28, 1952.
- [45] JC Fisher and Ivar Giaever. Tunneling through thin insulating layers. *Journal of Applied Physics*, 32(2):172–177, 2004.
- [46] JF Scott. Device physics of ferroelectric memories. *Ferroelectrics*, 183(1): 51–63, 1996.

- [47] Owen Y Loh and Horacio D Espinosa. Nanoelectromechanical contact switches. *Nature nanotechnology*, 7(5):283–295, 2012.
- [48] Jeong Oen Lee, Yong-Ha Song, Min-Wu Kim, Min-Ho Kang, Jae-Sub Oh, Hyun-Ho Yang, and Jun-Bo Yoon. A sub-1-volt nanoelectromechanical switching device. *Nature nanotechnology*, 8(1):36–40, 2013.
- [49] XL Feng, MH Matheny, CA Zorman, M Mehregany, and ML Roukes. Low voltage nanoelectromechanical switches based on silicon carbide nanowires. *Nano letters*, 10(8):2891–2896, 2010.
- [50] Rhesa Nathanael, Vincent Pott, Hei Kam, Jaeseok Jeon, and Tsu-Jae King Liu. 4-terminal relay technology for complementary logic. In *Electron Devices Meeting (IEDM), 2009 IEEE International*, pages 1–4. IEEE, 2009.
- [51] Gabriel Abadal, Zachary James Davis, Bjarne Helbo, X Borrise, R Ruiz, Anja Boisen, F Campabadal, J Esteve, E Figueras, F Perez-Murano, et al. Electromechanical model of a resonating nano-cantilever-based sensor for high-resolution and high-sensitivity mass detection. *Nanotechnology*, 12(2):100, 2001.
- [52] Woo Young Choi, Hei Kam, Donovan Lee, Joanna Lai, and Tsu-Jae King Liu. Compact nano-electro-mechanical non-volatile memory (NEMory) for 3D integration. In *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pages 603–606. IEEE, 2007.
- [53] In-Hyuk Choi, Min-Sang Kim, Sung-min Kim, Sung-young Lee, Ji-Myoung Lee, and Eun-Jung Yun. Multibit electro-mechanical memory device having cantilever electrodes, July 5 2011.
- [54] Huilong Zhu. Nanoelectromechanical digital inverter, November 3 2009. US Patent 7,612,270.
- [55] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits Revised Edition*. Oxford University Press, Inc., New York, NY, USA, 5th edition, 2007. ISBN 0195338839, 9780195338836.

- [56] Anupama B Kaul, Eric W Wong, Larry Epp, and Brian D Hunt. Electromechanical carbon nanotube switches for high-frequency applications. *Nano letters*, 6(5):942–947, 2006.
- [57] K Akarvardar, D Elata, R Parsa, GC Wan, K Yoo, J Provine, P Peumans, RT Howe, and H-SP Wong. Design considerations for complementary nanoelectromechanical logic gates. In *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pages 299–302. IEEE, 2007.
- [58] Ming Liu, Haigang Yang, Sansiri Tanachutiwat, and Wei Wang. FPGA based on integration of carbon nanorelays and CMOS devices. In *Nanoscale Architectures, 2009. NANOARCH'09. IEEE/ACM International Symposium on*, pages 61–64. IEEE, 2009.
- [59] Fred Chen, Hei Kam, Dejan Markovic, Tsu-Jae King Liu, Vladimir Stojanovic, and Elad Alon. Integrated circuit design with NEM relays. In *Proceedings of the 2008 IEEE/ACM International Conference on Computer-Aided Design*, pages 750–757. IEEE Press, 2008.
- [60] Tsu-Jae King Liu, Jaeseok Jeon, Hei Kam, et al. Prospects for MEM logic switch technology. In *2010 International Electron Devices Meeting*, pages 18–3, 2010.
- [61] Hamed Dadgour, Muhammad M Hussain, and Kaustav Banerjee. A new paradigm in the design of energy-efficient digital circuits using laterally-actuated double-gate nems. In *Proceedings of the 16th ACM/IEEE international symposium on Low power electronics and design*, pages 7–12. ACM, 2010.
- [62] Soogine Chong, Kerem Akarvardar, Roozbeh Parsa, Jun-Bo Yoon, Roger T Howe, Subhasish Mitra, and H-SP Wong. Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage. In *Computer-Aided Design-Digest of Technical Papers, 2009. ICCAD 2009. IEEE/ACM International Conference on*, pages 478–484. IEEE, 2009.

- [63] Woo Young Choi, Taro Osabe, and Tsu-Jae King Liu. Nano-electromechanical nonvolatile memory (NEMory) cell design and scaling. *Electron Devices, IEEE Transactions on*, 55(12):3482–3488, 2008.
- [64] Jaeseok Jeon, Vincent Pott, Hei Kam, Rhesa Nathanael, Elad Alon, and Tsu-Jae King Liu. Perfectly complementary relay design for digital logic applications. *Electron Device Letters, IEEE*, 31(4):371–373, 2010.
- [65] Te-Hao Lee, Swarup Bhunia, and Mehran Mehregany. Electromechanical computing at 500 c with silicon carbide. *Science*, 329(5997):1316–1318, 2010.
- [66] You Qian, Liang Lou, Minglin Julius Tsai, and Chengkuo Lee. A dual-silicon-nanowires based u-shape nanoelectromechanical switch with low pull-in voltage. *Applied Physics Letters*, 100(11):113102, 2012.
- [67] Daniel Grogg, Ute Drechsler, Armin Knoll, Urs Duerig, Yu Pu, Christoph Hagleitner, and Michel Despont. Curved in-plane electromechanical relay for low power logic applications. *Journal of Micromechanics and Microengineering*, 23(2):025024, 2013.
- [68] Wenfeng Xiang and Chengkuo Lee. Nanoelectromechanical torsion switch of low operation voltage for nonvolatile memory application. *Applied Physics Letters*, 96(19):193113, 2010.
- [69] Joshua Rubin, Ravishankar Sundararaman, Moonkyung Kim, and Sandip Tiwari. A low-voltage torsion nanorelay. *Electron Device Letters, IEEE*, 32(3):414–416, 2011.
- [70] Roozbeh Parsa, W Scott Lee, Mohammad Shavezipur, J Provine, Roya Maboudian, Subhasish Mitra, HP Wong, and Roger T Howe. Laterally actuated platinum-coated polysilicon NEM relays. *Microelectromechanical Systems, Journal of*, 22(3):768–778, 2013.
- [71] Tina He, Vaishnavi Ranganathan, Rui Yang, Srihari Rajgopal, Swarup Bhunia, Mehran Mehregany, and Philip X-L Feng. Time-domain AC characterization of silicon carbide (SiC) nanoelectromechanical switches toward



- high-speed operations. In *Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII), 2013 Transducers & Eurosensors XXVII: The 17th International Conference on*, pages 669–672. IEEE, 2013.
- [72] SN Cha, JE Jang, Y Choi, GAJ Amaratunga, D-J Kang, DG Hasko, JE Jung, and JM Kim. Fabrication of a nanoelectromechanical switch using a suspended carbon nanotube. *Applied Physics Letters*, 86(8):083105, 2005.
- [73] JE Jang, SN Cha, Y Choi, TP Butler, DJ Kang, DG Hasko, JE Jung, YW Jin, JM Kim, and GAJ Amaratunga. Nanoelectromechanical switch with low voltage drive. *Applied Physics Letters*, 93(11):113105, 2008.
- [74] Soogine Chong, Byoungil Lee, Kokab B Parizi, J Provine, Subhasish Mitra, Roger T Howe, and H-SP Wong. Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, pages 30–5. IEEE, 2011.
- [75] Nicolas Abelé, R Fritschi, K Boucart, F Casset, P Ancey, and Adrian Mihai Ionescu. Suspended-gate MOSFET: bringing new MEMS functionality into solid-state MOS transistor. In *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pages 479–481. IEEE, 2005.
- [76] Weon Wi Jang, Jeong Oen Lee, Jun-Bo Yoon, Min-Sang Kim, Ji-Myoung Lee, Sung-Min Kim, Keun-Hwi Cho, Dong-Won Kim, Donggun Park, and Won-Seong Lee. Fabrication and characterization of a nanoelectromechanical switch with 15-nm-thick suspension air gap. *Applied Physics Letters*, 92(10):103110, 2008.
- [77] Jana Andzane, Nikolay Petkov, Aleksandrs I Livshits, John J Boland, Justin D Holmes, and Donats Erts. Two-terminal nanoelectromechanical devices based on germanium nanowires. *Nano letters*, 9(5):1824–1829, 2009.

- [78] Jan Bienstman, Joos Vandewalle, and Robert Puers. The autonomous impact resonator: a new operating principle for a silicon resonant strain gauge. *Sensors and Actuators A: Physical*, 66(1):40–49, 1998.
- [79] SW Shaw. Forced vibrations of a beam with one-sided amplitude constraint: theory and experiment. *Journal of Sound and Vibration*, 99(2):199–212, 1985.
- [80] Steven Wayne Shaw and PJ Holmes. A periodically forced piecewise linear oscillator. *Journal of Sound and Vibration*, 90(1):129–155, 1983.
- [81] Yue Wu, Yi Cui, Lynn Huynh, Carl J Barrelet, David C Bell, and Charles M Lieber. Controlled growth and structures of molecular-scale silicon nanowires. *Nano Letters*, 4(3):433–436, 2004.
- [82] Zhipeng Huang, Hui Fang, and Jing Zhu. Fabrication of silicon nanowire arrays with controlled diameter, length, and density. *Advanced materials*, 19(5):744–748, 2007.
- [83] Gary K Fedder. Top-down design of MEMS. In *Proceedings of the 2000 Int. Conf. on Modeling and Simulation of Microsystems Semiconductors, Sensors and Actuators. San Diego (USA)*, volume 1, pages 7–10, 2000.
- [84] Henry Baltes, Oliver Brand, Gary K Fedder, Christofer Hierold, Jan G Korvink, and Osamu Tabata. *CMOS-MEMS: Advanced Micro and Nanosystems*. John Wiley & Sons, 2008.
- [85] JH Smith, S Montague, JJ Sniegowski, JR Murray, and PJ McWhorter. Embedded micromechanical devices for the monolithic integration of MEMS with CMOS. In *Electron Devices Meeting, 1995. IEDM'95., International*, pages 609–612. Ieee, 1995.
- [86] John A Yasaitis, Michael Judy, Tim Brosnihan, Peter M Garone, Nikolay Pokrovskiy, Debbie Sniderman, Scott Limb, Roger T Howe, Bernhard E Boser, Moorthi Palaniapan, et al. A modular process for integrating thick polysilicon MEMS devices with sub-micron CMOS. In *Micromachining and*

- Microfabrication*, pages 145–154. International Society for Optics and Photonics, 2003.
- [87] John A Geen, Steven J Sherman, John F Chang, and Stephen R Lewis. Single-chip surface micromachined integrated gyroscope with 50/h allan deviation. *IEEE Journal of Solid-State Circuits*, 37(12):1860–1866, 2002.
- [88] KH-L Chau, SR Lewis, Y Zhao, RT Howe, SF Bart, and RG Marcheselli. An integrated force-balanced capacitive accelerometer for low-g applications. *Sensors and Actuators A: Physical*, 54(1):472–476, 1996.
- [89] Christofer Hierold. Intelligent CMOS sensors. In *Micro Electro Mechanical Systems, 2000. MEMS 2000. The Thirteenth Annual International Conference on*, pages 1–6. IEEE, 2000.
- [90] Gary K Fedder, Suresh Santhanam, Michael L Reed, Steve C Eagle, David F Guillou, Mike S-C Lu, and L Richard Carley. Laminated high-aspect-ratio microstructures in a conventional CMOS process. In *Micro Electro Mechanical Systems, 1996, MEMS'96, Proceedings. An Investigation of Micro Structures, Sensors, Actuators, Machines and Systems. IEEE, The Ninth Annual International Workshop on*, pages 13–18. IEEE, 1996.
- [91] J Verd, A Uranga, G Abadal, JL Teva, F Torres, J Lopez, F Perez-Murano, J Esteve, and N Barniol. Monolithic CMOS-MEMS oscillator circuit for sensing in the attogram range. *IEEE electron device letters*, 29(2):146–148, 2008.
- [92] Wen-Chien Chen, Weileun Fang, and Sheng-Shian Li. High-integrated CMOS-MEMS resonators with deep-submicrometer gaps and quasi-linear frequency tuning. *Microelectromechanical Systems, Journal of*, 21(3):688–701, 2012.
- [93] DR Sparks, X Huang, W Higdon, and JD Johnson. Angular rate sensor and accelerometer combined on the same micromachined CMOS chip. *Microsystem technologies*, 4(3):139–142, 1998.

- [94] Peter F Van Kessel, Larry J Hornbeck, Robert E Meier, and Michael R Douglass. A MEMS-based projection display. *Proceedings of the IEEE*, 86(8):1687–1704, 1998.
- [95] Maxim K Zalalutdinov, Joshua D Cross, Jeffrey W Baldwin, Bojan R Ilic, Wenzhe Zhou, Brian H Houston, and Jeevak M Parpia. CMOS-integrated RF MEMS resonators. *Microelectromechanical Systems, Journal of*, 19(4):807–815, 2010.
- [96] MA Lemkin, TN Juneau, WA Clark, TA Roessig, and TJ Brosnihan. A low-noise digital accelerometer using integrated SOI-MEMS technology. *Tech. Digest, Transducers*, 99:1294–1297, 1999.
- [97] CT-C Nguyen and Roger T Howe. An integrated cmos micromechanical resonator high-Q oscillator. *Solid-State Circuits, IEEE Journal of*, 34(4):440–455, 1999.
- [98] Andrea Elke Franke, John M Heck, Tsu-Jae King, and Roger T Howe. Polycrystalline silicon-germanium films for integrated microsystems. *Microelectromechanical Systems, Journal of*, 12(2):160–171, 2003.
- [99] Radhika Marathe, Wentao Wang, and Dana Weinstein. Si-based unreleased hybrid MEMS-CMOS resonators in 32nm technology. In *Micro Electro Mechanical Systems (MEMS), 2012 IEEE 25th International Conference on*, pages 729–732. IEEE, 2012.
- [100] R. Marathe, B. Bahr, W. Wang, Z. Mahmood, L. Daniel, and D. Weinstein. Resonant body transistors in ibm’s 32 nm soi cmos technology. *Microelectromechanical Systems, Journal of*, 23(3):636–650, June 2014. ISSN 1057-7157. doi: 10.1109/JMEMS.2013.2283720.
- [101] J Giner, A Uranga, JL Muñoz-Gamarra, E Marigó, and N Barniol. VHF monolithically integrated CMOS-MEMS longitudinal bulk acoustic resonator. *Electronics letters*, 48(9):514–516, 2012.

- [102] Vinayak Pachkawade, Ming-Huang Li, Cheng-Syun Li, and Sheng-Shian Li. A CMOS-MEMS resonator integrated system for oscillator application. *Sensors Journal, IEEE*, 13(8):2882–2889, 2013.
- [103] Yu-Chia Liu, Ming-Han Tsai, Wen-Chien Chen, Sheng-Shian Li, and Weileun Fang. High-Q, large-stopband-rejection integrated CMOS-MEMS oxide resonators with embedded metal electrodes. In *Solid-State Sensors, Actuators and Microsystems Conference (TRANSDUCERS), 2011 16th International*, pages 934–937. IEEE, 2011.
- [104] C-C Lo and Gary K Fedder. On-chip high quality factor CMOS-MEMS silicon-fin resonators. In *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, pages 2449–2452. IEEE, 2007.
- [105] Jaume Verd, G Abadal, J Teva, M Villarroja Gaudó, Arantxa Uranga, Xavier Borrisé, Francesca Campabadal, Jaume Esteve, E Figueras Costa, Francesc Pérez-Murano, et al. Design, fabrication, and characterization of a submicroelectromechanical resonator with monolithically integrated CMOS readout circuit. *Microelectromechanical Systems, Journal of*, 14(3):508–519, 2005.
- [106] J.Giner-A.Uranga N.Barniol E. Marigo, J.L. Muñoz-Gamarra. A 230mhz CMOS-MEMS bulk acoustic wave resonator. *Microelectronic Engineering*, 98(0):458 – 462, 2012. ISSN 0167-9317. doi: <http://dx.doi.org/10.1016/j.mee.2012.07.102>.
- [107] J Giner, A Uranga, F Torres, E Marigo, and N Barniol. Fully CMOS integrated bandpass filter based on mechanical coupling of two RF MEMS resonators. *Electronics letters*, 46(9):640–641, 2010.
- [108] Joan Lluís Lopez, Jaume Verd, Arantxa Uranga, Joan Giner, Gonzalo Murillo, Francesc Torres, Gabriel Abadal, and Nuria Barniol. A CMOS–MEMS rf-tunable bandpass filter based on two high-22-mhz polysilicon

- clamped-clamped beam resonators. *Electron Device Letters, IEEE*, 30(7): 718–720, 2009.
- [109] J Verd, A Uranga, J Teva, JL Lopez, F Torres, J Esteve, G Abadal, F Perez-Murano, and N Barniol. Integrated CMOS-MEMS with on-chip readout electronics for high-frequency applications. *Electron Device Letters, IEEE*, 27(6):495–497, 2006.
- [110] Wen-Chien Chen, Weileun Fang, and Sheng-Shian Li. A generalized CMOS-MEMS platform for micromechanical resonators monolithically integrated with circuits. *Journal of Micromechanics and Microengineering*, 21(6): 065012, 2011.
- [111] Wen-Chien Chen, Ming-Huang Li, Weileun Fang, and Sheng-Shian Li. Realizing deep-submicron gap spacing for CMOS-MEMS resonators with frequency tuning capability via modulated boundary conditions. In *Micro Electro Mechanical Systems (MEMS), 2010 IEEE 23rd International Conference on*, pages 735–738. IEEE, 2010.
- [112] Cheng-Syun Li, Li-Jen Hou, and Sheng-Shian Li. Advanced CMOS-MEMS resonator platform. *Electron Device Letters, IEEE*, 33(2):272–274, 2012.
- [113] Wen-Chien Chen, Weileun Fang, and Sheng-Shian Li. VHF CMOS-MEMS oxide resonators with  $Q_i$  10,000. In *Frequency Control Symposium (FCS), 2012 IEEE International*, pages 1–4. IEEE, 2012.
- [114] Huikai Xie and Gary K Fedder. Vertical comb-finger capacitive actuation and sensing for CMOS-MEMS. *Sensors and Actuators A: Physical*, 95(2): 212–221, 2002.
- [115] Fang Chen, Jay Brotz, Umut Arslan, Chiung-Cheng Lo, Tamal Mukherjee, and Gary K Fedder. CMOS-MEMS resonant RF mixer-filters. In *Micro Electro Mechanical Systems, 2005. MEMS 2005. 18th IEEE International Conference on*, pages 24–27. IEEE, 2005.

- [116] Chiung-Cheng Lo, Fang Chen, and GK Fedder. Integrated HF CMOS-MEMS square-frame resonators with on-chip electronics and electrothermal narrow gap mechanism. In *Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS'05. The 13th International Conference on*, volume 2, pages 2074–2077. IEEE, 2005.
- [117] I Bargatin, EB Myers, JS Aldridge, C Marcoux, P Brianceau, L Duraffourg, E Colinet, S Hentz, P Andreucci, and ML Roukes. Large-scale integration of nanoelectromechanical systems for gas sensing applications. *Nano letters*, 12(3):1269–1274, 2012.
- [118] MS Hanay, S Kelber, AK Naik, D Chi, S Hentz, EC Bullard, E Colinet, L Duraffourg, and ML Roukes. Single-protein nanomechanical mass spectrometry in real time. *Nature nanotechnology*, 7(9):602–608, 2012.
- [119] St microelectronics. <http://www.st.com/>.
- [120] JL López, J Giner, G Murillo, F Torres, E Marigó, A Uranga, G Abadal, and N Barniol. Third-mode 48mhz free-free beam resonator used as a RF balun. *Microelectronic Engineering*, 87(5):1256–1258, 2010.
- [121] Marie-Ange Eyoum, N Hoivik, C Jahnes, J Cotte, and Xiao-Hu Liu. Analysis and modeling of curvature in copper-based MEMS structures fabricated using CMOS interconnect technology. In *Solid-State Sensors, Actuators and Microsystems, 2005. Digest of Technical Papers. TRANSDUCERS'05. The 13th International Conference on*, volume 1, pages 764–767. IEEE, 2005.
- [122] XL Feng, Rongrui He, Peidong Yang, and ML Roukes. Very high frequency silicon nanowire electromechanical resonators. *Nano Letters*, 7(7):1953–1959, 2007.
- [123] Bei Peng, Mark Locascio, Peter Zapol, Shuyou Li, Steven L Mielke, George C Schatz, and Horacio D Espinosa. Measurements of near-ultimate strength for multiwalled carbon nanotubes and irradiation-induced crosslinking improvements. *Nature nanotechnology*, 3(10):626–631, 2008.

- [124] Europractice. <http://www.europractice-ic.com/>.
- [125] Cmp. <http://cmp.imag.fr/>.
- [126] Y. Nishi and R. Doering. *Handbook of Semiconductor Manufacturing Technology, Second Edition*. Taylor & Francis, 2007. ISBN 9781420017663.
- [127] Harry JM Veendrick. *Nanometer CMOS ICs: From Basics to ASICs*. Springer, 2010.
- [128] Kirt R Williams and Richard S Muller. Etch rates for micromachining processing. *Microelectromechanical Systems, Journal of*, 5(4):256–269, 1996.
- [129] E. Marigo. *Monolithic packaging and transduction approaches for CMOS–MEMS resonator*. PhD thesis, 2012.
- [130] E.Marigo. J.L. Munoz-Gamarra. G. Vidal-Alvarez. F. Torres. N. Barniol. Characterization of a CMOS-NEMS resonator as a DC switch. In *International seminar on nanomechanical systems*. Toulouse, France, 2011.
- [131] JL Lopez, Jordi Teva, Arantxa Uranga, Francesc Torres, Jaume Verd, Gabriel Abadal, Nuria Barniol, Jaume Esteve, and Francesc Pérez-Murano. Mixing in a 220mhz CMOS-MEMS. In *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, pages 2630–2633. IEEE, 2007.
- [132] D Karabacak, T Kouh, CC Huang, and KL Ekinici. Optical knife-edge technique for nanomechanical displacement detection. *Applied physics letters*, 88(19):193122, 2006.
- [133] Weon Wi Jang, Jun-Bo Yoon, Min-Sang Kim, Ji-Myoung Lee, Sung-Min Kim, Eun-Jung Yoon, Keun Hwi Cho, Sung-Young Lee, In-Hyuk Choi, Dong-Won Kim, et al. NEMS switch with 30nm-thick beam and 20nm-thick air-gap for high density non-volatile memory applications. *Solid-State Electronics*, 52(10):1578–1583, 2008.
- [134] XM Zhang, FS Chau, C Quan, YL Lam, and AQ Liu. A study of the static characteristics of a torsional micromirror. *Sensors and Actuators A: Physical*, 90(1):73–81, 2001.



- [135] ROE Vijgen and JH Dautzenberg. Mechanical measurement of the residual stress in thin PVD films. *Thin Solid Films*, 270(1):264–269, 1995.
- [136] D Molinero, R Comulada, and L Castaner. Dielectric charge measurements in capacitive microelectromechanical switches. *Applied physics letters*, 89(10):103506, 2006.
- [137] D Molinero, N Abelé, L Castañer, and AM Ionescu. Oxide charging and memory effects in suspended-gate FET. In *Micro Electro Mechanical Systems, 2008. MEMS 2008. IEEE 21st International Conference on*, pages 685–688. IEEE, 2008.
- [138] J Iijima, J-W Lim, S-H Hong, S Suzuki, K Mimura, and M Isshiki. Native oxidation of ultra high purity cu bulk and thin films. *Applied Surface Science*, 253(5):2825–2829, 2006.
- [139] E Marigo, JL Lopez, G Murillo, F Torres, J Giner, A Uranga, G Abadal, J Esteve, and N Barniol. Zero-level packaging of MEMS in standard CMOS technology. *Journal of Micromechanics and Microengineering*, 20(6):064009, 2010.
- [140] Ali Husain, J Hone, Henk W Ch Postma, XMH Huang, T Drake, Mladen Barbic, Axel Scherer, and ML Roukes. Nanowire-based very-high-frequency electromechanical resonator. *Applied Physics Letters*, 83(6):1240–1242, 2003.
- [141] HB Peng, CW Chang, S Aloni, TD Yuzvinsky, and A Zettl. Ultrahigh frequency nanotube resonators. *Phys. Rev. Lett*, 97(8):087203, 2006.
- [142] Yuan Xie, Sheng-Shian Li, Yu-Wei Lin, Zeying Ren, and CT-C Nguyen. 1.52-ghz micromechanical extensional wine-glass mode ring resonators. *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, 55(4):890–907, 2008.
- [143] Dana Weinstein and Sunil A Bhave. Piezoresistive sensing of a dielectrically actuated silicon bar resonator. In *Solid-State Sensors, Actuators, and Microsystems Workshop*, pages 368–371, 2008.

- [144] AN Cleland, M Pophristic, and I Ferguson. Single-crystal aluminum nitride nanomechanical resonators. *Applied Physics Letters*, 79(13):2070–2072, 2001.
- [145] Dana Weinstein and Sunil A Bhave. Internal dielectric transduction of a 4.5 ghz silicon bar resonator. In *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pages 415–418. IEEE, 2007.
- [146] N Abelé, V Pott, K Boucart, F Casset, K Séguéni, P Ancey, and AM Ionescu. Comparison of RSG-MOSFET and capacitive MEMS resonator detection. *Electronics Letters*, 41(5):242–244, 2005.
- [147] N Abele, K Séguéni, K Boucart, F Casset, B Legrand, L Buchaillot, P Ancey, and AM Ionescu. Ultra-low voltage MEMS resonator based on RSG-MOSFET. In *Micro Electro Mechanical Systems, 2006. MEMS 2006 Istanbul. 19th IEEE International Conference on*, pages 882–885. IEEE, 2006.
- [148] Chi-Hang Chin, Cheng-Syun Li, Ming-Huang Li, and Sheng-Shian Li. A CMOS-MEMS resonant gate field effect transistor. In *Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII), 2013 Transducers & Eurosensors XXVII: The 17th International Conference on*, pages 2284–2287. IEEE, 2013.
- [149] Eric Colinet, Cédric Durand, Laurent Duraffourg, Patrick Audebert, Guillaume Dumas, Fabrice Casset, Eric Ollier, Pascal Ancey, J-F Carpentier, Lionel Buchaillot, et al. Ultra-sensitive capacitive detection based on SG-MOSFET compatible with front-end cmos process. *Solid-State Circuits, IEEE Journal of*, 44(1):247–257, 2009.
- [150] Daniel Grogg, Dimitrios Tsamados, Nicoleta Diana Badila, and Adrian Mihai Ionescu. Integration of MOSFET transistors in MEMS resonators for improved output detection. In *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, pages 1709–1712. IEEE, 2007.

- [151] Daniel Grogg, Marco Mazza, Dimitrios Tsamados, and Adrian Mihai Ionescu. Multi-gate vibrating-body field effect transistor (VB-FETs). In *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, pages 1–4. IEEE, 2008.
- [152] James HT Ransley, Colm Durkan, and Ashwin A Seshia. A depletion layer actuator. In *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*, pages 1393–1396. IEEE, 2007.
- [153] Eugene Hwang and Sunil A Bhawe. PN-diode transduced 3.7-ghz silicon resonator. In *Micro Electro Mechanical Systems (MEMS), 2010 IEEE 23rd International Conference on*, pages 208–211. IEEE, 2010.
- [154] James HT Ransley, A Aziz, C Durkan, and AA Seshia. Silicon depletion layer actuators. *Applied Physics Letters*, 92(18):184103, 2008.
- [155] Laurent Duraffourg, Eric Colinet, E Ollier, S Hentz, Philippe Andreucci, Bruno Reig, and Philippe Robert. Compact and explicit physical model for lateral metal-oxide-semiconductor field-effect transistor with nanoelectromechanical system based resonant gate. *Applied Physics Letters*, 92(17):174106, 2008.
- [156] Christian C Enz, François Krummenacher, and Eric A Vittoz. An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications. *Analog integrated circuits and signal processing*, 8(1):83–114, 1995.
- [157] Matthias Bucher, Christophe Lallement, and Christian C Enz. An efficient parameter extraction methodology for the EKV MOST model. In *Micro-electronic Test Structures, 1996. ICMTS 1996. Proceedings. 1996 IEEE International Conference on*, pages 145–150. IEEE, 1996.
- [158] Nicolas ABEL. *Design and fabrication of suspended-gate MOSFETs for MEMS resonator, switch and memory applications*. PhD thesis, École Polytechnique Fédérale de Lausanne, 2007.

- 
- [159] C. Hu. *Modern Semiconductor Devices for Integrated Circuits*. Prentice Hall, 2010. ISBN 9780136085256.
- [160] B.G. Streetman and S.K. Banerjee. *Solid State Electronic Devices*. Prentice Hall Series in Solid State Physical Electronics. Pearson Prentice Hall, 2006. ISBN 9780131497269.
- [161] H. Veendrick. *Nanometer CMOS ICs: From basics to ASICs*. Springer Netherlands, 2008. ISBN 9781402083327. URL <http://books.google.es/books?id=7jUqkgEACAAJ>.
- [162] Najib Kacem, Sébastien Baguet, Sebastien Hentz, and Régis Dufour. Computational and quasi-analytical models for non-linear vibrations of resonant MEMS and NEMS sensors. *International Journal of Non-Linear Mechanics*, 46(3):532–542, 2011.
- [163] Christian C Enz and Eric A Vittoz. MOS transistor modeling for low-voltage and low-power analog IC design. *Microelectronic engineering*, 39(1):59–76, 1997.
- [164] Hei Kam, Vincent Pott, Rhesa Nathanael, Jaeseok Jeon, Elad Alon, and Tsu-Jae King Liu. Design and reliability of a micro-relay technology for zero-standby-power digital logic applications. In *Electron Devices Meeting (IEDM), 2009 IEEE International*, pages 1–4. IEEE, 2009.