Universitat Autònoma de Barcelona
Departament de Microelectrònica i Sistemes Electrònics

Low-Power and Compact CMOS Circuit Design of Digital Pixel Sensors for X-Ray Imagers

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Memòria de Tesi
presentada per optar al títol de

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Dr. Lluís Terés Terés, Científic Titular del Consejo Superior de Investigaciones Científicas, i Dr. Francesc Serra Graells, Professor Titular del Departament de Microelectrònica i Sistemes Electrònics,

Certifiquen

que la Memòria de Tesi *Low-Power and Compact CMOS Circuit Design of Digital Pixel Sensors for X-Ray Imagers* presentada per Roger Figueras i Bagué per optar al títol de Doctor en Microelectrònica i Sistemes Electrònics s'ha realitzat sota la seva direcció a l'Institut de Microelectrònica de Barcelona pertanyent al Centre Nacional de Microelectrònica del Consejo Superior de Investigaciones Científicas i ha estat tutoritzada en el Departament de Microelectrònica i Sistemes Electrònics de la Universitat Autònoma de Barcelona.

Directors	Dr. Lluís Terés Terés	.....
	Dr. Francesc Serra Graells	.....

....., a ..... de ..... de .....

a la Bet, al Marc i a l'Anna

Resum

La obtenció d'imatges utilitzant raigs-X ha esdevingut una tecnologia clau per a un ampli rang d'aplicacions tant industrials com mèdiques o científiques, doncs permet estudiar l'interior dels objectes sense necessitat de destruir-los o desmantellar-los. En aquest sentit, hi ha un creixent interès en la recerca en aquests camps, com demostra la literatura, per desenvolupar sistemes avançats de raig-X capaços d'obtenir imatges d'alta qualitat a la vegada que es redueix la dosi total de radiació.

Actualment, els imagers de raig-X estan dominats per sistemes híbrids, basats en matrius de píxels en detectors de conversió directa de raig-X i els seus corresponents circuits integrats de lectura (ROICs). Tot i el seu elevat cost i les seves limitacions en àrea en comparació amb els clàssics sensors de conversió indirecta, els avantatges que ofereixen aquests sistemes són clars en quant a la reducció de la dosi de radiació necessària, la millora de la integritat del senyal i l'escalat en la resolució espacial. Pel que fa al mètode de lectura que empren els ROICs, l'estratègia més estesa es basa en el conteig de fotons, degut als avantatges en termes d'immunitat al soroll i de classificació dels fotons. No obstant, aquests sistemes d'imatge per raig-X pateixen de pèrdues d'informació degut a efectes com el charge-sharing i el pile-up.

És en aquest context que l'objectiu d'aquest treball de tesi és proposar tècniques específiques de disseny analògic i mixte de circuits per al desenvolupament de píxels digitals sensors (DPS) compactes i de baix consum per a ROICs focalitzats a imagers de raig-X híbrids de conversió directa.

L'arquitectura del píxel proposat, basada en el mètode de lectura per integració de càrrega, evita la pèrdua d'informació que pateixen els sistemes basats en el conteig de fotons i contribueix a la qualitat de les imatges per raig-X amb una àrea de píxel compacta i un baix consum per millorar la resolució de la imatge i reduir l'escalfament del detector, respectivament. En aquest sentit, el circuits CMOS del DPS proposat inclouen una conversió de la càrrega sense pèrdues a nivell de píxel per extendre el rang dinàmic, ajust individual del guany per compensar el FPN de la matriu de píxels, capaci-

tat d'autopolarització i comunicacions exclusivament digitals per reduir el crosstalk entre píxels, capacitat d'auto-test per reducció de costos, selecció de la càrrega col·lectable per ampliar el rang d'aplicacions i cancel·lació del corrent d'obscuritat a nivell de píxel. A més, les tècniques de disseny proposades s'orienten al desenvolupament futur de sistemes d'imatge de raig-X modulars 2D amb grans àrees escalables i contínues de sensat.

Aquesta recerca en disseny de circuits s'ha materialitzat en diverses generacions de demostradors DPS, amb valors de pitch des de 100μm baixant fins a 52μm, integrades utilitzant una tecnologia CMOS estàndard de 0.18μm i 1P6M.

S'ha fet una anàlisi exhaustiva de les mesures tant elèctriques com amb raigs-X dels prototips de circuits proposats per a la seva validació. Els resultats experimentals, alineen aquest treball inclús més enllà de l'estat de l'art en píxels actius en termes de resolució espacial, consum, linealitat, SNR i flexibilitat del píxel. Aquest últim punt adequa les tècniques de disseny de circuits proposades a una àmplia gamma d'aplicacions d'imatges de raigs-X.

Abstract

X-ray imaging has become a key enabling technology for a wide range of industrial, medical and scientific applications since it allows studying the inside of objects without the need to destroy or dismantle them. In this sense there is a growing research interest in literature to develop advanced X-ray systems capable of obtaining high quality images while reducing the total radiation dose.

Currently, X-ray imagers are dominated by hybrid systems, built from a pixel array of direct conversion X-ray detectors and its corresponding readout integrated circuit (ROIC). Despite their higher cost and limited area compared to classical indirect counterparts, the advantages of these systems are clear in terms of radiation dose reduction, signal integrity improvement and spatial resolution scaling. Concerning the readout method used by the ROICs, the most common design strategy is based on photon-counting, due to its advantages regarding circuit noise immunity and photon classification. However, these X-ray imaging systems tend to experience from information losses caused by charge-sharing and pile-up effects.

In this context, the goal of the presented thesis work is to propose specific analog and mixed circuit techniques for the full-custom CMOS design of low-power and compact pitch digital pixel sensors (DPS) for ROICs targeting hybrid and direct conversion X-ray imagers.

The proposed pixel architecture, based on the charge-integration readout method, avoids information losses experienced by photon-counting and contributes to X-ray image quality by a compact pixel area and low-power consumption to improve image resolution and reduce heating of X-ray detectors, respectively. In this sense, the proposed CMOS DPS circuits feature in-pixel A/D lossless charge conversion for extended dynamic range, individual gain tuning for pixel array FPN compensation, self-biasing capability and digital-only interface for inter-pixel crosstalk reduction, built-in test capability for costs reduction, selectable electron/hole collection to wide the applications range and in-pixel dark current cancellation. Furthermore, the proposed design techniques are oriented to the future development of truly

2D modular X-ray imager systems with large scale and seamless sensing areas.

All the above circuit design research has been materialized in several generations of DPS demonstrators, with pitch values ranging from 100μm down to 52μm, all of them integrated using standard 0.18μm 1P6M CMOS technology.

Extensive analysis of both electrical and X-ray measurements on the pixel circuit prototypes have been done to proof their validity. Experimental results align this work not only within but also beyond the state-of-the-art active pixels in terms of spatial resolution, power consumption, linearity, SNR and pixel flexibility. This last point makes the proposed pixel design techniques specially suitable for a wide range of X-ray image applications.

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Regarding the fabrication and assembling of the complete X-ray imaging systems, the development of the direct conversion Si detectors employed has been possible thanks to Giulio Pellegrini and all the IMB clean room staff. Equally important, Enric Cabruja has had a key role regarding the UBM process, the management of the bump-growing process and the flip-chip. Finally, concerning the PCBs fabrication and the wire-bonding process, I want to thank Joan Puertas and Alberto Moreno for their work.

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ADC analog to digital converter 9

APS active pixel sensor 7

ASIC application specific integrated circuit 8

BJT bipolar junction transistor 73

CCD charge coupled device 8

CDS correlated double sampling 35

CMOS complementary metal oxide semiconductor 3

CTIA capacitive transimpedance amplifier 35

DAC digital to analog converter 31

DFM design for manufacturing 99

DIL dual in-line 104

DPS digital pixel sensor 9

DQE detective quantum efficiency 13

DTG dual transmission gate 67

ENC equivalent noise charge 58

EP europractice 82

ESF edge spread function 13

FIFO first-in first-out 104

FOM figure of merit 10

FPA focal plane array 115

FPD flat panel detector 6

FPGA field programmable gate array 104

FPN fixed pattern noise 11

HMI human machine interface 106

IC integrated circuit 82

IMB-CNM Institut de Mictroelectrònica de Barcelona 26

LUT look-up-table 47

LSB least significant bit 37

LSF line spread function 13

MiM metal in metal 81

MOS metal oxide semiconductor 43

MOSFET metal oxide semiconductor field effect transistor 65

MPW multi project wafer 83

MTF modulated transfer function 11

MSB most significant bit 42

NPS noise power spectrum 14

NTF noise transfer function 54

OSR oversampling ratio 58

PC personal computer 104

PCB printed circuit board 104

PDM pulse density modulation 33

PRMLS pseudo-random maximum length sequence 47

PSF point spread function 12

PTAT proportional to absolute temperature 73

PWM pulse width modulation 33

ROI region of interest 10

ROIC read-out integrated circuit 8

SC switched-capacitor 58

S/H sample and hold 70

SNDR signal-to-noise and distortion ratio 58

SNR signal-to-noise ratio 10

SR spatial resolution 12

STF signal transfer function 52

TFT thin film transistor 6

UBM under bump metalization 102

USB universal serial bus 104

Introduction | 1

This chapter introduces the main motivation of the presented work together with the required background in terms of X-ray imaging fundamentals, existing technologies, practical metrics and state-of-the-art techniques. Also, the target objectives and scope of this thesis are exposed.

1.1 Motivation

X-ray imaging is a key technology in many application fields such as physics [1], medicine [2], industry [3], security [4], chemistry [5] or even art [6]. This is due to the ability of X-ray particles to pass through matter with a penetrating power related to their energy and matter properties. For example, water or fat are easily penetrated compared with bones or calcifications, which are more dense. This feature makes X-rays extremely useful to non-destructively image the inside of objects which are usually opaque to visual light. However, X-ray photons can also ionize atoms, which could damage living tissues. Therefore, and especially in medical applications, the compromise between radiation dose and image quality leads to a very intense and extensive research on this topic.

An X-ray imaging system can be schematized as in Fig. 1.1. It is mainly composed of an X-ray source, which generates the X-ray photons, and the X-ray sensor. The spatial distribution of X-ray photons after the interaction with the sample is captured by the X-ray sensor, which converts this information into image data. The X-ray sensor is composed of basic image units

called pixels (picture elements), whose size is related to the system spatial resolution. For each application, the sensor must meet certain performance figures in terms of X-ray photons energy, limited radiation dose, imager size or spatial resolution. For example, concerning X-ray imaging applications, mammography is probably one of the most demanding fields due to its large area and high resolution requirements at low radiation doses. Proof of this interest is the number of references in the literature, specially due to the social importance of the early detection of breast cancer in women [7, 8]. Table 1.1 summarizes some of these requirements. In this particular case, pixel pitch under 50μm are not advantageous since smaller microcalcifications do not provide useful information for diagnosis [9].

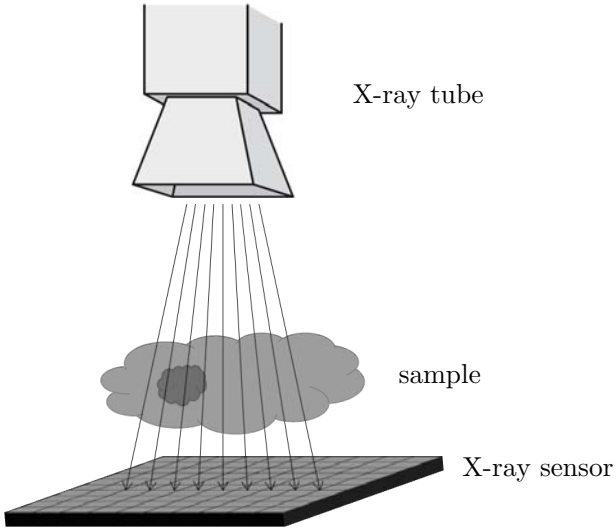

Figure 1.1 | Simplified scheme for an X-ray imaging system.

Current research in X-ray imaging systems is mainly focused in improving image quality at low radiation doses. In this sense, digital direct hybrid systems are one of the most promising technologies. As it will be discussed later in this chapter, obtaining large sensing areas with these systems is challenging, since the limited yield of technology tends to increase their costs. Also, pixel functionality and power efficiency are opposed to the spatial resolution and image quality.

Parameter	Requirement
Imager size	18cm×24cm
Pixel pitch	>50μm×50μm
Acquisition time	< 5s
X-ray photon energy	20keV to 50keV
Exposure dose	0.6mR to 240mR

Table 1.1 Main requirements for X-ray detectors targeting mammography applications [9].

This thesis presents novel low power complementary metal oxide semiconductor (CMOS) pixel circuits for digital direct X-ray imaging targeting low-cost and modular imaging systems.

1.2 X-Ray Imaging

1.2.1 Fundamentals

X-rays, which were discovered by Wilhelm Conrad Röntgen in 1895, are referred to the electromagnetic radiation with energies between 100eV and 100keV, corresponding to spectrum frequencies between 3×10^{16}Hz and 3×10^{19}Hz, and to wavelengths between 10nm and 0.01nm.

X-rays can be generated in a so-called X-ray tube by the acceleration of electrons applying high voltage potentials (typically tens of kV) between the hot cathode and the metal target (the anode) usually made of tungsten or molybdenum. The amount of applied voltage determines the maximum energy of the resulting X-ray photons. The collision of these accelerated electrons with the target generate X-rays due to the combination of two atomic processes: the X-ray fluorescence and the Bremsstrahlung. The former occurs when the accelerated electron kicks out an orbital electron of the target atoms and the electrons of high level energies fill the left vacancy and emit X-rays. The spectrum produced by this process is composed by discrete frequencies that depend on the target material properties. The Bremsstrahlung process consists on the accelerated electron being scattered,

which produces a continuous spectrum. Filters are usually employed to cut off a fraction of this part of the spectrum. Fig. 1.2 shows the typical spectrum obtained from an X-ray tube [9]. In order to generate X-rays with narrower spectrum windows and better linear polarizations and collimation, particle accelerators can be used for synchrotron radiation.

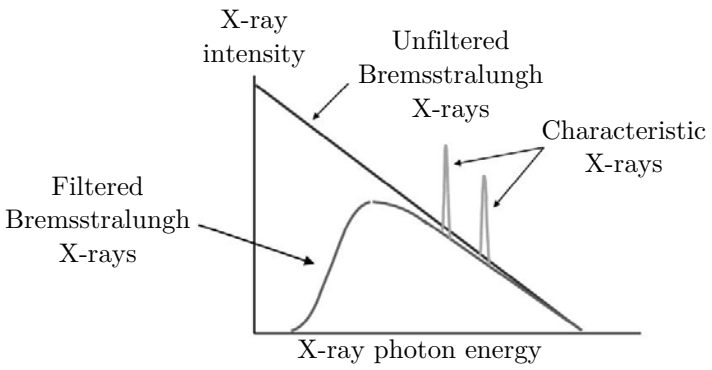

Figure 1.2 | Typical spectrum obtained from X-ray tubes with fluorescence peaks and Bremsstrahlung effects [9].

As for the interaction of X-rays with matter, in terms of penetrating power and absorbed dose, it depends on both X-rays properties and matter themselves. Basically, this interaction is dominated by three different processes, depending on photon energy ($h\nu$) and atomic number (Z) of the material [9]. First, the photoelectric effect occurs when a low-energy photon is absorbed by an atomic electron, which will be ejected. Second, the Compton scattering takes place when a high-energy photon transfers part of its energy to an electron, which will be emitted. Finally, the Rayleigh scattering happens when the photon simply varies its trajectory, with no energy transfer.

The absorbed dose is the radiation energy deposited in a material (e.g. human tissues) and it is measured in Grays (Gy) or rads (1rad= 0.01Gy), which are equivalent to the units of energy in Joules deposited in one kilogram of material. The biological effect of the radiation on a living tissue is different depending on its nature. Therefore, the equivalent or effective dose is quantified by weighting the absorbed dose with a factor (w_R) that depends on the type of radiation and tissue, and it is measured in Sieverts (Sv). The limit of effective dose, which is legally fixed by each country, is

around 1mSv/year. In comparison, the dose of a screening mammography or a chest radiography are around 3mSv and 0.1mSv respectively [10].

The distance traveled by an X-ray photon before interacting is called the mean free path and depends on the photon energy and the atomic number of the material. Once inside the material, the beam intensity at a depth x presents an exponential behavior following the Lambert-Beer law [11]:

$$I(x) = I_0 e^{-\mu(h\nu,Z)x} \tag{1.1}$$

where I_0 is the beam intensity before reaching the material and $\mu(h\nu, Z)$ (in cm^{-1}), which is proportional to the inverse of the mean free path, is the so-called linear attenuation coefficient and represents the fraction of incident photons interacting with the material per unit length. Attenuation increases with Z and decreases with $h\nu$. Fig. 1.3 shows the behavior of the attenuation coefficient of different elements versus the photon energy.

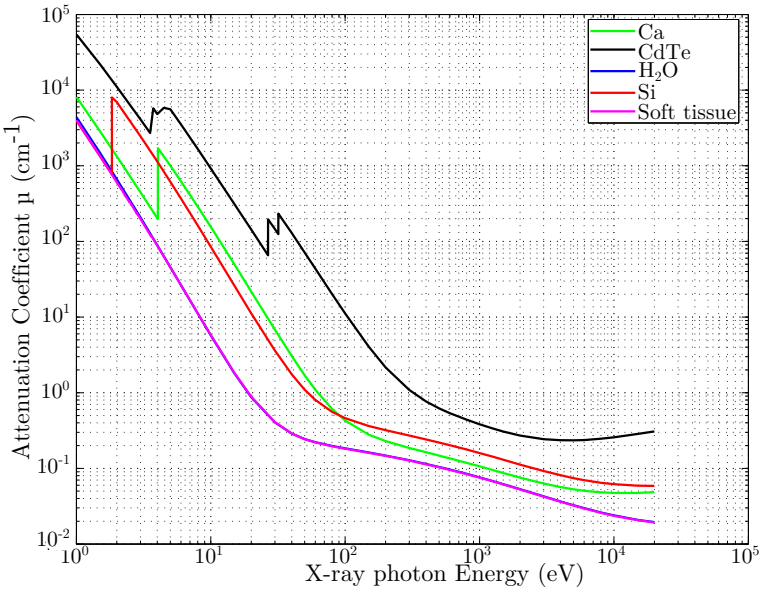

Figure 1.3 | Attenuation coefficient vs photons energy for different elements or materials [12].

In conclusion, the intensity of X-rays after crossing the sample in Fig. 1.1 depends on their energy and on the particular matter of the region they are passing through, thus an image is generated. For example, using X-rays of about 20keV, a beam passing through a soft tissue, which contain large quantities of water, will experience less absorption than a beam passing through a calcification tumor, which is mainly composed of calcium.

In practice, different beam intensities in different areas will reach the detector of Fig. 1.1 generating an image of the studied sample. Although image magnification is possible by modifying distances between the source generating the X-ray conic beam, the imaged sample and the detector, optical amplification is not feasible since X-rays are not easily focused [13].

Therefore, the detector must capture most of the incoming photons to obtain good quality image at low radiation doses. I.e. it must show a high efficiency, which is the ratio between absorbed and incoming photons.

Regarding the method to record the high energy photons, X-ray imaging systems have evolved through the following technologies:

Film systems. The earliest X-ray system was based on photographic film, which is composed of a sheet of plastic covered with a photosensitive emulsion. After being exposed to radiation and chemical processing, a visible image is created. Despite its low quantum detection efficiency, typically 1% to 2%, which translates into high radiation doses, this method is still in use thanks to its low cost, high resolution and the possibility of obtaining large sensitive areas. Efficiency can be improved by covering the emulsion with phosphor, which converts the incident X-rays to visible light, but at the cost of resolution losses.

Flat panel detectors. The introduction of pixelated flat panel detectors (FPDs) brought an improvement in the efficiency, contrast and dynamic range, as well as the possibility of image digitization. In short, they consist on a converter material coated or deposited on an array of thin film transistors (TFTs). Two types of FPDs can be distinguished: indirect conversion and direct conversion detectors.

Indirect conversion detectors convert X-rays to visible spectrum light through a scintillating material (typically cesium iodide) deposited

over an array of photodiodes in amorphous silicon substrates. The scintillator illuminates the photodiodes, which then convert the light into electronic charge and are connected to the readout circuitry. This photodiode together with the readout circuitry form the basic element called active pixel sensor (APS). This type of detectors tend to experience lateral light diffusion in the scintillator, lowering significantly the spatial resolution. Direct conversion detectors, on the other hand, exploit amorphous or polycrystalline semiconductor materials (typically amorphous selenium) to directly convert X-ray photons into electron-hole pairs avoiding the lateral diffusion issue at pixel level. Fig. 1.4 shows the operating principle and the signal profile for indirect and direct detection [14]. In both cases, the sensitive material is deposited directly over the readout circuit array. However, a large amount of energy is needed to create electron-hole pairs. Since the pixel circuitry area usually includes a photodiode or a capacitance together with at least a switching thin film transistor plus connectivity routing, the fill factor may be poor, weakening signal in tiny pixel sizes. The amount of generated charge, which is somehow proportional to the photon energy, is stored locally at each pixel and sent to the readout circuit, where information is processed and digitized. There are many advantages in digital imaging: images can be stored and displayed electronically with no need for material support, they can be shared easy and quick, and computer assisted post processing is also available [15, 16].

With this technology, large area X-ray imagers have been obtained with sizes up to 40cm×40cm and pixels pitchs down to 150μm [17].

Hybrid systems. In order to achieve a sensitive area of almost 100% filling factor and improve resolution and efficiency, a crystalline semiconductor direct conversion detector pixelated in an array of p-n junctions can be hybridized with the readout circuit. This hybridization is usually completed employing bump-bonding and flip-chip packaging techniques, which connect pixel-by-pixel the readout circuitry with its corresponding X-ray detector. Another advantage of this kind of sensors compared with monolithic solutions is that different detector and readout circuit technologies can be mixed, allowing the use of the same readout circuit with a wide range of detector materials. Hence,

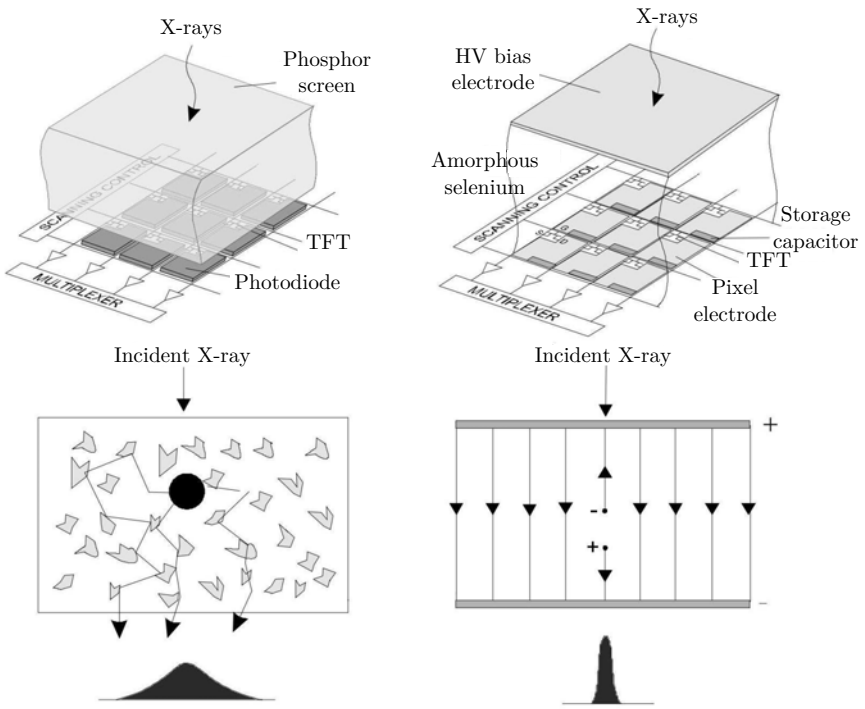

Figure 1.4 | Operation principle and signal profile given by indirect (left) and direct (right) X-ray detectors [18].

both parts can be chosen independently to satisfy the requirements of a particular application. Fig. 1.5 shows a representation of a direct conversion detector hybridized with the readout circuitry using bump-bonding and flip-chip techniques. A more detailed description of direct semiconductor detectors for hybrid systems can be found in Section 1.2.3.

Regarding the readout circuit technology for hybrid systems, it is usually composed of an application specific integrated circuit (ASIC) formed by an array of pixel readout circuits. These dedicated ASICs are called read-out integrated circuits (ROICs). The continuous advances of CMOS technologies, have made possible to increase the pixel functionality of these ROICs from the simplicity of charge coupled devices (CCDs), to highly complex

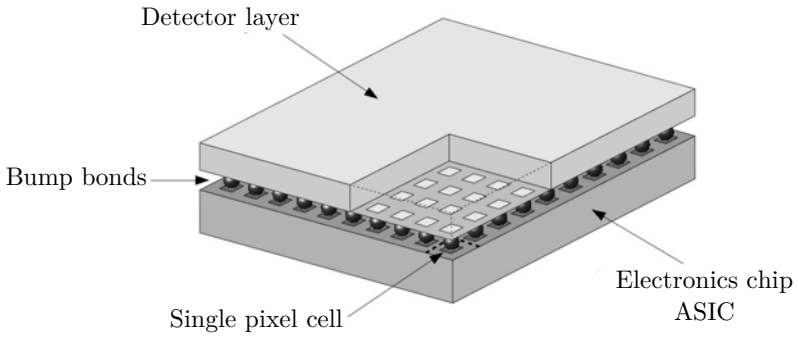

Figure 1.5 X-ray sensor consisting on the bump-bonding hybridization of a direct conversion detector with its readout circuitry.

APS cells including analog to digital converters (ADCs), programmability and data storage at a pixel level resulting in digital pixel sensors (DPSs).

The reading method of these pixels can be classified into two categories: charge-integration and photon-counting. The charge-integration method accumulates all the charge generated by X-rays, but also including circuit noise, over a certain time interval. On the other hand, photon-counting consists on counting only those individual photons whose energy exceeds a certain threshold. This alternative approach is more immune to circuit noise, but it can experience charge-sharing and pile-up effects. The first undesired effect occurs when the charge generated by an X-ray photon that should be counted is spreaded among some neighboring pixels either without exceeding the threshold in any of them causing the system to discard this photon, or exceeding this threshold in some of them causing multiple counts. Pile-up effect happens when photons arrive so close to each other that they can not be distinguished in time. A more detailed discussion about charge-integration versus photon-counting can be found in Section 1.2.4.

Nevertheless, and despite all the advantages of X-ray imagers based on the hybridization of direct conversion detectors with CMOS ROICs, large and seamless sensing areas can only be obtained at a high costs due to restrictions in technology yields [17], as explained in Section 1.2.3.

1.2.2 Figures of Merit

This section introduces the main metrics applied to X-ray imaging which will be used as figure of merits (FOMs) for evaluating the proposed work.

Contrast

The radiographic contrast, which quantifies the variation between different areas of the X-ray image, is defined according to Eq. 1.2, where ΔI_{ROI} is the variation of signal intensity in the region of interest (ROI) with respect to the background signal intensity I_{bkgnd}. The contrast depends on the difference of the attenuation coefficients of materials (areas), but not on the number of incident photons (dose). Therefore, it is affected by photons and charge scattering on the detector.

$$C \doteq \frac{\Delta I_{ROI}}{I_{bkgnd}} \tag{1.2}$$

Signal-to-Noise Ratio

The noise level determines the floor of the image quality, since at levels below this threshold true signal fluctuations are confused with noise fluctuations. For example, medical applications like mammography, show small contrast between the different soft tissues, so the higher the power signal-to-noise ratio (SNR) the better the image quality. The fluctuation of the number of photons absorbed in the detector per unit area is called the photonic noise, or quantum mottle, and it has a Poisson distribution behavior with the incoming signal power. The power SNR at the input of an imaging system for a monoenergetic X-ray beam can be written as:

$$SNR_{in} \doteq \frac{S_{in}}{\sqrt{N_{in}}} \equiv \frac{S_{in}}{\sqrt{S_{in}}} = \sqrt{S_{in}} \tag{1.3}$$

Hence, SNR is increased with higher doses, which leads to a compromise between image quality and radiated dose. It can also be argued that scaling

down pixel area, smaller details of an image become noticeable, but also SNR is reduced since the dose per pixel is smaller.

In a direct conversion detector, if η is the X-ray absorption efficiency of the detector and G is the conversion gain, signal power after the conversion of photons into charge is:

$$S_{conv} = \eta G S_{in} \tag{1.4}$$

On the other hand, noise power after the conversion is the uncorrelated sum of:

$$N_{conv} = \sqrt{S_{conv}G + S_{conv}F} = \sqrt{\eta G^2 S_{in} + F\eta G S_{in}} \tag{1.5}$$

where F stands for the Fano factor, the ratio between the variance of the observed mean energy and the variance predicted from Poisson statistics. F is specific for each material but almost independent of the photon energy [19]. For example the Fano Factor for Si is 0.115, while for GaAs is about 0.18 [20]. As a result, SNR at the output of the detector is given by

$$SNR_{conv} = \frac{\eta G S_{in}}{\sqrt{\eta G S_{in}}\sqrt{G+F}} \equiv \sqrt{\frac{\eta G S_{in}}{G+F}} \tag{1.6}$$

which equals SNR_{in} for the ideal case of $G >> F$ and $\eta = 1$. Other noise sources are related to inhomogeneities in the detector, and the electronic noise of the read-out circuit itself. The inhomogeneities in both the detector and the readout circuit produce fixed pattern noise (FPN), which is proportional to the signal power and can be reduced by calibration.

Modulation Transfer Function

The modulated transfer function (MTF) describes the spatial frequency response of an imaging system. In other words, MTF quantifies how the contrast is transmitted. It can be expressed as the ratio of the modulation

of a sinewave at the input and output of the detector at a given spatial frequency:

$$MTF \doteq \frac{C_{out}}{C_{in}} \equiv \frac{(\frac{A_{max}-A_{min}}{A_{max}+A_{min}})_{out}}{(\frac{A_{max}-A_{min}}{A_{max}+A_{min}})_{in}} \tag{1.7}$$

where A is the amplitude of the sinewave, and the spatial frequency is given in lines per millimeter (lp/mm). MTF is usually normalized to 1 at 0 spatial frequency and it decreases as the spatial frequency increases as shown in Fig. 1.6. The spatial frequency where MTF equals to 0.3 defines the spatial resolution (SR).

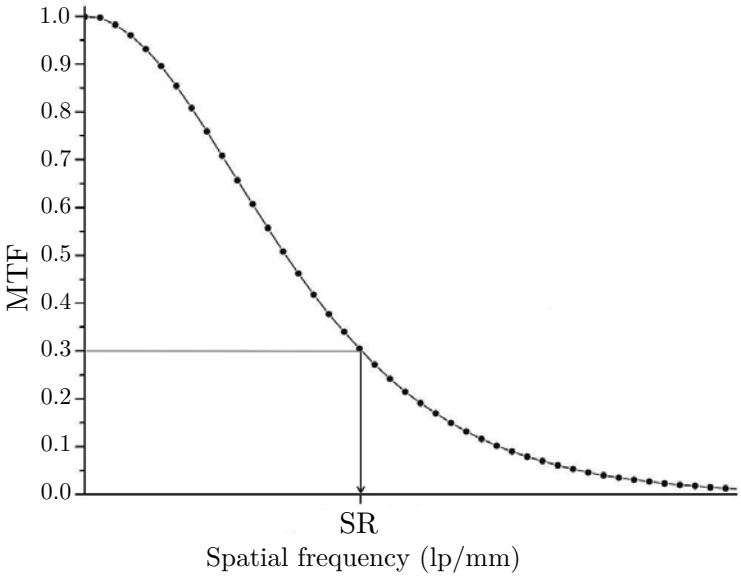

Figure 1.6 | Typical MTF behavior.

In multistage systems, the total MTF is the product of the individual MTFs.

The point spread function (PSF) is defined as the response of an imaging system to a point light source. Its degradation, which is observed as image unsharpness, is mainly caused by charge diffusion in the detector. Due to the

difficulty of its generation and measurement, the line spread function (LSF) is used instead and defined as the response of the imaging system to an infinite long and narrow line. Also, edge spread function (ESF) is defined as the distribution in absorbed energy per unit area that can be extracted from the image of a sharp edge of a total absorbing material.

The MTF is also defined as the Fourier transform of the LSF. Therefore, it can be measured by imaging a precision edge slightly tilted to the pixel column or row. The data along the direction of the edge gives the ESF figure, which leads to the LSF performance by differentiation, and to the MTF characteristic using the Fourier transformation.

The theoretical limit of MTF for squared shape pixels is determined by the pixel size L and the Fourier transform of a step function with a width of one pixel as:

$$MTF_{lim} = \frac{1}{L}\left|\int_{-L/2}^{L/2} e^{i2\pi fx}dx\right| = \frac{sin(\pi fL)}{\pi fL} = sinc(\pi fL) \tag{1.8}$$

where f stands for the spatial frequency. The Nyquist frequency is the maximum spatial frequency that can be reconstructed. In pixelated systems it is given by:

$$f_{Nyq} = \frac{1}{2L} \tag{1.9}$$

In images with spatial frequency contents higher than f_{Nyq}, aliasing creates distortion. Thus, it is important to have the highest possible MTF at this frequency.

Detective Quantum Efficiency

The detective quantum efficiency (DQE) of an image system is described at each spatial frequency by the ratio of the input to output SNRs:

$$DQE = \left(\frac{SNR_{out}}{SNR_{in}}\right) \tag{1.10}$$

In complex imaging systems, the overall DQE is the product of the DQEs of each stage. Therefore, it is never better than the worst DQE. For direct detecting systems it becomes critical the absorption efficiency η of the detector, as can be extracted from the ideal case of Eq. 1.6 and Eq. 1.3.

DQE can also be expressed in terms of MTF and the noise power spectrum (NPS), which is the variance of the signal for different spatial frequencies:

$$DQE = \frac{\overline{S}^2 \cdot MTF^2}{\Phi \cdot NPS} \tag{1.11}$$

where $\overline{S}$ is the average image signal and Φ is the entering X-ray fluence [19].

1.2.3 Direct Conversion Semiconductor Detectors

As introduced in Section 1.2.1, the most promising results in X-ray imaging are obtained from digital direct hybrid systems [21–24]. In general, they involve a ROIC hybridized through bump-bonding and flip-chip techniques with an X-ray detector material, which converts photons directly to the electronic charge to be read by the ROIC.

Direct conversion detectors for hybrid X-ray imaging systems usually employ high resistivity crystalline semiconductor materials to take benefit of the small amount of energy needed to create electron-hole pairs while still keeping this threshold high enough to avoid thermally generated charge carriers. Thanks to this property, the incoming X-ray photons generate photoelectrons in the detector material, which in turn will excite other electrons creating a charge cloud.

In order to locally collect this charge, the detector is designed as an array of reverse biased p-n junctions or Schottky diodes with a small opening in the passivation for the bump-bonding connection to the ROIC by flip-chip as shown in Fig. 1.7. Another advantage of crystalline semiconductors is that carriers lifetime is orders of magnitude higher than in amorphous or polycrystalline structures, allowing higher thickness and/or lower biasing voltages for the detectors [25]. Unfortunately, large area crystalline structures are difficult to obtain.

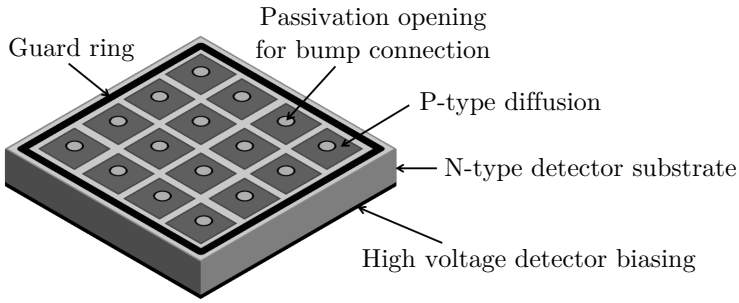

Figure 1.7 | Representation of a direct X-ray detector consisting in an array of reverse biased p-n junctions.

In practice, the polarization must be high enough to fully deplete the detector of free carriers to ensure the collection of almost all the generated charge, avoid charge recombination and minimize lateral charge diffusion. Furthermore, with the purpose of reducing leakage current and avoid undesired lateral effects on the peripheral pixels, the use of guard rings is strongly recommended [26, 27].

The most common materials in direct conversion X-ray detectors are Si, CdTe and GaAs [24], with different results in each case [28]. Their main characteristics are summarized in Table 1.2.

Property	**Si**	**CdTe**	**GaAs**
Atomic number (Z)	14	48/52	31/33
Density (g/cm^3)	2.33	6.20	5.31
Band Gap (eV)	1.12	1.56	1.42
Ionization energy (eV)	3.63	4.45	4.20
Electrons mobility (cm^2/Vs)	1500	1050	8500
Holes mobility (cm^2/Vs)	450	100	400

Table 1.2 | Main characteristics at room temperature of the most common materials for X-ray direct detection.

Since ionization energy, which is the energy needed to create an electron-hole pair, is similar in all of them, nearly the same performance is expected in terms of the generated charge per photon. The most important difference in

performance is given by their behavior in terms of X-ray photon absorption efficiency at different energies, as shown in Fig. 1.8.

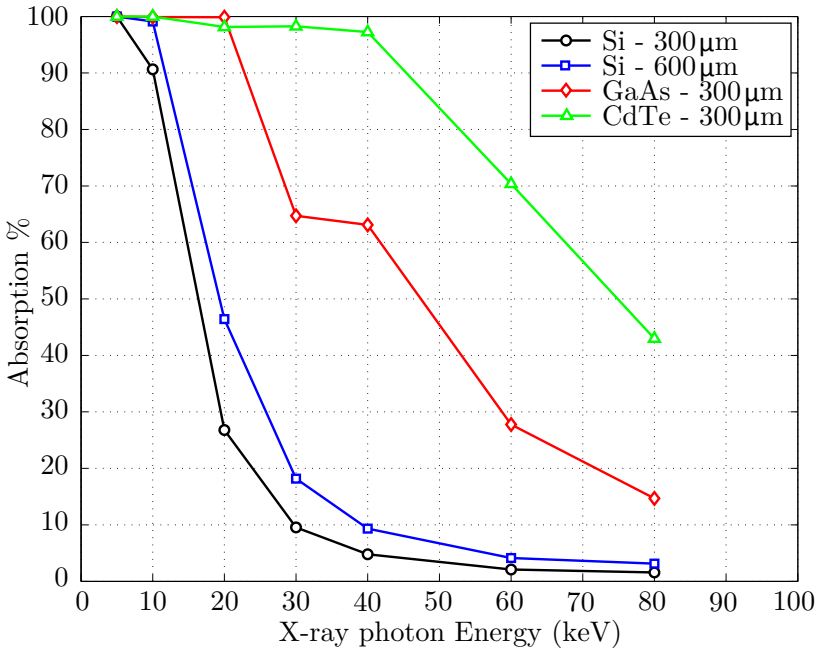

Figure 1.8 Comparison of absorption efficiency for detector materials of Table 1.2 versus X-Ray photon energy. Detector material and thickness are shown in the legend [29].

From Fig. 1.8 and Fig. 1.3, CdTe and GaAs detectors seem to be a better choice compared to Si. On the contrary, Si detectors are widely used thanks to their lower cost, mature technology, and higher yield in terms of purity.

In principle, higher thickness values should give better performance at the cost of higher biasing potentials to fully deplete the detector. However, this high voltage bias increases the diode inverse current, called dark current, which in turn increases with detector heating [30].

Lateral charge diffusion causes splitting of the generated charge cloud among several neighboring pixels of the array. This effect, called charge-sharing, is pronounced in small pitch pixels, and it might cause a problem for readout

circuits based on single photon-counting [31–33], as discussed in next section. This issue has been addressed with novel detector design approaches [34].

Regarding the sensing area, state-of-the-art technologies allow the fabrication of crystal silicon ingots for detectors which can reach 400mm diameter as best case. For GaAs and CdTe detectors, this area is much smaller. However, the larger the detector area, the more reduced the purity and uniformity.

In practice, the most limiting factor is the maximum size of ROIC dices due to the photolitographic stepper reticles of CMOS technologies [35]. Although this limitation may be overcome by stitching techniques at mask level [35], CMOS technology yield still dominates the maximum ROIC size.

1.2.4 Charge Integration versus Photon Counting

As already mentioned in Section 1.2.1, two processing strategies can be chosen to create an image from the collected charge generated in the direct X-ray detection: charge-integration or photon-counting modes [9].

Photon-counting systems are based on the comparison of the charge generated by a single X-ray photon with a given threshold to determine whether this photon contributes to the output image or is discarded. Thus, each counted photon contributes with the same weight and the lowest measurable signal is a single photon. Since the threshold is set above the noise, the background is eliminated, and large acquisition times are allowed. The dynamic range is therefore limited by the capacity of the digital counter. Furthermore, using multiple threshold levels or sweeping this threshold in consecutive acquisitions, information of the spectrum of the incoming X-ray photons can be obtained, at the expense of a more complex DPS.

On the other hand, charge-integrating systems count all the charge reaching the front-end ROIC, including the dark current itself. This strategy reduces the SNR and the dynamic range. Moreover, since the amount of charge is somehow proportional to the photon energy, the contribution of higher energy photons, which in some cases can carry less useful information show more weight in the output image.

Regarding the circuit complexity, the charge-integrating pixels can be very simple, for example including only few switching transistors and a capacitor as storing element. Generally, photon-counting require front-end electronics with higher complexity. The simplest implementation of Fig. 1.9 includes a pulse shaper amplifier with an RC feedback network and a discriminator to compare amplifier output with the given threshold. Finally, the corresponding event from the comparison result can be either sent outside the array for further processing or stored in the pixel built-in digital counter.

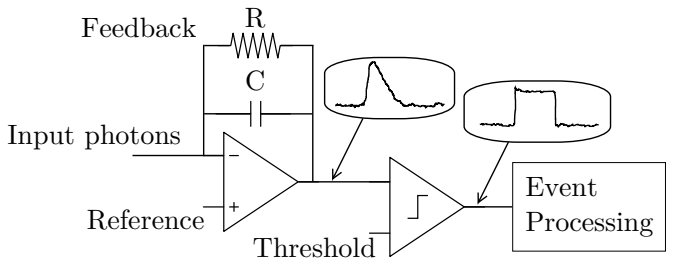

Figure 1.9 | Simplified schematic of a photon counter and operation waveforms when sensing electrons.

The principle of operation is as follows: the incoming charge is accumulated in the amplifier feedback capacitor and is continuously removed by the RC feedback. If the dynamic output temporally exceeds the threshold level, the comparator toggles, generating a single count event. Thanks to the scaling capabilities of CMOS technologies, it is possible to improve this basic circuit functionality at pixel level by adding more threshold levels to obtain spectral information, threshold programmability for calibration and to avoid mismatching in the response of different pixels under the same conditions.

From the above analysis it could be argued that despite the higher circuit complexity needed, photon-counting is superior to charge-integration. However, two practical undesired effects must be taken into account:

Pile-up. First, close in time individual photons can become indistinguishable, thus loosing their information. This effect, known as pile-up, increases at high fluxes, when photons arrive closer than the temporal resolution of the readout circuitry and can not be resolved, as in the

example of Fig. 1.10. The main drawback that this effect presents is the deviation of the response of the pixel from the linear behavior [29, 36]. Furthermore, the unregistered photons can increase up to the point where no photons are counted at all [37, 38].

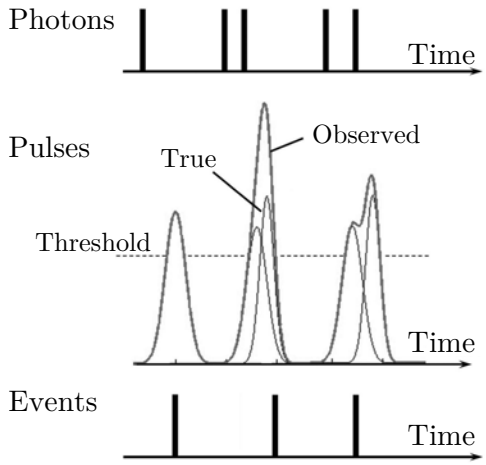

Figure 1.10 Explanatory example of the information losses in photon-counting due to the pile-up effect. In this study case, 5 photons reach the detector, but only 3 are counted. Moreover, if multiple thresholds were available, the obtained energy resolving information would also be erroneous [39].

Charge-sharing. Another drawback of photon-counting systems extensively studied is charge-sharing [31–33, 40]. Basically, this effect occurs when the charge cloud generated by an X-ray photon expands as a consequence of charge diffusion due to Coulomb repulsion between charges. As a consequence, the generated charge can be shared between two or more neighbored pixels. If the charge cloud that should be counted is highly dispersed, each pixel collects a portion of charge below the required to cause the output of the amplifier to exceed the threshold level. Hence no events are generated and the information carried by the X-ray photon is lost, degrading the image resolution and the spectrometric performance. On the other hand, if a high energy

X-ray photon generates a charge cloud shared by some neighboring pixels, multiple events could be recorded.

Fig. 1.11 summarizes the possible situations combining the energy and charge dispersion cases. Here, the X-ray photon energy level is illustrated as the depth where the X-ray photon interacts and the charge cloud dispersion is shown along with the width of the shadow. The output of the amplifier, which generates an event if the threshold level is exceeded, is also shown.

Hence, the impact of the charge-sharing effects grows as the pixel pitch is reduced and depends on the photon energy, on the detector material, characteristics and thickness, and the bias voltage of the detector. Therefore, it can not be easily compensated by digital post-processing.

Large pixels reduce the impact of these effects but at some time degrade the spatial resolution. In the same way, thinner detectors and high polarization voltages reduce the charge-sharing and parallax effects but deteriorate the efficiency and increase the dark current respectively. As an example, in the case of using a CdTe X-ray detector of 1mm thickness biased at 100V with 55μm-pitch, pixels studies [32, 40] show that if photons do not interact very close to the read-out pixel circuit electrode and close to its geometrical center, the maximum collected charge is around 50% only, with the rest of the charge more or less homogeneously distributed among the neighboring pixels. The consequences of this effect are decreases of contrast, SNR and MTF, and are significant enough to justify many redesign efforts on existing photon-counting pixels as in the case of the Medipix family [41].

In conclusion, there is not a clearly ideal readout method for X-ray imaging, since it is strongly dependent on the particular application requirements.

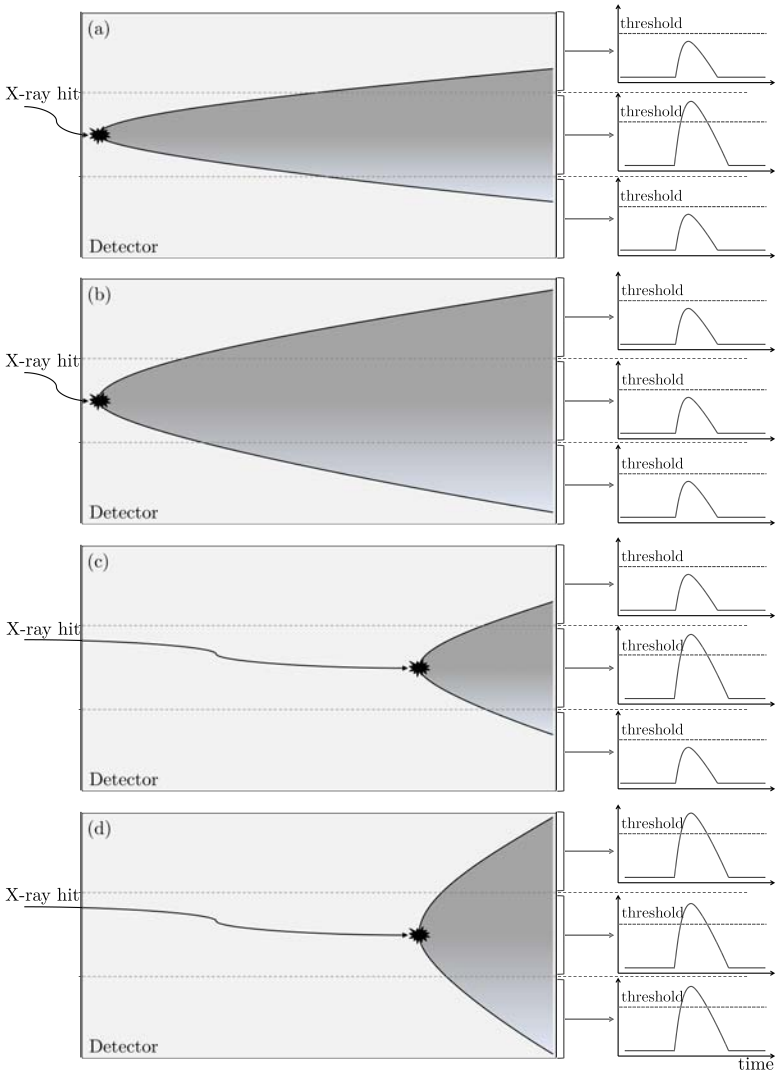

Figure 1.11 Charge-sharing effects description: mid-energy X-ray photon and low charge dispersion (a), mid-energy X-ray photon and high charge dispersion (b), high-energy X-ray photon and low charge dispersion (c) and high-energy X-ray photon and high charge dispersion. In (b) situation, no events are registered while in (d) situation, multiple events are registered.

1.3 State-of-the-Art Technologies

During recent years, extensive research has been carried out in order to improve the performance of X-ray imaging systems. Despite some proposals may be useful only for particular applications, most techniques are targeting high spatial resolution and large area imaging.

This section presents the state-of-the-art X-ray imaging systems at ROIC level, which is the focus of the work presented in this thesis. Lots of approaches can be found in the literature and can be classified following different criteria. Regarding the readout method, although the most studied strategy is photon-counting [22, 42–60], charge-integration is also addressed in many cases [61–70]. In fact, active pixels combining these two readout methods have also been studied [71, 72]. The circuit complexity at pixel level can range from few transistors with analog output and charge-integration approach [61–65] to highly complex circuits with in-pixel digital memory either based on charge-integration [66, 68, 69] or photon-counting [42, 45–47, 49–53, 58–60]. Other approaches provide analog or single bit digital outputs as trigger to external circuitry [43, 48, 54, 55]. In this sense, Table 1.3 summarizes a comparison between state-of-the-art pixels for digital direct X-ray imaging.

Chip[Ref]	Park[63]	PAD[64]	XPAD3[49]	PSIpix[53]	Medipix2[58]
CMOS technology	0.6μm CSM	1.2μm HP	0.25μm IBM	0.25μm UMC	0.25μm IBM
Pixel pitch	35μm	150μm	130μm	75μm	55μm
Array size	161082	92×100	80×120	256×256	256×256
Readout method	Ch-I	Ch-I	Ph-C	Ph-C	Ph-C
Programmable	no	no	yes	yes	yes
Readout output	Analog	Analog	Digital 12-bit	Digital 12-bit	Digital 13-bit
Power/pixel	N.A.	N.A.	40μW	8.8μW	8μW
Noise	N.A.	N.A.	$100e^-_{rms}$	$135e^-_{rms}$	$140e^-_{rms}$

Table 1.3 Comparison of state-of-the-art ROIC pixels for direct X-ray imaging. Readout methods are charge-integration (Ch-I) and photon-counting (Ph-C).

As it has been pointed out in previous sections, large size hybrid imagers are

difficult to obtain due to yield limitations of ROIC technology. Therefore, in order to cover the large areas required in some X-ray imaging applications, several approaches have been addressed such as generating a large image from moving a single chip taking sub-images, by using a multichip array or by combining both methods. The multichip approach requires chips specifically designed 3-side buttable with all external connection pads located on one side of the ROIC die as illustrated in Fig. 1.12 [73–75]. The main issue of this approach is the dead space left between chips. Also, since the coverage area is $2 \times N$ with respect to the single chip area, image size is fully scalable only in one dimension.

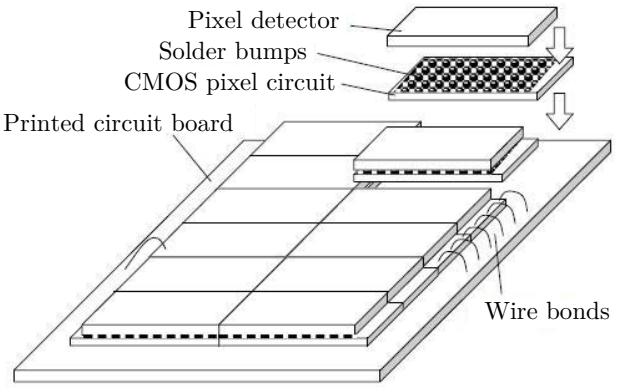

Figure 1.12 General arrangement for $2 \times N$ tiling of 3-side buttable small X-Ray imagers to obtain larger imaging areas. Dead zones between detector arrays are evident [19].

In order to overcome the scaling limitation and cover the dead areas between individual detectors at least in one dimension, more sophisticated assemblies have been studied by tilting individual detectors following Fig. 1.13 [19, 73]. Another way to avoid dead spaces between tiled imagers is to hybridize multiple ROICs to a single large detector. However, a similar issue would be present, as larger pixels in the boundary between adjacent chips would introduce non-uniformity in the resolution and higher count rates in periphery of the chips as fixed pattern noise.

An alternative approach, which involves step-scanning a large area with one or more small detectors has been also addressed [19, 76–79]. It basi-

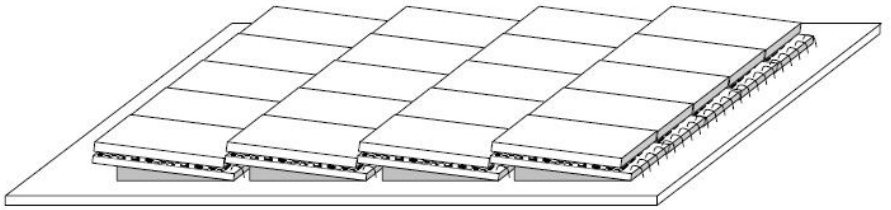

Figure 1.13 | A more sophisticated arrangement of M×N tiling multiple X-ray imagers to cover a large area [19].

cally consists in a master-board with one or more small imagers that scans a large area by taking a snapshot and mechanically moving the system to a new position for another snapshot until the full large area is covered as illustrated in Fig. 1.14. The full image is obtained by combining the different snapshots. The whole system complexity is very high since it requires precise control of mechanical movements, take several snapshots at the risk of patient movement and preferably turning off the X-ray source during the master-board movement, and perform time consuming postprocessing.

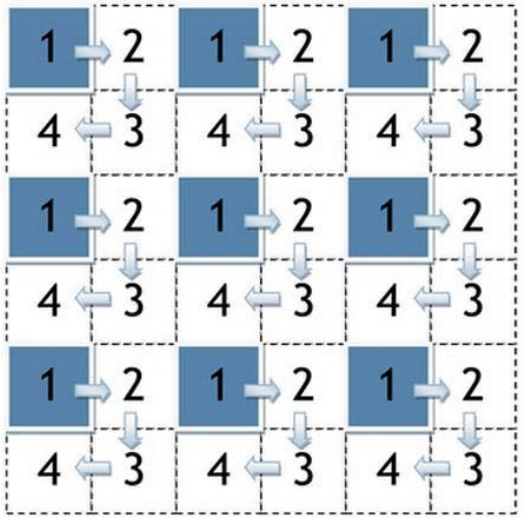

Figure 1.14 | Schematic process of scanning a large area with an array of single small detectors [76]

1.4 Objectives and Scope

This research work is focused on advanced CMOS design of DPS circuits for hybrid direct X-ray imagers. Fig. 1.15 shows the X-ray direct system general building blocks where CMOS DPS circuits are located, where V_{com} is the common voltage bias for the X-ray detector and I_{sens} stands for the current collecting the charge generated by the X-ray particle.

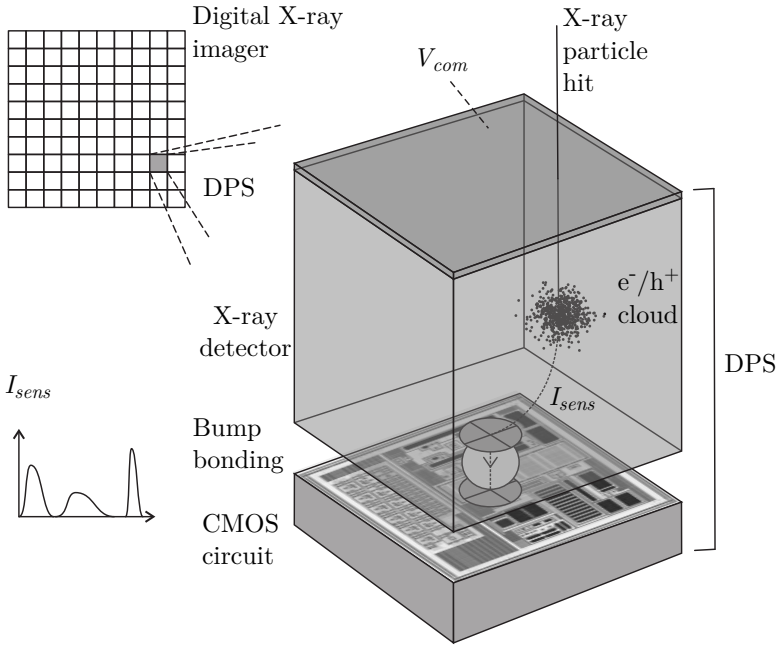

Figure 1.15 | General parts of an X-ray digital direct hybrid system.

In particular, the objectives of the current research work targets the design, integration and test of novel active pixels featuring:

- Lossless charge-integration readout method.
- Individual gain programming for FPN compensation.
- Local generation of voltage references and bias currents to reduce crosstalk.

- Digital-only communications also for crosstalk reduction.
- Built-in test capability to lower screening costs.
- Biphasic current sensing capability for different applications.
- Built-in temperature compensation.
- Design oriented for its use in modular imaging systems.
- Compact design for high spatial resolution.
- Low-power operation to avoid detector heating.

Despite being out of the scope of this thesis, the long term objective is to apply the resulting DPS techniques to build truly two-dimensional modular ROICs for low-cost and large area X-ray imaging systems.

The present thesis is structured following a top-down methodology. First, Chapter 1 reviews the required background in X-ray imaging, from the physical fundamentals to the state-of-the-art technologies. Chapter 2 introduces the novel pixel architecture for digital direct X-ray imaging, describing its main building blocks and principles of operation. The low-power and compact area CMOS pixel circuits specifically developed in order to implement the new DPS architecture are explained in detail in Chapter 3. Based on all the above proposals, Chapter 4 describes the different circuit designs integrated in 0.18μm 1P6M CMOS technology, either as pixel or array test chips. Experimental results are reported in Chapter 5, including both elctrical and X-ray tests together with a comparison respect to the state-of-the-art X-ray active pixels. Finally, conclusions are summarized in Chapter 6 in order to highlight the main contributions of the present thesis and its mid- and long-term future work.

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- Desarrollo de un nuevo chip y sistema electrónico para captura de imágenes radiológicas (Demostrador: Nuevo sistema de biopsia mamaria).

  PHOCOPIX-5: PROFIT-Tractor FIT-330101-2005-4.

  Partners: Unidad de Diagnóstico por la Imagen de Alta Tecnología (UDIAT) S.A., Instituto de Física de Altas Energías (IFAE-UAB) EMSOR S.A. and Sociedad Española de Electromedicina y Calidad (SEDECAL).

- Detector de rayos X de tipo pixel y su electrónica de captura integrada para aplicaciones de tratamiento de imagen médica.

  PHOCOPIX: PLAT-INN (AGAUR) RDITSCON05-1-0015.

  Partners: Unidad de Diagnóstico por la Imagen de Alta Tecnología (UDIAT) S.A., Instituto de Física de Altas Energías (IFAE-UAB) EMSOR S.A. and Sociedad Española de Electromedicina y Calidad (SEDECAL).

- Desarrollo de un sistema digital de biopsia estereotáxica de mama en tiempo real sobre MediPix.

  BIOPSYONPHOCOPIX: PROFIT FIT-350300-2007-37.

  Partner: Unidad de Diagnóstico por la Imagen de Alta Tecnología (UDIAT) S.A.

- DEAR MAMA++: Desarrollo de un sistema digital de biopsia estereotáxica de mama en tiempo real sobre MediPix.

  BIOPSYONPHOCOPIX-2: AVANZA TSI-020302-2009-82.

  Partners: Unidad de Diagnóstico por la Imagen de Alta Tecnología (UDIAT) S.A. and EMSOR S.A.

- Neutron detector and imaging system.

  NEUS: INNPACTO IPT-2012-0662-420000.

  Partner: X-Ray Imatek S.L.

Pixel Architecture | 2

As mentioned in the previous chapter, the core of any ROIC for hybrid X-ray digital imagers is the array of active pixels called DPS cells. This chapter proposes a new DPS architecture for X-ray imagers, including its basic building block description and principle of operation. The specific CMOS circuits proposals for its implementation are presented in Chapter 3.

2.1 DPS Architecture and Operation Proposal

From a functional point of view, the ideal requirements for a read-out pixel circuit in X-ray imaging can be listed as follows:

High spatial resolution. Integrated circuits have evolved to current submicron CMOS technologies, thus more circuitry, and therefore more functionality, can be included in smaller areas. In order to obtain a high spatial resolution system, a compact but fully-functional design is wanted. In this sense, extensive circuit reuse is proposed here to obtain a good enough trade-off.

Lossless charge-integration. Photon-counting charge losses due to pile-up and charge-sharing effects can introduce severe losses of information as explained in Section 1.2.4. In order to overcome these issues, a novel lossless scheme for charge-integration will be proposed.

Low-power. The heating of the ROIC chip can be easily transferred to the detector, increasing its dark-current. By exploiting the sub-threshold operation of the transistors together with the extensive circuit reuse already mentioned, a low-power solution can be obtained to minimize this drawback.

Biphasic current sensing. Different applications may require different materials for the detector. For example, X-ray Si detectors show good performance collecting either electrons or holes, while CdTe detector based systems usually work collecting electrons due to the low mobility of its holes. Therefore, the proposed pixel must be flexible enough to deal with both positive or negative charge collection.

Reduced crosstalk. In order to prevent blurring effects at image level, crosstalk between neighboring pixels should be minimized. For this purpose, digital-only communications are preferable at array level. Based on this strategy, the local generation at pixel level of all analog reference and bias levels is proposed here. As a positive side effect, interconnectivity between pixels is reduced and technology requirements at layout level are relaxed (e.g. number of metal layers). On the other hand, the complexity of pixel circuitry tends to increase.

Built-in test capability. Digital direct hybrid X-ray imagers are complex systems since they require the hybridization of the detector with its respective ROIC. The cost is thus increased while the yield is reduced. This is the reason why it is useful to include a local test mechanism inside each pixel to verify the correct behavior of the CMOS pixel arrays before hybridization. As a positive side effect, the same built-in mechanism can be used after hybridization to test the whole system without requiring any X-ray source.

FPN compensation. In general, mismatching between pixels may introduce FPN in the output image. In addition, certain applications can require different behavior for pixels in a particular image ROI in terms of charge-to-data gain conversion. In order to compensate for FPN and to bring flexibility to the system, an individual gain programming mechanism should be also added into each pixel.

Dark-current cancellation. X-ray detectors with high dark currents can experiment important restrictions in both their dynamic range and maximum acquisition time, also with an increase of pixel noise. An specific circuit for the auto-calibration and compensation of detector dark current may be necessary at pixel level.

Long acquisition time capability. For the system to be flexible enough to be used in X-ray applications where large acquisition times are required, pixel analog storing circuits must exhibit very low leakage.

High frame rate. Digital communications must assure good performance at communication speeds of 50Mbps or higher in order to meet demands of high frame rate applications.

High full-scale. Certain applications may need a high charge full-scale ($100Me^{-}$ or even more), which must be taken into account in terms of pixel sensitivity and capacity.

Considering the above requirements, the proposed architecture for the digital active pixel is shown in Fig. 2.1(a), where V_{com} is the common detector high-voltage biasing, I_{sens} the individual X-ray pixel detector output current, and $b_{in/out}$ the digital serial I/O ports of the daisy chained DPS cells.

Regarding the operation of this pixel architecture, two modes can be distinguished, acquisition and communication, as illustrated in Fig. 2.1 (b). In acquisition mode, signal processing inside the active pixel starts with the auto-calibration of the detector dark-current (I_{dark}) in absence of signal for its posterior cancellation. Also during acquisition, arbitrary test patterns (I_{test}) can be optionally added to the effective signal (I_{adc}), which is digitally quantified by the in-pixel charge-integration ADC. Once in communications phase, the digital output of the ADC (d_{adc}) is serially read-out through b_{out} while b_{in} is used to program-in, at the same time and without any extra speed cost, the gain (V_{th}) of the ADC through the (digital word d_{dac}). This gain is customized individually for each pixel by a local digital to analog converter (DAC) in order to compensate for any FPN in the next frame.

As observed in the same Fig. 2.1(a), analog references and biasing levels are locally generated inside each active pixel, thus connectivity between pixels is limited to digital signals only.

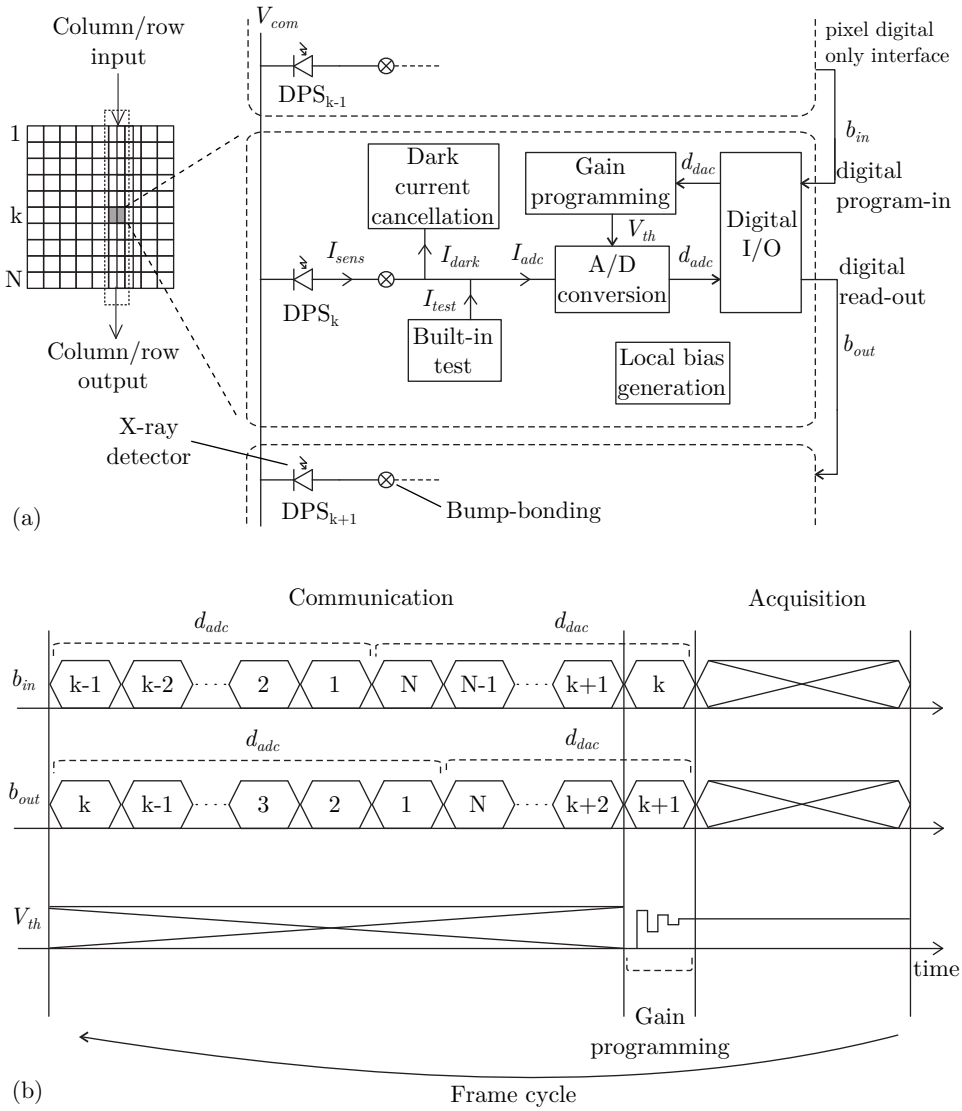


Figure 2.1 | Overall architecture (a) and operation (b) of the proposed DPS for digital X-ray imaging.

2.2 Charge-Integration and Digital Conversion

In general, charge-integration pixels integrate the input signal during a certain acquisition time. In most approaches reported in the literature study of Section 1.3, each pixel integrator circuit is read-out in the analog domain. In these cases, crosstalk between neighboring pixels and signal degradation may be significant. Therefore, A/D conversion must be implemented inside each pixel in order to reduce crosstalk and to obtain digital only communications pixels.

Having in mind the requirements for a compact and low-power pixel design, predictive A/D conversion is preferred over direct (e.g. flash) or algorithmic (e.g. successive approximation) architectures, as its internal feedback allows strong relaxation of the analog parts reducing area and power consumption [80].

For our purposes, sigma-delta modulators ($\Sigma\Delta$M) can be taken as the best example of predictive A/D conversion. In general, $\Sigma\Delta$M is built from a pulse modulator in cascade with a digital filter. The role of the pulse modulator is to quantize (typically at resolutions as low as 1-bit) the amplitude of the error between input signal and a given prediction while a feedback DAC is updating this signal prediction, so performing error correction. As a result of this modulation, the quantization error in the pulse stream is pushed to higher frequencies. Hence, the low-pass digital filter is in charge of cutting these frequency components and complete the discretization of the signal in time to finally obtain the digital output word (d_{adc}) at the Nyquist rate.

Two different circuit approaches can be selected regarding the resulting modulator: pulse width modulation (PWM) and pulse density modulation (PDM) [81]. The PWM approach scheme, also known as time-to-first-spike, is equivalent to a classic single or double ramp integrating ADC and requires the use of an external clock signal for the conversion. On the other hand, the asynchronous PDM approach, also called integrate-and-fire or spike-counting, is based on the scheme of Fig. 2.2(a) where the input signal coming from the sensor I_{adc} is first compared to the prediction and error is amplified by the high-gain but band-limited stage. The result is codified at 1-bit by the quantizer and the output pulse stream (V_{pdm}) is then fedback by the DAC to update the prediction. Thus, a clock signal is not needed and

dynamic power consumption is proportional to input signal amplitude. For these reasons, the PDM strategy is chosen here to meet low crosstalk and low power consumption requirements as listed in previous Section 2.1.

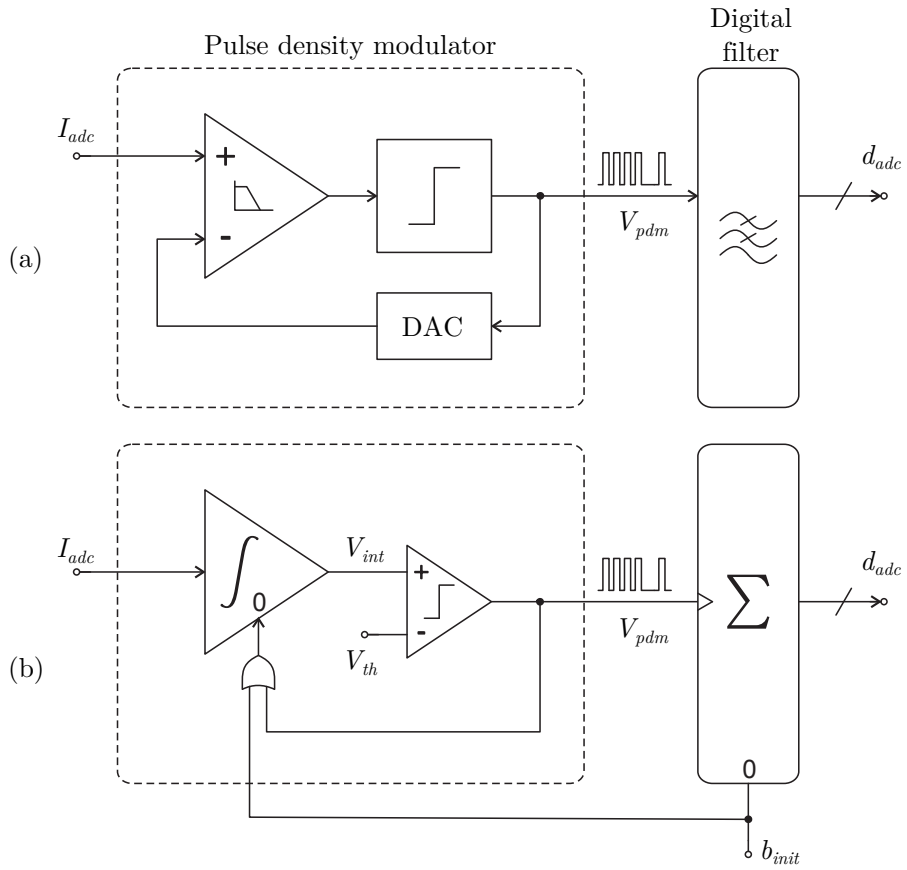


Figure 2.2 | General scheme (a) of a PDM predictive ADC, and asynchronous application to active pixel design (b).

In the context of CMOS circuits for DPS design, the general scheme of Fig. 2.2(a) is simplified to Fig. 2.2(b). Here, the high-gain and band-limited stage is replaced by a first order integration, which amplifies the low-frequency components of I_{adc} into V_{int}; the integrated signal is quantified by a comparator according to a given threshold (V_{th}), and resulting

pulses V_{pdm} are fedback to reset the analog integrator, so performing the same effect as a negative feedback from a single bit DAC. Concerning the first-order low-pass digital output filter, this block can be implemented by a simple integrator (i.e. counter) whose losses are controlled by the frame initialization signal (b_{init}).

A classic topology of the simplified PDM modulator of Fig. 2.2(b) is shown in Fig. 2.3. The analog integrator is implemented here by the C_{int}-based capacitive transimpedance amplifier (CTIA) stage. Apart from integrating I_{adc} into V_{int}, so amplifying the low-frequency components of the input signal, the CTIA is also in charge of compensating for the effects of the input parasitic capacitance C_{par} by keeping the X-ray detector biased at the constant potential V_{ref}. Due to small values for C_{int}, extra capacitor (C_{CDS}) is usually added to implement a correlated double sampling (CDS) mechanism and reduce the low-frequency noise generated by the CTIA stage.

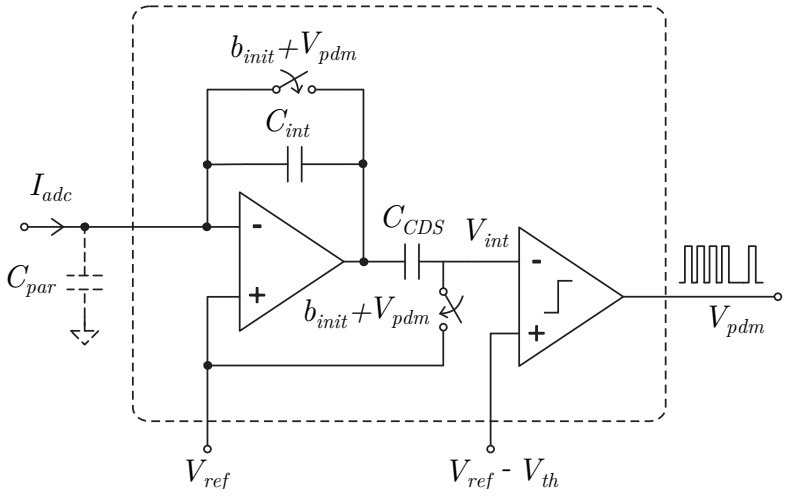


Figure 2.3 | Classical scheme for the PDM part of the in-pixel integrate-and-fire ADC ($I_{adc} > 0$ case).

The operation of the circuit of Fig. 2.3 starts with the frame initialization (b_{init} high), while the analog integrator based on C_{int} is reset and the offset and low frequency noise of the first stage are sampled and stored in C_{CDS}. Once in acquisition (b_{init} low), the detector quasi-static current I_{adc} is integrated into C_{int}, and C_{CDS} implements CDS noise cancellation at the

integrator output V_{int}. Finally, when the swing of the integrated signal V_{int} reaches the fixed threshold V_{th}, the comparator generates a spike usually called event (V_{pdm} high), which is sent to the digital counter of Fig. 2.2(b) and it is also fed back to the first stage as the reset signal. The ideal waveforms of this operation cycle are illustrated in Fig. 2.4(a).

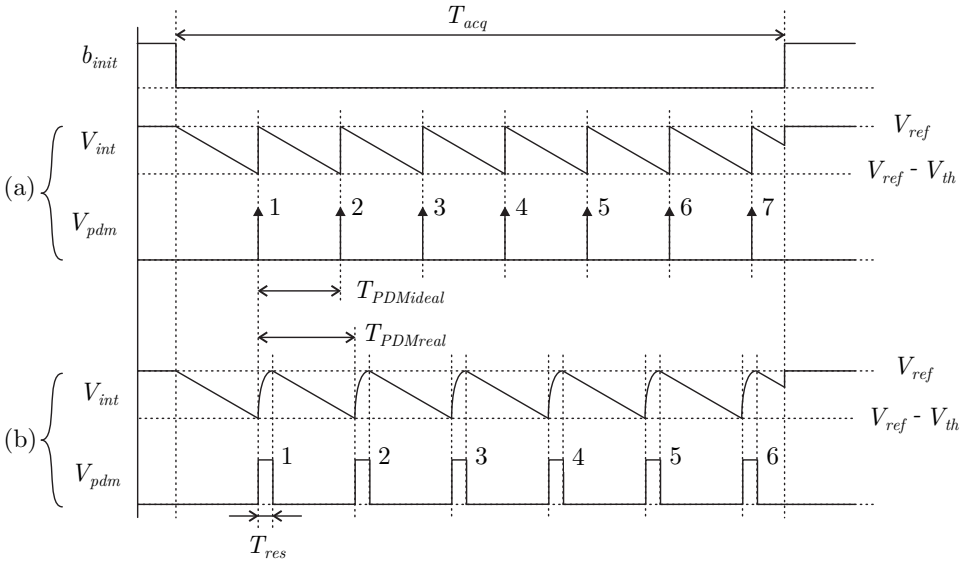


Figure 2.4 Ideal (a) and real (b) operation of the classical PDM scheme of Fig. 2.3 ($I_{adc} > 0$ case). In this example, 1 spike is lost in real operation (6 spikes) compared to the ideal behavior (7 spikes).

At the end of acquisition time T_{acq}, the A/D conversion is completed. The digital counter state according to this ideal operation should be:

$$q_{adcideal} = \lfloor n_{adcideal} \rfloor \tag{2.1}$$

$$n_{adcideal} = \frac{T_{acq}}{T_{PDMideal}} = \frac{T_{acq}}{C_{int}V_{th}} I_{adc} \rightarrow f_{PDM} = \frac{1}{T_{PDM}} = \frac{I_{adc}}{C_{int}V_{th}} \tag{2.2}$$

where $\lfloor x \rfloor$ stands for the floor integer approximation of x.

Due to the low biasing currents of the analog integrator and comparator in Fig. 2.3 required to achieve low power consumption, the pulse duration in Fig. 2.4(a) can not be null in practice. Hence, some time (T_{res}) is lost at each spike generation in order to reset the analog integrator, as depicted in Fig. 2.4(b). Following Fig. 2.3, no integration in C_{int} is possible during this reset time, so the resulting spike frequency in Fig. 2.4(b) is decreased compared to Fig. 2.4(a). Applying the same analysis as in Eqs. 2.1 and 2.2:

$$q_{adcreal} = \lfloor n_{adcreal} \rfloor \tag{2.3}$$

$$n_{adcreal} = \frac{n_{adcideal}}{1 + \frac{T_{res}}{T_{acq}} n_{adcideal}} \tag{2.4}$$

This non-linear effect is specially noticeable at full-scale of I_{adc}, where $T_{PDMideal}$ tends to be comparable to T_{res}. For a given integer digital output $0 < |q_{adc}| < d_{fullscale}$, the maximum non-linearity error is reached at $n_{adcideal} \equiv d_{fullscale}$. In order to ensure a peak deviation below half least significant bit (LSB), according to Eqs. 2.1 to 2.4:

$$max\left(|n_{adcreal} - n_{adcideal}|\right) = \left| \frac{d_{fullscale}}{1 + \frac{T_{res}}{T_{acq}} d_{fullscale}} - d_{fullscale} \right| \leq 0.5LSB = \frac{1}{2} \tag{2.5}$$

so, for $d_{fullscale} \gg 1$:

$$T_{res} \leq \frac{T_{acq}}{2d_{fullscale}^2} \tag{2.6}$$

For example, a 10-bit pixel with $T_{acq} = 100$ms requires $T_{res} < 50$ns, which demands high power consumption for the circuits of Fig. 2.3. As shown in Fig. 2.5, for a 10-bit output dynamic range with T_{res}/T_{acq} ratios as low as 0.01%, deviations already reach values of 10% or more. Hence, the only solution to maintain the nominal full scale and to reduce non-linearity using the architecture of Fig. 2.3, is the increase of biasing currents for the analog

circuits, leading to an increase of power consumption for the whole array of pixels.

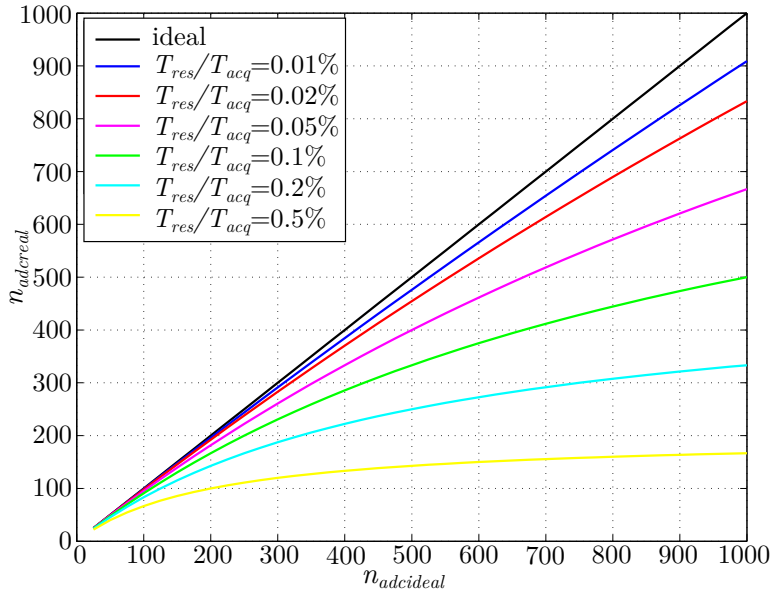


Figure 2.5 | Ideal and real n_{adc} curves for different T_{res}/T_{acq} ratios according to Eq. 2.5.

In order to overcome these reset time issues in conventional spike-counting circuits the alternative approach of Fig. 2.6 is proposed. The design proposal does not use a hard short-circuit but a novel switched capacitor technique to reset C_{int}.

In this case, the principle of operation is as follows: during frame initialization (b_{init} high), the analog integrator is reset, while $C_{reset/CDS}$ remains connected to V_{int}; once in acquisition (b_{init} low), the sensor quasi-static current I_{adc} is integrated in C_{int} while $C_{reset/CDS}$ is tracking the offset, the low frequency noise and the output signal itself of the first stage; finally, when the fixed threshold V_{th} is reached, the comparator generates a spike (V_{pdm} high), which is sent again to the digital counter of Fig. 2.2(b) and causes $C_{reset/CDS}$ to be connected to the input of the analog integrator. As a result, the charge stored in C_{int} is compensated by $C_{reset/CDS}$ and the reset is performed.

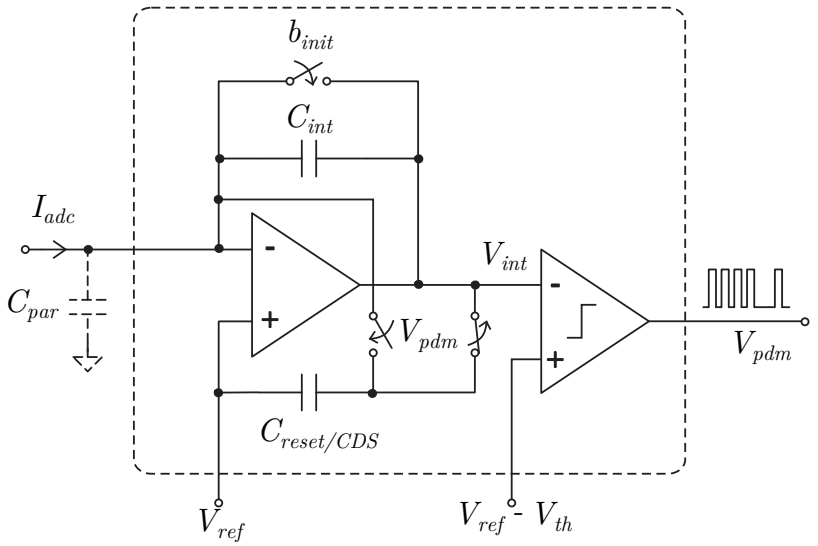


Figure 2.6 | Novel scheme proposed for the PDM part of the in-pixel integrate-and-fire ADC ($I_{adc} > 0$ case).

However, and unlike the classical implementation of Fig. 2.3, this novel strategy does not block the integration of I_{adc} in C_{int} during the reset time. In fact, the proposed scheme behaves like an analog APS design from this viewpoint, since the integrator is operating in continuous-time during the full acquisition time. Hence, integration of both the charge coming from I_{adc} and from $C_{reset/CDS}$ are linearly combined in C_{int} during the reset phase. This fact can be easily seen in Fig. 2.7(b), where V_{int} does not return to the reference level V_{ref} after each reset. In consequence, the spike frequency is no longer dependent on the reset time and matches the ideal target of Fig. 2.7(a). This behavior is maintained even for high photon fluxes, which in practice allows the extension of the dynamic range. In fact, just a minimum reset time is required to ensure complete charge redistribution between $C_{reset/CDS}$ and C_{int}, but its particular value is not relevant.

Since $C_{reset/CDS}$ is continuously sampling the offset and the low frequency noise of the analog integrator, it already implements the CDS function. Hence, the C_{CDS} element in Fig. 2.3 can be avoided, and no extra capacitors are finally added. In practice, technology mismatching between C_{int}

and $C_{reset/CDS}$ causes an equivalent small offset in V_{th}, but these gain errors are negligible compared to the absolute process deviations of C_{int}. Furthermore, this offset can be fully compensated by the DPS gain programming capabilities explained in Section 2.3. Also, charge injection is similar to conventional spike-counting due to the fact that the b_{init}-switch is not operated during A/D conversion and V_{pdm}-switches are working complementary.

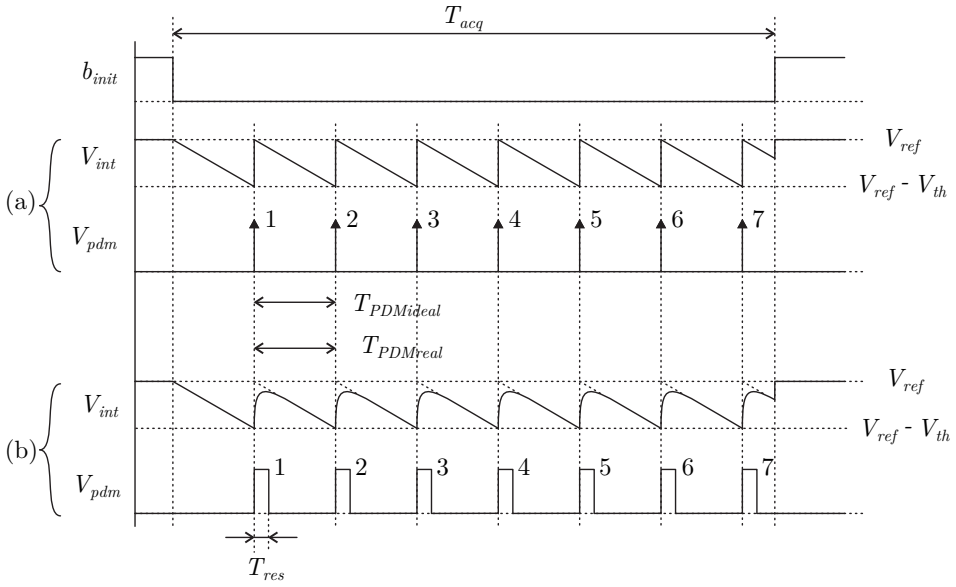


Figure 2.7 Ideal (a) and real (b) operation of the novel PDM scheme of Fig. 2.6 ($I_{adc} > 0$ case). As shown, no spikes are lost in real operation (7 spikes) compared to the ideal behavior (7 spikes).

The obtained output pulse stream V_{pdm} during acquisition time T_{acq} is counted and stored as d_{adc} in the in-pixel digital registers as explained in Section 2.5.

2.3 Individual Gain Programmability

According to the pixel architecture proposal of Fig. 2.1, the gain of the built-in ADC can be externally controlled through d_{dac} in every acquisition frame. Despite the consequent increase of pixel circuit complexity, this new feature has two practical advantages.

First, the independent gain programmability of each individual pixel can be seen as a compensation mechanism for the cancellation of any mismatching between pixels. This technological mismatching, caused by asymmetries either between X-ray detectors or between CMOS read-out circuits, is the main source of FPN in the digital output image.

Second, having the possibility of changing ADC gain for the whole array of pixels can be also used to adjust imager sensitivity to each particular X-ray application and detector-type. Hence, the flexibility of the resulting imager is strongly improved.

As already explained in Section 2.1, the pixel digital communications scheme proposed in Fig. 2.1(b) already allows to send a different programming code d_{dac} to each individual active pixel without any penalty on its read-out speed.

This d_{dac} code adjusts the A/D conversion gain by programming the value of the threshold voltage of the comparator of Fig. 2.6. Indeed, controlling V_{th} is equivalent to selecting the conversion gain from I_{adc} to $n_{adcideal}$ according to Eq. 2.2. Hence, a DAC block is needed inside each pixel to convert the digital code d_{dac} into the corresponding voltage level V_{th} and store it temporally during acquisition time. Moreover, as the pixel is required to be able to deal with positive and negative charge integration, the programmed threshold value V_{th} has to be either positive or negative respect to the signal baseline level V_{ref} of Fig. 2.6, depending on the charge collection mode selected.

Taking into account the above functional requirements together with the compact pitch target, the use of the switched-capacitor DAC [82] of Fig. 2.8 is proposed. This DAC block operates during I/O communications phase only, when d_{adc} is serially programmed through b_{in} according to the chronogram of Fig. 2.1(b).

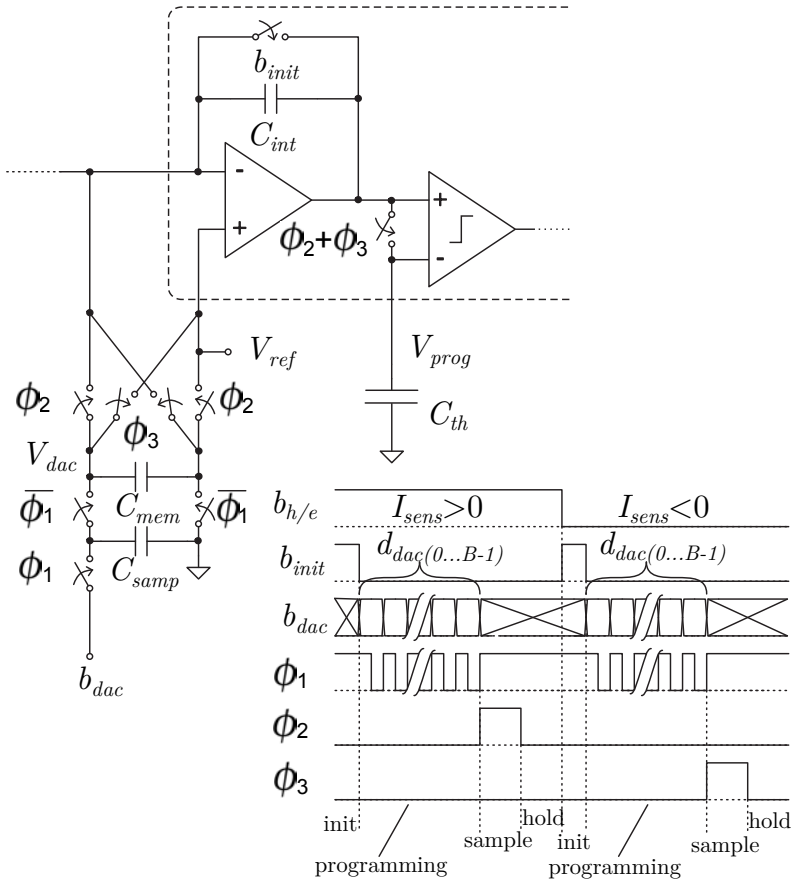


Figure 2.8 Simplified scheme and operation of the proposed in-pixel gain programming. Boxed blocks are reused from the PDM stage of Fig. 2.6.

The principle of operation is as follows. The first entering bit $d_{dac}(0)$ is the LSB, which charges C_{samp} during the high state of ϕ_1 to a reference voltage (V_R) if $d_{dac}(0) \equiv 1$, or to ground if $d_{dac}(0) \equiv 0$. For simplicity, V_R is typically the supply voltage (V_{DD}). When ϕ_1 is low, the charge in C_{samp} is redistributed between C_{samp} and C_{mem}. Holding the charge of C_{mem} for ϕ_1 high again, the next significant bit of d_{dac} charges C_{samp} to the corresponding value and the process is iterated until the most significant

bit (MSB) of the B-bits length word of d_{dac} is handled. If $C_{samp} \equiv C_{mem}$, the resulting programmed voltage level in C_{mem} is:

$$V_{dac} = V_R \sum_{i=0}^{B-1} \frac{d_{dac}(i)}{2^{B-i}} \geq 0 \tag{2.7}$$

After locally generating each particular V_{prog} level inside each pixel, the charge stored in C_{mem} is transferred to C_{int} using the same CTIA of the PDM stage of Fig. 2.6. Since the pixel has to be able to deal with either positive or negative input charges, the common digital selector bit $b_{h/e}$ is introduced to control ϕ_2 and ϕ_3, and thus, the polarity of this charge transfer. As a result:

$$V_{prog} = V_{ref} + (-1)^{b_{h/e}} \frac{C_{mem}}{C_{int}} V_{dac} \tag{2.8}$$

The reuse of the CTIA block means important silicon area and power consumption savings per DPS, but even more important, the low output impedance of this block allows to copy the resulting V_{int} in a high density non-linear metal oxide semiconductor (MOS) capacitor C_{th}. In this way, the effect of switch leakage during acquisition can be attenuated. Hence, the final expression of the equivalent threshold stored in this analog memory is:

$$V_{th} = (-1)^{b_{h/e}} \frac{C_{mem}}{C_{int}} V_R \sum_{i=0}^{B-1} \frac{d_{adc}(i)}{2^{B-i}} \tag{2.9}$$

In practice, $C_{int} \equiv C_{mem}$, so $|V_{th}| = |V_{dac}|$. Another advantage of using the same CTIA as the PDM modulator is that the comparator already compensates the input voltage offset during A/D conversion.

Finally, the sampling and hold switch implementation driven by $\phi_2 + \phi_3$ in Fig. 2.8 need to exhibit a very low leakage current in order to not degradate V_{th} during long acquisition times.

2.4 Built-In Test Capability

As mentioned in Section 2.1, and due to the extra cost of hybridizing imagers, the inclusion at pixel level of a pre-hybridization test mechanism is recommended. The aim of this mechanism is to check the full signal path inside and outside the active pixel, emulating the external signal without requiring any X-ray source. It works during the acquisition phase by injecting the input charge pulses I_{test} of Fig. 2.1. The polarity of these charge injections is selectable using the $b_{h/e}$ signal to meet the biphasic current sensing requirement.

Taking the above idea, a compact block implementation is proposed in Fig. 2.9. Most of this test circuitry is shared with the gain programming DAC introduced in Section 2.3 as both functions are not overlapped in time. Apart from the corresponding silicon area and power consumption reductions, the use of the same switched capacitors, for both test and threshold programmability, minimizes the effects of technology mismatching between C_{mem} and C_{int} in test mode.

The principle of operation for the generation of I_{test} is very similar to the mechanism of Fig. 2.8: during acquisition, C_{mem} is usually biased at the common test amplitude $V_{testamp}$; when a test stimulus is requested ($b_{testinj}$ high), the charge stored in C_{mem} is injected directly to the ADC input according to the polarity specified by $b_{h/e}$ and controlled by ϕ_1 and ϕ_2 in Fig. 2.9. The resulting change at the integrator output only due to I_{test} is:

$$\Delta V_{int} = (-1)^{b_{h/e}} \frac{C_{mem}}{C_{int}} V_{testamp} \tag{2.10}$$

Typically $C_{mem} \equiv C_{int}$, so the amplitude change $|\Delta V_{int}| \equiv V_{testamp}$. The separate control of amplitude and timing signals of the test pattern is of special interest to simplify external components and reduce noise in test mode. In fact, $V_{testamp}$ is the only external analog signal of the DPS which can inject noise from the outside, but it has no contribution during normal acquisition ($b_{testinj}$ low). Even in test mode, the external control of a constant DC voltage reference is simpler than distributing dynamic analog signals inside the pixels array.

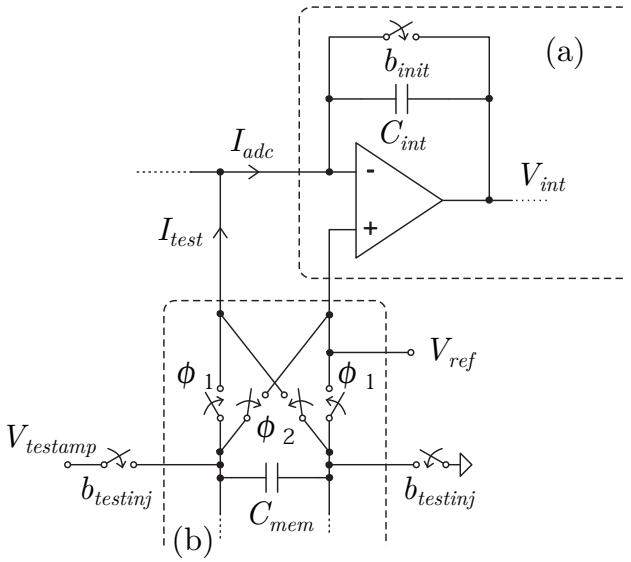


Figure 2.9 Proposed scheme for the in-pixel built-in test. Boxed elements are reused from the PDM stage (a) of Fig. 2.6 and the gain programming scheme (b) of Fig. 2.8.

In order to perform crosstalk or mismatching studies without increasing the number of external signals, test groups can be defined (e.g. A and B) and test patterns can be hardwired in the final imager by distributing the corresponding $V_{testampA,B}$ and/or $b_{testinjA,B}$ connectivity maps. In Fig. 2.10, two examples of test patterns are presented, where black and white pixels would be connected to A and B test signals, respectively.

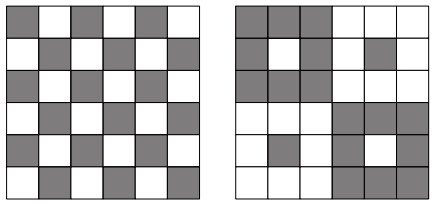


Figure 2.10 Examples of hardwired test pattern maps using the built-in pixel test mechanism of Fig. 2.9 in two pixel groups.

2.5 Digital Interface

As explained in Section 2.1, the digital I/O block of Fig. 2.1 is used both for pulse counting during acquisition phase, and for serial read-out and program-in of signal and gain data during communications phase, respectively. For these purposes, the reconfigurable digital I/O block of Fig. 2.11 is proposed, where B is the length of the equivalent register.

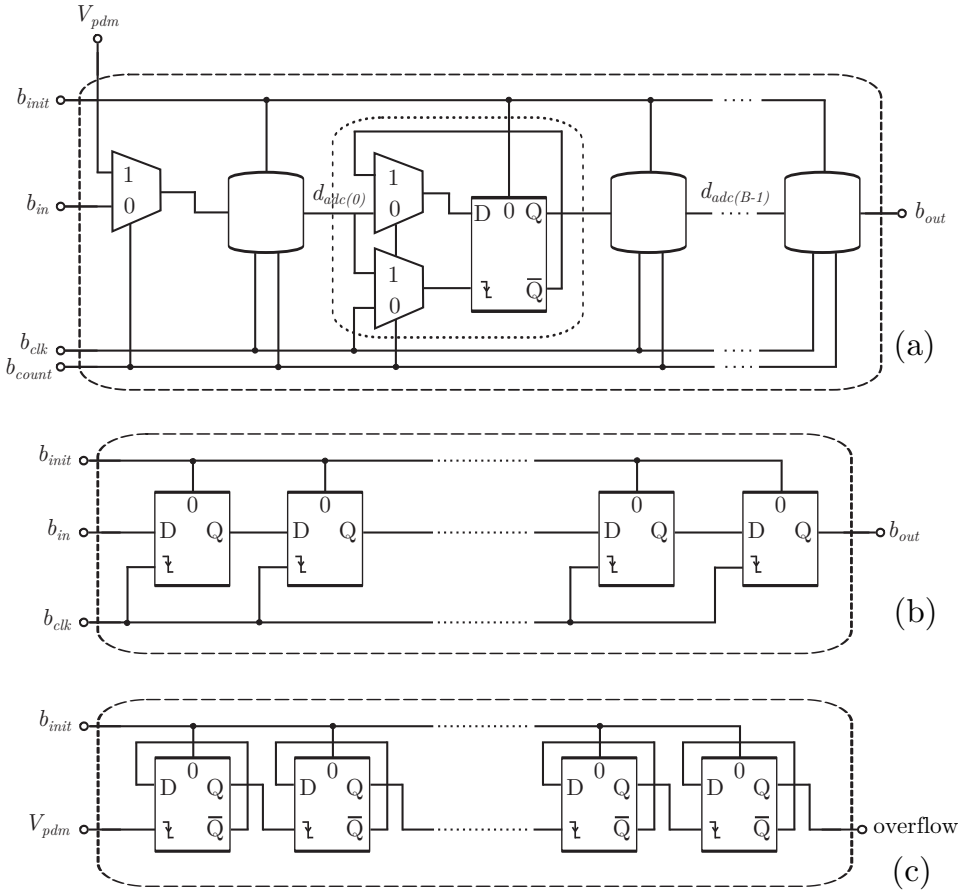


Figure 2.11 | Reconfigurable digital I/O block scheme (a) proposed for pixel communication (b) and acquisition (c).

The operation of the circuit of Fig. 2.11 can be described as follows. Before the first acquisition, this stage is configured as shift-register for communications (b_{count} low) following Fig. 2.11(b) and the individual pixel gain (d_{dac}) is serially programmed through b_{in} using b_{clk} as clock signal. During the same phase, the pixel DAC of Fig. 2.8 generates and stores the corresponding V_{th} level. Once in acquisition, the registers are reset (b_{init} high), and the digital I/O block is reconfigured as a ripple counter (b_{count} high) following Fig. 2.11(c) which digitally integrates the pulse stream V_{pdm} coming from the PDM stage. During this phase, the output of the last register is used as overflow flag. When set, the analog frontend stage is reset to avoid any pulses that would re-start the counting from the first code. Finally, a serial shift-register is again implemented (b_{count} low) to read-out the digital signal data while at the same time the individual pixel gain for the next acquisition phase is programmed.

For evaluation purposes, the pixel digital interface proposed in this section is compared with pseudo-random counter-based solutions, which already include shift registers. In particular, pseudo-random maximum length sequence (PRMLS) counters [83] are of special interest, since their linear feedback allows to exploit the full dynamic range of a B-bit classic counter (2^B). Fig. 2.12 shows the structure of a PRMLS-based solution for the 10-bit design case, with its XOR feedback network (ploynomial $1 + x^6 + x^9$).

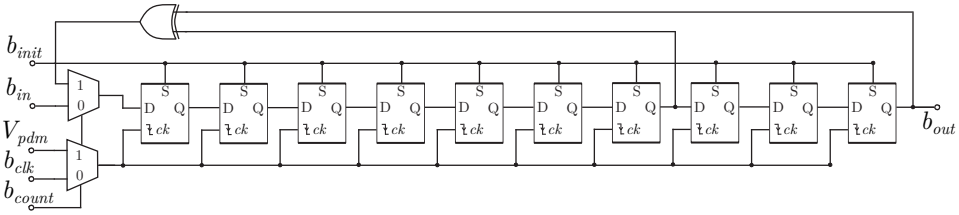


Figure 2.12 | 10-bit PRMLS reconfigurable counter. For b_{count} low, the structure behaves as a shift register.

Compared to the digital interface of Fig. 2.11, it is clear that reconfigurable PRMLS counters need less gate resources, thus more compact pixels may be obtained. However, their pseudo-random nature commonly require a look-up-table (LUT) for data decodification. This fact may become a practical bottle neck in large dynamic range or high speed image systems. Further-

more, the number of transitions, as changes in logical state at each flip-flop output, is higher compared to ripple counters.

As a particular example, Fig. 2.13 shows the ratio between transitions of a PRMLS counter and a ripple counter for the 10-bit case design. After only few counts, the number of transitions of a PRMLS counter is already more than twice the number of transitions of the corresponding ripple version.

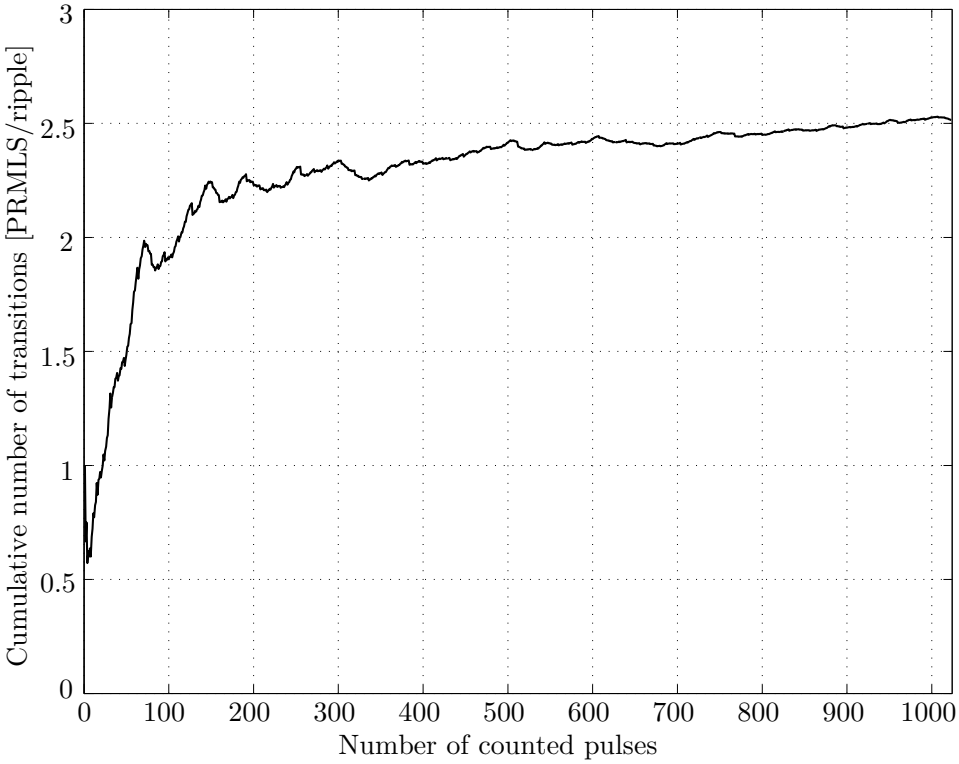


Figure 2.13 | Ratio between transitions of PRMLS and ripple counters for the 10-bits case design.

Based on the D-type flip-flops for the two alternatives, ripple and PRMLS counters can be compared in terms of number of transitions at full-scale and of required extra circuitry for their reconfigurability as shift-registers. The theoretical results of these comparisons are presented in Fig. 2.14 for different design cases regarding the number of bits of the counters.

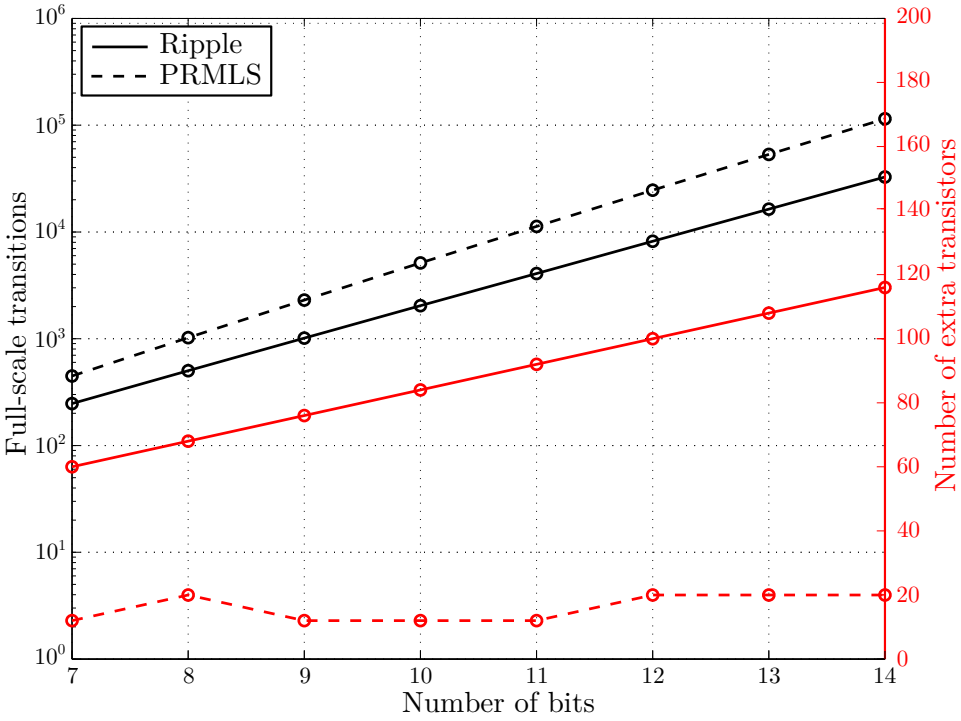


Figure 2.14 | Full-scale transitions (black) and extra transistors (red) in reconfigurable ripple (solid line) and PRMLS (dashed line) counters for 7 to 14-bit design cases.

As expected, configurable ripple counters require more extra circuitry compared to PRMLS counterparts, leading to larger pixel area occupancy for the digital blocks.

On the other hand, the number of logical transitions is much higher when using PRMLS counters, which is directly related with the dynamic power consumption of the digital part. Moreover, ripple counters power consumption exhibits a fixed weight for each position with the LSB winning almost 50% of the total consumption. Hence, the circuit optimization of ripple counters for low-power operation seems more feasible than in PRMLS counters, where power consumption is pseudo-randomly distributed along all the register positions.

Finally it is important to note that logical transitions are not only causing power consumption in the digital blocks but also crosstalk to the analog parts of the active pixel. Thus, this undesired effect can be more attenuated in ripple counters than in PRMLS solutions by following proper layout floorplans.

CMOS Pixel Circuits | 3

In previous chapter, a high level description of the main internal circuit blocks of the proposed read-out pixel architecture has been presented together with their operation modes. In this chapter, CMOS circuit implementations of these pixel blocks, to obtain all the desired pixel functionality, are proposed. In this sense, schematics at transistor level are exposed and main design parameters and challenges are discussed to meet the performance requirements introduced in Section 2.1.

3.1 Asynchronous A/D Conversion

As argued in Section 2.2, digitization of input current from the X-ray direct conversion detector should be already performed at pixel level in order to achieve low crosstalk between pixels. For low-power consumption and compact area, an asynchronous integrate-and-fire ADC architecture is chosen for the proposed pixel using a novel CTIA reset scheme presented in the circuit of Fig. 2.6 for lossless charge-integration.

Before presenting the CMOS circuit implementation proposal for the asynchronous PDM stage of Fig. 2.6, some modeling considerations will be discussed about CTIA being used for detector current-reading. For such a purpose, Fig. 3.1(a) includes a general model of this scenario, where I_{det} stands for the detector current to be sensed, while R_{det} and C_{det} are the resistive and capacitive parts of the detector impedance, respectively.

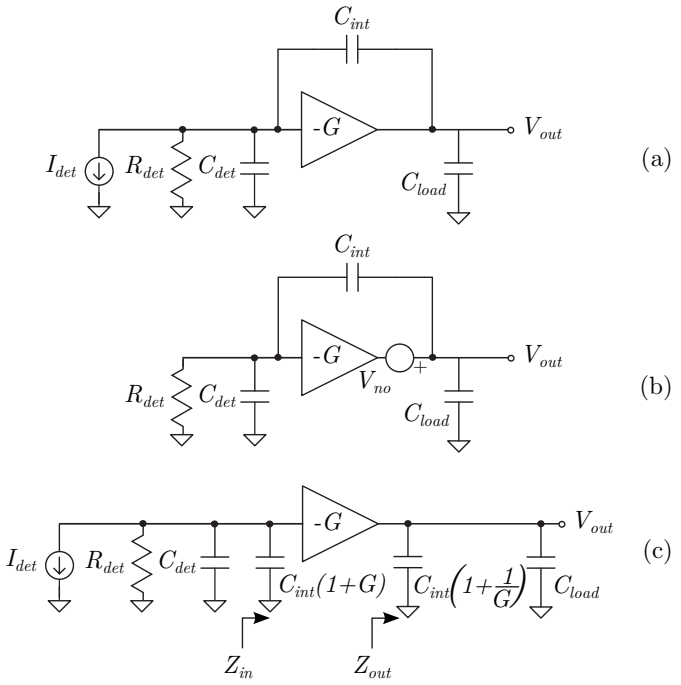


Figure 3.1 General model of CTIA-based detector current-reading for STF (a), NTF (b) and impedance splitting (c).

By defining signal transfer function (STF) as

$$STF \doteq \frac{V_{out}}{I_{det}} \tag{3.1}$$

and considering finite open loop gain (G) for the CTIA OpAmp, the resulting STF can be found to be:

$$STF = \frac{R_{det}G}{R_{det}[C_{det} + (G+1)C_{int}]s + 1} \tag{3.2}$$

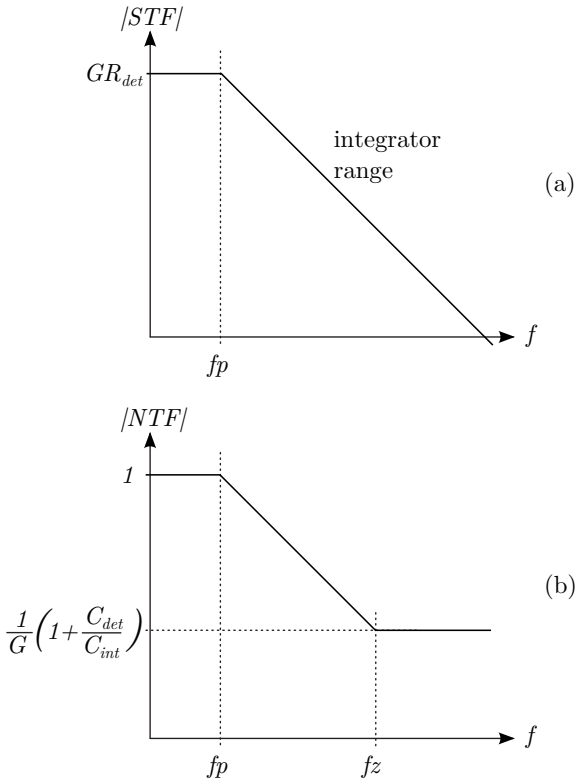


Figure 3.2 | Bode magnitude representation of STF (a) and NTF (b) for the corresponding models of Fig. 3.1.

The equivalent Bode transfer function is plotted in Fig. 3.2(a), with:

$$fp = \frac{1}{2\pi} \frac{1}{R_{det}[C_{det} + (G+1)C_{int}]} \tag{3.3}$$

In case of large enough open loop OpAmp gain, the entire stage behaves as the wanted continuous-time integrator:

$$STF \underset{G\to\infty}{=} \frac{1}{C_{int}s} \tag{3.4}$$

and the own impedance of the detector can be neglected.

Concerning the equivalent noise transfer function (NTF) of Fig. 3.1(b):

$$NTF \doteq \frac{V_{out}}{V_{no}} \tag{3.5}$$

where V_{no} stands for the OpAmp output noise voltage, its expression can be written as:

$$NTF = \frac{R_{det}(C_{det} + C_{int})s + 1}{R_{det}[C_{det} + (G+1)C_{int}]s + 1} \tag{3.6}$$

The corresponding Bode transfer function is shown in Fig. 3.2(b) with same pole as STF and the extra zero:

$$fz = \frac{1}{2\pi} \frac{1}{R_{det}(C_{det} + C_{int})} \tag{3.7}$$

Again, for practical values of OpAmp open loop gain and frequency range above fz, the resulting transfer function can be rewritten as:

$$NTF \underset{\substack{G\to\infty \\ f>fz}}{=} \frac{1}{G}\left(1 + \frac{C_{det}}{C_{int}}\right) \tag{3.8}$$

which is telling the output noise voltage of the full CTIA stage is similar to the equivalent input noise voltage of the OpAmp scaled by the detector parasitic to integration capacitance ratio.

Finally, the transcapacitance of Fig. 3.1(a) can be split according to Miller effect [84], obtaining the equivalent circuit of Fig. 3.1(c). This decoupling results in an equivalent input impedance seen from the detector viewpoint as:

$$Z_{in} = \frac{1}{1+G} \frac{1}{C_{int}s} \tag{3.9}$$

while the equivalent load impedance seen from the OpAmp block results in:

$$Z_{out} = \frac{1}{[(1+\frac{1}{G})C_{int} + C_{load}]s} \tag{3.10}$$

Coming back to the CMOS implementation of the PDM stage presented in Fig. 2.6, its circuit is proposed in Fig. 3.3. The modulator is composed of a compact CTIA (M1-M4 and C_{int}), with the new reset scheme (M5-M7 and $C_{reset/CDS}$), a comparator (M8-M15), and a latch to finally generate the reset signals b_{reset} and $\bar{b}_{reset}$.

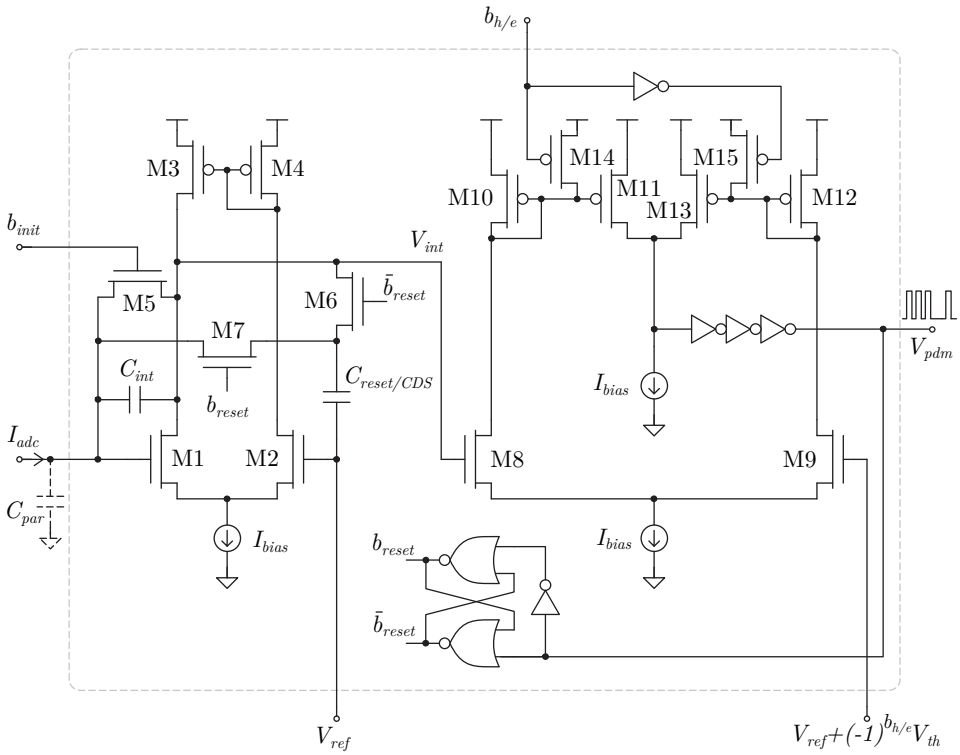


Figure 3.3 | CMOS circuit proposal for the lossless PDM stage of the in-pixel integrate-and-fire ADC.

From Eq. (3.4) and Eq. (3.8) it is clear that high gain factors are needed for the CTIA OpAmp in order to compensate for detector impedance and

minimize circuit noise impact on charge measurement. For this reason, big channel lengths and very low current biasing levels are chosen for M1-M4, avoiding the necessity of cascode topologies. As a side effect, offset and flicker noise are improved due to mismatching reduction and larges areas. In fact, thanks to the new reset scheme introduced in the CTIA, the limited slew-rate obtained from the low-power biasing strategy has little effect on the linearity of the PDM stage.

According to DPS requirements from Section 2.1, the proposed CMOS pixel may deal with positive (i.e. holes) or negative (i.e. electrons) charge collection, exclusively depending on an external and global digital signal ($b_{h/e}$). This programmability is implemented in Fig. 3.3 by switches M14 and M15, which select alternatively the sign of the comparison. Changing output path is preferred over switching inputs of the comparator as it would affect the preamplifier operation. Obviously, comparison level ($V_{ref} + (-1)^{b_{h/e}} V_{th}$) must be programmed accordingly, as explained in Section 3.3. Finally, comparator output is rectified and buffered.

In order to complete the preamplifier lossless reset, V_{pdm} is fedback generating complementary reset signals b_{reset} and $\bar{b}_{reset}$. A latch is used to avoid overlapping of these two reset signals that would cause a hard reset as in classic PDM schemes. In this sense, minimum size transistors (M6-M7) are chosen to implement reset switches for minimum charge injection. The inherent symmetry of the proposed reset scheme, both at switch and control signal levels, also helps in attenuating charge injection and clock feed through effects.

3.1.1 Full Scale

Pixel charge full scale is related to the following DPS design parameters: integration capacitor C_{int}, programmed threshold (gain) V_{th} and number of counter bits N_{count}. Charge full scale can then be written as:

$$Q_{fs} = Q_{LSB} \left(2^{N_{count}} - 1 \right) \tag{3.11}$$

where:

$$Q_{LSB} = C_{int} V_{th} \tag{3.12}$$

is the equivalent charge LSB. Since reasonable V_{th} levels can range from tens to hundreds of mV only, N_{count} is usually designed according to application full scale, while C_{int} comes from the resolution (noise) specification, as detailed in next section.

In practice, the additional full scale limitation of V_{pdm} frequency (f_{PDM}) must be considered for the circuit proposal of Fig. 3.3. According to Fig. 2.4:

$$f_{PDM} < \frac{1}{2T_{res}} \tag{3.13}$$

Hence, there is a minimum boundary for C_{int} not related with resolution but with:

$$\frac{|I_{adc}|_{max}}{C_{int} V_{th}} < \frac{1}{2T_{res}} \tag{3.14}$$

3.1.2 Equivalent Noise Charge

The resolution achievable by the PDM scheme of Fig. 3.3 is limited by both, detector noise itself and read-out circuit noise. The former is originated by the Poisson distribution of observed X-ray photons together with Gaussian fluctuations of the generated charge at the detector. Nevertheless, the study of this phenomenon is out of the scope of the present work.

Concerning read-out circuit noise, main contributions come from the CTIA section, as it is the input stage of the whole PDM circuit. In this sense, total noise power at the output of CTIA can be split into two uncorrelated phenomena:

$$V_{intn}^2 = V_{noa}^2 + V_{nsw}^2 \tag{3.15}$$

where V_{noa} and V_{nsw} stand for the noise voltage generated by the OpAmp (M1-M4) and the reset switches (M6-M7) of Fig. 3.3. Considering thermal noise only, OpAmp contributions can be directly derived from Eq. 3.8:

$$V_{noa}^2 = \frac{dV_{nin}^2/df}{T_{acq}} \left(1 + \frac{C_{det}}{C_{int}}\right)^2 \tag{3.16}$$

being dV_{nin}^2/df the equivalent input noise spectral density of the OpAmp block. In the case of reset switches, the general kT/C rule [84] is as in any switched-capacitor (SC) circuit. However, the asynchronous nature of the PDM operation described in Section 2.2 makes kT/C contributions dependent on signal amplitude. Taking the case of full-scale input, when the maximum signal-to-noise and distortion ratio (SNDR) is usually achieved:

$$V_{nsw}^2 = 2\frac{kT}{C_{int}} \frac{1}{2^{N_{count}} - 1} \tag{3.17}$$

where k and T are the well-known Boltzaman constant and the operation temperature, respectively. This expression already includes the first-order low-pass post-filtering supplied by the digital counter of Fig. 2.2, which is the responsible for the down-scaling factor. In other words, the CTIA stage can be described as a SC circuit operating at an oversampling ratio (OSR) of $2^{N_{count}} - 1$.

For charge sensitive amplifiers, electronic noise is evaluated in terms of equivalent noise charge (ENC):

$$ENC = \frac{V_{intn} C_{int}}{q} [e_{rms}] \tag{3.18}$$

Hence, the total contribution of the electronic noise coming from the pixel read-out circuit is found to be:

$$ENC = \frac{1}{q} \sqrt{\frac{dV_{nin}^2/df}{T_{acq}} \left(C_{int} + C_{det}\right)^2 + 2\frac{kTC_{int}}{2^{N_{count}} - 1}} \tag{3.19}$$

Two design conclusions can be argued from the above expression respect to dependence between ENC and C_{int}:

- If OpAmp noise is dominant, reducing C_{int} below C_{det} will not increase charge sensitivity.
- When reducing thermal noise contributions through C_{int}, the capacity of the digital counter (N_{count}) need to be rescaled accordingly in order to really improve the overall dynamic range.

As a rule of thumb, OpAmp and switches noise contributions should be balanced, and the final C_{int} value should be selected so:

$$Q_{LSB} \doteq 2ENC \tag{3.20}$$

Otherwise, either excess number of spikes will be generated at V_{pdm} (for $Q_{LSB} << 2ENC$) or resolution will be limited by C_{int} itself (for $Q_{LSB} >> 2ENC$). As a result of combining the above condition with Eq. 3.18 and Eq. 3.19, the main design equation for the optimum C_{int} value is:

$$\frac{(C_{int}V_{th})^2}{4} = \frac{dV_{nin}^2/df}{T_{acq}}\left(C_{int}+C_{det}\right)^2 + 2\frac{kTC_{int}}{2^{N_{cout}}-1} \tag{3.21}$$

Obviously, other practical design considerations have to be taken into account, like the upper limit of f_{PDM} in Eq. 3.13 or the maximum silicon area available inside the pixel to integrate C_{int} and $C_{reset/CDS}$.

Apart from generating thermal noise, the CMOS circuits of the pixel analog frontend also contribute with flicker noise. In general, flicker power components in terms of equivalent voltage at the gate of each MOS transistor can be expressed as [85]:

$$V_{nfi}^2 = \frac{(K_F)}{WL}\frac{1}{f} \tag{3.22}$$

where K_F stands for the flicker parameter of the target CMOS technology.

It is clear from the above equation that flicker voltage contributions are fairly independent from transistor bias point. Unfortunately, it is difficult in this case to reduce flicker effects through device area (WL) scaling due to the compact pixel pitch requirements. On the contrary, the low frequency nature of flicker phenomena is exploited here for its attenuation by the CDS function of the new CTIA reset scheme, as already explained in Section 2.2.

3.1.3 Integrated versus Counted Charge

Linearity losses resulting from classical integrator reset schemes when operating at high count rates have been already addressed and corrected by the new proposal of Section 2.2. However, other reset issues have to be taken into account for the CMOS circuit proposal of Fig. 3.3 also. Actually, charge coming from X-ray detectors exhibits a pulsed nature instead of a constant current profile. As long as the comparison between integrated signal and threshold voltage in the comparator of Fig. 3.3 is not instantaneous, the extra charge that makes V_{int} to exceed the threshold level is not really quantized. This behavior does not mean that this extra charge is not integrated nor compensated by the new reset scheme, but that it is not entirely counted. It is important to note that the proposed PDM stage counts for charge referred to threshold voltage only, and not to total voltage generated by a given particle. This behavior is illustrated in Fig. 3.4(a) where the instantaneous arrival of charge clouds generated by X-ray particles are integrated, exceeding the threshold level with error voltages $V_{e,k}$. While the reset scheme of Fig. 3.3 still compensates for $Q_{integrated,k}$, only Q_{count} is really counted. The resulting loss, $Q_{integrated,k} - Q_{count}$ depends on the particular incoming charge packet and the V_{int} level at the arrival of the packet. Moreover, its value varies randomly, causing a non-linear effect that cannot be compensated in any way, due to the unpredictable charge packets that trigger the reset scheme.

In practice, the CTIA stage preceding the comparator is also speed limited, so V_{int} slew-rate in the circuit of Fig. 3.3 can not be infinite. Therefore, every time a charge packet produces a threshold cross, the extra charge that it is not counted ($V_{e'}$) remains more or less the same for every particle regardless of its total charge, as illustrated in Fig. 3.4(b). Due to the independence

of this error respect to signal and its low value compared to full scale, this effect is the same as that of a comparator offset and the system remains linear, although with a gain error, certainly. In fact, this gain error can be compensated by using the pixel built-in DAC to program the threshold voltage during calibration.

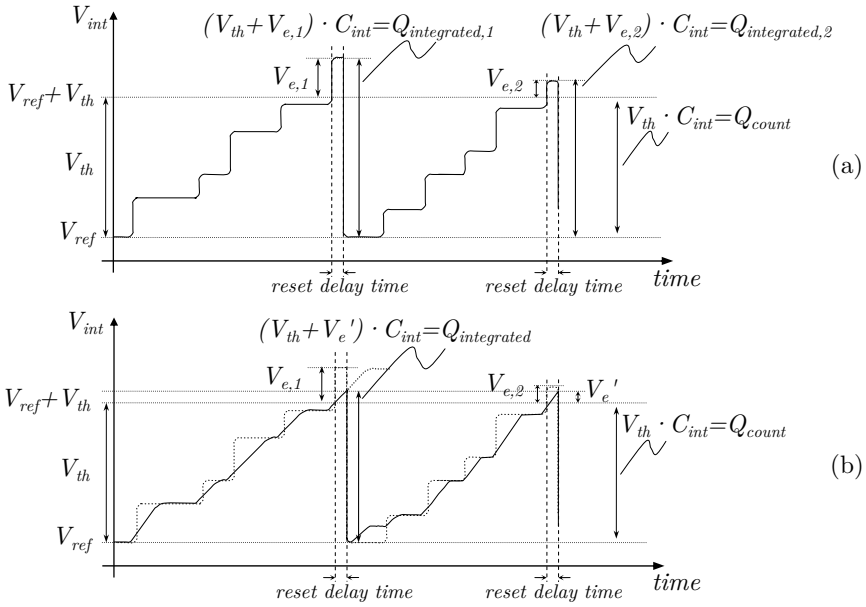


Figure 3.4 | Charge information losses due to comparator delay for ideal (a) and slew-rate limited (b) CTIA.

3.1.4 Phantom Event Issues

Electronic noise and coupling effects may cause multiple pulses at the output of the comparator of Fig. 3.3 when the integrated signal V_{int} approaches the threshold level $V_{ref}+(-1)^{b_{h/e}}V_{th}$ and just a single event should be generated. This unwanted behavior can be fixed by introducing some hysteresis in the quantization function as depicted in Fig. 3.5.

For this purpose, two circuit modifications of the comparator are considered in Fig. 3.6. The first approach uses current feedback to imple-

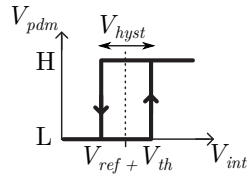


Figure 3.5 Mathematical model of the hysteresis cycle to be introduced in the quantization function against phantom events. Hole collection ($b_{h/e} = 0$) case.

ment an hysteresis cycle of width V_{hyst}, as shown in Fig. 3.6(a). When $V_{int} - (V_{ref} \pm V_{th}) \cong V_{hyst}$:

$$2I_{D1} = I_{bias} + I_{hyst} = I_{bias}\left(1 + \frac{1}{K}\right) \tag{3.23}$$

according to the geometrical scaling factor K. At the same operating point, from the differential pair M1 and M2 working in weak inversion saturation:

$$I_{D1} = \frac{I_{bias}}{1 + e^{\frac{V_{ref} \pm V_{th} - V_{int}}{nU_t}}} \tag{3.24}$$

Hence, the resulting hysteresis cycle width is found to be:

$$V_{hyst} = nU_t ln\frac{K+1}{K-1} \underset{K>>1}{\longrightarrow} \frac{2nU_t}{K} \tag{3.25}$$

Unfortunately, the obtained values for V_{hyst} are excessively high for practical K scaling factors, leading to reset pulses excessively wide and thus limiting signal full scale as in Eq. 3.14.

For this reason, a second approach is presented in Fig. 3.6(b). It is based on voltage threshold stacking by means of a cascaded Schmitt-Trigger stage (M8-M11). Here, the addition of M9 and M11 causes body effect to appear at M8 and M10 transistors, resulting in higher equivalent thresholds [84]:

$$V_{TB} = V_{TO} + \gamma\left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}\right) \tag{3.26}$$

Where V_{TO} is the threshold voltage without body effect, γ the body effect coefficient, $2\Phi_F$ the approximate potential drop between surface and bulk across the depletion layer when $V_{SB} = 0$, and V_{SB} the source to bulk voltage. This causes the transition step to occur at higher input voltages.

Furthermore, this stage also leads to higher settling times at its own output and thus, small variations at the input of this stage are weaken.

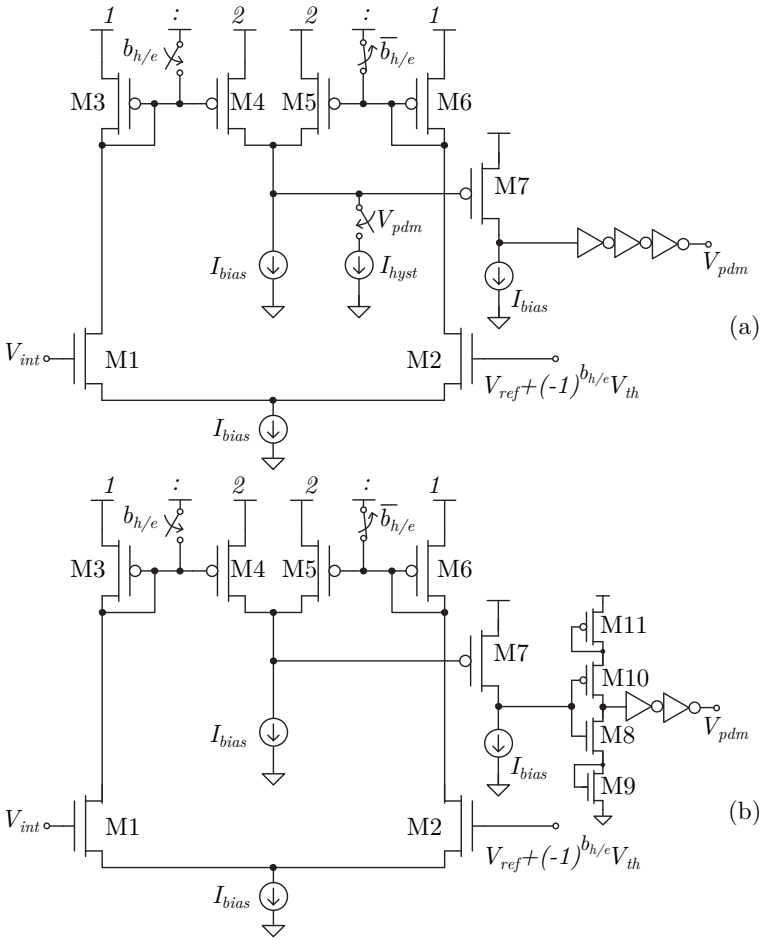


Figure 3.6 Circuit modifications to the Fig. 3.3 comparator to incorporate Fig. 3.5 hysteresis based on current feedback (a) and voltage threshold stacking (b).

3.2 Dark Current Cancellation

As explained in Section 1.2.3, direct X-ray detectors need to be reverse biased in order to create a depletion region through the whole detector depth. This high voltage biasing generates a reverse current even without signal presence, which is called dark current. In general, detector dark current can be treated as DC current, since it usually does not change over at least short time spans. However, its value depends on detector material, design, inhomogeneities and temperature. This last dependance imposes low-power operation for the full CMOS ROIC in order not to heat the array of X-ray detectors. In practice, dark current can be seen as offset FPN, which should be canceled to not decrease the full-scale of the CTIA integrator.

Hence, it is advantageous to include a block in each pixel circuit to compensate for its particular detector dark current (I_{dark}), as shown in Fig. 2.1. Since biphasic current sensing capability is wanted in the final DPS, this block must be able to compensate for both types of charge polarity. Fig. 3.7 shows the proposed CMOS circuit and its operation for dark current autocalibration and cancellation.

Basically, dual NMOS (M1-M2) and PMOS (M3-M4) dynamic current mirrors, also known as current copiers, are introduced to compensate for positive and negative I_{dark} values respectively, according to selection switches S_1-S_4. As it can be seen, these current copiers are driven by the CTIA itself of Fig. 3.3 through M5 (and M7) and M6 (and M8). In order to cancel out dark current components, a calibration time is needed prior to the regular integrating phase. During this calibration phase, dark current is tracked, filtered and its value stored as a voltage ($V_{dark1,2}$) in the capacitive memory node of the current copiers ($C_{dark1,2}$) following the operation sequence in Fig. 3.7 (b).

Analog memories V_{dark1} and V_{dark2} must therefore be able to hold the calibrated value for long integration times, so low-leakage is needed in $C_{dark1,2}$. For this reason, composite switching networks, M9-M12 and M13-M16, are introduced in nodes V_{dark1} and V_{dark2} of Fig. 3.7, respectively. Concerning leakage in sample and hold switches M9 and M13, drain current expression

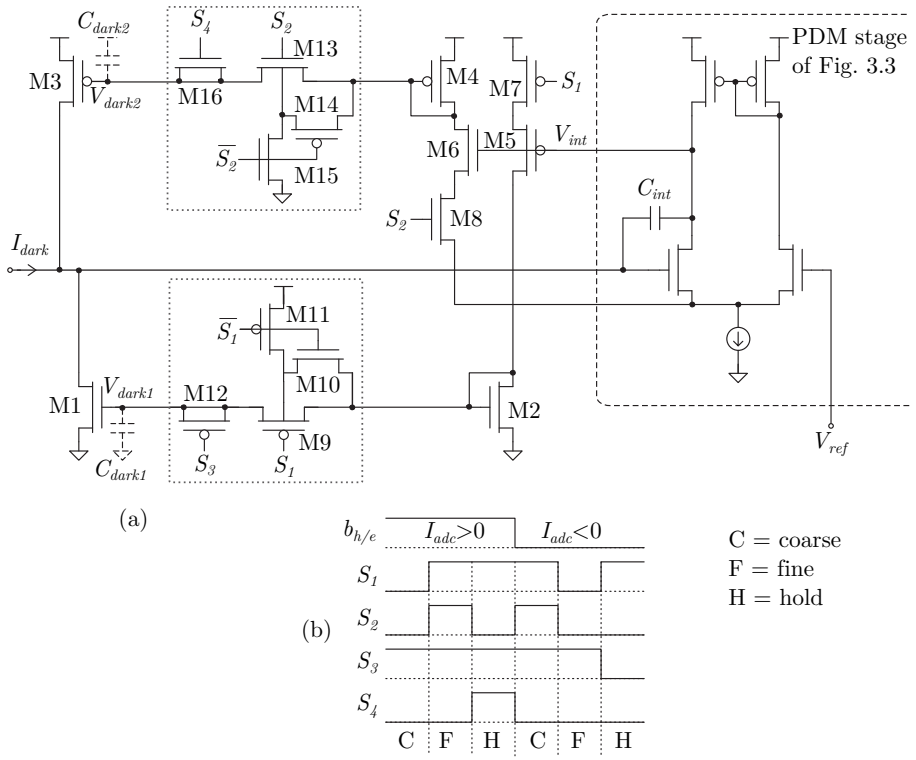


Figure 3.7 | Proposed CMOS implementation (a) and operation (b) of the in-pixel dark current cancellation circuit (chronogram not in scale).

in cut-off (i.e. deep weak inversion operation) according to [86] follows:

$$I_{leak} = I_S e^{-\frac{V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad I_S = 2n\beta \left(\frac{W}{L}\right) U_t^2 \tag{3.27}$$

where I_S, V_{TO}, n, U_t, β, W and L are the device specific current, threshold voltage, subthreshold slope, thermal potential, unitary current factor and channel width and length, respectively, while V_{SB} stands for the switch source-bulk voltage. In practice, leakage levels for regular metal oxide semiconductor field effect transistors (MOSFETs) in submicron technologies can easily reach pA-range, which is prohibited for long retention times. If thicker

gate oxide devices are available in the same CMOS process, the corresponding threshold voltage increase (ΔV_{TO}) can supply an attenuation factor of $e^{-\frac{\Delta V_{TO}}{nU_t}} \approx 10^{-3}$, reducing I_{leak} range to fA. However, this leakage level is still insufficient due to the small capacity of $C_{dark1,2}$. According to Eq. 3.27, further scaling down to I_{leak} into aA-range can be achieved selecting large V_{SB} potentials. This design solution is easily implemented by choosing complementary device types between switches and current copiers, as in Fig. 3.7(a) (e.g. M1 vs M9, M3 vs M13). However, the main disadvantage in this case is the high switch on resistance, which causes larger settling times. Hence, a dynamic bulk biasing is proposed in Fig. 3.7(a) for M9 and M13 through M10-M11 and M14-M15, respectively. In this way, high enough switching frequencies can be achieved together with low-leakage current levels.

Charge injection issues are also addressed by using a two-step coarse and fine calibration procedure in the circuit proposal of Fig. 3.7(a). Its principle of operation can be easily explained following the chronogram of Fig. 3.7(b). In the case of holes collection ($b_{h/e}$ high), M1 performs the coarse estimation of I_{dark} first, but its dummy counterpart M12, devoted to cancel charge injection errors, is not activated when holding. In fact, the always positive error in M1 current due to charge injection from M9 is then calibrated in the fine phase by M3. Finally, and unlike for the coarse period, the dummy pair M16 is activated when holding.

For electrons collection ($b_{h/e}$ low), the procedure is completely equivalent but interchanging the coarse and fine roles between M1 and M3, and the corresponding switches. As a result, even if final charge cancellation is not perfect, absolute residual is not depending directly on I_{dark} but on the error of I_{dark}, which is obviously smaller.

Since calibration is performed by integrating I_{dark} with the same CTIA circuit as for the ADC, the needed coarse and fine estimation times (T_{coarse} and T_{fine}) depend inversely on I_{dark} value itself. In the same way, calibrable dark current full-scale is also determined by the CTIA.

3.3 ADC Gain Tunning

Section 2.3 has reasoned the addition of a dedicated DAC circuit to adjust the gain of each pixel ADC through the programming of a digital code. Its scheme and operation at a high description level have been also discussed in the same section.

Based on this concept, Fig. 3.8 shows the circuit implementation at transistor level proposed for the in-pixel gain programming scheme of Fig. 2.8 employing dual transmission gates (DTGs). Low leakage transistors may be used for this circuit block to avoid undesired drifting of the programmed voltage value, V_{prog}. Besides, these transmission gates themselves can inject undesired charge into V_{prog} coming from transistor channel charge and clock feed through. With the purpose of absorbing this charge, dummy $DTG2c+$ and $DTG2c-$, with their input and output nodes shorted, are added in the DAC circuit of Fig. 3.8.

Apart from the own circuit non-idealities of the DAC itself, other factors can affect the effective threshold V_{th} during its transfer into the storing capacitor C_{th}. In this sense, input X-ray current and/or dark current from detector, as well as any offset or systematic errors may disturb the final V_{th} value.

In order to compensate for these effects, a calibration procedure is proposed in Fig. 3.9 and Fig. 3.10, where V_{err} stands for the overall threshold voltage error.

It starts with an initialization phase, when integration and reset capacitors are reset and, therefore, storage capacitor voltage is set at V_{ref}. Then, errors caused by detector current and parasitic charge injections from switches are sampled during T_{str} by reusing the $C_{reset/CDS}$ capacitor of Fig. 3.3. After that, this error is hold while the threshold value is programmed in the DAC capacitors following the principle of operation described in Section 2.3. Finally, the programmed threshold and the inverted previously sampled error are transferred during a T_{str} time interval into storing capacitor C_{th} thus compensating the programming error. In order to further reduce residual errors due to detector current, T_{str} must be chosen the minimum time needed to transfer the programmed threshold charge.

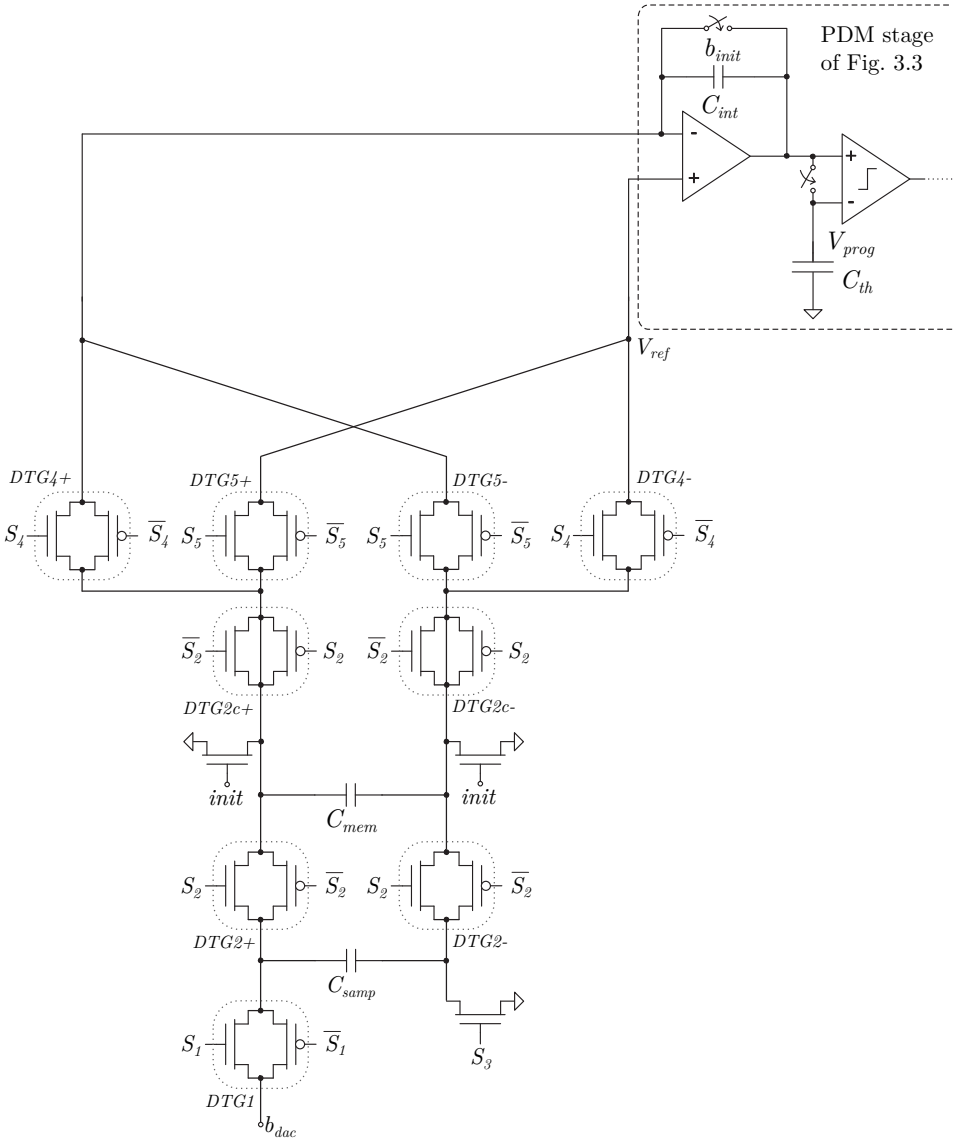


Figure 3.8 | Proposed CMOS implementation for the in-pixel gain tuning based on a switched capacitor DAC.

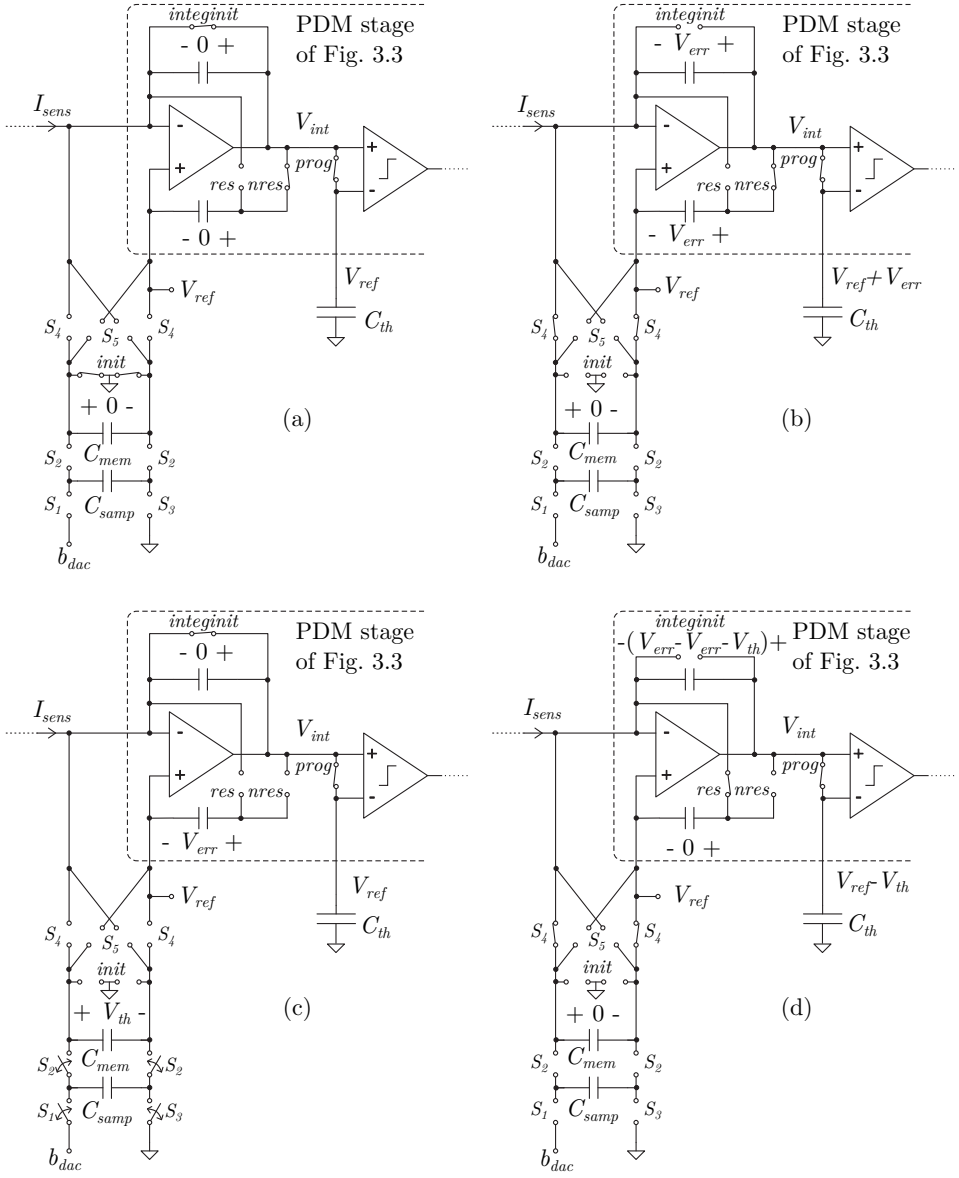


Figure 3.9 Procedure of DAC precalibration for $V_{th} < 0$ case: initialization (a); error sampling (b); threshold value programming and error holding (c); threshold value storing and error compensation (d).

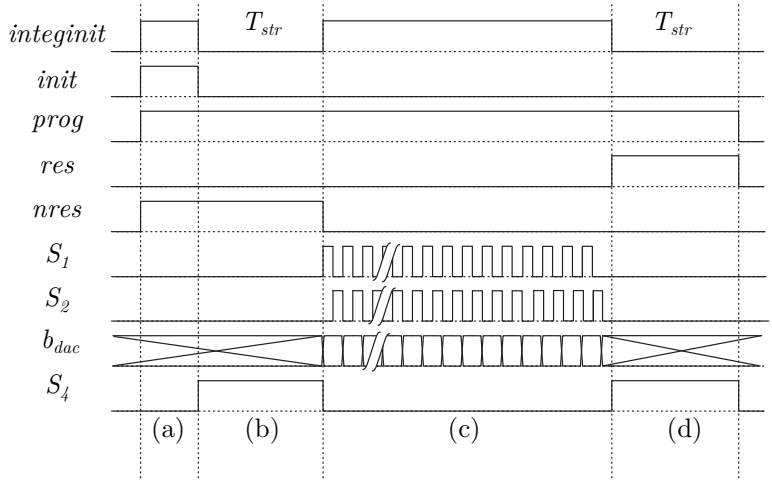


Figure 3.10 Operation of the DAC precalibration procedure proposed in Fig. 3.9 for $V_{th} < 0$ case (for simplicity, $S_3 = S_1$): initialization (a); error sampling (b); threshold value programming and error holding (c); error free threshold voltage storing (d).

Even assuming the programmed threshold value is error free thanks to the proposed calibration-compensation procedure, another important issue must be taken into account during its storage. In particular, the leakage off current of the sample and hold (S/H) switch controlled by *prog* signal in Fig. 3.9 must be limited by design to avoid ADC gain drifting during acquisition. In Section 3.2, a low-leakage switch has been described. However, since leakage magnitude is proportional to voltage difference between switch nodes, the alternative design of Fig. 3.11 is proposed for our purposes. It is based on a double switch (M7 and M8) and a differential pair with active current mirror configured as a follower (M1-M4). The latter has the purpose of matching the voltage of the two sides of the S/H switch (M7) connected to the threshold storing capacitor C_{th}. Here, M5 and M6 are devoted to reduce the effects of adding this circuit to the threshold programming of Fig. 3.9. It is clear that power consumption of this circuit is higher than using the low-leakage switch proposed for the dark current cancellation circuit of Fig. 3.7, but it performs better leakage figures of merit. Furthermore, its area occupancy is not necessarily larger, since the switch proposed in Sec-

tion 3.2 includes transistors bulk-biased at different potentials, which means including separated wells that, according to most technologies design rules, require a considerable widening of the area occupied.

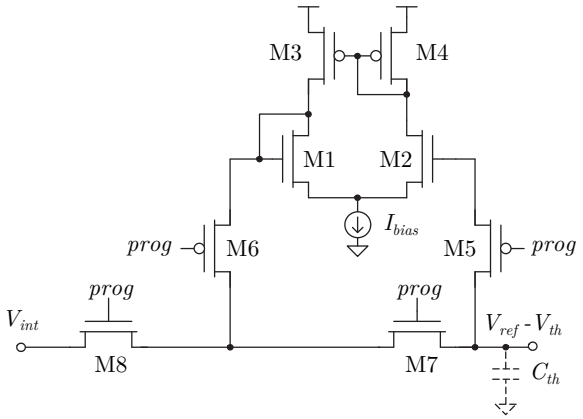


Figure 3.11 | Proposed low-leakage S/H switch to avoid ADC V_{th} drift in Fig. 3.9.

3.4 Built-In Test Mechanism

The addition of a dedicated circuit for self-testing the CMOS ROIC even before its hybridization to direct X-ray detectors has been already justified in Section 2.4. As described, minor modifications to the circuit of Fig. 3.8 are required in practice to obtain this testing functionality.

Fig. 3.12 emphasize the referred circuit additions at transistor level. Its operation during acquisition phase is based on biasing C_{mem} at the global test amplitude level $V_{testamp}$ with S_6 and injecting this charge to CTIA input with the polarity determined by S_4 (holes injection) or S_5 (electron injection). Obviously, during this operation $S_1 = S_2 = S_3 = 0$ and undesired charge injections from the switches are not compensated. Nevertheless, high accuracy is not usually required for functional testing only. In case of needing it, parasitic injections can be always compensated with the programming $V_{testamp}$ itself.

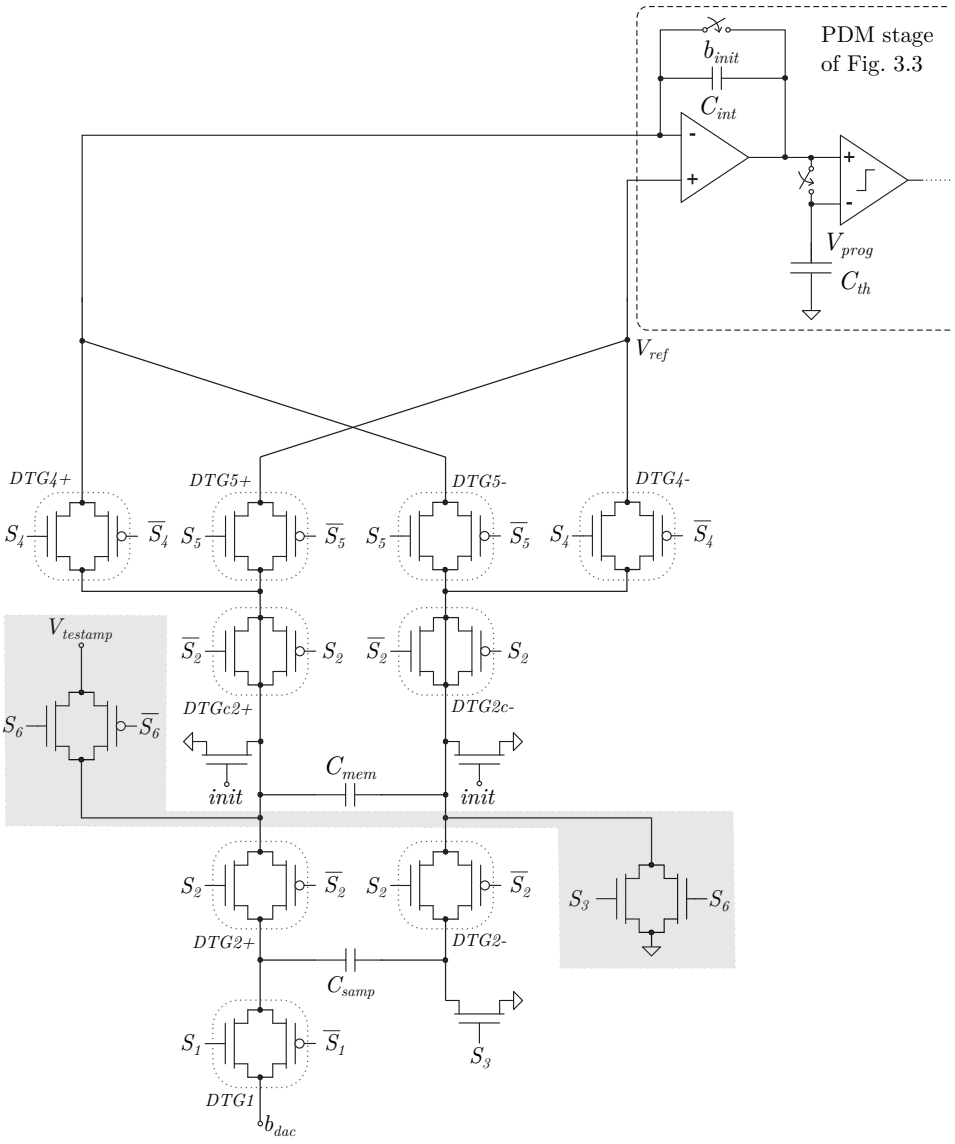


Figure 3.12 | Minor adjustments (highlighted) to the circuit of Fig. 3.8 in order to include the built-in test capability of Fig. 2.9.

3.5 Local Reference and Biasing Generation

The benefits of locally generating both biasing currents and voltages references needed by the proposed circuits inside the own pixel has been already argued in Section 2.1. Basically, the reduction of inter-pixel crosstalk together with the lower connectivity requirements for the target CMOS technology, undoubtedly compensate the area overhead of these local generators. Anyway, a low-power and compact reference circuit is recommended. Moreover, an all-MOS circuit is preferred over particular alternatives based on bipolar junction transistor (BJT) devices to avoid technology specific requirements.

Several low-power bandgap-like reference circuits have been already reported in literature to be compatible with CMOS technologies, [87–93]. However, some of them are not suitable for targeting modern CMOS processes due to the use of parasitic bipolar junction transistors [87] or diodes [88]. In the case of MOSFET-based solutions, some proposals still require linear resistors [89], multi-threshold process [90–92] or complex circuits [93].

The proposal of Fig. 3.13 is based on a single-threshold all-MOS devices circuit to generate voltage reference thermally compensated and biasing currents based on MOS specific current (I_S).

Basically, the generator is composed of three cascaded sections: the proportional to absolute temperature (PTAT) voltage core (M1-M4), the specific current generator (M5-M7) and the thermally compensated output voltage reference (M8-M9).

The principle of operation of the proposed circuit can be also split in the three stages of Fig. 3.13. Firstly, M1-M2 matched pair is operated in weak inversion (i.e. subthreshold) saturation. In what follows, channel length modulation effects are neglected and the bulk terminal of each MOS device is connected to the corresponding supply voltage. According to the EKV model [86], the drain current expression for this region of operation is:

$$I_D = I_S e^{\frac{V_{GB}-V_{TO}}{nU_t}} e^{-\frac{V_{SB}}{U_t}} \qquad I_S = 2n\beta U_t^2 \tag{3.28}$$

where I_S is the specific current, V_{TO} is the threshold voltage, n stands for

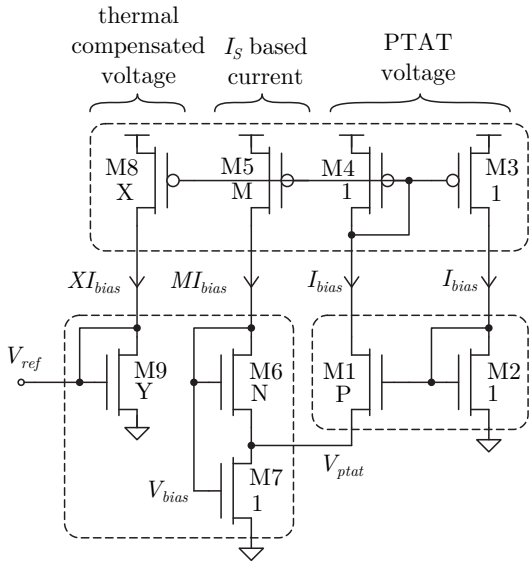


Figure 3.13 Low-voltage all-MOS pixel circuit proposed for the generation of thermally compensated voltage references (V_{ref}) and I_S-based biasing currents (I_{bias}). Dashed boxes indicate device matching.

the subthreshold slope factor, U_t is the common thermal voltage while β is the current factor. The symmetry of the current mirror M3-M4 forces:

$$I_{D1} \equiv I_{D2} \tag{3.29}$$

$$I_{S1} e^{-\frac{V_{ptat}}{U_t}} = I_{S2} \tag{3.30}$$

Hence, the P scaling ratio causes the source voltage of M1 to follow the PTAT law:

$$V_{ptat} = U_t \ln P \tag{3.31}$$

Secondly, I_{bias} is obtained from the equivalent non-linear load attached to

V_{ptat}. For such a purpose, M6 is biased in strong inversion saturation. According to [86]:

$$I_D = \frac{\beta}{2n}(V_{GB} - V_{TO} - nV_{SB})^2 \tag{3.32}$$

while M7 is also operated in strong inversion but conduction following [86]:

$$I_D = \beta\left[V_{GB} - V_{TO} - \frac{n}{2}(V_{DB} + V_{SB})\right](V_{DB} - V_{SB}) \tag{3.33}$$

Taking into account the M scaling factor of the current mirror output M5 and the N ratio between M6 and M7:

$$\begin{cases} MI_{bias} = \dfrac{N\beta_7}{2n}(V_{bias} - V_{TO} - nV_{ptat})^2 \\ (M+1)I_{bias} = \beta_7\left(V_{bias} - V_{TO} - \dfrac{n}{2}V_{ptat}\right)V_{ptat} \end{cases} \tag{3.34}$$

the resulting biasing current is proportional to the specific current [94]:

$$I_{bias} \doteq QI_{S7} \tag{3.35}$$

$$Q = \left[\frac{\ln P}{2(M+1)}\left(\sqrt{\frac{M}{N}} + \sqrt{\frac{M}{N} + M + 1}\right)\right]^2 \tag{3.36}$$

Thirdly and last, I_{bias} is X scaled through the mirror output M8 and driven to the active load M9 operating in strong inversion saturation as described by Eq. (3.32). The final voltage reference is found to be:

$$V_{ref} = 2n\sqrt{\frac{QX}{Y}}U_t + V_{TO} \tag{3.37}$$

It is well known that the MOSFET threshold voltage exhibits a negative thermal coefficient (NTC) following the general model [95]:

$$V_{TO}(T) = V_{TO}(T_O) - \alpha \left(\frac{T}{T_O} - 1 \right) \tag{3.38}$$

where α, T_O and T are the thermal coefficient for the particular CMOS technology, the reference and the working temperatures, respectively. Hence, combining the NTC behavior of V_{TO} in Eq. (3.38) with the PTAT law supplied by U_t in Eq. (3.37), thermal drifts in V_{ref} can be canceled. In particular, the design constraint for such an ideal thermal compensation is:

$$\sqrt{\frac{QX}{Y}} = \frac{1}{2n} \frac{\alpha}{U_t(T_O)} \tag{3.39}$$

resulting in the temperature independent reference:

$$V_{ref} \equiv \alpha + V_{TO}(T_O) \tag{3.40}$$

A couple of practical considerations must be taken into account during the design stage: $P \gg 1$ for minimizing technology mismatching effects between M1-M2; and both $\frac{QM}{N}$ and $\frac{QX}{Y} \gg 1$ to ensure strong inversion for M6, M7 and M9. As a side effect, I_{bias} can be reused for the current biasing of general analog circuits, as its I_S-dependence from Eq. (3.35) makes inversion coefficient of the device operation point (e.g. moderate inversion) to be robust against CMOS process variations.

In practice, the CMOS implementation of this circuit is shown in Fig. 3.14, where a cascode topology is obtained adding M1', M2', M6' and M9' to improve stability and current ratio accuracy. The biasing currents for the circuit blocks described in previous sections are obtained copying I_{bias} with M10, M11 and M12$_k$. Finally, a start-up circuit is preventively added to ensure bias in the desired state (M13-M20).

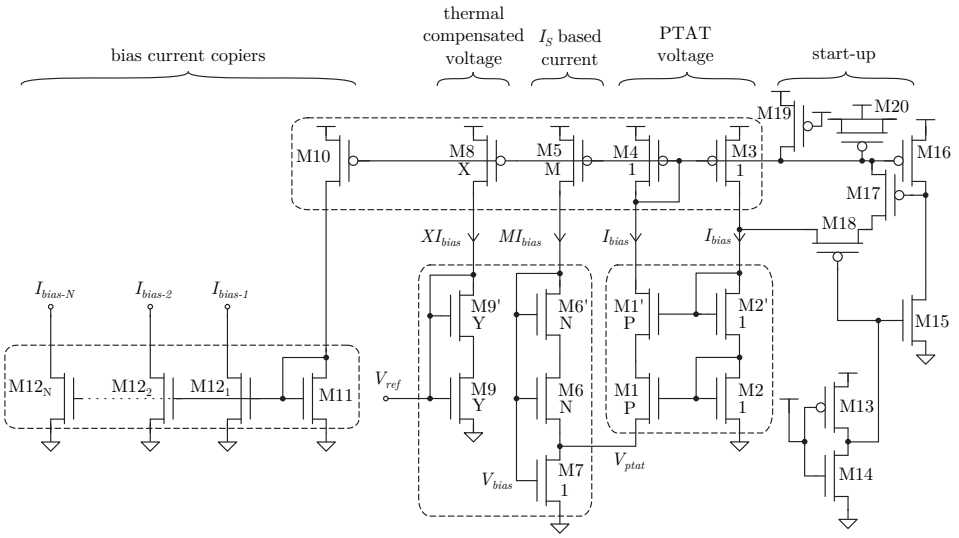


Figure 3.14 | CMOS implementation of the in-pixel reference voltage and biasing currents generator circuit based on the proposal of Fig. 3.13.

3.6 Digital I/O Block

Since all analog references and biasing levels needed by the presented pixel circuits are generated locally and detector signal is A/D converted already at pixel level, the input-output communication of the whole DPS can be kept entirely in the digital domain. This digital signaling of the proposed pixel can be classified into control and I/O communications.

Section 2.5 has presented a high level description of the in-pixel digital block used either as acquisition ripple-counter or as serial I/O shift-register. Fig. 3.15 shows the CMOS implementation of each module of the reconfigurable I/O block of Fig. 2.11(a), where none DTG is required to be low-leakage here, and *init* signal is introduced in order to reset register contents. As a rule of thumb to reduce both power consumption and area, minimum size transistors are recommended.

The principle of operation can be described as follows: during I/O communications phase (*count* low and *event* forced to low level), T and XT

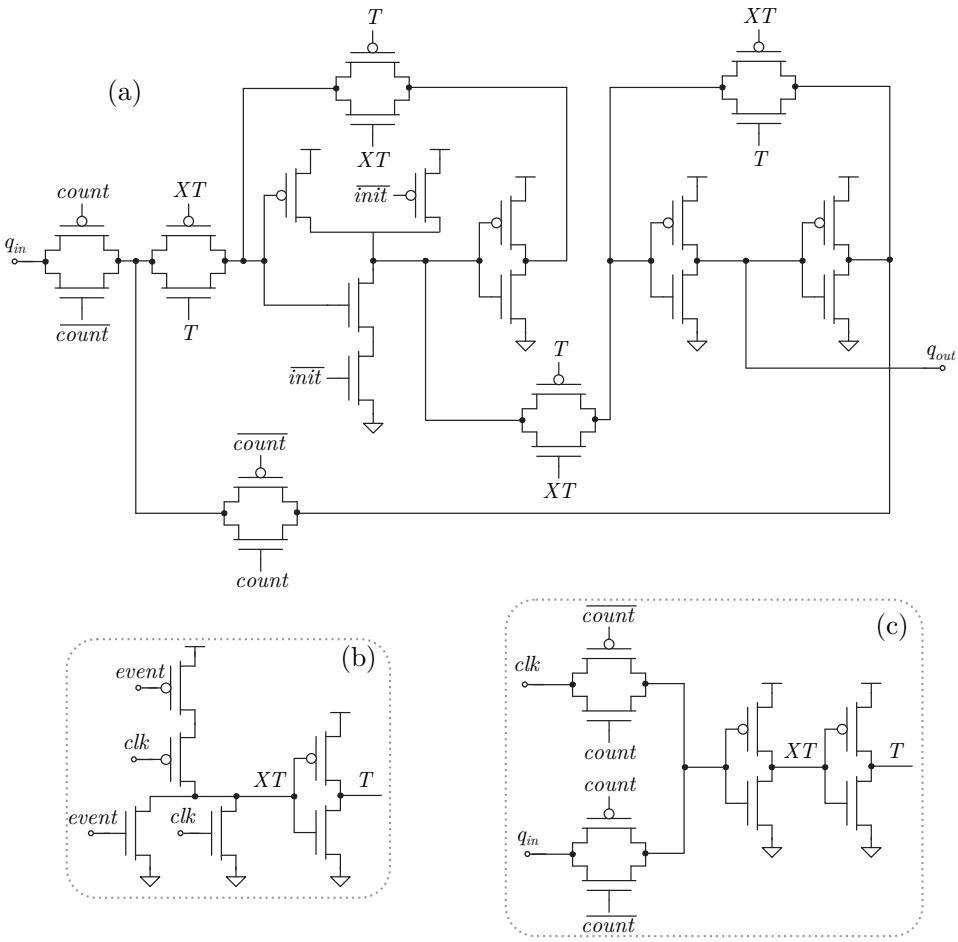


Figure 3.15 | Proposed CMOS implementation of each register bit module (a) and signals T and XT obtaining circuits for the LSB (b) and the MSB (c) modules.

signals are defined by *clk* and the daisy-chained register are configured as shift-register for serial sample read-out and individual gain program-in. Alternatively, in acquisition (*count* high), X and XT signals of the LSB module are driven by *event* signal coming from the output of the comparator of Fig. 3.3 (V_{pdm}) while for the rest of the bit modules, X and XT are given by the output of each previous module, behaving as a ripple counter.

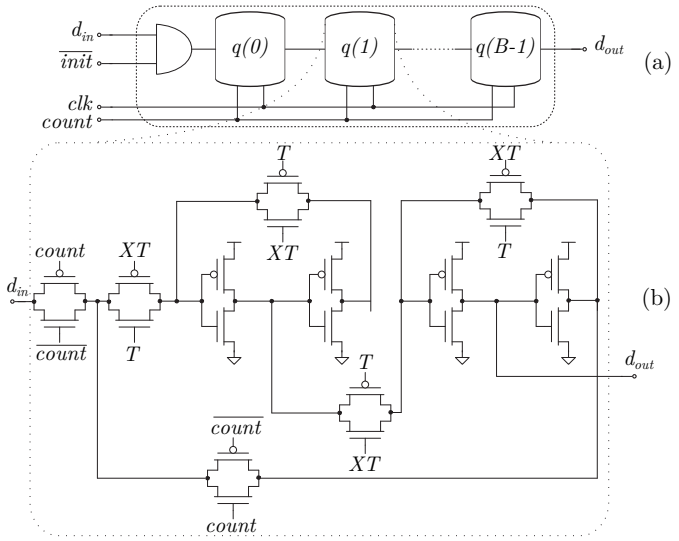


Figure 3.16 Simplified scheme for the reconfigurable I/O block of Fig. 2.11 modified with the alternative reset scheme (a) and CMOS implementation of each reconfigurable bit module (b).

In order to reduce pixel area occupancy, the reset circuit can be implemented using the alternative circuit of Fig. 3.16(a). In this case, each bit module in Fig. 3.16(b) requires 2 transistors less than the design of Fig. 3.15(a). Since only 6 extra transistors of the AND gate are needed per pixel for this new reset system, if the size of the reconfigurable register is 3-bit or higher, overall area reduction is achieved. The drawback of this alternative is that B clock cycles are needed to reset the whole I/O block as the reset is performed by serially introducing logic $'0'$s into the shift-register.

DPS Designs in 0.18μm CMOS Technology | 4

This chapter collects the architecture and circuit proposals of Chapter 2 and 3 to present practical design implementation in submicron CMOS technology. Four different DPS cells and their corresponding test chips for both electrical and radiation validation are presented.

4.1 DPS Specifications

Having in mind the pixel requirements exposed in Section 2.1, specifications have to be determined to focus on the concrete design of the readout CMOS pixel. In this sense, Table 4.1 summarizes initial specifications for the DPS.

Even though the circuits of Chapter 3 have been projected and studied with independence of the integrating technology, the target CMOS process must be chosen carefully in order to accomplish these specifications.

Submicron technologies may help achieving compact designs. Digital blocks of the pixel, which usually can be built using minimum size transistors, are expected to occupy about 50% of the total pixel area. This fact, together with a low supply voltage also benefits obtaining low power circuits. A high number of available metal layers (5 or more) and the possibility of using metal in metal (MiM) type capacitors are also highly recommended to obtain compact pixel pitch.

In order to reduce crosstalk between pixels, placing each CMOS DPS in separated wells is advantageous. Therefore, a triple well technology is preferred.

Additionally, the availability of different transistor types, such as low leakage or low voltage threshold options, can be positive for some specific circuit blocks, as discussed in Section 3.3.

Parameter	**Value**	**Comments**
Pixel pitch	55μm×55μm	pitch up to 100μm is acceptable
Charge resolution (Q_{res})	50kq to 250kq	e^-/h^+ selectable; programmable
Charge full-scale (Q_{fs})	100Mq	e^-/h^+ selectable
Readout dynamic range	> 10-bits	overflow detection
I/O speed	50Mbps	
Integrating time	1ms to 1000ms	
Crosstalk	< 0.5LSB	
Power consumption	< 20μW	avoid detector heating
Compensated dark current	up to 10nA	e^-/h^+ selectable
V_{ref} thermal coefficient	< 100ppm/°C	
Bias mismatching	< 10%	
Reset pulses duration	$< 500ns$	
Pulses frequency	up to 1×10^6events/s	
Equivalent Noise Charge	$< 2ke^-$	

Table 4.1 | Initial specifications for the DPS design example.

The 0.18μm technology from UMC, available through the europractice (EP) integrated circuit (IC) service [96], satisfies the above referred requirements. Table 4.2 summarizes some of its main characteristics.

4.2 Pitch Downscaling

With the aim of verifying the behavior of the proposed circuits, three pixel generations have been fully designed, both at schematic an physical layout levels, using circuits described in Chapters 2 and 3. These designs present 100, 70 and 55 μm pitch, respectively.

For each design generation, some general guidelines are obeyed as shown in Fig. 4.1.

Process	Name	UMCL180
	Critial dimension	0.18μm
	Wafer diameter	8 inch
	Reticle size	20mm×20mm
	Triple well	YES
	Number of metals	6
	Supply voltage	1.8V / 3.3V
Devices	MOSFET regular VT	+0.50V / -0.51V
	MOSFET low VT	(LV) +0.22V / -0.22V
	Thermal coefficient (α)	225mV
	Specific current (W/L)	390nA
	Capacitor type	MiM
	Capacitor density	1fF/μm^2
	Resistor type	HIPO
	Resistor density	1kOhm/sqr
	BJTs	PNP
	RF	Varactor
	Other options	Zero VT
CAD	MOSFET model	BSIM3v3
	Technology parameters	process + mismatching
	Cadence/Synopsys suport	YES/YES
MPW	Access	EP regular / EP mini
	Periodicity	5/3 run/year
	Turnaround time	3 months
	Minimum area	5mm×5mm / 1.5mm×1.5mm
	Costs	0.6k to 1k EUR/mm^2
	Samples	>45 / >20

Table 4.2 | UMC 0.18μm CMOS technology characteristics.

As appreciated, each pixel is placed inside its own well and surrounded by substrate contacts in order to assure low crosstalk. With the purpose of forming large arrays by simple assembling of individual pixels, I/O signals cross the whole pixel. It is important to note that power supply and ground signals are routed both from top to bottom and from left to right thus forming a mesh and therefore reducing losses and crosstalk through supply rails.

For each pixel generation, two ASICs are designed and integrated for both electrical and radiation response validation. Following sections detail information regarding each pixel generation design and their test ICs developed.

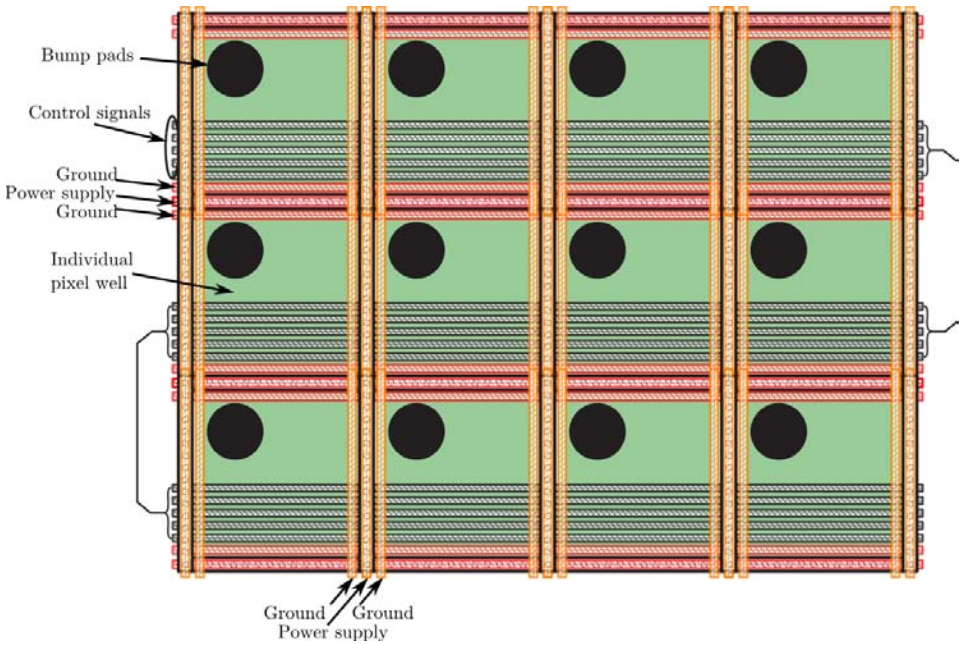


Figure 4.1 General floorplan of pixel physical interconnectivity and daisy chain arrangement followed in all pixel generations.

4.2.1 100μm-pitch DPS

A first pixel generation has been designed with 100μm-pitch (DPS100). This design, although having a size suitable for X-ray imaging applications, is materialized with the solely purpose of demonstrating both the validity of the proposed architecture and CMOS circuits and the possibility of integrating all this pixel functionality in less than 100μm$\times$100μm. Subsequent pixel generations are DPS100 evolutions according to the feedback obtained from its experimental tests results.

Fig. 4.2 shows the physical layout of DPS100 pixel and its main circuit blocks. Apart from the circuits presented in Chapter 3, a digital control extra circuit is added in order to minimize the I/O signals that generate all the control signals for those circuits. Low leakage switches for the dark current cancellation circuit and for the threshold storing capacitor are im-

plemented as explained in Section 3.2, and no hysteresis is added to the comparator in this case.

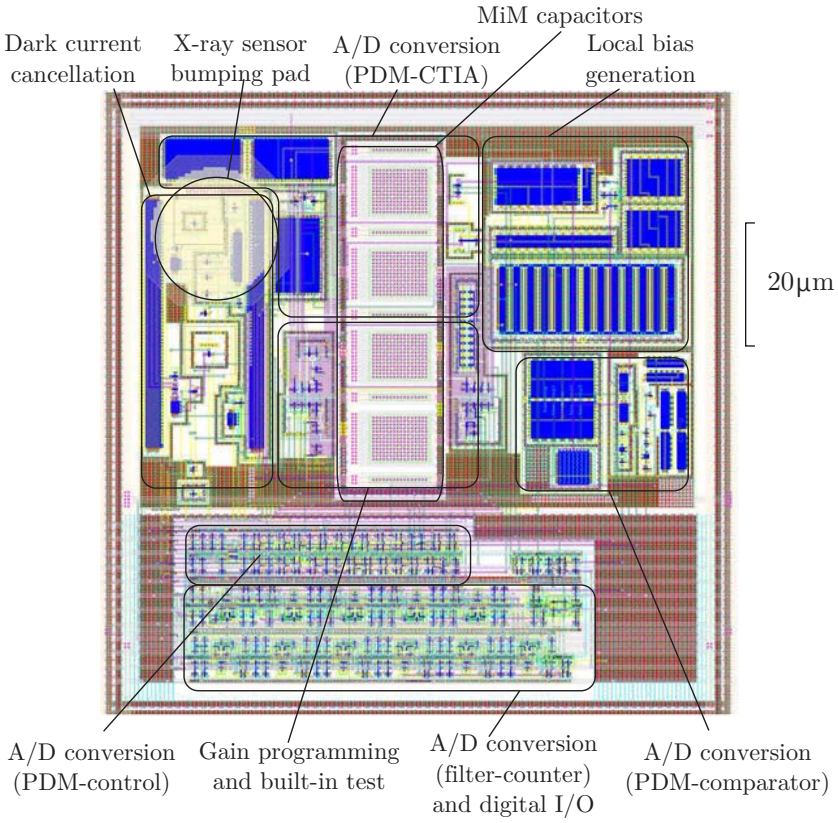


Figure 4.2 DPS100 pixel layout and main circuit blocks. Bounding box is 100μm×100μm while bumping pad diameter is 20μm.

Integrated capacitors are designed to present an extracted value of $C_{int} = C_{reset/CDS} = C_{mem} = C_{samp} \approx 130fF$. A 11-bit reconfigurable ripple counter and shift register circuit, as the proposal of Fig. 2.11, is employed as the counter/digital I/O block. Regarding the local bias generation circuit of Fig. 3.14, this design uses large transistors, and the scaling factors are $P = 10$, $M = 1$, $N = 1/2$, $X = 2$ and $Y = 1/4$. A flip-flop is also added as an enable flag for turning on the bias circuit.

The large area available in 100μm×100μm ease the compactness constraints. Guard rings are often used surrounding different circuit blocks, dummy structures are placed where convenient, and MiM capacitors do not overlap the rest of the circuitry.

Its operation begins with an initialization cycle, starting with a stand-by phase (SBY) where the biasing circuit of each pixel is disabled by resetting its power flag. In consequence, each DPS cell is inoperative except for its digital I/O functions. SBY phase is followed by a power-up stage (PWP) where pixels can be turned on individually, using the enable flag of the bias circuit in case they are daisy-chain arranged. Then, a no-operation cycle (NOP), where no processing activity is requested but the pixel is biased and ready to operate, can be optionally added. This dummy stage can be useful for example when a waiting period is needed in order to cool the detector.

After these initial cycles, digital I/O mode (DIO stage) is started and both serial input programming-in and output read-out are performed at the same time to optimize transfer speed, as was introduced in Fig. 2.1(b). On one hand, the digital sequence for programming the gain of each individual DPS cell is introduced serially too. On the other hand, the sequence containing the digital sample for each DPS cell is read serially. Over the first part of this stage, input bits move through the pixels chain until each programming code reaches the input of the corresponding pixel. Then, bits are directed to the DAC to program C_{mem} of Fig. 3.8 to finally transfer the programmed value to C_{th}, as explained in Section 3.3.

Finally, acquisition phase (ACQ), which is the main operation mode of the active pixel, starts. If dark current cancellation circuit is enabled, it is calibrated and compensated while the input sensor signal is A/D converted asynchronously, without any analog external reference or dynamic digital control, except when test is activated as detailed in Section 2.4. This state together with the digital I/O stage define the basic frame cycle.

Hence, regular operation of DPS100 is SBY+PWP+NOP+ (DIO+ACQ)+ (...), although can be changed to SBY+PWP+ (NOP+DIO+ACQ)+ (...) if some delay is needed at system level between frames, or even to SBY+ (PWP+NOP+DIO +ACQ+DIO)+ (...) in case of on-the-fly image reconfiguration.

4.2.2 70μm-pitch DPS

Based on the DPS100 pixel design and its experimental results obtained from its deep characterization explained in Chapter 5, a second DPS generation is developed with 70μm-pitch (DPS70). Its physical layout is presented in Fig. 4.3 again detailing its circuit blocks.

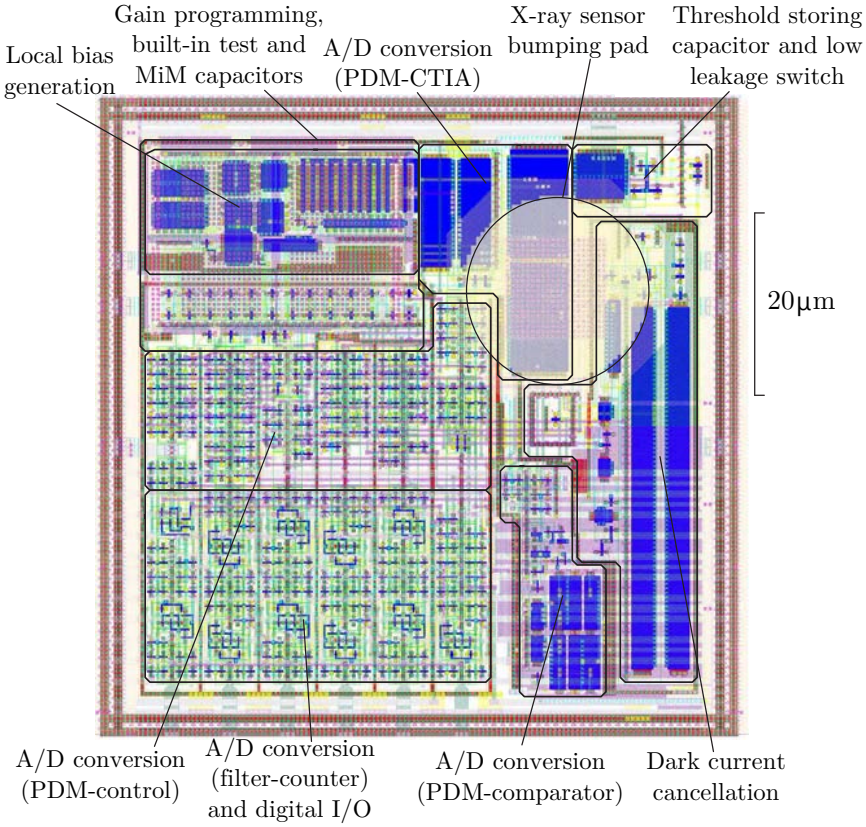


Figure 4.3 DPS70 pixel layout and main circuit blocks. Bounding box is 70μm×70μm while bumping pad diameter is 20μm.

Compared to DPS100, ADC comparator is modified as in Fig. 3.6(b) for hysteresis addition to prevent phantom events. Also, digital control circuit is minimized and test signals are converted to non-overlapped to avoid un-

desired test injections. On the other hand, the integrated capacitors values are maintained, but the 11-bit shift register is changed to cyclic in order to split the digital I/O and the threshold programming stages. While the scaling factors of the local bias generation circuit design are maintained, transistors are sized down.

As seen when comparing Fig. 4.3 to Fig. 4.2, the new layout is completely redesigned for a 50% pixel area reduction, and to incorporate all the changes described above. Although the analog and digital circuits are again physically separated, the drastic pixel area reduction impede the use of guard rings for internal circuit blocks and forces the use of minimum size transistors for digital circuits. Another key modification is the reuse of silicon area below MiM capacitors for circuitry integration as well.

Although many features of the operation of the DPS100 pixel are adopted, some modifications should be noted. A dark current calibration circuit initialization phase is added prior to the calibration itself. Finally, thanks to the fact that the shift register is also cyclic, the DIO stage is separated from the DAC programming phase (PROG) itself, so an extra no-operation phase (NOP) can be added just before this programming and the DAC precalibration of Fig. 3.9 can be preformed, minimizing errors in the threshold final value.

4.2.3 55μm-pitch DPS

A third generation of CMOS pixel has been designed with the purpose of reducing the pitch to 55μm (DPS55), which is in the state-of-the-art pixel size [58]. Equally important, this new design implement convenient improvements derived from the results of the exhaustive characterization of previous DPS70 design, as reported in Chapter 5.

Fig. 4.4 shows the DPS55 physical layout and its main circuit blocks. Again, a digital circuit is added in order to simplify external I/O connectivity. Also, the biasing circuit scaling factors and the MiM capacitor values are maintained. Equally, a cyclic register is selected. In contrast, a modification in this pixel design is the use of the low-leakage switch of Fig. 3.11 for the threshold storing capacitor.

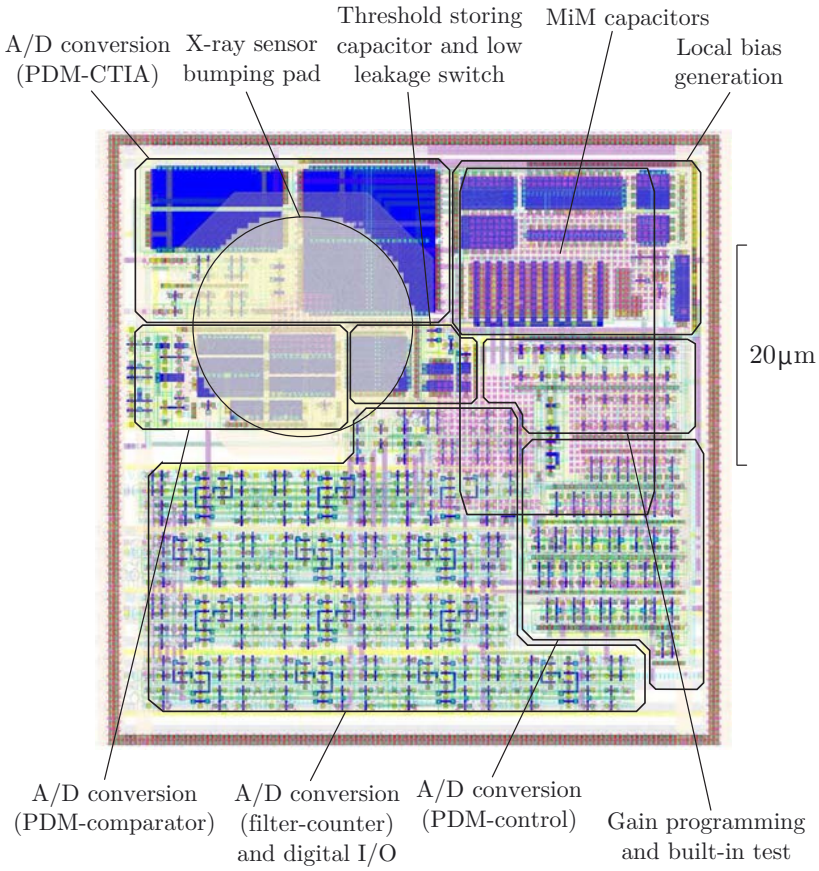


Figure 4.4 | DPS55 pixel layout and main circuit blocks. Bounding box is 55μm×55μm. Bumping pad diameter is 20μm.

It is already clear form the compact layout of Fig. 4.3 that all DPS70 circuit blocks can not fit in a 55μm×55μm area. The possibility of combining 4 pixels in a cluster sharing some of the circuits such as the digital control or the biasing blocks were studied but discarded to avoid any increase of the inter-pixel crosstalk. As an alternative solution, the main alteration in the architecture compared to DPS70 is the removal of the dark current cancellation circuit since the dark current can be in practice processed as a DC signal offset as will be verified in Chapter 5. Moreover, for the smaller area of this design, lower dark currents are expected. Consequently, the

dynamic range of the digital counter can be increased in order to absorb the resulting increase of signal full scale. In this case 2 bits are added, although this value is not a requirement from actual dark current levels. This fact also helps reducing the number of I/O signals together with simplifying the digital control circuit.

Furthermore, in favor of reducing pixel area, aggressive layout techniques have been employed like in DPS70 design. In particular, there is not enough area to use guard rings surrounding individual circuit blocks and some circuitry is again located under MiM capacitors.

The operation of the DPS55 pixel is almost the same as with its DPS70 counterpart except for the fact that the dark current cancellation circuit initialization and dark current tuning stages at the beginning of the acquisition phase are obviously eliminated.

4.3 2D Modular X-Ray Imagers

A last pixel design is developed presenting 52μm-pitch (DPS52). Section 1.4 already revealed that the long term objective of this CMOS DPS proposal is its use on truly 2D modular X-ray imagers. Despite the referred objective is out of the scope of this work, what follows is a brief introduction to the proposed 2D modular X-ray imager concept in order to justify the DPS52 development.

The proposed modular approach is based on the hybridization of multiple CMOS DPS arrays (ROIC modules) with a large seamless direct conversion detector as illustrated in Fig. 4.5(a).

Following Fig. 4.5(b), peripheral rows/columns (identified as I/O pixels) are added to ROIC pixels array for modules interconnection. Furthermore, flip-chip techniques require a minimum distance between modules (S) for satisfactory hybridization, and integration technology fixes the space of CMOS DPS array (F, L and E) to the chip cut. Therefore, in order to obtain a seamless detector array with P_{det} pitch, ROIC module pixels must reduce their pitch to P_{dps}, so rerouting at detector level is needed to connect each CMOS readout pixel with its corresponding detector pixel.

As a result, given an optimum ROIC size M due to economical rules, the number of pixels per ROIC module is:

$$N_{pix} = \frac{M + 2E + S}{P_{det}} \tag{4.1}$$

while the required pitch of the resulting DPS is found to be:

$$P_{dps} = \frac{M - 2(L + F + D)}{N_{pix}} = \frac{M - 2(L + F + D)}{M + 2E + S} P_{det} (< P_{det}) \tag{4.2}$$

If larger modules are used (higher M), larger P_{dps} values are obtained ($\partial P_{dps}/\partial M > 0$) and thus simpler detector routing is needed.

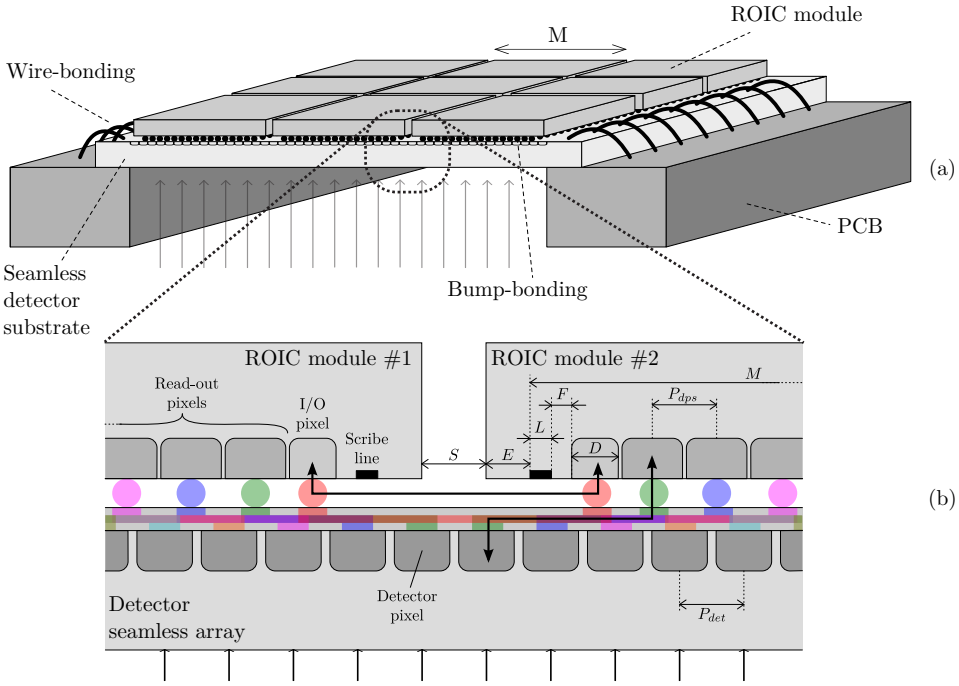


Figure 4.5 | General concept of the hybrid 2D modular assembly (a) and detailed cross section (b).

Taking the practical case of UMCL180 CMOS technology ($M = 5$mm, $E = 60\mu$m, $F = L = 10\mu$m), the in-house IMB-CNM(CSIC) available flip-chip technology ($S \geq 50\mu$m) and a target pixel pitch of 55μm at detector level, the required pitch at ROIC side is $51.6\mu\text{m} < P_{dps} < 52.2\mu\text{m}$ for $55/2\mu\text{m} < D < 55\mu\text{m}$, resulting in $N_{pix} = 94$ pixels per module.

For the reason discussed above, the DPS52 pixel design has been addressed, as shown in Fig. 4.6.

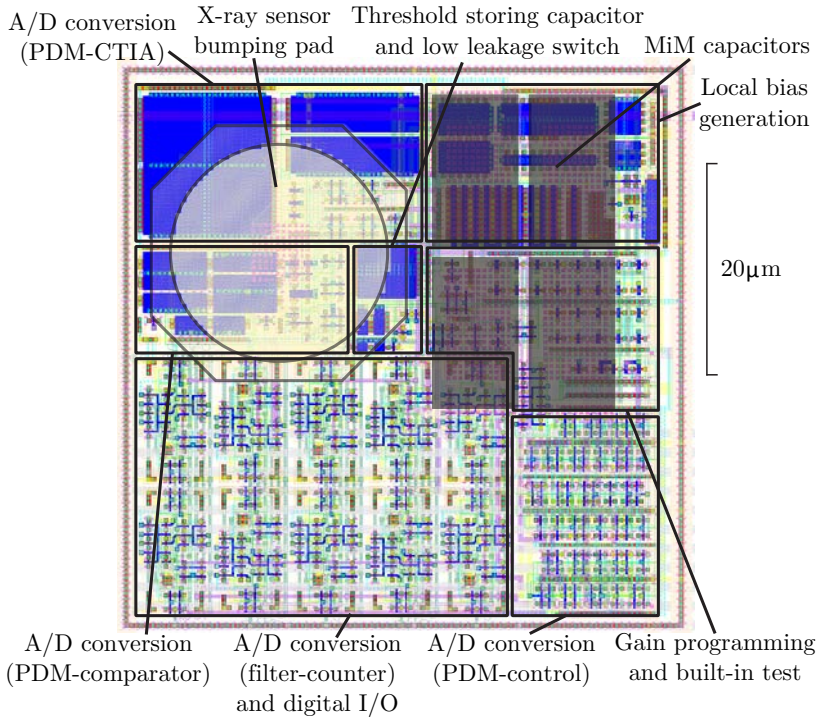


Figure 4.6 DPS52 pixel layout and main circuit blocks. Bounding box is $52\mu\text{m}\times52\mu\text{m}$ while bumping pad diameter is 20μm.

The only DPS52 pixel architectural difference respect to the DPS55 design is an improvement of the counter/shift-register modules, increasing their area and forcing a reduction in the number of bits to 11. This is not a major issue since dark current equivalent DC offset is very low for areas

as small as 55μm×55μm. Furthermore, the individual enable flag to turn on the bias circuits is also removed in order to save more area. As it will be seen in Chapter 5, no crosstalk is observed between pixels, and there is no need to turn off malfunctioning pixels. Therefore, the operation of the DPS52 is the same as with DPS55 but without the PWP stage. Finally, Fig. 4.7 shows all the pixel generations physical layouts for comparison.

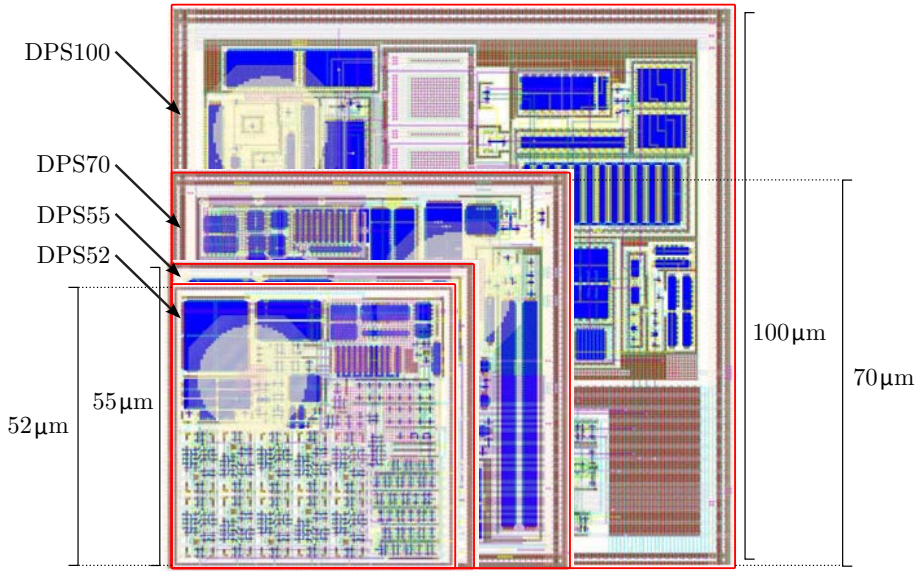


Figure 4.7 | Physical comparison of all CMOS DPS designs developed in UMCL180 technology.

4.4 Pixel Test Chips

Based on the proposed CMOS pixel designs, test vehicles have been developed for each DPS generation described in Section 4.2. These integrated circuits are designed for deep characterization of the internal pixel circuits. In this sense, a set of experiments are included in the test chips for pixel parameters extraction.

4.4.1 100μm-pitch DPS Test Vehicle

Fig. 4.8 shows the test vehicle chip for the DPS100 pixel design. It includes seven standalone pixels and a tiny array of pixels. This last experiment, aimed to study any crosstalk, is formed by pixels that can be tested using their built-in test mechanisms. Two alternatives for I/O test signals are implemented to deal with the test patterns commented in Section 2.4. In addition, the input of two particular pixels can be stimulated with a built-in current emulator. The other seven experiments are serially connected through the I/O interface, and aimed to extract different pixel parameters/characteristics as listed below:

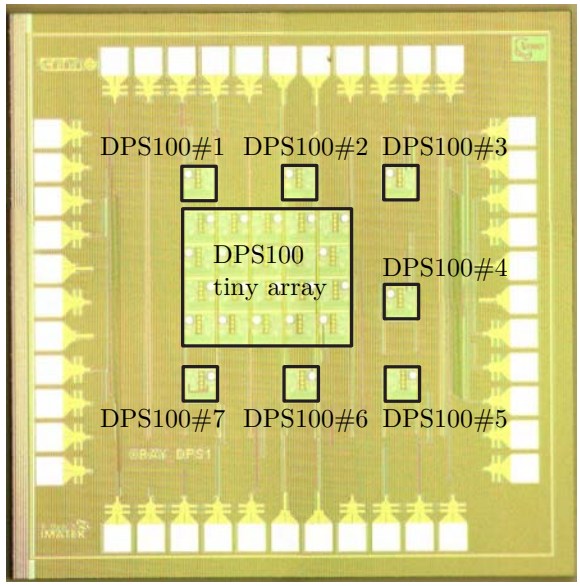


Figure 4.8 Microscope photography of the test chip integrated in UMCL180 technology for the exhaustive electrical characterization of the DPS100 pixel. Bounding box is 1.5mm×1.5mm.

Experiment DPS100#1. This standalone pixel is the first of the chain and is devoted to study CMOS DPS regular behavior using the built-in test capability by observing its digital output at the end of the

pixels chain. Therefore it requires no extra circuitry.

Experiment DPS100#2. This second pixel is also included to characterize the regular behavior of the CMOS DPS either using the built-in test capability or an external DC current stimulus (or both). In this case, a current emulator is added to supply an input current to the readout pixel.

Experiment DPS100#3. The third arrangement is focused on the characterization of the locally generated reference voltage and bias current (V_{ref} and I_{bias} in Fig. 3.14). Furthermore, biasing levels can be externally forced to test pixel behavior under different operating conditions for its internal circuits.

Experiment DPS100#4. As in the previous experiment, one can access V_{ref} and I_{bias} of this pixel. In this case, external input stimulation is also available using sensor emulator.

Experiment DPS100#5. The output of the CTIA (V_{int} in Fig. 2.6) of this pixel is buffered through a source follower stage with the aim of characterizing the in-pixel dark current cancellation, the charge integration and the built-in test circuit blocks.

Experiment DPS100#6. Like in the preceding experiment, V_{int} can be also studied. Moreover, this circuit includes direct external stimulation to further characterize the PDM CTIA stage of the in-pixel ADC.

Experiment DPS100#7. In this last case, V_{int} can be externally accessed as an input to bypass the PDM CTIA stage and characterize the in-pixel ADC quantizer.

Sensor emulators for the above experiments are simply made of large and long NMOS devices, which can be externally controlled and monitored to deliver both DC and dynamic input currents to the corresponding DPS cell.

4.4.2 70μm-pitch DPS Test Vehicle

Regarding DPS70 pixel validation, the corresponding test chip has been also integrated as shown in Fig. 4.9. In this case, it is comprised of four

experiments with their digital I/O linked in series plus a small array as in the preceding test vehicle chip.

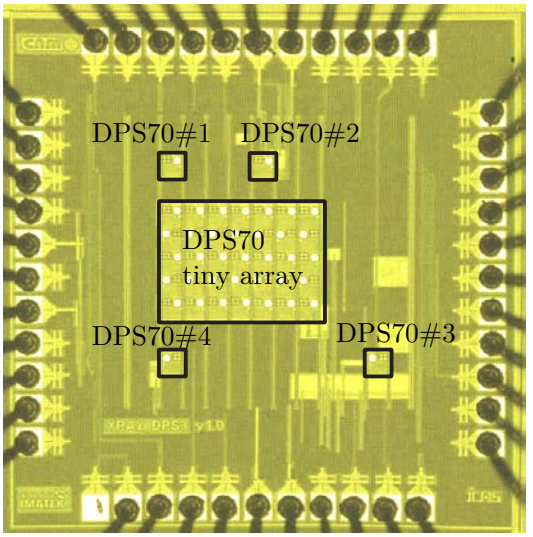


Figure 4.9 Microscope photography of the test chip integrated in UMCL180 technology for the exhaustive electrical characterization of the DPS70 pixel. Bounding box is 1.5mm×1.5mm.

Experiment DPS70#1. This first pixel of the chain, without any extra circuit, is included for the characterization of this new pixel version using the built-in test capability and observing its digital lecture at the output of the pixels chain.

Experiment DPS70#2. External access to V_{ref}, I_{bias}, V_{int} and the comparator output (V_{pdm} in Fig. 2.6) of this pixel allows a deep characterization of all its internal circuits. The biasing levels can be externally forced and V_{int} and V_{pdm} are output buffered using a source follower stage and a digital buffer, respectively.

Experiment DPS70#3. The third experiment is a copy of the previous one but using a 10-bit programmable current source as a sensor emulator, and a dedicated analog buffer specially designed to output signals

with waveforms as V_{int} in Fig. 2.7(b). This last circuit is used instead of the source follower stage of the previous experiment to overcome its dynamic range and bandwidth limitations..

Experiment DPS70#4. The last pixel in the chain is included for directly injecting an external signal at the input of its comparator and extract its output through a digital buffer. The digital output of the register/counter chain is also buffered to an external pin.

4.4.3 55μm-pitch DPS Test Vehicle

The test vehicle for DPS55 pixels is presented in Fig. 4.10 and it is comprised of seven experiments again linked in series together with a tiny array of pixels.

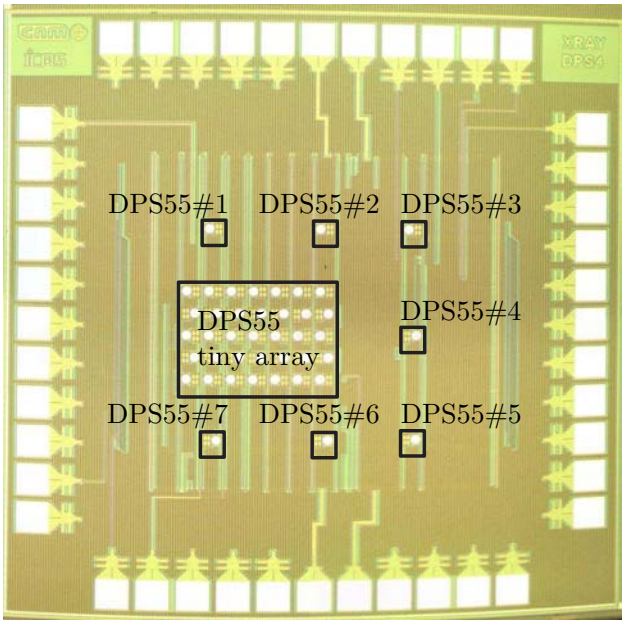


Figure 4.10 Microscope photography of the test chip integrated in UMCL180 technology for the exhaustive electrical characterization of the DPS55 pixel. Bounding box is 1.5mm×1.5mm.

Experiment DPS55#1. The digital lecture of this pixel can be used to study the pixel behavior under external input stimulus, using an NMOS transistor as a sensor emulator, and/or under charge test injections using the built-in test circuitry.

Experiment DPS55#2. Threshold value of this standalone pixel ($V_{ref} - V_{th}$ labeled node in Fig. 2.6) is extracted using an output analog buffer for the characterization of the in-pixel DAC and the low-leakage switch.

Experiment DPS55#3. For the characterization of the reference voltage and biasing current (V_{ref} and I_{bias} in Fig. 3.14), these parameters are extracted. They can also be externally forced to study the behavior of the pixel under different operating conditions.

Experiment DPS55#4. In this case, a current DAC is included to supply the input current stimulus. Also, input and output of the comparator are extracted using analog and digital output buffers respectively.

Experiment DPS55#5. For a full characterization of all the internal circuits of the pixel, this experiment includes a sensor emulator transistor and its V_{int}, V_{ref}, I_{bias} and V_{pdm} (from Fig. 2.6) are extracted.

Experiment DPS55#6. The comparator input of this pixel can be externally supplied and its output is digitally buffered in order to characterize the comparator stage.

Experiment DPS55#7. This pixel is added in order to study pixel power consumption. For this purpose, it has its own power supply pin but no extra circuitry.

4.5 Array Test Chips

Previous section has presented the custom ASICs developed for deep electrical characterization of the proposed CMOS pixel designs. In order to evaluate the behavior of these circuits under real radiation, small pixel arrays have been also developed for their hybridization with direct X-ray detectors.

Unlike pixel test chips, array test chips for each pixel generation include a matrix of as much pixels as can fit in the 1.5mm×1.5mm UMCL180 miniasic area taking into account that some room must be saved for the I/O padring.

In all cases, the array is formed by daisy chained pixels forming a chessboard test pattern, as in Fig. 2.10, by combining two splitted test signals. Therefore, only one serial data input and one serial data output are required.

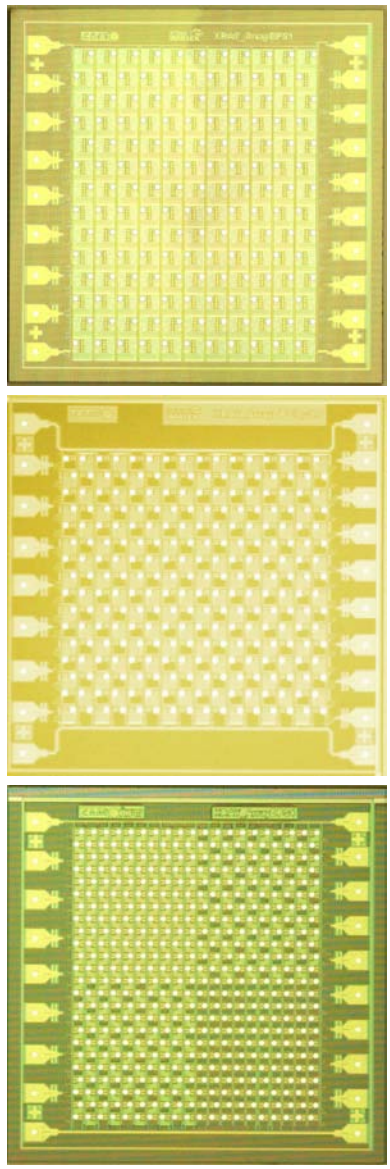
Fig. 4.11 shows microscope photographs of the resulting chips while Table 4.3 lists their array properties. As seen, all fabricated ICs present the same pinout configuration in order to be able to reuse the same test setup for each pixel generation.

	Array size	**Array area**
DPS100	11×14	1.10mm×1.40mm
DPS70	16×16	1.12mm×1.12mm
DPS55	20×24	1.10mm×1.32mm

Table 4.3 | Developed array properties for each pixel generation.

These pixel arrays can also be used to study the effect of CMOS design for manufacturing (DFM) metal filling on the X-ray image. In this sense, four different dummy patterns can be easily identified for each quadrant of the array of Fig. 4.11(c)

Concerning DPS52 design, since the only changes respect to DPS55 are related to digital communications and the layout, only the array test chip has been integrated. Considering that the scope of this work is the advanced CMOS design of DPS circuits for hybrid direct X-ray imagers, leaving ROIC modularity deep study for future studies, and in order to reuse most of the radiation test setup for the DPS55 pixels array, the integrated chip consists on a CMOS array of DPS52 pixels spaced out 55μm.



(a) (b) (c)

Figure 4.11 Microscope photographs of the DPS100 (a), DPS70 (b) and DPS55 (c) array test chips integrated in UMCL180. Bounding boxes are 1.5mm×1.5mm.

Experimental Results | 5

As explained in the preceding chapter, pixel designs are validated experimentally through two different types of test. First, the pixel test chips of Section 4.4 are used for characterization at electrical level. Second, array test ICs are hybridized with pixelated Si detectors and measured under X-ray radiation. Following sections describe the corresponding lab setups developed for these experimental tests. In this sense, obtained performance for all the three DPS generations are reported. Finally, the results of these characterizations are compared to the state-of-the-art already reviewed in Section 1.3.

5.1 Custom Si-Based X-Ray Detector Arrays

Regarding tests under radiation, results are extracted by illuminating a detector with an X-ray beam and acquiring information through the ROIC flip-chip hybridized to that.

Here, this ROIC corresponds to the arrays presented in Section 4.5, while the detector consists on a direct conversion semiconductor detector as reviewed in Section 1.2.3.

Based on the low-cost 2.5μm 1P1M CMOS technology available at the IMB-CNM(CSIC) clean room for micro and nano fabrication, the direct conversion semiconductor detectors have been designed and developed in the own institute using 4-inch diameter and 300μm-thickness N-type wafers.

As illustrated in Fig. 1.8, these detectors are suitable for X-rays particles with energies under 20keV. Although CdTe based detectors exhibit higher efficiencies when compared to their Si counterparts, the latter are used due to both economical and technology advantages.

Starting from N-type substrate, pixelated detectors are defined at back side with P-type implants to obtain p-n junctions which can collect holes under reverse bias. Each pixel includes also a pad where bumps for ROIC connection are grown. At substrate periphery, wire-bonding pads are included for external connectivity while the whole array of pixels at this detector level is surrounded by a guard ring, with its own wire-bonding pads. Regarding detector front side, it is fully metalized to apply the high-voltage bias.

Fig. 5.1 shows microscope photographs of the detector arrays designed for each CMOS pixel generation. As pointed in Section 4.5, the external connectivity is maintained in each design to reuse similar laboratory setups. In the same figure, some more detailed images of the connecting bumps are included. Bump growing step is carried out at Fraunhofer IZM [97], which offers an electroless bumping process of SnPb. Since the initial bumping pad is Al-based, a Ni-Au alloy is deposited on pads to make solderable bonding possible [98]. This process of under bump metalization (UBM), is previously done at in-house IMB-CNM(CSIC) facilities.

As pointed in Section 4.2, bump pads present 20μm-diameter for all the three design generations, which means that in the detector pixels array of Fig. 5.1(c), bumps are quite close to each other. However, the high repeatability of these technologies assures a good yield of the complete process.

The measured reverse saturation current of the p-n junctions at room temperature is around 5nA/cm^2. This value means dark current levels in the range of hundreds of fA per pixel for the proposed pitches. On the other hand, the detector is fully depleted at reverse polarizations of few tens of volts, and presents breakdown voltages around 500V of reverse bias.

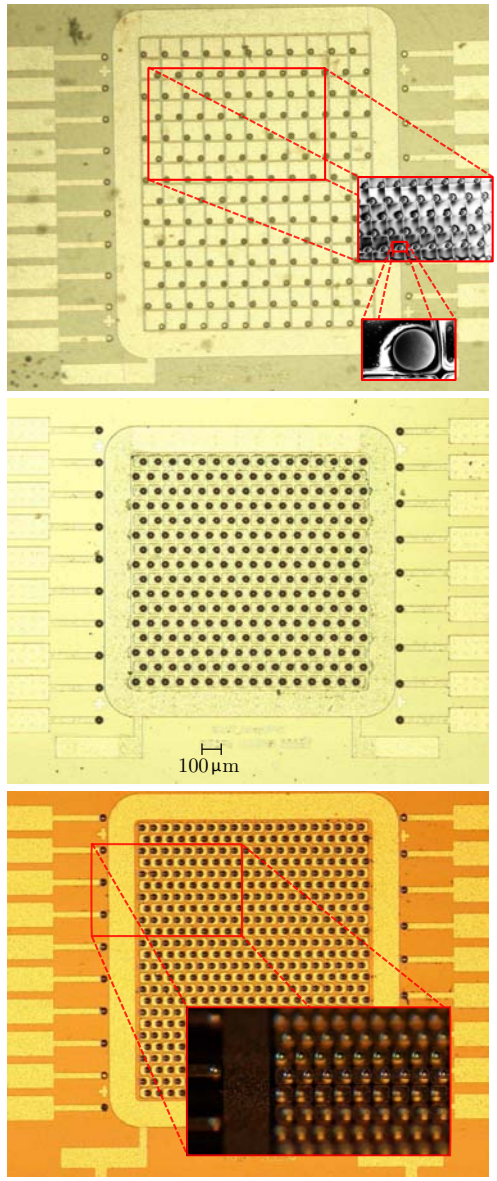


Figure 5.1 Microscope photographs of backsides of Si-based pixelated X-ray detectors with grown bumps to be hybridized with DPS100 (a), DPS70 (b) and DPS55/52 (c) CMOS ROICs of Fig. 4.11.

5.2 Hybrid Packaging and Lab Setup

Electrical tests are performed on pixel test chips of Section 4.4 and using instrumentation available at IMB-CNM(CSIC) laboratories. To interface these test vehicles, IC dies are encapsulated in 48-pin dual in-line (DIL) ceramic packages. For each DPS generation, printed circuit boards (PCBs), including zero insertion force socket for the packaged chips and all extra needed interface circuitry, are designed and fabricated at institute facilities in order to link test vehicles to lab instrumentation.

A more challenging setup is required for radiation tests. First, complete X-ray imagers are obtained hybridizing CMOS pixel arrays of Fig. 4.11 with Si-based detector pixel arrays of Fig. 5.1. This step is also done at IMB-CNM(CSIC) using flip-chip techniques [98]. Second, a custom PCB as global chip carrier is designed and fabricated. Fig. 5.2 depicts the full X-ray hybrid imager scheme. Since the wire-bonding pads and the ROIC are only accessible through detector back side, the custom PCB must contain a radiation window to allow the illumination of detector front side. On the other hand, detector substrate is glued to a PCB pad surrounding radiation window using thermal and electrical conductive adhesive in order to supply the required high-voltage biasing. Moreover, this pad and the wire bonding pads are gold coated to assure low resistivity contacts. Finally, both X-ray sensor and wire-bonds are protected with glob-top. The same Fig. 5.2 shows a photograph of the hybridized detector and ROIC once wire-bonded to the custom PCB and before glob-top coating.

To complete the setup for radiation tests, the X-ray imager is connected to a field programmable gate array (FPGA) based PCB which in turn communicates with a personal computer (PC) using an on-board universal serial bus (USB) interface controller module. The FPGA PCB is in charge of generating the control signals chronogram required for the DPS array operation, and receiving the digital lectures obtained in each image acquisition. It is based on a low cost Cyclone FPGA from Altera [99]. The hardware design is schematized in Fig. 5.3, including the chronogram signals generator, the finite state machine with all the operation stages and its control, registers for this control parameters and two first-in first-out (FIFO) data buffers for individual pixel programming codes and for pixel read-out.

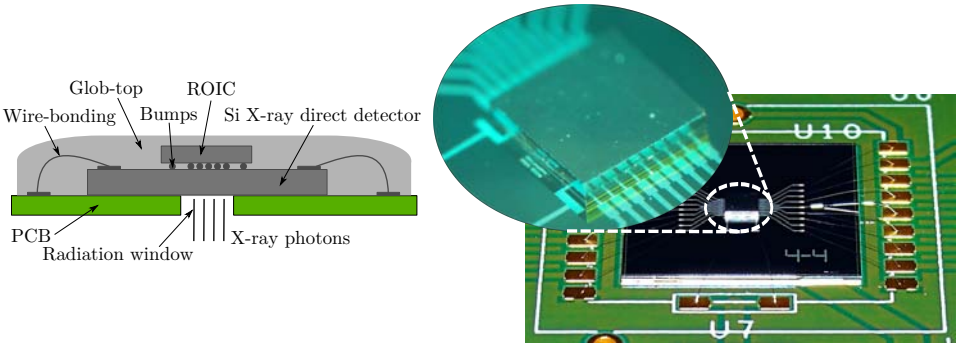


Figure 5.2 Cross-section scheme (left) and photograph (right) of the X-ray hybrid imager after flip-chip wire-bonding to the windowed PCB.

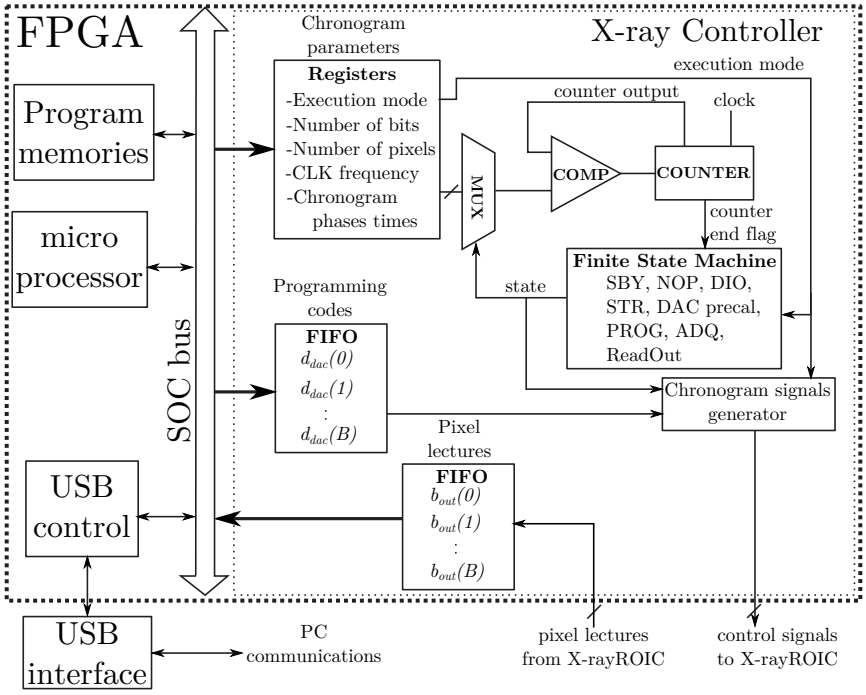


Figure 5.3 Simplified scheme of the FPGA-based interface for the radiation tests of X-ray hybrid imagers.

The last stage of the complete lab setup consists on an application running in standard PC. Apart from being the user interface, this custom software sets the configuration parameters of the chronogram operation, such as the execution mode, the individual programming codes for each pixel of the array and the chronogram phases duration. Moreover, it collects and saves the output lectures of the array, and it is able to perform post-processing equalization and read previously saved images. A screenshot example of the resulting human machine interface (HMI), which is fully developed in C++ general purpose programming language, is presented in Fig. 5.4.

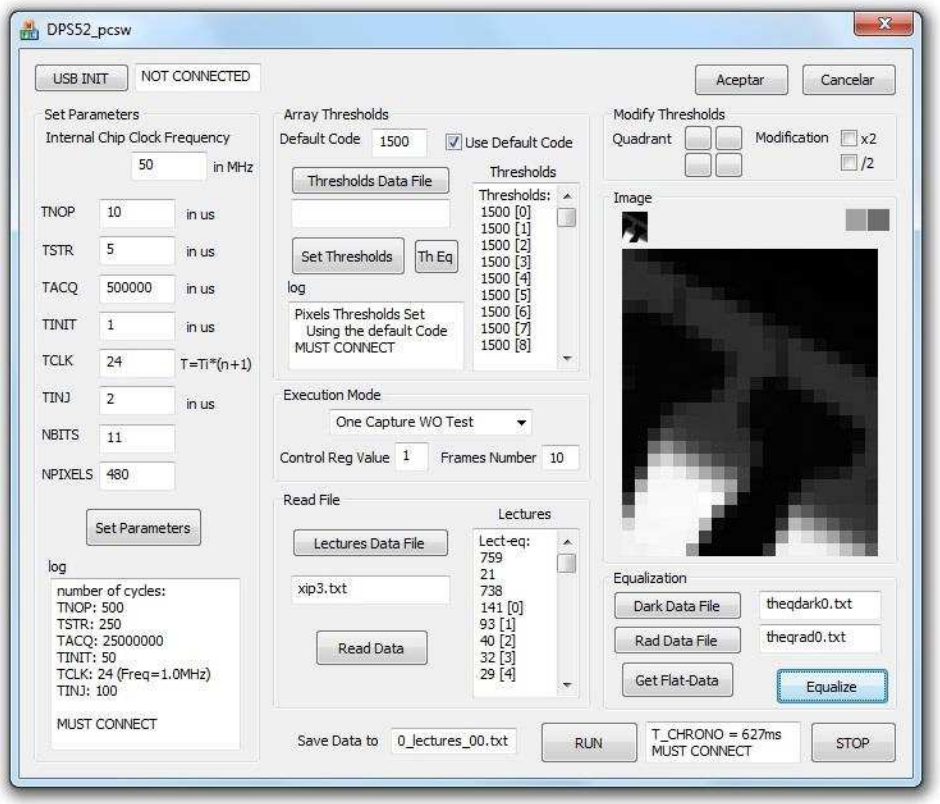


Figure 5.4 | Screenshot of the custom HMI developed for the radiation tests of X-ray hybrid imagers.

5.3 Electrical Tests

Standalone DPS cells of test chips described in Section 4.4 are intended for individual pixel blocks verification through electrical measurements at room-temperature. Obtained results from the characterization of all three generation pixel designs are summarized in Table 5.1. Regarding DPS52 design of Section 4.3, the experimental electrical results correspond to those of DPS55 design only updating the output dynamic range to 10 bit and silicon area to 52×52 μm^2. Furthermore, taking advantage of the extra circuitry added to these test chips, the expected behavior of the main signal waveforms can be verified.

Parameter	**DPS100**	**DPS70**	**DPS55**
Silicon area	100×100 μm^2	70×70 μm^2	55×55 μm^2
Supply voltage	1.8 V		
Reference voltage (V_{ref})	700 mV	815 mV	830 mV
Biasing current (I_{bias})	270 nA	550 nA	620 nA
Bias mismatching ($\pm\sigma$)	$< 10\%$	$< 15\%$	$< 15\%$
Static power consumption	< 10 μW		
Integrating capacitor	≈ 100 fF		
Output dynamic range	10 bit	10 bit	12 bit
Integration time	10 to 1000 ms		
Input full scale	> 10 nA		
Reset pulse width (T_{res})	0.5 μs		
Threshold programming word	11 bit	11 bit	13 bit
Conversion gain	1/250 to 1/25 LSB/ke$^-$		
Digital I/O speed	> 50 Mbps		
Max. PDM frequency	500 kHz	600 kHz	900 kHz
Inter-pixel crosstalk	< 0.5 LSB		
Dark current range	0.01 to 20 nA	0.01 to 20 nA	NA
Compensated dark current	95 %	95 %	NA
Equivalent noise charge	< 2 ke$^-_{rms}$		

Table 5.1 | Comparison of CMOS DPS parameters for the three design generations developed in this work.

The measured low-power consumption helps obtaining a good performance of the system at room-temperature since it does not cause relevant heating of the X-ray detector itself, which would otherwise degrade its behavior especially regarding its dark current.

The tiny arrays of pixels included in the pixel test chips are used to study inter-pixel crosstalk, since single pixels can be stimulated at full-scale input while their neighboring pixels receive no input signal. Thanks to the local references generation and digital-only communications between pixels, no crosstalk effects have been observed even working at low threshold levels, leading to an improvement of the sharpness and contrast of X-ray imagers.

The robustness of the proposed pixel designs and layout implementations is verified from the low mismatching of both V_{ref} and I_{bias} obtained from measurements on all fabricated samples. As manifested in Fig. 5.5 and Fig. 5.6, it has been proved that the bias generation circuit of Fig. 3.14 can work at supply voltages as low as 1.1V. According to Pelgrom Law [100], mismatching deviations are inversely proportional to the square root of the MOS transistor area, so the reduction of transistor length and width from DPS100 to DPS70 and DPS55 designs, doubles mismatch effects. Therefore, the large disparity observed in I_{bias} values for the three design generations is basically caused by the scaling down of transistor sizes and the repercussion of the traced layout, which magnify the mismatching and second order effects in parameters such as the current factor β considered in Section 3.5.

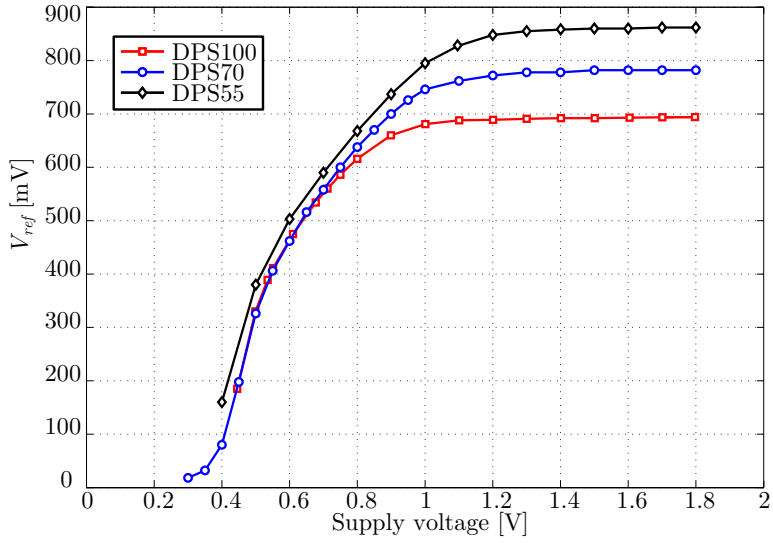


Figure 5.5 | Experimental voltage supply sensitivity of the in-pixel reference voltage for the three DPS generations.

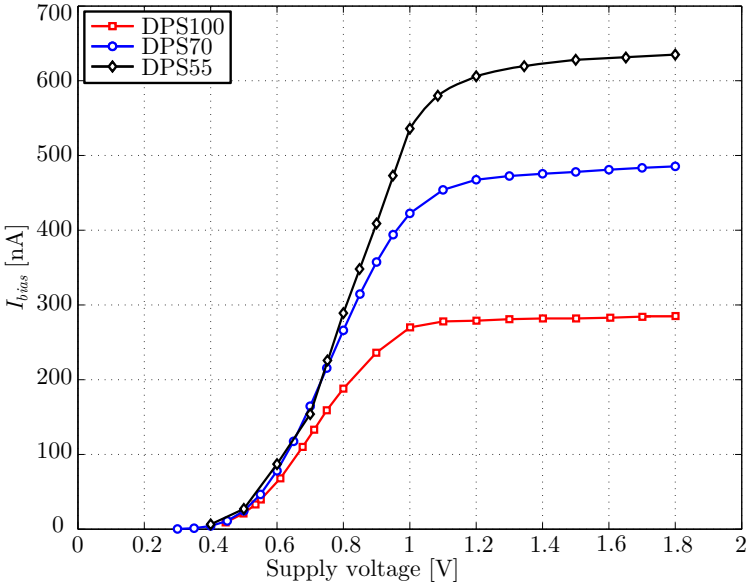


Figure 5.6 | Experimental voltage supply sensitivity of the in-pixel bias reference for the three DPS generations.

Regarding the temperature compensation of the in-pixel generated V_{ref}, sensitivities under 120ppm/°C are obtained in Fig. 5.7 despite the risk of mismatching effects on the compensation constraint of Eq. (3.39).

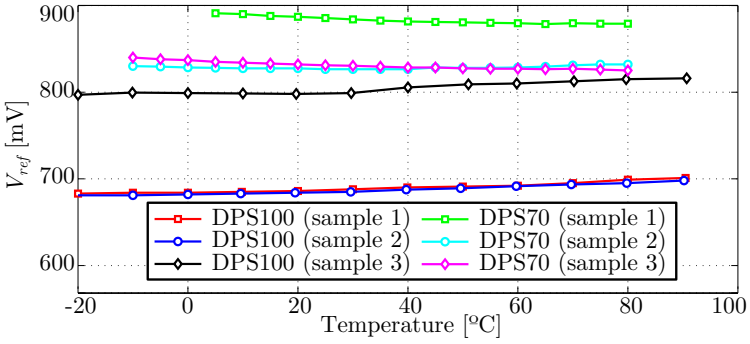


Figure 5.7 | Experimental thermal sensitivity of in-pixel reference voltage extracted from several samples of DPS100 and DPS70 designs (DPS55 design is similar).

The analog input circuit of the proposed DPS architecture does not saturate for input DC currents up to 10nA or higher, depending on the programmed conversion gain. The novel lossless charge integration circuit (Section 2.2) does not block the input signal integration during reset time. This strongly improves the linearity at high radiation fluxes as demonstrated in Figs. 5.8 and 5.9, where the frequency of the PDM output pulses presents a notorious linear response following the f_{PDM} behavior of Eq. (2.2), even for frequency values close to $1/T_{res}$, up to 1×10^6events/s. Since in charge-integration pixels each event corresponds to several photons, and the maximum count rates of photon-counting pixels is usually around 1MHz (1×10^6 photons/second) [71], it is clear that this proposal extends the dynamic range to photon fluxes that cause the pile-up effect on photon-counting pixels. This feature reduces the brightness distortion from the X-ray imaging point of view. The high linearity through all input signal range, combined with practical integration times reported in Table 5.1, make the proposed DPS suitable for a wide range of applications, from synchrotron equipments using high photon fluxes, to medical imaging requiring lower fluxes.

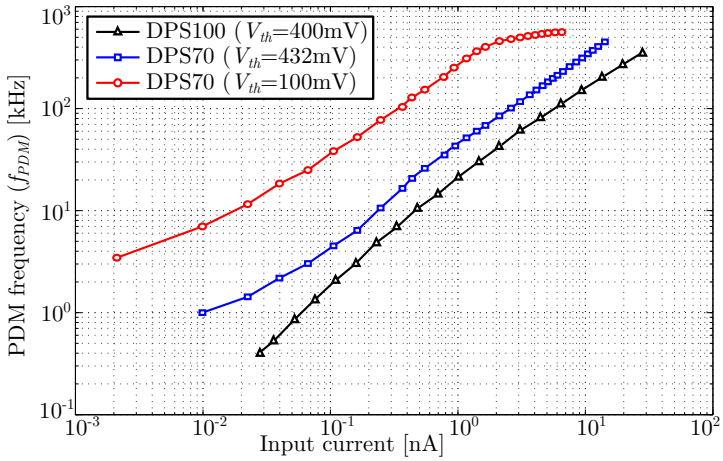


Figure 5.8 Experimental PDM transfer function of the in-pixel ADC measured in DPS100 and DPS70 pixel generations. In the case of DPS70, data for two different gain programming levels is shown. Results are obtained using a DC input current to standalone pixel experiments of Fig. 4.8 and Fig. 4.9.

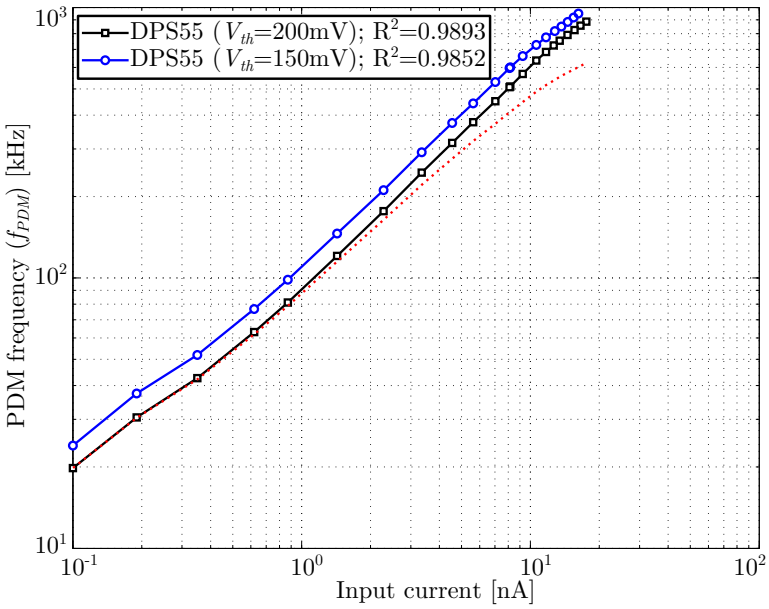


Figure 5.9 Experimental PDM transfer function of the in-pixel ADC measured in the DPS55 pixel design for two different gain programming levels. The red dashed line represents the transfer function using classic charge integration for $T_{res} = 0.5\mu$s. The classic schemes coefficient of determination ($R^2 \approx 0.95$) is clearly improved. Results are obtained using DC current as input to standalone pixel experiments of Fig. 4.10.

The conversion gain can be digitally programmed using the full range of digital codes supported by the pixel digital I/O interface. In this sense, the weight of a single count, also known as LSB, can be programmed from 25ke$^-$ to 250ke$^-$. Since the MSB of the counter is reserved as an overflow flag, the digital output dynamic range is given by the remaining bits of the ripple-counter, leading to a full scale charge above 250Me$^-$. On the other hand, the ENC is calculated using:

$$ENC = \frac{1}{q} C_{int} \sqrt{\int_{1/T_{acq}}^{\infty} V_{n\_CTIA-out}^2 df} \tag{5.1}$$

which is under 2ke^-_{rms} for a practical lower integration limit ($T_{acq} \leq 1\text{s}$). That is a reasonable value for a charge-integration system, which uses higher integrating capacitors when compared to their photon-counting counterparts. Furthermore, since it is much lower than the minimum LSB, it is not the limiting factor of the output dynamic range.

Concerning the compensation of FPN through the tunable gain of the in-pixel ADC, V_{th} in Eq. (2.2), Fig. 5.10 demonstrates the proper behavior described in Section 3.3 regarding the in-pixel DAC circuit and its precalibration procedure. Since programmability range extends over more than one decade, this feature is useful not only for practical FPN compensation but also brings flexibility to the system, allowing image preprocessing and adjustment of imager sensitivity to each particular X-ray application, detector type and image ROI. Results extracted from experiments on the DPS100 designs, where the precalibration procedure is not applicable, are not available since their pixel test chips do not include circuitry to directly obtain the programmed V_{th} value.

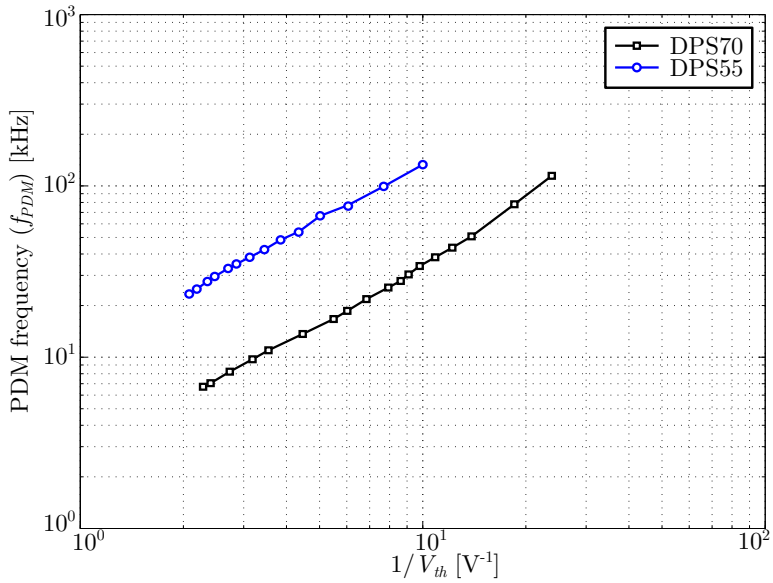


Figure 5.10 Experimental in-pixel ADC gain programming range under constant input currents for DPS70 and DPS55 pixel generations.

Dark current cancellation can be tested on DPS100 and DPS70 pixel designs. Fig. 5.11 depicts an example of the remaining current after compensating an equivalent dark current DC input in DPS70 pixels using the circuit described in Section 3.2.

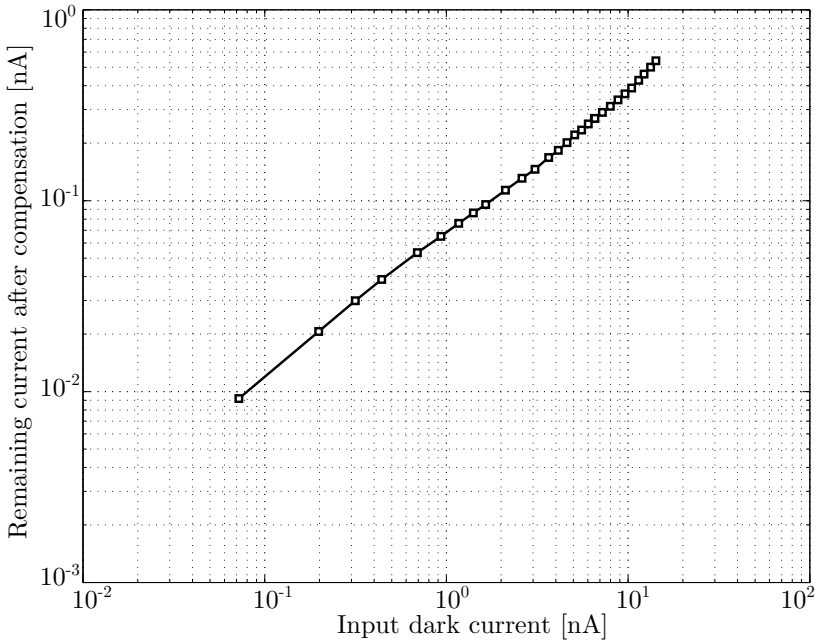


Figure 5.11 Experimental remaining current after dark current compensation for DPS70 pixel generation. Over 95% of the input dark current is canceled.

All the above experimental results are extracted after configuring the CMOS DPS cells for holes collection. Anyway, the tested behavior when collecting electrons is completely analogous.

5.4 X-Ray Tests

After hybridizing the ROICs of Fig. 4.11 with the detectors of Fig. 5.1 and using the setup described in Section 5.2, experimental results of tests under real radiation of the resulting X-ray imagers have been obtained.

For these experiments, more complex lab setups are needed compared to the previous tests of Section 5.3, since they require X-ray sources and high-voltage bisaing of detectors. Moreover, due to the small area of the arrays, standard evaluation methods to extract some of the FOMs, for example using commercial phantoms, are not applicable here.

All experimental data reported in this section corresponds to uncooled operation tests executed not only on DPS55 (or its analogous DPS52) but also on DPS70, since the latter incorporates features not included on the former, like the dark current cancellation circuit. As explained in Section 4.2.1, the initial 100μm-pitch pixel design example was developed mainly as a proof of concept of the proposed CMOS circuits, which are actually improved in subsequent pixel generations. Therefore, radiation tests results for DPS100 are not included here since they do not provide any significant extra information.

In this work test environment, radiation is produced through an X-ray tube with Tungsten anode, unfiltered output and with applied voltage (V_{tube}) and current intensity (I_{tube}). The former is associated with the maximum photon energy while the latter is directly related with the number of emitted photons. Fig. 5.12 shows the spectrum of a typical X-ray tube with Tungsten anode. Since in this case $V_{tube} \leq$ 50kV, only the characteristic peaks at about 10keV are present, while high energy photons of the characteristic peaks around 60keV and 70keV are not generated.

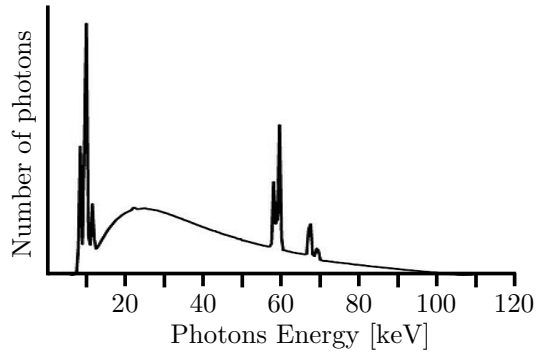


Figure 5.12 | Unfiltered spectrum of a typical X-ray tube with Tungsten anode [101].

X-ray detectors of Fig. 5.1 are fully depleted at biasing voltage (V_{com}) values as low as tens of volt. Unless otherwise stated, the nominal bias level is set at $V_{com} = 80$V. As already argued in Section 1.2.3,biasing of the guard ring surrounding detector array is also mandatory. If guard ring is disabled, outer pixels of the focal plane array (FPA) tend to collect a large amount of charge from the surrounding area of substrate detector.

Regarding dark current cancellation, which is usually performed before each acquisition, Fig. 5.13 shows comparative reading histograms for the DPS70 16×16 pixel array under the same test conditions but enabling or disabling dark current cancellation pixel circuits. The long acquisition time of these captures causes a wide distribution for the digital readings when dark current is not compensated. Furthermore, it demonstrates the validity of the circuit proposal since cancellation is maintained throughout the whole acquisition time, while the distributions mean verifies that about a 95% of that current is compensated. Moreover, the in-pixel gain programming circuit can also help in narrowing even more the final histogram.

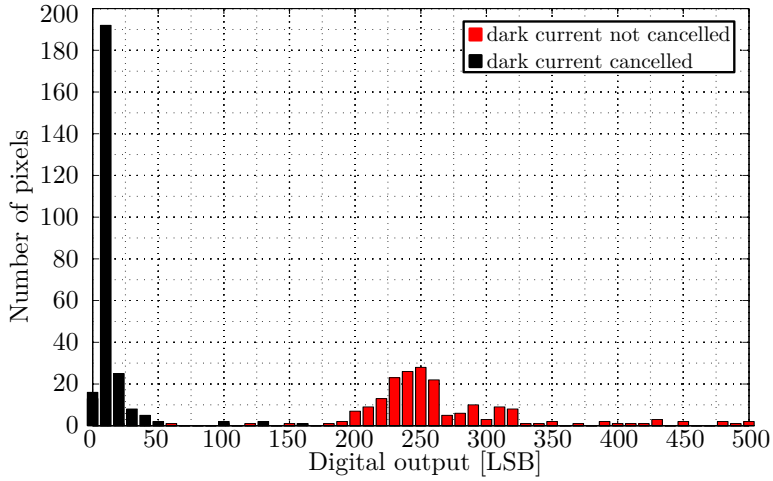


Figure 5.13 Experimental distribution of all pixel readings for the DPS70 16×16 pixel array under no X-ray illumination with and without in-pixel dark current cancellation. Detector is biased at $V_{com} = 50$V and large integration times are used ($T_{acq} = 3$s) without equalization ($q_{dac} = 1000$LSB for all pixels).

The behavior of the proposed X-ray sensors with photon flux is studied through the analysis of flat radiation images. Unless otherwise stated, the X-ray tube voltage and its current are set at their maximum values of V_{tube} = 50kV and I_{tube}=1000mA for all the following tests.

Fig. 5.14 reports digital outputs obtained for flat images captured with the DPS52 pixel array under several X-ray tube intensities. As it can be seen, the expected linear behavior with the number of incident photons is clearly obtained.

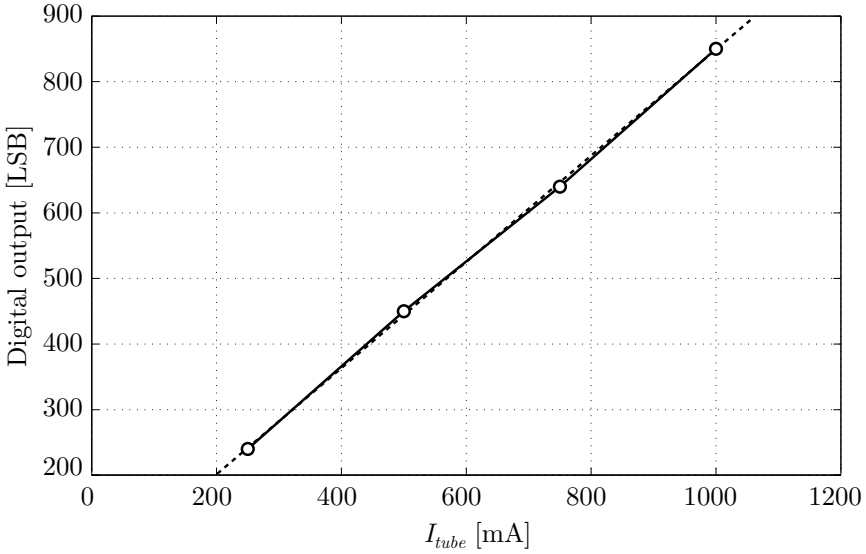


Figure 5.14 Experimental DPS52 digital output versus X-ray tube intensity for T_{acq}=1000ms and q_{dac}=2047LSB. Obtained coefficient of determination is $R^2 = 0.9996$.

The linear response to the number of photons is further verified in Fig. 5.15 by changing acquisition time as well. The low non-linearity demonstrates here the validity of the low leakage switch proposed in Fig. 3.11 to maintain the threshold programmed value during large integration times.

These results also proof that the proposed DPS can target several X-ray imaging applications, since good performance is maintained through wide ranges of acquisition times and radiation intensities.

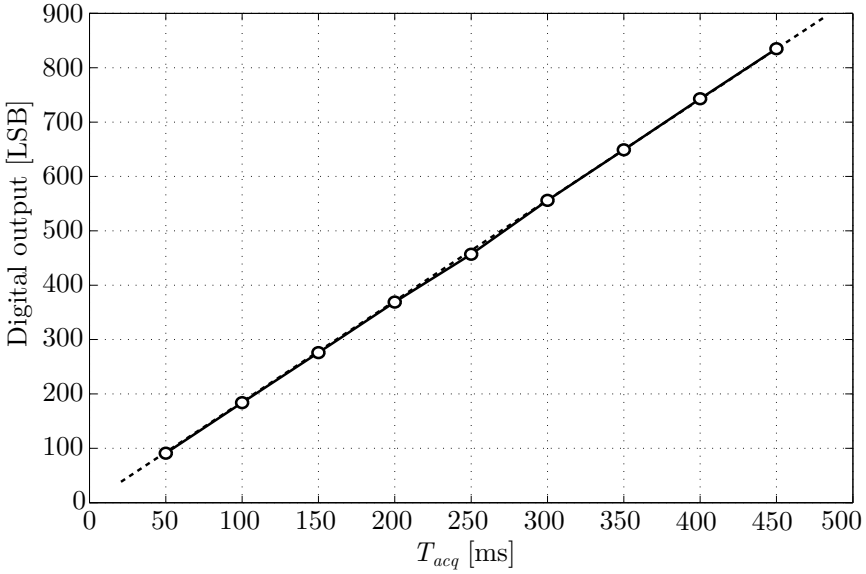


Figure 5.15 Experimental DPS52 digital output versus acquisition time for q_{dac}=1024LSB. Obtained coefficient of determination is $R^2 = 0.9999$.

Focusing on single pixel response, Fig. 5.16 demonstrates that high repeatability in pixel measurements is obtained. From the same results it is clear that dark current can be considered as DC input since dark current low variations ($< 3\%$) are obtained in repeated acquisitions. Dark current values extracted from Eq. (2.2) are around 3pA per 70μm×70μm pixel area, and they are mostly independent from detector biasing for $V_{com} \geq 20$V.

The same behavior is obviously observed in DPS52 pixels results of Fig. 5.17. In this case, the extracted dark current value is around 2pA per 55μm×55μm pixel detector area, which is consistent with the measurements on DPS70 counterparts. These current values are higher than the theoretically expected but still manageable without problem by the proposed pixel circuits.

The repeatability of single pixel readings under constant X-ray illumination is shown in Fig. 5.18 and Fig. 5.19 for DPS70 and DPS52, respectively. Deviations are under 3% in all cases.

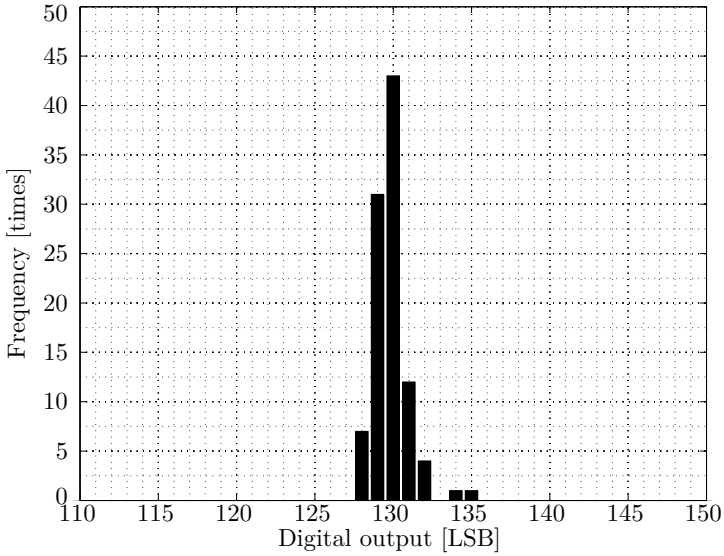


Figure 5.16 Experimental digital outputs distribution of a DPS70 pixel for 100 different dark current acquisitions. $V_{com} = 50$V, $T_{acq} = 1625$ms and $q_{dac} = 2047$LSB.

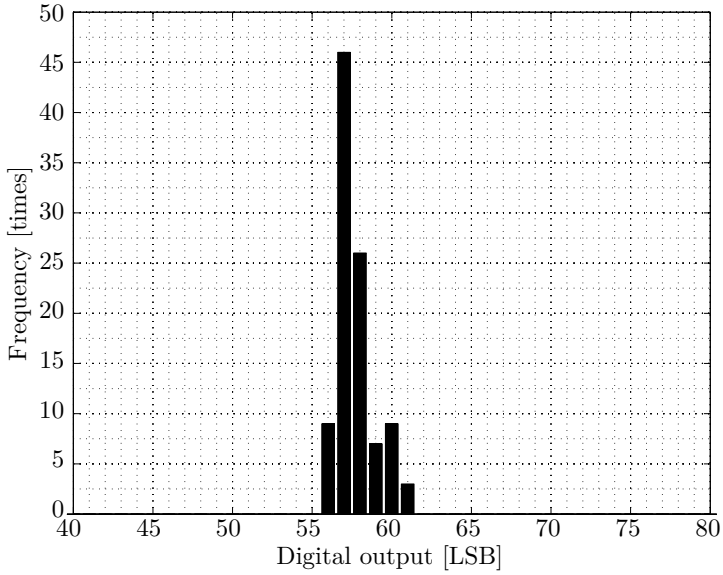


Figure 5.17 Experimental digital outputs distribution of a DPS52 pixel for 100 different dark current acquisitions. $V_{com} = 80$V, $T_{acq} = 1000$ms and $q_{dac} = 2047$LSB.

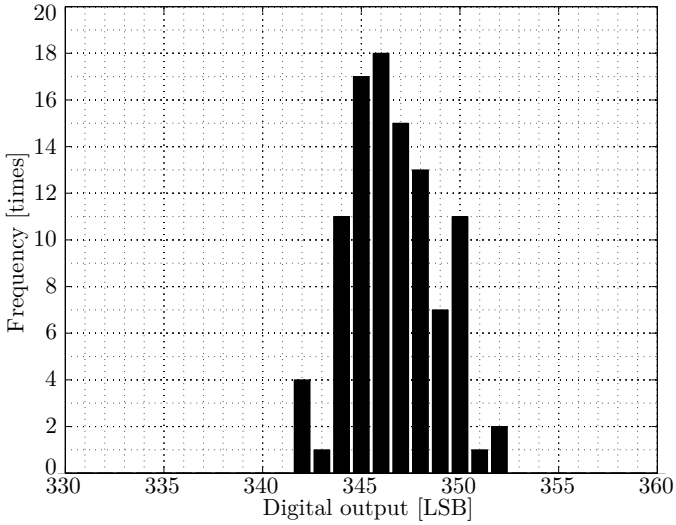


Figure 5.18 | Experimental digital outputs distribution of a DPS70 pixel for 100 different radiation acquisitions. $V_{com} = 80$V, $T_{acq} = 325$ms and $q_{dac} = 2047$LSB.

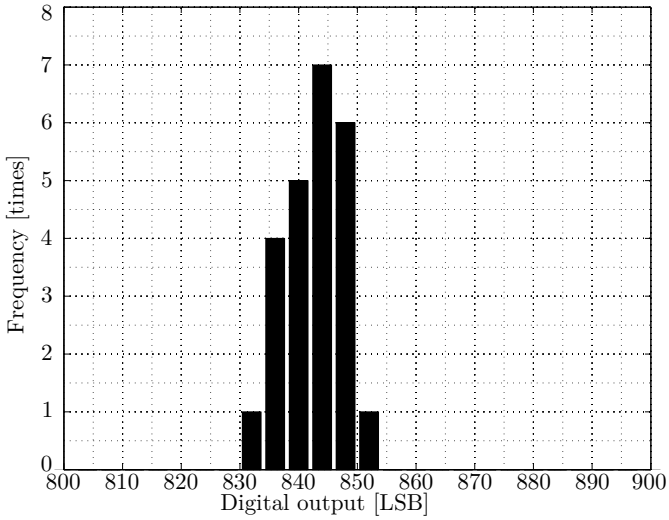


Figure 5.19 | Experimental digital outputs distribution of a DPS52 pixel for 24 different radiation acquisitions. $V_{com} = 80$V, $T_{acq} = 1000$ms and $q_{dac} = 2047$LSB.

Deviations in single pixel readings as shown in Fig. 5.16, 5.17, 5.18 and 5.19, yet small, are mainly caused by electronic noise, detector inhomogeneities and X-ray photons flux non-uniformity. Hence, they can be minimized reducing these three disturbances.

On the other hand, reading deviations in a flat illuminated pixel array, such as in Fig. 5.13, are originated not only from those three disturbances but also from inter-pixel mismatch. In practice, this unwanted behavior degrades SNR and contrast, resulting in a reduction of X-ray image sharpness. The distributions asymmetry is caused by the peripheral pixels of the array, which receive slightly more charge than the others despite the guard ring. The capability to reduce this and other mismatch effects is the main reason to introduce an individual gain programming circuit inside each pixel, which in turn brings flexibility to the system. Gain programmability capabilities of the PDM stage proposed in Fig. 2.8 is shown in Fig. 5.20 for the DPS52 array case, where average digital output for flat irradiated acquisitions is reported by modifying only the programming digital word q_{dac}. As proved with the experiment of Fig. 5.10, the programmability range is adequate both for practical FPN compensation and for adapting the system to the practical requirements of a wide range of applications.

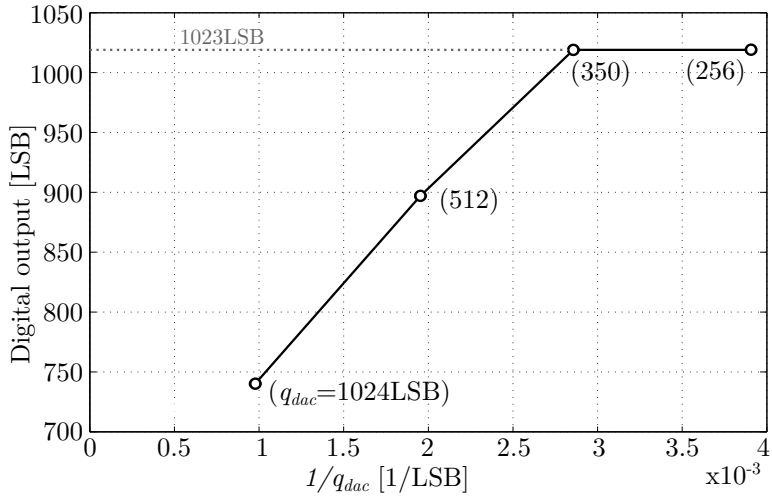


Figure 5.20 | Experimental digital output versus gain programming of a DPS52 pixel for T_{acq}=400ms.

FPN compensation feature can be also verified in Fig. 5.21, where the distribution of digital outputs for all pixels of the DPS52 array under flat radiation acquisition are shown before and after in-pixel equalization. This in-situ compensation is obtained after adapting each individual pixel threshold over few calibration iterations. As the number of iterations grows, more uniform digital images are obtained. The presented example corresponds to a case with only 10 calibration cycles of individual pixel gain reprogrammability. It is worth to note that even though the low number of iterations, a significant reduction of deviation in the measured digital output is achieved. The tail to high digital outputs of the equalized distribution of Fig. 5.21 occurs because the high initial q_{dac} code can not be incremented enough to further decrease the obtained digital output in some cases.

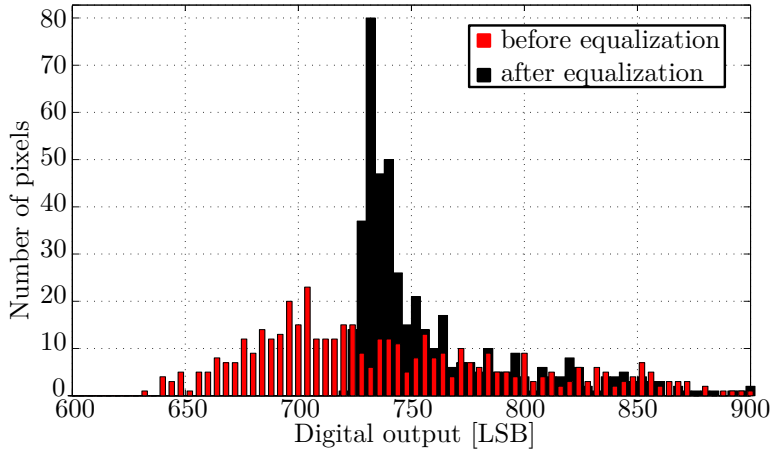


Figure 5.21 Experimental distribution of all DPS52 20×24 pixel array under flat radiation before and after in-pixel threshold equalization. Initial q_{dac} = 1000LSB is adapted for equalization in the course of 10 iterated captures (T_{acq}=400ms).

To further reduce image sharpness, and thanks to the high repeatability of pixel readings, a post-processing equalization, based on a flat-field correction, can be executed from the average dark current and non-attenuated radiation measurements of each pixel to merge all pixels responses to radiation. The more the measurements used to obtain these average measurements, the higher the reduction of residual statistic errors.

Fig. 5.22 shows the digital output distribution of the DPS52 pixel array from flat radiation captures before and after applying this post-processing equalization method. Final deviation on the digital outputs is clearly reduced, thus improving the resulting SNR.

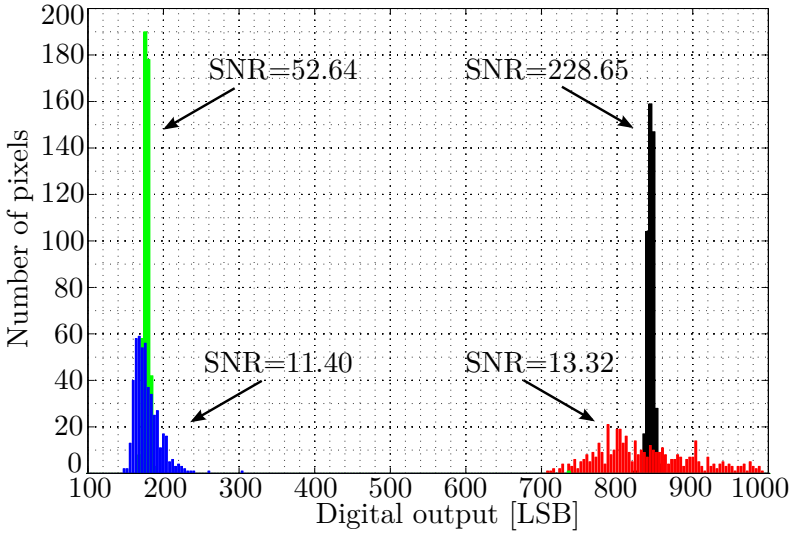


Figure 5.22 Experimental distribution of the DPS52 pixel array digital output under flat non-attenuated radiation before (red) and after (black) post-processing equalization. Distributions attenuating X-ray radiation with a 0.4mm thick Al sheet are additionally presented before (blue) and after (green) equalization. In both cases, T_{acq}=1000ms and q_{dac} = 2047LSB.

A widely used method to obtain X-ray imagers SNR is based on the analysis of distributions of pixel array readings under flat illumination [102]. This method consists in extracting the SNR from the mean value of the read-out distribution ($\bar{n}$) and its standard deviation (σ) as: SNR = $\bar{n}/\sigma$. Obtained SNR values with this method are included in Fig. 5.22. The charge-integrating nature of the proposed CMOS DPSs does not allow a direct calculation of the imager SNR theoretical limit, which depends on the radiation dose and it is already given by the Poisson statistics of the photons absorption in the detector as explained in Section 1.2.2. In a photon-counting sensor, this limit is given by the square root of the counted photons.

In this case, for the non-attenuated radiation capture of Fig. 5.22 and assuming an average energy for the incoming X-ray photons of 10keV, the average e^-/h^+ pairs generated per photon in a Si detector, which have an ionization energy of 3.63eV according to Section 1.2.3, is 2750. This means that given V_{th} = 0.40V and C_{int} = 100fF, each charge integration LSB corresponds to about 90 X-ray photons, leading to a SNR limit of 276 for this particular case. Therefore, the obtained SNR from the array lectures distribution corresponds to about 80% of this calculated theoretical limit.

Regarding the response to attenuated radiation, although standard phantoms are not practical in this case to extract typical contrast values, several materials and thickness values have been used to mitigate the incoming X-ray flux in Fig. 5.23. Again, the exponential behavior of the Lambert-Beer law referred to X-ray absorption can be observed, meaning that ROIC pixels do not degrade image contrast. Some pixel reading distributions for the radiation attenuated using kapton polyimide film and Al are mapped in Fig. 5.24.

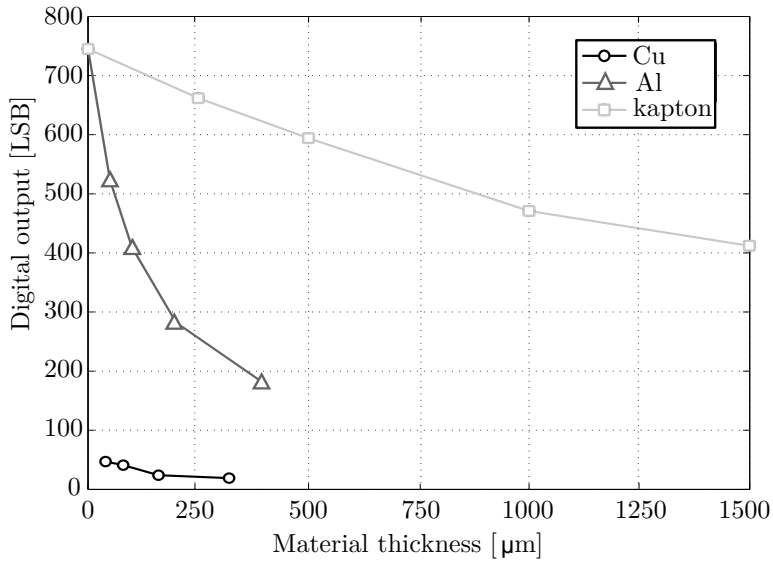


Figure 5.23 Experimental DPS52 pixel digital output obtained under radiation attenuation with several materials and thickness values for T_{acq}=400ms and q_{dac}=1024LSB.

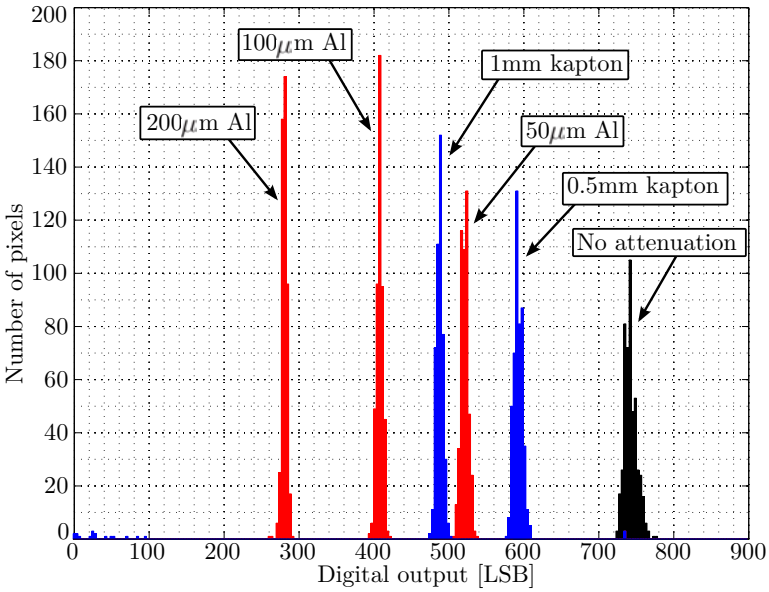


Figure 5.24 Experimental equalized distributions from DPS52 pixel array readings under flat non-attenuated radiation (black), and attenuation with 0.5mm and 1mm thickness of kapton (blue) and with 50μm, 100μm and 200μm thickness of Al (red). In all cases, T_{acq}=400ms and q_{dac}=1024LSB.

As explained in Section 1.2.2, MTF can be measured in practice by imaging a precision edge slightly tilted to the pixels column or row. Fig. 5.25 shows the MTF values obtained with DPS52 pixel array compared to Timepix [103] chip, used by commercial product XRI-UNO [104], operating in counting mode, hybridized with a 300μm-thick Si detector and using the same slanted edge MTF extraction algorithm [105]. This algorithm performs system MTF calculations up to twice the Nyquist frequency over slanted edge images. Due to the small size of the test array of this work, a single image has been replicated to obtain the minimum needed area by the algorithm for computation. As seen in Fig. 5.25, results from this work and Timepix pixels are comparable, since both pixels exhibit the same detector pitch (55μm) and MTF is extracted in both cases using the same algorithm on almost identical images.

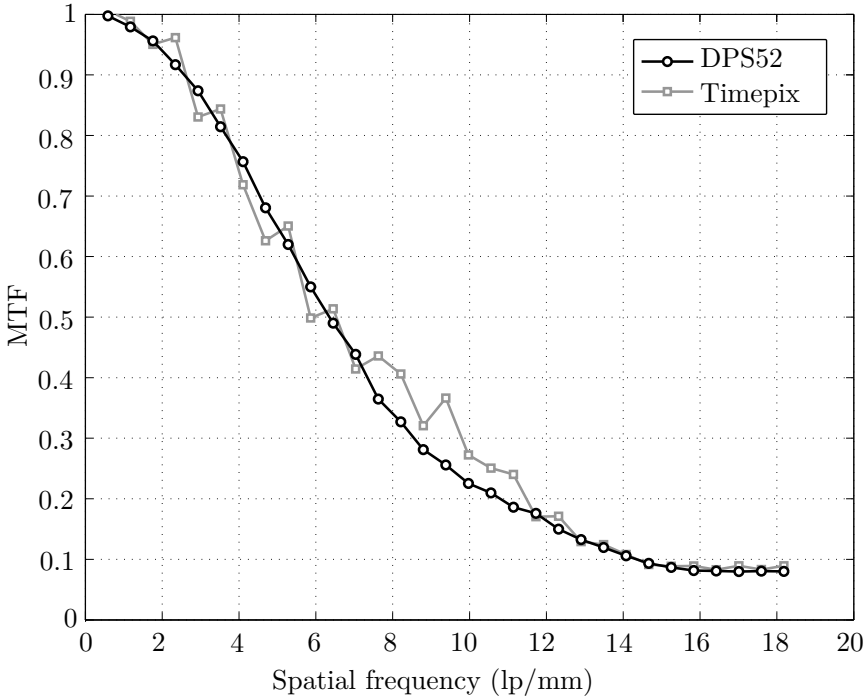


Figure 5.25 Experimental MTF from DPS52 pixel array compared to Timepix [103]. In both cases, the slanted edge MTF extraction algorithm described in Section 1.2.2 is used.

Despite the FPA area of the integrated arrays is quite small (typ. around $1mm^2$) Fig. 5.26 shows a composition of few single shots from DPS52 pixel array to obtain a larger image (about 7.040mm length) of an encapsulated chip, where pads inside packaging and even internal wire-bonds (typ. $25\mu m$ in diameter) are visible. Some other qualitative example single small equalized images are supplied in the same figure. As easily noticed in the provided images, one pixel presents a non-working behavior probably due to a defective bump bonding connection, since it does not block in practice the daisy chain communications scheme of Fig. 2.1. Moreover, this non-operable active pixel does not affect the neighboring pixels thanks to the low crosstalk architecture proposal at imager level.

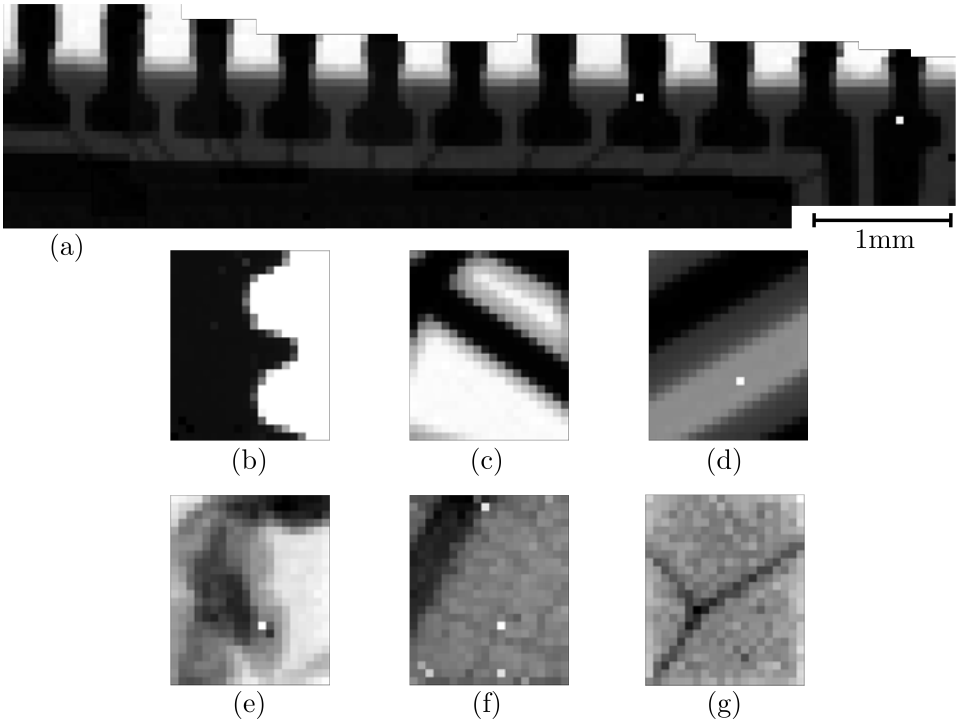


Figure 5.26 Experimental composition of several single equalized shots to obtain an equivalent larger area image of an encapsulated chip (a), and small single images of the profile of a small screw (b), metal wires covered with plastic (c), small region of a flat cable (d), part of an ant (e), a low contrast leaf (f) where the stem can be distinguished, and a bug wing (g) where considerably small and low contrast veins can be distinguished. For all cases, T_{acq}=400ms.

Finally, the test setup of Fig. 5.2 has also been mounted in ALBA synchrotron facility [106]. Taking advantage of the microfocus capabilities of this infrastructure, a 15μm×15μm monochromatic beam of 10keV X-ray photons is pointed to the DPS52 pixel array. Fig. 5.27 shows a section of the captured images, at room temperature and without any calibration, for four XY positions of this X-ray beam. For all these experiments, the initial beam intensity was attenuated using 0.35mm-thick Al film.

As appreciated in the figure, no crosstalk is observed. Moreover, these measurements confirm that the proposed DPS is suitable for high photon fluxes applications, since the DPS response is not saturated despite synchrotron beam intensity is much higher (typ. 30 times) than the X-ray tube used in previous experiments.

No radiation hardening of the CMOS ROIC designs has been observed neither during X-ray tube experiments nor during synchrotron measurements.

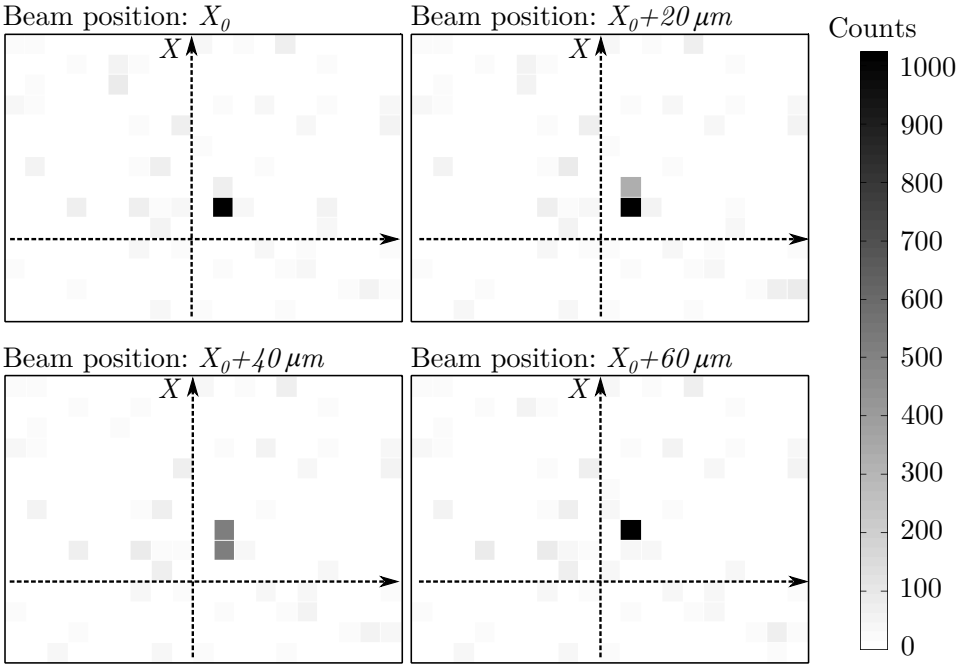


Figure 5.27 Experimental images captured from DPS52 pixel array with 50μm-pitch, by moving a 15μm×15μm focused X-ray beam through X axis direction in 20μm steps. For all cases, T_{acq}=17ms and q_{dac}=2047.

All the above results have been obtained with the developed ROICs hybridized to a 300μm-thick Si detectors. One of the advantages of hybrid technologies is that different detector materials can be used with the same CMOS read-out chip. Since CdTe detectors offer higher absorption efficiency compared with their Si counterparts, as explained in Section 1.2.3,

the use of this material allows a reduction either of the acquisition time or the X-ray tube intensity, but still maintaining the performance of the ROIC as the latter can operate at event frequencies much higher than the observed in the presented tests. This condition can be critical in certain applications where low radiation doses are required, such as in X-ray medical imaging. On the other hand, the biphasic current sensing capability of the proposed DPS designs also allows the use of CdTe detectors, which work collecting electrons as explained in Section 2.1. A similar analysis can be made when considering different X-ray tubes. Pixel linearity at high radiation doses assures good performance in applications requiring high energy photon radiation. In those cases, where each photon generates more charge in the direct conversion detector, the charge integrating nature and the lossless read-out method prevent charge losses and pile-up effects of photon-counting.

5.5 Comparison with State-of-the-Art X-Ray Pixels

In order to evaluate the results of the proposed pixel architecture and CMOS circuits, Table 1.3 summarizes the comparison of DPS52 generation respect to the state-of-the-art X-ray pixels introduced in Section 1.3. However, comparing the proposed designs with the state-of-the-art is not an easy essay.

First, since hybrid technologies allow the use of several detector technologies, ROICs can only be compared when hybridized to identical detectors and under the same radiation sources. Moreover, the small size of the integrated arrays in this work does not allow to perform the standard experiments usually reported in literature.

Second, pixel read-out method also imposes limitations in state-of-the-art comparisons. On one hand, charge integrating pixels usually do not include much functionality, generally providing analog output and thus achieving smaller pitches but at the cost of system performance. The proposed CMOS DPS, in addition to offering full functionality, digital output and programmability, it presents a competitive pixel pitch. Furthermore, the proposed pixel circuits include a novel lossless ADC scheme that keeps lin-

Chip [**Ref**]	This work	Park [63]	PAD [64]	XPAD3 [49]	PSIpix [53]	Medipix2 [58]
CMOS technology	0.18μm UMC	0.6μm CSM	1.2μm HP	0.25μm IBM	0.25μm UMC	0.25μm IBM
Pixel pitch	55μm	35μm	150μm	130μm	75μm	55μm
Array size	20×24	161082	92×100	80×120	256×256	256×256
Readout method	Ch-I	Ch-I	Ch-I	Ph-C	Ph-C	Ph-C
Programmable	yes	no	no	yes	yes	yes
Readout output	Digital 10-bit	Analog	Analog	Digital 12-bit	Digital 12-bit	Digital 13-bit
Power per pixel	10μW	N.A.	N.A.	40μW	8.8μW	8μW
Noise	$2ke^-_{rms}$	N.A.	N.A.	$100e^-_{rms}$	$135e^-_{rms}$	$140e^-_{rms}$

Table 5.2 Comparison of DPS52 generation to the state-of-the-art ROIC pixels for direct X-ray imaging. Read-out methods are charge-integration (Ch-I) and photon-counting (Ph-C).

earity at high photon fluxes. On the other hand, photon counting pixels can not be directly confronted to charge integration solutions. For example, the measured noise in terms of e^-_{rms}, although appearing higher, is actually similar to their counterparts with regard to the effect on the LSB and pixel performance, as corroborated with the calculation of an SNR reaching 80% of its theoretical limit. The level of pixel functionality of the proposed pixel and the state-of-the-art photon-counting pixels is equivalent and with a comparable measured power consumption.

Finally, the target application of the X-ray imager can also introduce limitations when comparing different proposals. As already discussed, the presented work is designed for imaging applications, excluding spectroscopy, as it is based on the charge-integration readout method. This feature, together with the extended linearity supplied by the lossless integrating circuit, makes this proposal particularly suitable for applications with high photon fluxes, where photon-counting pixels experience pile-up effects. Also, this work can benefit imaging applications using low energy photons, that are either filtered or lost by photon-counting imagers due to the charge-sharing effects.

Conclusions | 6

This last chapter presents the main contributions of this work to CMOS design of low-power and compact pitch digital active pixels for hybrid and direct X-ray imagers. First, initial hypothesis are reviewed. Then, each circuit design contribution is evaluated based on its supporting experimental results. Finally, possible future research lines related with this work are proposed.

6.1 Contributions

This thesis proposes specific analog and mixed circuit techniques for the full-custom CMOS design of low-power and compact pitch digital pixel sensors targeting hybrid and direct X-ray imagers.

The research work presented here relays on two main initial hypothesis:

- X-ray pixels based on charge-integration read-out are less sensitive to charge-sharing and pile-up effects under high radiation fluxes at expense of higher noise figures.

- Read-out pixels with digital-only I/O and not sharing any analog reference nor biasing are more immune to crosstalk at the probable cost of higher area and power requirements.

Based on the above premises, circuit design research has been materialized in several generations of DPS cells (100μm, 70μm, 55μm, 52μm pitch values) using standard 0.18μm 1P6M CMOS technology. The most relevant contributions to the design of X-ray pixel circuits resulting from these investigations can be summarized as follows:

- Digital-only I/O DPS architecture proposal compatible with compact area ($< 55\mu$m-pitch) and low-power operation ($< 10\mu$W/pix).
- In-pixel charge-lossless ADC topology specifically optimized for high radiation fluxes, performing ENC$< 2ke^-_{rms}$ and extending dynamic range full-scale above 10nA. This novel topology, together with the previous feature, improves the classic charge-integration schemes.
- On-the-fly and individual pixel gain digital tuning mechanism to compensate for DPS FPN with over 1 decade of programmability and long integration times (up to 1000ms.)
- In-pixel dark current cancellation circuits with auto-calibration and more than 3 decades of dynamic range.
- Direct pixel input test method for ROIC screening at wafer level before expensive hybrid packaging and also for in-field testing.
- Pixel built-in local analog reference and bias generator, with $< 15\%$ technology deviations and first-order thermal compensation, in order to build crosstalk-free DPS arrays.

Apart from the corresponding DPS CMOS test chips, Si direct conversion detectors have been designed and fabricated in-house for their hybridization with test ROICs in order to validate the proposed circuits both at electrical and radiation levels. In this sense, an FPGA based lab setup and associated software have been also developed.

Extensive analysis of both electrical and X-ray measurements aligns this work proposal not only within but also beyond the state-of-the-art active pixels in terms of spatial resolution, power consumption, linearity, SNR and pixel flexibility. This last point make the proposed pixel circuits suitable for a wide range of X-ray image applications.

Results obtained during the development of this work have been published in several international conferences and journals [107–112].

6.2 Future Work

As stated in Section 4.3, the proposed X-ray pixel CMOS circuit techniques are oriented to its use in truly 2D modular imagers in order to seamlessly cover large image areas.

For this purpose, the proposed pixel will be used in further works such as the NEUtron detector and imaging System (NEUS) project (IPT-2012-0662-420000), which aims two different objectives: to develop a neutron detector, obtained from Si X-ray detectors with conversion layers based on Boron deposition; and to proof the validity of the 2D modular ROIC approach to obtain large seamless sensing areas.

The development of these ROIC modules and detector designs discussed in Section 4.3 is currently ongoing. In particular, each 5mm×5mm ROIC module will consist on a 94×94-pixel array surrounded by dummy pixels devoted to ROIC interconnection and external accessibility. The ROIC sensing array will be in turn configured in 32 channels following the same daisy-chain imager architecture as this thesis. From the X-ray detector viewpoint, designs are being developed at wafer level to include several ROIC mosaic configurations (e.g. 3×3, 2×2), together with 1×1 arrangements with different number of serialized channels.

Hence, the contributions of the present work are being applied for future X-ray imagers.

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