Universitat Autònoma de Barcelona

A novel Depleted Monolithic Active Pixel Sensor for future High Energy Physics Detectors

Sonia Fernandez-Perez

Universitat Autònoma de Barcelona
Departament de Física

Institut de Física d'Altes Energies

A novel Depleted Monolithic Active Pixel Sensor for future High Energy Physics Detectors

Sonia Fernandez-Perez

PhD Thesis

April 2016

Supervised by:

Dr. Cristobal Padilla

Institut de Física d' Altes Energies
Edifici Cn E-08193 Bellaterra (Barcelona)

Tutored by:

Dr. Enrique Fernández

Universitat Autònoma de Barcelona (UAB)/ IFAE
Edifici Cn E-08193 Bellaterra (Barcelona)

Universitat Autònoma de Barcelona
Departament de Física

Institut de Física d'Altes Energies

A novel Depleted Monolithic Active Pixel Sensor for future High Energy Physics Detectors

Sonia Fernandez-Perez

PhD Thesis

April 2016

Supervised by:

Dr. Cristobal Padilla

Institut de Física d' Altes Energies
Edifici Cn E-08193 Bellaterra (Barcelona)

Tutored by:

Dr. Enrique Fernández

Universitat Autònoma de Barcelona (UAB)/ IFAE
Edifici Cn E-08193 Bellaterra (Barcelona)

Contents

Introduction

The Standard Model of particle physics provides the best knowledge of the ultimate constituents of matter and their nature. However, the Standard Model provides no explanation for a number of fundamental observations. Examples of these are the gravitational interactions, the dark matter observed in galaxy studies or the matter and anti-matter asymmetry observed in the universe. Giant particle accelerators all over the world try to find answers to these fundamental questions. The LHC (Large Hadron Collider) located at CERN (Conseil Européen pour la Recherche Nucléaire) is the most powerful of them built to date. The LHC, operative since 2009, has four main experiments distributed around its ring. They are: CMS (Compact Muon Spectrometer), ATLAS (A Toroidal LHC ApparatuS), LHCb (Large Hadron Collider beauty), and ALICE (A Large Ion Collider Experiment). In 2012, after fifty years of searching, the existence of the Higgs Boson was experimentally confirmed by the ATLAS and CMS experiments.

The upgrade of the LHC with the aim to extend its physics programme and to exploit all its possibilities is one of the highest priorities for the European Strategy for Particle Physics. The LHC expects to operate from 2026 to 2035 with an instantaneous luminosity of $7 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which corresponds to a seven times increase with respect to the design value. This will allow precision measurements for the 125 GeV Higgs boson, the study of rare Standard Model processes, and searches for phenomena beyond the Standard Model. A major upgrade of the LHC machine and its detectors, called HL-LHC (High Luminosity LHC) is foreseen to achieve successful operation in such conditions. The HL-LHC upgrade opens a big technological challenge to the LHC machine itself as well as to the detectors, in particular to the systems closest to the interaction point.

The ATLAS experiment is a proton-proton experiment at the LHC investigating a large variety of particle physics at the TeV energy scale, with the main focus on the electro-weak symmetry breaking mechanism, and physics beyond the Standard Model. The ATLAS Collaboration consists of more than 3000 scientists from 174 institutes in 38 countries. The ATLAS detector layout, composed of symmetrical and concentric sub-detectors, was designed to cover the maximum possible solid angle around the interaction point. The ATLAS detector is composed of a tracking detector immersed into a magnetic field to measure the particles position and momenta, two calorimeters to measure the particle and jet energies, and an spectrometer to detect muons. The current ATLAS tracking detector is composed of gas and solid state silicon detectors. It contains a dedicated vertex detector called Pixel Detector, which consists of four layers of segmented pixel silicon detectors. The Pixel Detector, located closest to the proton-proton collision point, has the most stringent requirements of all sub-detector systems. Due

to the high particle rate it must perform under high radiation levels and at the same time minimize the material budget. The present detector concepts constituting the vertex detector are hybrid modules developed at the cutting edge of the technology. The requirements imposed to the tracking detectors for the HL-LHC are at least one order of magnitude more stringent with respect to LHC in terms of radiation hardness, and number of particle traversing the detector per second and square centimetre. Thus, the HL-LHC ATLAS upgrade is a technological challenge, and it involves an extensive R&D effort. The ATLAS detector plans to install a new all silicon tracker for the HL-LHC upgrade. The final layout is under discussion, and the detector technology to be installed is not decided yet.

This is definitely one of those very exciting periods in which technology development is being pushed by the needs in the High Energy Physics community. These periods have been happening since the construction of LEP (Large Electron Positron collider) and LHC leading to the discovery of new technology which afterwards was changing once and forever the world, as the creation of the WWW (World Wide Web), or the utilization of the developed accelerator and sensor technology for tumour treatments.

The current hybrid pixel concepts used at the moment in ATLAS are unrivalled in terms of rate and radiation tolerance positioning them as a good candidate for HL-LHC. However, their material budget, production complexity, and their cost have boosted the development of the new detector concepts. The interest of CMOS-based pixel sensors have emerged due to their potential low cost in comparison with standard hybrid pixels and to the large area that must be covered in the outer layers. CMOS-based sensors use an industrial production process with a large throughput, a stringent quality assurance, and they are relatively cheap. They allow small pixel size fabrication, which improves the spatial resolution and the detection of two very near tracks. The possibility to produce smaller thickness of the sensor would also be beneficial for particle identification. Since several years an international community called the ATLAS CMOS Pixel Collaboration is seeking for new radiation-hard pixel sensor concepts, both hybrid and monolithic, based on industrial CMOS processes for HL-LHC. The work presented in this thesis is done within the framework of this collaboration.

A novel and promising concept of a depleted monolithic active pixel sensor built on silicon-on-insulator within a high voltage process has been fully characterized to evaluate its performance for the future ATLAS HL-LHC upgrade in this thesis. This promising sensor concept would reduce the material budget, pixel size, and cost with respect to hybrid approaches. The silicon dioxide layer used to separate the charge collecting diode from the electronics would reduce the coupling capacitance between charge collecting electrode and readout electronics with respect to other monolithic sensors. Additionally, the accomplishment of the HL-LHC requirements by a monolithic detector would lead to a new era of the high energy physics detectors, with a significant cost advantage and simpler detector assembly.

An overview of the LHC, the HL-LHC and its particle physics environment is given in chapter 1. Subsequently, the ATLAS detector layout, and its upgrade towards HL-LHC is de-

scribed. The requirements and challenges of the tracking detectors are emphasized in chapter 1. The interaction of particles with matter is described in chapter 2 in order to introduce the operation of solid state detectors. The chapter proceeds with the building block of solid state detectors for particle tracking from a semiconductor to a pixel detector. The chapter closes with a description of the main features and requirements for the design of vertexing and tracking detectors. The effect of radiation damage on silicon detectors is extensively explained in chapter 3. This chapter covers the radiation effects suffered at the silicon surface, mainly at the electronics, and the radiation effects suffered in the silicon bulk. An overview on the current development and trend of pixel detectors, where hybrids, high voltage and high resistivity CMOS, and depleted monolithic active pixel sensors are covered, is given in chapter 4. This chapter also describes in detail the monolithic prototype under study on this thesis.
A validation programme was defined and executed to evaluate the technology. The following chapters describe and discuss the performed measurements, and their results. Chapter 5 describes the radiation hardness characterization of the transistors to ionizing radiation. Total Ionizing Dose effects, Back Gate Effect, and the influence of the radiation induced charges in the silicon dioxide layer on the sensor are discussed. Chapter 6 describes the characterization of the charge collection properties at the diode. Different experimental techniques were used to extract the depletion depth and the electrical field shape on unirradiated and irradiated samples. The leakage current, the charge collected by diffusion and by drift, and hints to the Acceptor Removal effect are measured and discussed. The monolithic prototype under study in this thesis was also characterized in a pion beam test, which is described in chapter 7. The measured charge collection, charge sharing, spatial resolution, and tracking efficiency of the prototype are also explained in this chapter.

This work concludes with an extensive summary, providing an outlook towards the future of depleted monolithic active pixel sensors on silicon-on-insulator technology for high energy physics.

Chapter 1

The Large Hadron Collider and the ATLAS experiment

The Large Hadron Collider (LHC) is the largest and most powerful particle accelerator in the world. Scientists at the LHC aim to study of the ultimate constituents of matter and the nature of their interactions. The LHC, which is taking data since 2009, has four main experiments distributed around its ring where the result of the proton-proton and ion-proton collisions are studied. The Standard Model of particle physics, despite its successes coming from confirmed predictions is known to be incomplete. The LHC plans to enlarge its physics programme in the next decades by carrying out a major machine and detectors upgrade called High Luminosity LHC (HL-LHC), scheduled for 2024-2026. The upgrades to the detectors imply an enormous technological challenge, specially for the sub-detectors closest to the interaction point. All this is set into context in this chapter.

The chapter starts with a description of the physics context nowadays. The LHC accelerator, the HL-LHC upgrade, and the physics programme for 2024-2035 is introduced in section 1.2. Section 1.3 describes in detail the present layout of the A Toroidal LHC ApparatuS (ATLAS) detector as well as its scheduled upgrades towards HL-LHC. The chapter closes with an introspection on the requirements and technological challenges to optimize a tracking detector under such an environment as the HL-LHC.

1.1 Physics environment

The Standard Model [1] of particle physics is a quantum field theory describing all elementary particles and their interactions. The elementary particles are divided into three main categories: 6 quarks, 6 leptons and 5 bosons (4 force carriers and the Higgs boson) as is shown in figure 1.1 [2]. Leptons are particles with spin $1/2$ and -1,0,1 electrical charge, which appear as free particles. Quarks, with spin $1/2$ and a fractional electrical charge, are confined in groups of particles called Hadrons. Additionally, quarks carry colour. Leptons and quarks are subdivided into three generations with a notable mass hierarchy. The origin and nature of the mass hierarchy is not explained by the Standard Model. The lightest and most stable particles make up the first generation. All the stable matter in our universe belong to the first generation. Particles from the second and third generation are produced in high energy processes, which

shortly decay into first generation particles. The four force carriers mediate the interaction between the fundamental particles.

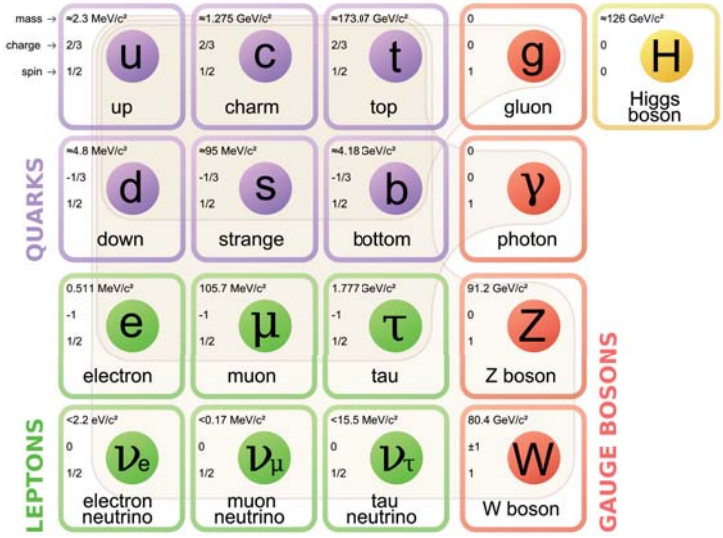


Figure 1.1: Elementary particles in the Standard Model of particle physics [2].

The Standard Model describes three of the four fundamental forces in nature: electromagnetic, weak, and strong force. The electromagnetic force underpins all of chemistry. It acts between all charged particles, and it is mediated by a charge-less photon with spin 1. This mediator couples only to charged particles and will not interact with neutral particles such as itself. Since the photon is massless its interaction range is infinite. The weak force is responsible for the beta decays. It acts between all fermions and it is mediated by three bosons, the charged $W^{\pm}$ bosons and the neutral Z boson. These bosons are massive, $W^{\pm} = (80.403 \pm 0.029)\,\text{GeV}$, $Z = (91.1876 \pm 0.0021)\,\text{GeV}$ [3, 4, 5, 6], and as a consequence the range of the weak interaction is short. The strong force is responsible for the confinement of quarks in hadrons and also for nuclear interactions. It is mediated by massless, coloured gluons (g) of spin 1. The electromagnetic and the weak force are unified into the electroweak force which builds the electroweak symmetry. However, the fact that the $W^{\pm}$ and Z were experimentally measured to be so massive while the photon is massless means that the electroweak symmetry is broken. The mechanism to spontaneously break the electroweak symmetry, which generate the masses of the $W^{\pm}$ and the Z boson, is called Higgs-mechanism [7, 8, 9, 10, 11], and it was proposed by Robert Brout, Francois Englert, Peter Higgs, Gerald Guralnik, C. R Hagen and Tom Kibble in 1964. The masses of the other particles are generated through the Yukawa interactions with the Higgs scale field [11]. The existence of the Higgs field results in at least one mass spin 0 boson referred to as the Higgs boson. Thus, the Higgs mechanism was postulated to explain the electroweak symmetry breaking, and its hunting has been the highlight of High Energy Physics (HEP) experiments all over the world. The Higgs Boson was discovered at the Conseil Européen pour la Recherche Nucléaire (CERN) in 2012 [12, 13]. On 2013 Francois Englert,

and Peter Higgs were awarded with the Nobel Prize for their work on the spontaneous symmetry breaking mechanism.

The Standard Model is an extremely successful theory, whose predictions have been rigorously tested by a variety of experiments over many decades. Despite its successes, the Standard Model is known to be incomplete. It does not include gravitational interactions, lacks an explanation for dark matter and dark energy, has no mechanism to generate neutrino masses, and cannot describe the matter/anti-matter asymmetry observed in the universe. Thus, there are several theoretical models, not supported by any experimental evidence yet, that go beyond the Standard Model and try to answer some or all of these questions. These are the subject of searches at the LHC for the next decade.

1.2 The Large Hadron Collider

The LHC [14] is a 27 km circular proton-proton collider located at CERN at around 100 m underground astride the Franco-Swiss border close to Geneva. The LHC was designed as proton-proton collider mainly due to two reasons. First, hadron collisions provide the possibility to probe a wide range of energies simultaneously and this makes hadron collisions a well suited tool to search for new particles with unpredicted masses. Second, in comparison to electrons, the loss of energy due to the synchrotron radiation is much smaller as is described in section 2.1. This allows to achieve higher collision energies.

The LHC provides four interaction points where its four experiments are located as figure 1.2 shows. They are named: Large Hadron Collider beauty (LHCb), A Large Ion Collider Experiment (ALICE), ATLAS and Compact Muon Spectrometer (CMS). LHCb is primarily designed to investigate the b-quark physics and therefore provide an insight into the CP-violation phenomenon while ALICE is dedicated to research in heavy-ion physics and quark gluon plasma formation [15]. ATLAS and CMS are two general purpose experiments, mainly investigating the proton-proton collisions to study the electroweak symmetry breaking mechanism and new physics beyond the Standard Model (SM) like, for example, SUperSYmmetry (SUSY) [16] or extra dimensions.

The luminosity (L) is the measure of the ability of a particle accelerator to produce a given number of interactions. The luminosity of a circular collider is given by the amount of particles traversing the interaction point in the detector per area and time:

$$L = \frac{n_b \cdot N_1 \cdot N_2 \cdot f}{A} \tag{1.1}$$

where n_b denotes the number of bunches per beam in the accelerator, N_i the number of particles in the bunches of the two beams, f the collision frequency of the bunches and A the cross sectional area.

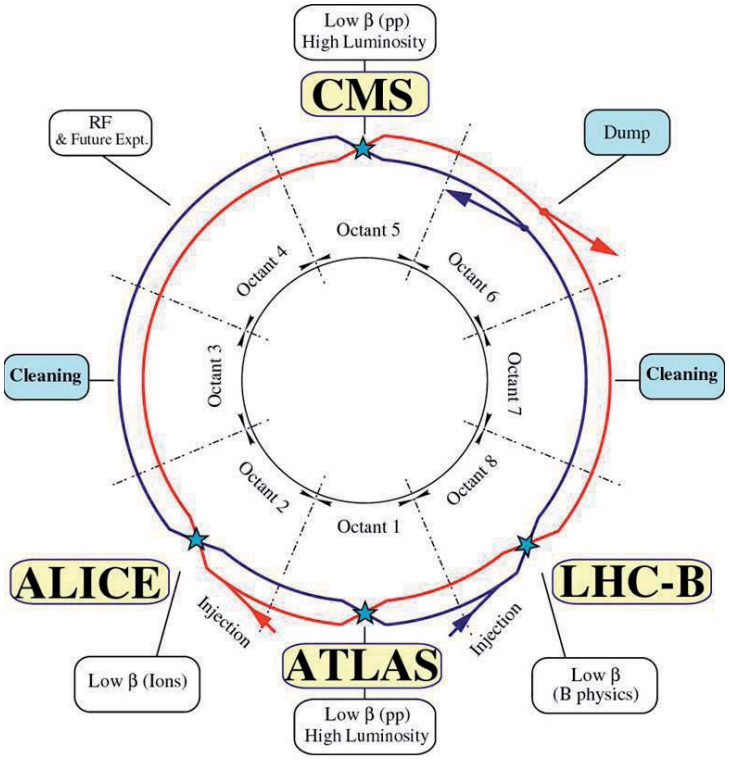


Figure 1.2: LHC collider and its four experiments location scheme [17].

The event rate ($\dot{N}_{event}$) describes the frequency to obtain an specific event. It is derived from the luminosity and the cross section of the examined event (σ_{event}) as:

$$\dot{N}_{event} = L \cdot \sigma_{event} \tag{1.2}$$

The cross section of the proton-proton collisions is about 10^{11} pb, the cross section of the well measured electroweak processes (e.g. W/Z) is about 10^4 pb, whereas the cross section of Higgs production is about 100 pb. This is shown in figure 1.3, which depicts experimental and theoretical cross sections for several SM processes. Thus, in order to increase $\dot{N}_{event}$ and provide enough statistics to measure unexplored physics processes, a high luminosity is required.

The high luminosity of LHC results in a number of proton-proton collisions per bunch crossing (currently in the order of 25). The collisions which do not originate from a hard scattering interaction among the proton constituents are called pile-up (μ). Pile-up degrades the physics object reconstruction by increasing the detector occupancy and creating ambiguities in the sources of deposited energy. To avoid that, the detectors must cope with the expected pile-up and must be able to resolve the simultaneous collisions separately.

The LHC was constructed between 2001-2007, using the former Large Electron Positron collider (LEP) [19] tunnel. The LHC was designed with a center of mass energy of 14 TeV, a luminosity of 10^{34} cm^{-2}s^{-1}, a dipole field of 8.33 T, and a beam size of 16 µm at the interaction

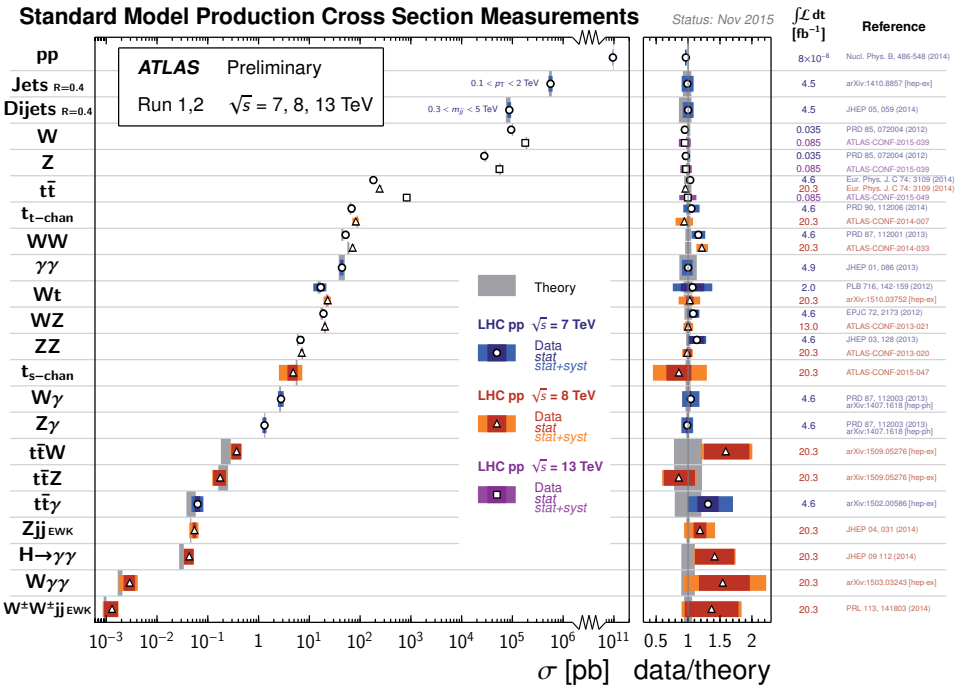


Figure 1.3: Summary of several Standard Model total production cross section measurements compared to the corresponding theoretical expectations [18].

point [20]. At the design luminosity, 2808 bunches per beam, consisting of 1.15×10^{11} protons each collide with a frequency of 25 ns. The LHC is operative for intervals of data-taking periods since 2009. During the first data-taking period (2009-2012), so called Run 1, the LHC operated at a luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, a collision energy of 8 TeV, and with 50 ns bunch crosses. The observed pile-up for the proton-proton experiments was μ=23. On August 2012, the ATLAS and CMS experiments made public the discovery of the Higgs Boson based on an integrated luminosity of $30\,\mathrm{fb}^{-1}$ collected data during Run 1.

1.2.1 The HL-LHC upgrade

The discovery of the new particle has boosted the interest of extending the physics programme at the LHC and to exploit all its possibilities. To extend the physics programme, a major upgrade of the LHC machine, so-called HL-LHC [21, 22], was approved. The HL-LHC upgrade, scheduled for 2024-2026, expects to operate with a nominal instantaneous luminosity $L = 7 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ corresponding to an expected pile-up of μ=200 [23], which is around ten times larger than the current pile-up. This programme aims to deliver a total integrated luminosity of $3000\,\mathrm{fb}^{-1}$ [23].

The upgrades toward the HL-LHC will happen gradually in several phases during the next ten years. During those phases the LHC machine but also the LHC experiments are planning various upgrades to their detector, trigger, and data acquisition systems in synchronization

with the LHC upgrades. The ten year upgrade schedule to achieve the HL-LHC is shown in figure 1.4 [23] where the blue boxes indicate the upgrades periods. The expected data delivered by LHC at the end of each run is summarized on the blue boxes. There are three upgrade phases known as Phase-0, Phase-1, Phase-2 taking place during the three long shutdowns LS1, LS2 and LS3. The data taking periods in between the upgrades are know as Run 1, Run 2, Run 3 and Run 4.

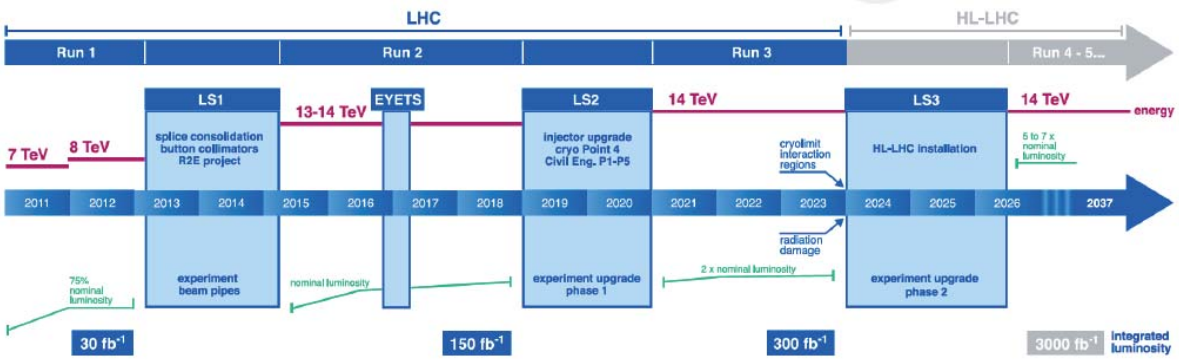


Figure 1.4: Ten years LHC roadmap towards HL-LHC. Run 1 to Run 5 indicate the data taking periods and the shut down periods are indicated as LS1 to LS3 [23].

LS1 - Phase 0

During 2013-2014 the first long shutdown so-called LS1 or Phase 0 took place. During Phase 0 the LHC machine was updated to go to the design collision energy of 14 TeV, to the nominal luminosity of 10^{34} cm^{-2}s^{-1}, and to a bunch spacing of 25 ns instead of the 50 ns bunch crossing performance during Run 1.
During LS1 all the magnet interconnections were consolidated to allow nominal current in the dipole and lattice quadrupole circuits of the LHC. In addition, other repairs, consolidation and cabling across the whole accelerator complex to bring all the equipment to the level needed for 7 TeV per beam were performed [24]. On May 2015, the LHC was turned on, and the Run 2 period started. The Run 2 started initially with 6.5 TeV per beam and will approach to 7 TeV per beam according to the magnet training progresses. First proton-proton collisions for data-taking are expected in April 2016. The expected data delivery during the following Run 2 is about 150 fb^{-1}.

LS2 - Phase I

The LS2 is foreseen in 2019-2020. During LS2, an exhaustive list of implementations will take place, of which only the main ones are listed here: the injectors of the LHC pre-accelerators (PS-Booster, PS) [24] will be upgraded in order to increase the injection energy. In addition, a new Radio Frequency cavity system is foreseen for the PS-Booster as well as a new main power converter [24]. A new Radio Frequency beam manipulation scheme will be implemented in PS

to increase the beam brightness. The goal is to double the luminosity up to $2 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ beyond the design value, and deliver about $300\,\mathrm{fb^{-1}}$ of data during Run 3 [21].

LS3 - Phase II

The LS3 is foreseen in 2024-2026. New IR-quadrupoles and new 11 T dipoles will be installed. Upgrades to the collimator, cryogenics and crab cavities will be needed, as well as cold powering, machine protection and many other system changes. The technology needed for the upgrades is not in the market, but in continuous development by R&D collaborations. The main goal is to reach a peak luminosity of $5\text{-}7 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ and deliver about $3000\,\mathrm{fb^{-1}}$ achieving then the HL-LHC goal [23].

1.3 The ATLAS experiment

The collaboration of the ATLAS experiment consists of more than 3000 scientists from 174 institutes in 38 countries. The ATLAS physics programme [25] covers most of the physics potential discoveries at LHC such as measuring the Higgs properties and the search for new physics beyond the SM, specially SUSY and extra dimensions. The physics programme is the benchmark for setting the detector layout, its requirements, and optimization. For example, to explore the full range of possible Higgs boson masses, high-resolution measurements of electrons, photons, and muons, an excellent vertex detection and high-resolution calorimetry for jets and missing transverse energy are required, which determines the size, weight and material types of the detector. The ATLAS detector plans to extend its physics programme at the HL-LHC, and thus requires a major upgrade of its sub-detector systems.

This section describes the impact of physics measurements on the detector requirements, the current ATLAS detector layout, and the planned upgrades of the ATLAS detector towards the HL-LHC.

1.3.1 Physics programme for HL-LHC

The physics programme of ATLAS for the HL-LHC focusses on precision measurements for the 125 GeV Higgs boson in many of its production and decay modes, as well as improved measurements of all relevant Standard Model processes and parameters including the study of rare Standard Model processes, and searches for phenomena beyond the Standard Model [23].

One of the key measurements of ATLAS at the HL-LHC is the identification of b-quarks, called b-tagging. On the one side, b-quarks are important to identify t-quark production, the most massive fundamental particle. On the other side, the $H \rightarrow bb$ channel has the largest branching fraction of Higgs decay (58%) [26], and it is possible for new physics to modify the branching ratio of $H \rightarrow bb$ [26]. However, this channel was not precisely measured yet due to the large statistic uncertainties after the background suppression. The increase of luminosity will increase the statistics of this channel at high transverse momentum. In addition, b-quark

identification allows many studies in flavour physics like CP-violation [27], which can also probe for new physics.

A majority of the b decays produce an hadronic shower [28]. Thus these b-quark decays are measured as a jet in the ATLAS detector. With the peculiarity of relatively long lifetimes, b-quarks travel a measurable distance before decaying. Thus, in order to identify b-quark jets two main steps are needed: first the rejection of pile-up jets, and second the reconstruction of the secondary vertex. The current technique used in ATLAS to tag and suppress pile-up jets using the tracking information is called R_{pT} [23]. R_{pT} is defined as the scalar transverse momentum (p_T) sum of the tracks that are associated with the jet and originate from the hard-scatter vertex, also called primary vertex, divided by the fully calibrated jet [23]:

$$R_{pT} = \frac{\sum p_T^{track,i}}{p_T^{jet}} \tag{1.3}$$

A simulation of the R_{pT} distribution for hard-scatter (solid line) and pile-up jets (dashed line) with $40 < p_T < 50$ GeV is shown in figure 1.5 [23] for different η regions. A cut allows selecting the hard-scatter jets. The R_{pT} method to reject pile-up jets relies on good separation between hard-scatter jets and pile-up jets, namely good tracking. The secondary vertex reconstruction relies on the good tracking and vertex resolution of the detector. The calculation of the vertex resolution of a detector system requires a profound understanding of the interaction of the particles with the detector material and of the detector properties. Therefore it is given in section 2.3.

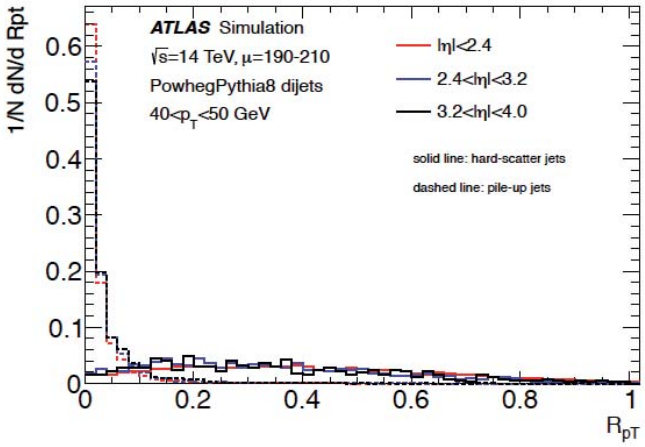


Figure 1.5: R_{pT} distribution for hard-scatter and pile-up jets with $40 < p_T < 50$ GeV in different η regions [23].

The success and precision of any of the physic analyses depend strongly on the performance of the sub-detectors systems, as just described on the example of b-tagging. Thus, the physics

programme provides the benchmarks for the detector layout including its requirements, and optimization.

1.3.2 Detector layout

The ATLAS Detector [29] is about 45 m long, 25 m high and weights approximately 7000 t. This corresponds to about half the dimensions of the Notre Dame Cathedral and weights the same as the Eiffel Tower. The detector consists of several specialized sub-detectors, cylindrical and concentric around the interaction point.

The detector layout and the coordinate system is shown in figure 1.6 whose origin is defined by the interaction point. The z axis is given by the beam direction, being the xy plane transversal to the beam direction. The positive x axis points to the center of the LHC ring. Another important coordinate used in any detector of hadronic collisions is the pseudorapidity. The pseudorapidity (η) is a space transformation of the beam angle (θ), defined as:

$$\eta = -ln\ tan(\frac{\theta}{2}) \tag{1.4}$$

The particle production is a constant distribution as a function of the rapidity. This facilitates the reconstruction and comparison of results with other detectors.

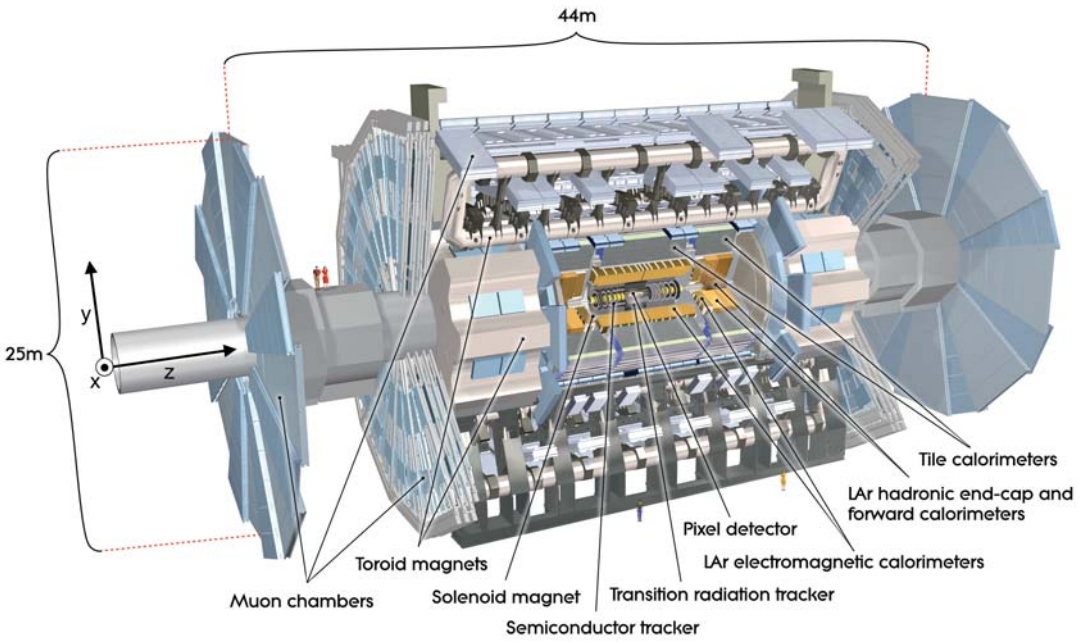


Figure 1.6: ATLAS Detector layout and its coordinate system [17]. The main sub-detectors: Inner Detector, Electromagnetic Calorimeter, Hadron Calorimeter, and Muon Spectrometer are indicated.

The ATLAS detector is designed for high transverse momentum measurements and a large acceptance in pseudorapidity in the sub-detectors. The main components of the ATLAS detector from inner to outer part are: Inner Detector, Electromagnetic Calorimeter, Hadron Calorimeter, and Muon Spectrometer. The Inner Detector, described in detail in section 1.3.3, allows precision measurement of charged particles trajectories. It is embedded within a solenoid magnetic field of 2 T responsible of bending the charged particles trajectories in the transverse plane in order to allow the measurement of the transverse momentum of the tracks. The calorimeter systems are placed just outside the solenoid. They measure the energies carried by the particles. The Electromagnetic Calorimeter is designed to measures the energy of electrons and photons i.e. electromagnetic interactions, while the Hadron Calorimeter is designed to measure the energy of hadrons and jets. Finally, the Muon Spectrometer measures the momenta of muons which were not stopped in the calorimeter systems. The momenta of the unabsorbed muons is measured using the Magnet System mentioned above, which comprises a thin superconducting solenoid surrounding the Inner Detector cavity, and three superconducting toroids (one barrel and two end-caps) around the calorimeters.

Trigger and Data Acquisition

The bunch crossing rate at the LHC is approximately 40 MHz. The available technology and resources limit the data recording to about several hundred Hz. As a consequence, not all event data produced from the interactions can be recorded, but only a selection of them.

The online selection of the events containing potentially interesting physics is the aim of the complex trigger system. The Data AcQuisition (DAQ) system is responsible of recording the data and building the events. The Trigger and Data AcQuisition (TDAQ) systems [30] are partitioned into sub-systems, associated with sub-detectors. The Trigger System has three distinct levels: Level 1 (L1), Level 2 (L2), and the Event Filter, each of them refines decisions made at the previous level.
The L1 trigger selects high transverse-momentum muons, electrons, photons and jets, as well as large missing transverse energy, which is a place where new physics is expected. The L1 defines Regions-of-Interest (ROIs) which is a storage of the detector parameters where its selection process has identified interesting features. The trigger rate is reduced from 40 MHz to 100 kHz [30].
The L2 selection uses, at full granularity and precision, all available data within the ROIs from the L1 trigger. L2 is designed to reduce the trigger rate from 100 kHz to 3 kHz [30]. After the L2, the events are built and the Event Filter reduces the trigger rate to approximately 200 Hz [30]. The events selected by the Event Filter are moved to the permanent storage at the CERN computer centre. The provided trigger numbers corresponds to design values of the detector.

1.3.3 The ATLAS Inner Detector

The Inner Detector is the innermost sub-detector of ATLAS and thus is the one undergone to the harshest conditions. It plays a fundamental role in the identification and reconstruction of

electrons, photons, muons, tau leptons, as well as, in tagging b-jets and in fully reconstructing certain hadronic decays [31].

The Inner Detector is composed of three sub-detectors, which from outer to inner are: the Transition Radiation Tracker (TRT), the Semiconductor Tracker (SCT), and the Pixel Detector. Each of those sub-detectors is composed of barrels on the beam direction and end-caps perpendicular to the beam direction for the high η region. Figure 1.7 [32] shows the Inner Detector cross section where its main sub-detectors and their distances to the beam are highlighted.
The operation principle is similar for all of them, which consists on ionizing the detector material and converting the produced electrons into an electrical signal. The TRT is a gas detector, thus the ionized material is gas. The TRT eases the pattern recognition while also contributes to electron identification. The SCT and the Pixel Detector are both semi-conductor detectors made of Silicon. The SCT detector is composed of four layers of silicon strip sensors (one dimensional segmented), which measures precisely the particle momenta in the important transverse plane. The Pixel Detector layers are composed of two dimensional segmented detectors, called silicon pixel modules, which mainly contribute to the accurate measurement of vertices.

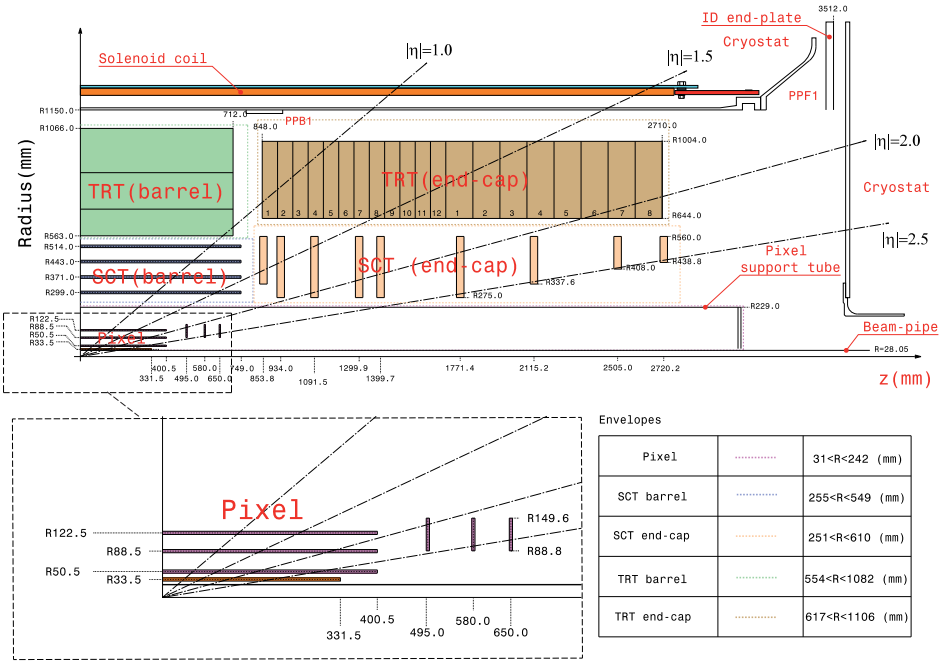


Figure 1.7: Plan view of a quarter-section of the ATLAS inner detector. The barrels and end-caps of the TRT, SCT, and Pixel Detector as well as their distances to the interaction point are shown [33].

The Pixel Detector [34] is the closest to the interaction point and it is exposed to the highest particle flux and radiation dose. The Pixel Detector is crucial for the identification and reconstruction of secondary vertices from the decay of, for example, particles containing a b-quark

or for b-tagging of jets [34]. In addition, it provides excellent spatial resolution for reconstructing primary vertices coming from the proton-proton interaction in the presence of pileup. It fulfils the harshest requirements of the entire ATLAS detector in terms of occupancy, speed, and radiation hardness.

The current Pixel Detector layout is composed of four layers as shown in figure 1.8 [35]. From the inner side to the outer side, they are called Insertable B-Layer (IBL), B-Layer, Layer-1, and Layer-2, with a nominal radius of 32.0, 50.5, 88.5 and 122.5 mm, respectively. At the bottom of figure 1.8 the radial placement of the barrel layers including the beam pipe is shown. The general performance requirements of the current pixel system are described in [34]. The IBL was inserted in 2014 during LS1.

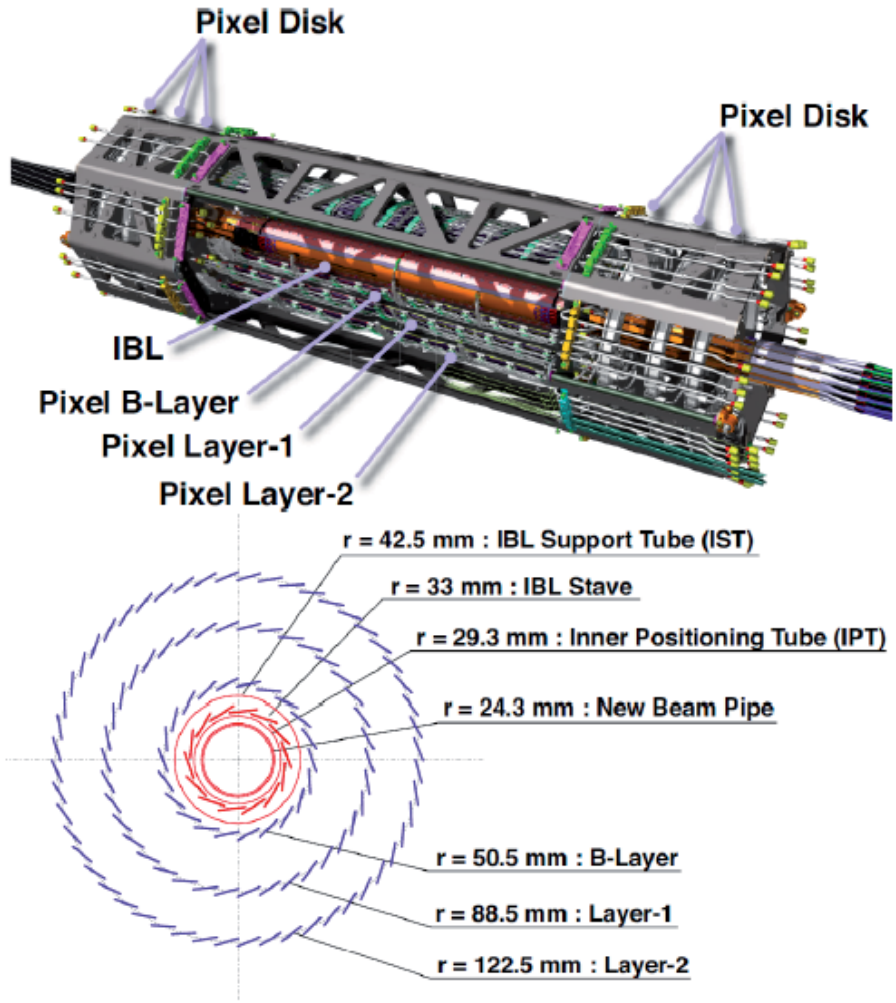


Figure 1.8: Schema of the current ATLAS 4-Layer Pixel Detector [35]. From the inner part to the outer part the layers are: IBL, B-Layer, Layer-1, and Layer-2. At the bottom, the radial placement of the barrel layers including the beam pipe is depicted.

The main motivations to include an extra layer in the ATLAS Pixel Detector were:

- Tracking robustness: failures on modules in the B-layer, and in other Pixel layers are expected to occur with time. A failure on the B-layer seriously deteriorates the impact parameter resolution, directly affecting the b-tagging performance. The IBL restores the full b-tagging efficiency even in case of a complete B-layer failure.
- Pile-up: the current Pixel Detector was designed to cope a peak luminosity of 1×10^{34} cm^{-2}s^{-1} and a pile-up of μ =23. In Run 2 the expected luminosity is twice that value and the expected pile-up is μ >50 [35] leading to high occupancy that can induce readout inefficiencies particularly in the B-layer as being closer to the interaction point.
- Tracking precision: the IBL is closer to the interaction point than the previous first layer, and therefore it will improve vertexing capability and b-tagging performance with respect to the previous years.

The insertion of the IBL has improved the impact parameter resolution of the ATLAS tracker by nearly a factor of two for low transverse momentum tracks as shown in figure 1.9 [36]. Additionally it has increased the pattern recognition robustness providing an additional point.

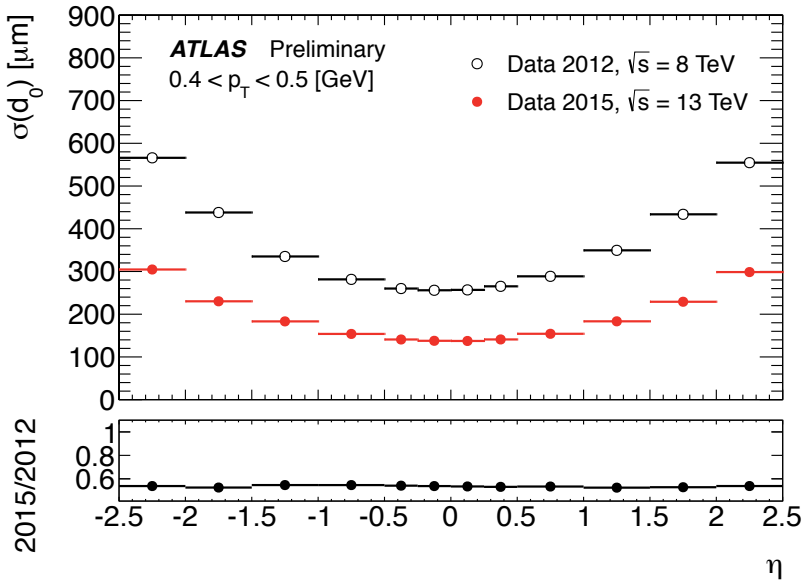


Figure 1.9: ATLAS transverse impact parameter resolution as a function of η measured from data in 2015, $\sqrt{s}$ =13 TeV, with the Inner Detector including IBL for values between $0.4 < p_T < 0.5$, compared to that measured from data in 2012, $\sqrt{s}$ =8 TeV [36].

1.3.4 Pileup performance and future expectations

The pile-up measured at ATLAS for different luminosities during Run 1 at 7 TeV centre-of-mass energy in 2011 and at 8 TeV center-of-mass energy in 2012 is shown in figure 1.10

[37]. The ATLAS detector, designed to overcome a pile-up of μ=23 [38], is close to its design limits. During Run 2 the pile-up is expected to increase to values of μ >50. This was one of the reasons to insert the IBL in the Pixel Detector as described in section 1.3.3. The presence of pile-up requires high granularity detectors and redundancy in the measurement of tracks to overcome possible fake rates arising from random combinations of clusters.

The ATLAS detector at HL-LHC must cope a pile-up of μ=200 [23]. This implies higher granularity resolution to the inner detector components in order to distinguish between the particles coming from collisions happening at the same time, higher speed to be able to record all the tracks, and higher radiation hardness to stand such conditions during several years. In addition pile-up affects the detector performance over time due to radiation. The Pixel detector being the closest to the interaction point is the most affected by the pile-up effect.

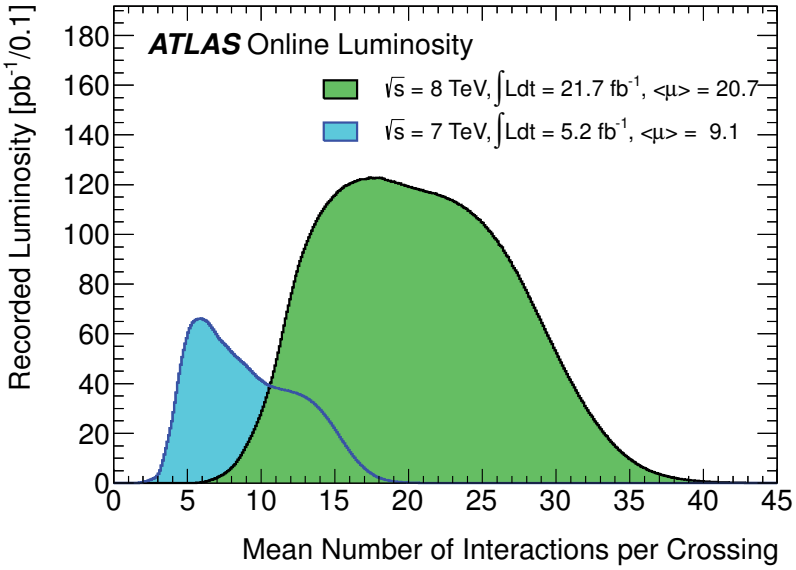


Figure 1.10: Recorded luminosity versus mean number of interactions per bunch crossing in ATLAS, for 7 TeV and 8 TeV centre-of-mass energy. The design value for the detector is of 23 interactions per bunch crossing.[17].

1.3.5 ATLAS upgrades towards HL-LHC

The HL-LHC experiments will have to face very high detector occupancies, higher pile-up, higher processing speed, and harsher radiation environment as a consequence of the huge multiplicity of particles produced per proton bunch crossing. Thus, the current experiments must be upgraded. The ATLAS experiment plans a major upgrade, which is split in three phases during the LHC long shutdowns [38, 31]. The time schedule shown in figure 1.4 is still valid here. In particular for the inner detector, forward calorimeters, and muon spectrometers the upgrades are crucial. A summary of the planned detector upgrades in each phase is described here.

Phase-0

It took place in 2013-2014 during the LS1 shutdown. The full Pixel Detector was extracted and brought to the surface for its refurbishment. A New Service Quarter Panels (nSQP) [39] was installed to replace the old one, which allowed to increase the data transmission bandwidth on layer 1 and on layer 2. Besides, the pixel extraction allowed the addition of the Diamond Beam Monitor [33, 40] consisting of eight telescopes of diamond pixel detectors for bunch to bunch luminosity measurements. In the Pixel Detector a new layer called IBL [39], was inserted between the actual B-layer and the new beam pipe, as described in section 1.3.3. Several years of R&D allowed the design, production, and commissioning of several technologies used to equip the IBL [33]. Finally two different sensor technologies (Planar and 3D silicon sensors) were included in the IBL, the last one included for the first time in any of the LHC experiments.

In addition, the present beam pipe was replaced by a new and smaller radius beam pipe, which can continue being used for the HL-LHC upgrade, unless a smaller beam pipe becomes possible by then.
Outside the Pixel Detector, a new thermoshipon cooling system was implemented for the Pixel and SCT Detectors keeping the evaporative cooling system as backup [39]. New Muon End-cap Extension chambers were inserted to improve the coverage at $1.0 < \eta < 1.3$. A specific neutron shielding was added and other detector consolidation works took place.

Phase-I

During Phase-I, the Small Muon Wheels [38] will be replaced with the New Small Wheel (NSW) which covers $1.3 < \eta < 2.7$ for forward muon spectroscopy. This will improve the tracking and trigger capabilities, and that will meet the LHC Phase-II requirements. The trigger capabilities will be improved to cope with higher rates through the High Precision Calorimeter Trigger [38] at the L1 Trigger, the Fast TracKing (FTK) [38] at the L2 Trigger, together with other Trigger and DAQ upgrades. The installation of a forward detector, the ATLAS Forward Physics (AFP) proton detector [41], will extend the physics programme at high pseudorapidity. For further details the reader is referred to [38].

Phase-II

During the Phase-II, the whole Inner Detector will be replaced by a new all silicon Tracking Detector. This upgrade is called Inner Tracker (ITk). The TRT will be replaced in favour of a new all-silicon tracker. An international R&D is currently working on the development of suited detector technologies to fulfil the HL-LHC requirements. The work described in this thesis is part of the ATLAS R&D for future tracking detectors. A new generation of pixel sensors, where material budget, cost and radiation hardness is optimized, is investigated and fully characterized in this thesis. The Inner Detector upgrade is explained in more detail in section 1.4. The other upgrades foreseen in Phase-II are related with the calorimeter electronics, muon trigger system and electronics, and possible changes to the forward calorimeters. For further details the reader is referred to [31].

1.4 Requirements and challenges for the ATLAS Inner Detector upgrade

The current Inner Detector can not survive the planned high luminosity operation nor meet the performance requirements for HL-LHC, specially in terms of radiation damage, bandwidth saturation, and occupancy. The Inner Detector was designed to operate for 10 years at a peak luminosity of $10^{34}\,\mathrm{cm^{-2}s^{-1}}$, with an assumed 23 pile-up events per 25 ns bunch crossing, and a level-1 trigger rate of 100 kHz [31]. That translated to the SCT requirements meant the use of detectors capable to operate up to fluences of $2 \times 10^{14}\,\mathrm{n_{eq}cm^{-2}}$. The Pixel Detector used radiation hard sensor and electronics technologies to withstand ionizing dose levels up to 50 Mrad, and the sensors needed to cope fluence levels degradation of $10^{15}\,\mathrm{n_{eq}cm^{-2}}$. This is estimated to correspond to $400\,\mathrm{fb^{-1}}$ [31].

Several years of international R&D on the cutting edge of technology, prototyping, requirement testing, and commissioning allowed the successful fabrication and insertion of IBL in ATLAS [33]. The IBL, designed to survive $850\,\mathrm{fb^{-1}}$ [31], copes with levels up to 250 Mrad, and fluence degradation of $5 \times 10^{15}\,\mathrm{n_{eq}cm^{-2}}$. It was a big technological challenge for the international community. One of the outcomes of this upgrade was the insertion of the 3D silicon sensor concept [42] for the first time in a HEP experiment.

The foreseen scenario of ATLAS at the HL-LHC is to operate at a peak luminosity of $7 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$, with 200 pile-up events per 25 ns bunch crossing as described in 1.2.1. That motivates the full replacement of the Inner Detector during LS2 (2024). The new Inner Detector will be an all-silicon tracker, replacing the TRT detector by strip and pixel silicon layers. The final layout is currently under discussion, and with a preliminary estimation of about $220\,\mathrm{m^2}$ silicon area to be distributed among pixel and strip detectors [23]. A preliminary layout of the ITk is depicted in figure 1.11. The final layout will likely contain 4-6 pixel layers, which corresponds to $22\,\mathrm{m^2}$ silicon pixel surface and 6-4 strip layers. The pixel area increase supports to distinguish the performance requirements of the ITk Pixel Detector between inner and outer layers as summarized in table 1.1.

	Pixels LHC	IBL	Pixels HL-LHC (inner layers)	Pixels HL-LHC (outer layers)
Particle rate	$1\,\mathrm{MHz/mm^2}$	$5\,\mathrm{MHz/mm^2}$	$10\,\mathrm{MHz/mm^2}$	$1\,\mathrm{MHz/mm^2}$
Total Ionizing Dose (TID)	50 Mrad	250 Mrad	1 Grad	50 Mrad
Non Ionizing Energy Loss (NIEL)	$10^{15}\,\mathrm{n_{eq}cm^{-2}}$	$5 \times 10^{15}\,\mathrm{n_{eq}cm^{-2}}$	$2 \times 10^{16}\,\mathrm{n_{eq}cm^{-2}}$	$1 \times 10^{15}\,\mathrm{n_{eq}cm^{-2}}$
Silicon Area	$\approx 1.73\,\mathrm{m^2}$	$\approx 0.15\,\mathrm{m^2}$	$\approx 1\,\mathrm{m^2}$	≈ 10 - $20\,\mathrm{m^2}$
Pile-up	23	23	200	-

Table 1.1: Requirements of the ATLAS Pixel Detector for the LHC and for the HL-LHC. The data provided in this table are extracted from [23], [31], [33], [43].

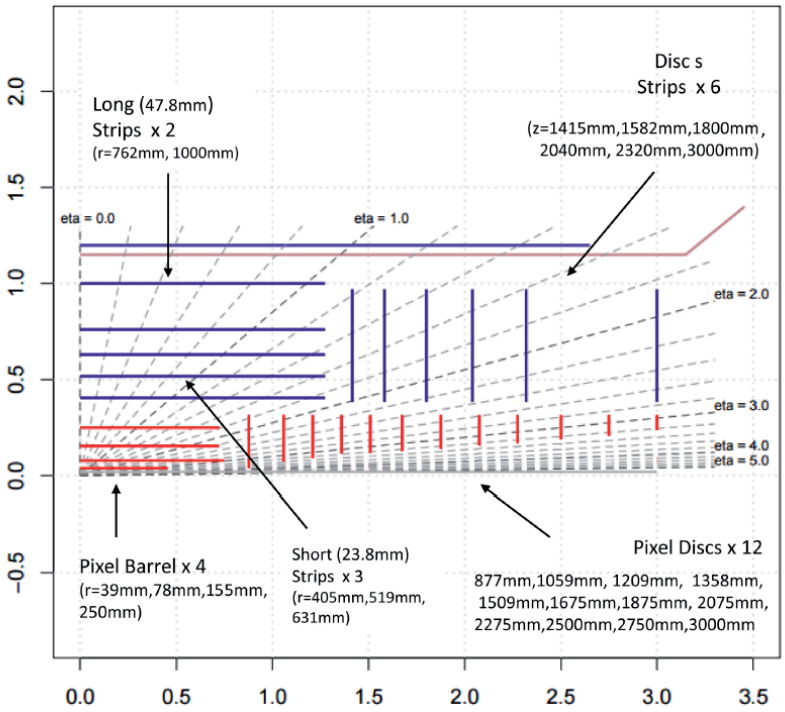


Figure 1.11: A cross-section of the Inner Detector middle scenario layout, where the pseudorapidity coverage extends up to $|\eta| = 3.2$. Blue and red lines represent strip and pixel layers, respectively [23].

The inner pixel layer challenges are driven by radiation hardness and particle rate per area and so far only hybrid pixels can cope these levels. The outer pixel layer challenges are driven by the cost and production effectiveness and new developments are being investigated.

The requirements increase by at least an order of magnitude which respect to the currently installed detectors, leading to an exciting and challenging R&D time. The international pixels and strip collaborations are very active since several years seeking for new technologies to fulfil the HL-LHC requirements. In addition, an international R&D collaboration, named the ATLAS CMOS Pixel Collaboration, was formed seeking new detector concepts as an option for the ITk pixel layers. Its proposal aims toward the development of both hybrid and monolithic approaches, based on industrially available Complementary Metal–Oxide–Semiconductor (CMOS) processes as sensor layer, which would lead to several advantages like smaller pixel sizes, lower material budget, cheaper price while fulfilling the radiation hardness requirements.

The focus of this thesis is the definition and performance of a validation program of a novel monolithic approach towards the HL-LHC. The different pixel trends and approaches, as well as the monolithic approach studied in this thesis, towards HL-LHC are explained in detail in chapter 4.

Chapter 2

Vertexing and tracking detectors in HEP experiments

Vertexing and tracking detectors are crucial for the physics analyses since they are responsible for primary vertex identification and reconstruction of secondary vertex for b-quarks identification as described in section 1.3.1. The vertex detection and impact parameter measurements are determined by particle tracking close to the interaction point. Solid state detectors and in particular pixel silicon detectors are used to accomplish that.
This chapter starts with a brief introduction of how particles are detected through their interaction with matter. Section 2.2 proceeds describing the building block of solid state detectors for tracking in order to describe a pixel detector, the signal formation, and transport. Section 2.3 describes the measurements that a tracking detector is responsible for, and calculates their resolution. That naturally brings up the requirements to accomplish by a tracking detector.

2.1 Interaction of particles with matter

Only charged particles are used for the vertexing and tracking measurements. There are two main features characterizing the passage of charged particles through matter. The first one is the loss of energy by the particle due to inelastic collisions with the atomic electrons of the material. The measurement of the energy loss by the particle on its path through the detector is the mechanism which allows particle detection. Therefore, the interaction of charged particles with matter is covered in section 2.1.1.
The second one is the deflection of the particle from its incident direction due to multiple scattering. This effect degrades the momentum resolution, vertex resolution and impact parameter resolution of a detector, thus this effect needs to be minimized. The multiple scattering is covered in section 2.1.2.
This section concludes with a description of the energy loss of photons in matter since the photon interaction with matter is extensively used in sensor characterization in the laboratory.

2.1.1 Detection of charged particles

Particles interact differently with matter depending on their energy and mass, that is why heavy and light charged particles are treated separately.

Charged particles with a mass well above the electron mass ($M >> m_e$) undergo energy losses mainly due to excitation and ionization of atoms of the medium along their passage through matter. The process responsible for that energy loss is the inelastic collisions with the atomic electrons. In these collisions a part of the kinetic energy of the particle is transferred to the atom, causing ionization (hard collisions) or excitation (soft collisions) of the latter. This leads to the release of free charge carriers or light from the excitation. The extraction of these free charges is the most used mechanism to detect relativistic heavy particles as will be explained in section 2.2. The average energy loss dE per unit path length dx (or the stopping power) is approximated by the Bethe-Bloch formula [28]:

$$-\frac{dE}{dx} = \frac{4\pi r_e^2 m_e c^2 N_A Z z^2}{A\beta^2} \cdot \left(\frac{1}{2}\ln\left(\frac{2m_e c^2\beta^2\gamma^2 T_{max}}{I^2}\right) - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right) \tag{2.1}$$

with:

c:	speed of light
m_e:	electron rest mass
r_e:	classical electron radius (r_e= 2.817×10^{-13} cm)
N_A:	Avogadros number (N_A= 6.022×10^{23} mol^{-1})
Z:	atomic number of absorbing material
z:	charge of incident particle in units of e
A:	atomic weight of absorbing material
I:	mean excitation energy of the material ($I \simeq I_0 Z$ with $I_0 = 12$ eV)
β:	$= \frac{v}{c}$ of the incident particle
γ:	Lorentz factor ($\gamma = \frac{1}{\sqrt{1-v^2/c^2}}$)
T_{max}:	maximum transferable kinetic energy from incident particle to atomic electrons

The energy loss $\frac{dE}{dx}$ given by eq. 2.1 is already normalized to the density of the material, and as a consequence it is independent of the material. The energy loss then depends only on the velocity of the particle, as it is illustrated in figure 2.1. At energies below the maximum ($\beta\gamma < 0.1$), the velocity of the incident particle is comparable or smaller than the orbital velocity of the atomic electrons. Thus, the assumption that the electron is stationary with respect to the incident particle is not valid. The Bethe-Bloch formula breaks down and the Shell correction (C) needs to be applied [44]. At not-relativistic energies, the loss of energy is dominated by the $1/\beta^2$ term and decreases with increasing velocity as observed in figure 2.1. At relativistic energies ($\beta \approx 1$) the energy-loss curve arrives to a minimum. A particle at the minimum energy-loss is called Minimum Ionizing Particle (MIP). It is often used to quantify the detector response without particularizing the particle energy. A MIP is considered the worse-case scenario for detectors since the provided particle signal is the lowest. At energies beyond this point, the term $1/\beta^2$ becomes constant and the energy loss rises due to the relativistic component. However the relativistic rise (dashed blue line) is cancellated by the density correction [44] (dashed brown line) which needs to be applied.
The amount of kinetic energy transferred in each collision is generally a very small fraction of the total kinetic energy. However, the number of collisions per unit path length is so large,

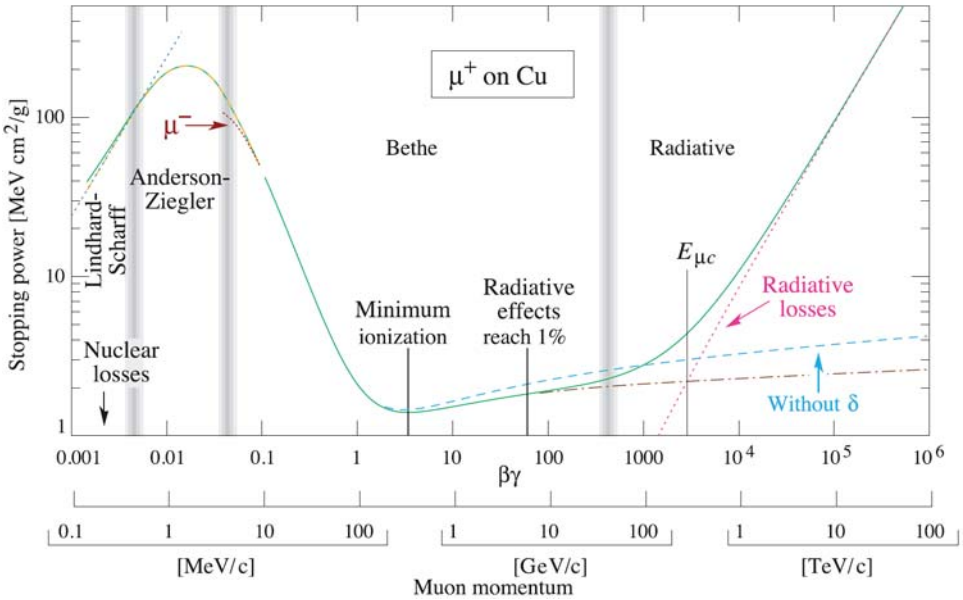


Figure 2.1: Energy loss or stopping power for muons penetrating copper as a function of $\beta\gamma$ [28]. The dashed lines for $\beta\gamma > 1$ illustrate the energy loss for heavy charged particles as described by the Bethe-Bloch-Formula with (brown) and without (blue) density correction. The solid line for $\beta\gamma > 1$ illustrates the Bremsstrahlung looses which becomes dominant at high momentum for light charged particles.

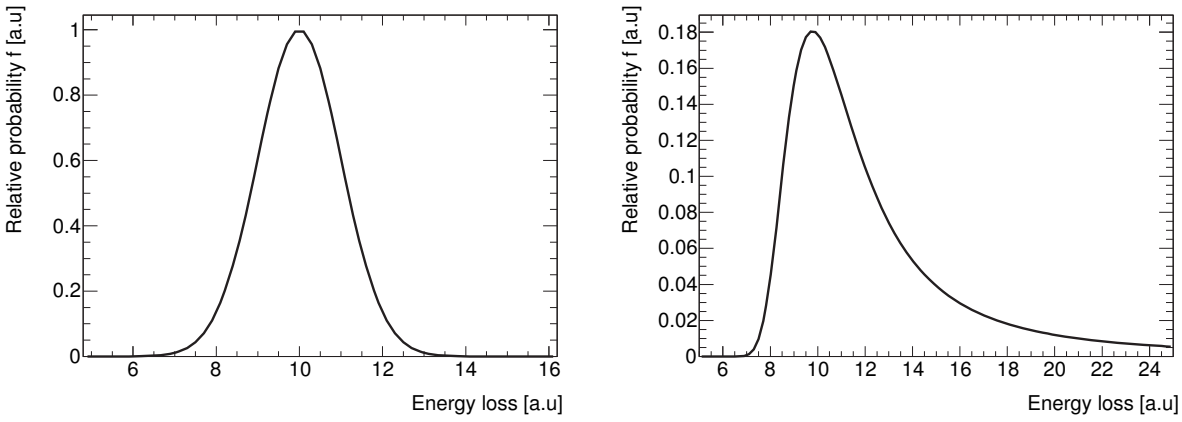
that a considerable cumulative loss of energy is observed, even in thin layers of material. For example, a 10 MeV proton loses all its energy in 0.25 mm of copper. In tracking detectors ideally the particles pass through and deposit a negligible quantity of its energy before entering in the calorimeters where its full energy is absorbed and measured. To minimize the loss of energy while keeping excellent tracking performance, the detector thickness and the material type must be chosen carefully in tracking detectors.

Lightweight charged particles, like electrons, at low energies lose energy when traversing matter mainly due to ionization, although other processes contribute [44]. In addition, at high energies their energy loss is completely dominated by Bremsstrahlung emission as observed in figure 2.1. An incident electron decelerates due to its interaction with the Coulomb field of the nucleus. This deceleration provokes photon emission, known as Bremsstrahlung emission. The energy loss due to Bremsstrahlung is proportional to the energy E of the incident particle accordingly to:

$$-\left(\frac{dE}{dx}\right)_{rad} = \frac{E}{X_o} \tag{2.2}$$

where the proportional constant is so called radiation length (X_o). The X_o corresponds to the mean distance in which a high energy lightweight particle looses $1-1/e = 63\%$ of its energy by Bremsstrahlung. X_o is a material property which depends mainly on the material density, mass number and atomic number of the material [44]. X_o is commonly used as an unit to quantify the detector mass, also referred to as material budget.

Inelastic collisions are statistical in nature, thus they happen with a certain quantum mechanical probability and the energy loss value is within a distribution. However as the fluctuations are very small, the average energy loss is used. For relatively thick absorbers, where the number of collisions is large, the energy loss distribution approaches a Gaussian distribution as shown in figure 2.2a. Whereas for thin absorbers, as is the case of tracking detectors, the energy loss distribution is described by a Landau distribution as shown in figure 2.2b.



(a) (b)

Figure 2.2: Typical energy loss distribution of a MIP in a (a) relatively thick absorber, which approaches a Gaussian distribution (b) thin absorber (silicon detector like), which approaches to a Landau distribution.

2.1.2 Multiple scattering

Charged particles passing through matter, in addition to inelastic collisions, suffer also elastic collisions with the nuclei. These collisions lead to small angular deflections. Thus, the particle path can be visualized as a zigzag path with a net deflection from its incident direction. The net scattering in a layer of width d, result of a large number of collisions, is called multiple scattering. The multiple scattering distribution can be approximated by a Gaussian with the mean value at zero and the standard deviation (distribution width) [45]:

$$\sigma_0 \approx \frac{13.6\,\text{MeV}}{p\,v} \cdot \sqrt{\frac{d}{X_o}} \tag{2.3}$$

where p is the momentum, and v the velocity of the incident particle. A 10 GeV electron beam traversing a 250 µm thick silicon layer results in a sigma of the deflection angle histogram of 70 µrad. In practice the multiple scattering limits the precision of the particle direction measurement, and in consequence the precision of the momentum resolution, vertex and impact parameter resolution. To minimize the multiple scattering, the detector layers need to be composed by a thin and high X_o material.

2.1.3 Energy deposition of photons

Photons interact completely different with matter due to its electrical neutral nature. The major interactions of photons in matter are:

- **Photoelectric Effect** happens when the energy of the incident photon E_γ is slightly higher than the ionization energy of the atom E_i ($E_\gamma \geq E_i$). The photon is absorbed by the atomic electron, and in consequence the electron is ejected from the atom with a energy $E = h\upsilon - E_i$ where h is the Plank constant and υ the frequency of the atomic electron.

- **Compton Scattering** happens when the incident photon E_γ is very energetic ($E_\gamma \gg E_i$). In this case, the atomic electron can be considered as free. The result is the ejection of the atomic electron with a certain angle and a deflected photon with energy $E_\gamma^{`}$ where $E_\gamma^{`} < E_\gamma$.

- **Pair Production** may happen when the incident photon has an energy higher than 1.022 MeV ($E_\gamma > 2m_e$). The result is the transformation of the incident photon into an electron-positron pair.

There are two main features characterizing the interaction of photons with matter. The first one is that the total cross section of photons interaction with matter ($\sigma_{tot} = \sigma_{photoE} + \sigma_{compton} + \sigma_{pair}$) is much smaller than the cross section relative to inelastic collisions. As a consequence, the photons penetrate deeper into matter. The second one is that the above processes describe how the incident photon is either absorbed or removed from the beam. Therefore, a beam of photons does not reduce its energy in its path through matter but rather its intensity is attenuated as:

$$I(x) = I_0(x) \cdot e^{-\mu x} \tag{2.4}$$

where I_0 is the initial intensity, x is the absorber thickness and μ is the absorption coefficient depending on the material and energy. A more detailed mathematical formalism of these processes is described in [44].

As an example, a beam of γ-photons coming from a ^{55}Fe source has reduced its intensity by 80% after 50 µm of silicon. For the 80% absorbed photons all their energy was deposited on the silicon. That makes γ sources very interesting detectors characterization in the laboratory. Figure 2.3 shows the typical spectrum of a ^{55}Fe radioactive source in a silicon detector. The contribution at small energies is due to the electrons generated by the Compton effect, whereas the peaks at higher energies corresponds to the electrons generated by the Photoelectric effect, in which the full energy is absorbed in the silicon.

The interaction of charged particles and photons with matter are extensively used for detectors characterization in the laboratory. The charge calibration measurements of the detectors are performed by the use of radioactive γ-sources as ^{55}Fe while the depletion depth measurements are based on β-sources (charged particles) as it will be described in chapter 6.

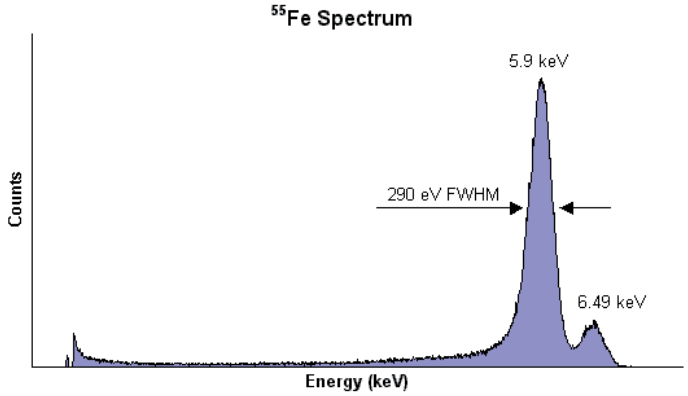


Figure 2.3: Typical spectrum of ^{55}Fe radioactive source in silicon [46]. The contribution at small energies is due to the electrons generated by the Compton effect. The peaks at higher energies corresponds to the electrons generated by the Photoelectric effect.

2.2 From a semiconductor to a silicon pixel detector

The building block of tracking detectors in the current HEP experiments are solid state detectors, and sometimes gas detectors. The solid state detectors use semiconductor material, most commonly silicon. Depending on the required precision strip or pixel silicon detectors are used.
This section describes briefly the characteristics of semiconductors, and pn-junction properties to arrive to the description of a silicon pixel detector for tracking purposes, which is essentially a reversely biased pn-junction. Subsequently, the signal formation and the transport mechanism in a pixel silicon detector are explained in section 2.2.4. Finally the readout electronics of a silicon detector is introduced in section 2.2.5.

2.2.1 Energy band structure: semiconductors

Although atoms in a crystal are shown as discrete objects, the wavefunctions of the atomic electrons extend over distances of 1-2 Å. These wavefunctions will overlap with each other, resulting in electrons being shared with neighbouring atoms to form covalent bonds and make the outer shells fully occupied. These interactions result in splitting each of their energy-levels into separate energy-levels, consistently with the Pauli exclusion principle. In a crystal, the large number of energy-levels scales almost continuously, and as a consequence they can be represented by energy bands, as shown in figure 2.4. The band structure is formed by bonding states (valence band) filled up with valence electrons, by a forbidden gap, and by anti-bonding states (conduction band). The width of the forbidden band is commonly called gap energy (E_g) and leads to the classification of solids in insulators, conductors and semiconductors.

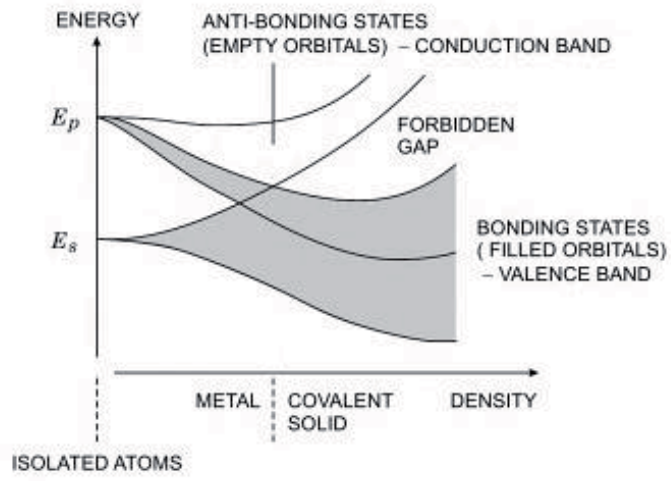


Figure 2.4: Energy bands structure on a solid [47]. The left part shows the energy bands of a conductor while the right part the energy bands of a semiconductor. E_p and E_s are the energy of the p- and s-bonding states,respectively.

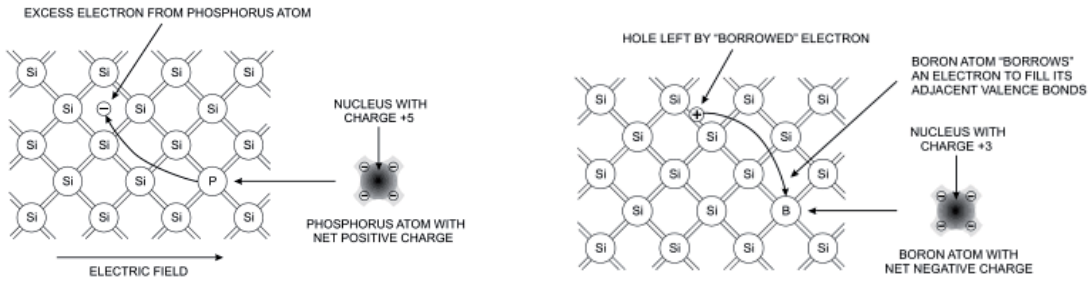
Semiconductors are characterized by an energy gap between 1 eV and 5 eV. At 0 K all electrons occupy bonding states, filling completely the valence band. As no states are occupied in the conductive band, no electrical conduction is possible. At energies $E > E_{gap}$, imparted either by incident radiation or by thermal energy, an electron of the valence band is excited to the conductive band, leaving a vacant, so called hole, in the valence band. The electron and the hole can move freely within the conduction and valence band, respectively, which produces an electrical current. In silicon the E_{gap} is 1.2 eV and the average energy needed to create an electron-hole pair is 3.6 eV, also called electron affinity [47]. The low E_{gap} and therefore the high signal per energy loss makes semiconductors, and in particular silicon, very interesting for particle detection.
Furthermore, the conductivity of a semiconductor can be controlled by introducing impurities.

Doping

The introduction of impurities to the semiconductor causes the apparition of intermediate levels into the forbidden gap. This is called doping. As a consequence, less energy needs to be provided to create free charges in the semiconductor and the electrical parameters such as resistivity can be adjusted conveniently.

The n-type doping consists in replacing a silicon atom (group IV) by an atom with five valence electrons (group V). This leaves one valence electron without a partner as illustrated in figure 2.5a. This impurity is called donor since it contributes to an excess of electrons in the lattice. The donor electron generates a new state inside the forbidden gap. This bound level is illustrated in figure 2.6b, and is of the order of 0.01 eV below the conduction band [47]. In consequence, at room temperature the probability of ionization by the thermal energy

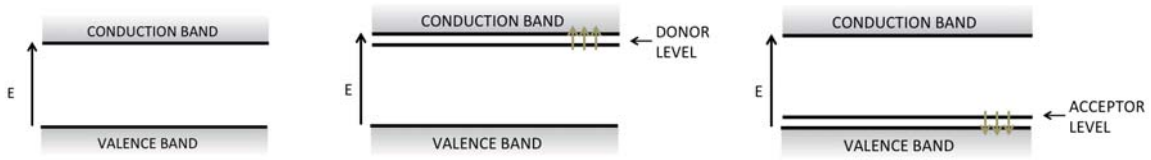
(E ≃ 0.026 eV) is significant. For an n-type doped material, the majority of the conduction is provided by electrons.



(a) (b)

Figure 2.5: Introduction of impurities in pure silicon material. (a) n-doping case, which consists on replacing a silicon atom by an atom from group V. (b) p-doping case, which consists on replacing a silicon atom by an atom from group III [47].

The p-type doping consists on replacing a silicon atom by an atom with three valence electrons (group III), called acceptor. In that case, an electron is missing in the valence band, forming a positive charge state called hole as illustrated in figure 2.5b. This introduces a bound state in the forbidden gap, illustrated in figure 2.6c, which is located in the order of 0.01 eV above the valence band [47]. The majority of the conduction is generated by holes.



(a) (b) (c)

Figure 2.6: Energy band structure for a semiconductor (a) with no doping (b) n-doped (c) p-doped. The doping generates new levels inside the forbidden gap, called donor level for a n-doped, and acceptor level for a p-doped.

The concentration of electrons (holes) in the conductive band (valence band) is given by the Fermi-Dirac function [48]:

$$n = 2\left(\frac{2\pi m_n kT}{h^2}\right)^{\frac{3}{2}} e^{-\frac{E_C - E_F}{kT}} \tag{2.5}$$

$$p = 2\left(\frac{2\pi m_p kT}{h^2}\right)^{\frac{3}{2}} e^{-\frac{E_F - E_V}{kT}} \tag{2.6}$$

A semiconductor as described above can not be used for particle detection. The reason for that is that by thermal generation the semiconductor is always conductive or insulating. For particle detection it is desirable that the semiconductor behaves approximately as an insulator until a charged particle passes through it. In this case, the collected current is related with the detected particle. That behaviour is achieved by creating a reversely biased pn-junction (pn diode).

2.2.2 pn-junction

A silicon detector for particle tracking, careless of its electrode geometry, is a pn diode operated in reversed bias mode with the depleted zone acting as an ionization chamber.

Unbiased pn-junction

A pn-junction is a silicon crystal properly doped in a way that one part is p-type doped and the other side is n-type doped as illustrated in figure 2.7 [49]. Initially the p- and n-regions are electrically neutral, but the density gradient between them results in thermal diffusion. Thermal diffusion stimulates the movement of holes into the n-region and electrons to the p-region. Space charges are built-up which generates an electrical field in the opposite direction. The equilibrium, so called thermal equilibrium, is achieved when diffusion and electrical field compensate each other, as shown in figure 2.7b. At thermal equilibrium two zones can be distinguished: the space charge or depletion region and the outer part. The depletion region does not contain free charges, but only ionized donors or acceptor impurities, whereas the outer part is conductive.

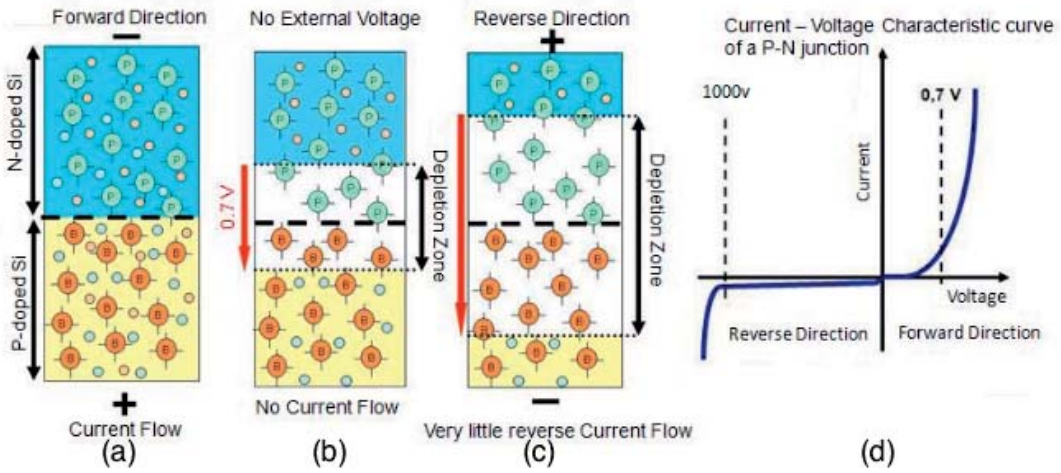


Figure 2.7: A pn-junction under different bias conditions [49] (a) forward bias voltage is applied leading to a large current flow (b) no external bias voltage is applied, leading to the pn-junction equilibrium and no current flow (c) reversely biased voltage is applied leading to a very little current flow. The Current-Voltage curve of a pn-junction is shown in (d).

Only when a particle traverses the depletion region free charges are created by ionization of the media. As a consequence, the depletion region is the interesting part for tracking detection. The width of the depleted zone defines the signal size in a silicon detector and thus is one of the most important characteristics in the sensor characterization. The width of the depletion region in an unbiased pn-junction is given by:

$$W = \sqrt{\frac{2\epsilon V_0}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{2.7}$$

where V_0 is the intrinsic potential, which is of about 0.5-1 V for the typical detectors used in ATLAS [50]. and N_a, N_d are the acceptor and donor concentrations, respectively. A typical silicon detector in ATLAS with $N_d = 10^{12}\,\mathrm{cm}^{-3}$, $N_a = 10^{18}\,\mathrm{cm}^{-3}$ and $n_i = 1.45 \times 10^{10}\,\mathrm{cm}^{-3}$ shows a depletion width of approximately 0.16 nm. The width of the depletion layer of an unbiased junction for detector bulk made of n-type silicon with $N_d \leq 10^{12}\,\mathrm{cm}^{-3}$ can be estimated to a few 10 µm [50].

Reversely biased pn-junction

The application of a negative bias (reverse bias) to the pn-junction increases the potential barrier, and the width of the depletion zone grows as illustrated in figure 2.7c. In addition, the application of an electrical field in the depletion region makes the free charges drift to the electrodes. This increases the speed of the particle detection in the junction. This is the case which is useful for a particle detector.

The depletion width for reversely bias voltage ($V_b < 0$) pn-junction is given by:

$$W = \sqrt{\frac{2\epsilon(V_0 - V_b)}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)} \tag{2.8}$$

In most particle detection applications, the doping concentration is asymmetrical ($N_d \neq N_a$) in order to make the depletion depth grow only in one direction according to $N_d \cdot x_n = N_a \cdot x_p$ [47]. Therefore, two cases are possible:

$$W = \sqrt{\frac{2\epsilon}{qN_d} \cdot (V_0 + V_b)} \quad \text{n-type detector } (p^+ n \, junction) \quad N_d \leqslant N_a \tag{2.9}$$

$$W = \sqrt{\frac{2\epsilon}{qN_a} \cdot (V_0 + V_b)} \quad \text{p-type detector } (n^+ p \, junction) \quad N_a \leqslant N_d \tag{2.10}$$

The contact potential V_0 is very small with respect to the depletion voltage, thus in the following it is neglected. The silicon detector resistivity ρ is given by:

$$\rho = \frac{1}{\mu \, q \, |N_{eff}|} \qquad N_{eff} = N_d - N_a \tag{2.11}$$

where μ is the mobility of electrons (n-type detector) or holes (p-type detector), q the electron charge, and N_{eff} is the effective doping concentration. The depletion depth can be re-written with the use of equation 2.8 and 2.11 as follow:

$$W = \sqrt{2\,\epsilon\,\mu\,\rho\,V_b} \tag{2.12}$$

The fact that the depletion zone does not contain free charges (unless created by thermal energy resulting in leakage current or by an ionizing particle resulting in signal current) makes it desirable for particle detectors. At the same time, due to the electrical field in the depletion zone, the charges generated in the depletion zone move by drift as explained in section 2.2.4 and contribute to a fast and large signal.

Leakage Current

The leakage current is the current induced by thermally created electron-hole pairs. The particle signal in the detectors will accumulate on top of the leakage current background. Therefore, it is crucial to keep the leakage current small. The leakage current as a function of the high voltage and the break-down voltage (V_{bd}) are important characteristics to qualify in silicon detectors. The dependence of the current as a function of the voltage in the pn-junction is illustrated in figure 2.7d and given by:

$$I = I_0(e^{\frac{eV}{kT}} - 1) \tag{2.13}$$

For a positive bias voltage (forward bias) the exponential term dominates and the current increases rapidly. This case reduces the electrostatic voltage and depletion width, which leads to an increase of the conduction across the pn-junction. For large negative bias voltage (reverse biased) the absence of free charges was assumed and in consequence the lack of current flow. However, the thermal excitation can promote electrons to the conductive band, so current flows even in absence of radiation or particles traversing the detector. In reverse bias mode the exponential term in equation 2.13 becomes negligible and the current is in saturation (I = I_0) up to the break-down voltage (V_{bd}). That small current produced when a diode is reversely biased is called dark current or leakage current. At a certain high voltage named break-down voltage, the free electrons have energy enough to generate secondary free electrons and an uncontrolled avalanche starts, and thus the current through the sensor drastically increases.

The leakage current is proportional to the detector volume V and to the intrinsic density $n_i(T)$ and temperature as follows:

$$I_{leak} = \frac{en_i(T)V}{2\tau} \tag{2.14}$$

or:

$$I_{leak} \propto T^{\frac{3}{2}} e^{-\frac{E_G}{2k_BT}} \tag{2.15}$$

The leakage current is highly temperature dependent. An increase of about 7 °C doubles the leakage current. The leakage current is a source of noise in the detector. Typically this contri-

bution is negligible in comparison to the total electronic noise for the low leakage current of silicon detectors. After irradiation, the increase of the leakage current, which is explained in chapter 3, is considerable and the leakage current becomes a significant noise source.

2.2.3 Silicon pixel sensors

A silicon pixel sensor is a reversely biased pn-junction, where the charge collecting electrode is segmented in two directions to achieve the needed position resolution for tracking. A cross section of a typical pixel silicon detector is shown in figure 2.8.
The $n^+ - p$ junction, where $N_d > N_a$, aims to create the depletion width only in the bulk direction as depicted in figure 2.8. The sensor is backside processed to provide an ohmic contact, allowing the bias voltage appliance from the bottom of the sensor. The depletion region grows from the n^+ electrodes to the bulk. The electrons generated by charged particles move towards the n^+ collecting electrodes.

As an example, a typical 300 µm thick sensor with a resistivity of 2 kΩ cm, and a doping

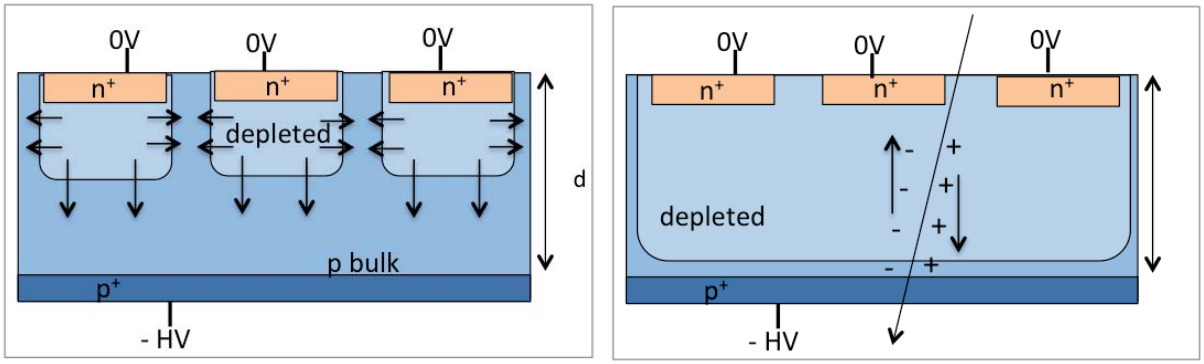


Figure 2.8: Cross section of a p-in-n pixel silicon detector where (a) shows the depletion region growth and (b) shows the drift of charge carriers generated by an ionizing particle.

concentration of 10^{18} cm^{-3} is fully depleted at a bias voltage of 200 V. The leakage current for a typical pixel sensor in ATLAS before irradiation is about 400 nA at room temperature [51].

2.2.4 Signal generation and transport in a silicon sensor

The electron-hole pairs generated by an ionizing particle traversing the detector can move through the silicon, as mentioned in section 2.2.1. They can move according to two mechanisms: drift (dominates inside the depletion zone) and diffusion (dominates outside the depletion zone). Both movements results in a signal.

In case the sensor is fully depleted, all the generated free carriers move driven by drift with a velocity, which only depends on the local electrical field:

$$\vec{v}(x) = \mu\vec{E}(x) \tag{2.16}$$

In case the sensor is partially depleted, the generated carriers inside the depletion zone will move toward the electrode by drift as just described. Meanwhile, the generated carriers outside the depletion region will move by diffusion until they reach the depletion zone. It is not the collection of the carriers at the electrodes what produces a signal, but their movement. The movement of the charge carriers induces a signal in the electrodes. The current induced by a moving charge is described by Ramo's theorem [47]:

$$I = q_0\vec{v}(\vec{r}) \cdot \vec{E}_W(\vec{r}) \tag{2.17}$$

where $\vec{E}_W$ is the weighting field and $\vec{v}$ is the carrier velocity. The weighting field depends only on the device topology and it is obtained by applying unit potential to the measured electrode and zero to the rest. For a two planar electrode geometry of distance d the result is:

$$\vec{E}_W = -\frac{1}{d}\vec{z} \tag{2.18}$$

While the electrical field determines the charge trajectory and velocity, the weighting field determines how the charge motion couples to an specific electrode. The total signal measured $\int I(t)dt$ in any detector is the sum of the electrons and holes contribution.

The signal is generated faster if the carriers move by drift than by diffusion. One should mention that for HEP experiments, as ATLAS or CMS, where fast processing time and radiation hardness requirements are crucial, the sensor needs to be fully depleted. This implies that all charge carriers generated by an ionizing particle move due to the drift mechanism and as a consequence the signal is collected fast. In addition, it suffers less trapping after irradiation as it will be described in chapter 3. However, for other experiments in which radiation and collection time are less important, as for example ALICE or the Solenoidal Tracker at RHIC (STAR), operation with partial depletion or without any depletion is sufficient.

2.2.5 Detector readout

The signal induced in the n^+ electrodes is sent to the readout electronics of the detector. The electronic readout can be located in the same piece of silicon (monolithic approach) or in a different piece of silicon (hybrid approach). Both detector types are described in detail in chapter 4. The readout electronics usually consist of an analogue part to amplify and shape the signal and a digital data processing logic. The detector readout architecture is developed explicitly matching the requirements of the experiment and thus a detailed description is out of the scope of this thesis.
However, the building block of any readout electronics are the Metal–Oxide–Semiconductor

Field-Effect Transistor (MOSFET) transistors. Thousands of transistors compound the actual readout chip of the ATLAS Pixel Detector per pixel. The transistors performance are going to determine the performance of all the components (amplifier, switches ...). A qualitative introduction to the bases of a MOSFET transistor is provided here.

MOSFET Characteristics and Transfer characteristics

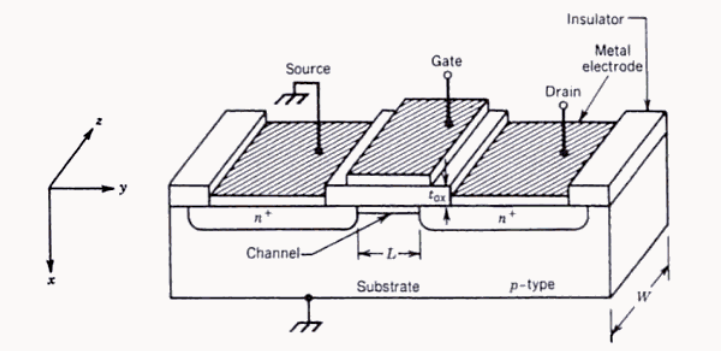


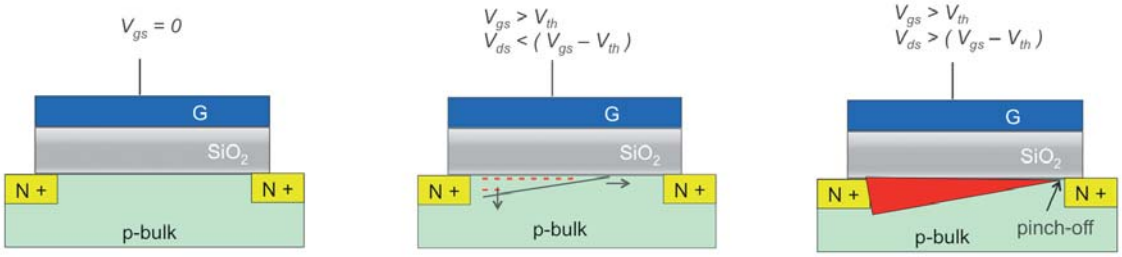
Figure 2.9: Schematic cross section of a MOSFET electron channel (nMOS) [52].

A MOSFET [53] is a four terminal device designated as gate (G), source (S), drain (D), and substrate (B) as illustrated in figure 2.9. The current between drain and source is controlled by the electric field established on the channel by the gate potential. A MOSFET can be classified depending on the type of conducting carriers flowing in the channel. It is called nMOS when electrons flow in the channel, and pMOS when holes flow in the channel. For simplicity, further on will focus on a nMOS transistor, a similar description can be done for a pMOS transistor. The MOSFET is essentially a Metal–Oxide–Semiconductor (MOS) capacitor with two p-n junctions placed adjacent to the channel. The understanding of the MOS structure is the key for understanding the MOSFET operation.

A MOS structure has three operation modes: accumulation, depletion and inversion. Lets consider a MOS structure where the semiconductor is p-type. When a negative voltage is applied to the metal gate ($V_G < 0$) holes will be attracted by the SiO_2-Si interface leading to an accumulation of majority charge carries (holes) close to the SiO_2-Si interface. This mode is called accumulation. When a small positive gate voltage ($V_G > 0$), the holes are repelled from the oxide-semiconductor interface leaving behind a space charge region formed by charged acceptors. At the same time minority charges (electrons) are attracted to the oxide-semiconductor interface. This is called depletion. If V_G increases, eventually the electron concentration at the oxide-semiconductor interface will increase to a value equal or bigger than the hole concentration in the bulk. When this happens, the inversion is reached. The applied voltage at which the inversion is reached is called threshold voltage V_{th}.

Therefore in a MOSFET transistor, the applied gate-to-source voltage (V_{gs}) controls the channel formation and the drain-to-source voltage (V_{ds}) provokes the flow of drain-to-source current (I_{ds}). Considering now the full transistor of figure 2.9 three operation regions can be achieved as sketched in figure 2.10.

When no voltage is applied to the gate, the region between the source and the drain imme-

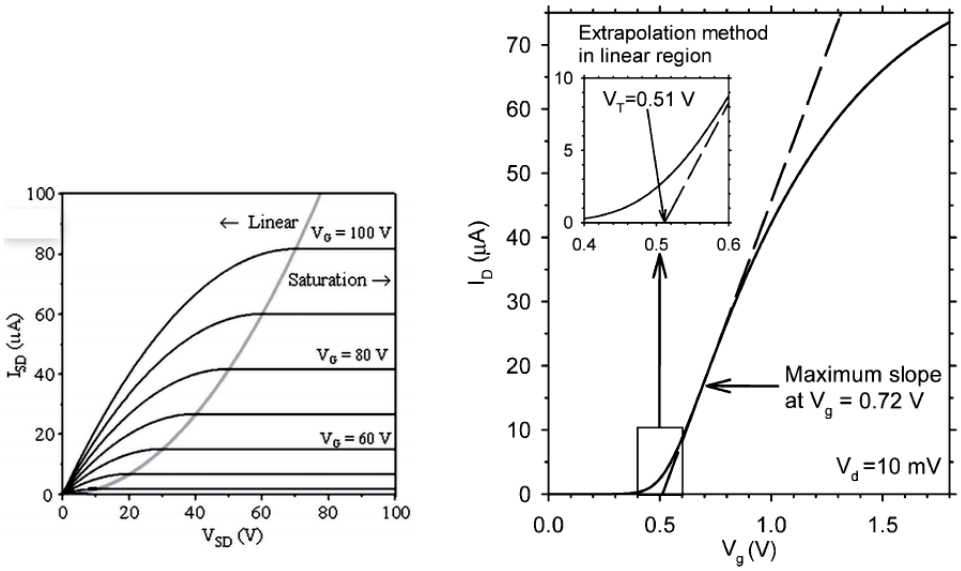


(a) (b) (c)

Figure 2.10: Operational modes of a nMOS transistor. (a) Cutoff mode: no channel is formed and no current is possible. (b) Linear mode: a channel is formed and a current flux between drain and source is enabled. (c) Saturation mode: current is formed and the current flux is constant. The bias conditions for each mode are summarized on top of each figure.

diately below the oxide contains an excess of holes. Effectively, this is an open circuit since no current can flow between the drain and the source. This is called "cutoff" region as shown in figure 2.10a. When applying a sufficiently positive voltage to the gate $V_{gs}(V_{gs} > V_{th})$ an inversion layer forms creating the n-channel. This enables a current flow between the drain and the source when $V_{ds} \neq 0$. The bigger is V_{gs}, the stronger the inversion in the conducting channel and the higher the current between source and drain. This is called linear mode and is illustrated in figure 2.10b. For a fixed value of V_{gs} above the threshold, the drain-to-source current following the conducting channel is controlled by V_{ds}. In the linear region the transistors acts like a variable resistance in function of V_{gs}. When V_{ds} is increased, it eventually reaches a point at which the inversion layer width is reduced to zero close to the drain implant. This is known as the "pinch-off" point above which the drain current remains essentially constant. Beyond the pinch-off point, the operation regimen is known as saturation region, as shown in figure 2.10c. The transistors operational modes are quantitatively summarized in figure 2.11. Figure 2.11a shows the $I_{ds} - V_{ds}$ curve, known as Transistor Characteristics, where the linear and saturation mode are observed for different gate voltages. Figure 2.11b shows the $I_{ds} - V_{gs}$ curve, known as Transfer Characteristics, where the V_{th} at which the transistor start to conduct is depicted.

The electrical parameters of a transistor can be extracted directly from the Transfer Characteristics. The electrical parameters define the transistor performance and in consequence the amplifiers, switches and other devices made of transistors in the readout electronic of the



(a) (b)

Figure 2.11: (a) MOSFET Characteristics where linear and saturation region are distinguished. (b) MOSFET Transfer Characteristics where the point in which the transistor start to conduct (V_{th}) is highlighted.

detector. Ionizing radiation traversing transistors creates several kind of damage, shifting its electrical parameters. The radiation damage mechanisms on MOSFET and its consequences is described in chapter 3. For the HEP experiments exposed to high ionizing doses the quantification of the transistor parameters shifts and the guarantee of its performance after irradiation is crucial. Therefore, this is one of the very primary characterization measurements that need to be performed when producing a new prototype.

2.3 Tracking and vertexing with tracking detectors

Tracking detectors measure the position of the particles when traversing the detector layers. They are responsible for momentum resolution, reconstruction of primary and secondary vertices, as well as for the identification of individual collisions through reconstruction of multiple primary vertices, b-tagging and reconstruction of tracks in jets. These measurements are crucial in HEP experiments. Pattern recognition algorithms use the position at the different layers to reconstruct the particle tracks. The reconstructed tracks are then combined to find primary and secondary vertices in the event, and to determine the transversal momentum of the particles coming out of the collision. This section uses some concepts previously described such as radiation length and multiple scattering, to explain the transverse momentum resolution, vertex resolution, and impact parameter resolution. The required momentum, vertex, and impact parameter resolution in a HEP experiment translates into a set of guidelines for the

detector design which is also covered in this section.

2.3.1 Transverse momentum resolution

The resolution of the transverse momentum measurement of a detector immersed in a magnetic field B, made of $N+1$ layers, each with an intrinsic spatial resolution σ is discussed here. The layers are spaced at a radii $r_0, r_1, ..., r_N$ and the detector lever arm is $L = r_N - r_0$. The resolution of the transverse momentum (p_T) is given by the quadratic sum of two terms:

$$\frac{\sigma_{p_T}}{p_T} = \sqrt{\left(\frac{\sigma_{p_T}}{p_T}\right)^2_{point} + \left(\frac{\sigma_{p_T}}{p_T}\right)^2_{MS}} \tag{2.19}$$

The first term, called point resolution, corresponds to the resolution to which a track can be measured neglecting the multiple scattering. The point resolution term of the transverse momentum is given by [54]:

$$\frac{\sigma_{p_T}}{p_T}_{point} = p_T \cdot \frac{\sigma}{0.3BL^2} \cdot \sqrt{\frac{720N^3}{(N-1)(N+1)(N+2)(N+3)}} \tag{2.20}$$

This brings up that higher resolution is achieved with low p_T particles, high layer-spatial resolution σ, large lever arm L, and large magnetic field B. The dependence on the number layers is only $1/\sqrt{N}$, but a high number of measurements points is important for the robustness of pattern recognition.
The second term corresponds to the uncertainty introduced by the multiple scattering, and it is given by [55]:

$$\frac{\sigma_{p_T}}{p_T}_{MS} = \frac{1}{0.3B}\frac{0.0136}{\beta}\sqrt{\frac{C_N}{X_0 L}} \tag{2.21}$$

where C_N is equal to 1.3 with a 10% accurancy [55]. According to eq. 2.21, when the multiple scattering is considered, the transverse momentum is highly dependent on the detector mass X_0. The multiple scattering limits the precision of the momentum resolution. To minimize its effect the detector layers need to be composed by thin material. In a tracking detector it is desirable that the multiple scattering contribution is negligible with respect to the point contribution.

2.3.2 Vertex and impact parameter resolution

The primary vertex is defined as the one presenting the largest sum of transverse momentum ($\sum_{track,vertex} p_T$). This allows to distinguish the hard-scatter or primary vertex from the other pile-up vertices. The vertex resolution for a two layer detector is calculated here. The detector layers, sketched in figure 2.12, are located at radius r_1, and r_2 from the beam axis. The layers spatial resolution is respectively σ_1 and σ_2. The vertex resolution is calculated as the intersection of at least two different particle trajectories. Two cases are shown in figure 2.12. First, it is assumed that $\sigma_1 \neq 0$ and $\sigma_2 = 0$, i.e. the position of the track is unequivocally calculated for layer 2, while for layer 1 has an uncertainty σ_1, as illustrated in the left part of figure 2.12.

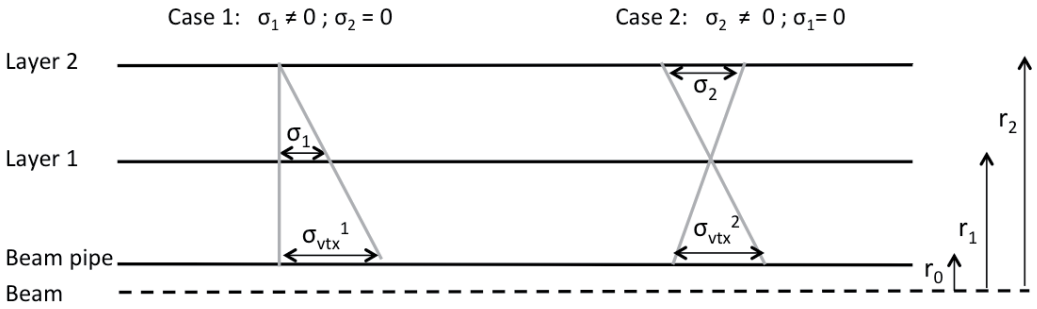


Figure 2.12: Schema of the vertex calculation measurement of a simple detector composed of two tracking layers located at radii r_1 and r_2 from the beam axis with resolutions σ_1 and σ_2. Two cases are highlighted in order to calculate the vertex resolution.

Thus, the vertex resolution σ^1_{vtx} is:

$$\sigma^1_{vtx} = \sigma_1 \cdot \frac{r_2}{r_1 - r_2} \tag{2.22}$$

Subsequently the other possibility ($\sigma_1 = 0$ and $\sigma_2 \neq 0$) is assumed as shown on the right part of figure 2.12. In that case, the vertex resolution σ^2_{vtx} is:

$$\sigma^2_{vtx} = \sigma_2 \cdot \frac{r_1}{r_1 - r_2} \tag{2.23}$$

The total vertex resolution is calculated as the quadratic combination of both contributions. But in addition the contribution from multiple scattering in the beam pipe and in the precedent detector layers needs to be taken into account. Here, only multiple scattering in the beam pipe is considered where r_0 is the beam pipe radius and σ_0 is the standard deviation of the scattering angle shown in eq. 2.3. This correction results in an additional degradation to the layers resolution:

$$\sigma_1 = \sigma_1 \oplus (r_1 - r_0) \cdot \sigma_0$$
$$\sigma_2 = \sigma_2 \oplus (r_2 - r_0) \cdot \sigma_0$$

Substituting the modified terms into the eqs. 2.22 and 2.25, and calculating the quadratic combination lead to the vertex resolution:

$$\sigma^2_{vtx} = \frac{r_1^2\sigma_1^2 + r_2^2\sigma_2^2}{(r_2 - r_1)^2} + \frac{(2r_1r_2 - r_0(r_1 + r_2))^2}{(r_2 - r_1)^2} \cdot \sigma_0^2 \tag{2.24}$$

or:

$$\sigma^2_{vtx} \sim \frac{r_1^2\sigma_1^2 + r_2^2\sigma_2^2}{(r_2 - r_1)^2} + \frac{(2r_1r_2 - r_0(r_1 + r_2))^2}{(r_2 - r_1)^2} \cdot \left(\frac{13.6\,\text{MeV}}{pv} \cdot \sqrt{\frac{d}{X_o}} \right)^2 \tag{2.25}$$

To achieve a small vertex resolution, the following requirements are desirable:

- a big lever arm, which comes from the $\frac{1}{(r_2 - r_1)^2}$ term.

- the need of thin layers of high radiation lengths material, which comes from the term $\frac{d}{X_0}$. Not only for the beam pipe (as used in this simplified calculation), but for every detector layer.
- a short distance between the first layer and the interaction point.
- a fine sensor segmentation, which reduces the layer spatial resolution.

The impact parameter shown in figure 2.13 is the closest distance of a track to the primary vertex as described in section 1. The impact parameter resolution determines the reconstruction performance of secondary vertices, being mandatory for reconstruction of heavy flavour vertices (c and b vertex). The impact parameter resolution in the transversal plane $\sigma(d_0)$ without

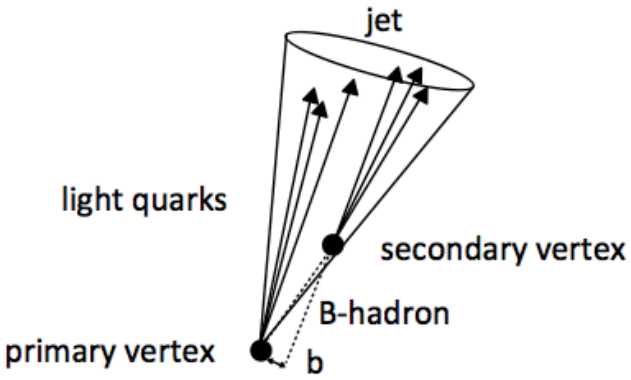


Figure 2.13: Determination of the impact parameter b of a track generated from a secondary vertex.

considering multiple scattering is given by [45]:

$$\sigma_{d_0} = \sqrt{\frac{\sigma^2}{(N+1)} + \frac{\sigma^2}{(N+1)}\frac{12N}{(N+2)}\frac{z_c^2}{L^2}}; \qquad z_c = (z_N - z_0)/2 \tag{2.26}$$

The achievement of good impact parameter resolution requires the use of fine segmented layers, large lever arm, and (considering multiple scattering) a small radius for the innermost detector layer and low material for the beam pipe and detector layers. The insertion of the IBL closer to the interaction point, and with lower material budget and an increased spatial resolution has improved the impact parameter resolution of the ATLAS detector by nearly 50% as shown in figure 1.9.

2.3.3 Requirements on detector design

The achievement of a good transverse momentum, vertex and impact parameter resolution by the tracking detectors brings to light several implications on the detector layout which are discussed here. Other requirements come from the environment, as in terms of radiation or

collisions per second.
The requirements to design a tracking detector for a HEP experiment are:

- large detector coverage in η
- a trade off the number of layers
- location of the first layer as close as possible to the interaction point
- high magnetic field
- low detector and beam pipe thickness
- fine detector segmentation, specially in the layers close to the interaction point
- detector radiation hardness up to the expected fluences
- excellent detector efficiency which ensures a measurement point per detector layer
- high speed (25 ns in-time)

Additionally to these design guidelines, possible defects in the detector layers need to be respected and avoided. There are two kind of defects sketched in figure 2.14 limiting the tracking algorithm performance: fake hits due to noisy pixels and non-detected hits so-called holes due inefficiencies. Additional measurement points due to fake hits originated from noise complicate the track reconstruction. Furthermore, the detector bandwidth can become a bottleneck due the existence of fake hits. The bandwidth is the limit of data that the chip can send per time. The transmission of fake hits may limit the transmission of real hits, leading to inefficiencies. The absence of a measurement point in a layer is called hole, and it is due to inefficiency. The number of holes and fake hits must be minimized.
A vertex detectors task is to give the best performance to avoid these defects, which is obtained by achieving high efficiency. High efficiency is achieved by a high signal and the ability to operate the detector at low threshold.

Signal

The detector signal amplitude is Landau-distributed and related to the amount of created electron-hole pairs as described in section 2.1.1. In a typical pixel detector of 200 µm thick silicon at the ATLAS IBL approximately 16 000 electron-hole pairs are generated at a bias voltage of 80 V by a MIP before irradiation. After an irradiation fluence of $5 \times 10^{15}\,\mathrm{n_{eq}cm^{-2}}$ the signal decreases due to bulk trapping to around 10 000 $\mathrm{e^-}$ at a bias voltage of 1000 V [51]. The radiation effects causing this degradation are explained in section 3.
To increase the detector signal and to cope with the 25 ns bunch crossing time full depletion is mandatory. In addition, a signal increase is achieved by a high ratio between the area of the charge collecting electrode and the detector segmentation size, which is called fill factor.

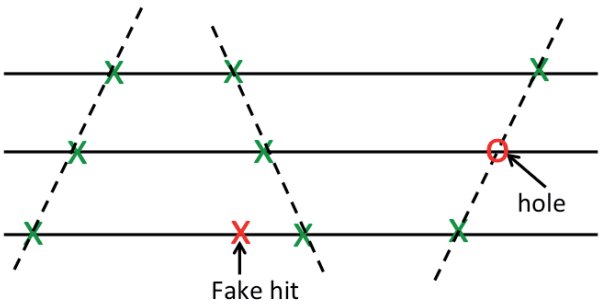


Figure 2.14: Schema showing a track reconstruction on a three layer detector. On the left, a single measurement is contained in each layer and the particle track is drawn. There are two kind of defects limiting the tracking reconstruction. On the middle, one of the layers see two hits, the one which is not a real hit is called fake. On the right, the absence of a point measurement in one of the layers is shown, which is called hole.

Threshold

The threshold is a set value to discriminate between a hit and the noise. A low threshold is required to increase the efficiency. The factor which limits the minimum threshold value is the noise. The noise is Gaussian-distributed around zero. The existence of noise increases the fake hit probability. Each pixel has a certain probability to exceed the threshold. Ideally the threshold value completely decouples signal from noise, while in reality there is some overlapping. The current fake hit probability in ATLAS is around 10^{-7} while the occupancy (real hit probability) is 10^{-4}. This results that one out of 1000 hits is a fake hit. To achieve a low threshold, low noise is required. The noise in a typical pixel detector of the ATLAS IBL is about 130 e^- and the threshold is set to 2500 e^-. The noise after irradiation increases up to around 150 e^- and the threshold is reduced to 1600 e^- [51] to cope with the decrease signal. To decrease the detector noise low capacitance and low leakage current are required. Thus, a high Signal-to-Noise Ratio (SNR) factor is required to achieve high efficiency.

Chapter 3

Radiation damage in silicon detectors

Silicon detectors are affected by two radiation damage mechanisms, namely displacement damage and ionization damage. Both damages limit the use of silicon detectors in the HEP experiments. The displacement damage appears when the incident radiation displaces silicon atoms from its lattice sites. It is caused by hadrons. The resulting defects alter the electrical characteristics of the crystal, and in consequence the detector properties. The displacement damage is negligible at the surface and in the silicon dioxide, since the atom displacement in an amorphous material does not change its properties substantially. However, the displacement damage is the main reason of permanent damage in the silicon bulk (crystalline lattice). The ionization damage occurs when the incident radiation loses its energy by ionizing electrons from the atoms lattice. The resulting defects alter the electrical parameters of transistors and other elements affecting in consequence the electronics performance of the detector. The ionization damage is negligible in silicon bulk but important in the silicon dioxide layers. Therefore the ionizing damage is crucial for the electronic readout chain and sensors, which contain silicon dioxide. The ionization damage is caused by ionizing radiation like electrons, photons, or even neutrons.

This chapter covers a description of both kind of damage and their implications on the detector properties, since the core of this thesis is the validation program of a new depleted monolithic pixel sensor, in which electronics and sensor part are contained in the same piece of silicon. Section 3.1 describes the damage mechanism on MOSFET transistors, as they are the building block of any readout chain. Subsequently, the changes in MOSFET transistors and in the detector properties due to the ionizing radiation is explained for both, bulk and Silicon-On-Insulator (SOI) transistors. Section 3.2 gives a short overview of the radiation damage mechanisms in the bulk silicon and subsequently focusses on the changes in the detector properties due to radiation damage.

3.1 Radiation induced damage in transistors

The ionizing damage is a cumulative effect due to the energy deposited by the particles passing through. Therefore the deposited energy is given in TID, whose typical units are 1 Gy = 100 rad.

3.1.1 Damage mechanism of ionizing radiation

The ionizing radiation damage generated in a MOS structure can be explained in four steps (1) charge generation and recombination in SiO_2, (2) hole transport in SiO_2 , (3) deep hole trapping near Si/SiO_2 interface, and (4) radiation-induced interface traps. Those processes are indicated in figure 3.1 [52] for when a positive voltage is applied at the gate. They are explained in detail in this section.

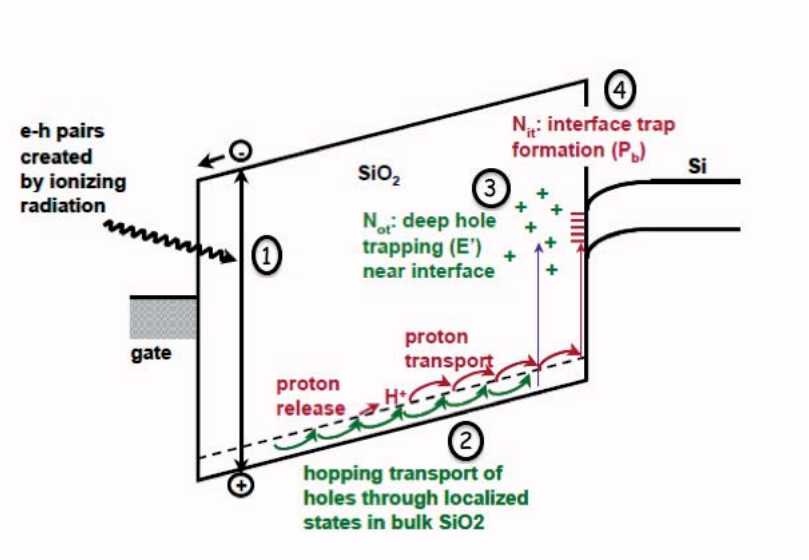


Figure 3.1: Sketch of ionizing-radiation-induced effects in a MOS structure for a positive bias voltage applied at the gate [52]. The effects can be summarised in four steps: e-h pair generation due to the ionizing radiation, hole transport, deep hole trapping, and interface trap formation.

Electron-hole generation, recombination and mobilities

When ionizing radiation traverses a MOS structure, electron-holes pairs are created in the silicon dioxide. The necessary amount of energy to create an electron-hole pairs in a SiO_2 film is 17 eV [56].
Some of the generated electron-holes recombines within 1 ps. The amount of recombined carriers depends on the electrical field and the incident particle type [52].

The rest of the electrons and holes left from the recombination are free to move in the oxide. The mobility of electrons in SiO_2 is $20\,cmV^{-1}s^{-1}$ at room temperature [57, 58], while the hole mobility is typically $10^{-4}\,cmV^{-1}s^{-1}$ to $10^{-11}\,cmV^{-1}s^{-1}$ [59, 60] depending on the temperature and field. As a consequence, the holes are relatively static on the SiO_2 if compared with electrons. The fast mobility of electrons in SiO_2 and their small long-term trapping (six orders of magnitude less than holes) in SiO_2 are the two factors why electrons do not play a significant role in the response of MOS structures after irradiation [52].

Hole transport in silicon dioxide

The hole transport is an anomalous process whose details are out of the scope of this work. Thus, a qualitative description is given here. In presence of an electrical field, the holes left from the initial recombination transport through the oxide either towards the gate (for a negative V_g) or towards the SiO_2-Si interface (for a positive V_g). The holes movement create a local potential field distortion. This distortion increase the trap depth at the localize places, tending to confine the holes within its vicinity, sometimes referred as self-trapping or polaron [52]. In that way, the holes move, and the distortion makes the effective mass of holes increase and their mobility decrease. The movement of holes between localized states is called hopping transport in SiO_2 [52, 61, 62].

Deep hole trapping at the oxide

A missing oxide atom in the amorphous SiO_2 results in a localized energy level of about 3 eV above the valence band. This results in an electrically neutral trapping center for holes. This trapping center are homogeneously distributed in the SiO_2 volume. However, in the vicinity of the interface (5 − 20 nm) there is normally a higher deficiency of oxygen, leading to a higher density of hole trapping centers [52]. The application of a positive voltage to the transistor gate implies the movement of the radiation-induced holes towards the $SiO_2 - Si$ interface. In its approach to the interface a fraction of them will be trapped by the trapping centers, mostly close to the interface. In this way, a positive space charge is built. The cross-section of hole capture depends on the applied electrical field and the fabrication process.
The holes trapped in the SiO_2 after irradiation are not permanently trapped. They disappear from the oxide over time from milliseconds to years. There are two processes explaining this annealing of oxide traps: the tunnelling of an electron from the silicon substrate and the thermal excitation of an electron from the valence band [52]. The later one is accelerated with increasing temperature.

Radiation-induced interface traps

At the SiO_2- Si interface the transition between amorphous and crystalline material results in uncompleted or dangling bonds. These dangling bonds are the origin of the so-called interface traps [52]. The dangling bonds build energy levels in the silicon band gap. Depending on the Fermi Level and thus, the doping of the silicon (n or p) holes or electrons are captured. The interface traps are located within one or two atomic bond distances (0.5 nm) from the silicon lattice [52].

The described interface traps are present before irradiation and influence the transistor performance. To avoid that, the manufactures introduce impurities (H ions) to the interface during the production process. The introduced H ions fill the dangling silicon bonds ($Si \cdot + H \rightarrow$ Si-H) and therefore reduce the density of traps. The filled bonds are also called passivated dangling bonds. The radiation induced holes mentioned above react with the passivated dangling bonds. This breaks the $Si - H$ bonds and thus the interface traps get re-activated due to ionizing dose.

As the radiation induced holes are necessary to re-activate the interface traps, these generally appear at higher TID. The electron or hole trapped at the interface traps builds up a space charge with the sign depending on the silicon type.

There are many variables affecting the quantity of the built interface traps. Some of them are: the electrical field applied during the irradiation, the temperature or energy of the incident radiation. As well, the device production process has a strong influence, in particular the amount of hydrogen introduced, and the material used building the gate (metal versus silicon) or the thickness of the oxide [52]. The interface traps do not anneal at room temperatures, but only occurs for T>100 °C and it is very sensitive to how the oxide was processed [52].

3.1.2 Changes in transistor properties

The generation of trapped holes in the SiO_2 and the activated interface traps lead to the device degradation and failure. Concretely, the electrical parameters of the transistors will shift.

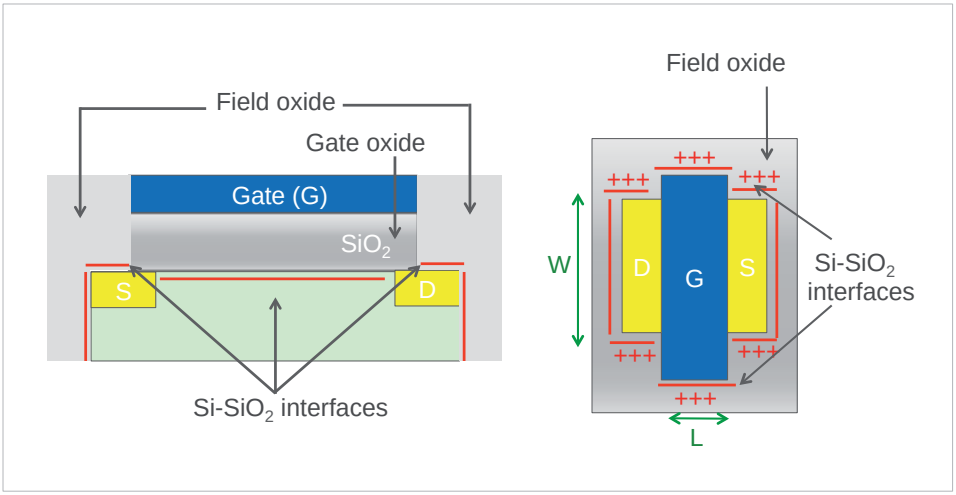


Figure 3.2: Schematic cross section (left) and a top view (right) of a bulk MOSFET transistor. The silicon dioxide and interface regions are pointed out.

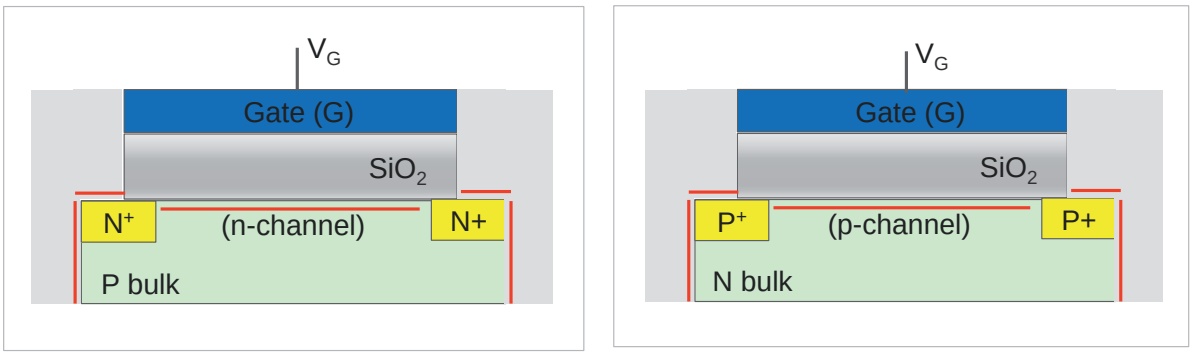
The cross section and the top view of a bulk transistor where the zones containing SiO_2 and the $SiO_2 - Si$ interfaces are pointed out is shown in figure 3.2. The SiO_2 located below the gate is called gate oxide and the one located in between the structures is called field oxide. In advanced technologies with very thin gate oxide, the response is dominated by the effect at the field oxide and not by the gate oxide. The SiO_2-Si interfaces are marked in red.

To validate any device or technology for its future use in a LHC experiment, the parameters shift must be quantified up to the dose that the detector will accumulate at the LHC experiment.

The shift value is a crucial information for the chip designers. Ideally the electrical parameters shift due to TID are within the fabrication process variation. In such case, the designers can easily work in the technology for further prototyping. Subsequently, complex structures as the whole chip can be further tested to other effects like Single Event Effects (SEE) or Latchup [52]. The following subsections explain the expected shift in the electrical parameters.

Changes in transistors characteristics

The transistor electrical parameters are: threshold voltage, leakage current, transconductance and mobility. A description of them and their shift due to ionizing radiation is given here for bulk and SOI transistors. Figure 3.3 illustrates the cross section of a nMOS and an pMOS transistor to guide the reader in the coming explanations.



(a) (b)

Figure 3.3: Cross section view of a (a) nMOS transistor and a (b) pMOS transistor where SiO_2 is drawn on grey and Si – SiO_2 interfaces on red. The dimensions are not to scale.

- **Threshold voltage shift**
  The threshold voltage of a MOS transistor is the minimum amount of voltage applied to the gate for creating a conduction channel and allowing a current flow in the transistor channel. The threshold voltage shift ΔV_{th} due to TID is given by two contributions, due to the oxide charges (ΔV_{ox}) and interface traps (ΔV_{it}):

$$\Delta V_{th} = \Delta V_{ox} + \Delta V_{it} \tag{3.1}$$

  Let's consider a nMOS transistor in which negative bias at the gate is applied as the one shown in figure 3.3a. For low TID the electrical field of the positive charges trapped in the gate and field oxides attract negative charges to the Si-SiO_2 interface. As a consequence, the amount of voltage which needs to be supplied at the gate for making the

channel conductive is smaller than before irradiation. Thus, the threshold voltage decreases. For high TID the interface traps get re-activated. As a consequence, in a nMOS transistor the electrical field of the resulting negative space charge compensates the field of the positive charges trapped in the SiO_2. This leads to an increase of the threshold voltage. Therefore, the threshold voltage of a nMOS transistor is expected to shift in a rebound way.
In pMOS transistors both effects increase the threshold voltage. In the oxide as well as in the interface traps, holes are captured, and only a positive space charge appears. The electrical field pushes away holes from the p-channel. Thus, a higher voltage needs to be supplied to make the channel conductive.

- **Leakage current shift**
  The leakage current is the existing current when the transistor is off, therefore is not current drifted in the channel but mainly along the field oxide due to defects. The leakage current shift ΔI is also given by the sum of the ΔI_{ox} and ΔI_{it} contributions.
  In a nMOS transistor at low TID, the positive charges in the field oxide attract negative charges to the Si-SiO_2 interfaces creating an induced negative channel. Hence, the leakage current increases. At high TID, once the interface traps get activated, the carriers at the induced channel (leakage) get trapped. Thus, the leakage current tends to reduce.
  For a pMOS transistor, the leakage current remains constant. The creation and variation of an induced channel of electrons does not affect a pMOS transistor performance, since its current is formed by holes.

- **Mobility and transconductance**
  The transconductance (g_m) is the derivative of the I_{ds} over V_{gs}, therefore the amplification of the transistor, while the mobility is related with the charge carriers movement. The mobility decreases during irradiation essentially due to the increase of the interface traps, since the carrier motion close to the Si-SiO_2 interface determines the conduction in MOS transistor. The degradation of the mobility in turn gives origin to a degradation of the transconductance. The decrease of the transconductance reduces the driving capabilities of the device.

The impact of these effects depends on the transistor geometries. As an example, a transistor can be designed in different geometries in order to reduce its leakage current, for example the enclosed transistors were developed for such purpose. They definitely have better performance in terms of leakage than linear transistors before and after irradiation, but they also need more space.
The bias conditions of the gate during irradiation are crucial since they will influence the quantity of charges trapped in the Si-SiO_2, the location of the trapped charges, as well as the electrical field at the Si-SiO_2 interface. In a nMOS transistor in which $V_g > 0$, the positive voltage at the gate will push the generated holes towards the interface. In a nMOS transistor in which

$V_{gs} = 0$, the holes are rather being distributed all over the oxide. As a consequence, an nMOS transistor irradiated under a bias voltage $V_{gs} = 0$ presents a smaller shift in its parameters than the same nMOS irradiated under a bias $V_{gs} > 0$. Both cases are shown in figure 3.4. However for pMOS transistors it is not clear which are best or worst bias conditions, with the result that it is technology dependent [52]. A more extensive description of the TID effects on bulk transistors is given in [52].

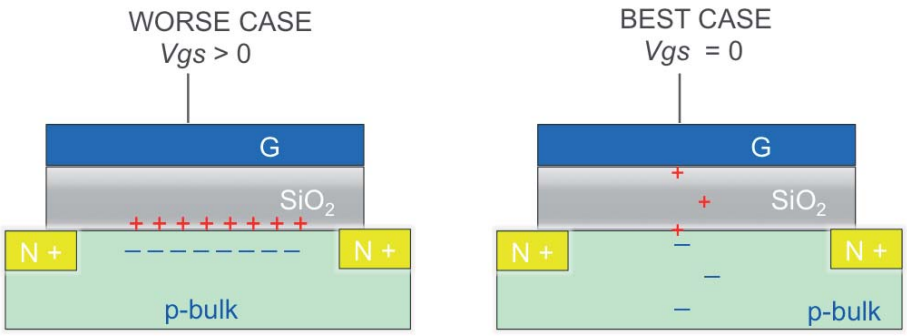


Figure 3.4: Impact of the bias conditions on nMOS transistors during X-ray irradiation. Schematic of a cross section of a nMOS transistor being irradiated at (a) V_gs >0 which pushes the generated holes to the interface and generates more damage and at (b) V_gs =0 where the generated holes are homogeneously distributed in the SiO_2.

Changes in SOI transistor characteristics

SOI transistors were developed on the 1950s. They emerged from the idea to separate the active volume for carrier transport ($0.1 - 0.2\,\mu m$) from the bulk silicon substrate usually used as mechanical support by an oxide layer. This oxide layer is commonly known as Buried OXide (BOX). Since then, they were extensively used, first on military applications and later on a wide-scale consumer applications (microprocessors, SRAMs...). Figure 3.5 shows a cross section view of a SOI transistor where zones containing either oxide and an interface are pointed out. SOI devices exhibit major advantages over bulk devices as superior Single Event Upset (SEU) tolerance, better noise isolation, speed and density [63, 64]. Its development for HEP and X-rays applications was first investigated by Japanese colleagues from OKI manufacture (the actual LAPIS). In the LAPIS SOI technology the BOX of a few hundred of nanometers width is located at a few nanometers from the transistors gate [65]. Thus the transistor body is fully depleted, known as FD SOI.

The same type of oxide is normally used for both transistor types, bulk and SOI. Therefore, in a first approach, one could just transcript to here the effects of the bulk transistors. However, on SOI transistors the SiO_2 layer of the BOX needs to be considered. The BOX inclusion makes SOI devices more sensitive to TID damage due to the build-up of positive charges in the BOX during irradiation [66], [67].

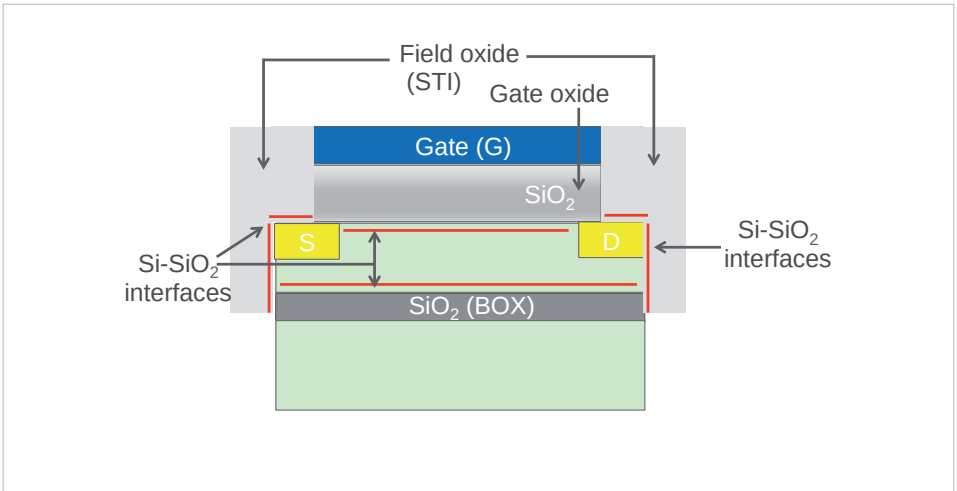


Figure 3.5: Cross section view of a MOSFET transistor build on SOI technology. The SiO_2 and the $Si - SiO_2$ interfaces are pointed out in grey and red, respectively.

The accumulated charges in the BOX lead to a significant influence on the transistor, with a significant shift after a few hundred krad of accumulated radiation as has been observed and published [68], [69]. On the other hand, it has been also observed that the applied electric field in the silicon bulk below the BOX also affects the transistors operation, which is called Back Gate Effect [70].

New process and device design techniques are being applied since the last years in order to reduce the amount of positive charged trapped in the oxide and mitigate the effect of the ones trapped. For example, in order to mitigate the Back Gate Effect, a second BOX is introduced and the potential of the silicon in between is used to to cancel the field of the trapped charges and the Back Gate Effect [70, 71]. An extensive description of the TID mechanisms and effects on SOI transistors is covered in [72], [73].

3.2 Radiation damage in the silicon bulk

The displacement of atoms in the silicon bulk causes changes in the detector properties such as the leakage current or the effective doping concentration. These changes are the main limiting factor for operating the detectors at high fluencies as the ones at LHC. An introduction to the damage mechanism and the NIEL hypothesis is given in the following section. Subsequently, the resulting changes in the detector properties are described.

3.2.1 Damage mechanism and defect generation

The interaction of high energetic particles (mainly hadrons) with a silicon crystal may displace a silicon atom from its lattice site, resulting in a left vacancy and a silicon interstitial, also

called Frenkel pair. The displaced atom is called Primary Knock-on Atom (PKA) [74]. The necessary energy to displace an atom from its lattice site (displacement threshold) is $E_d \approx 20\,\text{eV}$ [75].
The generated vacancies and interstitials are mobile at room temperature. Simulations have shown that about 60% of the overall Frenkel pairs and from 75% to 95% in highly disordered regions will recombine [74]. The left vacancies and interstitials move through the silicon lattice interacting among themselves and with silicon impurities. This results in the point defect generation. When the imparted energy to the PKA is high enough, the PKA moves through the lattice. Its energy loss along its path consists of two contributions: ionization energy loss and further atoms displacement. The ionization loss does not lead to a change in the lattice, since it is reversible. On the other hand, a consecutive displacement of atoms give rise to a PKA cascade, creating zones with very high density of the vacancies-interstitials. This agglomeration of defects is called cluster. Figure 3.6 [74] shows Monte Carlo simulations of the track of a PKA atom with a primary energy E_R =50 keV, the average kinetic energy that a 1 MeV neutron transfers to a PKA. The PKA transfers its energy over a distance about 1000 Å.

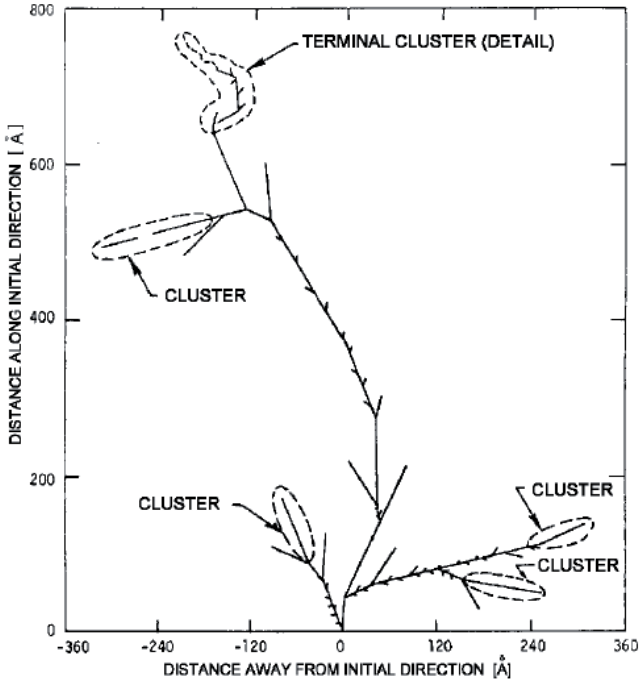


Figure 3.6: Monte Carlo simulations of a PKA track with a primary energy E_R =50 keV [74]. It is observed that point defects and defect agglomerations called clusters are formed.

Point defects and clusters are responsible for the several damage effects in the bulk of silicon detectors. They induce additional energy levels in the band gap.

3.2.2 The NIEL hypotesis

The interaction of particles with the silicon crystal depends on the kind of particle and on its energy as described in section 2.1. In the same way, the defect kind and the lattice damage depends on the particle type and its energy.

The non ionizing loss of energy is mainly due to Coulomb interactions for charged particles, and mainly due to elastic scattering with nuclei for neutrons. The necessary kinetic energy to produce a Frenkel pair and a cluster for different particles is shown in table 3.1. The data were calculated using the maximum kinetic energy transferred by the incident particle, the displacement threshold and the cluster threshold given in [74]. It is observed that neutrons need less energy than electrons to create a Frenkel pair, or a cluster. Therefore, different kind of particles create different defects on the lattice.

	E_K (Frenkel pair)	E_K (cluster)
Neutrons	$\sim 185\,\text{eV}$	$\sim 35\,\text{keV}$
Electrons	$\sim 255\,\text{eV}$	$\sim 8\,\text{MeV}$

Table 3.1: Kinetic energy E_K needed to create a Frenkel pair and a cluster for different particles type.

Additionally the same particle at different energies produces different type of damage. The proton damage is dominated by Coulomb interactions at low energies creating mainly point defects (much more than neutrons do). However in the range of GeV the contribution of Coulomb interactions become very small and it is dominated by nuclear reactions. The PKA atom is able to split the nucleus directly, creating a mixing between cluster damage and point defect damage. Figure 3.7 [75] shows a simulation of defect generation for 10 MeV protons, 24 GeV/c protons and 1 MeV neutrons.

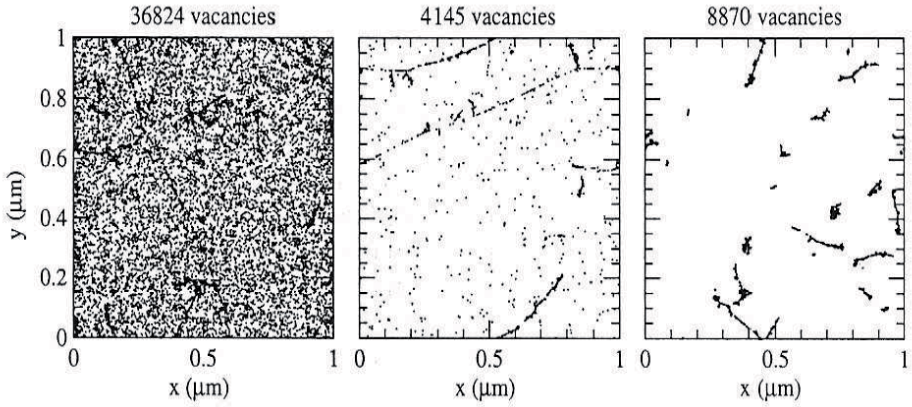


Figure 3.7: Vacancies distribution caused by 10 MeV protons (left), 24 GeV/c protons (middle) and 1 MeV neutrons on silicon material. [75].

The NIEL hypothesis allows comparing the damage caused by different particles with different energies. The assumption of the NIEL hypothesis is that the displacement damage scales with the amount of energy imparted in the displacing collision. The spatial distribution of the defects within the cascade and the annealing are not taken into account in this formalism. The created displacement damage cross section or damage function is given as:

$$D(E) = \sum_{\upsilon} \sigma_{\upsilon}(E) \int_0^{E_R^{max}} f_{\upsilon}(E, E_R) P(E_R) dE_R \tag{3.2}$$

The index υ indicates all possible interactions between the approaching particle of energy E and σ_{υ} is the cross section of those reactions. $f_{\upsilon}(E, E_R)$ gives the probability to generate a PKA and $P(E_R)$ is the so called Lindhard partition function [74] used to calculate the amount of damage from the deposited energy. Figure 3.8 [75] shows the displacement function versus energy for protons, neutrons, pions and electrons.

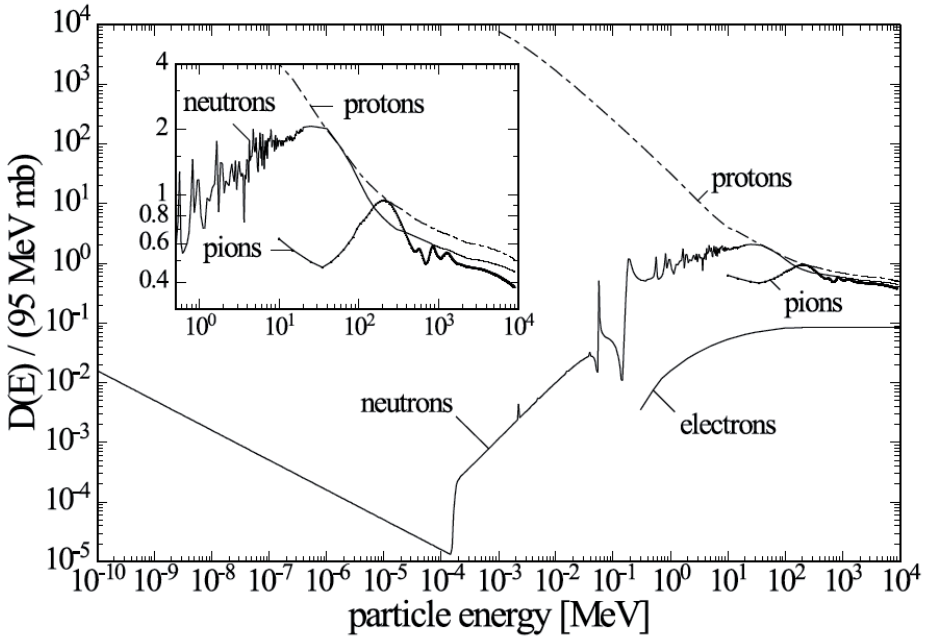


Figure 3.8: Displacement damage function D(E) versus particle energy for protons, neutrons, electron and pions. D(E) is normalized to 95 MeVmb which is equivalent to 1 MeV neutron. [75].

To compare the damage generated by different particles it needs to be scaled to 1 MeV neutron. The hardness factor k is defined for that purpose [74].

The usual unit system for fluence is [1 MeVn_{eq} cm^{-2}], which is extensively written as [n_{eq} cm^{-2}]. This short notation will also be used in this work. The full picture of defect types, their nature, and their electrical properties is a very complex subject which are out the scope of this work. Further explanations of these phenomenons are given in [74, 75].

3.2.3 Changes in detector properties

The changes in the detector properties due to the bulk damage can be summarized as follows:

- **Trapping**
  The radiation induced energy levels in the band gap act as charge carrier traps [74]. As a consequence, the mean life time of the charge carriers and thus the signal decreases. In a typical pixel detector of 200 µm thick silicon at the ATLAS IBL approximately 16 000 electron-hole pairs are generated at a bias voltage of 80 V by a MIP before irradiation. After an irradiation fluence of 5×10^{15} $n_{eq}cm^{-2}$ the signal decreases due to bulk trapping to around 10 000 e^- but after increasing the bias voltage to 1000 V [51].

- **Leakage current**
  The leakage current is an important property of silicon detectors as described in section 2.2.2. The leakage current, generated by the generation centers in the forbidden area, is desirable to keep it as small as possible. The radiation generates additional energy levels in the band gap leading to an increase of the leakage current [74]. The leakage current increases with the fluence (ϕ) as follow:

  $$\Delta I_{vol} = \alpha \cdot \phi \tag{3.3}$$

  where ΔI_{vol} is the change in the leakage current per volume due to irradiation and α is the damage constant, which is temperature dependent. An usual value of the leakage current for a typical pixel sensor in ATLAS is about 400 nA before irradiation. After a fluence of 6×10^{15} $n_{eq}cm^{-2}$ the leakage current increased to about 50 µA (at 120 V) [51]. The consequences of a too high leakage current are an increase of the electronic noise and of the power dissipation. The latter one increases the sensor heat up, which must not exceed the specifications of the cooling system.

- **Effective doping and full depletion voltage**
  The additional energy levels introduced due to radiation are mostly located at the middle of the band gap [74]. They act as acceptor levels in the silicon lattice. The N_{eff} dependence as a function of the fluence (ϕ) is parametrize as:

  $$N_{eff}(\phi) = N_{eff,0} \cdot e^{-c\phi} + \beta\phi \tag{3.4}$$

  where c and β are constants. The increase of the effective number of acceptors causes an increase in the effective doping concentration N_{eff} on a p-bulk sensor accordingly with equation 3.4. As a consequence the material resistivity ρ decreases (see equation 2.11), and according with equation 2.12, a higher voltage needs to be applied to fully deplete the sensor.

- **Acceptor Removal**

  During the last few years a new effect has been observed in low resistivity (10-20 Ω cm) p-type silicon material. Experimental measurements have shown an increase in the signal after irradiation up to 2×10^{15} $n_{eq}cm^{-2}$ [76]. This is explained by the so called Acceptor Removal Effect [76]. Low resistivity p-type silicon presents a large number of acceptors in the lattice. The acceptor removal effect claims that those acceptors are removed by radiation. A new term is added to equation 3.4, which results into:

  $$N_{eff}(\phi) = N_{eff,0} - N_C \left(1 - \cdot e^{-c\phi}\right) + \beta\phi \tag{3.5}$$

  Thus, according to equation 2.11 the resistivity increases initially due to the Acceptor Removal effect. At higher fluences the previously described acceptor generation dominates and the resistivity decreases.

This effect has not been observed before since in the high resistivity materials (1-5 kΩ cm) used for sensors up to now, only a small number of acceptors is present. Figure 3.9 [77] shows a simulation of the signal of a MIP versus fluence when both effects, the acceptor level created by the radiation and the acceptor removal effect are taken into account. The initial decrease of the signal corresponds to the signal loss due to trapping. The signal increase as a function of the fluence is due to the Acceptor Removal Effect, which depends on the material resistivity. The decrease is due to the described acceptor levels introduced due to radiation. Choosing carefully the initial number of acceptors in the silicon (and thus the resistivity) provides the possibility to use this effect in order to achieve a resistivity above the initial value during the full lifetime of the detector.

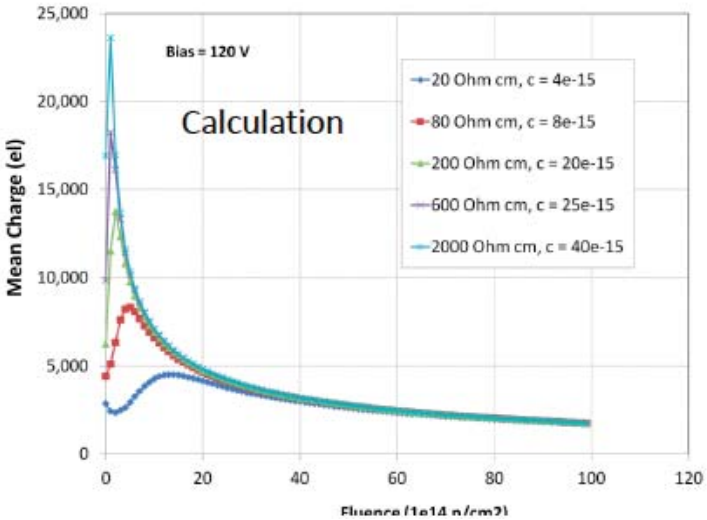


Figure 3.9: Simulated collected charge versus fluence at different resistivities of the p-bulk silicon when the Acceptor Removal Effect is taken into account [77]. For low resistivities the initial increase of the collected charge with fluence due to the Acceptor Removal Effect is visible.

Chapter 4

Pixel detectors: Developments and Trends

The current architecture of tracking detectors at the LHC experiments are hybrid pixel detectors [78], in which the sensor and the readout Integrated Circuit (IC) are separate entities. Hybrid pixels are so far the only viable approach to cope with the particle rate and radiation environment of the LHC pp-experiments. The requirements for the future HL-LHC ATLAS Inner Detector were summarized in section 1.4. These stringent requirements have opened a technological challenge and are driving a new era of developments on different pixel detector types.

The current hybrid pixel concepts used in ATLAS and CMS are unrivalled in terms of rate and radiation tolerance positioning them as a good candidate for HL-LHC. However, their material budget, production complexity, and their cost have boosted the development of new module concepts. Since several years an international community called ATLAS CMOS collaboration is seeking for new radiation-hard pixel sensor concepts, both hybrid and monolithic, based on industrial CMOS processes for the ITk pixel layers [79, 80, 81].

The current trends and developments of pixel detectors in ATLAS towards the HL-LHC can be subdivided in three categories: hybrid pixel detectors for the inner pixel layers, active hybrid pixel, and monolithic CMOS detectors for the outer pixel layers as sketched in figure 4.1. The so called semi-monolithic detectors are still hybrid detectors, but amplifier stages are

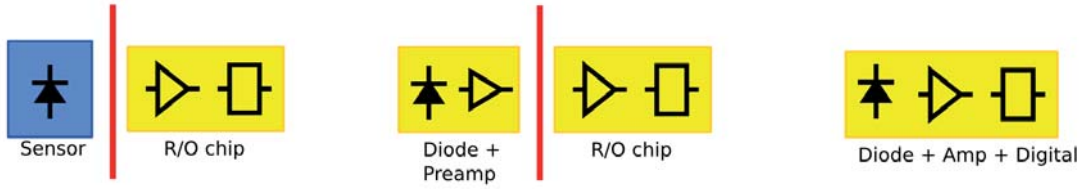


Figure 4.1: Pixel development categories (a) hybrid pixel sensors (b) active hybrid pixel sensor or semi-monolithic and (c) monolithic pixel sensors [82].

implemented in the sensor part. Monolithic pixel detectors combine the sensor and the readout

Integrated Circuitry (IC) in a single piece of silicon.

An overview to the current developments and trends of Pixel Detectors for the ATLAS HL-LHC are given in this chapter. Section 4.1 describes the current options and their developments in the hybrid pixel sensor approach. New approaches to achieve cheaper hybrid pixel detectors concepts are also described. Section 4.2 reviews the different CMOS pixels under instigation for the ATLAS HL-LHC upgrade, which is divided into: high resistivity CMOS, high voltage CMOS, and monolithic active pixels on SOI. The monolithic active pixel approach is investigated in this thesis. The investigated prototypes are described in detail in section 4.2.3.

4.1 Hybrid pixel detectors

Hybrid pixel detectors [78] are a mature and established technology whose capabilities have been demonstrated during the last five years of LHC operation. An hybrid detector is composed of two separated entities: a R/O-chip and a sensor as depicted in figure 4.2 [78]. The interconnection between them is so far done by conductive balls, so-called bump-bonds. This process is expensive and limits the minimal pixel size. The hybrid pixel technologies have many advantages mainly due to its split functionality (sensor and chip). The sensor silicon is specially optimized to stand radiation by oxygen enriched high resistivity silicon and the readout chip to digest and process high rates (~MHz/ mm^2).

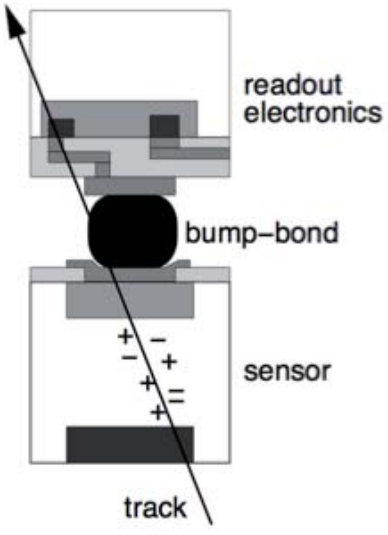
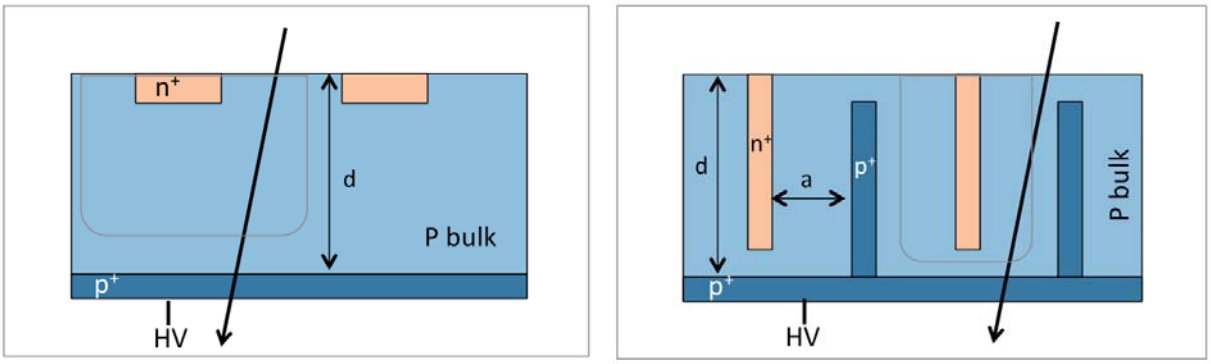


Figure 4.2: Schematic cross section of an hybrid pixel sensor where the sensor and the readout integrated circuit are connected by bump bonding [78].

Two types of sensors lead the hybrid approach for pp-collision experiments: planar and 3D silicon sensors whose pixel cross sections are sketched in figure 4.3. Planar silicon sensors

[34] are a well established technology where the depletion depth is coupled to the sensor width d. 3D silicon sensors [42] contains electrodes vertically placed, which decouples the depletion depth a from the sensor width d. This leads to the following advantages: fast and full charge collection at low bias voltages, more radiation tolerance since $a < d$. However, the fabrication of 3D sensors is a non-standard process, increasing its cost.



(a) (b)

Figure 4.3: Pixel cross section of (a) a planar silicon sensor whose drift length is coupled to the sensor thickness d and (b) a 3D silicon sensor where the drift length a is independent of the sensor thickness d.

The current ATLAS Pixel Detector is fully made of hybrid pixels. Layer 0, Layer 1, and Layer 2 are loaded with planar silicon sensors bumped to a R/O-chip (so called FE-I3 [83]). The IBL, described in section 1.3.3, was loaded with 75% of planar silicon sensors with slim edges and with 25% 3D silicon sensors, located at the end of the IBL staves [39, 33]. 3D silicon sensors were for the first time installed in a LHC pp-experiment [42]. The IBL sensor technologies were bonded to a new R/O-chip (FE-I4 [84]). Both Planar and 3D sensors are proven radiation hard up to $5 \times 10^{15}\,\mathrm{n_{eq}cm^{-2}}$, efficiency above of 97 %, and spatial resolution of the order of 10 µm [51]. They stand as a mature and established option for the future ATLAS upgrade.
The R&D Planar and 3D Collaborations are actively working on proving the sensor performances in the HL-LHC environment [85, 86]. The R/O-chip for the HL-LHC is being addressed by the R&D Collaboration RD53, which aims for a pixel R/O-chip in 65 nm CMOS technology [87, 88]. This chip will be able to digest a hit rate of $10\,\mathrm{MHz/\,mm^2}$ and tolerate an ionizing dose of 1 Grad.

The hybrid choice has some limitations or disadvantages. They constitute a relatively large material budget, typically more than 3% X_0 per layer in ATLAS and CMS. This is due to the different components, but significantly to the sensor, and to the R/O-chip thickness. The current state of the art hybrid pixel detector modules (IBL) have 0.25-0.29% X_0, 0.18% X_0, and 0.27% X_0 in sensor, R/O-chip and passive components, respectively [89]. Additionally, bump-bonding is an expensive process and it limits the lowest pixel size to about 50 µm. Furthermore,

in the current state of the art hybrid pixel detector modules the R/O-chip needs to be larger than the sensor in one of the directions in order to provide signal and power to it (wirebond pads). This leads to an additional material, dead area, and no possibility of wafer to wafer interconnection. In addition, in the current hybrid modules, the cooling to the sensor is not provided directly to it, but through the R/O-chip and the bumps. The module production is a complex multi-step process, leading to high failure rate and price.

Several alternatives are coming into focus with the aim of addressing the limitations just mentioned and keeping the advantages of hybrid detectors. R&D efforts on different hybridization techniques are taking place. Some of them aim to go from chip-chip bonding to chip-wafer or wafer-wafer. Other R&D projects focus on 3D-integration. A separate wafer for the analogue and the digital part enables reducing the space used by the electronics. This allows smaller pixel sizes. An arising R&D investigates a new module concept. In this approach, the R/O-chip does not need to exceed the sensor in any direction, and the wirebond pads are connected to the bottom of the R/O-chip by Through-Silicon Vias (TSV). This enables wafer to wafer connections, cooling directly on the sensor side, and reduction of dead areas. The readout chips become four side abutable, which enable the production of bigger sensor sizes. Furthermore, the ATLAS CMOS collaboration is seeking new radiation-hard pixel sensor concepts, both hybrid and monolithic, based on industrial CMOS processes for HL-LHC.

4.2 CMOS pixels for the ATLAS HL-LHC upgrade

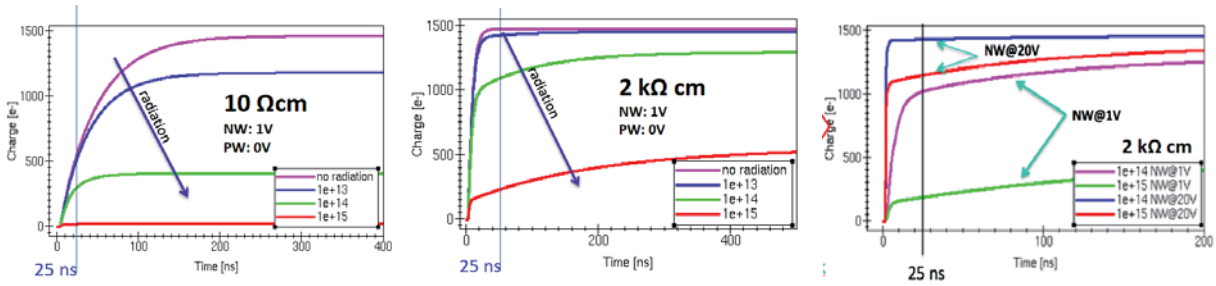
The interest of CMOS-based pixel sensors for HL-LHC have emerged due to their potential low cost in comparison with standard hybrid pixels and to the large area that the outer layers have to cover. CMOS-based pixel sensors provide the possibility to implement a sensor collecting the charge by drift in a depleted region, and allows logic implementation in the same silicon tile. That enables the use of capacitive coupled connections between sensor and front-end electronics, replacing the current bump-bonding process. Three main benefits could result from that: less cost, less material budget, and smaller pixel size fabrication, which improves the spatial resolution of the detector layers. Additionally, the CMOS-based sensors are an industrial process, promising a higher production yield and cheaper sensors. It is possible to produce the sensors in small thickness (50-80 µm) since they do not need to be handled and heated for the connection with the front-end electronics. To assess the feasibility of such sensors, two effort are ongoing within the ATLAS ITk: the CMOS Strip Project [90] towards CMOS strips and the CMOS Pixel Demonstrator Programme towards CMOS Pixels.

The target for CMOS Pixels in ATLAS is:

- Depletion zone of about 40-80 µm together with a similar sensor thickness to achieve a fully depleted sensor, ensuring charge collected by drift.
- Large signal of about $\sim 4000\,e^-$.
- Fast charge collection (within 25 ns) to ensure excellent in-time efficiency.

- A short collection path to avoid signal loss due to trapping after irradiation.

Recent simulations [82] have shown that these goals can be addressed by the proper combination of: resistivity, voltage and fill factor. Figure 4.4 [82] shows the collected charge versus the charge collection time at different fluences on a) a low resistivity substrate b) a high resistivity substrate and on c) a high resistivity substrate with high voltage. The earlier introduced Acceptor Removal Effect is not considered in this simulation. The combination of high resistivity substrate and the application of high voltage leads to higher collected signal within 25 ns.



(a) (b) (c)

Figure 4.4: Simulation of the collected charge versus charge collection time at different sample fluences on a (a) low resistivity substrate (b) high resistivity substrate and (c) high resistivity substrate with high voltage process [82]. The combination of high resistivity and high voltage leads to a higher collected charge.

The ultimate goal of the CMOS Pixel Demonstrator Programme is to prove the CMOS-based sensors feasibility for the pixel layers of the future ITk, and to be considered as an option in the ATLAS Technical Design Report (TDR). A first phase of the Demonstrator Programme consists of the testing of small test-chip on many different technologies to then identify the most promising one. Subsequently, a second phase aims to the submission of engineering runs with the 2-3 most promising technologies on a large chip. At the writing time, AMS on 350 nm, LFoundry on 180 nm technologies, and the XFAB technology tested in this thesis have been chosen for being produced in large scale. Their submissions are happening in the coming months. Further on, the goal is to demonstrate:

- Feasibility on the construction and operation of a pixel module of 1-4 cm^2.
- Performance when produced as an hybrid module and also monolithic sensor.
- Characterization with pulses, radioactive sources, and test beam on unirradiated and irradiated up to 10^{15} $n_{eq}cm^{-2}$.

The ultimate achievement the collaboration aims for is to provide this on a monolithic chip that unites sensor and readout circuitry. Since a radiation hard and fast Monolithic Active Pixel Sensor (MAPS) is complex and a big challenge, intermediate steps are being investigated

first. This corresponds to the so-called semi-monolithic approach in figure 4.1, in which a spatial separation between the high-speed digital readout and the analogue pre-amplifier blocks integrated in the sensor. Since a radiation-hard MAPS have immense potential to increase the performance of the detector, they are also being investigated. The current development lines investigated within the Demonstrator Programme are divided into: High Voltage CMOS, High Resistivity CMOS and Monolithic CMOS on SOI pixels.

4.2.1 HV-CMOS pixel sensors

CMOS pixels with a depletion zone was first implemented by I. Peric [91] using a high voltage technology, allowing the application of up to 100 V. This approach is so called High Voltage CMOS (HV-CMOS). Figure 4.5 shows the pixel cross section of a generic HV-CMOS structure. Full CMOS circuitry is housed in a large n-well which acts as a charge collection electrode. Such a big n-well leads to a high fill factor (close to 100%) at the price of increasing the capacitance of the pixel. In this approach, the analogue pre-amplifier blocks are integrated in the sensor. Thus, the output is an already amplified signal.

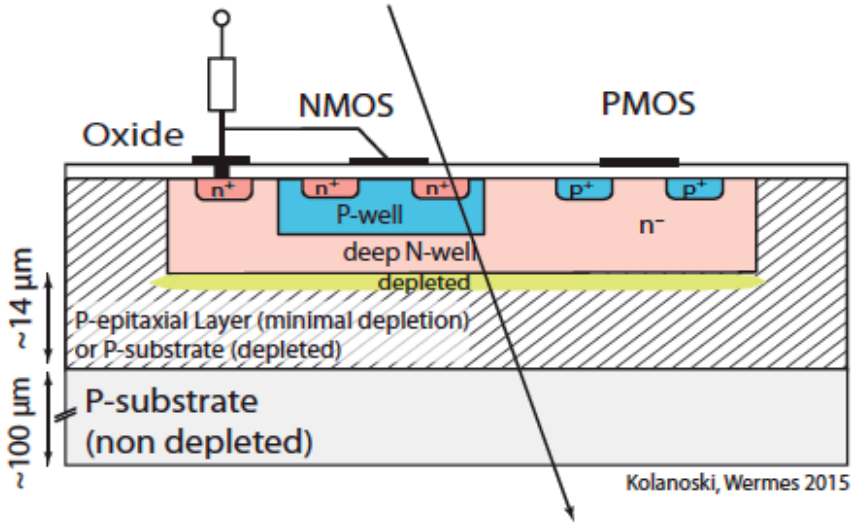


Figure 4.5: Pixel cross section of a generic HV-CMOS pixel structure, where the deep n-well is used as a charge collecting electrode [82]. Dimensions are not to scale.

There are two approaches under investigation to couple the sensor to the ATLAS FE-I4 R/O-chip. The first one is directly via bump bonds and the second one is capacitive coupling via isolating glue. The later one is usually referred as Capacitively Coupled Pixel Detector (CCPD). The prototypes under the HV-CMOS label lie under the active hybrid pixel detector category.

The last years investigations in laboratory with radioactive sources in the lab, laser set-up, and test beam campaigns have brought many interesting results up. HV-CMOS pixel sensors

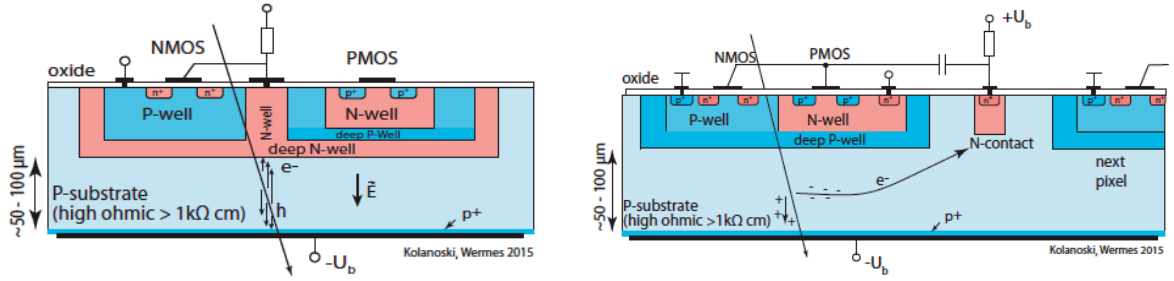
have proven to stand a TID of up to 1 Grad, showing a signal of 1500 e^- and a noise of about 60 e^- for the mentioned dose [79]. HV-CMOS pixel sensors have proven to stand fluences up to 10^{15} $n_{eq}cm^{-2}$. Results from several test beam campaigns have shown an in-time efficiency of 99% before irradiation and 96% after 10^{15} $n_{eq}cm^{-2}$ [79]. The measured depletion depth is about (10-20 µm) at 100 V [79]. The signal rise-time is still too slow (typically about 100 ns) for ATLAS.

A HV-CMOS prototype in AMS 350 nm feature size has been selected to be produced in large scale. The submission had recently taken place and further details are given in [92].

4.2.2 HR-CMOS pixel sensors

The High Resistivity CMOS (HR-CMOS) approach has been produced in different technologies (ESPROS 150 nm, LFoundry 150 nm) [93]. These technologies offer high resistivity substrates, the addition of multiple wells, and in some cases a backside contact.

Prototypes are being investigated in two generic variants shown in figure 4.6. Variant A (figure 4.6a) looks similar to the HV-CMOS structure in the way that the electronics sit in the collecting n-well electrode. However this approach includes an extra p-well to isolate the n-well of the PMOS from the n-well of the collecting electrode. Thus, less cross talk is expected. Variant B (figure 4.6b) presents a small collecting n-well placed outside the electronics. Decoupling the collecting electrode from the electronics, and at the same time shielding the n-well of the PMOS reduces the cross talk. The small size of the collecting electrode provides a small capacitance. However, a small fill factor is achieved and a longer drift path is needed. In a prior comparison, variant B will benefit from smaller capacitance than variant A, but it will be likely less radiation tolerant.



(a) (b)

Figure 4.6: Pixel cross section of a generic HR-CMOS pixel structure (a) variant A (b) variant B [82]. The deep n-well is used as a charge collecting electrode in both variants. Dimensions are not to scale.

Recent results have shown a mean signal of 6200 e^- at 20 V corresponding to a depletion depth of about 60 µm. The amount of charge collected within 25 ns are dependent on the

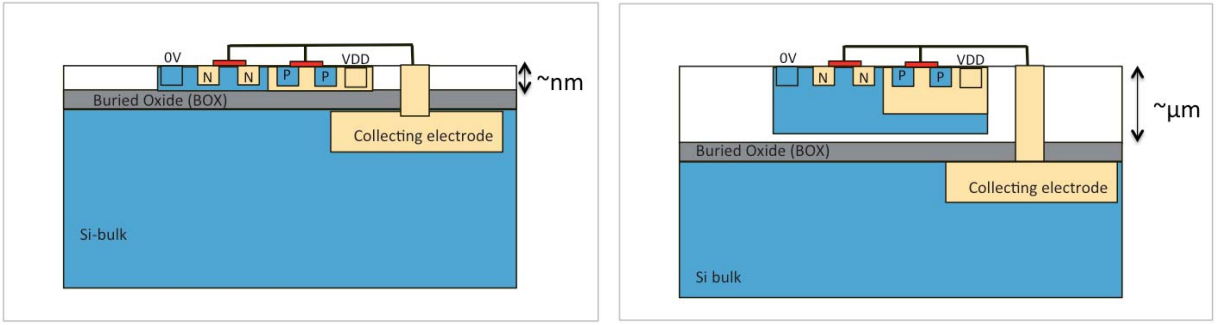
threshold value [94] (91% for a threshold value of 2600 e^-). Test beam campaigns took recently place. The next steps are to thin down the sensors to 300 µm and the implementation of a backside implant for bias voltage connection.

A HR-CMOS prototype in LFoundry 150 nm feature size has been selected to be produced in large scale. The submission will take place within the coming months.

4.2.3 CMOS-on-SOI monolithic pixels

The SOI technology provides a BOX which separates the CMOS electronics from the wafer substrate as described in section 3.1.2. This facilitates the use as a monolithic detector by using the wafer substrate as a sensor. Both parts, sensor and electronics, are connected by vertical structures through the BOX leading to the collecting well. The complete isolation between electronics and collecting electrode, plus the absence of competing n-wells make this approach very interesting.

Monolithic SOI-based pixel detectors have been developed for some time mainly for imaging applications [95]. Here the LAPIS technology is used, where the distance between the transistors gate and the BOX is in the order of nanometers. This approach is sketched in figure 4.7a. This leads to a full depletion (FD) of the transistor body, and it is usually named FD-SOI. Measurements have shown that this approach suffers from effects inherent to the BOX oxide layer [66, 67]. A first observed effect is the higher sensitivity to ionizing irradiation due to the additional oxide of the BOX [68, 69]. A second observed effect is the so called Back Gate Effect. These effects were described in section 3.1.2



(a) (b)

Figure 4.7: SOI-based CMOS pixel types. (a) FD-SOI: the distance between the transistors gate and the BOX is in the order of nanometers, thus the transistor body is full depleted. (b) Thick film SOI: the distance between the transistors gate and the BOX is one order of magnitude bigger. Thus, the transistor body is partially depleted and additional structures to isolate readout from sensor can be added.

The CMOS-on-SOI monolithic approach investigated in this thesis for the ATLAS HL-LHC upgrade is instead built on a thick film SOI process, sometimes named as Thick film HV-SOI

MAPS. A simple pixel cross section of this approach is shown in figure 4.7b. In contrast to FD-SOI technologies, the thick film SOI provides a thick electronics silicon layer. This enables on one side a double well structure to shield the thin gate transistors from the BOX. On the other side, the larger distance makes the technology promising against the radiation effects in the BOX on the transistors and against the Back Gate Effect.

In this line, two prototypes were designed by University of Bonn using the XFAB process [96]. The XFAB process makes it possible to apply high bias voltages (up to 300 V) which are used to partially deplete the substrate. It is possible to fabricate devices in higher resistivity (1 k$\Omega\cdot$ cm). Therefore, a fully depleted substrate could be achieved after thinning. Currently there is no backside processing, thus the HV is applied from the top using a p^+ implant ring, but it would be desirable for future submissions. The process allows different n-well sizes, giving freedom to trade the pixel capacitance versus the fill factor. The validation programme corresponds to the work presented in this thesis. Therefore, no results are advanced in this section. Instead, a deeper description to the prototypes is given.

XTB01 Prototype

The first prototype fabricated, called XTB01 [97], is 300 µm thick, with a size of 5 mm × 2 mm. The chip includes four independent matrices with different pixel sizes (25 µm × 25 µm , 50 µm × 50 µm (x2), 100 µm × 100 µm) and different n-well sizes. The BOX isolates the full CMOS electronics technology from the substrate which is reversely biased and used as a sensor diode as illustrated in the pixel cross section of figure 4.8. The substrate is p-type silicon with 100 Ω cm resistivity. The charge is collected in a small deep n-well of 10.5 µm × 14 µm size, which reduces the capacitance with respect to HV-CMOS approaches, which use a large deep n-well as charge collecting electrode [91]. The deep n-well is connected to the readout circuitry as illustrated in the pixel cross section shown in figure 4.8.

The HV is applied from an outer guard ring (HV ring), and in addition the chip includes three additional grids surrounding each pixel of all matrices. The HV can be applied through these grids, too. A sketched top view of the prototype is shown in figure 4.9 where the HV structures and different matrices are highlighted. On the left figure the chip layout is shown and the different matrices type are observed. The chip includes transistor test structures of different width, length, and type to test the radiation hardness. On the right figure a sketch shows the HV structures (p-well) in blue and the n-well structures in orange. The n-ring surrounding each matrix ensures that the pixels located at the outer part of the matrix have same potential than the ones located at the center.

The readout implemented in every pixel is a standard 3T cell circuit as shown in figure 4.10 [97]. A 3T cell circuit is composed of three transistors, M_{RST} as a reset transistor, M_{IN} as an amplifier or input transistor and M_{SEL} as select pixel transistor. While M_{RST} and M_{SEL} work as simple switches, M_{IN} works as a source follower stage.

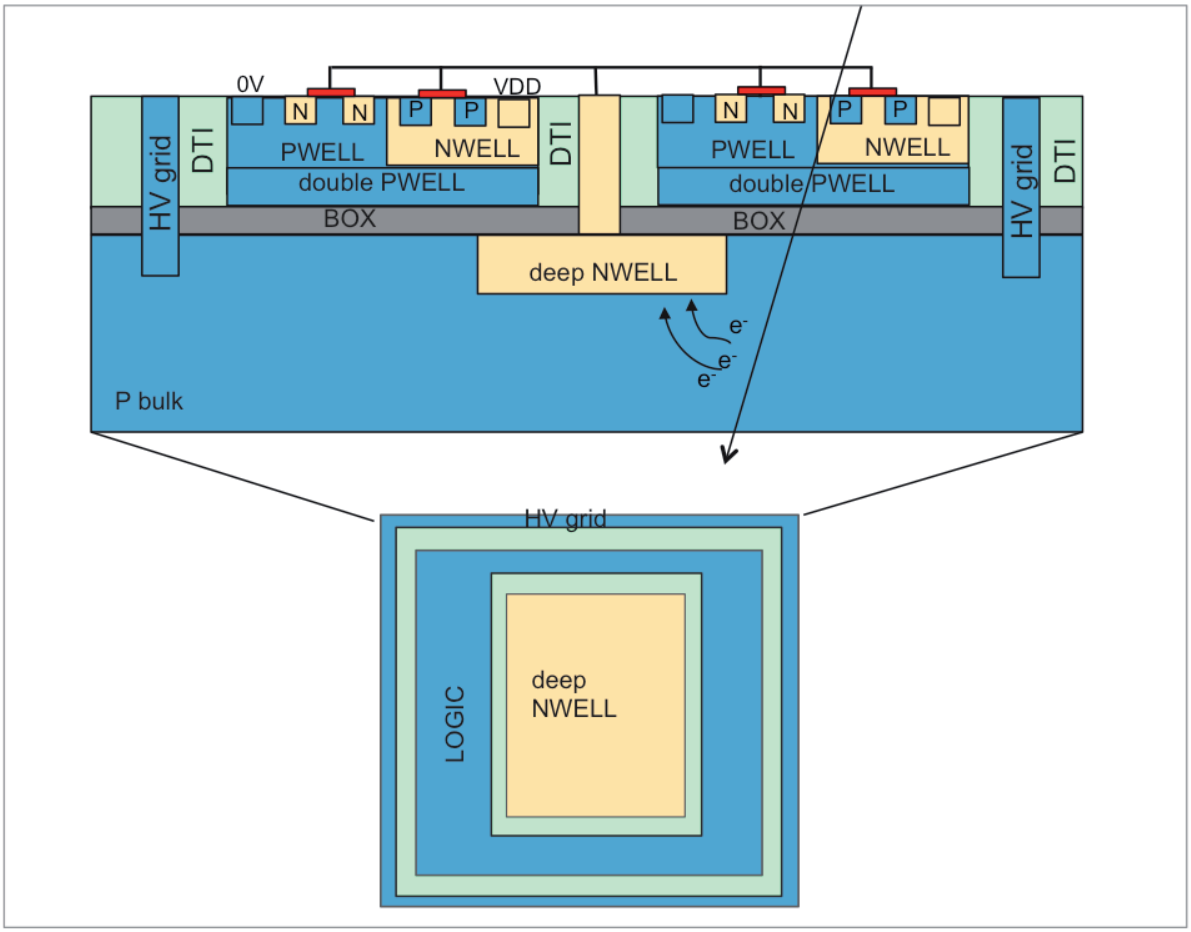


Figure 4.8: A pixel cross section and top view of the XTB01 prototype. The BOX isolates the integrated circuit from the sensor diode. In this prototype, the deep n-well is used as a charge collecting electrode, and the high voltage is applied from the top. Dimensions are not to scale.

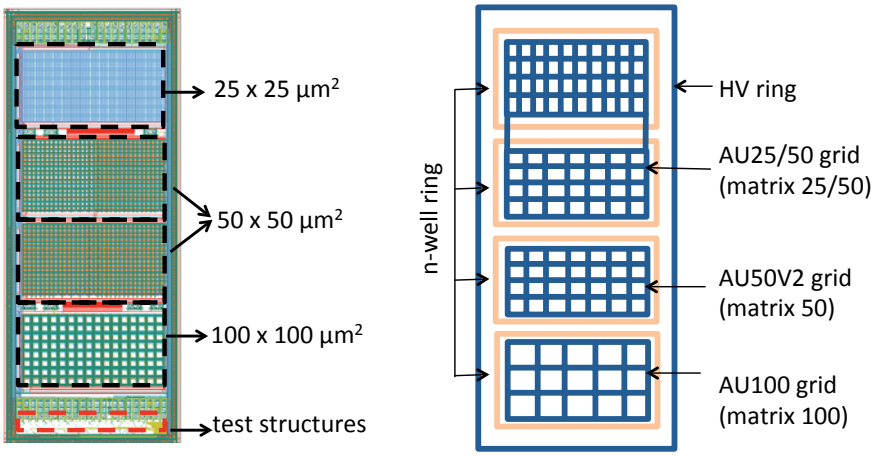


Figure 4.9: Top view sketch of prototype XTB01 and its ring structures. On the left, the chip layout is depicted and the different matrices are indicated. On the right, a top view sketch of the XTB01 prototype is shown where the HV structures and n-well rings are highlighted in blue and orange, respectively.

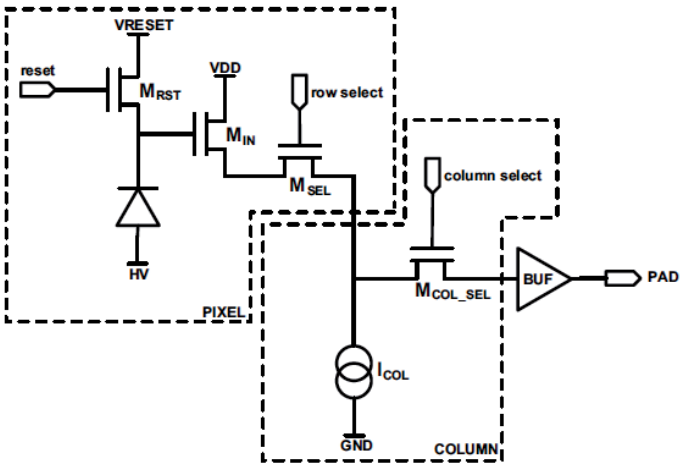


Figure 4.10: Simplified schematics of the XTB01 pixel readout [97]. A 3T pixel cell circuit is implemented in each pixel. The current on the input transistor M_{IN} is controlled by the constant current source.

When a particle passes through the diode, M_{RST} is open and thus the negative charge is accumulated at the gate of M_{IN}. As the current passing through M_{IN} is constant, a different charge accumulated on the gate will change the resistance value, and in consequence the output voltage. For the selected pixel, M_{SEL} would be closed and in consequence the output voltage is read. After that, M_{RST} is closed in order to discharge the accumulated charge on M_{IN}.
In this kind of readout, either the output signal of a single pixel can be permanently monitored, or the full matrix can be read out using a rolling shutter [98] with correlated double sampling. This means that only one pixel can be read it at a time. Such a readout is too slow for an ATLAS application but is sufficient for the characterization of first prototypes and technology validation. In further steps, a new readout architecture needs to be implemented.

The typical output signal of a pixel in the XTB01 prototype is sketched in figure 4.11 where four cases are depicted. The top one shows the reset signal which lasts at least 200 ns. During

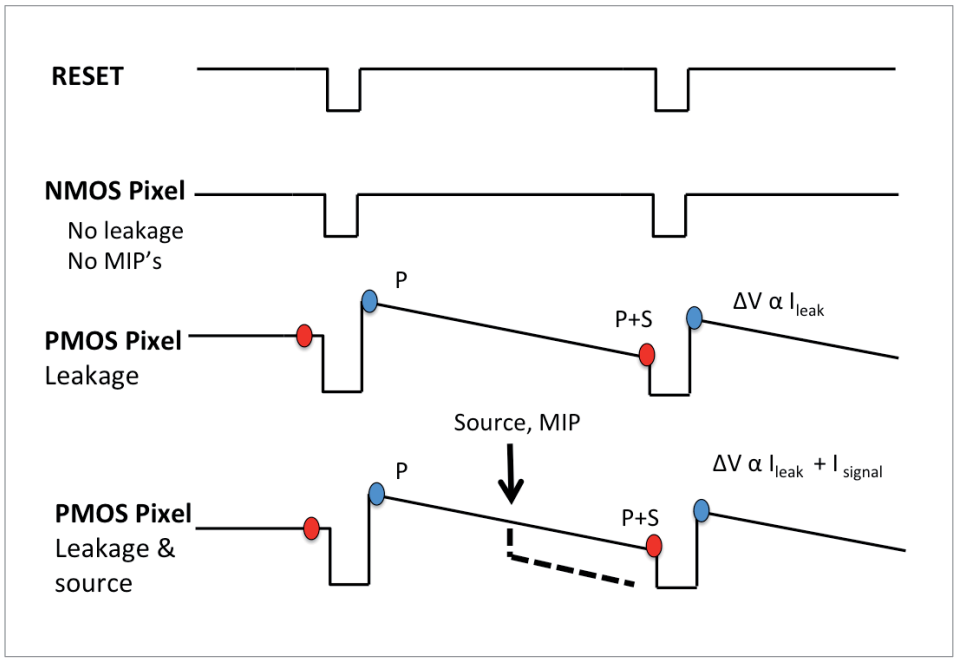


Figure 4.11: Typical output signal of a pixel of the XTB01 prototype, where the charge is accumulated within two resets. On the top the reset signal is shown. On the second top the ideal case: HV applied and not leakage current contribution is observed. On the second bottom, the real case: HV is applied and leakage current is accumulated. On the bottom the real case when HV is applied and MIP is traversing the pixel is shown.

the reset periods the chip is not readout. The second top one shows the ideal output signal, in which HV is applied and the leakage current is zero. The third top one corresponds a case where HV is applied and leakage current is accumulated between resets. This is the usual case. The difference in voltage is proportional to the leakage current value. Due to the constant signal increase, the pixel needs to be reset frequently. The bottom figure corresponds to the

case in which a HV is applied and a MIP is traversing the pixel. In this case, the different in voltage is proportional to the leakage current plus to the MIP signal.

XTB02 Prototype

A new version, called XTB02, was designed by University of Bonn to investigate purely the charge collection properties of the silicon bulk bellow the BOX. Thus, in XTB02 the deep n-well is not connected any more to the readout circuitry but is kept as an output going to an external amplifier. Thus this prototype behaves as a simple passive diode. The chip size, geometry and distances to the BOX are comparable to the XTB01 prototype. However the process has slightly changed: some process modifications were implemented to reduce the high leakage current observed in the XTB01 prototype, and increase the diode breakdown voltage [99].
XTB02 as well presents several matrices with different pixel sizes. Figure 4.12 shows a top view of the XTB02 prototype where the measured matrices, matrix II-A and matrix I-A, are highlighted.

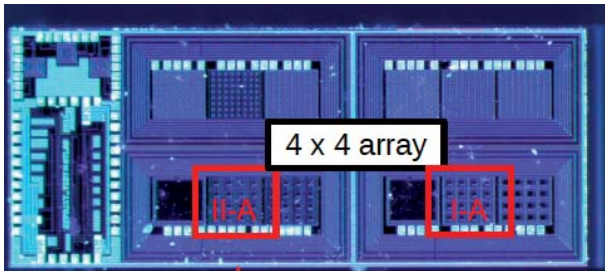
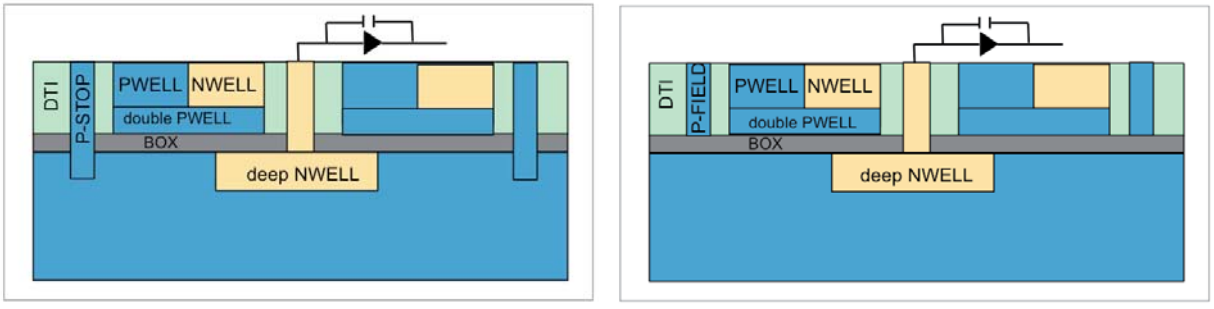


Figure 4.12: Top view of XTB02 prototype where the different matrices types are observed. The matrix II-A and matrix I-A are highlighted.



(a) (b)

Figure 4.13: A pixel cross section of prototype XTB02. (a) Pixel corresponding to matrix I-A. It possess a p-stop structure. (b) Pixel corresponding to matrix II-A, which possess a structure called p-field. Both structures are included to reduce the leakage current specially after ionizing irradiation. Dimensions are not to scale.

Figure 4.13 illustrates the cross section of the two pixel diode types, both 100 µm pitch, investigated in this thesis. The pixel shown in figure 4.13a, located in matrix I-A, includes a p-stop structure surrounding every pixel, while the one shown in figure 4.13b, located in matrix II-A, includes an structure which can be biased and does not penetrate the BOX, called p-field. The aim of both structures is to modify the electrical field bellow the BOX and to break the conductive channel formed in the bulk due to the space charge formed in the BOX after irradiation [99]. The n-well size for both pixel diode types is 40 µm × 50 µm.

Chapter 5

Characterization of the radiation hardness to Total Ionizing Dose

To validate the 180 nm SOI technology described in chapter 4 for its use in the HL-LHC upgrade, its radiation hardness against TID must be demonstrated up to the expected fluences in the experiment. Within this context the XTB01 prototype ,described in section 4.2.3, was irradiated with X-rays up to 700 Mrad.

This chapter starts with a description of the transistor test structures on the prototype. Section 5.2 and 5.3 describe the transistor characterization setup and the X-ray irradiation setup. Section 5.4 describes the shift of the electrical parameters of various transistors, the existence of Back Gate Effect, and the impact of the TID in the BOX on the sensor diode.

5.1 XTB01 transistors test structures

The XTB01 prototype contains transistor test structures to characterize its radiation hardness with TID. The schematic of the XTB01 test structures is shown in figure 5.1. The transistors are of various types: standard transistors nMOS type transistors (RD_N0, ..., RD_N15) and pMOS types (RD_P0, ..., RD_P15) with different geometries, and two enclosed transistors (RD_P16 and RD_N16).

The nMOS types are located on the left part and pMOS types on the right part of the figure. The red hexagonal pads correspond to the accessible pads in order to measure the transistor transfer characteristics. As shown in figure 5.1 all transistors share the same gate pad (RD_GATE). This limits the possible bias conditions of the transistors during irradiation. The source of nMOS transistors is connected to AVSS=0 V and the drain pad is accessible. For pMOS, the source is connected to AVDD=1.8 V and the drain is an accessible pad.

The transistors selected for characterization during the irradiations are shown in table 5.1. A total of 16 linear transistors with different width/length, and the 2 enclosed ones were selected. The scope of irradiating different transistor types and geometries is to compare the shift of the transistor electrical parameters with scaling the transistors width and length, to observe the

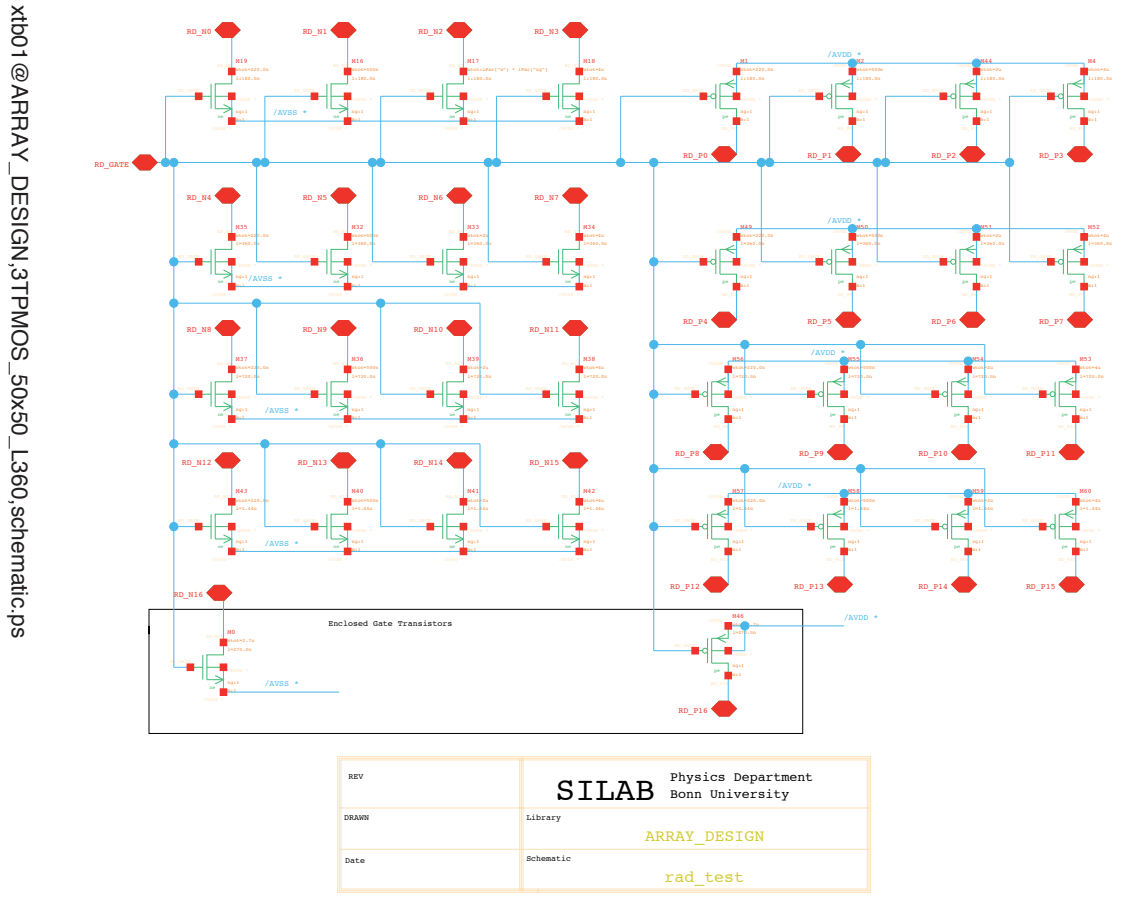


Figure 5.1: Transistor test structures of the XTB01 prototype. All transistors share the same gate. The nMOS transistors are located on the left while the pMOS transistors on the right. All transistors are standard linear transistors, except RD_N16 and RD_P16 which are enclosed transistors.

Name	W [µm]/L[µm]	Scope
RD_N0	0.22/0.18	W scaling
RD_N1	0.5/0.18	
RD_N2	2.0/0.18	
RD_N3	4.0/0.18	
RD_N6	2.0/0.36	L scaling
RD_N10	2.0/0.72	
RD_N14	2.0/1.4	
RD_N16	2.7/0.27	enclosed
RD_N12	0.22/1.4	smallest gain

(a)

Name	W [µm]/L[µm]	Scope
RD_P16	2.7/0.27	enclosed
RD_P12	0.22/1.4	min gain
RD_P0	0.22/0.18	W scaling
RD_P1	0.5/0.18	
RD_P2	2.0/0.18	
RD_P3	4.0/0.18	
RD_P6	2.0/0.36	L scaling
RD_P10	2.0/0.72	
RD_P14	2.0/1.4	

(b)

Table 5.1: List of selected transistors on XTB01 to perform characterization to TID separated on (a) nMOS and (b) pMOS. The width (W)/length (L) and the scope for choosing those transistors are shown.

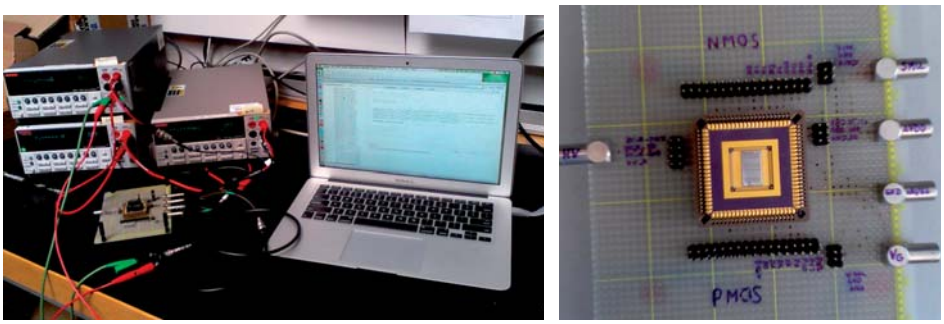
behaviour of the minimum gain transistor and to compare standard and enclosed transistors behaviour.

5.2 Transistors characterization setup

The transistor characterization consists on a direct measurement of the drain current as a function of the gate voltage, known as transistor transfer characteristics. Subsequently, the electrical parameters of the transistors are extracted from it.

The transistors characterization setup is shown in figure 5.2a. It consists of a home-made board, which allows the selection of each individual transistor, and three power supplies to measure the transfer characteristics. The home-made board containing the XTB01 chip is shown in figure 5.2b. The four SubMiniature version A (SMA) connectors on the right provide AVDD and AVSS voltage to the structures, the drain voltage, and V_G voltage to the gate for all transistors. The drain of the individual transistors is labelled on the board. Each individual transistor is then selected by placing a jumper for the corresponding transistor. A second jumper selects to which SMA connector the drain is addressed to. The SMA connector on the left labelled as HV allows performing a Current-Voltage measurement on the external ring, which surrounds the transistors structure.

A dedicated routine was developed to extract the threshold voltage, leakage current, and transconductance from the transistor transfer characteristics. The threshold extraction is based on the extrapolation method in the saturated region (ESR) [100]. The implemented algorithm goes through each point of the square root of the characteristics curve. The largest slope between consecutive points is identified, and subsequently a linear extrapolation between them



(a) (b)

Figure 5.2: The transistors characterization setup. (a) It shows the full setup consisting in a home-made board containing the XTB01 to select each individual transistor and three power supplies to measure the characteristics. (b) It shows the home-made board where the pins to select individual transistors, and the connectors to bias the gate, source, and drain are depicted.

is made. The threshold voltage value is calculated as the interception between the linear extrapolation and the x-axis.
The leakage current is extracted as the drain current value when the gate bias voltage is V_{GS} =0 V (nMOS) and V_{GS} =1.8 V (pMOS). The transconductance or transistor gain is extracted by derivating the $I_{DS} - V_{GS}$ curve and calculating the maximum value [100].
Figure 5.3 shows the output of the implemented routine for five nMOS transistors before irradiation. The top left plot shows the measured characteristics and the bottom left one the threshold extraction. The transconductance is extracted as the maximum value from the top right plot, and the leakage is extracted as the minimum value from the bottom right plot.

5.3 X-ray irradiation facility and setup

Two irradiation campaigns were carried out in the X-ray Irradiation Facility at CERN. The system is composed of an X-ray machine, a semi-automatic wafer prober, which was not used in our measurements, and a thermal chuck, a cooling element and a controller to set and maintain the temperature of the chuck [101]. It is also composed of a CCD camera and a dry air system, which filters and dries the air to lower the dew point inside the irradiation cabinet. The X-ray tube uses a Tungsten target (peak 10 keV) and an aluminium filter of 0.15 mm to ensure reasonably uniform dose rate in the Device Under Test (DUT).
The dose rate is variable depending on the supplied voltage, the tube current and the tube to DUT distance. The tube to DUT distance (z-axis) can be set and measured by a mechanical system of the setup. The diameter of the X-ray beam is around 3-4 mm in the high dose rate configuration (9 Mrad/h) [101]. A laser pointer allows to align the DUT with the X-ray beam center (xy alignment). First, the DUT is aligned to be pointed by the laser and this position is recorded. Subsequently, a mechanical controller which has stored the fixed laser-tube distance moves the tube to the stored laser position. Figure 5.4 shows the X-ray setup with the XTB01 prototype installed on it.

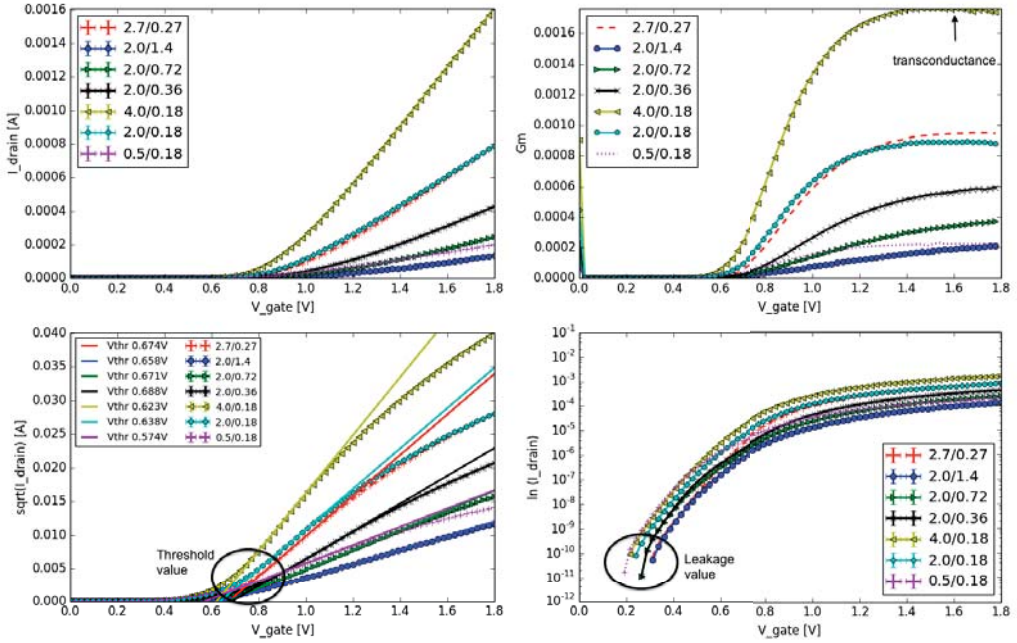


Figure 5.3: The output of the analysis algorithm to extract the transistor electrical parameters. The routine output always shows the measured transfer characteristics (top left) and the threshold extraction at bottom left. The transconductance is extracted as the maximum value of the top right plot, and the leakage current is extracted as the first point on the bottom right plot. This example shows the case of five nMOS transistors before irradiation.

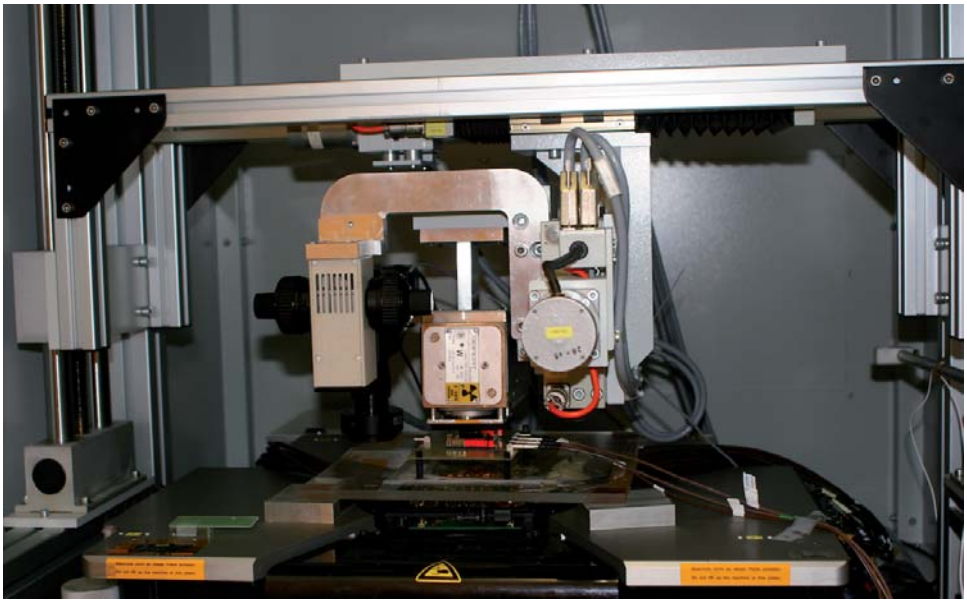


Figure 5.4: The X-ray machine at the X-ray Irradiation Facility at CERN. The X-ray tube is aligned to the XTBO1 sample thanks to the laser tube on the left.

The two irradiation campaigns were performed up to a TID of 700 Mrad in several steps at room temperature. The dose steps were: 100 krad, 200 krad, 300 krad, 400 krad, 500 krad, 600 krad , 800 krad, 1 Mrad, 3 Mrad, 5 Mrad, 15 Mrad, 50 Mrad, 100 Mrad, 150 Mrad, 300 Mrad, 500 Mrad and 700 Mrad. The dose steps up to 3 Mrad are very small because the largest characteristic shifts are expected at small TID.
The machine dose rate configuration was 8 Mrad h^{-1} achieved by setting the X-ray tube to 2 cm distance to the DUT, 40 kV and 50 mA. The z-alignment was achieved by setting the tube-DUT distance to 2 cm and the xy-alignment was performed with the laser pointer. Some marks were drawn on the glass where the XTB01 board is placed as shown in figure 5.4, in order to unequivocally locate the board within the glass.
The test procedure followed the Standard test method ESA/SCC BS 22900 [102], in which the transistor characteristics are tested right away after the irradiation step. Therefore, the annealing is considered negligible during irradiation and testing. Once the machine is set and the XTB01 is aligned, the cabinet is closed and the irradiation started. Immediately after each irradiation step, the board is removed from the X-ray cabinet to the transistor characterization setup where the transfer characteristics of each transistor are measured. Subsequently, the board is newly installed on the marked place using the previous xy-alignment.
The bias conditions applied on the transistors during irradiation are crucial for the created damage as described in section 3.1.2. The bias conditions applied during both irradiation campaigns are summarized on table 5.2.

Bias conditions		
Campaign A	nMOS	V_G= 1.8 V, V_D=V_S=0 V (corresponds to nMOS ON)
	pMOS	V_G=V_D=V_S=1.8 V (corresponds to pMOS OFF)
Campaign B	nMOS	V_G=V_D=V_S=0 V (corresponds to nMOS OFF)
	pMOS	V_G= 0 V, V_D=V_S=1.8 V (corresponds to pMOS ON)

Table 5.2: Bias conditions of the XTB01 transistors during X-ray irradiation for both irradiation campaigns.

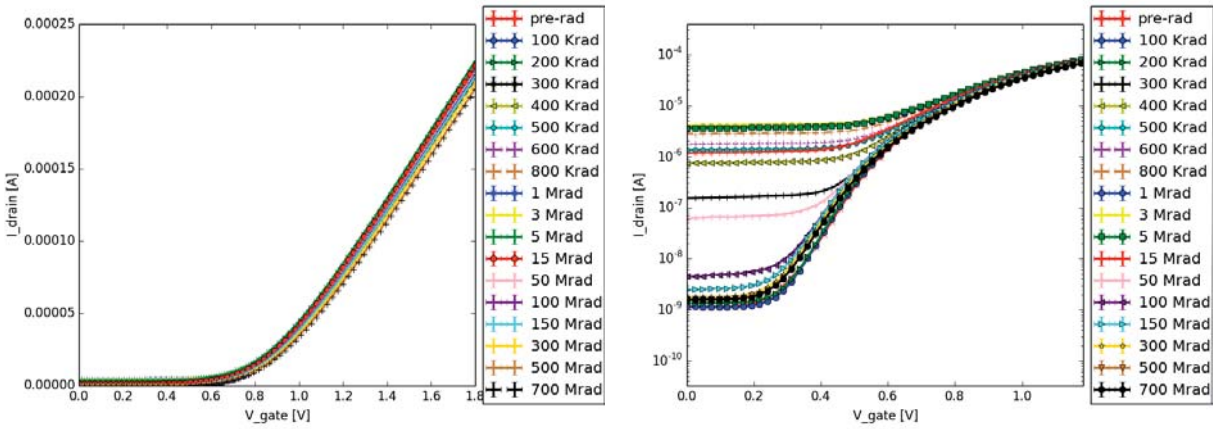
5.4 Results

5.4.1 Transistors response to Total Ionizing Dose

The ionizing effects on the transistors are visible in the transfer characteristics curve. Figure 5.5 shows the transfer characteristics of the smallest nMOS transistor -0.5/0.18- for all the irradiation steps. The curve shifts under radiation, first to the left up to a certain dose that shifts to the right accordantly with the described in section 3.1.2. Thus, a change in the threshold voltage is inferred in figure 5.5a. The leakage value which is identified with the initial value in figure 5.5b, obviously shifts with TID.
The ionizing effects are also visible in the characteristic curve of a pMOS transistor. The transfer characteristics of the smallest pMOS transistor -0.5/0.18- for all the irradiation steps are shown in figure 5.6. The shift of the curves of figure 5.6a infers a shift of the threshold. A shift of the leakage current, which corresponds to the last value in figure 5.6b is observed. As expected, the nMOS transistor is more susceptible than pMOS to a leakage current shift (see section 3.1.2). The shifts on the electrical parameters are explained in detail in the following subsections.

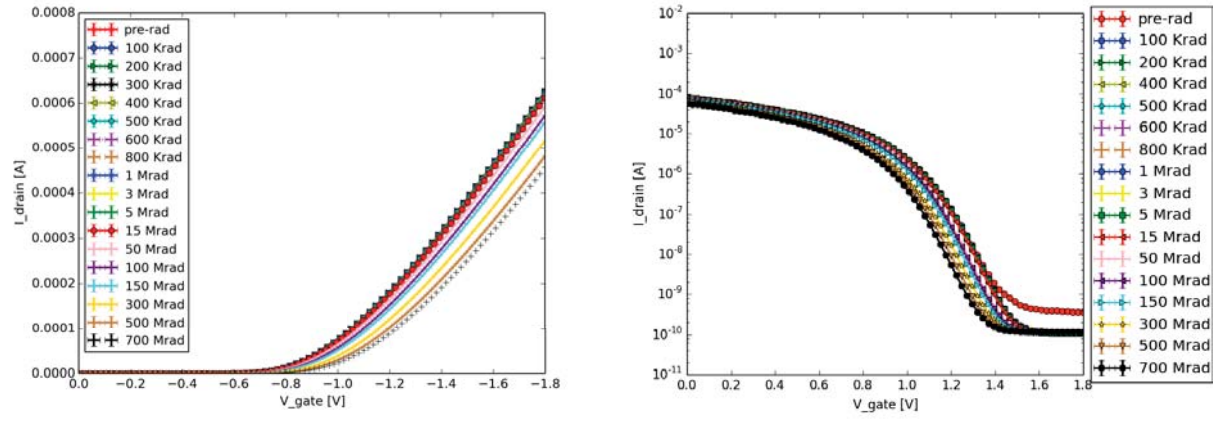
Threshold Voltage Shift

The threshold voltage shift evolution with TID of the nMOS transistors is shown in figure 5.7 for the two bias options. Figure 5.7a shows the threshold voltage shift evolution with TID for bias option A, which corresponds to the nMOS on. It is observed that up to 5 Mrad the threshold voltage decreases due to the charges trapped in the oxide while for a dose >5 Mrad an increase of the threshold value starts due to the interface traps. Therefore, the rebound shift expected on nMOS bulk transistors as explained in section 3.1.2, is similarly observed for the thick film SOI transistors of this prototype. The enclosed transistor - 2.7/0.27 labelled in red - is the one showing the smallest degradation, as is expected, with a threshold shift $\triangle V_{th}$ <10 mV up to 700 Mrad. The smallest transistor - 0.5/0.18- shows the largest threshold variation with a shift of $\triangle V_{th}$ = 80 mV. The maximum $\triangle V_{th}$ corresponding to 80 mV is within fabrication process variations. An additional conclusion can be extracted. Section 3.1.2 described how both oxides, the gate oxide and the field oxide, contribute to the transistor degradation. The strong W scaling shows that the effect on field oxide is dominating rather than the gate oxide one. This is known and expected for thin gate oxide transistors (~nm) [52].



(a) (b)

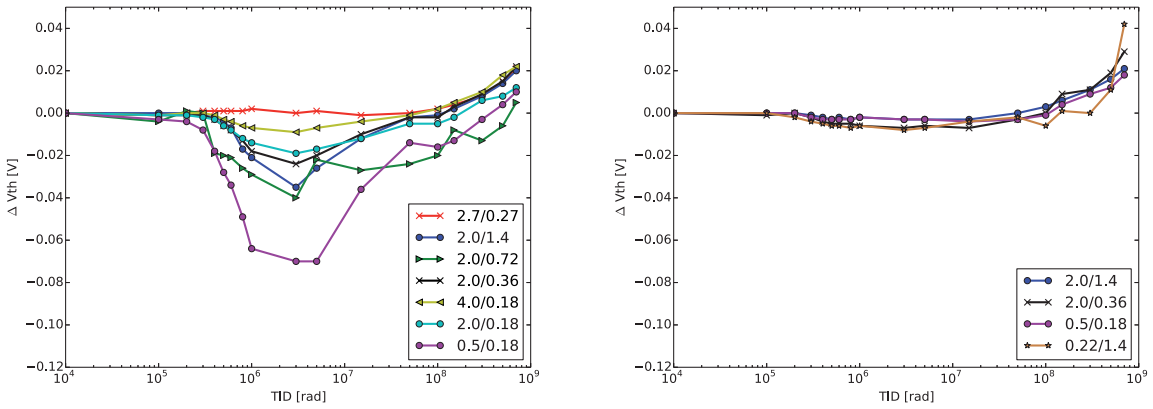
Figure 5.5: Transistor Transfer Characteristics for various radiation levels of a 0.5/0.18 nMOS (a) in linear scale where the change in the curve infers a change on the threshold voltage (b) in logarithmic where the shift on the leakage current value is observed.



(a) (b)

Figure 5.6: Transistor Transfer Characteristics for various radiation levels of a 0.5/0.18 pMOS (a) in linear scale where a change on the curve infers a change on the threshold voltage (b) in logarithmic where the shift on the leakage current value is observed.

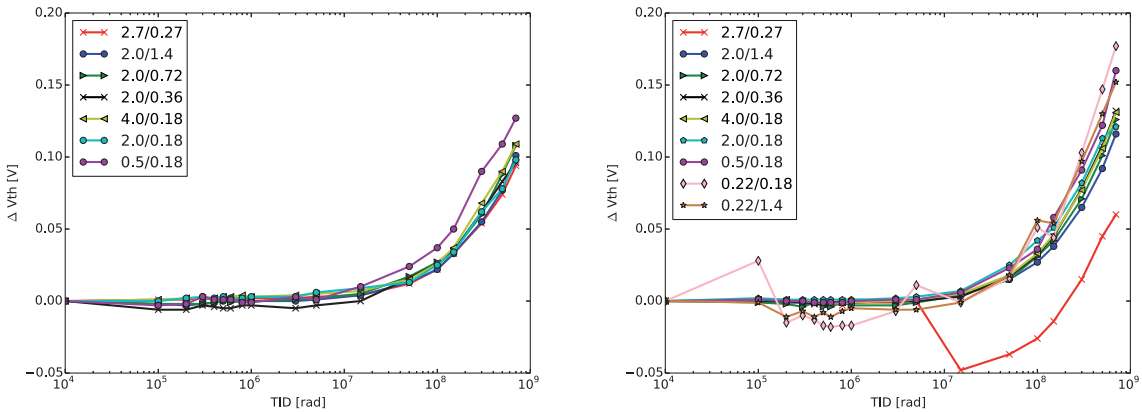
The threshold voltage shift evolution with TID of the nMOS transistors when nMOS are off during irradiation is shown in figure 5.7b. The degradation due to the oxide charge (up to 5 Mrad) is reduced in comparison with the case A for all transistor types. The smallest transistor - 0.5/0.18- shows the largest threshold variation with a shift of $\triangle V_{th} = 40\,\text{mV}$ up to 700 Mrad. By comparing figure 5.7a and figure 5.7b, one realizes that similar to bulk transistors the bias conditions of the gate during irradiation are crucial. nMOS off (figure 5.7b) is considered the best bias condition, since generated holes will not be pushed to the interface but rather being distributed all over the oxide. nMOS on (figure 5.7a) is considered the worst bias case, since the positive voltage at the gate will push the generated holes towards the interface and as described in section 3.1, holes accumulated close to the interface causes more degradation.



(a) (b)

Figure 5.7: Threshold shift as a function of the TID in nMOS transistors for two bias options (a) option A (nMOS on) and (b) option B (nMOS off). The threshold shift in a rebound way as expected and the degradation is reduced when nMOS are off, confirming the importance of the bias conditions during irradiation. The largest shift measured is within the fabrication process and comparable with non SOI technologies. Note that the value 10^4 corresponds to the value before irradiation.

The threshold voltage shift evolution with TID for pMOS transistors of the XTB01 prototype for both bias options is shown in figure 5.8. As described in section 3.1.2 in a pMOS it is not clear which are worse bias conditions during irradiation. The threshold voltage in pMOS transistors increases with TID. The same behaviour as the expected on bulk transistors is observed here. The results of both bias conditions are comparable in this technology. The maximum threshold variation is around $\triangle V_{th} = 120\,\text{mV}$ for the smallest transistor (0.5/0.18). This variation is within the fabrication process variation and compatible with non SOI technologies [103]. The enclosed transistor - 2.7/0.27 labelled in red - got broken during the characterization as is observed in figure 5.8b.



(a) (b)

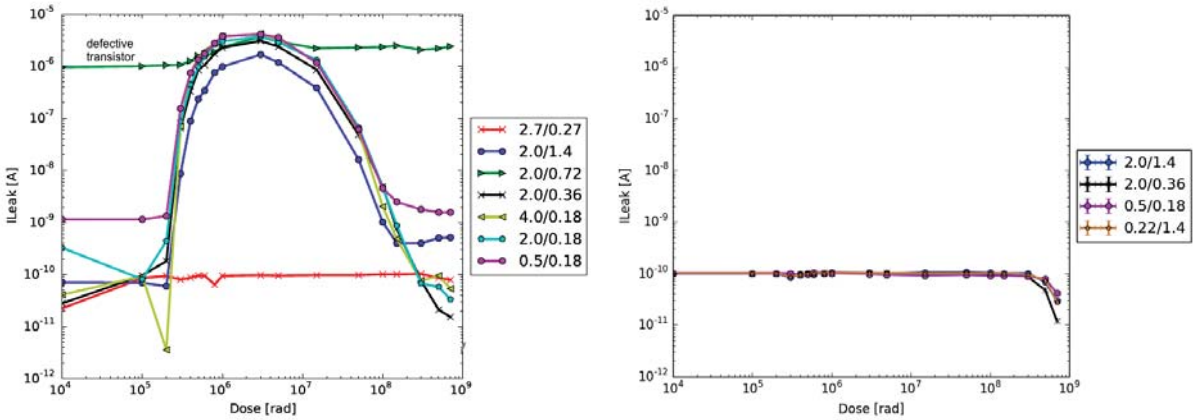
Figure 5.8: Threshold shift as a function of the TID in pMOS transistors for two bias voltage conditions: (a) option A (pMOS off) and (b) option B (pMOS on). The largest shift is within the fabrication process, and comparable to non SOI technologies. In this technology both bias conditions are comparable. Note that the value 10^4 corresponds to the value before irradiation.

Leakage Current and Transconductance Shift

The leakage current shift on nMOS with TID is shown in figure 5.9 for both bias conditions (on and off) during irradiation. For nMOS on, the leakage shifts in rebound way, as described in section 3.1.2. For nMOS off, the leakage shift is observable at higher doses, and no rebound shift is observed. Thus, also here is observed the importance of the bias conditions during irradiation. The transistor 2.0/0.72 (labelled in green) presented very high leakage current already before irradiation. The enclosed transistor - 2.7/0.27 labelled in red- is one presenting less leakage shift, as expected. The leakage current shift for nMOS on goes from 10^{-10} A to 10^{-6} A for the smallest linear transistor, while remains constant at 10^{-10} A for the enclosed transistor up to 700 Mrad.

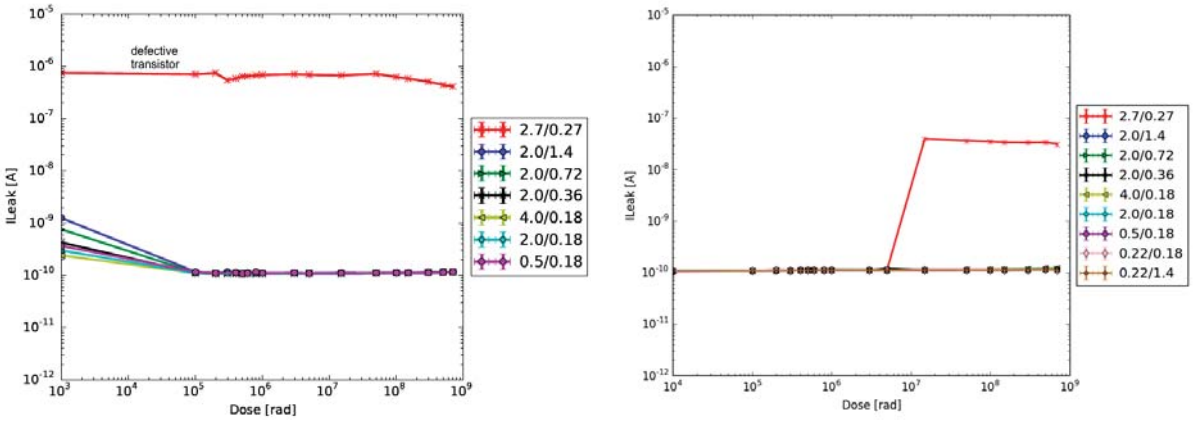
The leakage current shift with TID is shown in figure 5.10 for pMOS. The leakage current for pMOS transistors goes from 10^{-9} A to 10^{-10} A for the smallest linear transistor up to 700 Mrad. The bias conditions during irradiation are comparable. The enclosed transistor - 2.7/0.27 labelled in red- was broken from before irradiation in the first chip and got broken during measurements in the second chip.

The transconductance variation with TID is shown in figure 5.11 for nMOS and figure 5.12 for pMOS. The transconductance shift is around 20% for pMOS and 5% for nMOS transistors up to 700 Mrad.



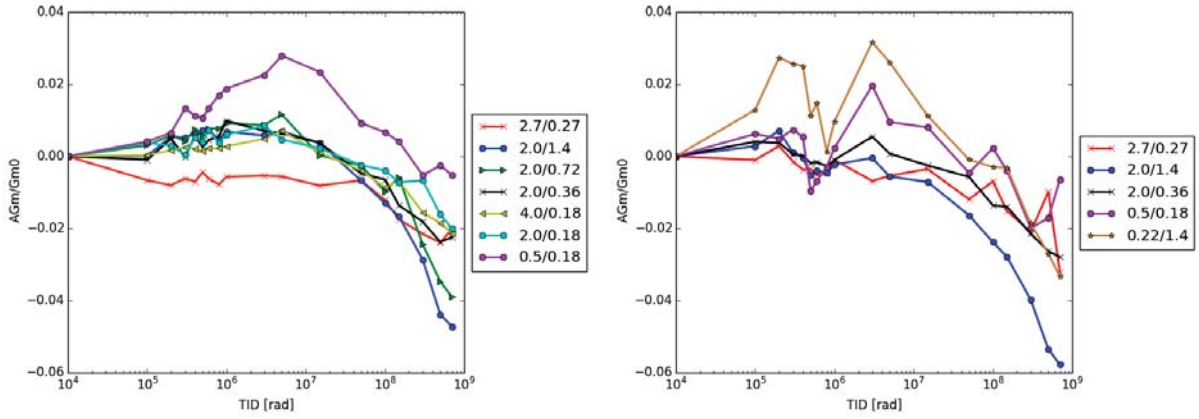
(a) (b)

Figure 5.9: Leakage shift as a function of the TID in nMOS transistors for two bias conditions: (a) option A (nMOS on) and (b) option B (nMOS off). The leakage current suffers a bigger shift when the nMOS transistors are on. The largest shift is within the fabrication process, and comparable to non SOI technologies. Note that the value 10^4 corresponds to the value before irradiation.



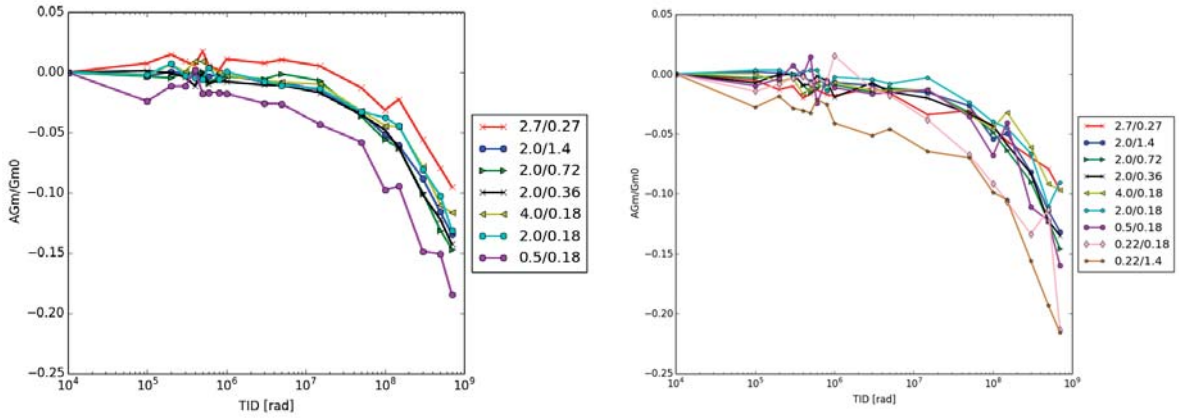
(a) (b)

Figure 5.10: Leakage shift as a function of the TID in pMOS transistors for two bias conditions: (a) option A (pMOS off) and (b) option B (pMOS on). As expected, the leakage current shift on pMOS transistors is smaller than in nMOS transistors. In this technology both bias conditions are comparable. Note that the value 10^4 corresponds to the value before irradiation.



(a) (b)

Figure 5.11: Transconductance shift as a function of the TID in nMOS transistors (a) for bias option A and (b) for bias option B. The transconductance shift on nMOS is around 5% in both cases. It is observed that the smallest transistor is more affected. Note that the value 10^4 corresponds to the value before irradiation.



(a) (b)

Figure 5.12: Transconductance shift as a function of the TID in pMOS transistors (a) for bias option A and (b) for bias option B. The transconductance shift on pMOS is around 20% in both cases. It is observed that the smallest transistor is the most affected and the enclosed one the less affected. Note that the value 10^4 corresponds to the value before irradiation.

In contrast to other SOI technologies in which the parameters shift after a few hundred krad [67], in this technology the accumulated charge in the BOX does not affect the electronics performance. The largest threshold variation is for nMOS $\triangle V_{th} = 80$ mV and for pMOS $\triangle V_{th} = 120$ mV up to 700 Mrad. The largest leakage current shifts is for nMOS from 10^{-10} A to 10^{-6} A and for pMOS from 10^{-9} A to 10^{-10} A up to 700 Mrad. The transconductance shift is around 20% for pMOS and 5% for nMOS transistors. These degradation of the electrical parameters obtained up to 700 Mrad is within the fabrication process variation and fully consistent with non SOI thin gate technologies like IBM 130 nm used for the ATLAS IBL readout chip FE-I4 [103]. Thus, its radiation hardness have been proven with this measurements up to 700 Mrad. This technology could be used for the outer layers of the HL-LHC ATLAS Pixel Detector where sensors have to withstand accumulated radiation doses up to50 Mrad. An additional irradiation campaign would need to be performed to prove it up 1 Grad, and then fulfilling the requirements for the innermost layers.

5.4.2 Back Gate Effect in XTB01

The Back Gate Effect, described in section 3.1.2, consists of the coupling between the electric field in the sensor and the transistor's operation. This phenomenon limits the applicable sensor bias and therefore techniques to reduce the Back Gate Effect are being investigated [70], [71]. nMOS transistors, especially, are affected by the Back Gate Effect [70]. Recent publications have shown an increase of up to eight orders of magnitude in the leakage current of nMOS transistors when a bias voltage of −50 V was applied to the sensor diode [70].

In order to investigate the magnitude of the Back Gate Effect in the XTB01 prototype, all transistor characteristics were measured on the 700 Mrad irradiated chip in two configurations: a) with the sensor diode floating and b) with a bias voltage of −40 V on the sensor diode. Figure 5.13 shows the transfer characteristics curve for three nMOS transistors. The overlapping characteristics of the transistors - without HV on the diode and with −40 V on the diode - prove that there is no coupling between the electronics and the electric field in the sensor. Thus no Back Gate Effect is present in our prototype, making it a very promising detector option.

5.4.3 Coupling between the buried oxide and the sensor diode

The results presented above show that the accumulated charge in the BOX does not affect the electronics performance. However, the influence of the accumulated charge in the BOX to the sensor part also needs to be evaluated. In order to do that, an Current-Voltage curve is first measured on an unirradiated chip, and subsequently on the irradiated chip up 700 Mrad with X-rays. All measurements were carried out at room temperature in all the HV rings of the matrix.
Figure 5.14a shows the Current-Voltage curves of the different rings in logarithmic scale for the unirradiated and irradiated chip. The leakage current increases by a factor eighty in the irradiated chip. This is explained by the fact that the electrical field, created by the positive charges accumulated in the BOX, attracts electrons to the Si-SiO_2 interface. This way a conductive

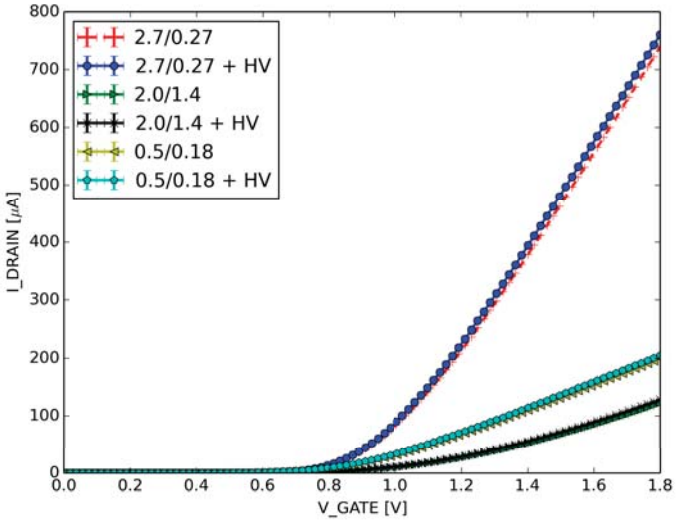
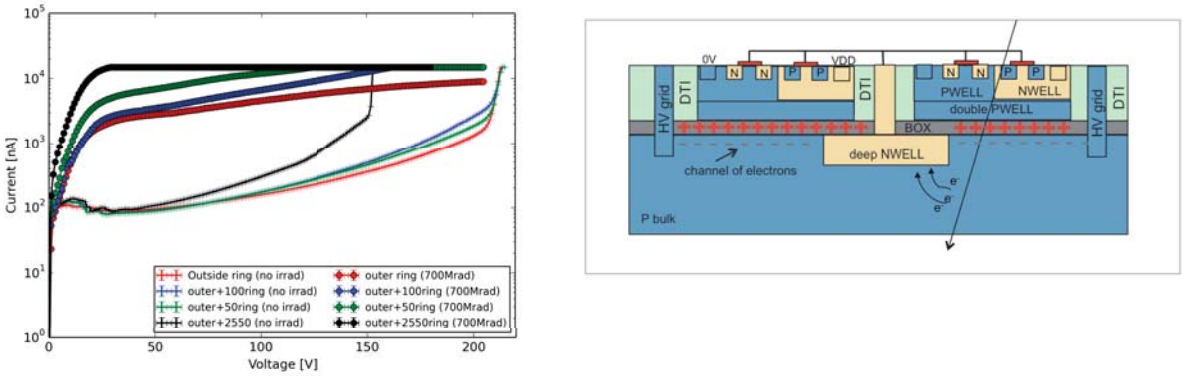


Figure 5.13: Transistor Transfer Characteristics of three nMOS transistors applying no voltage and −40 V to the sensor diode. The overlapping of the curves prove that the electric field in the sensor does not influence the electronics.

channel, sketched in figure 5.14b, is created which breaks the pn-diode. As a consequence the measured current increases. Therefore, accumulated charge in the BOX influences the sensor diode performance. A p-stop and p-spray was implemented in XTB02 prototype to avoid this channel. Measurements to investigate the effect of theses structures after irradiation have started.



(a) (b)

Figure 5.14: (a) Current-Voltage curves in logarithmic scale of each ring before and after 700 Mrad X-ray irradiation. The current increases by a factor of eighty after irradiation. (b) Sketch explaining the leakage current increase after irradiation. The positive charges accumulated in the BOX create a channel which breaks the diode.

Chapter 6

Charge collection measurements

The characterization of the charge collecting diode contains two major subjects: the characterization of the leakage current and breakdown voltage, and the charge collection measurements. These are crucial for performance characterization of any particle detector. The quantification of the leakage current, the demonstration of MIPs detection, the measurement of signal-over-noise, and the properties of the depletion region are measured and discussed over the next sections. The XTB01 and XTB02 prototypes described in detail in section 4.2.3 have both been used for this, depending on their specifications. On XTB01 the collection properties were measured with radioactive sources in the laboratory, while XTB02 was used for edge Transisent Current Technique measurements to investigate the depletion region. The available samples used for these measurements are summarized in table 6.1. The irradiated samples were stored at a temperature of -15 °C to avoid annealing. The neutron irradiation campaigns were performed using thermal reactor neutrons at the Jozef Stefan Institute in Ljubljana.

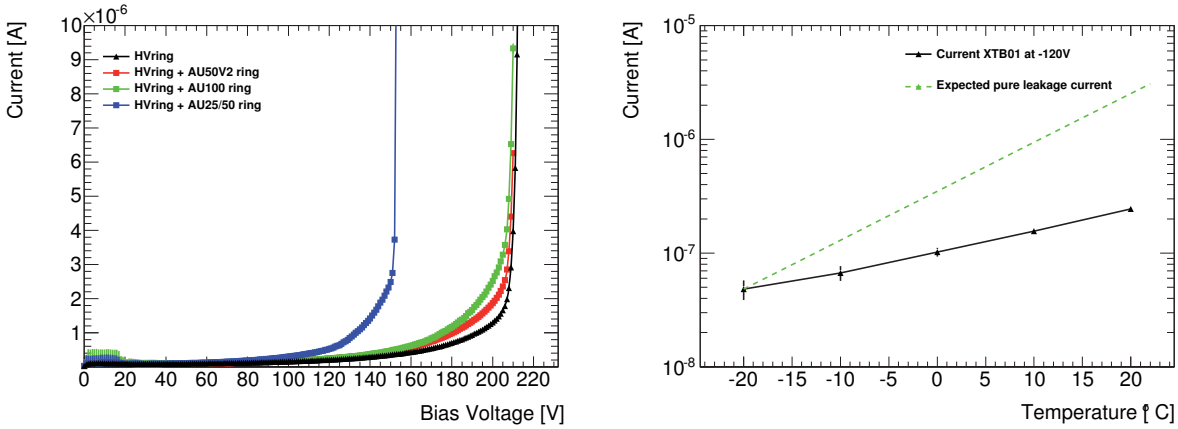
samples type	identifier	fluence [$n_{eq}cm^{-2}$]
XTB01	0B	unirradiated
XTB01	2B	1×10^{13} (neutrons)
XTB01	3B	5×10^{13} (neutrons)
XTB01	5B	1×10^{14} (neutrons)
XTB01	4B	5×10^{14} (neutrons)
XTB02	1A	unirradiated
XTB02	2A	unirradiated $\rightarrow 2 \times 10^{14}$

Table 6.1: List of the available XTB01 and XTB02 samples.

6.1 Leakage current characterization

The leakage current is measured on both prototypes by selecting the proper biasing ring and applying high voltage to the DUT board. The Current-Voltage curve for all rings (HV ring, AU100, AU50V2, AU25/50) of the unirradiated XTB01 chip at room temperature is shown in figure 6.1a. The different XTB01 rings were described in section 4.2.3. The expected operation current is 5 fA/μm^2 at 160 V, which in a 5 mm × 2 mm chip corresponds to a current of about 50 nA. However, because of unknown reasons, the current observed in figure 6.1a at

80 V is a factor of ten higher than expected for this prototype. The matrix with 25 µm × 25 µm pitch presents the smallest breakdown at around 140 V as one would expect since the distance for the biasing grid to the n-well is the smallest. For the other rings the breakdown voltage is around 200 V. There is no significant difference in terms of leakage current when the HV is applied on the individual matrix ring or in addition to the external ring. Thus, in the following measurements both rings were biased. The change on the leakage current as a function of the temperature was also evaluated. Figure 6.1b shows the Current-Voltage curve on the unirradiated sample at different temperatures when the AU50V2 ring and the HV ring were selected. The scaling of current with temperature is not in agreement with the exponential law in which roughly every 7 °C the current doubles described in section 2.2 and shown in figure 6.1b. This indicates that there is an additional contribution to the measured current with respect to the pure leakage current described in section 2.2. This contribution is likely a current flowing along the Si-SiO_2 interface below the BOX. These kind of currents are usually technology dependent and influenced by the production process.



(a) (b)

Figure 6.1: (a) Current-Voltage curves on the unirradiated XTB01 sample at room temperature when all the HV rings are connected. Except for the smallest matrix ring, the breakdown voltage is around −200 V (b) Current versus temperature at −120 V when the AU50V2 ring and the HV ring are connected (in logarithmic scale). The current evolution is not in agreement with the exponential law.

A comparison between the Current-Voltage curves in logarithmic scale of prototype XTB01 and XTB02 is shown in figure 6.2. The measurement was performed at room temperature and only the external ring was selected in both prototypes. The leakage current decreases by a factor of ten and the breakdown voltage increases from 150 V to above 300 V in the unirradiated XTB02 prototype. As described in section 4.2.3 XTB02 incorporates some structures with the aim of breaking the conductive channel formed in the bulk specially after irradiation. Additionally, some improvements in the manufacturing process were implemented by the foundry. The mentioned reduction of the leakage by a factor of ten demonstrate the effectiveness of these changes. For XTB02 the measured leakage current is in agreement with the expectations.

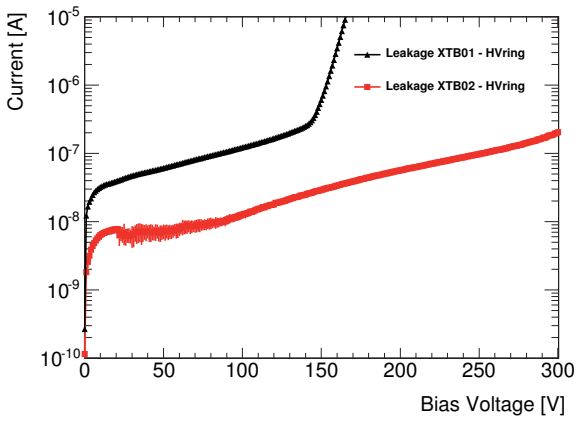
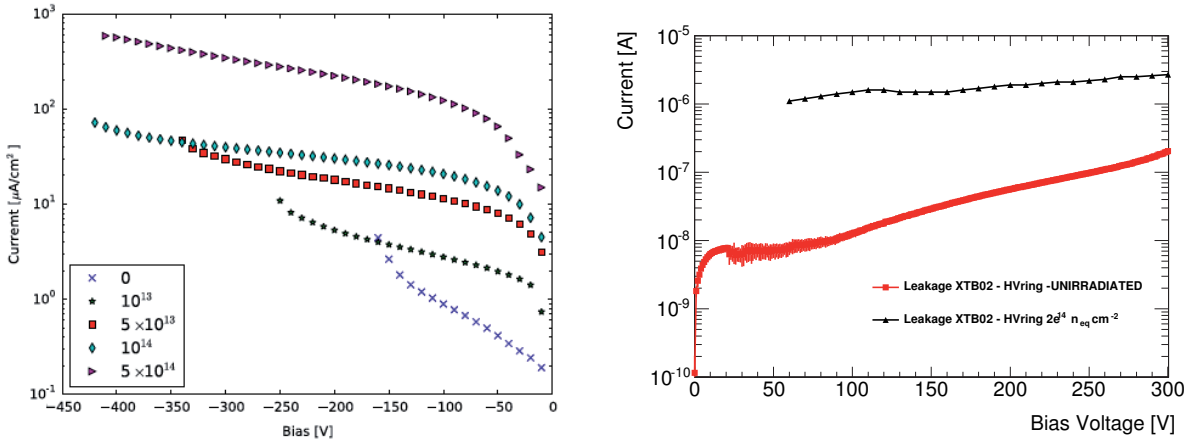


Figure 6.2: Current-Voltage curve comparison between prototype XTB01 and prototype XTB02. On XTB02 the leakage current decreases by a factor of ten and the breakdown voltage increases increases from 150 V to above 300 V.

The Current-Voltage curve was measured for irradiated and unirradiated samples in both prototypes at 25 °C with only the external ring biased. Figure 6.3a [97] shows the Current-Voltage curve of the XTB01 samples in logarithmic scale. It is observed that the leakage increases by a factor of hundred for the highest irradiated sample. In order to reduce the leakage current and in consequence the electronic noise, the temperature was kept at −30 °C during the following measurements. Figure 6.3b shows the Current-Voltage curve of XTB02 on an unirradiated sample and on sample irradiated up to 2×10^{14} $n_{eq}cm^{-2}$.



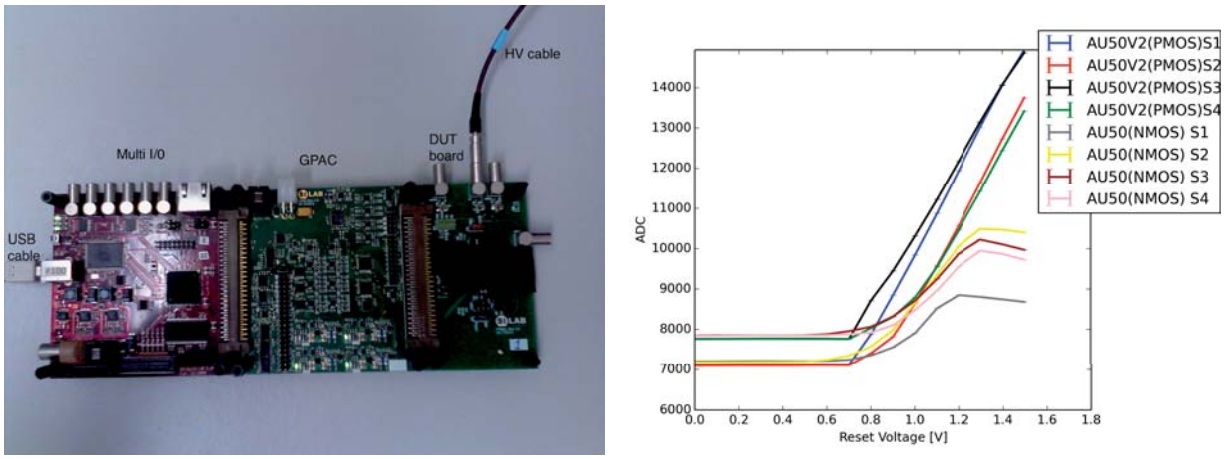
(a) (b)

Figure 6.3: (a) Current-Voltage curve on unirradiated and irradiated XTB01 samples at 25 °C when the HV ring was selected [97]. (b) Current-Voltage curve on unirradiated and irradiated XTB02 samples at 25 °C when the HV ring was selected.

6.2 3T-Cell circuit operation

The XTB01 prototype contains a 3T-cell circuit as pixel readout, which needs to be configured properly before any measurement can be performed. This is not true for the XTB02 prototype. The XTB02 prototype was specially produced in order to deeply investigate the charge collection properties of the sensor diode. Thus, it is a passive diode and the collection electrode is connected to an external amplifier, which avoids any limitations of on-chip amplification stages.

The single pixel of the XTB01 chip is configured through the XTB01 test system. The test system is composed of a Multi I/O board which makes the digital interface with the computer, a General Purpose Adapter Card (GPAC), which provides all the analogue functionalities to the chip, and a DUT board. The test system is shown in figure 6.4a. In addition, it allows monitoring of the analogue signal of the prototype using a fast on-board Analogue to Digital Converter (ADC), which is described in section 6.3.1.



(a) (b)

Figure 6.4: (a) XTB01 test system composed of a Multi I/O board, a GPAC, and a DUT board. (b) Analogue output in ADC as a function of the reset voltage of a single pixel in all the 50 µm × 50 µm sub-matrices. The reset transistor in the AU50 matrix is always a nMOS transistor while in the AU50V2 is a pMOS.

The 3T-cell circuit described in section 4.2.3 needs to be configured in a way that the input transistor works in linear mode. The pixel analogue output of an operative 3T-cell circuit was shown in figure 4.11. In that case, the step on the slope of the 3T-cell analogue signal is proportional to the accumulated charge. Thus, the performance of a reset voltage scan with the slope step for fixed values of the digital (DVDD) and analogue (AVDD) voltage is the first measurement in every sample. Figure 6.4b shows the reset voltage scan of a single pixel in

all 50 μm × 50 μm sub-matrices of the unirradiated sample for DVDD=AVDD=1.8 V. The y-axis shows the output voltage in ADC units. Both matrices AU50V2 and AU50 contain pixels of size 50 μm × 50 μm, as described in section 4.2.3. However, the reset transistor of matrix AU50V2 is pMOS type, and in matrix AU50 is nMOS type. As observed in figure 6.4b, in a AU50V2 pixel the input transistor works within the linear range for a reset voltage (V_{RST}) between 0.8 V and 1.5 V. However, in a AU50 pixel the input transistor saturates above 1.2 V. Thus, the reset voltage needs to be set between 0.8 V and 1.2 V. It is not understood why the nMOS reset saturates earlier than the pMOS transistor reset.

This measurement was performed in all samples and the operation parameters of all samples for matrix AU50V2 are listed in table 6.2. V_N is the voltage applied to the n-ring surrounding every matrix. This voltage determines the voltage seen by the outer pixels, and thus must be similar to the reset voltage.

	AVDD [V]	DVDD [V]	V_{RST} [V]	V_N [V]	Comments
0B, 2B, 3B	1.8	1.8	1.2	1.2	-
4B, 5B	-	-	-	-	no combination was found

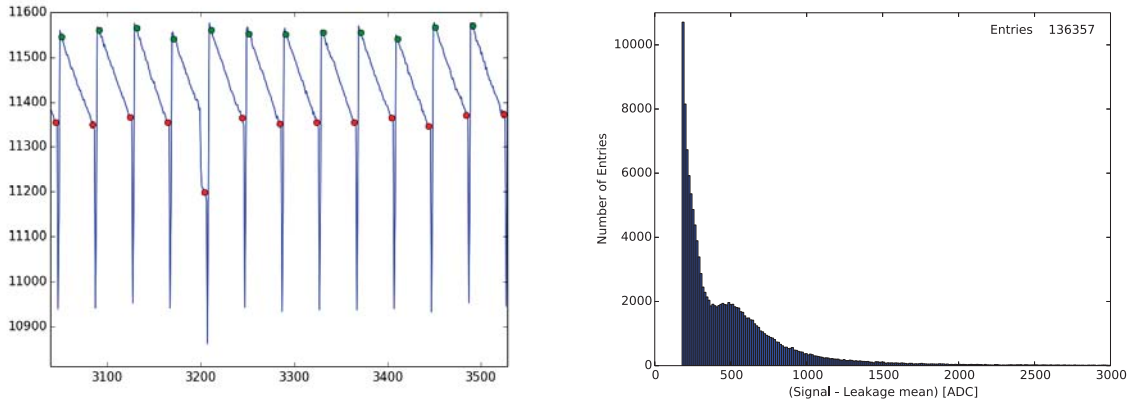
Table 6.2: List of the selected 3T-cell circuit parameters to operate each sample (matrix AU50V2) in order to make the input transistor working in the linear region.

6.3 Charge collection measurements with radioactive sources

Charge collection measurements with radioactive sources are performed to quantify the noise, signal size, and the depletion depth of a solid state detector for unirradiated and irradiated samples. Gamma sources are used for charge calibration measurements, since they deposit the full photon energy of the absorbed photons as described in section 2.1.3. The deposited energy distribution of the photon-peak is Gasussian and the mean value allows to obtain the calibration constant (k), which correlates the signal of the detector given in voltage to the charge collected by the detector. Beta sources are MIPs depositing energy all along the particle path as described in section 2.1.1. This measurement allows the understanding of the depletion depth and its evolution as a function of the bias voltage. The Most Probable Value (MPV) of the Landau distribution is used as a way to quantify the amount of collected charge.
This section describes the measurement setup, the signal distribution versus time distribution, the charge calibration, and charge distribution, and the depletion depth measurements on the XTB01 samples. XTB02 was very sensitive to noise sources in the laboratory environment, and gamma sources could not be measured.

6.3.1 Measurements method

The charge collection measurements with radioactive sources were performed by two methods. The first measurement method is a correlated double sampling method, typically used in case of 3T-cell circuit readout. This method uses the fast ADC on the GPAC. Figure 6.5a shows the pixel analogue output of the ADC. The fast ADC on the GPAC stores the pixel analogue output value after a reset (green dots) and before a reset (red dots), whose differences are computed and plotted. This histogram is used to extract the value of the electronic noise and the collected charge. Due to the lack of an online discrimination of hits and thus many empty samples, the noise contribution in the histogram is very large, and also the needed measurement time. Figure 6.5b shows the ^{90}Sr spectrum on a pixel of 50 µm × 50 µm at 150 V operated at 20 °C performed by this method. The measurement took 15 hours and around 140 000 events were needed to distinguish the signal peak from the noise. The signal from the ^{90}Sr corresponds to the small bump on the right, while the tail of the noise peak still dominates. Due to the noise contribution and the lack of charge collection time information a different measurement method and analysis was developed.

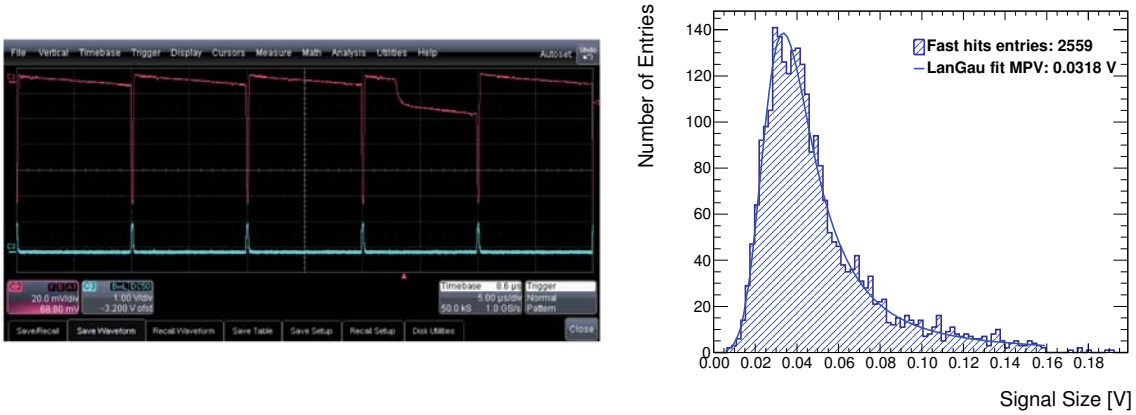


(a) (b)

Figure 6.5: Correlated Double Sampling readout of the 3T-cell circuit to measure the charge collection and electronic noise. (a) shows the ADC output versus time. The difference between the green and red points gives the collected charge by a signal or by leakage current. (b) shows the resulting ^{90}Sr spectrum at 150 V and 20 °C on a pixel 50 µm × 50 µm pitch in ADC units. The tail of the leakage current peak and the signal from the ^{90}Sr can be seen.

The developed measurement method consists of probing the analogue output signal of the pixel with an oscilloscope, storing the pixel analogue signal, and analyse the properties of the signals offline. This is possible by triggering on the signal, above a threshold slightly higher than the signal baseline, and vetoing the reset periods as shown in figure 6.6a. This let to record every waveform containing a hit and still some empty waveforms. An offline analysis was developed in order to select the waveforms containing a hit and to extract the collected charge and charge collection time. Figure 6.6b shows the ^{90}Sr spectrum on a 50 µm × 50 µm

pixel at 120 V and 0 °C performed by this method. The measurement took 1.5 hours and the obtained Landau distribution is very clean. Thus, this method was decided to be further used for all following measurements presented in this thesis. The previous results, using the correlated double sampling method, can be found in [97, 99].



(a) (b)

Figure 6.6: Developed measurement method to extract the charge collection, the charge collection time, detection time, and electronic noise (a) shows the analogue output signal of the pixel probed with an oscilloscope. The pixel analogue signal is stored and analysed offline. (b) shows the ^{90}Sr spectrum at 120 V and 0 °C on a pixel of 50 µm × 50 µm in ADC units.

The offline analysis goes through every stored waveform. The full process is summarized in figure 6.7. The algorithm first smooths the raw data without reducing the number of points as shown in figure 6.7a. Then, identifies the period between two resets in the reset signal. The identified period in the pixel analogue output is then used for the further analysis as shown in figure 6.7b (in such a case the reset is deleted). At that point, if the signal size is higher than an adjustable threshold, the analyser proceeds. Only events where the slew rate is above a certain threshold cut are further processed (figure 6.7c). In case a hit is detected, the following function is fitted and the collected charge and the charge collection time are obtained from the fit parameters:

$$\begin{aligned} t \leq t_0 \qquad & f = a + m \cdot (t - t_0) \\ t > t_0 \qquad & f = a + m \cdot (t - t_0) + b \cdot (e^{\frac{t-t_0}{c}} - 1) \end{aligned} \tag{6.1}$$

where t_0 the hit detection time, b is the collected charge, and c the charge collection time. If the mentioned cut is not passed, the waveform just contains the charge accumulated due to the leakage current, and no hit. Those cases are used to calculate the electronic noise, which is given by the RMS of the Gaussian distribution of the leakage current centered at zero. Figure 6.7d shows the Gaussian distribution of the pixel at a biased voltage of 120 V and 0 °C.

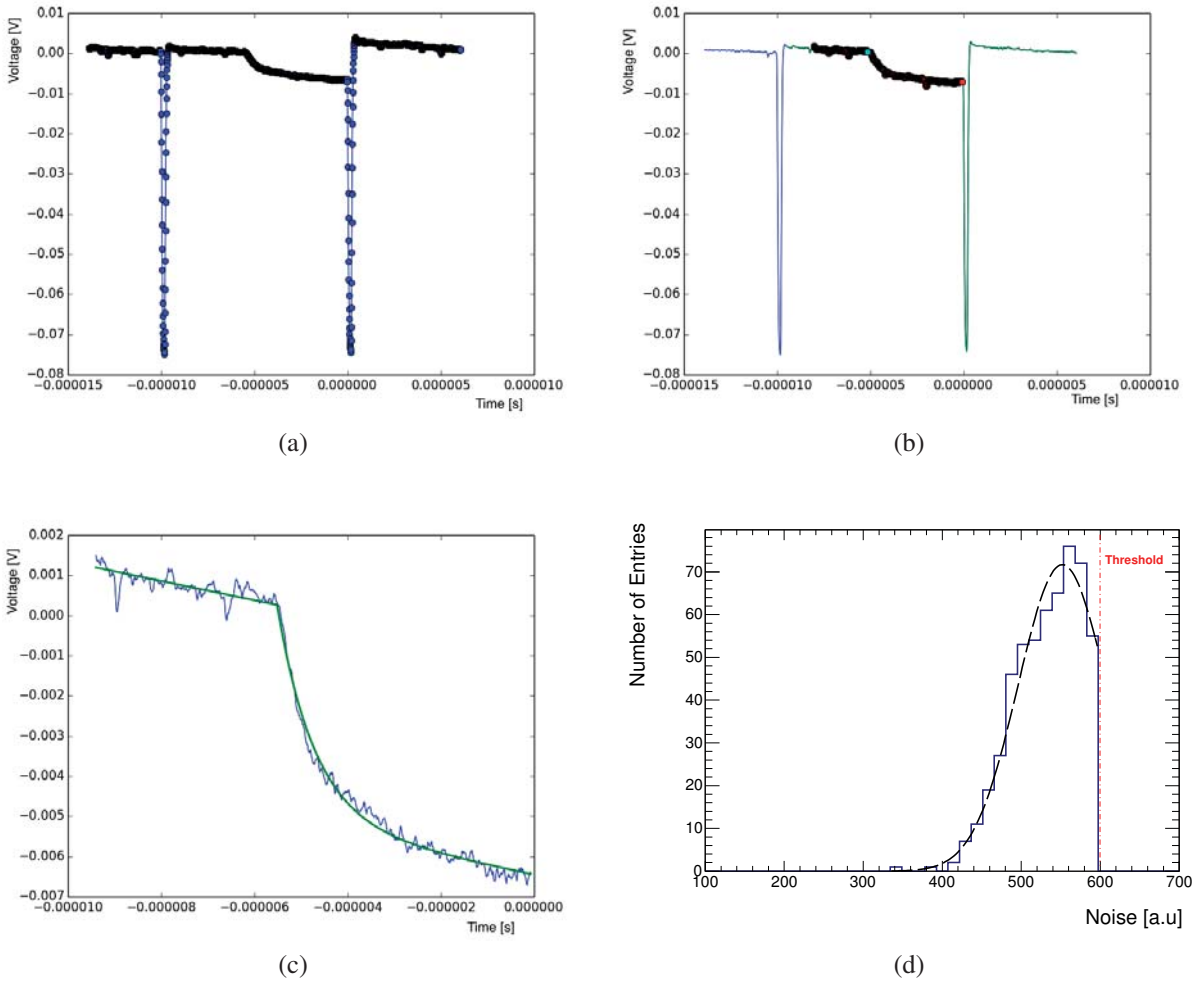


Figure 6.7: Developed readout algorithm as an alternative to the Correlated Double Sampling. The process is shown on a 50 µm × 50 µm pixel at a biased voltage of 30 V and 0 °C. (a) raw data smoothing (b) reset identification and removal (c) hit fitted to the function described in equation 6.1 to extract the collected charge and charge collection time. (d) Gaussian distribution of the leakage current on a 50 µm × 50 µm pixel at a biased voltage of 120 V and 0 °C.

6.3.2 MIP signal as a function of timing distribution

The signal size of the detector was measured in presence of a ^{90}Sr source as a function of the time distribution. The signal size versus charge collection time is shown in figure 6.8 for the unirradiated sample at 30 V and 120 V, for 1×10^{13} $n_{eq}cm^{-2}$ and 5×10^{13} $n_{eq}cm^{-2}$ samples at 120 V. When all the detected hits are considered in the unirradiated sample at 30 V (figure 6.8a), two different contributions to the collected charge are observed. Some hits are collected within 150 ns while others are collected much slower. By increasing the HV on the sample up to 120 V (figure 6.8b), the charge is collected faster and the slow contribution becomes smaller. This can be explained by the fact that device depletion depth increases by increasing the voltage and therefore the drift contribution to the collected charge increases as well. Additionally, the slow charge contribution completely disappears after irradiation as shown in figure 6.8c for sample 1×10^{13} $n_{eq}cm^{-2}$ at 120 V and 6.8d for sample 5×10^{13} $n_{eq}cm^{-2}$ at 120 V. This is explained by the trapping of the diffusing charge carriers in the silicon bulk. Thus, the slow component is interpreted as charge collection by diffusion and the fast component is interpreted as charge collected by drift.

In order to distinguish and to select the charge collected by drift from the charge collected by diffusion, a cut on the charge collection time over the collected charge is applied from now on. This cut corresponds to:

$$\frac{\text{CCT}}{\text{Signal Size}} \leqslant 0.743 \times 10^{-5} \tag{6.2}$$

and it is shown by a red line in figure 6.8. In what follows, the charge collection analysis will only consider the events that are below the selection cut defined by the red line in figure 6.8. This is also done for consistency on the irradiated sample, even if no significant change is observed on the results with the appliance of the cut.

These measurements confirmed the presence of diffusion and drift component on the collected charge, since the 300 µm thick sensor is partially depleted. A next version of the chip would be thinned down in order to strictly collect charge by drift. The ATLAS detector requires a in-time collection of 25 ns, which is only achieved by electrons collected by drift. The fact that the drift component of XTB01 seems to be about 150 ns as observed in figure 6.8 is just due to the slow 3T-cell readout. The selection criteria described above allows to decouple the diffusion and the drift contribution, and select only the drift component for further characterization.

6.3.3 Calibration and charge distribution

A 370 MBq ^{55}Fe radioactive source was used to make the charge calibration of the device. Other radioactive sources were available, but due to the source activity and small pixel size, the rate was too low (order of 1 particle/10 min) to make it feasible for this study. The particle

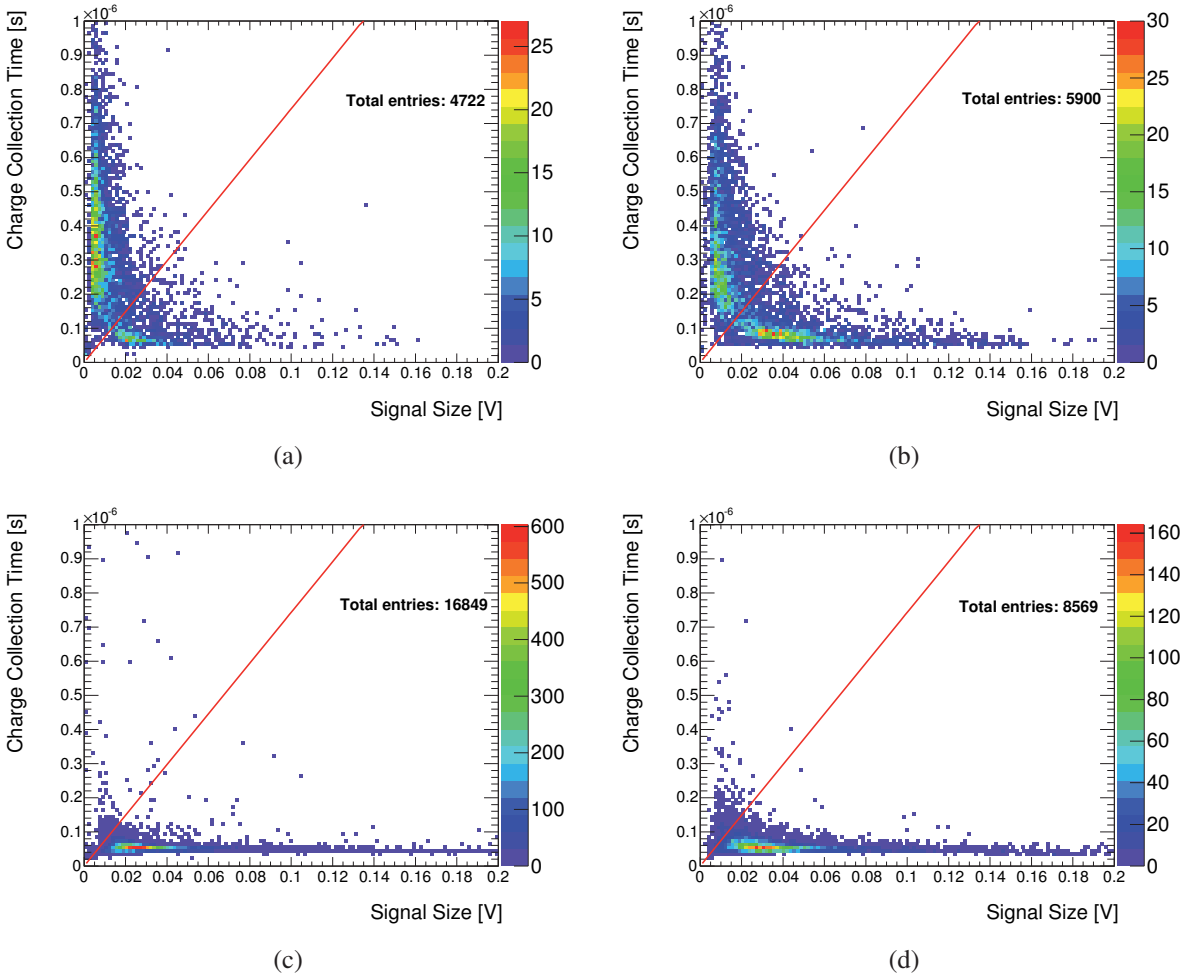


Figure 6.8: Collected charge versus charge collection time on a 50 µm × 50 µm XTB01 pixel in presence of ^{90}Sr source (a) unirradiated sample at 60 V (b) unirradiated sample at 120 V (c) 1×10^{13} $n_{eq}cm^{-2}$ neutron irradiated sample at 120 V (d) 5×10^{13} $n_{eq}cm^{-2}$ neutron irradiated sample at 120 V. The charge collected more slowly decreases with high voltage, and it disappears after irradiation.

rate of 370 MBq ^{55}Fe on a 50 µm × 50 µm pixel located at 5 cm distance from the source is:

$$^{55}\text{Fe particles rate} = \frac{50\,\mu\text{m} \times 50\,\mu\text{m}}{4\pi(5 \times 10^4\,\mu\text{m})^2} \cdot 370 \times 10^6\,\text{particles/s} = 29\,\text{particles/s} \tag{6.3}$$

The single pixels of matrix 100 µm × 100 µm showed saturation when a source was placed on top as depicted in figure 6.9. The pink line corresponds to the pixel analogue signal, and the change in slope after the MIP has passed through the pixel indicates saturation. In that case the step size of the slope is not proportional to the collected charge. Thus, measurements on 100 µm × 100 µm pixel sizes could not be performed. A compromise between time and amount of measurements made us discard the 25 µm × 25 µm pixels. Thus, all following measurements performed in XTB01 correspond to single pixels of size 50 µm × 50 µm from matrix AU50V2. The following measurements were performed to a temperature of 0 °C in the unirradiated sample, and −30 °C in the irradiated samples, to reduce the leakage current and therefore the noise.

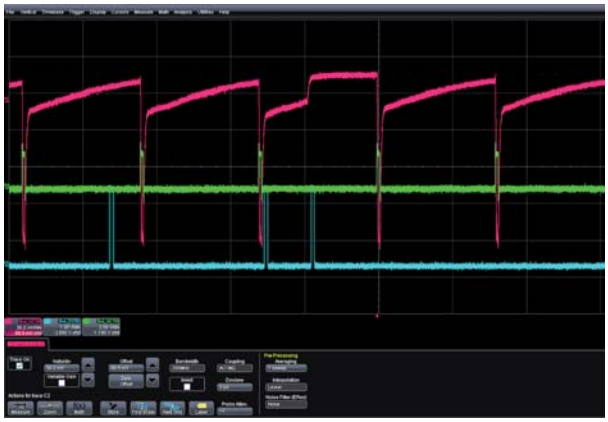
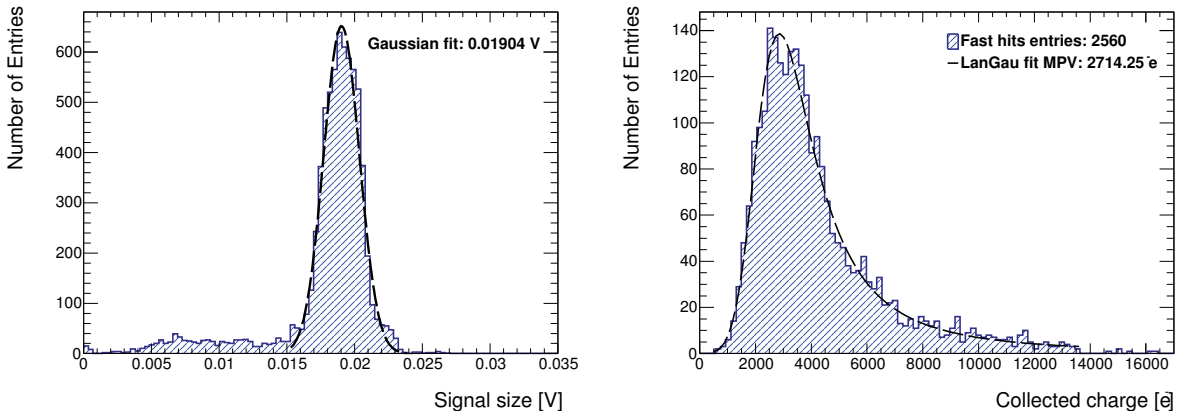


Figure 6.9: Analogue pixel signal of a 100 µm × 100 µm pixel (in pink) exposed to 160 GeV pions. The change in slope after the passage of the MIP through the pixel indicates saturation.

The ^{55}Fe spectrum of a 50 µm × 50 µm pixel of the unirradiated sample, biased to −100 V at 0 °C is shown in figure 6.10a. The mean value of the fitted Gaussian is 0.019 04 V which corresponds to 5.9 keV. This allows to calculate the calibration factor (k):

$$k[V/e^-] = \frac{mean[V]}{5900\,\text{eV}} \cdot 3.61\,\text{eV/e}^- \tag{6.4}$$

where 3.61 eV/e$^-$ is the electron affinity introduced in section 2.2.1. The width of the Gaussian fit, σ, corresponds to the charge resolution of the detector and gives the systematic error. The uncertainty on the mean value of the fit, σ_{mean}, is the statistical error, which is here negligible with respect to the systematic.



(a) (b)

Figure 6.10: Charge calibration and charge distribution on 50 µm × 50 µm XTB01 pixel unirradiated. (a) It shows the ^{55}Fe spectrum at 100 V and 0 °C. (b) It shows the ^{90}Sr spectrum in electron units of the same pixel at 120 V and 0 °C.

The systematic error is calculated by the Gaussian error propagation:

$$\sigma_k^{sys} = \sqrt{\left(\frac{\partial k}{\partial mean}\right)^2 \cdot \sigma^2} \tag{6.5}$$

approximating the electron affinity to be constant. The statistical error is derived from the Gaussian fit. Thus, the conversion factor of the unirradiated sample is k=(11.65 ± 0.79$_{(sys)}$ ± 0.01$_{(stat)}$) × 10^{-6} V/e$^-$. The calibration factor is used to determine the collected charge by the ^{90}Sr in electron units using:

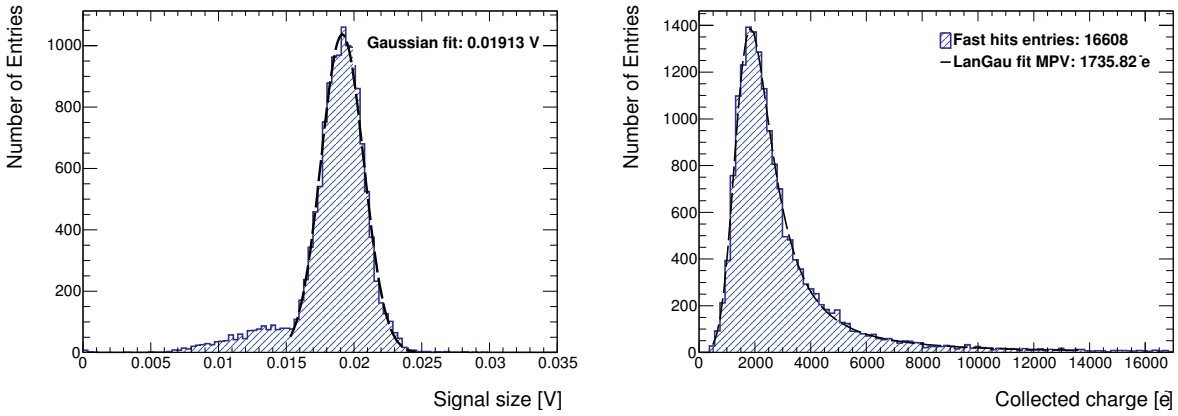
$$Q[e^-] = \frac{1}{k[V/e^-]} \cdot MPV[V] \tag{6.6}$$

whose systematic error calculated by the Gaussian error propagation is

$$\sigma_{Q(e^-)}^{tot} = \left(\sqrt{\left(\frac{\partial Q}{\partial MPV}\right)^2 \cdot \sigma_{MPV}^2}\right)^{stat} + \left(\sqrt{\left(\frac{\partial Q}{\partial k}\right)^2 \cdot \sigma_k^2}\right)^{sys} \tag{6.7}$$

The ^{90}Sr spectrum of the same pixel at −120 V is shown in electrons in figure 6.10b. All the hits detected within the selection criteria described in section 6.3.2 were considered. The most probable value of the Landau fit corresponds to 2714.25 ± 219.20$_{tot}$ e$^-$ whose total error is calculated with equation 6.7. This value divided by 60 e$^-$ /µm, which is a reasonable approximation for this thin detector layer according to [104], gives a depletion depth of 33.9 ± 2.7$_{tot}$ µm. This value agrees with the theoretical depletion depths calculated to be 34.8 µm for 100 Ω· cm material at 120 V bias voltage using equation 2.12.

The same measurements were performed for the irradiated samples. Figure 6.11 shows the ^{55}Fe and ^{90}Sr spectrum of a 50 µm × 50 µm pixel for the sample irradiated to 1×10^{13} $n_{eq}cm^{-2}$. The mean value of the fitted Gaussian is nearly the same than in the unirradiated sample. This is explained by the fact that photons deposit their energy at the surface and no long drift is required. Thus the effect of trapping is negligible in this case. The conversion factor of this sample is $k = (11.71 \pm 0.97_{(sys)} \pm 0.01_{(stat)}) \times 10^{-6}$ V/e$^-$ and the most probable value of the Landau distribution in the ^{90}Sr measurement is $1735.82 \pm 143.96_{(tot)}$ As expected, the collected charge by the irradiated sample is lower than by the unirradiated sample at the same voltage. That is due to the trapping generated in the bulk due to irradiation.



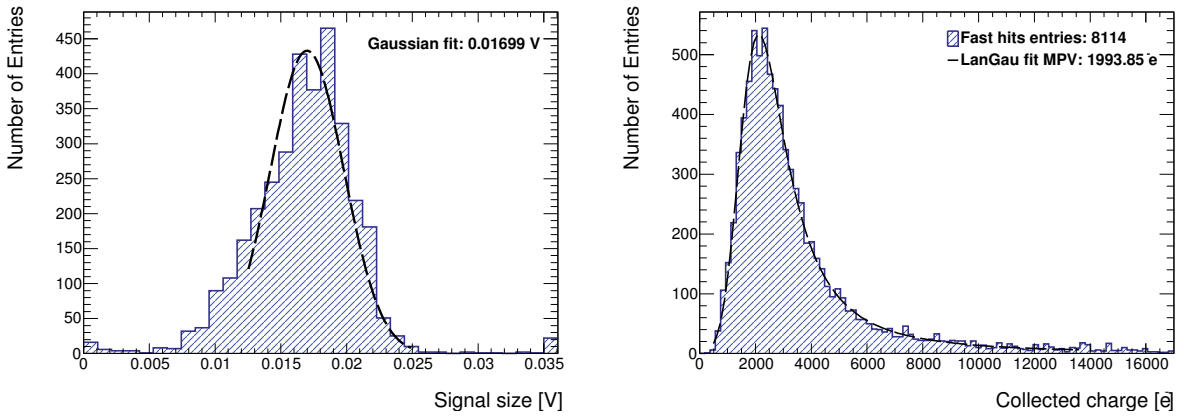
(a) (b)

Figure 6.11: Charge calibration and charge distribution on 50 µm × 50 µm XTB01 pixel irradiated to 1×10^{13} $n_{eq}cm^{-2}$. (a) It shows the ^{55}Fe spectrum at 100 V and −30 °C. (b) It shows the ^{90}Sr spectrum in electron units of the same pixel at 120 V and −30 °C.

The ^{55}Fe and ^{90}Sr spectrum of a 50 µm × 50 µm pixel in the neutron irradiated sample to 5×10^{13} $n_{eq}cm^{-2}$ is shown in figure 6.12. The ^{55}Fe shows a weird shape which does not exactly match to a Gaussian distribution. Thus, for calibration the conversion factor of 10^{13} $n_{eq}cm^{-2}$ irradiated sample was used. The most probable value in the ^{90}Sr scan is $1993.85 \pm 165.71_{(tot)}$

As described in section 6.2, the samples irradiated to 1×10^{14} $n_{eq}cm^{-2}$ and 5×10^{14} $n_{eq}cm^{-2}$ presented a strange behaviour. None parameter combination was found to make their input transistor work within the linear region, and no further measurements could be performed.

These results prove the excellent charge collecting properties of the 180 nm SOI XTB01 monolithic prototype on unirradiated and irradiated samples. This prototype is comparable to other CMOS prototype approaches being investigated as described in section 4.2.

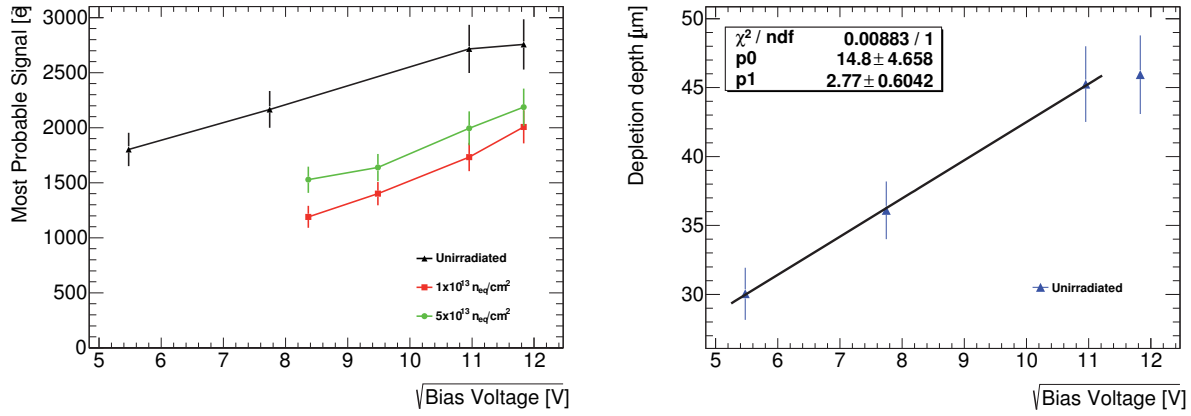


(a) (b)

Figure 6.12: Charge calibration and charge distribution on 50 µm × 50 µm XTB01 pixel irradiated to 5×10^{13} $n_{eq}cm^{-2}$. (a) It shows the ^{55}Fe spectrum at 100 V and −30 °C. (b) It shows the ^{90}Sr spectrum in electron units of the same pixel at 120 V and -30 °C.

6.3.4 Source bias voltage scan and depletion depth formation

Subsequently a source scan at different voltages was performed for the unirradiated and neutron irradiated samples to 1×10^{13} $n_{eq}cm^{-2}$ and 5×10^{13} $n_{eq}cm^{-2}$. Figure 6.13a shows the most probable value versus the bias voltage for all samples. First, it is observed that the MPV grows



(a) (b)

Figure 6.13: Source bias voltage scan and depletion depth formation on XTB01. (a) It shows the most probable value of the collected charge versus voltage for all the samples at different voltages. The sample irradiated to 5×10^{13} $n_{eq}cm^{-2}$ collects more charge than sample 1×10^{13} $n_{eq}cm^{-2}$ at same conditions. (b) It shows the depletion depth versus voltage for the unirradiated sample.

linearly with the square root of the voltage. That is expected since the MPV is proportional to the depletion depth, and this one to the square root of the applied voltage as shown in equa-

tion 2.12. Second, it becomes visible that the sample irradiated to $5 \times 10^{13}\,\mathrm{n_{eq}cm^{-2}}$ collects more charge than the sample irradiated to $1 \times 10^{13}\,\mathrm{n_{eq}cm^{-2}}$ at the same conditions. A similar behaviour has been observed for low resistivity substrates ($10 - 20\,\Omega\cdot$ cm) by G. Kramberger, I. Mandic et al [76]. This could be explained by the Acceptor Removal Effect described in section 3.2.3. This effect is being investigated on this prototype and it is briefly described in section 6.5. The depletion depth was calculated using the most probable value of the Landau distribution divided by $60\,\mathrm{e^-}$ /µm for the unirradiated sample. The resulting depletion depth as a function of the voltage is shown in 6.13b. The depletion is proportional to the square root of the bias voltage, as expected.
Furthermore, according to equation 2.8, the slope of the applied linear fit ($Depletion = p1 \cdot \sqrt{V} + p0$) corresponds to:

$$p1 = \sqrt{2\epsilon\mu\rho} \tag{6.8}$$

This allows the extraction of the bulk resistivity. The measured resistivity is $82\,\Omega$ cm. Keeping in mind that the depletion depth measurement is an indirect measurement the extracted resistivity value is in very good agreement with the $100\,\Omega$ cm resistivity of XTB01. This result is confirmed by the direct measurement of the depletion depth using the edge transient current technique in section 6.4.2.
This step is not performed on the irradiated samples because the $60\,\mathrm{e^-}$ /µm rule is not valid in the presence of trapping. Instead, the depletion depths on irradiated samples can be better investigated using the edge transient current technique measurements.

6.4 Position resolved charge collection behaviour

The edge Transient Current Technique (eTCT) measurements study the development of the depletion region and its corresponding electric field within a silicon detector [105]. Infra-red laser pulses (1064 nm) of 150 pico seconds penetrate the device through the sensor edge generating a path of electron hole pairs. The movement of these charge carriers in the presence of an electric field induces a current signal on the readout electrode of the DUT. The properties of the electrical field can be extracted from the shape of the induced signal on the electrodes. Moving the sample perpendicular to the focused laser beam allows to determine the shape and properties of the depleted region. The eTCT measurements were performed in the setup of the CERN SSD group. These measurements were later on repeated in Ljubljana to confirm the presence of the Acceptor Removal Effect in the XFAB technology. These measurements were performed on the matrix II-A of prototype XTB02, described in detail in section 4.2.3.

6.4.1 edge Transient Current Technique setup

The eTCT measurements were performed on the matrix II-A of prototype XTB02, whose resistivity is $100\,\Omega$ cm. A mistake on the Printed Circuit Board (PCB) did not make possible the foreseen characterization on matrix I-A. Figure 6.14 shows the pixels cross section of matrix II-A. Matrix II-A contains a 4×4 pixels array of a $100\,\mu\mathrm{m} \times 100\,\mu\mathrm{m}$ pixel size. The n-well

size is 40 µm × 50 µm. As described in section 4.2.3, this chip contains a inter pixel insulation structure so called p-field, which can be biased. It also contains an outside ring so called GR-field which can be biased, too. Matrix II-A allows the readout of a single central pixel or its entire array expect the central pixel.

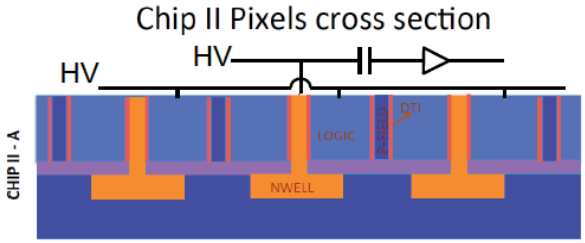
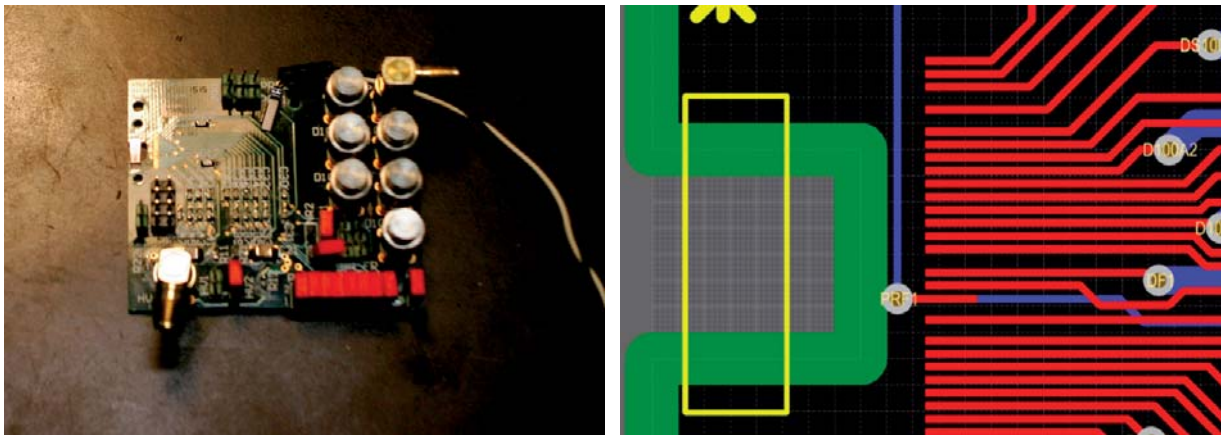


Figure 6.14: Three pixels cross section of matrix II-A (XTB02 prototype). The bias voltage settings are indicated. Dimensions are not to scale.

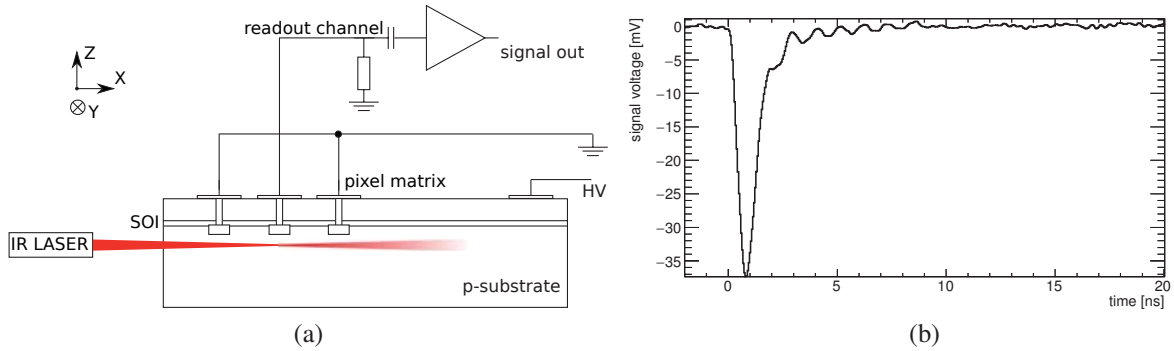
A dedicated PCB was produced to allow the eTCT measurements performance. Several wire-bond connections were placed to access to the HV ring from where the bias voltage is applied, GR-field, p-field structures, logic, single pixels, and pixel arrays. Figure 6.15a shows the PCB with the XTB02 chip glued on top. The single diodes were accessible by right SMA connectors, while high voltage is applied from the left SMA connector, and the different bias conditions are selected by jumpers. The XTB02 chip is glued close to the PCB edge to avoid reflections and on top of the PCB hole, which allows shooting with the laser from the bottom, known Transient Current Technique (TCT) measurements. Figure 6.15b shows an schema of the position of the XTB02 chip (yellow) on the PCB.



(a) (b)

Figure 6.15: Photo and schema of the XTB02 PCB for eTCT measurements. (a) It shows the XTB02 glued on the dedicated PCB to perform eTCT measurements. (b) Schematic of the location of XTB02 (yellow) on the PCB.

The readout and biasing scheme used for eTCT measurements on our single pixel is illustrated in figure 6.16a. The single diode is connected to the oscilloscope while the others are connected to a 50 Ω termination in order to have the same conditions. The high voltage is applied from the external HV ring. The induced current signal in the passive diode is shown in figure 6.16b is amplified by a fast current amplifier (40 dB) and recorded by a high bandwidth oscilloscope. The integration time used to calculate the collected charge was 5 ns. All scans were performed at room temperature.



(a) (b)

Figure 6.16: (a) schematic drawing of the edge TCT measurement setup showing the readout scheme for a single pixel. (b) current signal induced during a edge TCT measurement in the center of the depletion region of matrix 2A at 300 V.

6.4.2 Charge collection and depletion depth

The minimum spatial resolution of the measurement depends on the Gaussian width of the focused laser spot. This corresponds to $\sigma = 10\,\mu m$ for the CERN setup. Thus, one need to take into account that structures below 40 µm are dominated by the contribution of the laser and are overestimating the real structure width. This is due to the fact that the measurement represents a convolution of the depletion region and the width of the laser.

Several *zy* scans were performed on the 100 µm × 100 µm single central pixel at different biasing voltage where the p-field and GR-field structure were kept floating and the logic was grounded. Figures 6.17a and 6.17b show the *zy* scan at 100 V and 300 V respectively. The grey line represents the BOX and the black lines the pixel pitch. The depletion depth is then identified, and its growth with voltage is clearly observed. From figure 6.17b can be concluded that the depletion depth can be increased up to 60 µm for a bias voltage of 300 V. The depletion depth in the *z* axis (bulk direction) agrees with the results of the source measurements in the laboratory described in section 6.3.4. The depletion depth in the *y* direction seems to increase with HV in a different way. In a 100 µm × 100 µm pixel with 40 µm × 50 µm n-well we expect that the remaining 30 µm at the sides of the n-well were fully depleted at 100 V. However, neither at 300 V the pixel seems to be fully depleted in the *y* direction. The region in which

higher charge is collected corresponds to the region below the n-well where the electric field is highest.

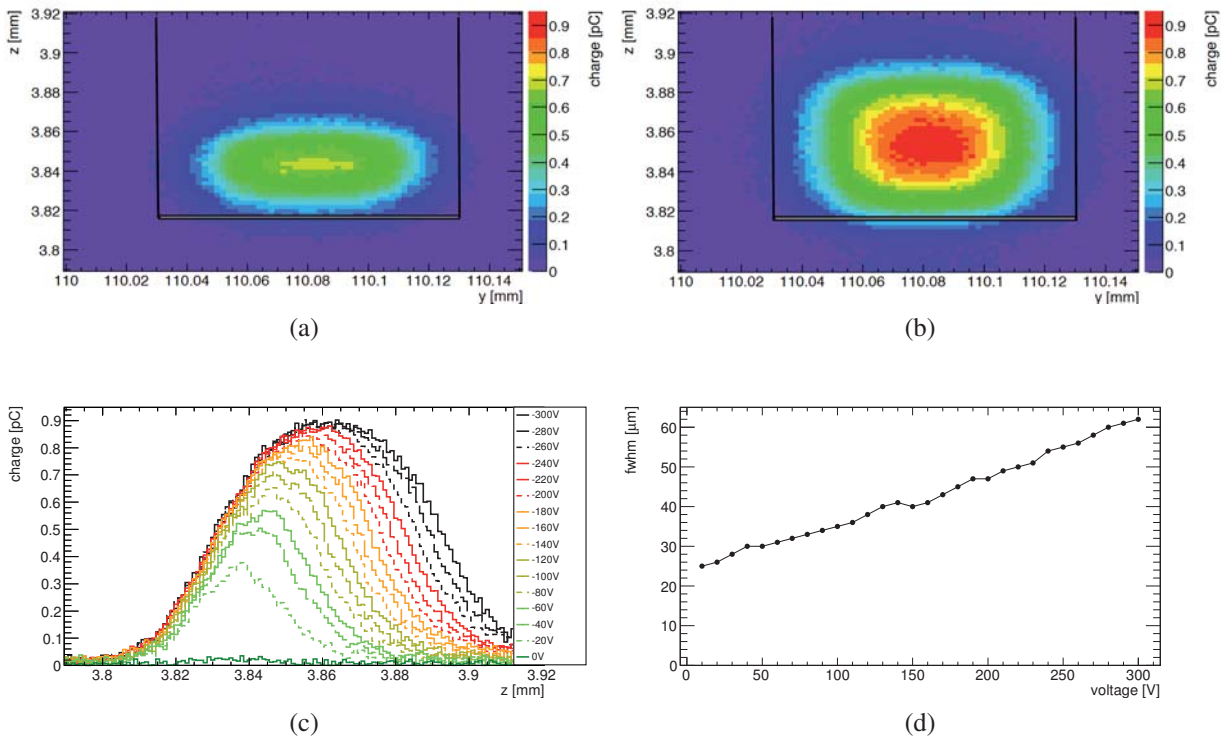
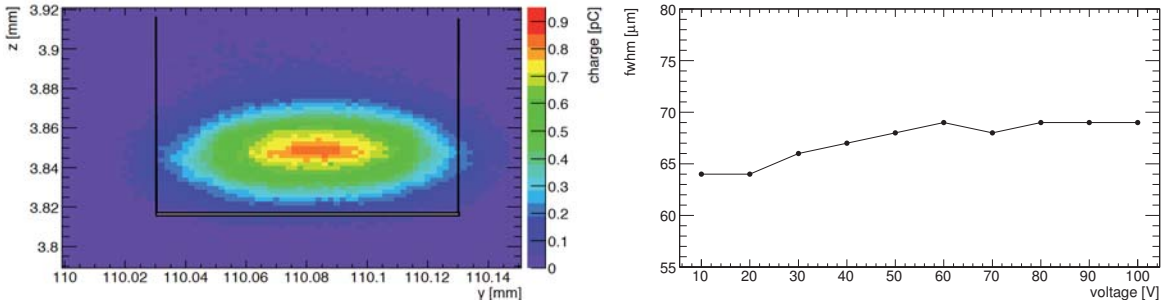


Figure 6.17: Depletion depth growth on a single pixel of 100 µm pitch in matrix II-A where the p-field structure was kept floating. A ZY scan is shown for different bias voltage (a) 100 V an (b) 300 V, whereas (c) shows the collected charge for a bias voltage range from 0 V to 300 V versus depth and (d) the FWHM as measure of the depleted zone in the z direction versus the voltage.

The collected charge along the z axis of the pixel for bias voltages at the external bias ring ranging from 0 - 300 V is shown in figure 6.17c. The p-field and GR-field were kept floating, and the logic was grounded. The FWHM in the z direction can be considered as the depletion depth. Figure 6.17d shows the FWHM in the z direction extracted from figure 6.17c versus the applied voltage. The depletion depth does not grow linearly to the square root of the bias voltage due to the fact that the measurement is dominated by the laser width as mentioned before.

To investigate the effect of the p-field structure on the depletion zone, the p-field structure was biased to different voltages for a fixed bias voltage of the external ring of 100 V. Figure 6.18a shows the zy scan on the single pixel at a bias ring voltage of 100 V when the p-field was biased to 100 V. These results can be compared with Figure 6.17a where the p-field was kept floating. The change of the shape shows that the potential of the p-field influences the depletion in the y direction. To quantify this change, the FWHM was extracted from the collected charge

at different voltages at the p-field in *y* direction as shown in figure 6.18b. An increase of about 5 µm is observed when increasing the p-field potential from 20 V to 60 V. The depletion depth *z* direction seemed to be independent of the applied p-filed voltage and stayed at about 34.5 µm. An extensive study using TCAD simulations has been started to investigate the field distribution in the substrate.

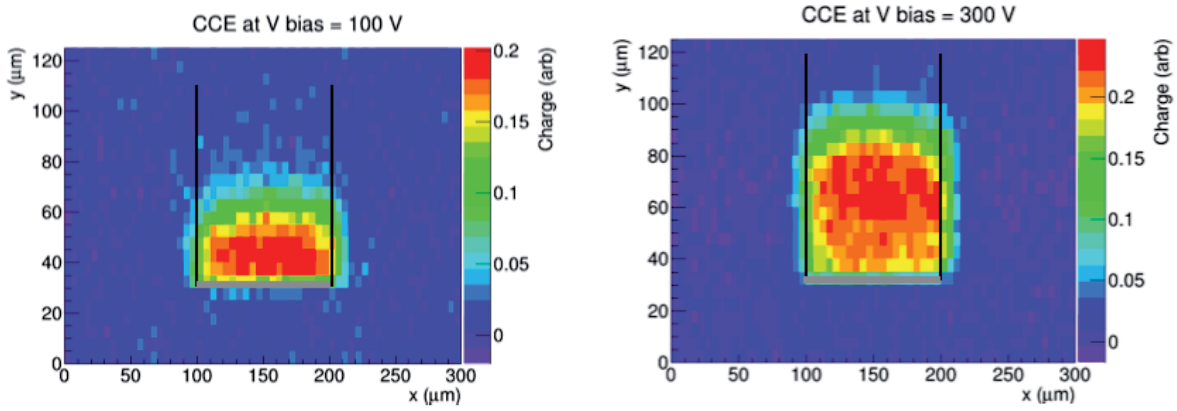


(a) (b)

Figure 6.18: Depletion depth growth on a single pixel of 100 µm pitch in matrix II-A where the external bias ring is kept constant at 100 V and the p-field structure is biased at different voltages. (a) shows a ZY scan for 100 V applied on both, the external ring and the p-field. (b) shows the depletion depth in the *y* direction in function of the p-field voltage for 100 V at the external bias ring.

Similar results have been observed by colleagues at Ljubljana. Figure 6.19 [106] shows the *yx* scan of the single central pixel at 100 V and 300 V performed in Ljubljana. The y and x axis on the Ljubljana setup corresponds to the z and y axis, respectively, on the CERN setup. Thus the plots on figures 6.17 and 6.19 are comparable. These measurements were performed with p-field, GR-field, and the logic floated. Previous measurements on an unirradiated chip would have indicated that keeping the logic floating or grounded does not have an effect. The resolution at the Lujbiana setup is about $\sigma = 6$ µm and the integration time used to calculate the collected charge was 25 ns. This explain that the diode shape is sharper here. On the bulk direction the depletion depth is similar, while in the lateral direction the diode seems completely depleted here. This may be related to the setup resolution or to the logic bias condition, which was the only different parameter used in both setups.
Additionally, the better resolution at the Ljubljana setup allowed to extract and correctly interpret the depletion depth from the FWHM as shown in figure 6.20 for the single central pixel [106]. The depletion depth values are fitted to equation 2.12, which leads to a resistivity of 109 Ω cm. This value is in agreement with the 100 Ω cm prototype resistivity.

From the eTCT measurements can be concluded that the depletion depth can be increased up to 60 µm for a bias voltage of 300 V for unirradiated samples, which fits to the results obtained by radioactive source measurements in section 6.3.4.



(a) (b)

Figure 6.19: Depletion depth growth on a single pixel of 100 µm pitch in matrix II-A performed in Ljubljana [106] (a) at 100 V with p-field and logic floating (b) at 300 V with p-field and logic floating. The depletion depth growth is in agreement with the measurements performed at CERN (figure 6.17).

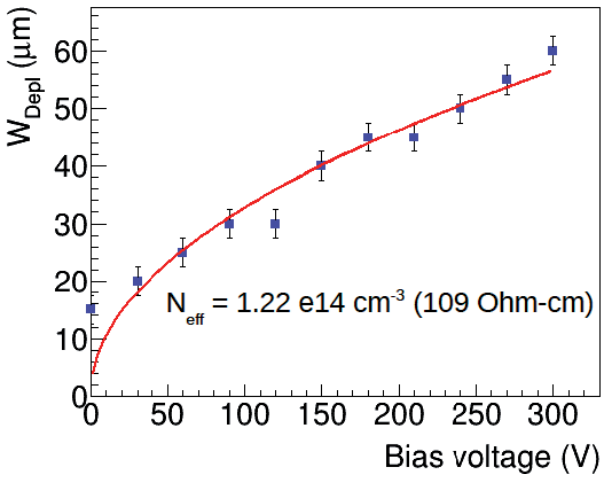


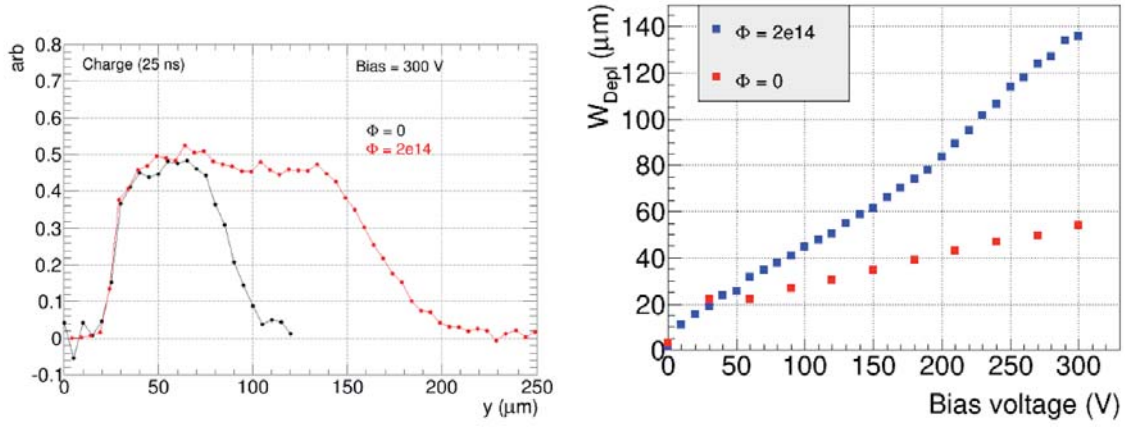
Figure 6.20: Depletion depth of XTB02 at different bias voltage when a single pixel is readout [106]. The depletion depth was extracted from the FWHM in the *y*-axis.

6.5 Acceptor Removal effect

The Acceptor Removal effect, explained in section 3.2.3, describes how radiation induces the removal of acceptors causing a decrease in effective doping concentration N_{eff}.
The variation of N_{eff} as a function of the fluence when taking into account the Acceptor Removal effect was shown in equation 3.5. According to it, the radiation produces a decrease in N_{eff} up to a certain fluence. This fluence is depends on the initial doping concentration. Thus, the depletion zone depth explained in section 2.2.2 and given by equation 2.8 increases.

Experimental measurements in low resistivity ($10 - 20\,\Omega\cdot$ cm) p-type silicon material have shown an increase in the signal after irradiation up to $2 \times 10^{15}\,\mathrm{n_{eq}cm^{-2}}$ [76].

The characterization of irradiated samples with radioactive sources described in section 6.3.4 brought up hints to the presence of acceptor removal on the XFAB technology. This is being investigated at the moment in Ljubljana with the performance of eTCT measurements from where the depletion depth is extracted versus fluence on matrix II-A. Some preliminary results are shown here. Figure 6.21a [106] shows the collected charge along the sensor depth on the single pixel at 300 V for an unirradiated and a $2 \times 10^{14}\,\mathrm{n_{eq}cm^{-2}}$ neutron device. The integration time used to calculated the collected charge was 25 ns, and p-field, GR-field and logic were kept floating in both devices. After irradiation a large increase of the collection depth is observed.



(a) (b)

Figure 6.21: (a) shows the collected charge along the sensor depth on a single XTB02 pixel at 300 V unirradiated and neutron irradiated to $2 \times 10^{14}\,\mathrm{n_{eq}cm^{-2}}$ [106]. (b) shows the depletion depth on a single XTB02 pixel for unirradiated and the $2 \times 10^{14}\,\mathrm{n_{eq}cm^{-2}}$ neutron irradiated device [106].

The depletion depth was extracted from the FWHM in the y axis at different bias voltage. Figure 6.21b [106] shows the depletion depth for the unirradiated and neutron irradiated to $2 \times 10^{14}\,\mathrm{n_{eq}cm^{-2}}$ device. After irradiation the depletion depth deviates from the behaviour

expected from equation 2.8. This is a strong evidence pointing to the reduction of N_{eff}, and the Acceptor Removal Effect. Further measurements will be performed in the coming months for different fluences to confirm these preliminary results.

The discovery of the acceptor removal effect in the XFAB prototype would make this technology very attractive. High resistivity would not be needed to increase the collected charge, at least for applications up to 2-3 $\times 10^{15}$ $n_{eq}cm^{-2}$ [107].

Chapter 7

Test beam characterization

Beam tests are crucial for performance characterization and optimization of any particle detector. The unirradiated XTB01 device was placed in a test beam for the first time during 2014 and 2015, where a single 50 µm × 50 µm pixel was monitored and read out. The data presented in this thesis were recorded in 2015 at the CERN SPS North Area beam line H6 with a beam energy of 120 GeV pions. The trajectories of the beam particles were reconstructed using the AIDA SBM FE-I4 telescope. This chapter is divided into two main sections. Section 7.1 describes in detail the testbeam instrumentation as well as the AIDA SBM FE-I4 telescope and the DUT readout. Section 7.2 discusses the measurements performed and the results obtained.

7.1 Test beam instrumentation

The Super Proton Synchrotron (SPS) at CERN is the second-largest machine in CERN's accelerator complex with nearly 7 kilometres of circumference. It receives particles from the Proton Synchrotron (PS) and accelerates them to provide beams to the LHC, and to other experiments as the NA61/SHINE, NA62, COMPASS or the CNGS project. The CERN accelerator complex is illustrated in figure 7.1. As observed SPS also provides beam to the North Area. This area is mainly used for test beam measurements. The North Area is divided in different lines, which provide different beam properties. The test beam measurements presented in this thesis were performed at the beam line H6 with a beam energy of 120 GeVπ^+. The high momentum of the beam particles minimizes the effect of multiple scattering, which is a prerequisite for high-precision tracking measurements.

7.1.1 AIDA SBM FE-I4 telescope

The telescope aligned to the beam direction and used to reconstruct the trajectories of the beam particles was built by the CERN group during 2014. A significant contribution to its construction and commissioning was done in the framework of this thesis. Its name is AIDA SBM FE-I4 telescope. The AIDA SBM FE-I4 telescope mechanics are rather compact with a size of 60 cm×20 cm×20 cm and a weight of 4 kg. It is composed of two telescope arms, which are movable independently along the global z and y axes as shown in figure 7.2. The space between the arms, configurable up to a maximum of 40 cm, is used to place the DUT. The telescope is equipped with six single-chip FE-I4B modules with silicon planar sensors [84], three per telescope arm, with a 250 × 50 µm pitch in its local x and y directions respectively,

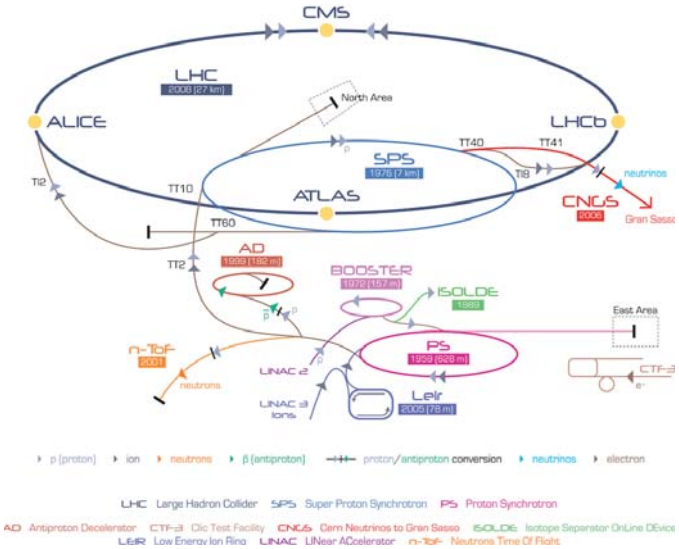
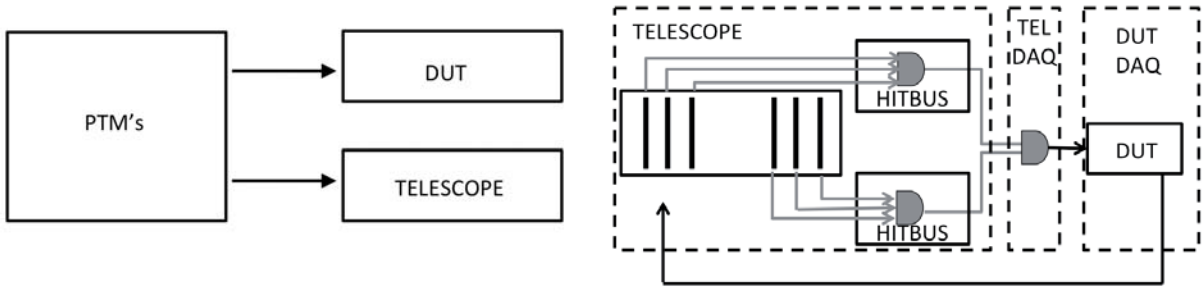


Figure 7.1: Schema of the CERN accelerators complex. The SPS provides beam to the so-called North Area, where the test beam measurements take place.

and an active area of $\sim 2 \times 2\,\mathrm{cm}^2$. Every second plane is rotated by 90° along the global z axis in order to achieve $\sim 8\,\mu\mathrm{m}$ resolution in both directions. In addition, plane 1, 3, 4 and 6 can be tilted by 0°, 15° and 30° along its local y axis in order to increase the cluster size, and therefore the position resolution.

Figure 7.2: Photo of the AIDA SBM FE-I4 telescope. The two telescope arms are movable along the z and y axes.

The AIDA SBM FE-I4 telescope triggering block diagram is sketched in figure 7.3. The telescope trigger can be applied externally as in other telescopes through external Photo Multipliers (PMTs) (figure 7.3a). Additionally, as a novel technique, the telescope trigger can be applied internally through the Hitbus chip which provides online track Region-of-Interest (ROI) triggering. This is sketched in figure 7.3b. The Hitbus chip handles the HitOr trigger functionality of the FE-I4 planes. There are two Hitbus chips, one per arm, so that simultaneously hits can be requested in all six telescope planes.



(a) (b)

Figure 7.3: AIDA SBM FE-I4 telescope trigger schema showing on (a) the external trigger possibility using the PMTs and on (b) the internal trigger possibility through the Hitbus chip.

The AIDA SBM FE-I4 telescope readout consists of two Reconfigurable Cluster Element (RCE) systems, and one High Speed Input Output (HSIO) board. The RCE software was modified to incorporate the Hitbus triggering. Currently the analysis is performed using the Judith software [108] but converters to the EUTelescope [109] file format are available.

The DUT readout system used for the presented XTB01 measurements is explained in detail in section 7.1.2. A DUT with digital output can be considered as an extra plane of the telescope and be readout using the RCE system, which would internally synchronize the telescope and DUT data. This is the usual approach in other testbeams. On the other hand, any DUT with analogue output can be readout by an additional analogue readout system. In this case, a combination of the one-directional online synchronization shown in figure 7.3b and offline synchronization is used to synchronize the data, typically using timestamps. This is the method used in the testbeam measurements presented here.

7.1.2 XTB01 analogue readout

Our single pixel was considered independent of the telescope planes and read out by an additional analogue readout. Once the XTB01 data were analysed offline, they were merged to the telescope data offline, with a one directional synchronization algorithm using the timestamps.

The analogue output of the 50 µm × 50 µm single pixel was sent to a DRS4 board [110], which provides basically the same functionalities as a high speed oscilloscope. The DRS4 interface during data taking is illustrated in figure 7.4 where the coincidence between signal hit and telescope trigger indicates that a particle has crossed the telescope and the selected pixel of our device.

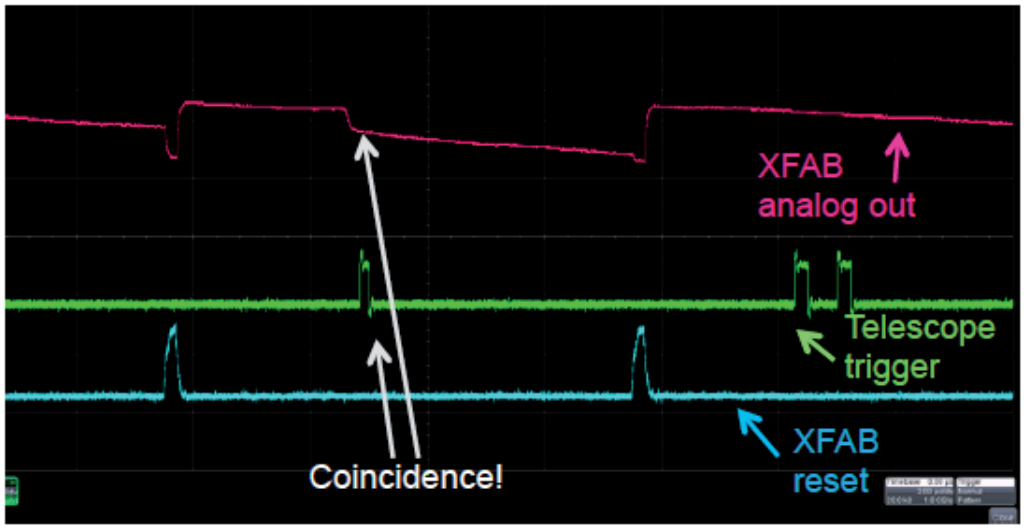
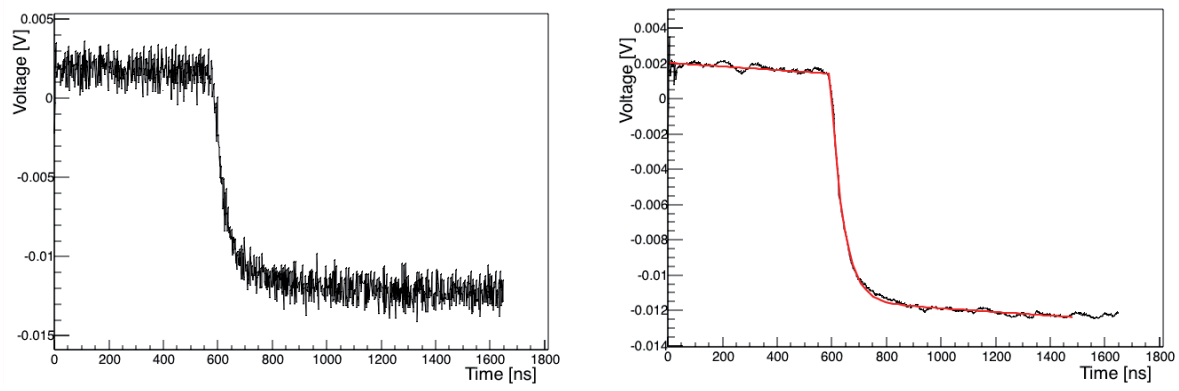


Figure 7.4: DRS4 interface during data taking. The analogue output of a 50 µm × 50 µm XTB01 pixel biased to 120 V is shown in pink and the telescope trigger in green. The coincidence of the telescope trigger and the edge in the XFAB analogue output indicates the passage of a particle.

Only the Hitbus chip corresponding to telescope arm 1 was operative, requiring a hit to be detected in all three planes. The reset periods, which clear the accumulated charge from the gate of the input transistor in the used 3T cell to avoid saturation, were vetoed because the DUT is insensitive in this time. As a consequence, only a particle detected in all three planes outside the reset periods generates a trigger to be sent to the DRS4. If the DRS4 is not busy, an acknowledge signal is sent back to the telescope and both, telescope and DRS4 record the event. The data saved by the DRS4 for each event are the output waveform, reset waveform, event number and timestamp.

The offline analysis developed for the hit recognition with sources, described in section 6.3.1 was adapted for the test beam case. It allows to distinguish the waveforms containing a DUT hit and the waveforms without a DUT hit. Additionally, the collected charge b, hit detection time t_0, and charge collection time c are extracted from equation 6.1. Figure 7.5b shows the analyser process on a 50 µm × 50 µm pixel at a bias voltage of 120 V with pion beam. Also here, the cases when no hit is detected are used to calculate the electronic noise. Thus, the analogue readout of the single pixel during test beam measurements is very similar to the one

used for radioactive source measurements.



(a) (b)

Figure 7.5: Developed readout algorithm implemented on test beam measurements. Offline waveform analysis on a 50 µm × 50 µm pixel at a bias voltage of 120 V (a) Signal Size [V] of the DUT hit before smoothing (b) hit fitted to the function described in equation 6.3 to extract the collected charge, hit detection time and charge collection time.

There are two essential differences. First, the test beam measurements were triggered directly on the particles seen by the telescope planes. That was not the case with the radioactive sources, where the XTB01 signal itself was used for triggering. Second, during the test beam measurements the oscilloscope was replaced by a DRS4 board [110], which is 1000 times faster storing the data. The offline analysis to distinguish the waveforms containing or no a hit was very similar, but made use of additional available information as the hit detection time.

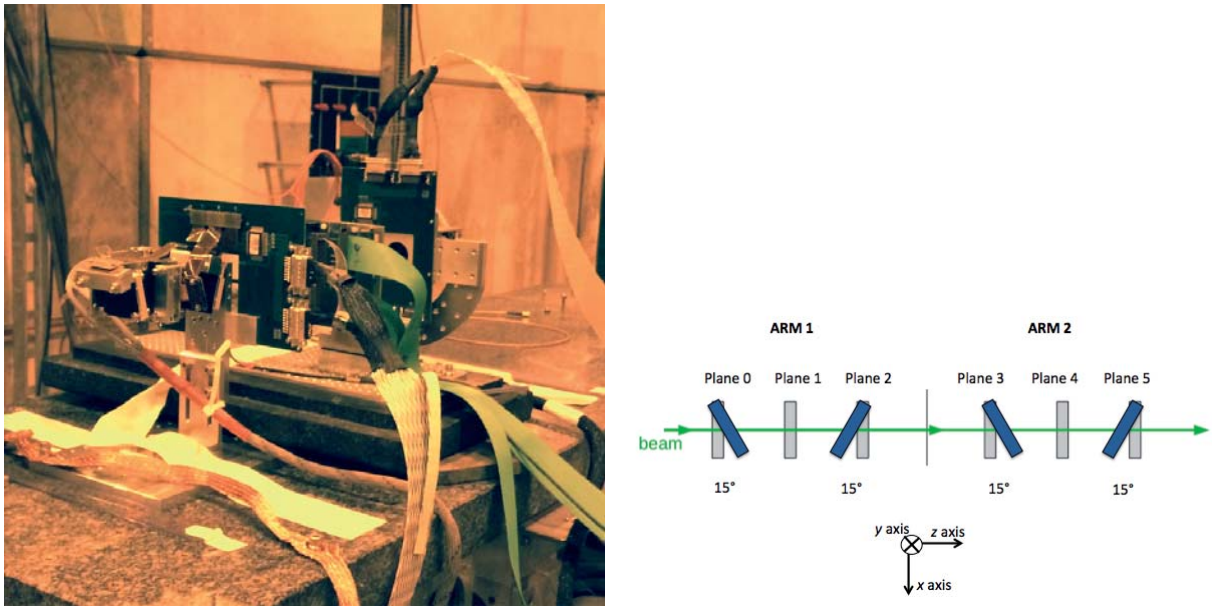
7.2 Test beam measurements and results

The unirradiated device was characterized for a bias voltage of 60 V, 90 V and 120 V. This section starts with a detailed description on finding the single pixel in the beam, and how the ROI was selected. Section 7.2.2 discusses the collected charge, the noise and the charge sharing measurements. The two possible selection criteria to analyse the data are described in section 7.2.3, and in section 7.2.4 and 7.2.5 the spatial resolution and the tracking efficiency are discussed.

7.2.1 Pixel search and Region-of-Interest definition

After the XTB01 is installed between the telescope arms, and the system is set up, the device is aligned to the beam. The procedure to align the selected testing pixel to the beam is performed a priori with a laser pointer. Figure 7.6a shows a photo of the telescope and XTB01 after installation and alignment. The configuration of the telescope planes during data taking is shown in figure 7.6b. The indicated planes were tilted by 15° in order to increase the

cluster size. However, the alignment of a single pixel of 50 µm × 50 µm within the beam spot



(a) (b)

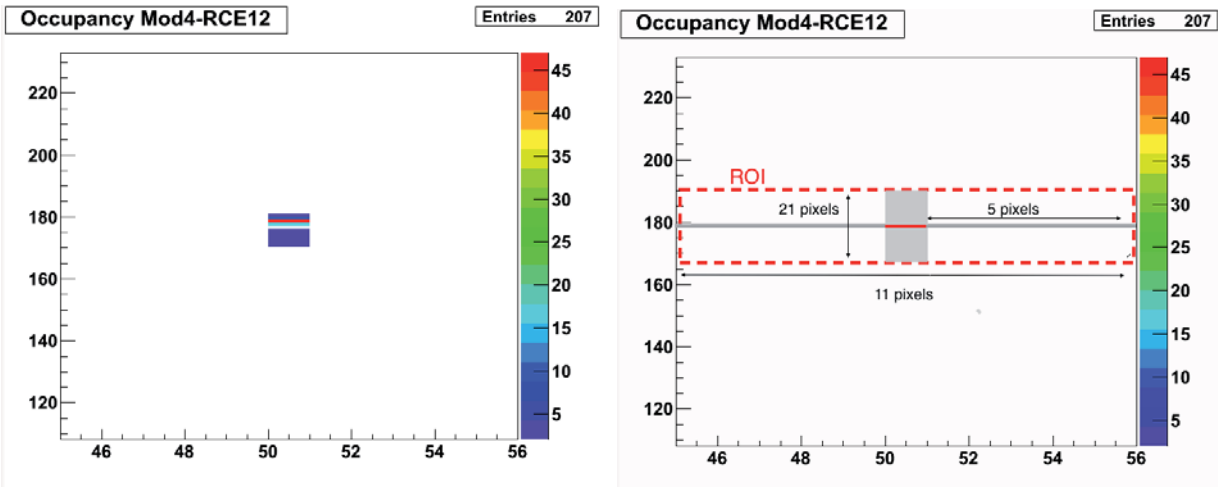
Figure 7.6: AIDA SBM FE-I4 testbeam setup a) after installation and alginment of the XTB01 prototype. b) Schematic top view of the telescope planes configuration. Arm 2 is additionally rotated by 90° around the z axis.

is quite arduous task. A first measurement triggering on the analogue signal of the single pixel while vetoing the resets periods is performed. Only when a MIP passes through the XTB01 pixel, the RCE stores the data of the telescope. This measurement takes about twenty minutes until one can unequivocally decide whether the pixel is within the beam spot or not. The online monitor of the telescope readout software when triggering in the single pixel biased to −60 V and the beam on is shown in figure 7.7a. It is seen that the pixel located in column 50 row 178 triggered 207 times. Thus it is mostly the selected pixel, and it is within the beam spot. In case, the telescope readout software does not show any hit pixel, a re-alignment of the sample with respect to the beam is needed.

Once the pixel is aligned to the beam spot, a track ROI needs to be defined with the aim to mask the telescope planes, and reduce the measurement window. The size of the ROI is totally arbitrary within the FE-I4 granularity. It can go from the actual size of the prototype to the full 2 cm × 2 cm FE-I4 size. The ROI in our measurements was decided to be the size of 11 × 250 µm FE-I4 pixels and 21 × 50 µm FE-I4 pixels as shown in figure 7.7b. This makes a total active surface of 1050 µm × 2750 µm and ensures that the pixel being readout is certainly inside of the ROI. The expected fraction of particles in the 50 µm × 50 µm pixel of the XTB01 is:

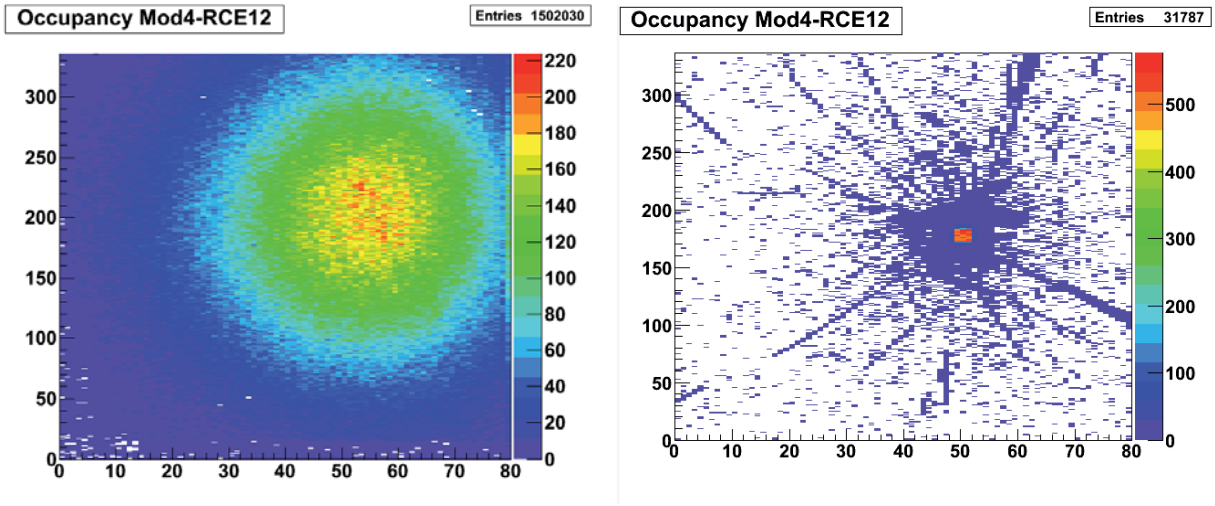
$$\frac{50\,\mu\text{m} \times 50\,\mu\text{m}}{1050\,\mu\text{m} \times 2750\,\mu\text{m}} = 0.000\,866 \tag{7.1}$$

which means that for every 10 000 particles passing through the ROI only 8 pass through the pixel being readout.



(a) (b)

Figure 7.7: (a) Online histogram when triggering in the single pixel. It is seen that the pixel located in column 50 row 178 triggered 207 times being mostly the pixel being readout. (b) Schema showing our ROI selection, which is composed of 11 × 250 µm FE-I4 pixels and 21 × 50 µm FE-I4 pixels.



(a) (b)

Figure 7.8: Online occupancy histograms for a run triggering on the three telescope planes (a) when no mask is applied on the telescope planes and without including the XTB01 as DUT. Thus, the beam profile is seen (b) when the mask is applied on the telescope planes and the XTB01 is included. This is the data taking mode, and the ROI is clearly observed.

The single pixel search and the ROI definition was performed for the three planes associated to the working Hitbus chip. Since the planes are rotated, this was done independently on each plane. The three telescope planes associated to the working Hitbus chip were masked to the defined ROI. Thus, only a particle passing by the track ROI in every plane would trigger the DRS4, increasing the chances that a trigger comes from a beam particle.

The last check before data taking consists on the performance of two runs. A first run triggering externally on the telescope planes without masking them nor including the XTB01 pixel in order to see the beam profile. This run is later used during the offline reconstruction for the telescope alignment. The online histogram of this run is shown in figure 7.8a. A second run triggering externally on the masked telescope planes and including the XTB01 pixel is performed. The online histogram of this run is shown in figure 7.8b. The comparison of both runs tells us about the relative position between the ROI and the beam, and ensures the proper operation of the ROI on the three planes. The comparison between figure 7.8a and 7.8b demonstrates the good alignment of the readout pixel within the beam spot, which is nearly at the center.

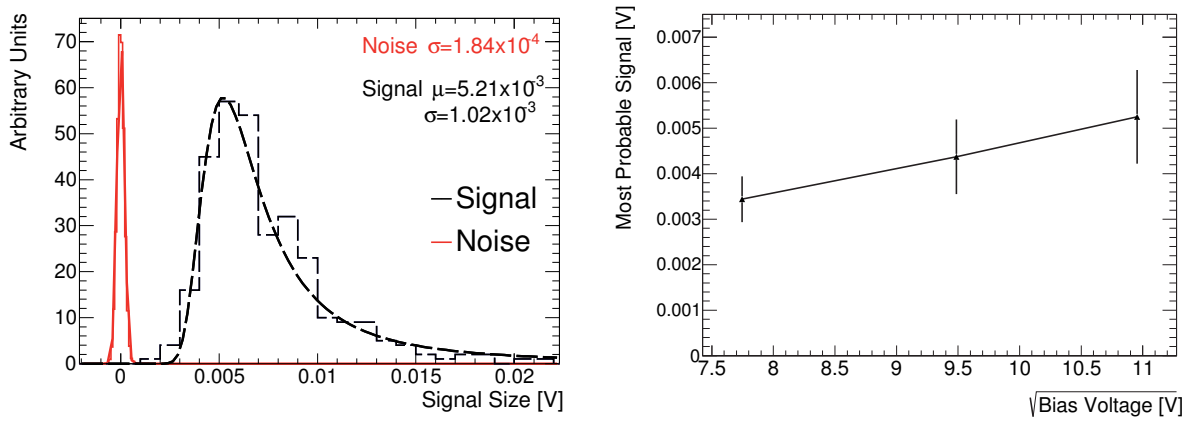
Once this is done, the trigger is set externally to the masked telescope planes, the XTB01 pixel is included and data taking starts.

7.2.2 Charge collection and charge sharing

The collected charge and the noise during the beam tests have been measured for the different voltages settings of the device. The signal and noise distribution for a single run with 150 000 events at a bias voltage of 120 V is shown in figure 7.9a. The Landau distributed signal is very well separated from the Gaussian noise, leading to a SNR of 22, which is comparable to the SNR of other HV/HR CMOS devices [91]. However, one needs to be aware that the noise is related with the electronics density and readout architecture, and the 3T-cell will not be the final pixel readout. Thus, SNR will be different in future prototypes. The signal size threshold used to define a DUT hit was 0.0012 V.

The MPV for the collected signal size as a function of the applied bias voltage is shown in figure 7.9b. The DRS4 functionality did not allow the sample calibration with an ^{55}Fe source. Thus all results regarding charge are given in signal size, and expressed in units of volts as shown in both figures. The signal size grows linearly with the square root of the bias voltage, in agreement with previous laboratory measurements shown in section 6.3.4 and with theoretical expectations.

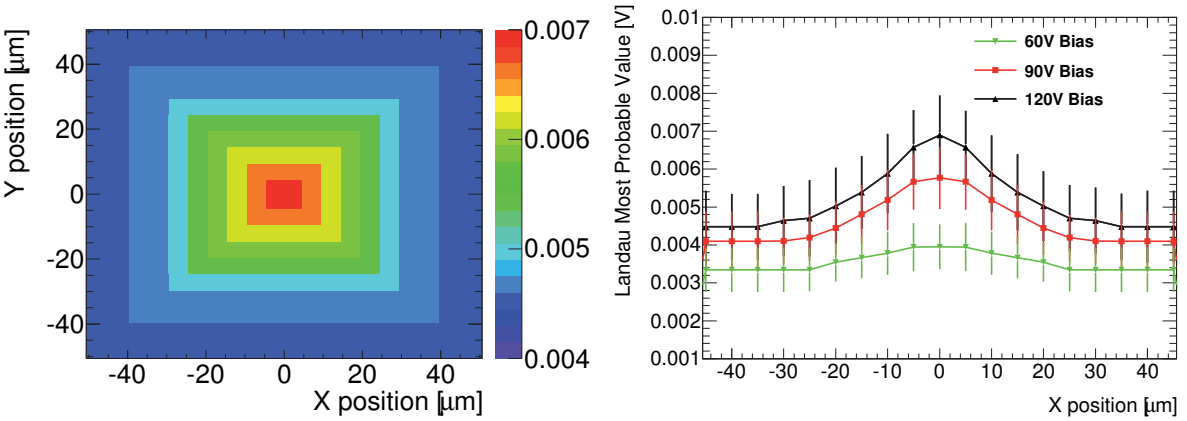
Charge sharing is another important feature of pixel detectors as it is directly related to tracking resolution and radiation hardness. The generated electron cloud of a track going through the sensor increases its volume due to diffusion while drifting to the collecting electrode in the electrical field. As a consequence, the electron cloud can be collected by two or more pixel cells, leading to the charge sharing effect. On the one hand, high charge sharing results in better



(a) (b)

Figure 7.9: (a) Signal over noise at an applied bias voltage of 120 V taken on a single run. The SNR is 22 for the threshold of 0.0012 V used during the measurement. (b) Most Probable Signal as a function of the different bias voltages applied during the test beam measurements with the width of the distributions shown in the vertical bars.

tracking resolution as the track position can be interpolated between the pixels using charge weighting if the signal size information is available per pixel. On the other hand, less signal will be available to each pixel cell, which may become a problem especially for irradiated devices where the signal decreases due to trapping effects.



(a) (b)

Figure 7.10: The (a) 2D map showing the MPV signal size as a function of the *xy* position within the pixel for an applied bias voltage of 120 V. The (b) MPV as a function of the *x* position within the pixel for 60 V, 90 V and 120 V.

The charge sharing effect is observed in the XTB01 prototype as shown in figure 7.10. Figure 7.10a shows a 2D map of the MPV signal of the DUT at different positions within the pixel

with a bias voltage of 120 V. Assuming that the XTB01 pixel is symmetric in square frames, the collected charge is histogrammed in square frames to increase the statistics and thus reduce the statistical variations. The inner part of the pixel ($-20\,\mu m \leq xy \leq 20\,\mu m$) collects signals above 0.006 V, whereas the outer part of the pixel collects signals below 0.005 V due to the charge sharing effect. Figure 7.10b shows the MPV as a function of the x position for all bias voltages, where the same conclusion is underlined for all the applied voltages. However, the telescope resolution of 8 μm has a significant impact on this distribution.

7.2.3 Selection criteria

Two different selection criteria were investigated to obtain the hit track residuals. These are the charge collection time (CCT) over the collected charge, so-called slew rate criteria, and the hit detection time (t_0). These parameters are obtained during the reconstruction and provide two possible selection criteria to improve the purity of real DUT hits.

The slew rate criteria selects the charge collection time over collected charge in order to extract the charges collected by drift and not those collected by diffusion. The used slew rate criteria corresponds to:

$$\text{CCT} < 100\,\text{ns} + \frac{50\,\text{ns}}{0.01} \times \text{Signal size} \tag{7.2}$$

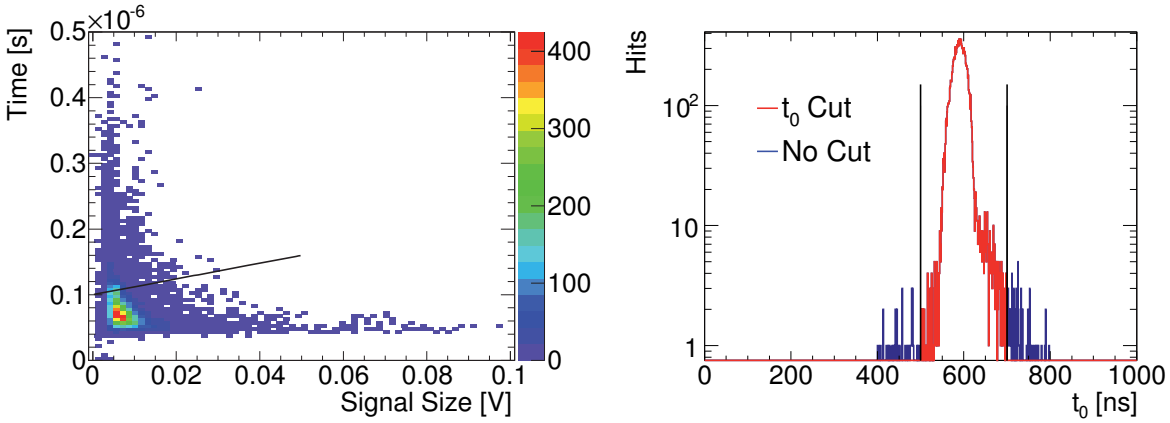
The t_0 selection criteria consists of excluding from the analysis the hits collected outside the 500-700 ns interval as depicted in figure 7.11b. As the trigger is applied externally, t_0 should be constant at around a certain value, which was set to 600 ns. A margin of 100 ns was allowed to cope with delays. Both selection criteria were applied to all bias voltages.

The CCT distribution versus the collected charge for all collected hits on a run at 120 V is shown in figure 7.11a. The slew rate criteria is depicted here, where only the hits below the black line are selected for the analysis. This selection was also applied for the analysis of the radioactive source measurements described in section 6.3.2. Figure 7.11b shows the t_0 distribution for all collected hits on a run at 120 V and the t_0 selection criteria.

A 2D projection of the collected charge in a run where the applied bias was 120 V is shown in figure 7.12a for the cut on the slew rate and in figure 7.12b for the cut on t_0. Both selections produce the same effect on the collected charge, as shown in figure 7.12. This implies that the hits collected slower due to the diffusion component, are related with a delay in the hit detection time. Therefore, all results shown later in this chapter include the t_0 selection criteria on the DUT hits.

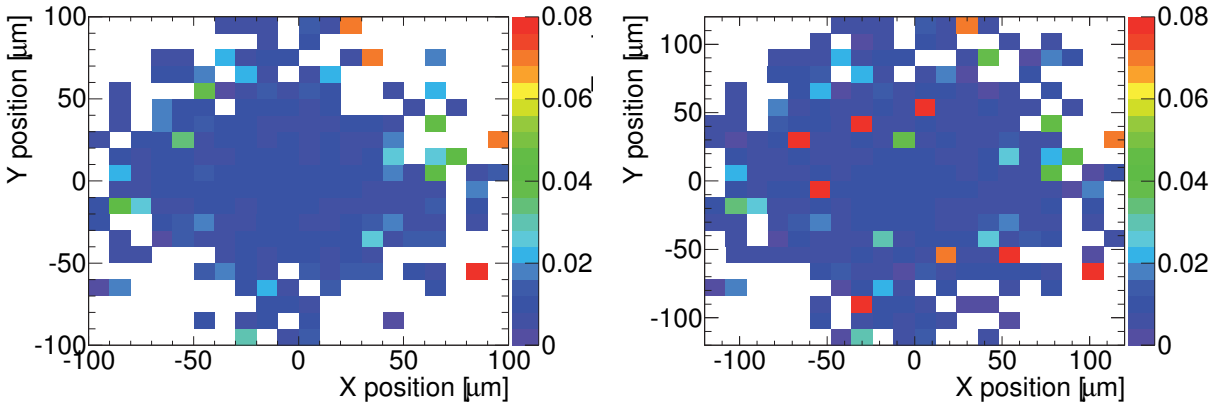
7.2.4 Spatial resolution

The spatial resolution is a fundamental feature of pixel detectors, which is determined by the pixel pitch. However, the choice of the readout mode, the reconstruction algorithm, and



(a) (b)

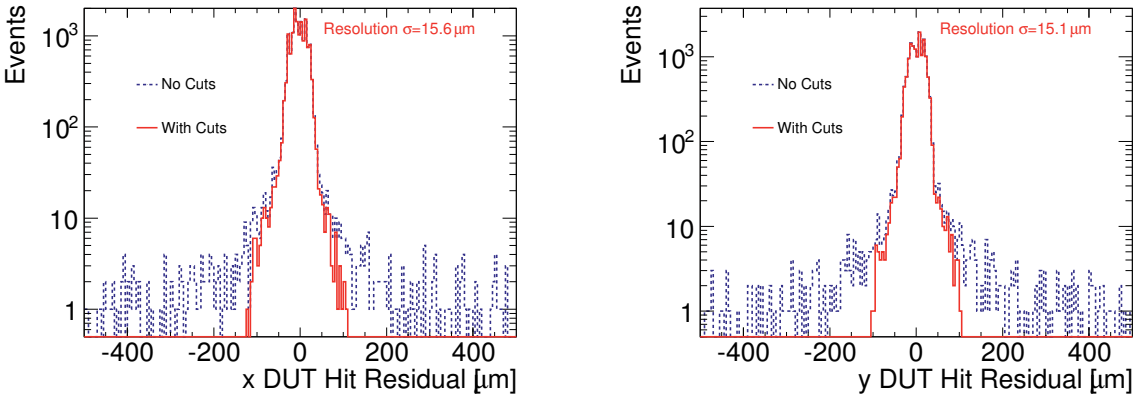
Figure 7.11: Selection cuts on a run at 120 V (a) Selection on the slew rate, which only considers hits collected fast for the analysis (b) Selection on the t_0, which only considers hits detected within 500-700 ns interval.



(a) (b)

Figure 7.12: 2D projection map of the collected charge in a run where the applied bias was 120 V (a) Selection on the slew rate, which only considers hits collected fast for the analysis (b) Selection on the t_0, which only considers hits detected within 500-700 ns interval.

the amount of charge sharing also play a role [78]. For a single pixel with full efficiency the spatial resolution is expected to be equal to the pixel pitch divided by the square root of twelve. The spatial resolution in a test beam is obtained through the hit track residuals. The track residuals at a bias voltage of 120 V in the x and y planes with and without applying the t_0 cut are shown in figure 7.13. It is observed that the t_0 cut removes almost all hits with a residual larger than 100 µm. The spatial resolution after the cut is around 17 µm in comparison with the 14.4 µm expected using the pixel pitch calculation. The measured value is limited by the telescope resolution (~ 8 µm), which adds in quadrature with the pixel resolution. Taking that into account, the measured spatial pixel resolution is around 15 µm. This is compatible with the required 15 µm pixel resolution in ATLAS as described in section 2.3.3. Additionally, in a simultaneous readout of all pixels the charge sharing effect can be used to increase the spatial resolution using the weighted charge sum [78].



(a) (b)

Figure 7.13: Track Residual for a bias voltage of 120 V with and without applying the T_0 cut (a) in the x direction (b) in the y direction

7.2.5 Tracking efficiency

The hit detection efficiency is another fundamental characteristic of pixel detectors. As described in section 2.3.3, the 97% efficiency in the active area was required for IBL [39]. The tracking efficiency is computed as the ratio of the reconstructed telescope tracks extrapolated to within the DUT pixel pitch and the DUT hits.

The computed efficiency of the tested XTB01 with the t_0 selection criteria applied at a bias voltage of 60 V, 90 V and 120 V is shown respectively in figure 7.14a, 7.14b, and 7.14c. The hit efficiency is again calculated in square frames to reduce the statistical variations. It is observed that the inner and outer pixel efficiencies grow with the bias voltage, approximating the pixel size for the highest voltage.

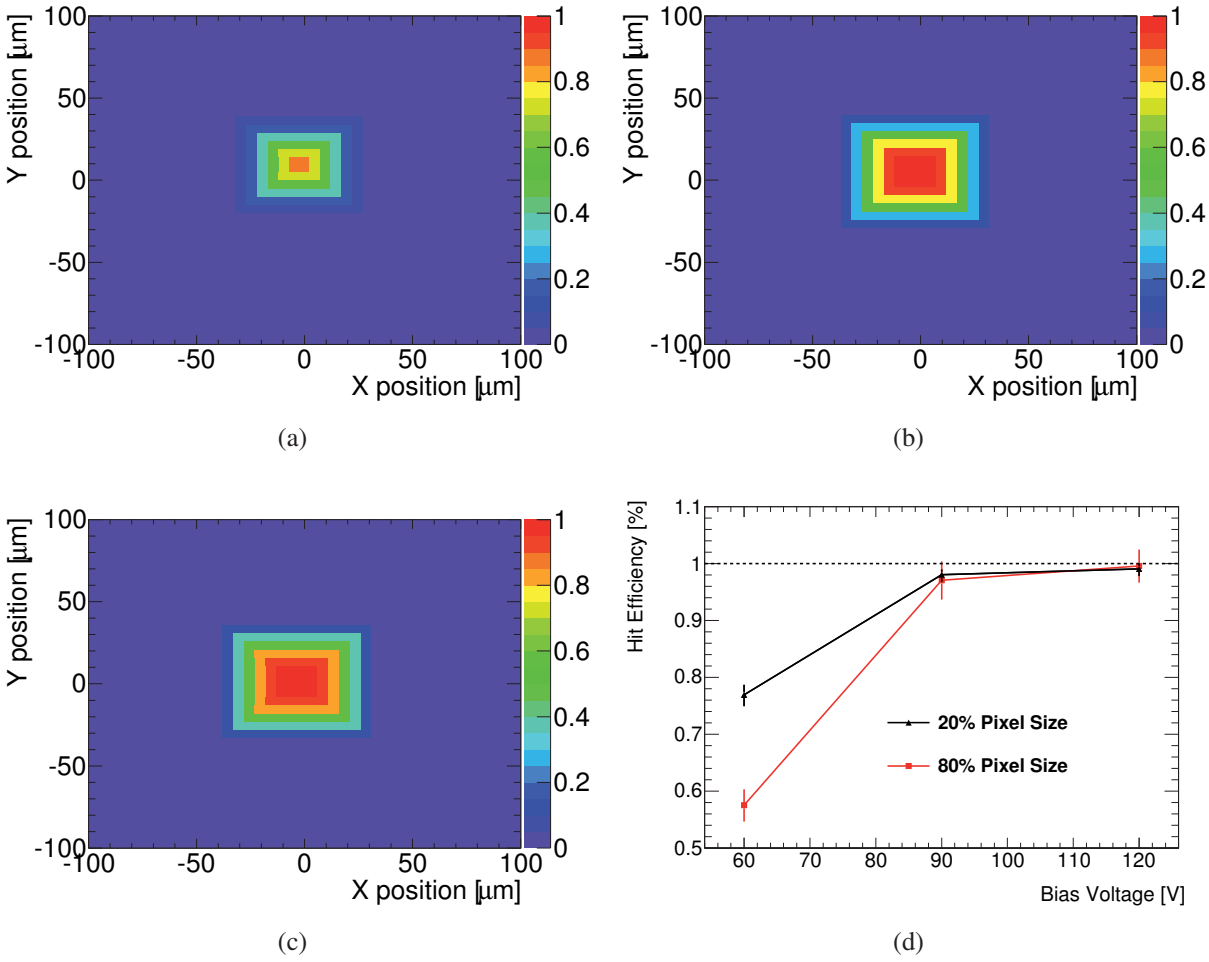


Figure 7.14: Tracking efficiency in a 50 µm × 50 µm pixel with no cuts on the DUT hits. The DUT efficiency is computed in rings to increase the statistics for bias voltages of (a) 60 V (b) 90 V and (c) 120 V. The DUT hit efficiency (d) is shown as a function of the bias voltage for different pixel regions with the t_0 cut applied.

A simulation was used to compute corrections to the efficiency coming from the finite position resolution of the telescope tracks. A 50 µm × 50 µm box with 100% efficiency was simulated. Subsequently, a 8 µm wide Gaussian, which corresponds to the telescope resolution, was convoluted with the edges of the box to represent the expected smearing of the telescope resolution. A correction factor is extracted as a result on the efficiency change of the 100% box due to the telescope resolution. The systematic uncertainties on these corrections are computed by varying the telescope resolution up and down by 1 µm. Figure 7.15 shows the simulated efficiency of the Gaussian smeared box and table 7.1 list the corrections obtained. The correction factor was applied to all further results presented in this thesis.

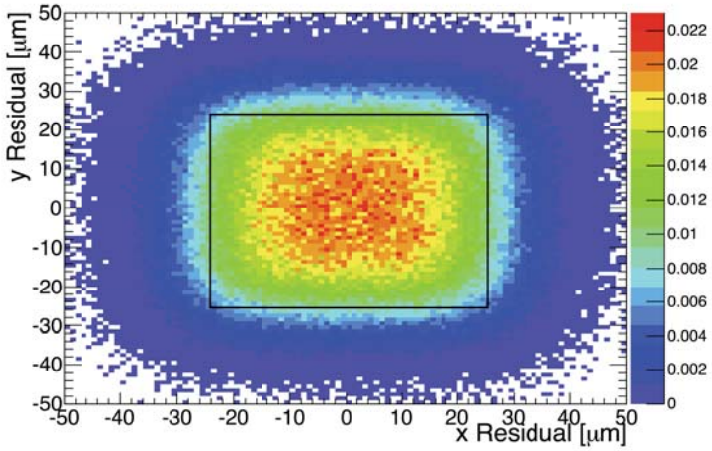


Figure 7.15: Simulation of a 50 µm × 50 µm pixel 100% efficient smeared by a 8 µm wide Gaussian, which corresponds to the telescope resolution.

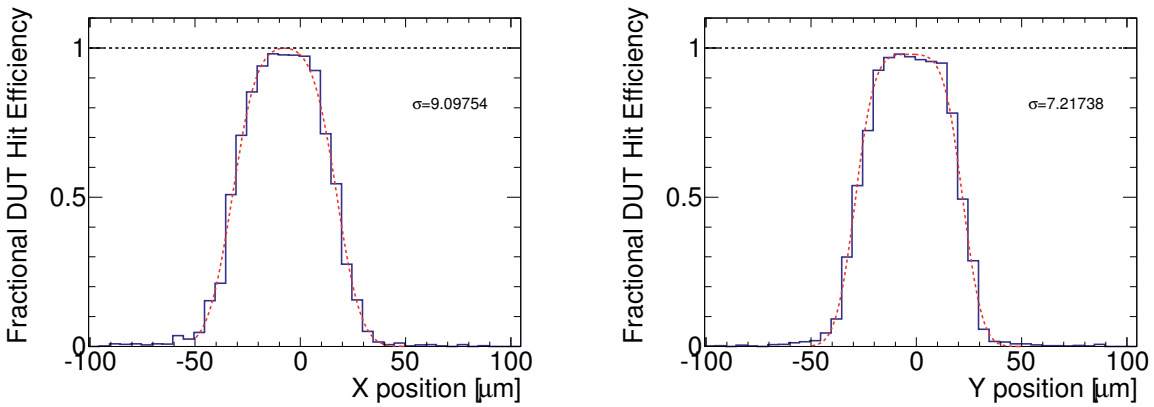
Pixel Area	Truth Efficiency	Correction
80%	0.8675	1.150 ± 0.024
20%	0.8675	1.012 ± 0.006

Table 7.1: List of the correction and uncertainty values obtained from the simulation of a 100% efficient pixel convoluted with the telescope resolution.

The track efficiency as a function of the bias voltage has been computed for the central 20% and central 80% of the pixel with the t_0 cut applied in figure 7.14d. The tracking efficiency at the central 80% of the pixel is $99.6^{\pm 0.6}_{\pm 1.1}$%(tot) at a bias voltage of 120 V. The efficiency results were calculated together with its total error calculated as the quadratic sum of systematic and statistical error. The statistical error is negligible in comparison with the alignment uncertainty computed in the systematic error.

To investigate the tracking efficiency as a function of the direction, the tracking efficiency was projected for the x and y directions with the t_0 cut applied and for a bias voltage of 120 V

as shown in figure 7.16. Figure 7.16a shows the track efficiency projected in the x direction for $-10\,\mu\text{m} \leq y \leq 10\,\mu\text{m}$, whereas figure 7.16b shows the projection in the y direction for $-10\,\mu\text{m} \leq x \leq 10\,\mu\text{m}$. The width of the efficiency plateau corresponds to $\sim 14\,\mu\text{m}$ and $\sim 20\,\mu\text{m}$ in the x and y direction, respectively. The given absolute numbers are not so important but rather the difference between the x and y directions. This fits with the fact that the n-well electrode is not square, and one would expect a higher efficiency in the longer n-well size direction as observed here.



(a) (b)

Figure 7.16: Projected efficiency at a bias voltage of 120 V with cut t_0 applied (a) in the x direction (b) in the y direction. The fitted Gaussian resolution (σ) of the telescope is shown for both the x and y directions.

In conclusion, the presented test beam results confirm the excellent charge collection properties observed with radioactive sources and eTCT. At the edge of the pixel, about 30% of the deposited charge is shared with the neighbouring pixels. The measured spatial resolution is about 15 µm which is in rough agreement with the 14 µm one would expect from the pixel pitch formula. This is compatible with the measured pixel resolution in IBL modules [33]. The device is $99.6^{\pm 0.6}_{\pm 1.1}$%(tot) efficient at the central 80% of the pixel before irradiation. That is compatible with well stablished hybrid module concepts [33]. The next step in the coming months is the performance of test beam campaigns on irradiated devices to evaluate its performances at the ATLAS expected fluence.

Chapter 8

Summary and Outlook

A large variety of fundamental physics questions will be addressed by the experiments of the HL-LHC. The high precision measurements needed to seek for answers to these questions result in challenging instrumentational requirements, especially for the inner tracking systems of the experiments. These requirements set stringent demands to the sensors used for particle detection. Thus, the development of novel radiation hard silicon sensors is required. Currently, passive silicon pixel sensors are most commonly used. So far they are unrivalled to cope such hard conditions. These silicon pixel sensors are bump bonded to a dedicated and highly complex readout chip. Besides several strong benefits of one silicon tile dedicated to the particle detection and one to the readout electronics, the needed bump bonding process and the needed high resistivity sensor material impact the possible segmentation, the material budget, and the cost.

Commercial high-voltage and/or high-resistivity CMOS technologies are being investigated within the ATLAS CMOS collaboration as an alternative to the currently used hybrid pixel detectors. These technologies provide the possibility to implement a sensor collecting the charge by drift in a depleted region, and allows logic implementation in the same silicon tile. That enables the use of capacitive coupled connections between sensor and front-end electronics, replacing the current bump-bonding process. Three main benefits could result from that: less cost, less material budget, and smaller pixel size fabrication, which improves the spatial resolution of the detector layers. Additionally, the CMOS-based sensors are an industrial process, promising a higher production yield and cheaper sensors. It is possible to produce the sensors in small thickness (50-80 µm) since they do not need to be handled and heated for the connection with the front-end electronics. The use of fully monolithic detectors in HEP experiments currently leads to a new era of tracking detectors.

A novel depleted Monolithic Active Pixel Sensor built on thick film SOI 180 nm technology was evaluated in this thesis for its use in the future ATLAS tracking detector. A layer of silicon dioxide (BOX) isolates the full CMOS electronics technology from the substrate, which is reversely biased and used as a sensor diode. This allows the fabrication of the electronics in standard low resistivity, and the sensor diode in high resistivity, if needed. The SOI 180 nm technology provides a double well structure to shield the thin gate oxide transistors from the BOX, and the transistor's bulk silicon is partially depleted. This makes the technology promising against the radiation effects on the transistors and against the Back Gate Effect observed

in other SOI technologies. The process makes it possible to apply high bias voltages up to 300 V, which are used to partially deplete the substrate. It is possible to fabricate devices with higher resistivity material (1 k$\Omega\cdot$ cm) in the sensor diode. Therefore, a fully depleted substrate could be achieved after thinning the sensor.

The work presented in this thesis has proven the radiation hardness of the SOI transistors on this technology up to 700 Mrad. This enables the technology for being used at the outer pixel layers, and an additional measurement up to 1 Grad would prove its possible use in the innermost pixel layers. The transistors electrical parameter shift is within the process variations up to 700 Mrad. All results are consistent with non SOI thin gate technologies like the IBM 130 nm used for ATLAS IBL FE-I4. In contrast to other SOI technologies, no effect of the BOX is observed. Additionally, the overlapping transfer characteristics of the transistors for an irradiated chip in two configurations - without HV on the diode and with -40 V on the diode - prove that there is no coupling between the electronics and the electric field in the sensor.

The unexpected high leakage current before irradiation observed in the first version of the chip (XTB01) was corrected in the second prototype (XTB02) by slight changes in the production process. As a consequence, XTB02 presents a factor of ten less leakage current and an increase of the breakdown voltage to above 300 V.

In the framework of this thesis the charge collection properties of the sensor diode were extensively characterized with different experimental techniques. Beta and gamma radioactive sources, laser pulses, and high energetic beam test were used.
Gamma sources were used to calibrate the prototype whereas beta sources and MIPs were used to evaluate the tracking performance of the sensor. The new readout algorithm developed for these measurements provides significantly more valuable observables than the previously used correlated double sampling and therefore allowed the analysis of the collected charge as a function of the charge collection time. These measurements on unirradiated and irradiated samples at different bias voltages allowed the observation of drift and diffusion contribution in the collected charge of the prototype. This technique confirmed the partial depletion of the prototype. In the following, a selection criteria was applied to allow considering only the charge collected by drift. Clear ^{55}Fe and ^{90}Sr spectrum for unirradiated and irradiated devices up to 5×10^{13} $n_{eq}cm^{-2}$ have been shown and discussed in chapter 6 demonstrating the MIP detection of the prototype. Source scans, and depletion depth calculations were performed.
A depletion depth of about 34 μm was achieved at a bias voltage of 120 V, confirming its expected growth in depth. The depletion depth was confirmed with radioactive source measurements in the laboratory (chapter 6), with high energy pions on the beam (chapter 7), and with edge TCT measurements (chapter 6).
The radioactive source measurements also show hints towards the Acceptor Removal effect for the first time observed in this resistivity. The irradiated sample up to 5×10^{13} $n_{eq}cm^{-2}$ was oberved to collect more charge than the irradiated one to 1×10^{13} $n_{eq}cm^{-2}$. This result lead to the further investigation in Ljubljana and strong evidences have already been seen as it is discussed in chapter 6.

In this thesis, for the first time the new readout algorithm was implemented in a test beam measurements. The first test beam results of pixel sensors in XFAB SOI technology on unirradiated devices have brought out interesting results. Regarding the collected charge, the measured SNR=22 is comparable to other HV/HR-CMOS devices, and the signal size grows linearly as a function of the square root of the voltage, as expected. At the edge of the pixel, about 30% of the deposited charge is shared with the neighbouring pixels. The measured spatial resolution is about 15 µm and in comparison with the 14 µm one would expect from the pixel pitch formula. The computed efficiency at the central 80% of the pixel is 99.6% at a bias voltage of 120 V. This is competitive with well established hybrid technologies.

In the coming months, test beam campaigns with irradiated devices are foreseen. That would permit to evaluate the pixel spatial resolution and pixel efficiency after irradiation. The performance of eTCT measurements at different fluences up to 5×10^{15} $n_{eq}cm^{-2}$ is currently taking place. Those measurements will allow the extraction of the depletion depth at different fluences, and to confirm or discard the presence of the Acceptor Removal effect on 100 Ω cm silicon. In case the Acceptor Removal effect is confirmed in this prototype high resistivity would not be needed to increase the collected charge, at least for applications up to 2-5 $\times 10^{15}$ $n_{eq}cm^{-2}$.

The work performed in this thesis has boosted the interest in this technology and it was chosen to be one of the three most promising technologies for the ATLAS CMOS Demonstrator Programme. During this year a submission of a 2 cm × 2 cm large sensor is planned. A new readout architecture will be incorporated substituting the slow 3T-cell circuit. This submission targets to demonstrate the feasibility and performance of a ATLAS pixel module in SOI technology.

Additionally, this prototype has shown many benefits and possible applications beyond the ATLAS upgrade for HL-LHC. Its promising results make it attractive for its use in future linear colliders as International Linear Collider (ILC), or Compact Linear Collider (CLIC), and future circular colliders as the foreseen Future Circular Collider (FCC), whose requirements drive towards the usage of CMOS processes. For those experiments the position resolution and low mass are the major challenges together with the radiation hardness, whereas speed requirements are not so critical. Table 8.1 summarizes the requirements for the different, existing and planned, colliders.
Additionally, this prototype could be highly interesting for X-ray detection applications, where currently hybrid detectors are used. Monolithic sensors are in full swing due to their potential in terms of resolution and price.

	Luminosity cm^2s^{-1}	BX time ns	Particle rate kHz/ mm^2	NIEL $n_{eq}cm^{-2}$/lifetime	TID Mrad/lifetime
LHC	1×10^{34}	25	1000	2×10^{15}	79
HL-LHC	1×10^{35}	25	10 000	2×10^{15}	> 500
LHC Heavy Ions	6×10^{27}	20 000	10	$> 10^{13}$	> 0.7
Relativistic Heavy Ion Collider (RHIC)	8×10^{27}	110	3.8	few 10^{12}	> 0.2
SuperKEKB	1×10^{35}	2	400	3×10^{12}	> 10
ILC	1×10^{34}	250	350	10^{12}	> 0.4
FCC	5-30 $\times 10^{35}$	-	-	$> 10^{16}$	> Grad range

Table 8.1: Detectors requirement comparison of pixel detectors located the closest to the interaction point for some particle colliders [82]. The assumed lifetimes are 7,10, and 5 years for LHC, HL-LHC and ILC.

Bibliography

[1] C. P. Burgess and G. D. Moore. *The standard model: A primer*. Vol. ISBN-9780521860369. Cambridge University Press, 2006.

[2] D. Schaefer. "Evidence for the Higgs boson in the H to WW to nu nu decay channel". PhD thesis. University of Pennsylvania, 2014.

[3] The UA1 Collaboration. "Experimental observation of isolated large transverse energy electrons with associated missing energy at s=540 GeV". In: *Physics Letters B* 122.1 (1983), pp. 103 –116. ISSN: 0370-2693. DOI: http://dx.doi.org/10.1016/0370-2693(83)91177-2.

[4] The UA2 Collaboration. "Observation of single isolated electrons of high transverse momentum in events with missing transverse energy at the CERN pp collider". In: *Physics Letters B* 122.5–6 (1983), pp. 476 –485. ISSN: 0370-2693. DOI: http://dx.doi.org/10.1016/0370-2693(83)91605-2.

[5] The UA1 Collaboration. "Experimental observation of lepton pairs of invariant mass around 95 GeV/c2 at the CERN SPS collider". In: *Physics Letters B* 126.5 (1983), pp. 398 –410. ISSN: 0370-2693. DOI: http://dx.doi.org/10.1016/0370-2693(83)90188-0.

[6] The UA2 Collaboration. "Evidence for Z0→e+e at the CERN pp collider". In: *Physics Letters B* 129.1 (1983), pp. 130 –140. ISSN: 0370-2693. DOI: http://dx.doi.org/10.1016/0370-2693(83)90744-X.

[7] F. Englert and R. Brout. "Broken Symmetry and the Mass of Gauge Vector Mesons". In: *Phys. Rev. Lett.* 13 (9 1964), pp. 321–323. DOI: 10.1103/PhysRevLett.13.321. URL: http://link.aps.org/doi/10.1103/PhysRevLett.13.321.

[8] Peter W. Higgs. "Broken Symmetries and the Masses of Gauge Bosons". In: *Phys. Rev. Lett.* 13 (16 1964), pp. 508–509. DOI: 10.1103/PhysRevLett.13.508. URL: http://link.aps.org/doi/10.1103/PhysRevLett.13.508.

[9] G. S. Guralnik, C. R. Hagen and T. W. B. Kibble. "Global Conservation Laws and Massless Particles". In: *Phys. Rev. Lett.* 13 (20 1964), pp. 585–587. DOI: 10.1103/PhysRevLett.13.585.

[10] Peter W. Higgs. "Spontaneous Symmetry Breakdown without Massless Bosons". In: *Phys. Rev.* 145 (4 1966), pp. 1156–1163. DOI: 10.1103/PhysRev.145.1156.

[11] T. W. B. Kibble. "Symmetry Breaking in Non-Abelian Gauge Theories". In: *Phys. Rev.* 155 (5 1967), pp. 1554–1561. DOI: 10.1103/PhysRev.155.1554.

[12] ATLAS Collaboration. "Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 1 –29. ISSN: 0370-2693. DOI: 10.1016/j.physletb.2012.08.020.

[13] CMS Collaboration. "Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC". In: *Physics Letters B* (2012).

[14] Oliver Sim Bruning et al. *LHC Design Report*. CERN, 2004.

[15] Peter Braun-Munzinger and Johanna Stachel. "The quest for the quark gluon plasma". In: *Nature* 448.7151 (2007), pp. 302–309.

[16] H Muller-Kirsten and Alfred Wiedemann. *Supersymmetry-an introduction with conceptual and calculational details*. World Scientific Pub. Co., Teaneck, NJ, 1987.

[17] ATLAS Collaboration. *ATLAS Experiment - Public Results*. Website. https://twiki.cern.ch/twiki/bin/view/AtlasPublic. 2013.

[18] *The ATLAS Collaboration*. https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/CombinedSummaryPlots/SM/.

[19] Rolf-Dieter Heuer and Herwig Schopper. *LEP-the lord of the collider rings at CERN 1980-2000. The making, operation and legacy of the World's largest scientific instrument*. Springer Science & Business Media, 2009.

[20] Lyndon Evans and Philip Bryant. "LHC Machine". In: *Journal of Instrumentation* 3.08 (2008), S08001.

[21] L. Rossi and 0. Brüning. *High Luminosity Large Hadron Collider A description for the European Strategy Preparatory Group*. Tech. rep. CERN LHC, 2012.

[22] F. Riggi. P. La Rocca. "The upgrade programme of the major experiments at the Large Hadron Collider". In: *Journal of Physics: Conference Series* 515 (2014), pp. 13–18.

[23] ATLAS collaboration et al. *ATLAS Phase-II Upgrade Scoping Document*. Tech. rep. CERN-LHCC-2015-020, 2015.

[24] M Lamont. "LHC, HL-LHC and beyond". In: *Proceedings of The European Physical Society Conference on High Energy Physics (EPS-HEP 2013). 18-24 July, 2013. Stockholm, Sweden*. Vol. 1. 2013, p. 149.

[25] ATLAS Collaboration. *ATLAS detector and physics performance: Technical Design Report, Volume II*. Technical Design Report ATLAS. Electronic version not available. Geneva: CERN, 1999.

[26] G Sciolla. "LHC, HL-LHC and beyond". In: *PACIFIC Conference on High Energy Physics*. 2014.

[27] Yosef Nir and Helen R Quinn. "CP violation in B physics". In: *Annual Review of Nuclear and Particle Science* 42.1 (1992), pp. 211–250.

[28] Particle Data Group Collaboration. "Review of Particle Physics". In: *Phys. Rev. D* 86 (1 2012), p. 010001. DOI: 10.1103/PhysRevD.86.010001. URL: http://link.aps.org/doi/10.1103/PhysRevD.86.010001.

[29] ATLAS Collaboration. *ATLAS detector and physics performance: Technical Design Report, Volume I*. Technical Design Report ATLAS. Electronic version not available. Geneva: CERN, 1999.

[30] ATLAS Collaboration. *ATLAS high-level trigger, data-acquisition and controls: Technical Design Report*. Technical Design Report ATLAS. CERN, 2003.

[31] ATLAS Collaboration. *Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment*. Tech. rep. CERN-LHCC-2012-022. LHCC-I-023. CERN, 2012.

[32] The ATLAS Collaboration. "The ATLAS Experiment at the CERN Large Hadron Collider". In: *Journal of Instrumentation* 3.08 (2008), S08003.

[33] The ALTAS IBL Collaboration. "Production and Integration of the ATLAS Insertable B-Layer". In: *to be submmited in JINST*. 2016.

[34] G Aad et al. "ATLAS pixel detector electronics and sensors". In: *Journal of Instrumentation* 3.07 (2008), P07007.

[35] Malte Backhaus. *The upgraded Pixel Detector of the ATLAS Experiment for Run2 at the Large Hadron Collider*. Tech. rep. ATL-COM-INDET-2015-089, 2015.

[36] *The ATLAS Collaboration*. `https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/IDTR-2015-007/`.

[37] *The ATLAS Collaboration*. `https://twiki.cern.ch/twiki/bin/view/AtlasPublic/LuminosityPublicResults`.

[38] ATLAS Collaboration. *Letter of Intent for the Phase-I Upgrade of the ATLAS Experiment*. Tech. rep. CERN-LHCC-2011-012. LHCC-I-020. CERN, 2011.

[39] The ATLAS Collaboration. *ATLAS Insertable B-Layer Technical Design Report*. Tech. rep. CERN-LHCC-2010-013. ATLAS-TDR-19. CERN, 2010.

[40] M. Mikuz H. Kagan and W. Trischuk. *ATLAS Diamond Beam Monitor (DBM)*. Tech. rep. ATL-IP-ES-0187, `https://edms.cern.ch/document/1211792/1`. Geneva: CERN.

[41] L Adamczyk et al. *Technical Design Report for the ATLAS Forward Proton Detector*. Tech. rep. CERN-LHCC-2015-009. ATLAS-TDR-024. Geneva: CERN, 2015.

[42] et al. C. Da Via. "3D silicon sensors: Design, large area production and quality assurance for the ATLAS IBL pixel detector upgrade". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 694 (2012), pp. 321–330.

[43] Norbert Wermes. "Pixel detectors for charged particles". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 604.1 (2009), pp. 370–379.

[44] W.R. Leo. *Techniques for Nuclear and Particle Physics Experiments: A How-to Approach*. 978-3540572800: Springer, 1994.

[45] Malte Backhaus. "High bandwidth pixel detector modules for the ATLAS Insertable B-Layer". PhD thesis. Bonn U., 2014.

[46] *Amptek*. Website. http://www.amptek.com/wp-content/uploads/2013/12/cdte_3.png. 2013.

[47] H. Spieler. *Semiconductor Detector Systems*. 978-0198527848: Oxford science publications, 2014.

[48] Charles Kittel. *Introduction to solid state physics*. Wiley, 2005.

[49] *pn-junction*. Website. http://www.powerguru.org/p-n-junction/.

[50] Gregor Kramberger. "Signal development in irradiated silicon detectors". PhD thesis. Doktorska disertacija, Ljubljana, 2001.

[51] ATLAS IBL collaboration et al. "Prototype ATLAS IBL modules using the FE-I4A front-end readout chip". In: *Journal of Instrumentation* 7.11 (2012), P11010.

[52] Tso-Ping Ma and Paul V Dressendorfer. *Ionizing radiation effects in MOS devices and circuits*. John Wiley & Sons, 1989.

[53] Simon M Sze and Kwok K Ng. *Physics of semiconductor devices*. John Wiley & Sons, 2006.

[54] F Ragusa and L Rolandi. "Tracking at LHC". In: *New Journal of Physics* 9.9 (2007), p. 336.

[55] Walter Blum, Werner Riegler and Luigi Rolandi. *Particle detection with drift chambers*. Springer Science & Business Media, 2008.

[56] Joseph M Benedetto and HE Boesch. "The relationship between 60co and 10-kev x-ray damage in mos devices". In: *Nuclear Science, IEEE Transactions on* 33.6 (1986), pp. 1317–1323.

[57] RC Hughes. "Charge-Carrier Transport Phenomena in Amorphous SiO2: Direct Measurement of the Drift Mobility and Lifetime". In: *Physical Review Letters* 30.26 (1973), p. 1333.

[58] RC Hughes. "Hot Electrons in Si O 2". In: *Physical Review Letters* 35.7 (1975), p. 449.

[59] HE Boesch Jr et al. "Hole Transport and Charge Relaxation in Irradiated SiO2 MOS Capacitors". In: *Nuclear Science, IEEE Transactions on* 22.6 (1975), pp. 2163–2167.

[60] FB McLean, HE Boesch Jr and JM McGarrity. "Hole transport and recovery characteristics of SiO2 gate insulators". In: *Nuclear Science, IEEE Transactions on* 23.6 (1976), pp. 1506–1512.

[61] FB McLean et al. "Application of stochastic hopping transport to hole conduction in amorphous SiO2". In: *Journal of Applied Physics* 47.4 (1976), pp. 1529–1532.

[62] F Barry McLean and Timothy R Oldham. *Basic mechanisms of radiation effects in electronic materials and devices*. Tech. rep. DTIC Document, 1987.

[63] AJ Auberton-Herve. "SOI: materials to systems". In: *Electron Devices Meeting, 1996. IEDM96., International*. IEEE. 1996, pp. 3–10.

[64] Jean-Pierre Colinge and J Colinge. *Silicon-On-Insulator technology: materials to VLSI*. Vol. 3. Springer, 2004.

[65] M Kochiyama et al. “Radiation effects in silicon-on-insulator transistors with back-gate control method fabricated with OKI Semiconductor 0.20 μm FD-SOI technology”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 636.1 (2011), S62–S67.

[66] J.R. Schwank et al. “Radiation effects in SOI technologies”. In: *Nuclear Science, IEEE Transactions on* 50.3 (2003), pp. 522–538. ISSN: 0018-9499. DOI: 10.1109/TNS.2003.812930.

[67] F.E. et al. Mamouni. “Gate-Length and Drain-Bias Dependence of Band-to-Band Tunneling-Induced Drain Leakage in Irradiated Fully Depleted SOI Devices”. In: *Nuclear Science, IEEE Transactions on* 55.6 (2008), pp. 3259–3264. ISSN: 0018-9499. DOI: 10.1109/TNS.2008.2006500.

[68] P. et al. Paillet. “Total ionizing dose effects on deca-nanometer fully depleted SOI devices”. In: *Nuclear Science, IEEE-TNS* 52.6 (2005), pp. 2345–2352. ISSN: 0018-9499. DOI: 10.1109/TNS.2005.860699.

[69] O. Flament, A. Torres and V. Ferlet-Cavrois. “Bias dependence of FD transistor response to total dose irradiation”. In: *Nuclear Science, IEEE-TNS* 50.6 (2003), pp. 2316–2321. ISSN: 0018-9499. DOI: 10.1109/TNS.2003.822594.

[70] R Ichimiya et al. “Reduction techniques of the back gate effect in the SOI Pixel Detector”. In: (2009).

[71] M et al. Kochiyama. “Radiation effects in Silicon-On-Insulator transistors with back-gate control method fabricated with OKI Semiconductor 0.20 μm FD-SOI technology”. In: *Nucl. Instrum. Meth. A* 636.1 (2011), S62–S67.

[72] Timothy R Oldham, FB McLean et al. “Total Ionizing Dose Effects in MOS Oxides and Devices”. In: *IEEE Transactions on Nuclear Science* 50.3 (2003), pp. 483–499.

[73] Timothy R Oldham. “Basic mechanisms of TID and DDD response in MOS and bipolar microelectronics”. In: *IEEE Nucl. Space Radiation Effects Conf. Short Course Notes*. 2011.

[74] M. Moll. “Radiation Damage in Silicon Particle Detectors - microscopic defects and macroscopic properties -”. PhD thesis. 1999.

[75] F. Honniger. “Radiation Damage in Silicon - Defect Analysis and Detector Properties -”. PhD thesis. 2007.

[76] G. Kramberger et al. “Initial acceptor removal in p-type silicon”. 2015.

[77] et al. I. Mandic. *E-TCT and charge collection studies with irradiated HVCMOS detectors*. Tech. rep. ATLAS ITk week Jun, 2015.

[78] P. Rossi L. Fischer, T. Rohe and N. Wermes. *Pixel detectors: From fundamentals to applications*. Springer, 2006, pp. 204–210.

[79] N Wermes, ATLAS CMOS Collaboration et al. “Depleted CMOS pixels for LHC proton–proton experiments”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (2015).

[80] Heinz Pernegger, ATLAS CMOS Collaboration et al. “Development of radiation hard CMOS active pixel sensors for HL-LHC”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (2015).

[81] Malte Backhaus. “Radiation-hard active CMOS pixel sensors for HL-LHC detector upgrades”. In: *Journal of Instrumentation* 10.02 (2015), p. C02031.

[82] Norbert Wermes. “From hybrid to CMOS pixels... a possibility for LHCs pixel future?” In: *Journal of Instrumentation* 10.12 (2015), p. C12023.

[83] Ivan Perić et al. “The FEI3 readout chip for the ATLAS pixel detector”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 565.1 (2006), pp. 178–187.

[84] M. Garcia-Sciveres et al. “The FE-I4 pixel readout integrated circuit”. In: *Nucl. Instrum. Meth. A* 636.1, Supplement (2011), S155 –S159. ISSN: 0168-9002. DOI: http://dx.doi.org/10.1016/j.nima.2010.04.101. URL: http://www.sciencedirect.com/science/article/pii/S0168900210009551.

[85] G-F Dalla Betta et al. “Development of a new generation of 3D pixel sensors for HL-LHC”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (2015).

[86] G Pellegrini et al. “3D double sided detector fabrication at IMB-CNM”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 699 (2013), pp. 27–30.

[87] J Chistiansen and M Garcia-Sciveres. *RD Collaboration Proposal: Development of pixel readout integrated circuits for extreme rate and radiation*. Tech. rep. CERN-LHCC-2013-008, 2013.

[88] P Valerio et al. “65nm technology for HEP: status et perspective”. In: *23rd International Workshop on Vertex Detectors (VERTEX 2014)*. 2014, p. 043.

[89] L. Gonella et al. “The shunt-LDO regulator to power the upgraded ATLAS pixel detector”. In: *JINST* 7.01 (2012), p. C01034. URL: http://stacks.iop.org/1748-0221/7/i=01/a=C01034.

[90] V. Fadeyev on behalf of Strip CMOS Collaboration. “Investigation of HV/HR-CMOS technology for the ATLAS Phase-II Strip Tracker Upgrade”. In: 2015.

[91] I. Peric. “Active pixel sensors in high-voltage CMOS technologies for ATLAS”. In: *Journal of Instrumentation* 7.08 (2012), p. C08002. URL: http://stacks.iop.org/1748-0221/7/i=08/a=C08002.

[92] E Vilella et al. “Prototyping of an HV-CMOS demonstrator for the High Luminosity-LHC upgrade”. In: *Journal of Instrumentation* 11.01 (2016), p. C01012.

[93] T Obermann et al. “Characterization of a Depleted Monolithic Active Pixel Sensor (DMAPS) prototype”. In: *Journal of Instrumentation* 10.03 (2015), p. C03049.

[94] T Kishishita et al. “Characterization of Depleted Monolithic Active Pixel detectors implemented with a high-resistive CMOS technology”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* (2015).

[95] Toshinobu Miyoshi et al. “Recent Progress of Pixel Detector R&D based on SOI Technology”. In: *Physics Procedia* 37 (2012), pp. 1039–1045.

[96] A. Holke et al. “A 200V partial SOI 0.18μm CMOS technology”. In: *Proc. of 22th International Symposium on Power Semiconductor Devices & ICS ISPSD, 2010, Japan, pp. 257-260* ().

[97] T. Hemperek et al. “A Monolithic Active Pixel Sensor for ionizing radiation using a 180nm HV-SOI process”. In: *Nucl. Instrum. Meth. A* 796 (2015), pp. 8–12.

[98] R. Turchetta et al. “A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology”. In: *Nucl. Instrum. Meth. A* 458.3 (2001), pp. 667–689.

[99] S. Fernandez-Perez et al. “Radiation hardness of a 180 nm SOI monolithic active pixel sensor”. In: *Nucl. Instrum. Meth. A* 796 (2015), pp. 13–18.

[100] Adelmo Ortiz-Conde et al. “A review of recent MOSFET threshold voltage extraction methods”. In: *Microelectronics Reliability* 42.4 (2002), pp. 583–596.

[101] *CERN group Irradiation system*. Website. `http://proj-xraymic.web.cern.ch/proj-xraymic/`.

[102] James R Schwank, Marty R Shaneyfelt and Paul E Dodd. “Radiation hardness assurance testing of microelectronic devices and integrated circuits: Radiation environments, physical mechanisms, and foundations for hardness assurance”. In: *Nuclear Science, IEEE Transactions on* 60.3 (2013), pp. 2074–2100.

[103] L Gonella et al. “Total Ionizing Dose effects in 130-nm commercial CMOS technologies for HEP experiments”. In: *Nucl. Instrum. Meth. A* 582.3 (2007), pp. 750–754.

[104] Hans Bichsel. “Straggling in thin silicon detectors”. In: *Reviews of Modern Physics* 60.3 (1988), p. 663.

[105] C. Gallrapp et al. “TCT, eTCT and I-DLTS measurement setups at the CERN SSD Lab”. 2014.

[106] et al. I. Mandic. *Status of TCT measurements with different HVCMOS test structures in Ljubljana*. Tech. rep. RD50 workshop December, 2015.

[107] et al. I. Mandic. *Studies of HV-CMOS sensors irradiated with neutrons*. Tech. rep. ATLAS MAPS Workshop Heidelberg, 2014.

[108] Garrin McGoldrick, Matevz Cerv and Andrej Gorisek. “Synchronized analysis of testbeam data with the Judith software”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 765 (2014), pp. 140–145.

[109] H. Perrey. “EUDAQ and EUTelescope Software Frameworks for Testbeam Data Acquisition and Analysis”. In: *Proceedings of Science (TIPP2014) 353*.

[110] *DRS4 Evaluation Board Users Manual*. Paul Scherrer Institute.

List of Figures

List of Tables

List of Acronyms

ADC Analogue to Digital Converter 88
AFP Forward Physics 15
ALICE A Large Ion Collider Experiment 3
ATLAS A Toroidal LHC ApparatuS 1
BOX Buried OXide 47
CCPD Capacitively Coupled Pixel Detector 60
CERN Conseil Européen pour la Recherche Nucléaire 2
CLIC Compact Linear Collider 125
CMS Compact Muon Spectrometer 3
CMOS Complementary Metal–Oxide–Semiconductor 17
DAQ Data AcQuisition 10
DUT Device Under Test 72
eTCT edge Transient Current Technique 99
FCC Future Circular Collider 125
FWHM Full Width at Half Maximum
GPAC General Purpose Adapter Card 88
HEP High Energy Physics 2
HL-LHC High Luminosity LHC 1
HSIO High Speed Input Output 109
IBL Insertable B-Layer 12
ILC International Linear Collider 125
ITk Inner Tracker 15
LEP Large Electron Positron collider 4
LHC Large Hadron Collider 1
LHCb Large Hadron Collider beauty 3
MAPS Monolithic Active Pixel Sensor 59
MIP Minimum Ionizing Particle 20
MOSFET Metal–Oxide–Semiconductor Field-Effect Transistor 31

MOS Metal–Oxide–Semiconductor 32
MPV Most Probable Value 89
NIEL Non Ionizing Energy Loss 16
nSQP New Service Quarter Panels 15
PCB Printed Circuit Board 99
PKA Primary Knock-on Atom 49
PMTs Photo Multipliers 109
PS Proton Synchrotron 107
RCE Reconfigurable Cluster Element 109
RHIC Relativistic Heavy Ion Collider 126
ROIs Regions-of-Interest 10
ROI Region-of-Interest 109
SCT Semiconductor Tracker 11
SEE Single Event Effects 45
SEU Single Event Upset 47
SM Standard Model 3
SMA SubMiniature version A 71
SNR Signal-to-Noise Ratio 39
SOI Silicon-On-Insulator 41
SPS Super Proton Synchrotron 107
STAR Solenoidal Tracker at RHIC 31
SUSY SUperSYmmetry 3
TCT Transient Current Technique 100
TDAQ Trigger and Data AcQuisition 10
TDR Technical Design Report 59
TID Total Ionizing Dose 16
TRT Transition Radiation Tracker 11
TSV Through-Silicon Vias 58