Universitat Autònoma de Barcelona

Analysis of Bidirectional Switch Power Modules for Matrix Converter Application

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Thesis dissertation presented to obtain the qualification of Doctor of Philosophy in Electronic and Telecommunication Engineering from the Electronic Engineering Department of Universitat Autònoma de Barcelona (UAB) by:

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1. Introduction

This chapter introduces the reader to the challenges of the Matrix Converter (MC) practical implementation. One fundamental problem with the MC topology is that it requires a matrix of switches called bidirectional switches (BDS) to connect each input phase to each output phase. Other commonly used names for these bidirectional switches are Alternating Current (AC) switches or four-quadrant switches. The focus of this thesis is upon the study and development of bidirectional switches with high level of integration allowing friendly and reliable MC realisation. An updated state of the art of MC as well as some aspects about the BDS implementation is introduced. The aims and the main structure of the thesis are also presented.

1.1. Background of the Thesis

The MC is a single-stage converter which carries out a direct AC-AC conversion by means of a matrix of switches [1]. A typical configuration of this topology is a three-phase voltage source with a three-phase load (generally a motor) as shown in Figure 1-1. This matrix of switches constitutes the power stage of the converter. As the industrial interest toward MCs has increased, different power stages specifically designed for MC applications are now available in industry standard packages. For instance, a full MC power stage in a single package is developed by Eupec [2] and a single AC switch is packaged separately in a module by Dinex [3]. All these different MC power stage implementations can be a solution to build more efficient MC prototypes. But, from the industrial applications point of view, a versatile, compact, high power density, high performance and efficient four-quadrant switch element is demanded. This is the basic idea behind the development of a new controlled bidirectional switch which integrates the power stage functionality with the intelligence in one device. That is, the controlled switching element should manage to switch-on or switch-off by itself depending on a simple control signal, to generate suitable control patterns to carry out a safe and efficient commutation processes and to implement local and global protection strategies to prevent the damage of the switch and the converter. Those can be some benefits of using this new switch which can make easy the MC implementation. The main disadvantages can be the complexity of integrating the control stage with the power one, the increase of the cost due to the different

components required to implement the control functionalities such as the gate drives, the isolated power supplies, the microcontroller or Field Programmable Gate Array (FPGA).

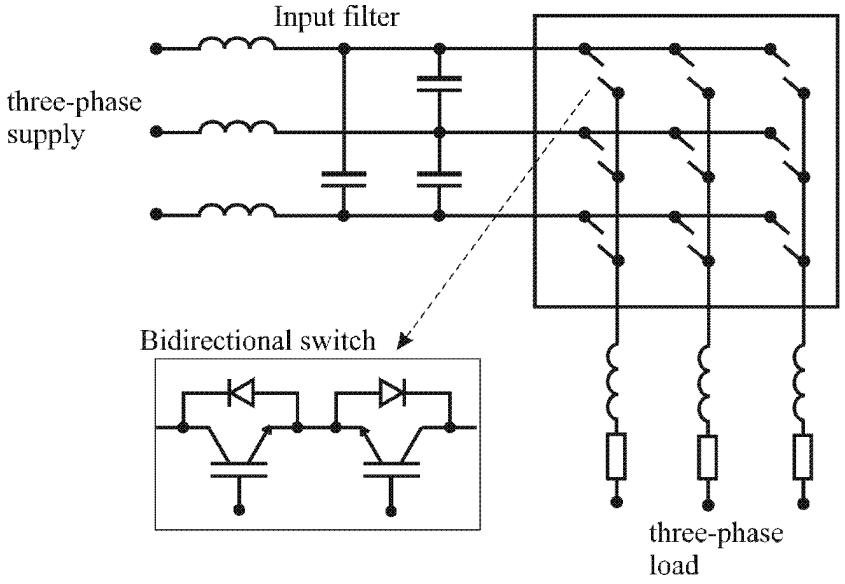


Figure 1-1 Matrix Converter topology

1.2. The Matrix Converter and its Implementation

Since one of the first attempts to establish the MC technology in 1976 by [1] till the first commercial Matrix Converter product in 2004 by Yaskawa Company [4] a great research effort in the fields of control algorithms, current commutation strategies and practical implementation has been carried out for thirty years [5]. The potential of this topology to perform direct AC-AC conversion as well as the growing number of industrial applications which require bidirectional transfer of power between the AC mains and a load has worth all this research work. The MC does not require large, bulky and expensive energy storage components so that it can be presented such as an almost all silicon compact solution for AC-AC power conversion. An array of controlled bidirectional switches (BDSs) are needed to connect directly an n-phase source to an m-phase load so that a variable output voltage of a desired amplitude and frequency can be generated [6].

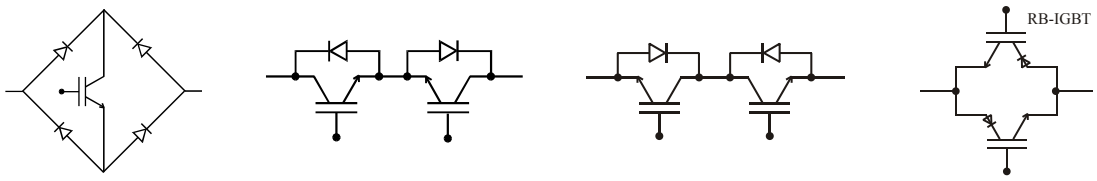
As there are no DC-link capacitors, the MC can be also a proper solution for Aerospace applications [7] where temperature and size are a handicap. Another application which can be fulfilled by the MC topology is in electric vehicles since weight and size as well as bidirectional power flow are the main constraints [8].

In the MC application as a motor drive [9] for rolling mills, elevators, centrifuges and escalators significant energy and cost savings can be achieved by returning the wasted energy to the main power supply, in addition, a space saving is obtained since no additional equipment for breaking is necessary. Another important application related to renewable energies that often require bidirectional power flow is processing energy from alternative sources such as wind [10, 11], photo voltaic [12] and fuel cells [13]. Smart-grids is also a potential application for MCs [14] due to its capability to control the bidirectional power flow, i.e. between the utility and smart-grids. Besides, the BDS itself has a potential role within the smart-grid acting as a power router. Power routers, distributed throughout the smart-grid according to the load-demand, can perform switching to connect particular loads with the desired input sources. Table 1-1 resumes the advantages, disadvantages of MC as an induction motor drive and the proposed solutions to overcome the main problems of this topology, too.

Advantages	
- No DC-link capacitors	
- No large, bulky and expensive internal energy storage components	
- Sinusoidal input/output currents with unity input power factor	
- High output voltage quality	
- Less harmonic distortion	
- Natural bidirectional power flow capability	
- High efficiency	
- Compact converter design	
- Suitable for applications under high temperature and pressure conditions	
Disadvantages	**Proposed solutions**
Poor voltage transfer ratio	Optimise modulation [15]
Large number of semiconductors and gate drives	Using RB-IGBTs [16] reduce the number of the power devices; a complete MC in a single package using devices connected in common collector configuration which requires only six gate drivers [2]. Use of specific modules implementing intelligent bidirectional switches [40].
Complexity of the control algorithms	Modern direct theories [17], [18]
Protection circuit	Alternative protection circuits [19],[20]
Sensitive to input voltage disturbances	New modulation strategies [21], [22]
Problems in the current commutation between BDSs	Multistep commutation strategies [23], [24], [25]
Not yet a mature technology	increase the reliability of MC hardware [26], [27]

Table 1-1 Pros, cons and solutions of MC as an induction motor drive

The MC implementation is the key point of the success of this alternative topology. A review of today solutions to build a MC and a power device status to construct a bidirectional switch is presented. As already explained MCs require bidirectional switches capable of blocking voltage in both polarities as well as conducting current in both directions. Nowadays, there are no such devices commercially available that accomplish these needs, so discrete devices need to be used to construct suitable BDSs as shown in Figure 1-2.



Diode bridge

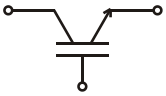
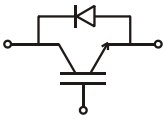
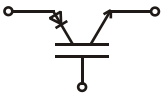
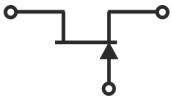
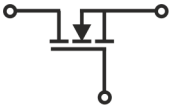
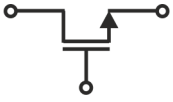
Anti-series IGBT and anti-parallel diode in Common Emitter

Anti-series IGBT and anti-parallel diode in Common Collector

Anti-parallel RB-IGBT

Figure 1-2 Possible BDS discrete implementations

The diode bridge (DB) arrangement uses only one active switching device so that current direction cannot be controlled. The common emitter (CE) and common collector (CC) arrangements allow the current direction to be controlled. Besides, the development of Silicon based devices as alternative to conventional Insulated Gate Bipolar Transistors (IGBTs) like the RB-IGBT (Reverse Blocking IGBT) [28] lead to simple BDS assemblies since such devices are able to block voltage in both polarities. The development of RC-IGBTs (Reverse Conducting IGBTs) [29] led also to the fabrication of compact BDSs with less chip count, as the anti-parallel diode usually connected with standard IGBTs is integrated in the same Silicon die in RC-IGBTs. In the framework of this thesis, a RB-IGBT was designed and fabricated in the clean room facility of the Institut de Microelectrònica de Barcelona - Centre Nacional de Microelectrònica (IMB-CNM, CSIC). This work led to apply for a patent [30]. Other emerging devices realised by the potential use of new semiconductor materials, such as Silicon Carbide (SiC) [31] or Gallium Nitride (GaN) [32] are also considered to build a BDS having fast switching and low loss characteristics because of their superior material properties. Other transition power devices in the form of a cascodes comprising SiC JFETs and low voltage Si power MOSFETs from Infineon [33], SiCED [34] and IXYS [35] have also been reported. Nowadays, commercial SiC JFET devices are already available [33]. Table 1-2 summarises the main features of the current and new device solutions in order to implement efficient BDSs. The BDS trend makes the MC topology less dependent on the device count so that its power stage cost can be minimised and a compact design achieved.

Controlled device	Pros	Cons	Accessible
Conventional IGBT (Si) 	Maturity technology, spread used in industrial drive applications.	Limited reverse blocking capability. Requires external diode	Great range in current and Breakdown voltage (BV)
RC-IGBT (Si) 	Less silicon, simple module assembly	Need to add in series another RC-IGBT to block reverse voltage	• Infineon , Semikron and Fuji Electric [36]: Great range in current and BV • IXYS: IXGA30N60C3C1, 600V, 30A, IGBT (Si) + SiC Anti-Parallel Diode
RB-IGBT (Si) 	Forward and reverse voltage can be blocked	Slow turn-off switching	• IXYS: IXRH50N120, 1200V, 60A • Fuji Electric: FGW85N60RB, 1200V, 85A
MOS Turn-off Thyristor (MTO) (Si)	reverse voltage blocking capability	Two devices in antiparallel are needed	Range in high current and high BV
SiC JFET 	Reduced switching losses with respect to the available IGBT (Si), low conduction losses, high temperature operation, high BV	High cost, few commercial devices	Infineon: IJW120R100T1, 1200V
SiC MOSFET 	High switching frequency, low switching losses, high temperature operation,	High cost, high conduction losses	Cree: CMF10120D, 1200V, 24A
GaN HEMT 	High speed switching frequency, high efficiency operation, low on-state resistance	High cost, lack of commercial specific gate drivers	

Blocked device	Pros	Cons	Accessible
Conventional Diode (Si)	Technology maturity	Limited in temperature, significant switching losses due to their reverse recovery behaviour	Great range in current and BV
SiC-SBD (Schottky Barrier Diode)	High temperature operation, low losses characteristics, high BV	High cost	CNM, Infineon, IXYS, Fuji Electric

Table 1-2 Power devices useful for developing BDSs

In terms of device count a comparison can be made between the MC and a conventional AC-AC converter with intermediate DC-link taking into account the switch configuration. This comparison is summarised in Table 1-3.

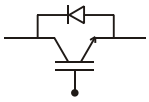
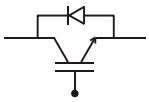
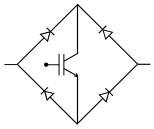
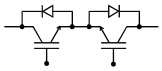
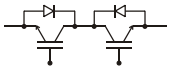
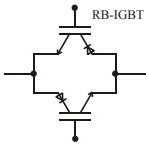
Topology		Switch Configuration	Fully controlled devices	Fast diodes	Rectifier diodes	Electrolytic capacitors bank	Large inductors	Total devices count
Conventional AC-DC-AC	Inverter with diode bridge		6	6	6	1	0 or 1	18
	Back-to-Back inverter		12	12	0	1	3*	24
Matrix Converter	1		9	36	0	0	0	45
	2		18	18	0	0	0	36
	3		18	18	0	0	0	36
	4		18	0	0	0	0	18

*Table 1-3 Switch configurations and chip count of AC-AC converters. *Inductors on the input side of the back-to-back converter [37]*

As it is described in Table 1-3, a back-to-back inverter requires twenty-four semiconductors (twelve IGBTs, twelve diodes), in the same way the MC needs thirty-six semiconductors (eighteen IGBTs, eighteen diodes) if conventional IGBTs in a common emitter or in a common collector configuration are applied. However, the use of RB-IGBTs reduces the number of semiconductors in the MC by 50% bringing the converter in a real competitive position to the well-known DC-link topology.

Some semiconductors manufacturers have produced power modules specially designed to build MCs and thus, enhance its realisation.

A complete MC in a single package (Figure 1-3a, Figure 1-3b) for lower power levels is possible to be built using power devices connected in the common collector

configuration [2]. To implement a power stage of a MC in a module all eighteen diodes and eighteen IGBTs must be connected in such a way that they build nine BDSs in a common collector configuration. The matrix structure should be realised internally, so that the twenty-four necessary external connections can be grouped in to six emitter potentials as deduced from Figure 1-3c. For instance, one emitter group could be G_{R1}, G_{R2}, G_{R3} and E_R and so on. While emitters and gates of the input are already sorted, emitters and gates of the output are still spread over the whole module. To get a symmetric module, the gate and emitter connections of the output would need to be sorted. With a bus bar structure running along the middle of the module a symmetric module can be realised. Thus, three gates belong to each of six emitter potentials as shown in Figure 1-3c. Every gate needs its own gate unit, but isolated power supplies are only needed for each emitter potential. Therefore, only six isolated power supplies are required for the whole converter.

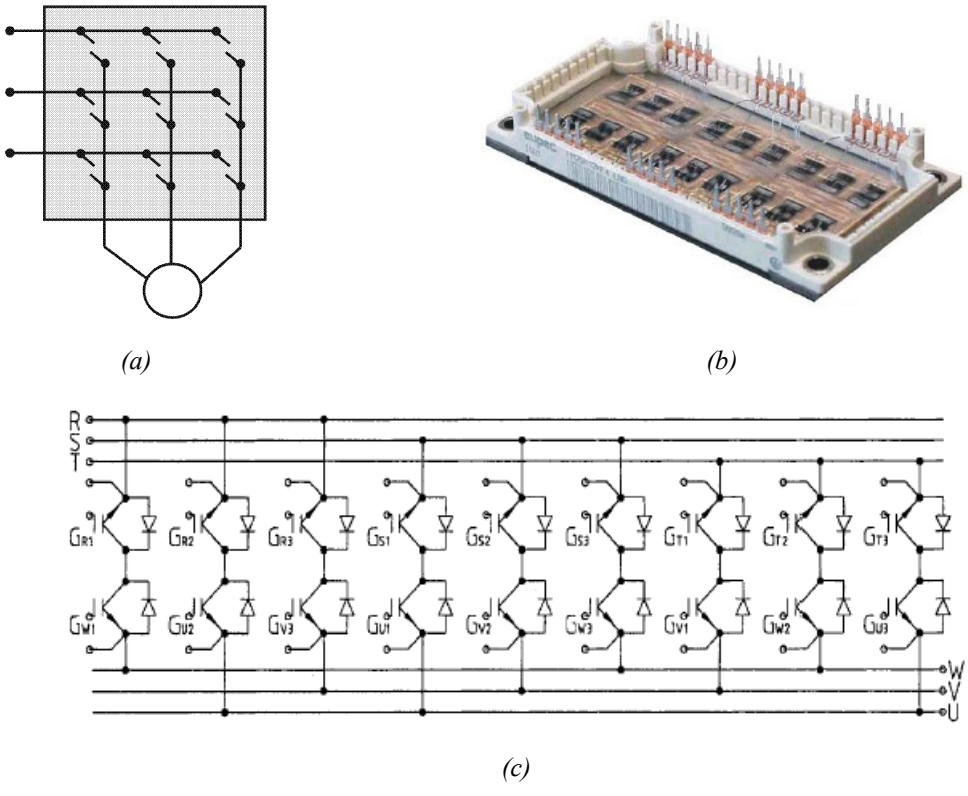
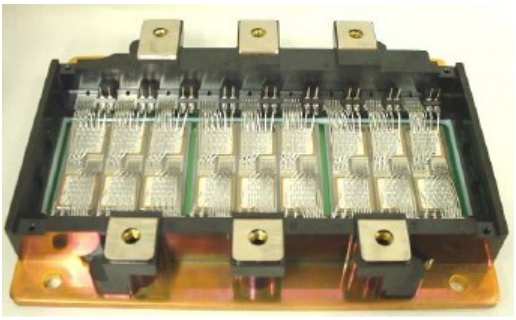
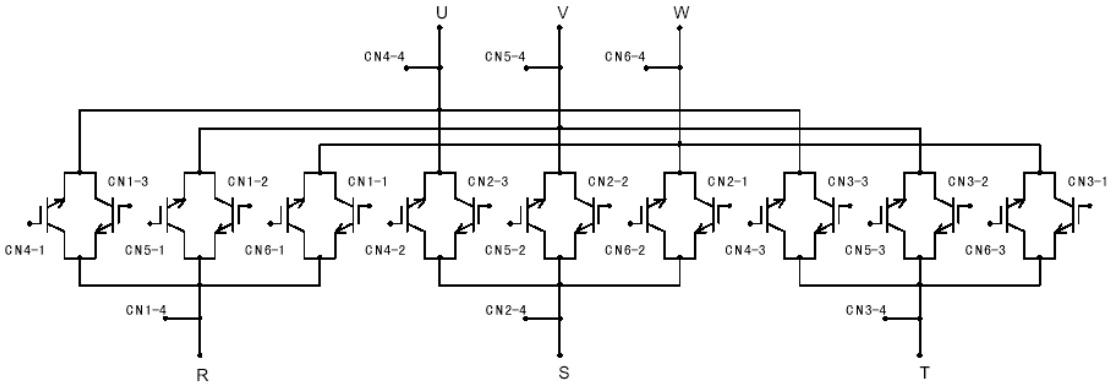


Figure 1-3 a) Scheme of a complete MC in one package. b) An EUPEC & SIEMENS 7.5 kW Matrix Converter module. c) Schematic of the Power stage module, R, S, T are the input phases; W, U, V, are the output phases and G_{R1} till G_{W3} are the eighteen IGBT gate terminals

A prototype module configured for the MC application using RB-IGBTs in [16] follows the same module concept as mentioned before, a MC in a single module. Figure 1-4a shows the internal layout with the eighteen RB-IGBTs chips building a complete MC power stage. As it can be appreciated in the connection diagram of Figure 1-4b the number of discrete devices is half of the Eupec module. The need for series connected diodes is eliminated due to the RB-IGBT behaviour.



(a)



(b)

Figure 1-4 a) 22kW prototype MC module. b) Schematic of the power stage module

It is also possible to build a complete MC with three output legs in a single package (see Figure 1-5). One of the first approximations was possible by rearranging the interconnection of the devices in a standard six-pack IGBT module, giving the converter a greater power density and lower stray inductance as found in a six-pack IGBT module of Semikron [38] for MC applications. It operates with currents up to 450 A and voltages up to 1700 V. This module includes an integrated NTC temperature sensor for measuring the heat sink temperature in the vicinity of the chips. There are also available commercially modules from Dynex and Semelab [39] as depicted in Figure 1-5c and in

Figure 1-5e, respectively. They implement one output leg of a MC in common emitter configuration. A schematic diagram of the internal circuit arrangement of Dynex and Semelab modules is shown in Figure 1-5b and Figure 1-5d, respectively. These modules allow the designer to build high power converters.

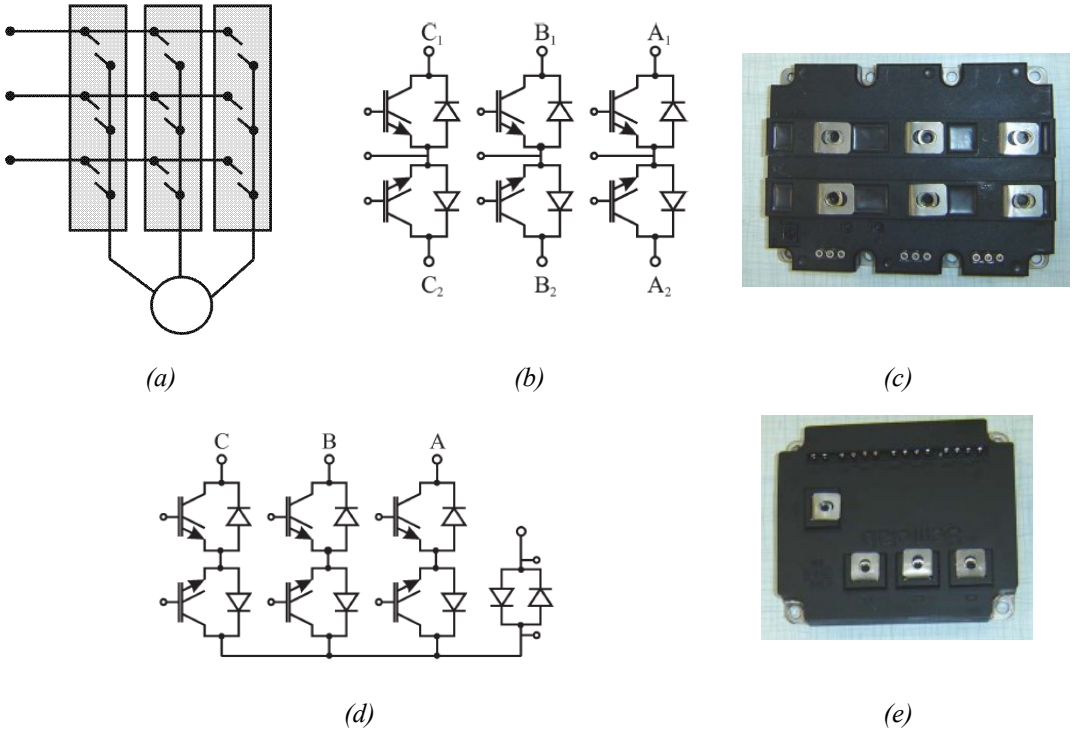
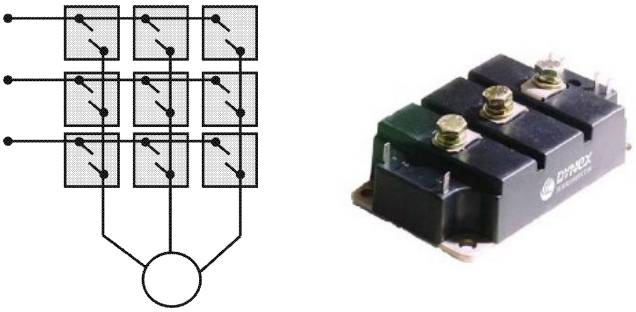


Figure 1-5 a) Scheme of a MC output leg in a single package. b) Schematic diagram of the internal circuit of DIM600EZM17-E000. c) Dynex module, DIM600EZM17- E000, 1700V, 600A. d) Schematic diagram of the internal layout of SML300MAT06. e) Semelab module, SML300MAT06, 600V, 300A

Finally, a whole MC can be also implemented by assembling in the right way nine BDS packaged separately in a module as shown in Figure 1-6a. The first attempt to build a BDS is the diode bridge FIO50-12BD from IXYS (schematic diagram shown in Figure 1-2), but it presents high conduction losses since three devices are always conducting. In addition, the direction of the current cannot be controlled. On the other hand, a BDS in a common emitter configuration allows the current direction to be controlled. This device is accessible commercially by Dynex [3]. It is suitable for higher power applications, which allow operating with currents up to 400 A and voltages up to 1700 V. The main advantage of this module is the modularity that introduces in the MC design as well as the easy replacement of a damaged component without throwing away the entire module as it could be the case in the power modules of Figure 1-3, Figure 1-4

and Figure 1-5. Nevertheless, the main drawbacks of this solution compared with the previous module solutions are the achievement of a worse compactness, the increase of the converter size and the addition of stray inductances in the power circuit. Therefore, there is a trade-off between modularity and compactness in MC design. One of the objectives of this thesis will be the development of BDS modules including part of the control circuitry in order to achieve additional levels of integration.



(a) *(b)*

Figure 1-6a) BDS of the MC in a single package. b) Dynex module, DIM400PBM17, 1700V, 400A

Table 1-4 summarises the main aspects to be taken into account when selecting one of the power modules to construct a MC.

Characteristics	**Part reference**	**Configuration, No. of BDSs**	**Isolated gate drive power supplies**	**Manufacturer**
1200V, 50A	FIO50-12BD	DB, 1	9	Ixys
1200V, 60A	SK60GM123	CE, 1	9	Semikron
1700V, 400A	DIM400PBM17	CE, 1	9	Dynex
600V, 300A	SML300MAT06	CE, 3	9	Semelab
1700V, 600A	DIM600EZM17-E000	CE, 3	9	Dynex
1200V, 35A	FM35R12KE3	CC, 9	6	Eupec
1200V, 50A	18MBI150W-120A	RB-IGBT, 9	6	Fuji

Table 1-4 Main features of power modules commercially available to build a MC

1.3. Aims and Structure of the Thesis

A list of power modules based on the bidirectional switch concept for implementing MCs has been presented in this chapter. All these possible solutions implement only the power stage of the converter, an external control stage is needed to carry out the power conversion, and most of them become useless if one power device of the module is destroyed. One of the aims of this work is to improve the feasibility of the MC topology by using an intelligent bidirectional switch power module capable of full controlling itself. In this way, a local control circuitry is included in the module providing for instance the smart switching sequences for the current commutation strategy. In addition, the modular design allows easy replacement of damaged BDSs in an entire MC and makes the power and signals interconnections easier. Moreover, more efficient BDS modules can be implemented taking advantage of the new emergent power semiconductor devices.

The realisation of specific power modules implementing the BDS function for MC applications needs an in depth understanding of the commutation processes involved in this kind of power converter. In addition, the MC can be best suited to several applications with different specifications (voltage and current levels, volume, temperature, frequency operation) to be satisfied by the power components as the heart of the circuit. Hence, the selection of the optimum power semiconductors to implement MC applications determining the associated power losses is another aim of this research work. Cooling requirements can also be deduced from this analysis.

This PhD thesis report will try to develop the different issues mentioned above. It consists of seven chapters including the present one (introductory chapter 1). Conclusions are drawn in each chapter and a final conclusion will sum-up the main results. A list of references supporting the work is also included. In the appendix A, acronyms and symbols used in the thesis are enumerated. Appendix B describes how the switching losses are calculated. Appendix C explains in detail the implementation of the Venturini and double-sided space vector modulation algorithms.

Chapter 2 deals with the analysis of aspects related to the BDS concept such as the BDS configuration and realisation from discrete power devices. A SPICE simulation of a simplified MC, i.e. two-phase to single-phase MC, is performed in order to analyse the commutation processes involved between BDSs. Identification of a critical time interval during the commutation procedure is also discussed.

Chapter 3 introduces the test of BDS devices. A specific test circuit based on a simplified two-phase to one-phase MC structure is designed and fabricated in order to study the switching behaviour of BDSs formed by discrete devices or by a power module. The voltage and current of the devices involved in the commutation are measured so that the associated power losses can be directly determined. BDSs of different technologies are implemented and tested under the reduced MC switching test circuit. From the acquired data, static and dynamic power losses models are presented and discussed for each power device involved in BDS implementations.

Chapter 4 describes a method for the estimation of the semiconductor power losses in MC based on the static and dynamic characterisation of the BDSs devices performed in chapter 3. The conduction and switching power dissipation modelling are derived from the power device physical behaviour. The numerical calculation power losses method is presented, applied and validated for a standard VSI converter. It is important to have an accurate power losses model to acquire a better understanding of effects of the device technology on the power dissipation of AC/AC converters as analysed in chapter 5.

Chapter 5 extends the numerical power losses computation method validated for a VSI in chapter 4 to a MC. Higher complexity is added in the MC since the energy losses depend on the voltage and current throughout the output period of the converter. The implementation of the dissipation computation method is performed by means of MATLAB scripts allowing a fast evaluation and a modular design. The semiconductor power losses within a BDS are calculated according to the converter operating parameters such as: the modulation control, input and output frequency, input and output voltage rate, output current, switching frequency, power factor of the load, etc. A

prediction of the losses is crucial to help the designer to, for instance, select the suitable power devices according to the converter application.

Chapter 6 presents the implementation of an integrated bidirectional switch intelligent power module (BDS-IPM). Its structure, fabrication and electrical characterisation are detailed. In addition, an application example of the BDS module which consists of building a prototype three-phase to one-phase MC is described and discussed. This work has derived in the request of a patent [40].

Chapter 7 summarises and highlights the main achievements of the work done.

2. Analysis of the BDS's Commutation Phenomena

This chapter describes different BDS implementations which enable the MC construction (Figure 2-1). The static and dynamic characteristics of the power semiconductors devices forming a BDS are described. Current commutation strategies based on the output phase current direction are discussed in this chapter. We will focus on the study of BDS's commutation process.

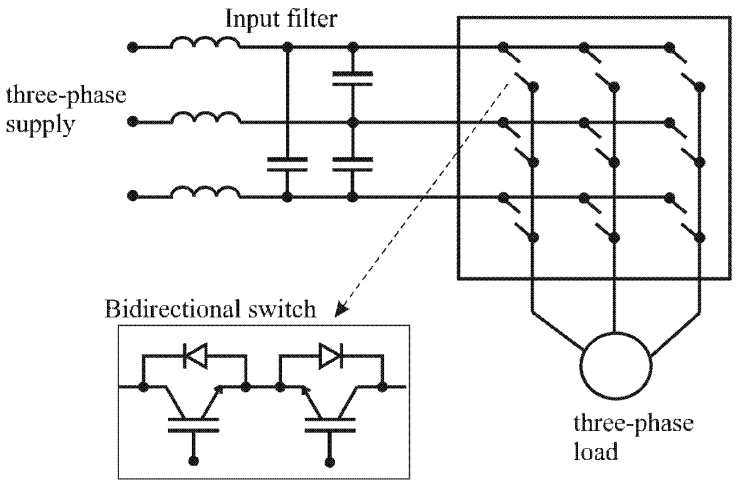


Figure 2-1 A three-phase to three-phase MC circuit

2.1. BDS Topology

The key element for implementing MCs is the controlled BDS, which can be realized by power semiconductor devices allowing high frequency operation. These BDSs will be opened and closed in a controllable way so that the desired output voltage and input current can be achieved. It must be kept in mind that input terminals of the MC should not be short circuited because it is usually fed by a voltage source, and that the output phases must be never opened because the load has an inductive nature. So a suitable control must be provided to avoid overcurrents and overvoltages in the MC. With these constraints, the three-phase to three-phase MC has twenty-seven possible switching states [41].

BDSs must capable of blocking voltage of both polarities as well as conducting current in both directions. Nowadays, discrete devices need to be used to construct suitable BDSs. These are diodes and controlled switching devices. Nevertheless, a monolithic bidirectional device concept has recently appeared and is under

development. It will provide bidirectional behaviour in one single die as referred in subsection 2.1.6. In the following BDS realisations, it has been assumed that the Silicon (Si) controlled switching device would be an IGBT, but other power devices such as MOSFETs, MCTs and Integrated Gate-Commutated Thyristors (IGCTs) can be used in the same way. Likewise, controlled gate devices based on wide band-gap (WBG) semiconductor materials such as Silicon Carbide (SiC) are also a very promising option to build a BDS. Different BDS realisation with discrete semiconductors are now presented.

2.1.1. Diode Bridge BDS

The diode bridge (DB) was the first BDS used for a MC application [42]. It is made up of an IGBT at the centre of a single-phase diode bridge arrangement as shown in Figure 2-2. The main advantage is that both current directions are carried by the same switching device, therefore, only one gate driver is required per each BDS. Device losses are relatively high since there are three devices in series in each conduction path. Currently, other BDSs realisations with better characteristics are implemented, we discuss them next.

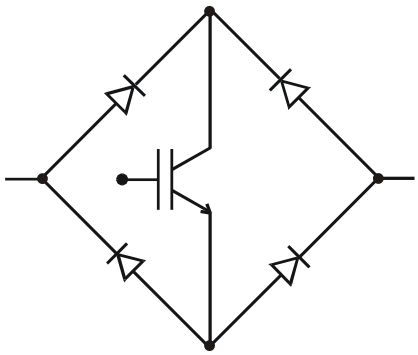
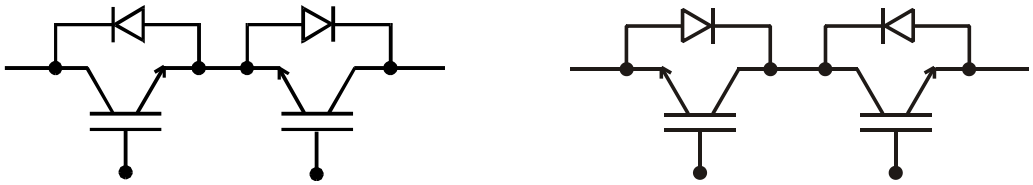


Figure 2-2 Diode bridge BDS

2.1.2. Common Emitter BDS

The common emitter (CE) BDS arrangement consists of two diodes and two controlled IGBTs connected in anti-parallel and anti-series, respectively, as depicted in Figure 2-3a.



(a) *(b)*

Figure 2-3 BDS realisation: a) Common Emitter, b) Common Collector

The diodes are included to provide the reverse blocking capability. This configuration, unlike the diode bridge BDS, allows controlling independently the direction of the current in the BDS. In addition, conduction losses are reduced since only two devices carry the current at any one time. One possible disadvantage is that each BDS requires an isolated power supply for the gate drives, but both devices can be driven with respect to the common emitter point.

2.1.3. Common Collector BDS

The common collector (CC) BDS arrangement is shown in Figure 2-3b. The conduction losses are the same as the CE BDS. The advantage of this configuration is that only six isolated power supplies are needed to supply the gate drive signals of a whole three-phase to three-phase MC. A more detailed description will be presented in the integrated power modules section. However, this arrangement is often not feasible in a large practical system since stray inductances between commutation cells cause problems. Hence, the common emitter configuration is often preferred for creating the BDSs required for a MC.

2.1.4. BDS with RB-IGBTs

The development of IGBTs with reverse-blocking capability (RB-IGBTs) allows forming a bidirectional switch without the diodes (Figure 2-4). This BDS consists of two RB-IGBTs connected in anti-parallel. This arrangement leads to voltage drop reduction of the switch, due to lack of the diode and because current towards the load flows only through one device. In the literature, we can find a simulated MC with RB-IGBTs [43] and a practical MC motor drive implementation with RB-IGBTs [44], too.

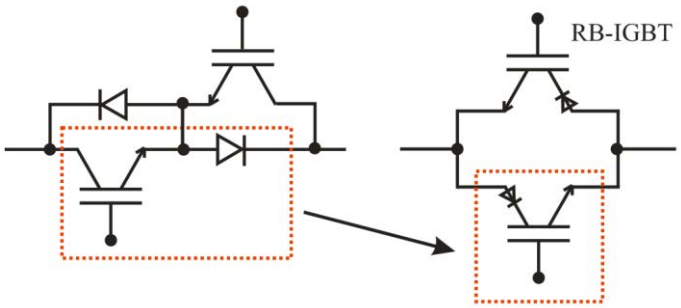


Figure 2-4 BDS is built with two anti-parallel RB-IGBTs

In the framework of this thesis an RB-IGBT power device has been designed, fabricated in the clean room facility of the IMB - CNM (CSIC) institute and later tested [45] as a solution to implement a BDS. This work has led to a patent [46] which claims for a low-cost trench isolation technique for reverse blocking using Boron Nitride doping wafers. A conventional IGBT cell is depicted in Figure 2-5a. This structure is not capable to block a significant negative collector-emitter voltage since the device suffers from leakage current because the depletion region reaches dicing surface at the chip side, where severe strain remains after mechanical dicing process and no passivation layer exists. Then, a proper periphery termination is mandatory in order to obtain reliable reverse blocking capability as shown in Figure 2-5b.

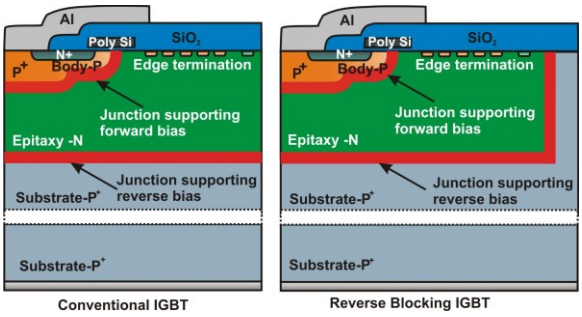
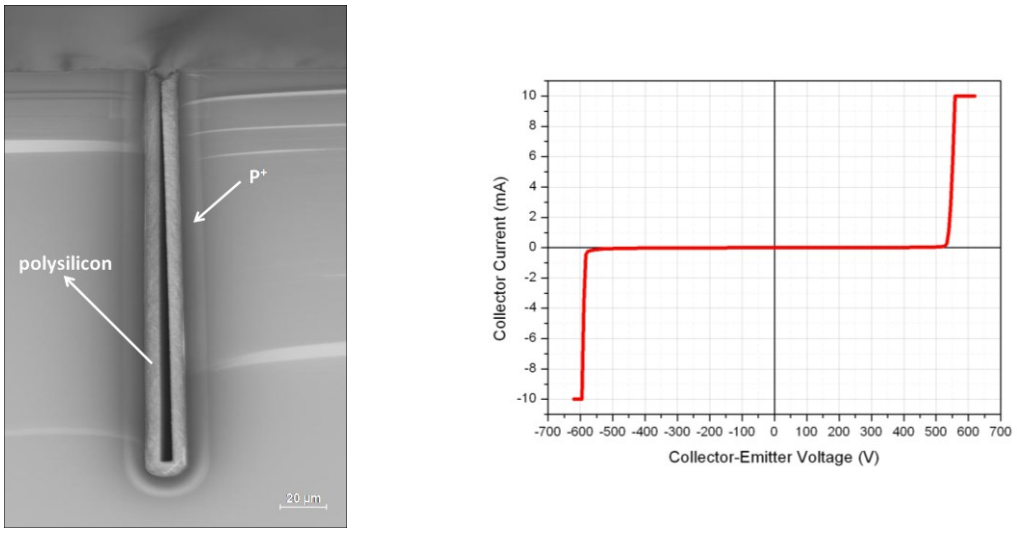


Figure 2-5 Basic cell and termination of a conventional a) IGBT; b) RB-IGBT

Different techniques are used in order to provide a reliable reverse blocking capability. The diffusion isolation technique is the most spread one used in commercial devices [47]. However, the area used to protect the periphery is elevated, i.e. waste of material and rise of the process cost. In addition, this diffusion process requires important resources (high temperature, >1250ºC, and long thermal process) as well as the use of specific equipment. On the other hand, our proposed technique is based on

the trench isolation method which consists in defining a shallow trench in the silicon with an appropriate etch technique at both sides of the scribe-line of the chip. Since the width of the trench can be around 15 µm, the save in the silicon area used to protect the periphery is significant in comparison with other techniques. The doping of the trenches has been performed using a solid source instead of ionic implantation. The use of a solid source means to place Boron Nitride (BN) doping wafers between process wafers and to perform an oxidation at high temperature in order to introduce boron impurities inside the trenches as shown in the cross-section Scanning Electron Microscope (SEM) of Figure 2-6a. The main advantages of this method are a simple, repetitive, uniform and low-cost process technology. In addition, the equipments needed are standard diffusion and annealing furnaces used in any clean room.

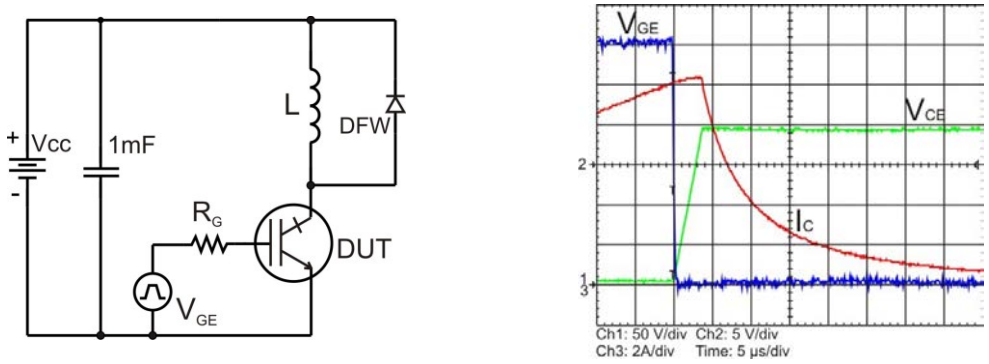


(a) *(b)*

Figure 2-6 a) SEM picture of a trench region cross section. The uniformity of the P+ diffusion around the walls with a depth of around 10 µm can be appreciated; b) Bidirectional blocking characteristics of the fabricated RB-IGBT

Figure 2-6b shows the forward and reverse blocking characteristics of one of the fabricated RB-IGBT assembled on a TO-247 size package. Reverse blocking voltages of 600V have been successfully achieved at gate-emitter shorted. The evaluation of the switching behaviour of the RB-IGBT has been carried out under inductive load (Figure 2-7a) obtaining the turn off waveforms shown in Figure 2-7b. As expected, a long current tail is clearly depicted when the RB-IGBT is turned-off (V_{GE} = -15 V) with the full applied voltage (200 V) since the RB-IGBT has not an N+ buffer layer to control

the carriers' injection from the collector side. So, a lifetime control process will be required. This work will be done in a further step. It will consist on an irradiation process to kill the carrier lifetime improving the switching characteristics. For this reason, the in home RB-IGBT will not be used in the following studies, but a commercial RB-IGBT will be used instead.



(a) *(b)*

Figure 2-7 Turn-off of a non-irradiated RB-IGBT a) Test circuit; b) Waveforms

2.1.5. BDS with SiC Power Devices

SiC power semiconductors have become very attractive devices for power converters applications due to its intrinsic advantages as high-voltage blocking capability, low on-state voltage drop, high switching speed, and low thermal resistance [48]. In addition, power converters with higher efficiencies are possible with SiC devices due to lower switching losses compared to conventional Si based devices [49]. Unipolar SiC devices can also operate at a high temperature due to its high thermal conductivity and wide band energy favouring them for applications with high ambient temperatures such as the aerospace one [50]. Recently, two types of unipolar SiC power devices are commercially available, Schottky Barrier Diodes (SBDs) from several manufacturers (Infineon [33], Cree [51], IXYS [35], etc) and power switches like Metal-Oxide-Semiconductors-Field-Effect-Transistors (MOSFETs) [51]; normally-on [33] and normally-off (enhancement mode, EM) Junction-FETs (JFETs) [52]; and Bipolar Junction transistor (BJT) [53]. An improvement of the limitations associated to the Si technology (i.e. high operating temperatures, high demanding switching frequencies, lower switching losses, high power efficiency) will be possible due to SiC semiconductors. Different works have investigated the performance and switching

characteristics of the SiC devices in matrix converters topologies [54, 55]. Figure 2-8 shows different BDS realisations based on SiC power devices.

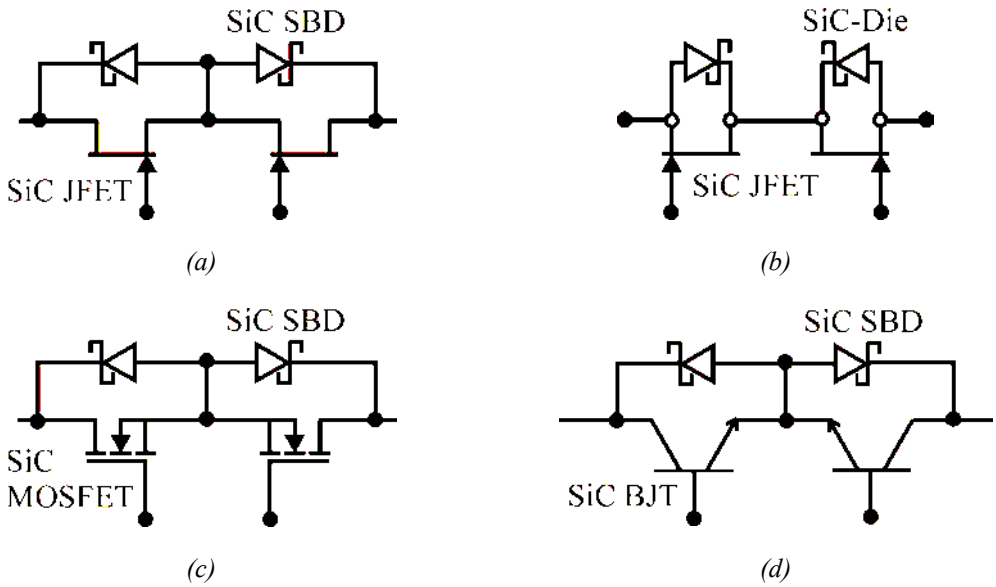
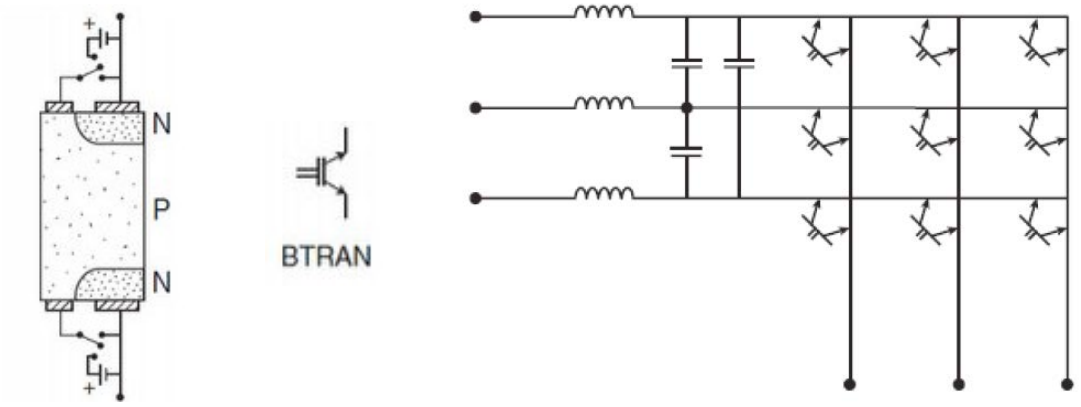


Figure 2-8 Full SiC BDS realisations based on. a) Normally-Off SiC JFETs in common source with anti-parallel SiC Schottky diodes; b) Normally-On SiC JFETs in common drain with built-in diodes; c) SiC MOSFETs in common source with anti-parallel SiC SBDs; d) SiC BJTs in common emitter with anti-parallel SiC SBDs

2.1.6. Bidirectional Bi-Polar Junction Transistor (B-TRAN)

A new Silicon power semiconductor switch has been recently developed by Ideal Power [56]. It is called Bi-directional Bipolar Junction TRANsistor (B-TRAN). Figure 2-9a shows the topology of the new switch which has a simple, 3 layer, 4 terminal, vertically symmetric double sided structure with a control switch on each side. This topology allows the B-TRAN device to block voltage or conduct current in each direction with equal performance. Figure 2-9b shows the corresponding electrical symbol. A Matrix converters application based on B-TRAN devices is depicted in Figure 2-9c. The number of required AC switches should be only nine compared to the eighteen elements if the converter is based on RB-IGBTs or thirty-six if the BDS is formed by two IGBTs and two diodes. This will result in a small, compact and low cost converter. At present B-TRAN device is a concept under development.



(a) *(b)* *(c)*

Figure 2-9 a) B-TRAN topology; b) B-TRAN circuit symbol; c) Matrix Converter application [56]

2.1.7. Dual-gate Normally-ON GaN HEMT

A concept of bidirectional device based on a dual-gate normally-ON Gallium Nitride High-Electron-Mobility Transistor (GaN HEMT) device is shown in Figure 2-10. This high voltage switch can be an excellent candidate for the emerging solid-state circuit break (SSCB) applications [57] i.e. DC circuit protection. The GaN switch is essentially made of two HEMTs sharing a common drain to stand high voltage blocking in either direction.

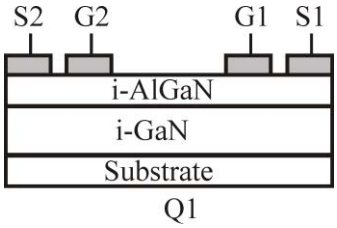


Figure 2-10 Concept of a dual-gate normally-ON GaN HEMT device [57]

2.2. Current Commutation

MCs, unlike VSIs (Voltage Source Inverter, typical inverter topology), have no natural freewheel paths. This fact can cause problems when commutating current from one device to another. Hence, the commutation has to be actively controlled at all times with respect two basic rules:

- There is only one switch in on state connected to an output phase during any instant of time; i.e. this would avoid an input line to line short circuit.
- At least two switches of the MC must be in on state in order to guarantee a closed-loop path for the inductive load current.

These two considerations and the fact that power devices cannot be switched instantaneously, make necessary employing control methods to provide a safe commutation.

2.2.1. Basic Current Commutation

The two simplest forms of commutation strategy, overlap and dead-time current commutation need extra circuitry to avoid destruction of the converter. Dead-time commutation [58] uses a period where no devices are gated, causing a momentary open circuit of the load. Then some form of voltage clamping or snubber is need across the switch cells to provide a path for the load current. The introduction of dead times increases the losses and the clamping devices result in an increase of the converter size. The overlap current commutation [59] was used as an alternative to dead-time. The incoming cell is fired before the outgoing cell is switched off. This would normally cause a line-to-line short circuit but extra line inductance in the input lines slows the rise in current so that safe commutation is achieved. This method is undesirable since the inductors are large and expensive.

2.2.2. Current Direction Based Commutation

The most wide spread current commutation method applied to MC is the four-step. Others methods derived from the four-step such as two-step, three-step and single-step are also briefly described.

2.2.2.1. Four-step Current Commutation

A more reliable method of current commutation is based on the four-step commutation strategy [60] in which the direction of current flow through the BDS must be known in order to achieve a safe commutation. In order to explain the four-step strategy and the following current commutation methods a two-phase to single-phase MC circuit (Figure 2-11) has been considered since all undergone commutations in a three-phase to three-phase MC can be reproduced in this simplified circuit. In steady state, it is assumed that the load current (I_L) is in the direction shown in Figure 2-11 and that *BDS-Aa* is closed, that is both of the devices in the active BDS (S_{Aa1} *and* S_{Aa2}) are gated in order to accommodate both current directions, and *BDS-Ba* is opened. The timing diagram of Figure 2-12a shows the order and time each device is conducting when the direction of I_L is positive; the delay time (t_d) is the time interval between each switching event and is determined mainly by the dynamic characteristics of the devices

used in the BDS implementation. The states diagram in Figure 2-12b describes the safe switch state combinations for a commutation between switch S_{Aa} and S_{Ba} based on commutation sequence shown in Figure 2-12a.

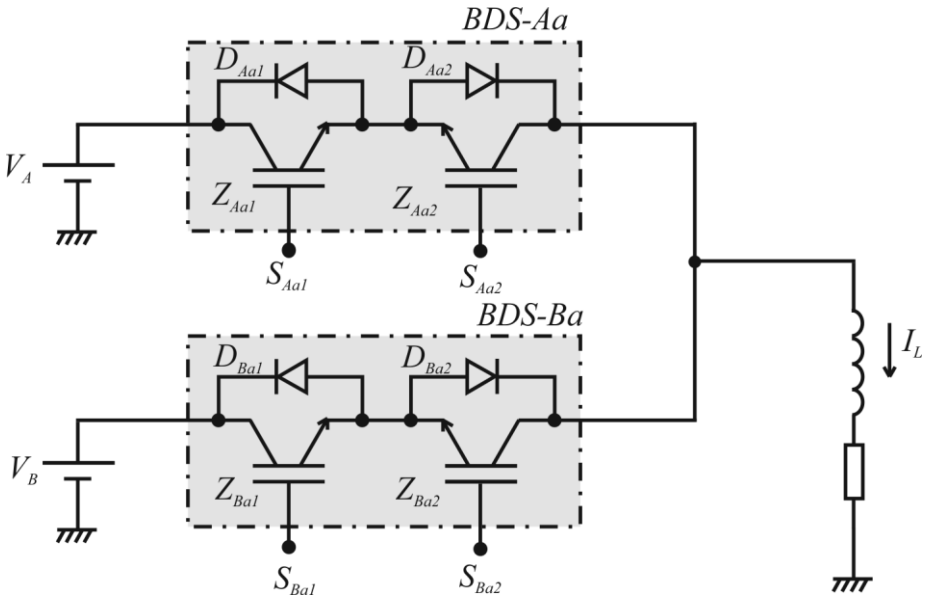
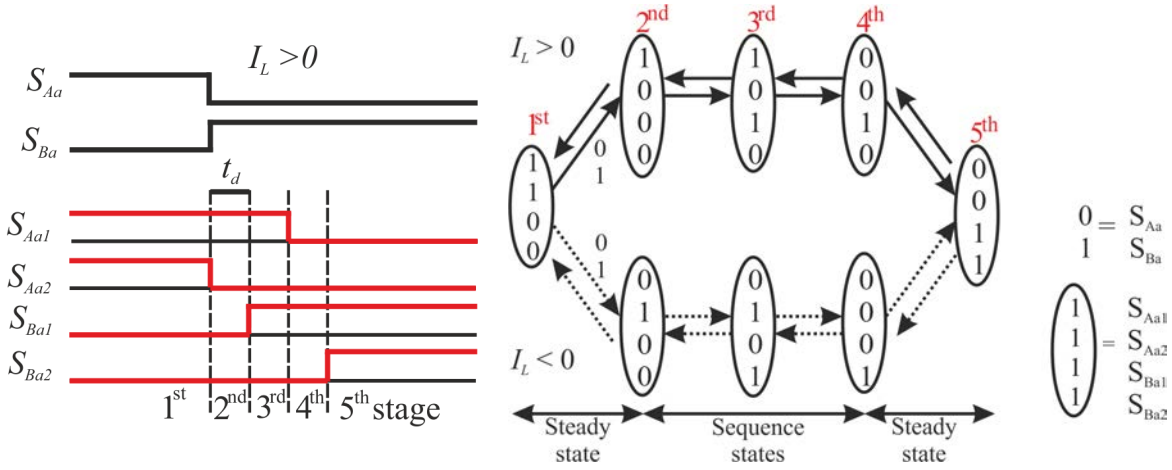


Figure 2-11 Schematic of a two-phase to single-phase MC



(a) *(b)*

Figure 2-12 Four-step current commutation between two BDSs. a) Timing diagram when the direction of I_L is positive; b) State representation. (SAa and SBa are the switch control signals provided by microcontroller or DSP and SAa1 , SAa2, SBa1, SBa2 are the gate control signals of each IGBT within the BDS, the direction of I_L is positive (solid lines) when the current flows towards the load and negative (dashed lines) when it flows towards the input voltage source.)

The commutation sequence is now described:

- **1st stage**: the load current flows through device S_{Aa1} towards the load.
- **2nd stage:** a commutation to S_{Ba} is required, the current direction is used to determine which device in the active BDS is not conducting. Thus, device S_{Aa2} is turned-off.
- **3rd stage**: the device within *BDS-Ba* that will carry the current is then gated, in this case S_{Ba1}. This fact does not cause any short circuit between input phase *A* and *B*, because the current through S_{Aa1} and S_{Ba1} flows in the same direction.
- **4th stage**: S_{Aa1} is turned off. In this way, S_{Ba1} conducts the entire load current.
- **5th stage**: S_{Ba2} is switched on in order to allow the *BDS-Ba* to behave bidirectional in current flow.

This method allows a reliable current commutation from one BDS to another BDS. It has also the advantage that the switching losses in the devices are reduced by 50 % because half of the commutation process is soft switching [61], that is, S_{Aa2} and S_{Ba2} are switched at zero current in our case. Hence, this method is often called "semi-soft current commutation".

2.2.2.2. Other-step Current Commutation

One modification of the four-step commutation method is to only gate the conductive device in the BDS as shown in Figure 2-13a, which leads to a two-step current commutation strategy [62].

The four-step current commutation strategy can be reduced to a three-step commutation strategy, as depicted in Figure 2-13b, if the turn-off delay time of the switching device is greater than the turn-on delay under all possible operating conditions. Thus, the delay time of this stage can be reduced to zero [63]. None commutation failure occurs in the three-step current commutation at the 2nd stage, if the turn-off delay of the Z_{Aa1} IGBT (outgoing device) is larger than the turn-on delay of the incoming IGBT (Z_{Ba1}). Likewise, the corresponding two-step current commutation strategy would reduce to a single-step current commutation, as shown in Figure 2-13c, if the same statement as in the three-step strategy is followed. In this case, the delay time of the current commutation is obviously at the minimum.

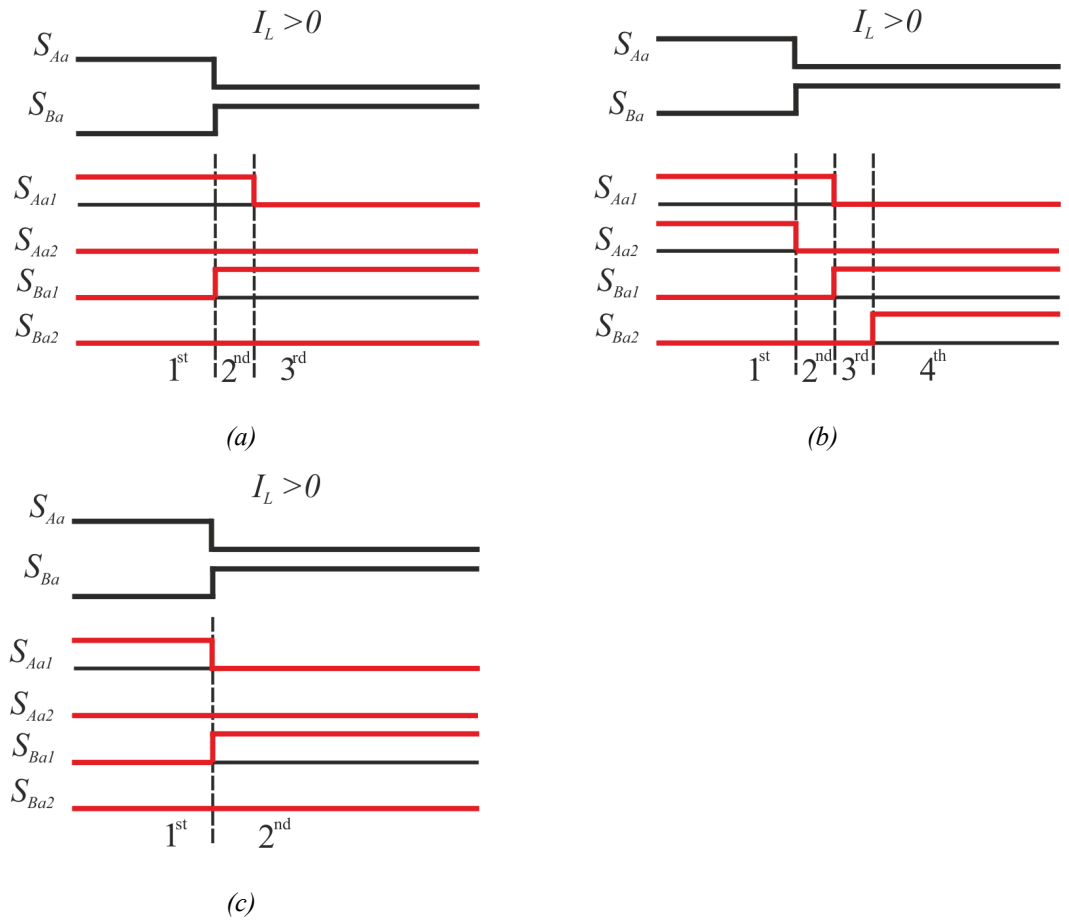


Figure 2-13 Timing diagram of several current commutation methods when the direction of load current is positive. a) Two-step; b) Three-step and c) Single-step

2.2.2.3. Current Sign Detection

All the current commutation techniques discussed until now rely on the knowledge of the output phase current direction. Thus, for a current commutation strategy to be fully reliable in practical applications, accurate current direction information must be obtained. Sometimes, this can be uncertain, especially at low current levels in high power drives where traditional current sensors such as Hall-effect probes can produce uncertain results. In addition, we must keep in mind that a commutation can be demanded when a BDS is conducting and at the same time that the output current changes direction. In order to avoid these possible hazard conditions, a method based on threshold level current has been used [64]. This method is described in Figure 2-14 for a two-step strategy. If the load current is within the threshold level and both IGBTs within a BDS are turned on, the commutation is not allowed to take place. The normal operation continues when the load current leaves the threshold level. This commutation process would not also be suitable if the load current was within the threshold level during a relatively long time. Therefore, this method can affect seriously the output

waveform quality. A solution for this problem has been described in [65]. It consists in using the voltage across the BDS devices to determine the current direction as depicted in Figure 2-15. This method allows very accurate current direction detection with no external sensors.

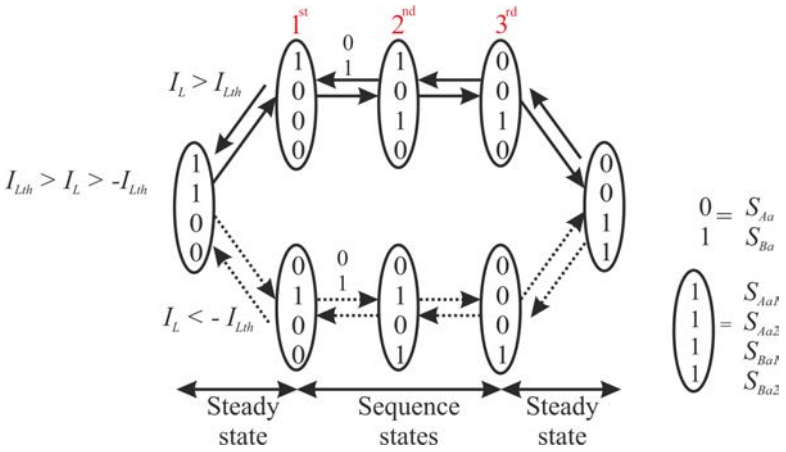
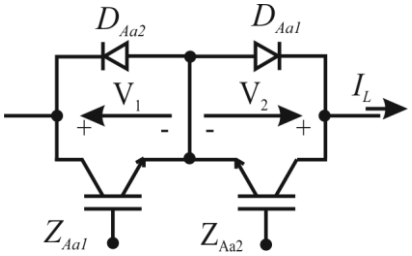


Figure 2-14 Two-step commutation using current threshold detection. I_{Lth} is the current threshold level



	V_1 (V)	V_2(V)	Z_{Aa1}-D_{Aa1}	Z_{Aa2} - D_{Aa2}
$I_L > 0$	2.5V	-1.2V	*on*	*off*
$I_L < 0$	-1.2V	2.5V	*off*	*on*

Figure 2-15 Current sense detection based on the voltage drop across the BDS emitter point

2.3. BDS Commutation Process Analysis

2.3.1. Introduction

The commutation process depends basically on the MC modulation, on the dynamic parameters of the power semiconductors of the BDS (i.e. switching and blocking devices), and on the parasitic inductances that are introduced in the power module layout. The main elements to be considered when analysing the commutation process from the device point of view are:

- Gate drive design: gate drive voltage (V_{GG}) and series gate resistance (R_G) [66].
- Diode recovery effects: the reverse recovery characteristics are mainly determined by *di/dt*, reverse-recovery time (t_{rr}), maximum reverse current (I_{rr}), reverse-recovery charge (Q_{rr}) [67]. It is clear that the performance of the conventional Si

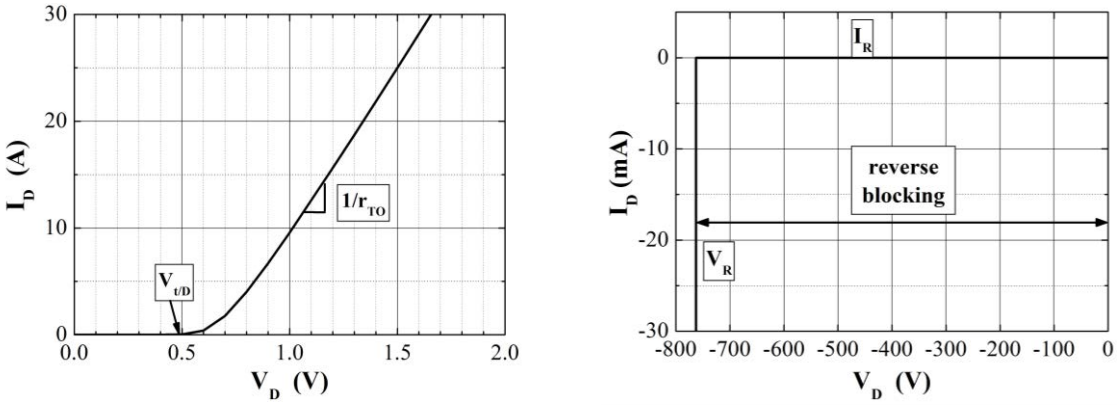
diode will differ from the SiC-based device due to the benefits of being a wide bandgap semiconductor.

- IGBT's current tail: minority carrier stored charges in the epitaxi -n region (Figure 2-5a) recombine at a rate determined by the carrier lifetime. The input parasitic capacitances of the IGBT determine also the final value for the *di/dt* and switching times.
- Parasitic inductances associated with the layout of the BDS package.

The power devices behaviour of a BDS plays an important role in the commutation phenomena. In order to understand this role, a SPICE simulation of typical real power devices within a common emitter (CE) BDS has been firstly performed in order to introduce the static and dynamic features of these power devices. The power diode model is based on the DSEI30-06A diode from IXYS [35] and the IGBT model is directly the SPICE model of the IXGH28N60B device provided by IXYS [35], too. Secondly, the SPICE simulation of the two-phase to single-phase MC (Figure 2-11) based on real components has allowed understanding how works the commutation process between BDSs. The concepts learnt from this study will be analogous for the CC BDS and BDS with RB-IGBTs (hereinafter RB BDS).

2.3.1.1. Diode and IGBT Static Characteristics

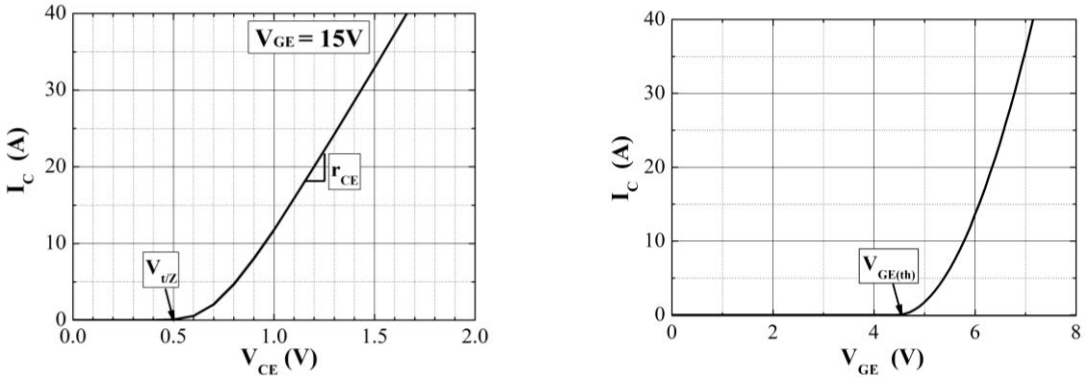
Figure 2-16 shows I-V characteristics when the diode is forward and reverse biased. $V_{t/D}$ and r_{TO} are the on-state voltage and resistance, respectively. The V_R and I_R are reverse voltage and current, respectively. The diode begins to conduct $V_D > V_{t/D}$. The current rises rapidly due to the large slope $1/r_{TO}$. Figure 2-16b displays the reverse blocking operation of the diode.



(a) *(b)*

Figure 2-16 Diode I-V characteristics: a) forward biased, b) reverse biased

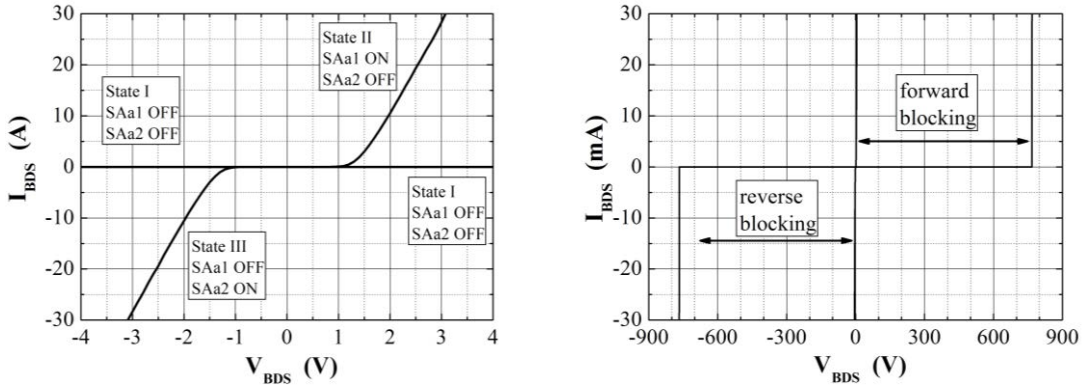
The IGBT current-voltage characteristics are depicted in Figure 2-17. $v_{t/Z}$ (or $V_{CE(ON)}$ as generally appeared in datasheets) and r_{CE} are the Collector-to-Emitter saturation voltage (i.e. on-state voltage) and on-state resistance, respectively. $V_{GE(th)}$ is the gate threshold voltage. When $V_{GE} > V_{GE(th)}$, the IGBT is conducting current.



(a) *(b)*

Figure 2-17 IGBT I-V characteristic: a) output characteristic, b) transfer characteristic

The static behaviour of a CE BDS is depicted in Figure 2-18. The four-quadrant operation of the BDS can be appreciated in Figure 2-18a. The forward voltage VF BDS is essentially the vt/Z of the IGBT plus the vt/D of the diode. The blocking capability for positive and negative polarities of the AC switch is probed and displayed in Figure 2-18b.



(a) *(b)*

Figure 2-18 BDS I-V characteristics: a) forward and reverse conducting, b) forward and reverse blocking

Table 2-1 shows the different BDS operation states. State IV is denoted by the switch *on* of S_{Aa1} and S_{Aa2}.

State	S_{Aa1}	S_{Aa2}	Comment
I	0	0	BDS is switched OFF and able to block both polarities
II	1	0	BDs is conducting current towards the load
III	0	1	BDs is conducting current towards the input
IV	1	1	BDS is ready to conduct current in any direction

Table 2-1 Description of the BDS states

2.3.1.2. Diode and IGBT Dynamic Characteristics

In order to extract the switching characteristics of the CE BDS semiconductors, a typical test circuit based on a diode-clamped inductive load circuit in a buck converter configuration is used in the simulation. The current, voltage and energy dissipation waveforms of the diode during the on and off transition are depicted in Figure 2-19. At the turn-off the diode current reverses for a specific time called reverse-recovery time (t_{rr}), as indicated in Figure 2-19b, before falling to zero. The reverse-recovery current has its maximum reverse value I_{rr} when the diode becomes reverse biased. The decrease of the recovery current ($-di_R/dt$) versus time is of special importance, because influences the reverse recovery current, i.e. the faster $-di_R/dt$, the higher I_{rr} is exhibited by the diode. The diode reverse recovery energy losses, E_{rec}, can be defined as the area under the reverse power losses curve comprised from the 10% of V_D to the 10% of I_{rr} as the diode current is extinguished.

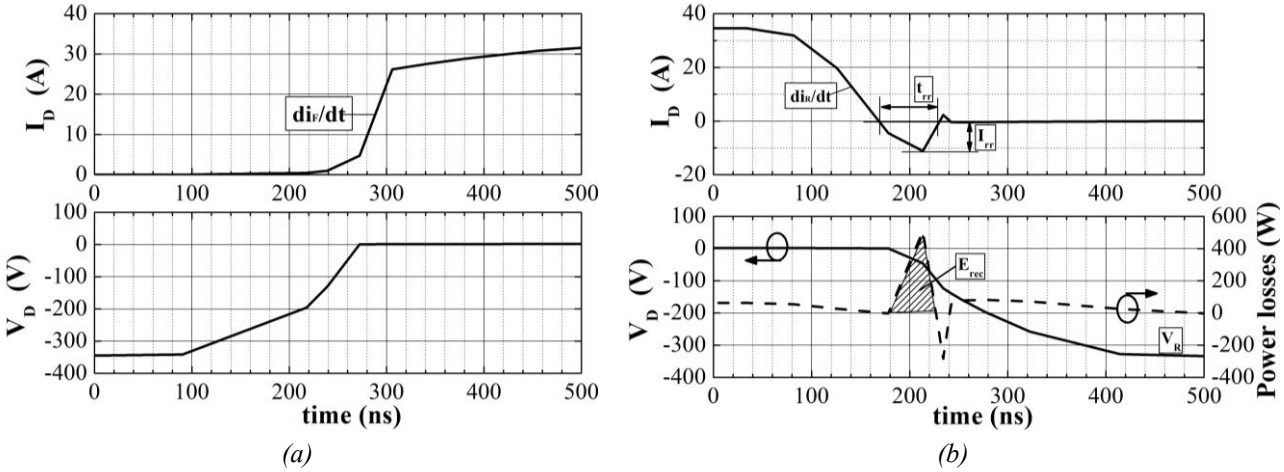


Figure 2-19 Switching voltage, current and power losses waveforms of diode. a) Turn-on, b) Turn-off and reverse recovery losses

The IGBT embedded in the test circuit shows the following current, voltage and energy dissipation waveforms. The switching *on* and *off* processes are not instantaneous, they are delayed by the charge and discharge of the parasitic input capacitances of the IGBT, respectively. Thus, the on transition, Figure 2-20a, presents a turn-on delay time, $t_{d(on)}$, which is defined as the elapsed time from 10% of V_{GE} (gate drive voltage) to 10% of I_C current. The V_{GE} voltage increases according to a time constant dependent on the input parasitic capacitances of the IGBT and the gate resistance associated with the driver circuit. On the other hand, I_C current exhibits a current peak during the rise time because of the reverse recovery current of the diode. The turn-on energy losses, E_{on}, can be defined as the area under the power losses curve comprised from the 10% of I_C to the 5% of V_{CE} as the IGBT is fully *on*.

The turn-off transition can be observed in Figure 2-20b. The turn-off procedure is delayed by the turn-off delay time, $t_{d(off)}$. It can be defined as the elapsed time between 90% of V_{GE} and 10% of $V_{CE.}$ The I_C current does not decreases rapidly to zero due to the stored charge in the n^- drift region of the IGBT, as shown in Figure 2-20b. This portion of the I_C current corresponds to the turn-off of the BJT section of the IGBT and is commonly known as current tail. This time is named as fall time (t_f) and is defined as the elapsed time between 90% and 5% of the I_C initial current value. The turn-off energy losses, E_{off}, can be defined as the area under the power losses curve comprised from the 10% of V_{CE} to the I_C of 5% as the current extinguishes.

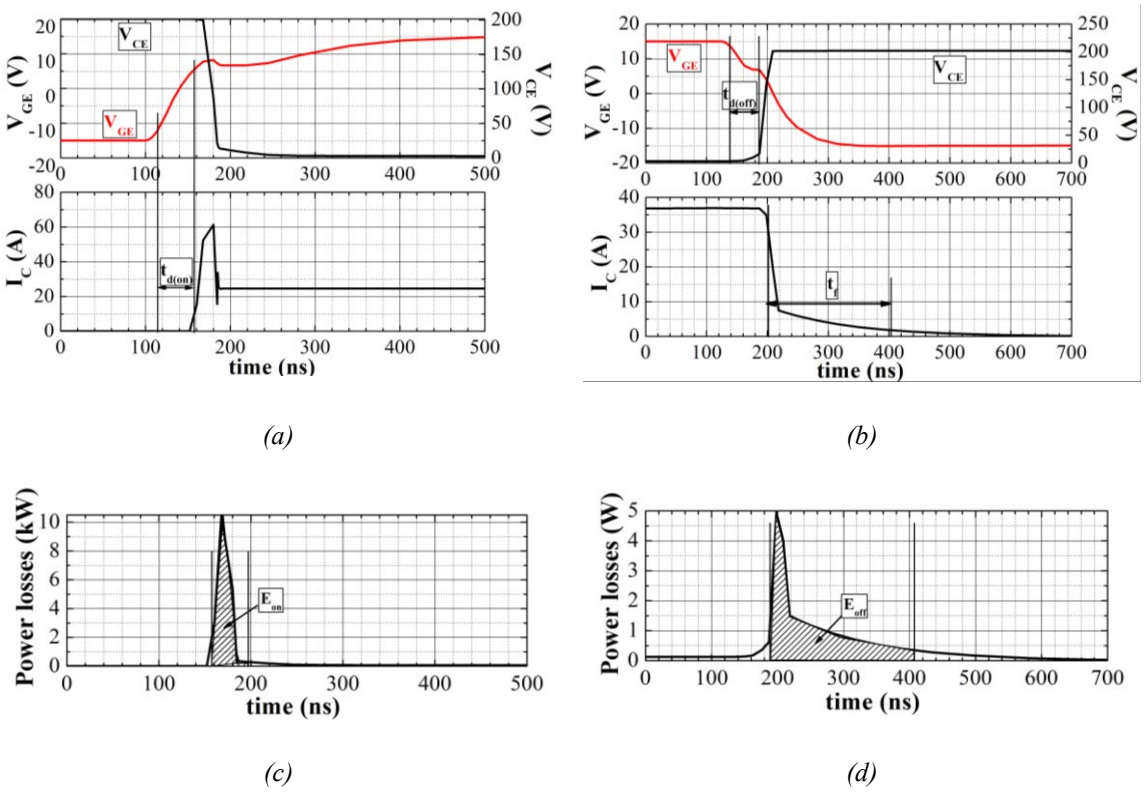


Figure 2-20 Switching IGBT waveforms: a) Turn-on, b) Turn-off, Energy losses c) Turn-on, d) Turn-off

2.3.2. Study of Commutation Processes Based on a Four-step Commutation Strategy

The schematic circuit of Figure 2-11 is simulated in order to study the commutation processes between conventional CE BDSs with an inductive load (2 mH and 5 Ω). All possible commutation types in a complete three-phase to three-phase MC occur in a two-phase to single-phase MC [68]. In order to provide a safe commutation between BDSs, the current commutation strategy based on the four-step strategy has been implemented. Depending on the direction of the current and the polarity of the voltage drop in a BDS, the commutation processes can be characterised by a soft or natural switching when the associated power losses are low, otherwise by a hard or forced switching when power losses involved in the commutation are high.

The simulation conditions for the study of commutations represent the truly conditions of the relative voltages of V_A and V_B in a whole three-phase to three-phase MC. The gate drive for each controlled switch was simplified to a series gate resistance, R_G, with a value of 20 Ω and a control voltage source with defined transition times. The maximum and minimum amplitude of such control voltage source are 15V (V_{GG}^+) and -15 (V_{GG}^-), respectively. A delay time of 200 ns is applied to each gate control signal of

the BDSs involved in the switching in order to achieve a reliable and safe commutation following the four-step strategy, i.e. 1st step, 2nd step, 3rd step and 4th step corresponds to a delay of 0 ns, 200 ns, 400 ns and 600 ns, respectively. The stated simulation conditions will be applied to the entire study of the commutation processes.

2.3.2.1. Type I Commutation (BDS-Aa to BDS-Ba)

Type I commutation is denoted by the following simulation conditions: V_A-V_B > 0 (V_A= 300 V, V_B= 52 V), I_L > 0. The voltage and current waveforms of the devices involved in the commutation process, as well as their associated power losses are depicted in Figure 2-21. Figure 2-22 shows the current path of different intervals of time during type I commutation process. A full line indicates full current load. Otherwise, it is indicated as a dash line. The IGBT gate is also highlighted when it is switched on.
The time instants t_0, t_1, t_2; t_3 and t_4 define the time intervals of this type of commutation process. Before commutation the load current flows through IGBT Z_{Aa1} and diode D_{Aa2}.

- Interval t_0-t_1: Z_{Aa1} is on and conducting. Commutation occurs at the instant when Z_{Aa2} is gated off.
- Interval t_1-t_2: Z_{Ba1} is gated on, the current commutation to *BDS-Ba* is being prepared, but any current flows still through *BDS-Ba* since $V_A > V_B$ and then D_{Ba2} is reverse biased.
- Interval t_2-t_3: IGBT *ZAa1* receives the logic control signal to switch-off. Z_{Aa1} undergoes a hard turn-off, because Z_{Aa1} is standing the high input phase voltage while the full load current begins to decrease. The commutation to the incoming device, Z_{Ba1}, is beginning and carrying a small portion of I_L. Z_{Ba1} undergoes a soft turn-on, because the current begins in 0 A and the switch voltage rises from a low voltage value to the forward voltage drop.
- Interval t_3- t_4: Z_{Ba2} is gated on in order to accommodate a possible change of the direction of I_L. The current commutation is almost completed. The current tail of Z_{Aa1} is extinguishing.
- After t_4: end of the commutation procedure. *BDS-Ba* carries the entire load current (I_L).

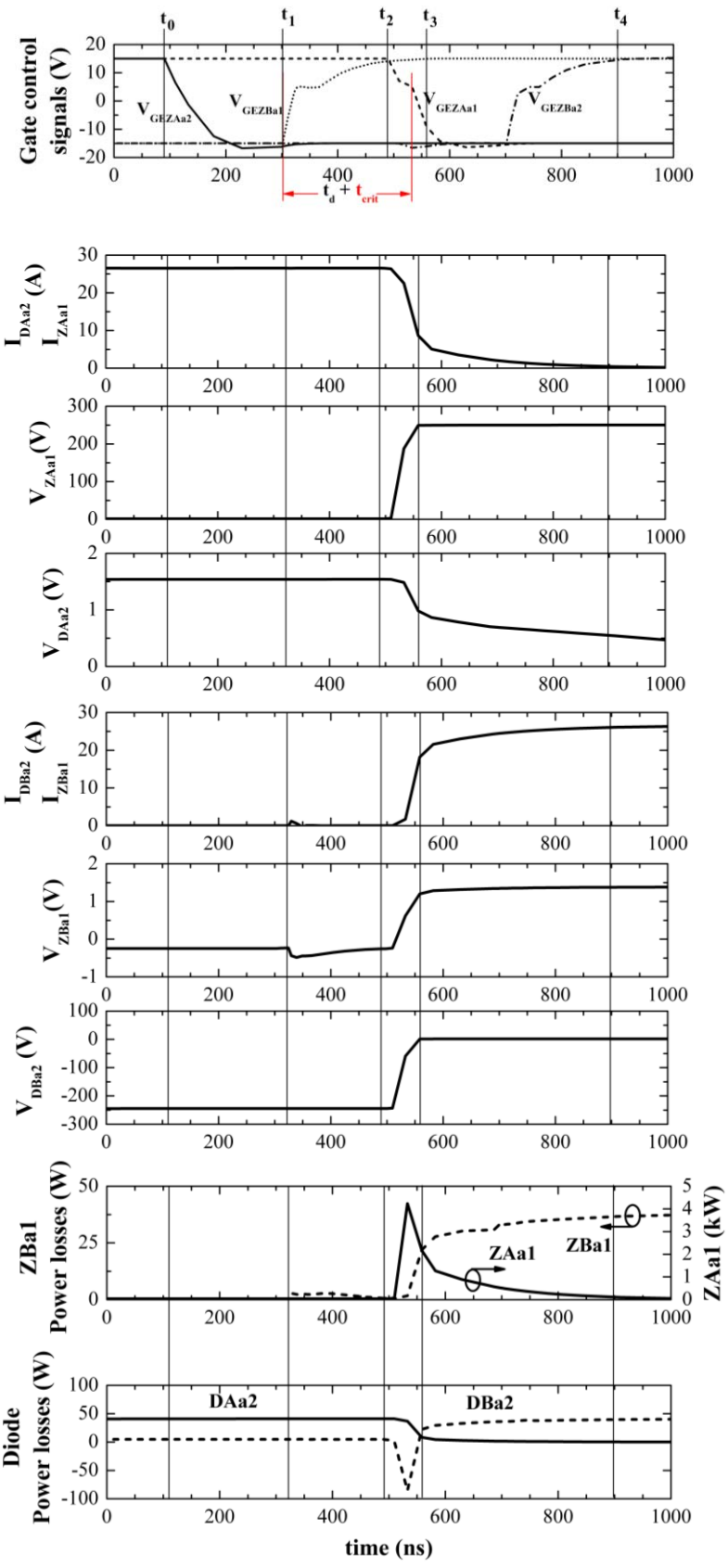


Figure 2-21 Device waveforms of type I commutation process

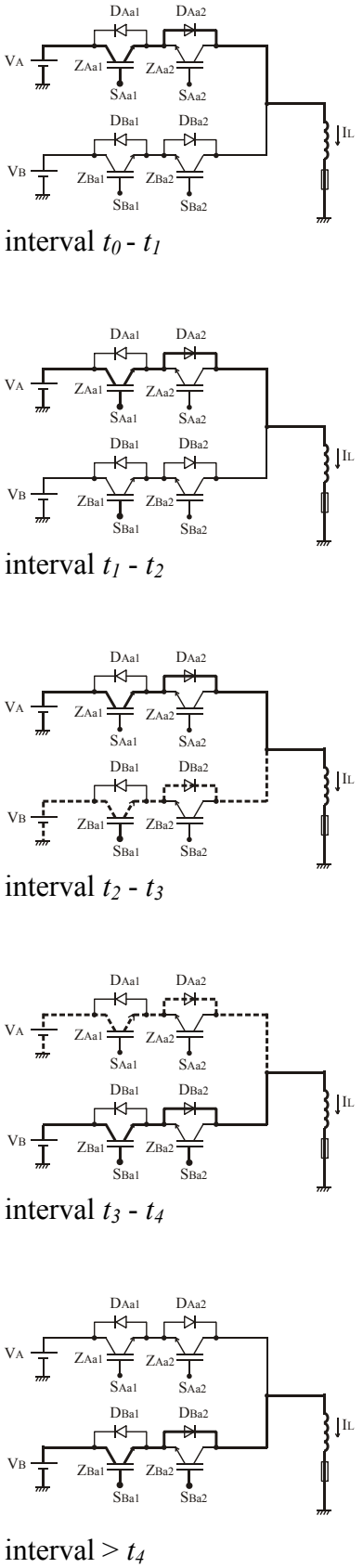


Figure 2-22 Type I current path

For any type of commutation process a critical delay time interval, t_{crit}, can be identified e. g. as shown in Figure 2-21. It can be defined as the time required for the incoming device to turn on before the outcoming device is turned off. The critical delay time interval is:

- related to the instant when the current commutation occurs.
- dependent on the switching characteristics of the power devices (i.e. $t_{d(off)}$, $t_{d(on)}$, t_{rr}) involved in the commutation.
- independent of the current commutation strategy.

The t_{crit} for type I commutation ($t_{crit\text{-}I}$) can be deduced from Figure 2-21. $t_{crit\text{-}I}$ can be defined as the elapse time of V_{GE} of Z_{Ba1} (incoming device) to reach $V_{GE(th)}$ value before Z_{Aa1} (outcoming device) is opened. $t_{crit\text{-}I}$ can be estimated as:

$$V_{GE}(t) = V_{GG}^{+} + \left(V_{GG}^{-} - V_{GG}^{+}\right) e^{-t/R_G C_{ies}} \tag{2.1}$$

$$t_{VGE(th)} = C_{ies} R_G \, ln\left(\frac{V_{GG}^{-} - V_{GG}^{+}}{V_{GE(th)} - V_{GG}^{+}}\right) \tag{2.2}$$

$$t_{crit\text{-}I} = (t_{d(on)} + t_{VGE(th)}) \text{ incoming IGBT} + t_{d(off)} \text{ outcoming IGBT} \tag{2.3}$$

Equation (2.1) describes the general behaviour of V_{GE} voltage. Equation (2.2) results from imposing V_{GE} equal to $V_{GE(th)}$ and resolving the time. Thus, $t_{VGE(th)}$ indicates the time needed for V_{GE} voltage to rise from V_{GG}^{-} till $V_{GE(th)}$ value. As denoted in (2.3), $t_{crit\text{-}I}$ is determined by the characteristics of the switching devices of the BDS. These parameters can be easily found in the datasheet under specific test conditions. Such conditions cannot be the corresponding conditions of the MC operation so that $t_{crit\text{-}I}$ must be carefully selected. $t_{crit\text{-}I}$ must be respected, i.e. the delay time t_d of the commutation strategy should be greater than $t_{crit\text{-}I}$, in order to assure a safe current commutation between BDSs. Otherwise, i.e. t_d is smaller than $t_{crit\text{-}I}$, a failure can happen in the switching process as shown in Figure 2-23. Accordingly, the current path is interrupted and overvoltages can appear in the active IGBTs since the inductive load is opened. As a result, such devices could operate out of their safe operating area (SOA) leading to an irreversible damage. On the other hand, a longer t_d implies a worst quality

of the output phase currents of the MC since their harmonics are of higher amplitude. A trade-off is necessary in order to choose the suitable t_d.

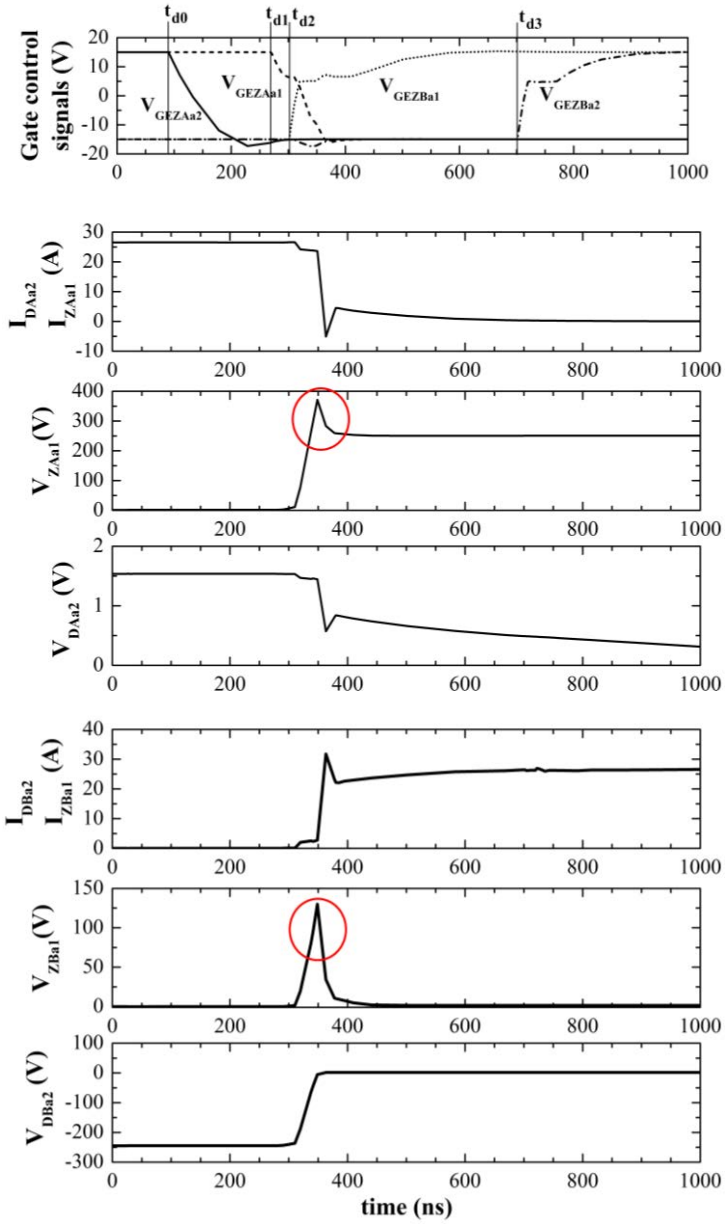


Figure 2-23 Device waveforms under a failure in the Type I commutation. Time instants t_{d0}, t_{d1}, t_{d2}; t_{d3} and t_{d4} correspond to the activation of the respective control gate signals.

2.3.2.2. Type II commutation (BDS-Aa to BDS-Ba)

Type II commutation is denoted by the following simulation conditions: V_A-V_B < 0 (V_A= 100 V, V_B= 267 V), I_L > 0. The voltage and current waveforms of the devices involved in the commutation process, as well as their associated power losses are depicted in Figure 2-24. On the other hand, Figure 2-25 shows the current path of

different intervals of time during type II commutation process. The time instants t_0, t_1, t_2; t_3 and t_4 define the time intervals of this type of commutation procedure. Prior to commutation, the load current flows through IGBT Z_{Aa1} and diode D_{Aa2}.

- Interval t_0 - t_1: *ZAa2* is gated off. The full load current flows still through *BDS-Aa*. ZBa1 is standing the difference voltage between the input V_B voltage and the output phase one.
- Interval t_1 - t_2: IGBT *ZBa1* receives the logic control signal to switch-on. The commutation occurs at the instant when V_{GE} Z_{Ba1} is larger than $V_{GE(th)}$ voltage. Thus, Z_{Ba1} is forced to conduct and hence a hard turn-on commutation is undergone. The hard turn-on is characterised by an almost total voltage switch drop over the device (Z_{Ba1}) which is carrying the current in this present commutation instant. At the same time, D_{Aa2} begins to recover to V_R because it is reverse biased ($V_A < V_B$). The I_{rr} current of D_{Aa2} is added to I_{ZBA1} resulting in a *BDS-Ba* current overshoot.
- Interval t_2 - t_3: D_{Aa2} is standing the negative voltage of *BDS-Aa* ($V_A < V_B$). In fact, this is the mission of the diode in series with IGBT; it provides the reverse blocking capability of the BDS. The current commutation is completed. *BDS-Ba* carries the entire load current.
- Interval t_3 - t_4: Z_{Aa1} is gated off and undergoes a soft turn-off since the commutation occurs at low voltage and current.
- After t_4: Z_{Ba2} is gated on in order to accommodate a possible change of the direction of I_L.

A critical delay time interval, $t_{crit\text{-}II}$, can be also identified for type II commutation as shown in Figure 2-24. $t_{crit\text{-}II}$ can be defined as the time interval from Z_{Ba1} (incoming device) is conducting till Z_{Aa1} (outcoming device) is opened. It can be estimated as:

$$t_{crit\text{-}II} = t_{d(on)} \text{ incoming IGBT} + t_{rr} \text{ outcoming diode} + t_{d(off)} \text{ outcoming IGBT} \qquad (2.4)$$

As commented for $t_{crit\text{-}I}$, all parameters of (2.4) are described in the respective datasheets under specific test conditions. These conditions could not be the same as in the MC operation. A safe commutation is undertaken when t_d is larger than $t_{crit\text{-}II}$.

Otherwise, a failure can possibly occur in the process commutation as represented in Figure 2-26. Voltage and current spikes in the active devices appear since the inductive load is opened. It could happen that the devices operate out of their SOA so that they could probably suffer a destructive damage.

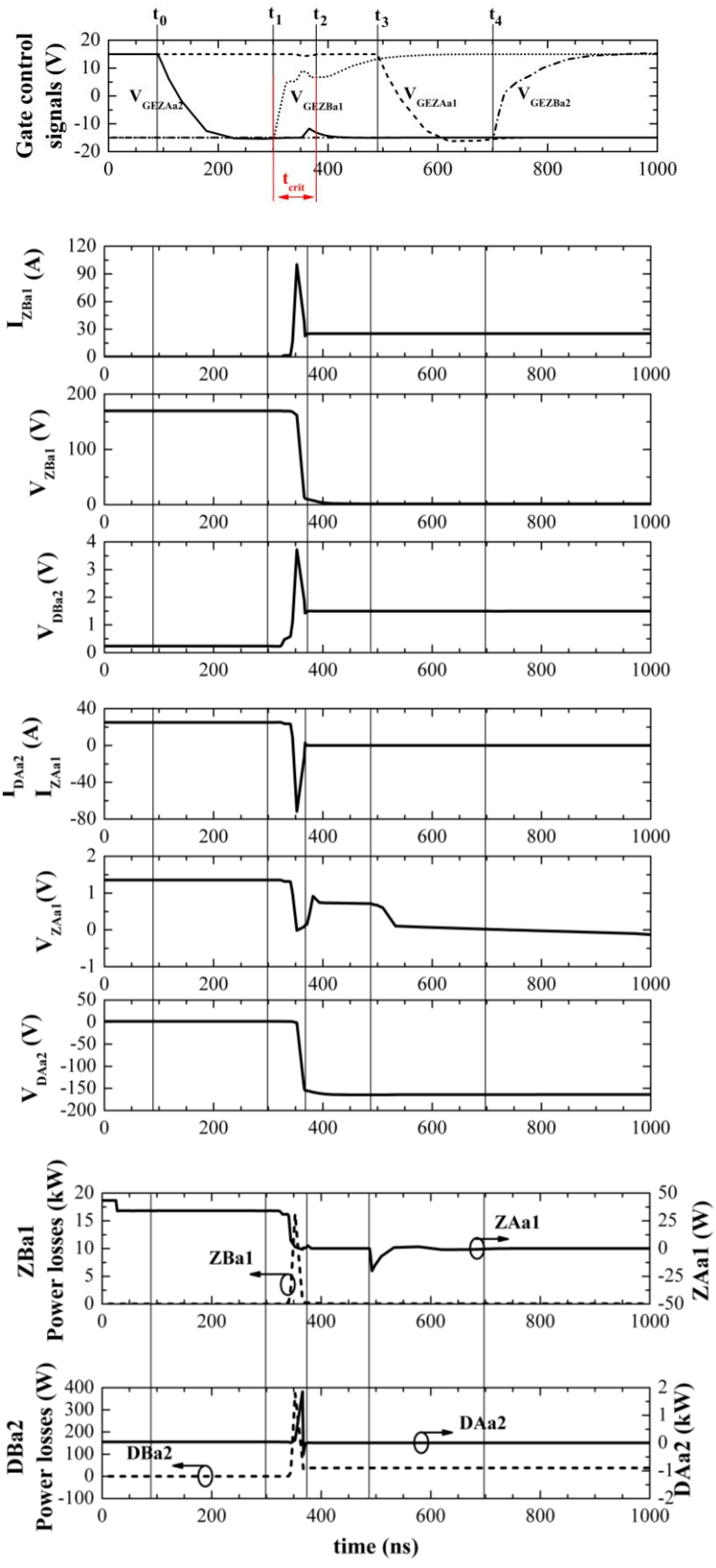
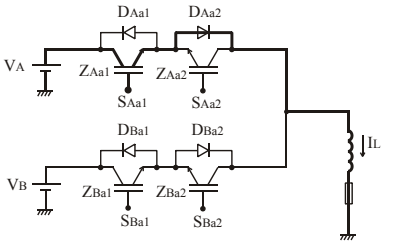
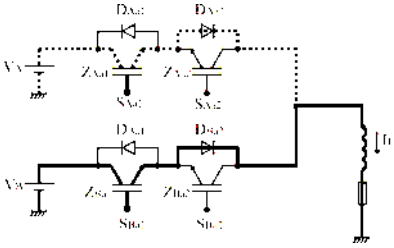


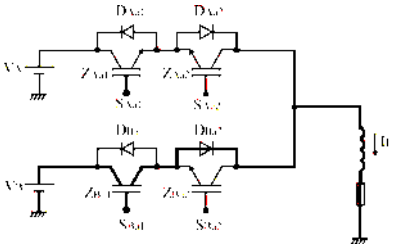
Figure 2-24 Device waveforms of type II commutation process



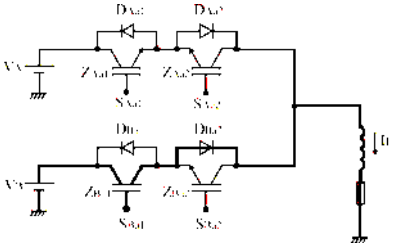
interval t_0 - t_1



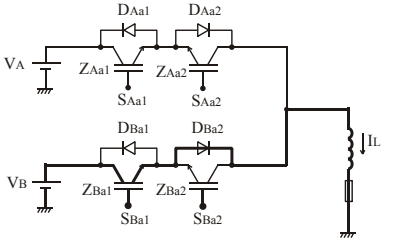
interval t_1 - t_2



interval t_2 - t_3



interval t_3 - t_4



interval > t_4

Figure 2-25 Type II current path

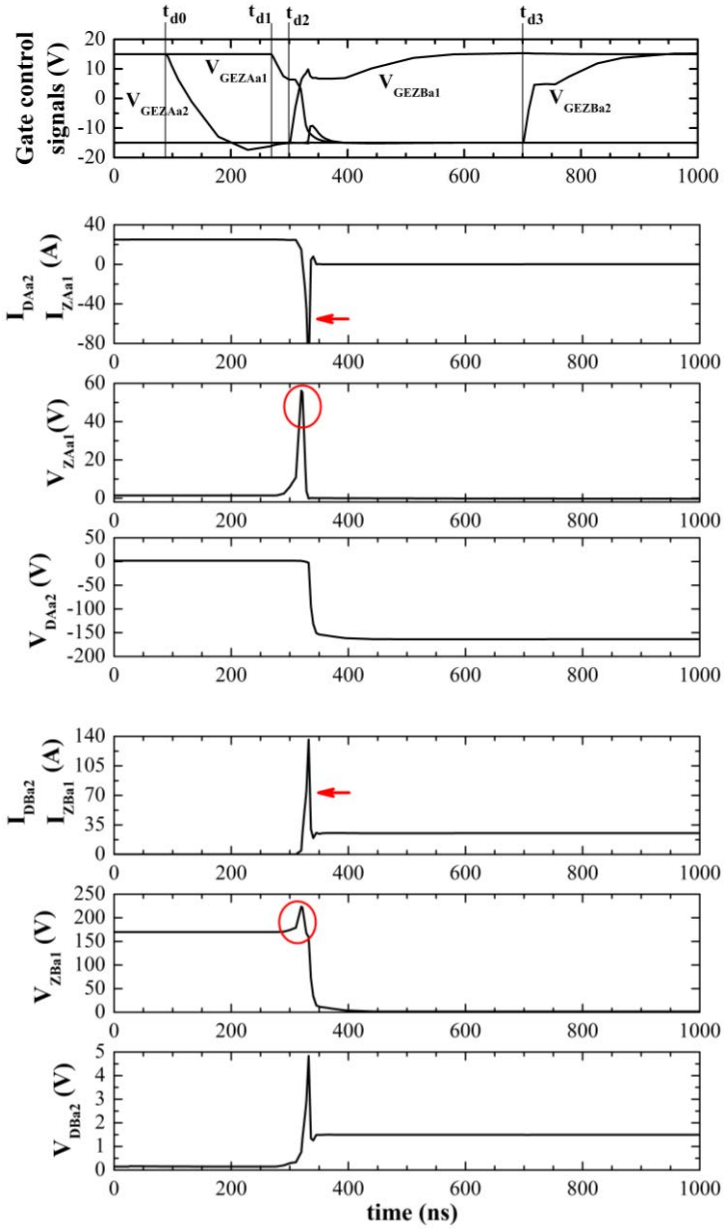


Figure 2-26 Device waveforms under a failure in the Type II commutation. Time instants t_{d0}, t_{d1}, t_{d2}; t_{d3} and t_{d4} correspond to the activation of the respective control gate signals.

2.3.2.3. Type III Commutation (BDS-Ba to BDS-Aa)

Type III commutation is denoted by the following simulation conditions: V_A-V_B > 0 (V_A= 300 V, V_B= 52 V), I_L > 0. The voltage and current waveforms of the devices involved in the commutation process, as well as their associated power losses are depicted in Figure 2-27. On the other hand, Figure 2-28 shows the current path of different intervals of time during type III commutation process. The time instants t_0, t_1, t_2; t_3 and t_4 define the time intervals of this type of commutation procedure. As it can be appreciated, type II (Figure 2-24) and type III (Figure 2-27) commutation processes are

analogous, but in opposite BDSs. Thus, a hard turn-on is involved in Z_{BA1} in type II, but in Z_{Aa1} in type III. Similarly, D_{Aa2} is reverse recovery in type II, but in type III is diode D_{Ba2}. A soft turn-off is undergone in Z_{Aa1} in type II, but in Z_{Ba1} in type III.

A delay critical time interval can also be identified and estimated analogous to type II commutation.

2.3.2.4. Type IV Commutation (BDS-Ba to BDS-Aa)

Type IV commutation is denoted by the following simulation conditions: V_A-V_B < 0 (V_A= 100 V, V_B= 267 V), I_L > 0. The voltage and current waveforms of the devices involved in the commutation process, as well as their associated power losses are depicted in Figure 2-29. On the other hand, Figure 2-30 shows the current path of different intervals of time during type IV commutation process. The time instants t_0, t_1, t_2; t_3 and t_4 define the time intervals of this type of commutation procedure. It can be derived from Figure 2-21 (type II commutation) and Figure 2-29 (type IV commutation) both commutation processes are analogous, but they happen in opposite BDSs. Thus, a hard turn-off is involved in Z_{Aa1} in type I, while it happens in Z_{Ba1} in type IV. A soft turn-on is undergone in Z_{Ba1} in type I, but in Z_{Aa1} in type IV.

A delay critical time interval can also be identified and estimated analogous to type I commutation.

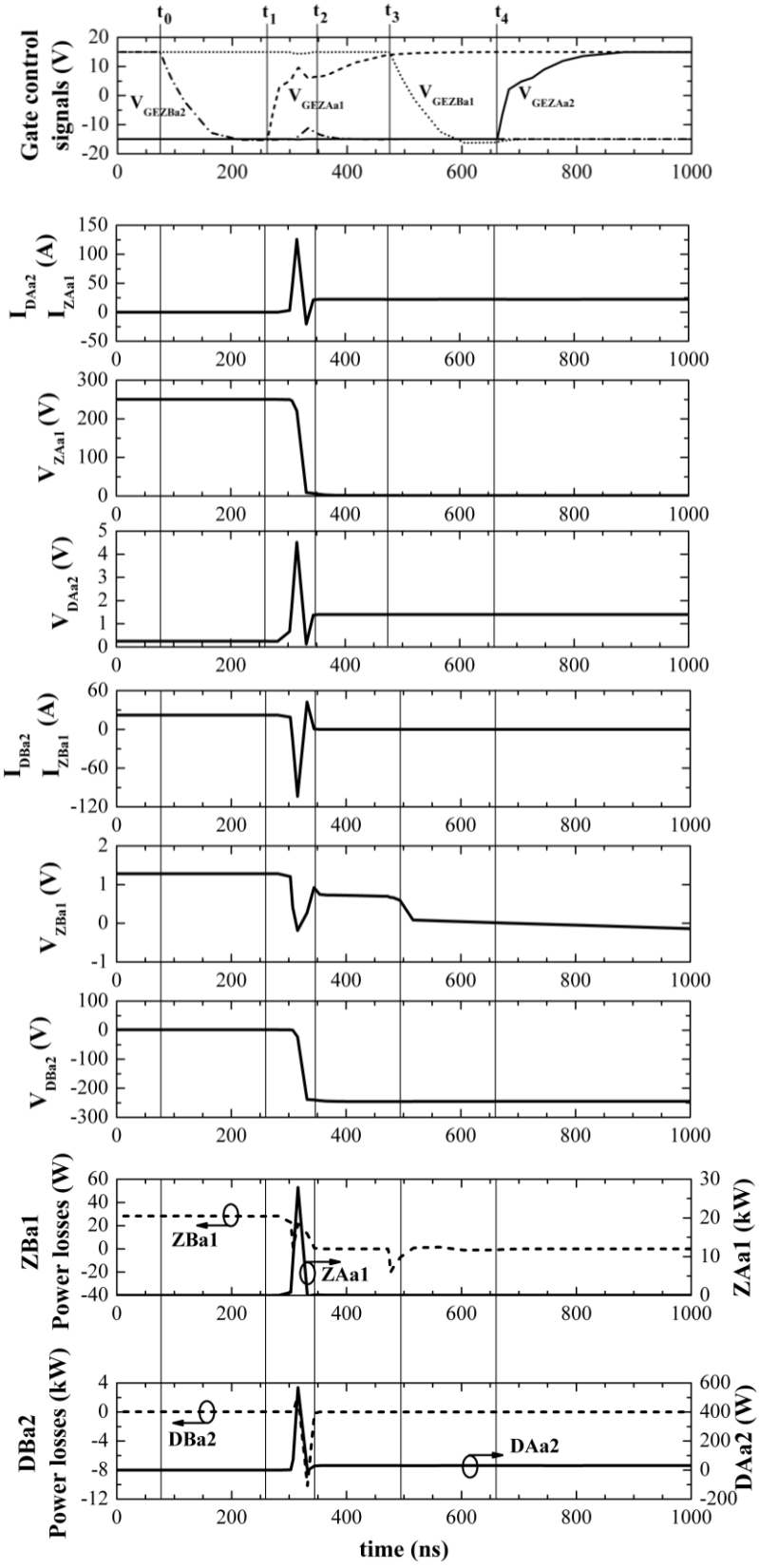
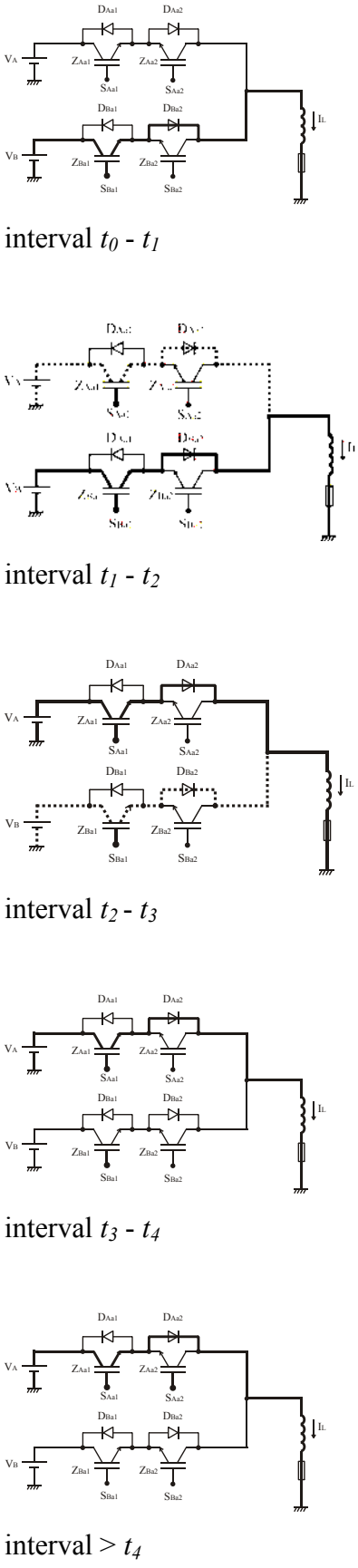


Figure 2-27 Device waveforms of type III commutation process



interval t_0 - t_1

interval t_1 - t_2

interval t_2 - t_3

interval t_3 - t_4

interval > t_4

Figure 2-28 Type III current path

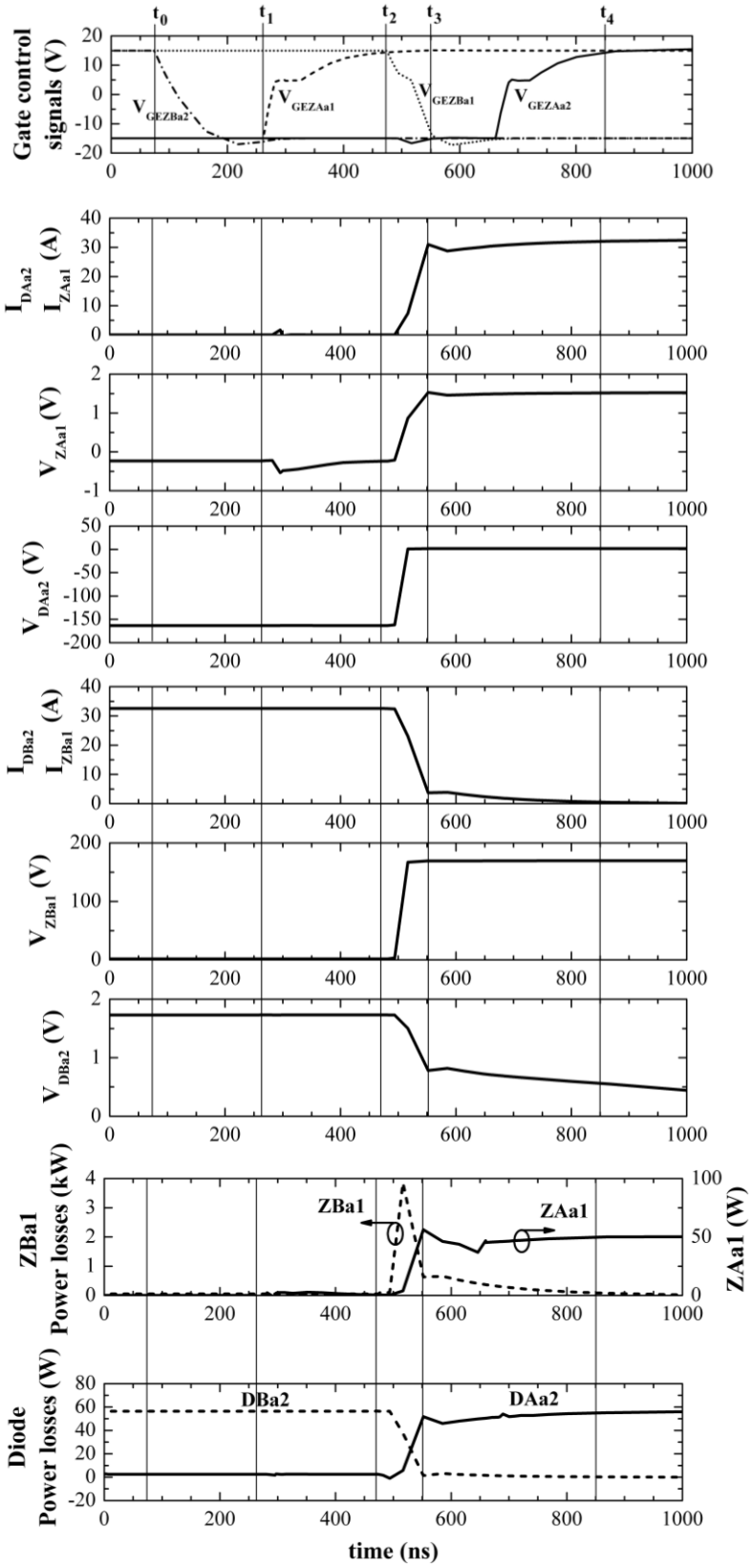


Figure 2-29 Device waveforms of type IV commutation process

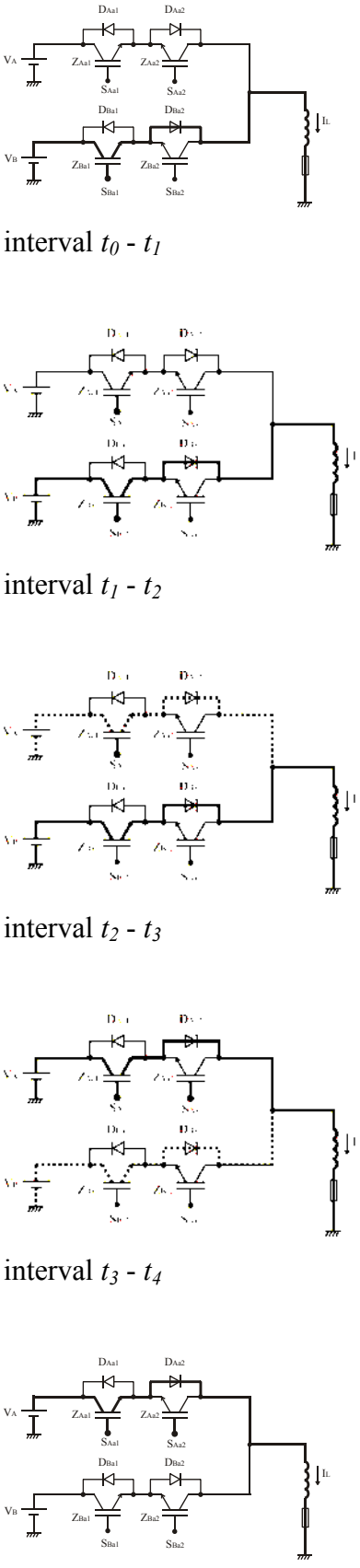


Figure 2-30 Type IV current path

Table 2-2 summarises all the possible commutation scenarios according to the relative voltages of V_A and V_B, and the direction of I_L.

	Commutation	V_A-V_B	I_L	***BDS-Aa***	***BDS-Ba***
Type I	*BDS-Aa → BDS-Ba*	> 0	> 0	$H_{OFF}\ Z_{Aa1}$	$S_{ON}\ Z_{Ba1}$
	BDS-Aa→BDS-Ba	> 0	< 0	$H_{OFF}\ Z_{Aa2}$	$S_{ON}\ Z_{Ba2}$
Type II	*BDS-Aa→BDS-Ba*	< 0	> 0	$S_{OFF}\ Z_{Aa1}$ $H_{OFF}\ D_{Aa2}$	$H_{ON}\ Z_{Ba1}$
	BDS-Aa→BDS-Ba	< 0	< 0	$S_{OFF}\ Z_{Aa2}$ $H_{OFF}\ D_{Aa1}$	$H_{ON}\ Z_{Ba2}$
Type III	*BDS-Ba→BDS-Aa*	> 0	> 0	$H_{ON}\ Z_{Aa1}$	$S_{OFF}\ Z_{Ba1}$ $H_{OFF}\ D_{Ba2}$
	BDS-Ba→BDS-Aa	> 0	< 0	$H_{ON}\ Z_{Aa2}$	$S_{OFF}\ Z_{Ba2}$ $H_{OFF}\ D_{Ba1}$
Type IV	*BDS-Ba→BDS-Aa*	< 0	> 0	$S_{ON}\ Z_{Aa1}$	$H_{OFF}\ Z_{Ba1}$
	BDS-Ba→BDS-Aa	< 0	< 0	$S_{ON}\ Z_{Aa2}$	$H_{OFF}\ Z_{Ba2}$

Table 2-2 Types of commutation processes: S_{OFF}: soft turn-off, S_{ON}: soft turn-on, H_{OFF}: hard turn-off, H_{ON}: hard turn-on, H_{OFF}: diode turn-off reverse recovery

As it can be inferred from Table 2-2, four different types of commutations are identified. In addition, type I and IV commutations as well as type II and III show the same switching characteristics, but in opposite BDSs. Likewise, the commutations for case $I_L < 0$ result in the same types of commutations for $I_L > 0$, but with Z_{Aa2} and Z_{Ba2} as active devices instead of Z_{Aa1} and Z_{Ba1}. For all types of commutation, half of the switching actions are lossless, since there is no conduction current neither when $I_L > 0$ nor when $I_L < 0$. Another important conclusion derived from this study is the effect of the BDS power devices in the commutation process. The total commutation procedure time for type I and IV (approximately 900 ns) is larger than the type II and III (approximately 535 ns). This fact is essentially due to the commutation type, which is characterised by a hard turn-off in case of type I, and in a second order because of the current tail of the IGBT. This issue results in a critical problem, because the larger the total commutation time, the worst quality are the output voltages of the MC [69]. Hence, the study of the influence of different BDS realisations, i.e. different commercial families of IGBTs and FREDs, RB-IGBTs as well as SiC realisations, will be a key

point to understand better the commutation process. This task will be addressed in chapter 3. The result of this study will allow the MC designer to adjust the delay times associated to the commutation strategy in order to optimise the MC operation taking into account the delay critical time interval.

2.4. Summary

The main target of this chapter is the analysis of the commutation process between BDSs. First, a detailed description of different BDS topologies has been introduced. New power devices are emerging due to the better performance of novel materials such as SiC and GaN so that better performances in the BDS will be achieved in a short time.

Second, it has been adopted a reduced MC, i.e. two-phase to one-phase MC, built with two CE BDSs in order to understand and study the commutation phenomena by means of simulation. Thus, four types of commutations have been identified, I, II, II and IV according to the relative voltages of V_A and V_B, and the direction of I_L. However, they can be reduced to two types since the same kind of commutation occurs in the opposite device within the BDS when $I_L < 0$ or in the opposite BDS when is *on* / *off*:

- Type I and IV are characterised by a H_{OFF} / S_{ON} (hard turn-off / soft turn-on) of the outcoming and incoming device, respectively.
- Type II and III are characterised by a S_{OFF} / H_{ON} (soft turn-off / hard turn-on) of the outcoming and incoming device, respectively.

The hard switching implies normally high power dissipation. On the other hand, a low or moderate power loss will be exhibited in case of a soft commutation. All types of commutations have been fully described in the chapter. An important feature of commutation phenomena is the critical delay time interval, t_{crit}. It is generally described as the time required for the incoming device to conduct current before the outcoming device is turned off. This time needs to be respected (i.e. $t_d > t_{crit}$) in order to succeed in the commutation process.

The energy losses, especially, related to the hard or forced commutations are also an important factor to be considered in order to assure the safe operation of the MC power devices. The influence of different BDS realisations and their associated power losses are aspects which will be studied in detail in chapter 3.

3. Characterisation of BDS Devices

This chapter presents the static and dynamic characterisation of the power semiconductor devices within a BDS. The attention is focused on the methodology for performing the dynamic characterisation and experimental evaluation of the switching losses (hard and soft types) of different BDS implementations in true Matrix Converter operation conditions. The influence of various power semiconductor devices within the BDS on the commutation process can be also analysed thanks to such characterisation. Therefore, a switching test circuit based on a two-phase to one-phase MC is designed and fabricated for this purpose. Several BDS circuits (i.e. CE, CC, RB-IGBTs and power integrated modules) can be tested due to the flexibility and modularity of the test circuit. The overall structure of the switching test circuit is introduced. The design and the functionality of its power stage circuit, the BDS commutation cells, the control circuit and the measurement probes are described in detail. The test of different BDS implementations is performed and discussed. This characterisation will also allow modelling the static and dynamic behaviour of the devices. In addition, these models will be used to derive the conduction and the switching losses associated with these power devices.

3.1. BDS Static Characterisation

3.1.1. Static Device Measurement

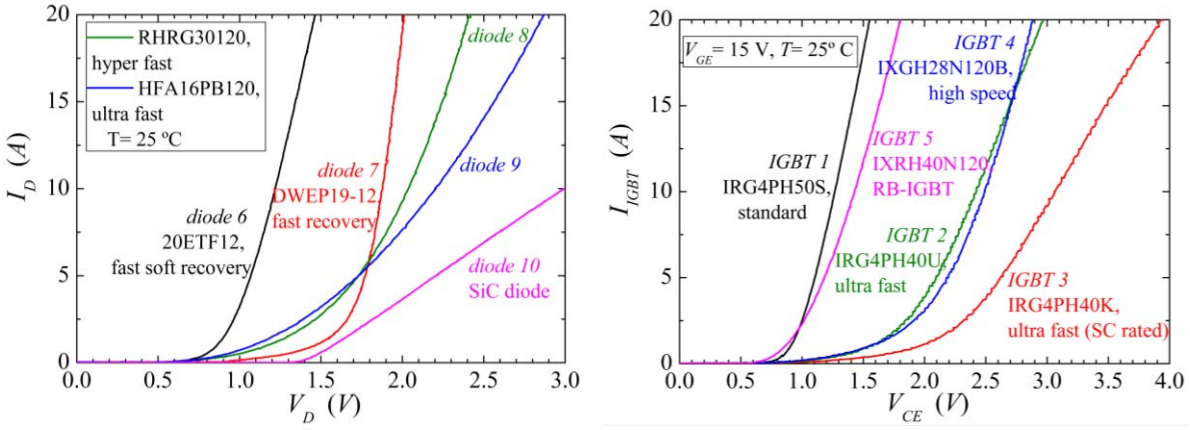
Table 3-1 shows the main power semiconductors characteristics, employed to construct the discrete BDSs under study. For instance, the *BDS 1-6* means the combination of IGBT number *1* with diode number *6*. Different commercial IGBTs and diodes are selected according to their switching speed, forward voltage drop and recovery behaviour. All the selected devices are packaged in a TO-247 case. A blocking voltage capability of 1200 V is required to implement a three-phase to three-phase MC with a nominal input voltage of 230 V (rms).

The I-V measurements of these discrete power devices as well as the BDSs built from theses semiconductors (Table 3-1) are carried out by means of a curve tracer (TEK371 [70]) at room temperature as illustrated in Figure 3-1. It can be inferred from Figure 3-1a that the faster recovery behaviour has the diode, the larger forward voltage drop. Likewise, Figure 3-1b shows how the fast and very fast IGBTs exhibit a large

voltage drops, whereas the standard IGBT and RB-IGBT have a lower voltage drop since their operating frequency is low (i.e. < 1 kHz). The standard IGBT is optimised for showing minimum saturation voltage at expenses of higher switching losses.

Switching device	**N°**	**$V_{CE(ON)}$ [V] @ I_{C25}=20 A**	**E_{on} - E_{off} [mJ]**	**Characte-ristics**	**Breakdown voltage [V]**
IGBT	1	1.3	1.8 – 19.6 @V_{GE}= 15 V, *Rg*=5 Ohms	IRG4PH50S Standard	1200
	2	2.5	1.31 – 1.12 @V_{GE}= 15 V, *Rg*=10 Ohms	IRG4PH40U Ultra fast	
	3	3.1	0.73 – 1.66 @V_{GE} = 15 V, *Rg*=10 Ohms	IRGPH40K Ultra fast (short-circuit rated)	
	4	2.7	0.3 - 2.2 @V_{GE} = 15 V, *Rg*= 5 Ohms	IXGH28N120B High speed	
RB-IGBT	5	1.8	3 - 0.7 @V_{GE} = ± 15 V, *Rg*= 15 Ohms	IXRH40N120 RB IGBT	
Device	**N°**	**V_F [V] @I_{F25}= 20 A**	**I_{rr} [A] - t_{rr} [ns]**	**Characte-ristics**	**Breakdown voltage [V]**
Si diode	6	1.31	6.1 - 95@ 1 A, dI_R/dt=100 A/µs	20ETF12 Fast soft recovery	1200 V
	7	2.5	7 - 40@1 A, dI_R/dt=100 A/µs	DWEP19-12 Fast recovery	
	8	2.5	- 65@1 A, dI_R/dt=100 A/µs	RHRG30120 Hyper fast	
	9	3.2	5.8 - 30@ 1 A, dI_R/dt=200 A/µs	HFA16PB120 Ultra fast soft recovery	
SiC schottky	10	2.9	-	CNM SiC ultra fast	

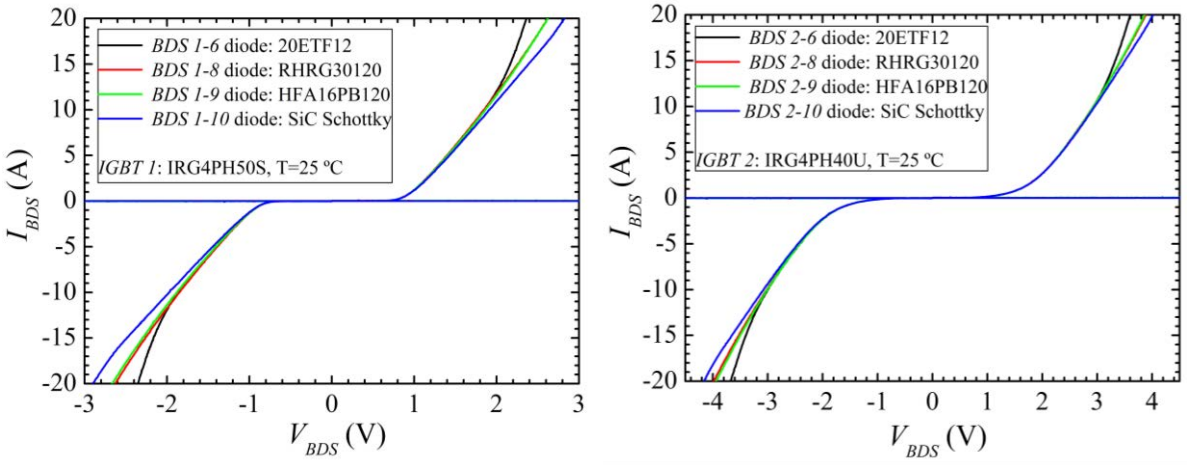
Table 3-1 Typical characteristics of the power devices employed to build the BDSs under test



(a) *(b)*

Figure 3-1 Static characteristics of the discrete devices a) diodes; b) IGBTs and RB-IGBTs

BDSs in a common emitter configuration are built with the discrete devices to study their static behaviour. The I/Vs of the combinations of one IGBT and different diodes, one diode and different IGBTs and a *RB BDS* (a BDS built with RB-IGBTs) are shown in Figure 3-2a, Figure 3-2b and Figure 3-3a, from Figure 3-3a to Figure 3-3e and Figure 3-3f, respectively.



(a) *(b)*

Figure 3-2 Comparative of the static characteristics of discrete common emitter BDSs a) standard IGBT + different diodes; b) ultra fast IGBT + different diodes

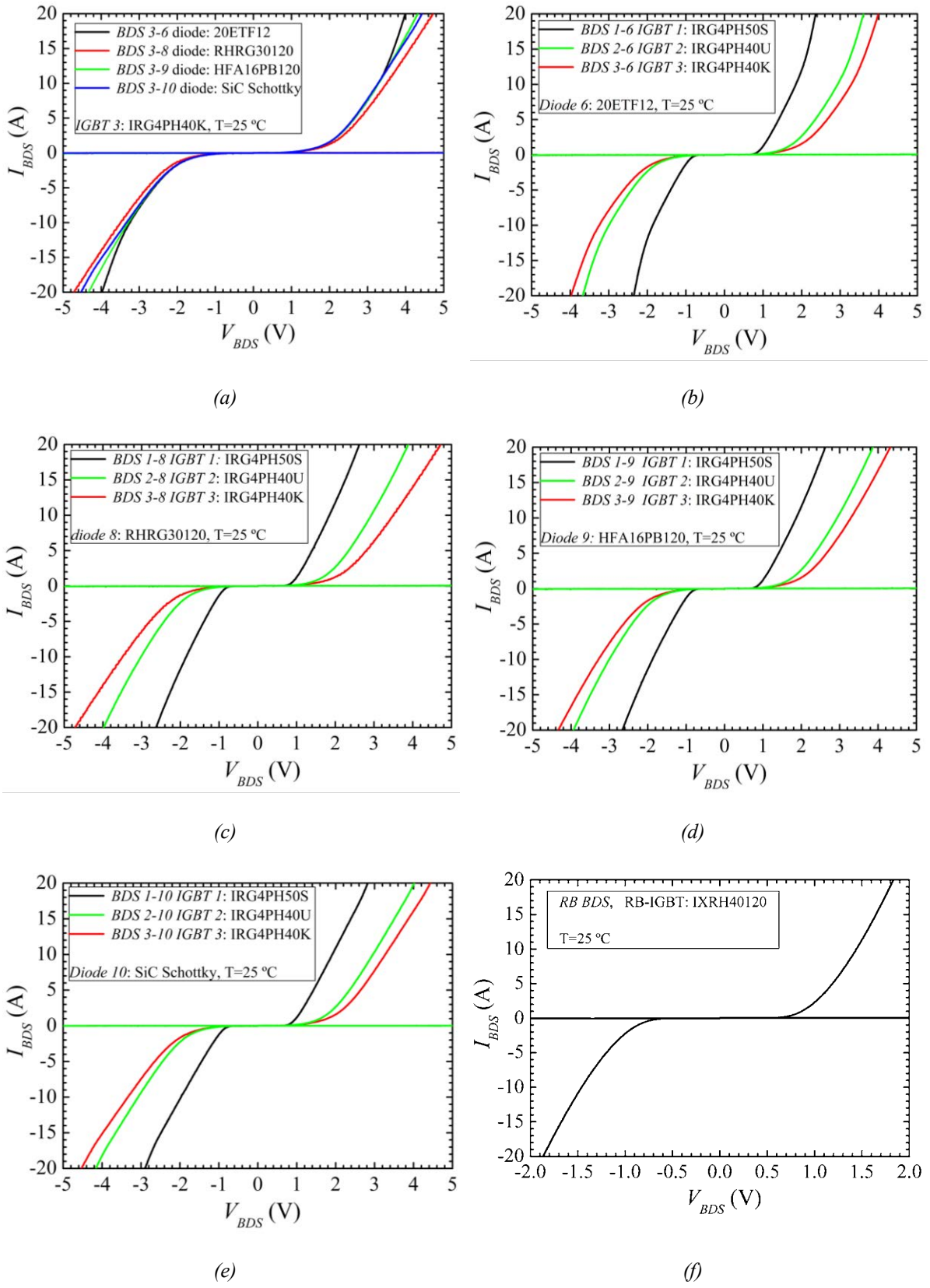


Figure 3-3 Comparative of the static characteristics of discrete common emitter BDSs a) ultra fast (SC) IGBT + different diodes; b) different IGBTs + soft recovery diode; c) different IGBTs + hyper fast diode, d) different IGBTs + ultra fast diode, e) different IGBTs + SiC diode; f) RB BDS

The on-state characteristics of the built discrete BDSs can be summarised by means of Figure 3-4 where the BDS voltage drop at 20 A is shown. As expected, the RB BDS shows the lowest voltage drop since the current flows only through one device. The second BDSs with less voltage drop are the ones combined with the standard IGBT (*BDS 1-X*) due to its low collector-emitter on-state voltage drop since it is optimised to operate at low frequency. The largest voltage drop is exhibited by the BDSs made from the ultra fast (SC) IGBT (*BDS 3-X*). This device is designed to work at high switching speed at the expense of showing a large on-state voltage as depicted in Figure 3-3b. The BDSs combined with the diode *10* (SiC Schottky diode) exhibit generally a higher voltage drop when it is compared to the BDSs combined with a Si diode (diode *6*, *8* and *9*) since Si diode on-resistance is smaller than SiC diode.

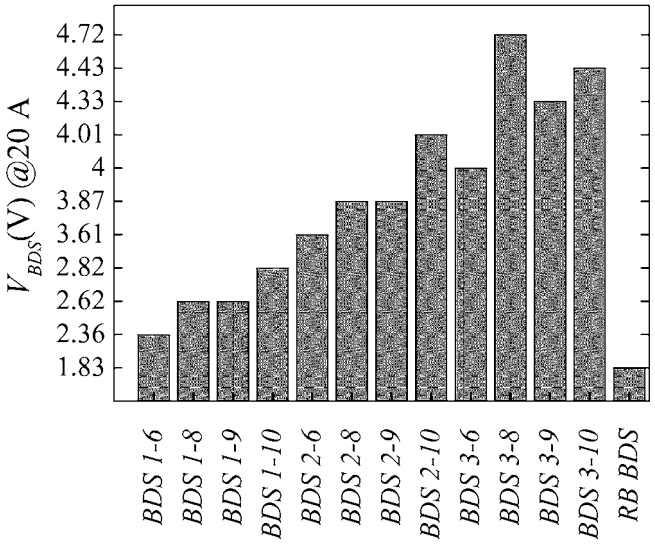


Figure 3-4 Comparison among the voltage drop of the built BDSs at 20 A

The conduction losses associated to a power semiconductor are due to the forward voltage drop across the device and the current through it during the conduction time (the time the device is active). Hence, the *RB BDS* will exhibit the lowest conduction power dissipation whereas *BDS 3-X* the largest one.

3.1.2. Static Device Modelling

The most spread mathematical models to characterise the device on-state voltage versus current characteristic for an IGBT and a diode are presented in (3.1) and (3.2), respectively, assuming the voltage drop shows a linear dependence with current [71].

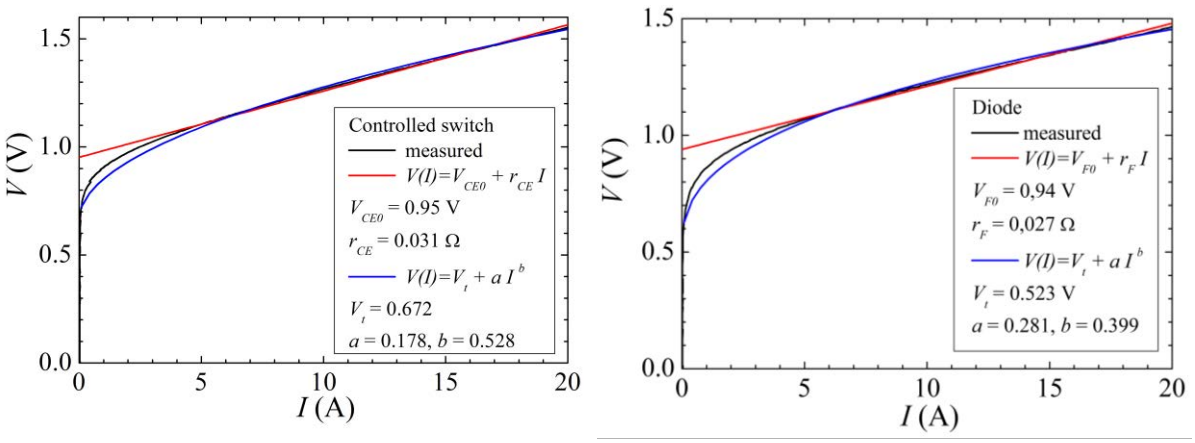
$$V(I) = V_{CE0} + r_{CE}\, I \tag{3.1}$$

$$V(I) = V_{F0} + r_F\, I \tag{3.2}$$

where V_{CE0} and V_{F0} are the IGBT and diode off-set voltages respectively and r_{CE} and r_F are the corresponding dynamic resistances. These parameters can be obtained by fitting the experimental curves of Figure 3-5. The models based on the expressions (3.1) and (3.2) show poor accuracy at low current levels, hence, expression (3.3) will be used in order to improve the static modelling accuracy [72]:

$$V(I) = V_t + a\, I^b(t) \tag{3.3}$$

V_t represents the off-set voltage, a is associated with the dynamic resistance and b is a fitting parameter. The relative error of (3.2) respect to the measured data at 1 A is 11.6 % whereas 6.2 % is for (3.3).



(a) *(b)*

Figure 3-5 Static characterisation and modelling a) controlled switch, IGBT 1 (IRG4PH50S), b) diode 6 (20ETF12) fast recovery diode

3.2. BDS Switching Test Circuit

All the commutation processes given in a typical three-phase to three-phase MC can be reproduced in the equivalent two-phase to one-phase commutation test circuit of Figure 3-6 [68]. The dynamic behaviour of the power elements within the BDSs can be precisely studied from this circuit by measuring their current and voltage drop at different test conditions, determining the switching losses associated to both, hard soft commutations. The switching losses are due to the energy dissipated by the device

during the switching transients. These energy losses depend on the simultaneous voltage and current at the instant of the commutation [73].

The switching test system is modular in the sense it allows characterising different discrete BDSs combinations as well as BDSs integrated in power modules [40]. In addition, it is flexible since any kind of current commutation strategy [24] can be implemented by the control circuit. The switching test system is split in two main parts: the power and the control circuit.

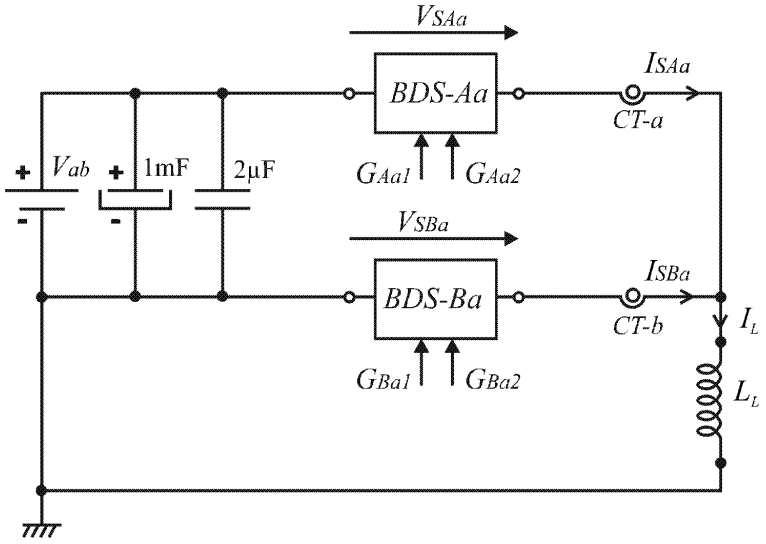


Figure 3-6 Schematic of the power stage of the experimental rig

3.2.1. Power Circuit

The power stage implements two generic BDS cells (*BDS-Aa* and *BDS-Ba*) allowing devices current measurement (I_{SAa} and I_{SBa}) by means of two current transducers (*CT-a* and *CT-b*) and voltage drop across the power devices (V_{SAa} and V_{SBa}) with two differential voltage probes. The power circuit of the BDS cell itself is a modular element since discrete power semiconductor devices can be easily replaced using low-inductance screwed connectors which allow building BDSs with different operating characteristics and different arrangements, i.e. CE BDS (Figure 3-7a), RB BDS (Figure 3-7c) or a CC BDS. A CC BDS has been not implemented since two power supplies with a positive and negatives polarity are needed to supply the gate driver of each IGBT within the BDS, i.e. in total four power supplies for BDS. On the contrary, the CE configuration requires only two power supplies (positive and negative polarity) to control both IGBTs within a BDS since they share the emitter connection. In addition, the results obtained by the CE configuration are analogous to the CC due to its

symmetry. The implemented BDS cell circuits (Figure 3-7b and Figure 3-7d) include also two gate resistors, *Rg1* and *Rg2*, mounted on insertion connectors to adjust the turn-on and turn-off transitions; two Zener diodes connected back to back (*Dz1* and *Dz2*) which provide transient voltage protection in both polarities of each gate of the switching device; and the corresponding control connectors to switch on/off the gate power devices. *GAa1*, *GAa2*, *GBa1* and *GBa2* are the corresponding gate activation signals provided by the high level control. The V_{ab} DC voltage is intended to be the voltage between two input phases of a MC at the moment of the commutation and the inductive load L_L and the pulse test duration determine the test current. The sign of the test current is positive when the I_L current is flowing into the load L_L.

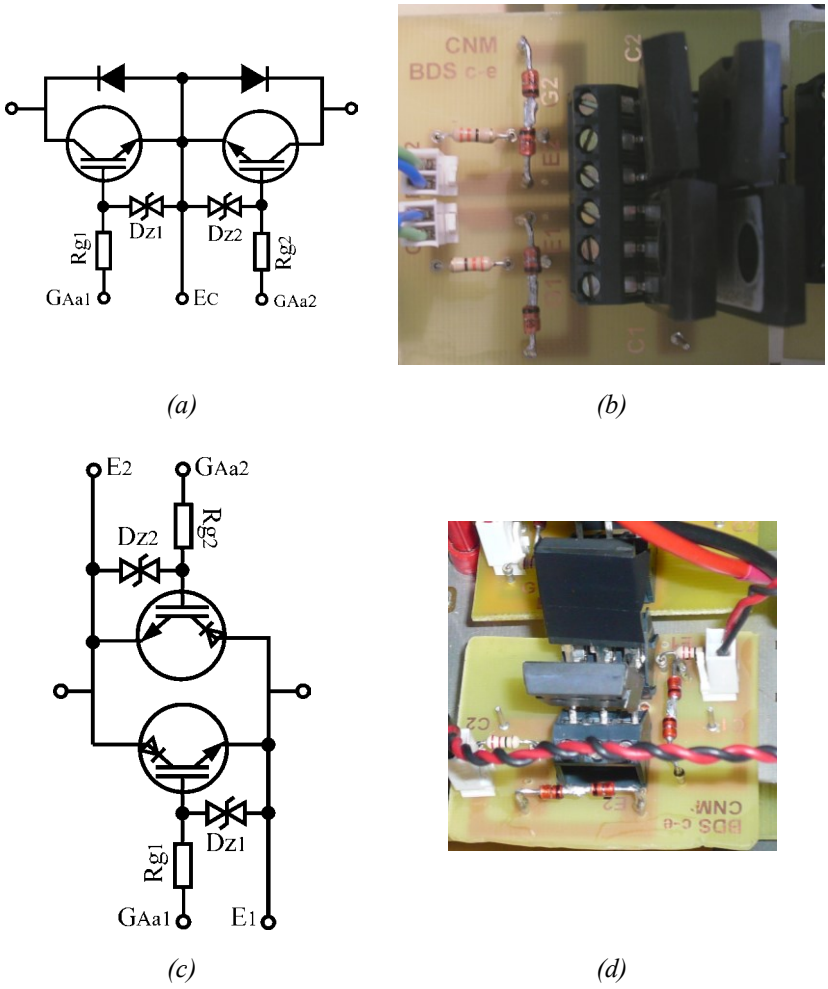


Figure 3-7 CE BDS commutation cell a) schematic; b) discrete implementation. RB BDS commutation cell c) schematic; d) discrete implementation

3.2.2. Control Circuit

The control stage has been designed to be a universal BDS control circuit, that is, all kind of BDSs implementations can be driven with the same board providing a safe commutation between BDSs. The main blocks of the control board are depicted in Figure 3-8.

The *local control* block provides smart switching sequences for the current commutation strategy ("four-step", "two-step", etc.) [24] by means of two general purpose PIC microcontrollers [74]. The block inputs are the current sign (e.g. *Isign-A*) and state of the corresponding BDS (e.g. *In-A*). The output is given by the logic signals (e.g. *OAa1* and *OAa2*) which control the on/off state of the BDS. A "four-step" commutation strategy [23] has been firstly implemented by the local control block (details can be found in chapter 2) because it is the most spread and reliable solution to implement the commutation strategy in MCs [26].

The *Opto-coupled gate driver* block is led by the HCPL-312 integrated circuit [75]. On one hand, it provides the drive voltages required to fire the gates of IGBTs and RB-IGBTs (e.g. *GAa1* and *GAa2*). On the other hand, it optically isolates the logic signals of the *local control* block from the high voltages and current of the BDSs under test.

Two *floating voltage power supplies* are required to generate the positive and negative power supplies of each one of the *Opto-coupled gate driver* blocks.

In this particular case, the *High level BDS control signals* block consists of a simplified logic circuitry which generates two complementary TTL signals (*In-A* and *In-B*) from a pulse train (*In*) set by an external pulse generator. The pulse train is well characterised by its frequency and duty cycle. These two adjustable parameters allow generating the desired test current in the test circuit as shown in Figure 3-9. For instance, a turn-off and turn-on test current is set at 10 A by means of *In* pulse train with frequency of 15 kHz and duty cycle of 50 % at the descending edge of the first pulse and at the ascending edge of the second pulse, respectively. Just modifying the frequency and duty cycle of *In* signal (and of course the load value), the test current can be fixed.

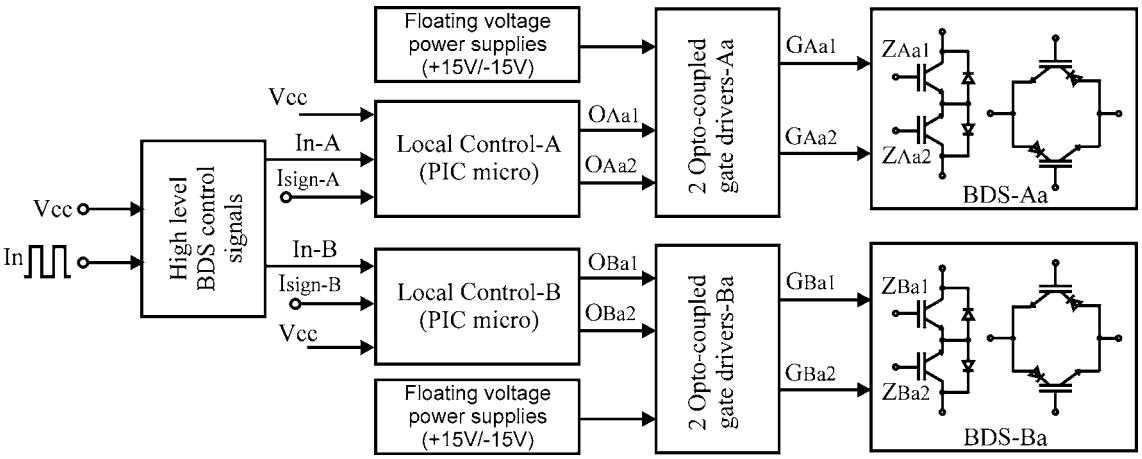


Figure 3-8 Block diagram of the universal BDS control board for a two-phase to one-phase MC

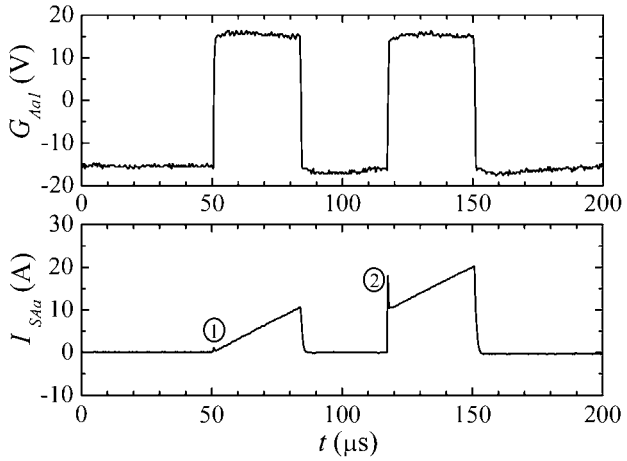


Figure 3-9 GAa1 gate driver signal and BDS-Aa current are set by an In signal with frequency of 15 kHz and duty cycle of 50 %

The waveforms of Figure 3-10 depict the correct functionality of the control board. Figure 3-10a describes the behaviour when the current in the load is positive (i.e. current is flowing into the load so that *Isign-A* value is 5 V) and a commutation is demanded in *BDS-Aa* (*In-A* is activated). First, the IGBT in line with the current direction (Z_{Aa1}) is gated on by *GAa1* signal and after the IGBT don't carrying current (Z_{Aa2}) is gated on when *GAa2* signal is *on*. When the *BDS-Aa* switching-off is demanded (*In-A* is *off*), first Z_{Aa2} is gated *off* (*GAa2* signal is *off*) and after Z_{Aa1} is gated *off* (*GAa1* signal is *off*) because it was carrying the current. In case the load current is flowing in opposite direction (*Isign-A* value is 0 V) as shown in Figure 3-10b, Z_{Aa2} gates on (*GAa2* signal is *on*) first, followed by Z_{Aa1} gating on (*GAa1* signal is *on*) because it is carrying no current. In case of a turn off demand (*In-A* is *off*), *ZAa1* switches-off first

(*GAa1* signal is *off*), and after Z_{Aa2} gates off (*GAa2* signal is *off*). As it can be observed from Figure 3-10 the voltage range of the IGBT gate control signals (*GAa1*, *GAa2, GBa1* and *GBa2*) is from -15 V to +15 V. This negative gate voltage speeds up the turn-off and assures the IGBT is totally *off* avoiding a possible false turn on due to spurious voltage peaks on the gate terminal. +15 V is the typical value used for turning-on the device and allows fully enhanced performance.

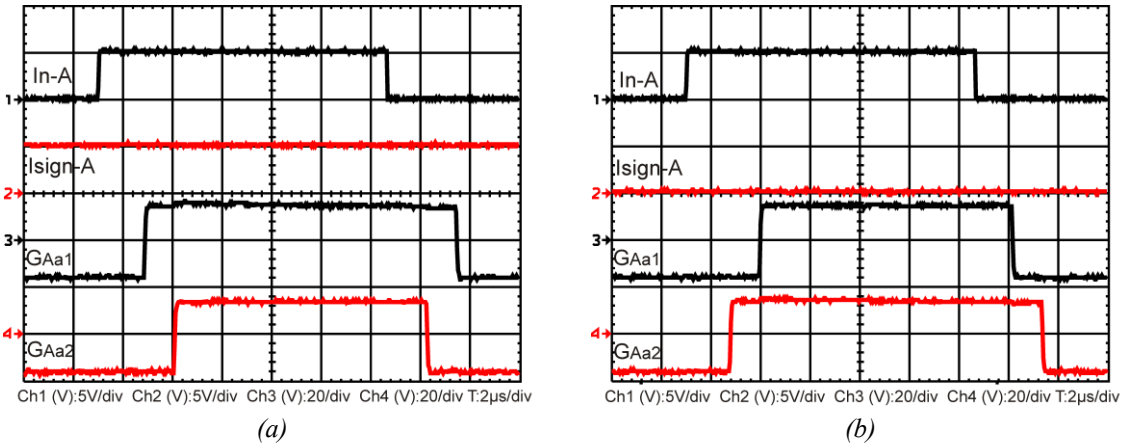


Figure 3-10 Universal BDS control board operation. Gate control signals for a signal demand on BDS-Aa, a) Ising-A > 0. b) Ising < 0.

3.2.3. Design and Measuring Considerations

The interconnection of the power stage, the universal BDS control board and both BDS cells result in the experimental BDS switching test circuit shown in Figure 3-11. In order to obtain a good signal performance a list of practical aspects are taken into account in the design of the power stage and control circuits. For instance, the cable length of the probe as well as differences in the lengths of the voltage and current signal paths could be possible causes of delay in the measurement. A good accuracy in the voltage and current measurement is required to avoid problems. For this reason, a study of the delays associated with the measuring probes is first performed.

3.2.3.1. Power Circuit Considerations

The power PCB layout is carefully designed following these tips:

- The board layout is designed to obtain low stray inductance using a double sided PCB and bus-bar layouts.

- PCB tracks are kept as short as possible and thick to reduce parasitic inductance and parasitic resistance. Right angles are avoided during the routing. Loop areas are avoided in order to minimise radiated noise.
- Power and return traces are placed one directly on the top of the other in order to provide field cancellation and minimum loop areas.

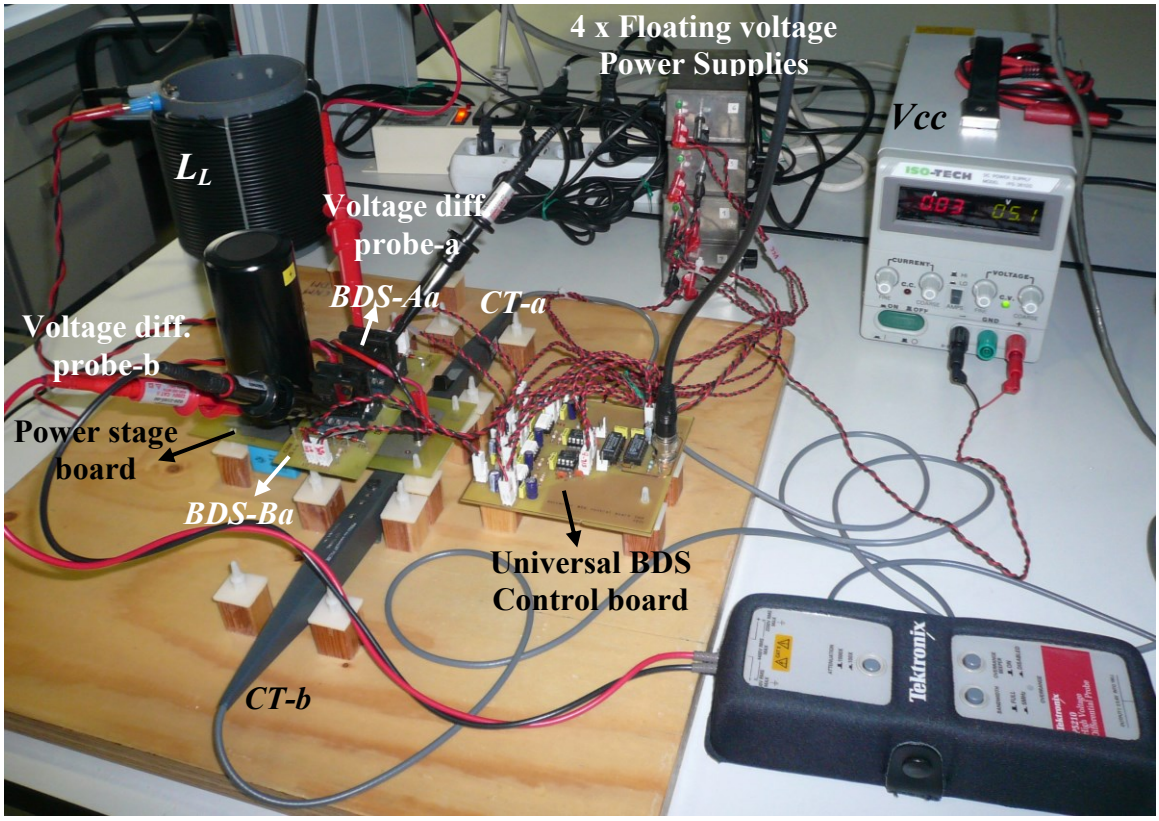


Figure 3-11 Experimental BDS switching test circuit

3.2.3.2. Control circuit considerations

The design of the control PCB is done keeping in mind these aspects:

- Minimising the loop area that contains the gate drive decoupling capacitor improves gate driver noise immunity.
- Using one opto-coupler for each gating device and routing each gate drive return directly to the emitter of its corresponding power device is one of the ways to provide noise immunity.
- Routing the gate drive signal directly beneath (or above) its return helps to reduce loop area.

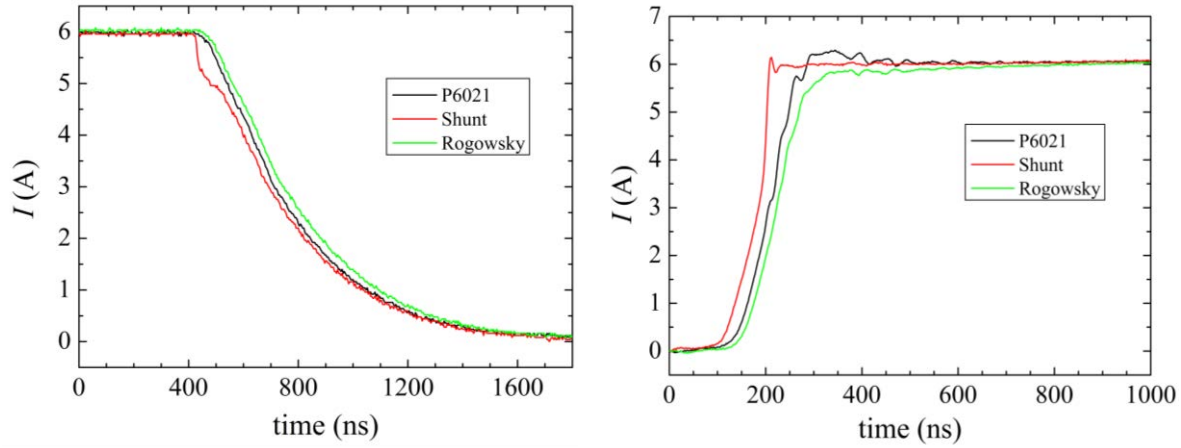
- Twisted-pair cables are used to connect each gate driver output to the gate-emitter terminals of the corresponding power device and to connect the -15 V / +15 V floating power supplies to the supply voltage (V_{CC}, V_{EE}) of the gate drive opto-coupler. Length cables are as short as possible.
- Gate control signals are placed as far away as possible from the power terminals and power cables.

3.2.3.3. Current and Voltage Probes

The probes become part of the measurement and they introduce loading to the circuit. The resistive, capacitive and inductive components on the probe could affect the response of the circuit under test. In addition, the probes delay can also severely affect the switching power measurements. The influence of the probes on the voltage and current device measurements is now discussed.

3.2.3.3.1. Current Probe

Several current probes (P6021 from Tektronix [76], a low inductance shunt resistor [77] and a Rogowsky probe [78]) are tested in the same circuit and under the same conditions measuring the IGBT current during turn-off and turn-on processes. The resulting performance of these probes is shown in Figure 3-12. Regarding the delay and response, there is almost no difference among the three current probes in the current measurement during the IGBT turn-off as depicted in Figure 3-12a. In case of the IGBT turn-on current measurement (Figure 3-12b), the shunt shows a fast response and short delay; the Rogowsky probe displays the minimum ringing and P6021's behaviour is between the other probes. P6021 probe is chosen because it fulfils a priory the expected IGBT current response (e. g. *di/dt*), provides isolated measurements and allows a compact integration in the test circuit as shown in Figure 3-11.



(a) *(b)*

Figure 3-12 Current measurement with different current probes during IGBT a) turn-off, b) turn-on.

The selected current probe is characterised under different *di/dt* and current levels. The shunt measurements are taken as a reference so that the delay and gain associated to the P6021 current probe can be inferred from it. The results for both current probes, *CT-a* and *CT-b*, can be appreciated in Figure 3-13.

It can be observed from Figure 3-13 that *CT-a* shows a larger delay than *CT-b* in all conditions and the delay is slightly larger for the IGBT turn-on measurement. A maximum delay variation for both probes of 5 % is experimented for different values of *di/dt*. On the other hand, a large delay variation for both probes till 19 % is exhibited for different current values. The probe gain keeps almost constant against different *di/dt* values as a variation of less than 2 % is experimented.

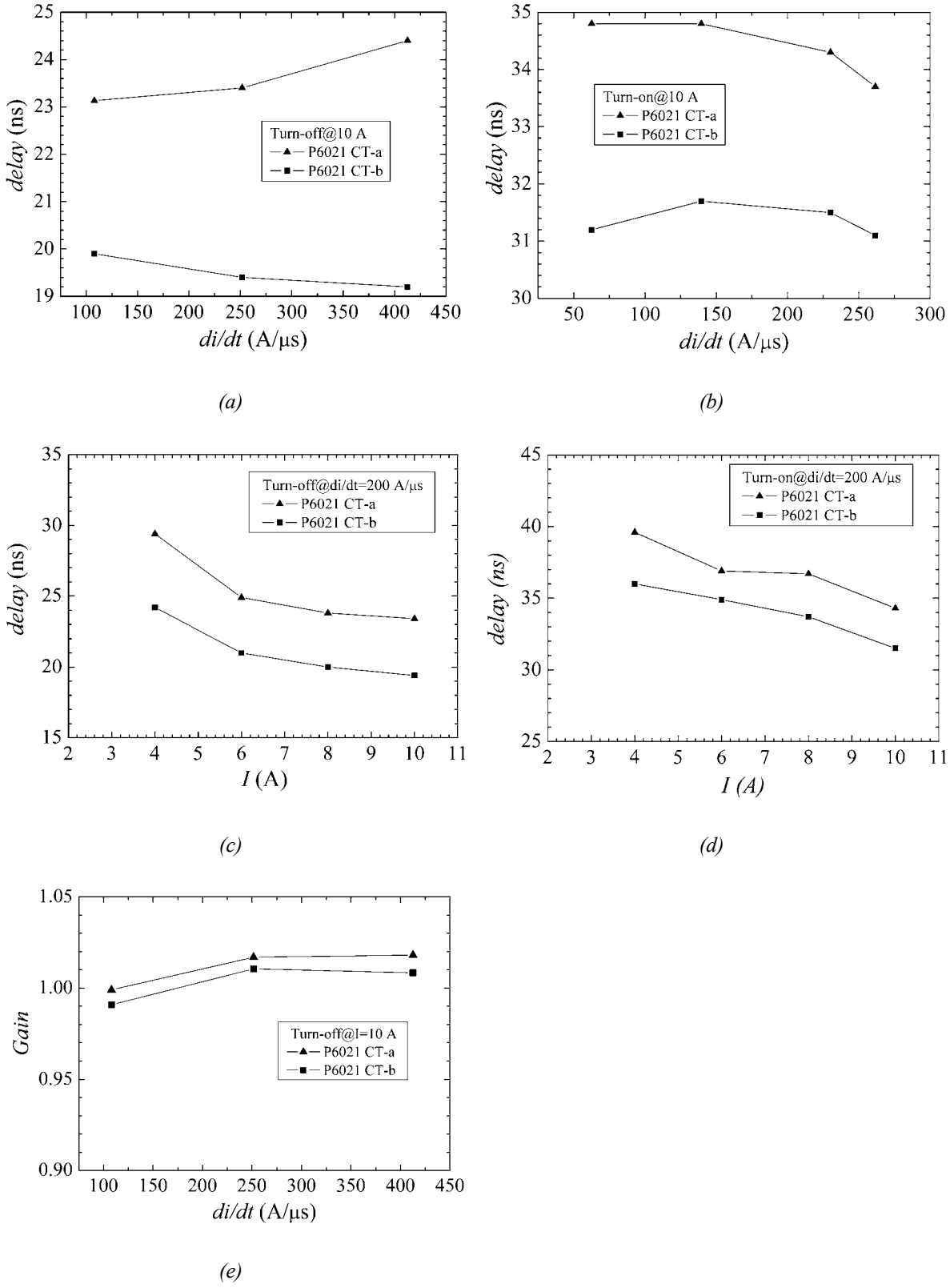


Figure 3-13 P6021 current probe test. a) delay vs di/dt during a turn-off. b) delay vs di/dt during a turn-on. c) delay vs current during a turn-off. d) delay vs current during a turn-on. e) gain vs di/dt during a turn-off

3.2.3.3.2. Voltage Probe

Different voltage probes (passive [79] and differential probes [80]) are tested in the same circuit as for the current probes and under the same conditions, measuring the IGBT voltage during a turn-off and a turn-on. Figure 3-14 shows the results of such tests. The differential probe exhibits a slightly larger delay than the passive one. Both probes show a sufficient dynamic range and bandwidth for the IGBT voltage measurement.

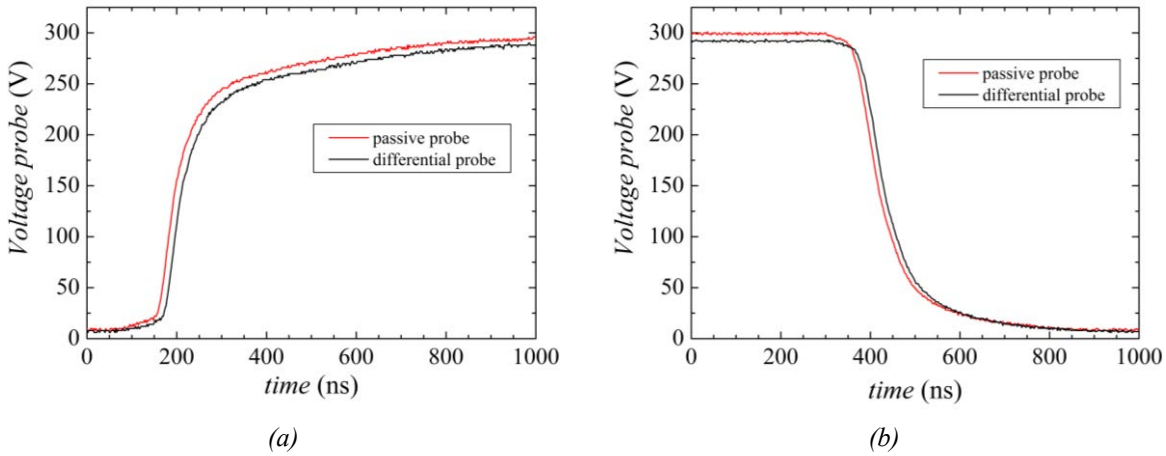


Figure 3-14 Voltage measurement by means of different probes during a) IGBT turn-off. b) IGBT turn-on.

Using a high voltage differential probe is a much better solution since accurate floating measurements are required. The emitter point of any of the BDS implementations is not at ground reference, so that a differential probe is needed to measure the IGBT V_{CE} voltage. A detailed assessment is performed to characterise the differential probe under different *dv/dt* and voltage level switching conditions. The results are depicted in Figure 3-15. The delay due to the IGBT turn on is 9 % larger than the turn-off. The influence of the *dv/dt* and voltage on the delay associated to the probe is very similar in both cases, around 13.3 ns for the turn on and 12.4 ns in case of the turn off. The gain dependence on the *dv/dt* and voltage is also quite similar, 2 % variation can be exhibited between them by the turn-on case, while almost no variation is shown by the turn-off.

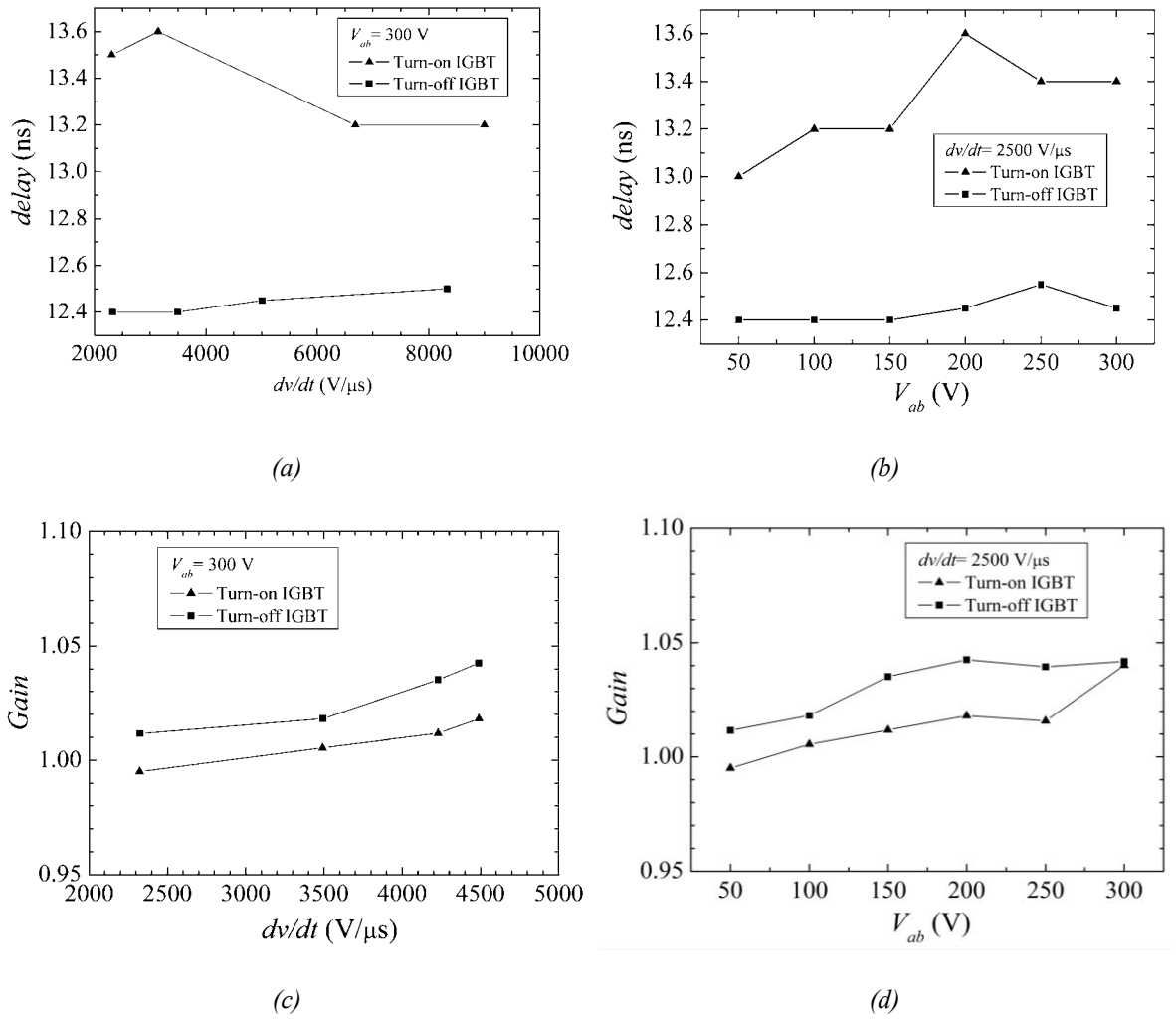


Figure 3-15 Differential voltage probe tests. a) delay vs dv/dt during a turn off and turn-on. b) delay vs V_{ab} during a turn-off and turn-on. c) Gain vs dv/dt during a turn-off and turn-on. d) Gain vs V_{ab} during a turn-off and turn-on

In conclusion, P6021 current probe shows a larger delay than the differential voltage probe, around 10 ns for the turn-off and 20 ns approximately for the turn-on. Thus, a delay compensation should be carried out in order to minimise the difference in the delays between voltage and current probes. This compensation is implemented in the MATLAB script which processes the acquired current and voltage waveforms from the test circuit as described in Appendix B. Regarding the gain, both probes show a stable gain against different switching conditions (*di/dt*, *dv/dt*, current and voltage levels).

3.3. Dynamic BDS Characterisation

The BDS test switching circuit of Figure 3-11 is now used to characterise the commutation process of different discrete BDSs as depicted in Figure 3-16 and Figure 3-17 under the following test conditions: Gate controls (*GAa1*, *GAa2*, *GBa1*, *GBa2*) = ±15V, *Rg1=Rg2*= 33 Ω, V_{ab}= 300 V, I_L = 10 A. These conditions have been selected in order to compare the main switching phenomena found with the different power devices under study. In the next section, test conditions at different voltages and currents will be used in order to develop a power losses modelling. The gate-emitter voltage of the active IGBT within the *BDS-Aa* (V_{GE} Z_{Aa1}), the voltage across *BDS-Aa* (V_{SAa}), and the current through *BDS-Aa* (I_{SAa}) and *BDS-Ba* (I_{SBa}) are measured, where *BDS* means each one of the built discrete BDSs (i.e. *BDS 1-6*, etc). Once the *BDS-Aa* voltage and current are known, the turn-on and turn-off energy losses are calculated as stated in section 2.3 of chapter 2. The hard turn-on (Figure 3-16) and hard turn-off (Figure 3-17) switching phenomena follow the type II and type I commutation processes described in detail in chapter 2, respectively. Moreover, the soft commutation processes are also described in Figure 3-18. Likewise, the influence of the power devices characteristics within the BDS on the commutation can be appreciated in those figures as it will be commented.

Prior to a commutation demand, the load current is flowing through *BDS-Ba* and $V_{ab} > 0$. When the commutation occurs, *BDS-Aa* (the incoming BDS) undergoes a hard turn-on switching as depicted in Figure 3-16. Figure 3-16a shows the hard turn-on commutation voltages and currents for *BDS 1-X* (IGBT *1* combined with diodes *6, 8,* and *9*). The effect of the diode turn-off recovery characteristic is highlighted in the *BDS-Ba* current curves of Figure 3-16a. Diode *6* (fast soft recovery behaviour) requires a large reverse recovery time in order to sweep out the excess charge stored and this leads to a high reverse recovery current value. This reverse recovery current is added to the *BDS-Aa* current, resulting in a current peak of almost 30 A. As diodes *8* and *9* show a faster reverse recovery time than diode *6*, a lower current overshoot is exhibited by each respective BDS as appreciated in Figure 3-16a. The most remarkable power dissipation results for *BDS1-6* due to its large reverse recovery current.

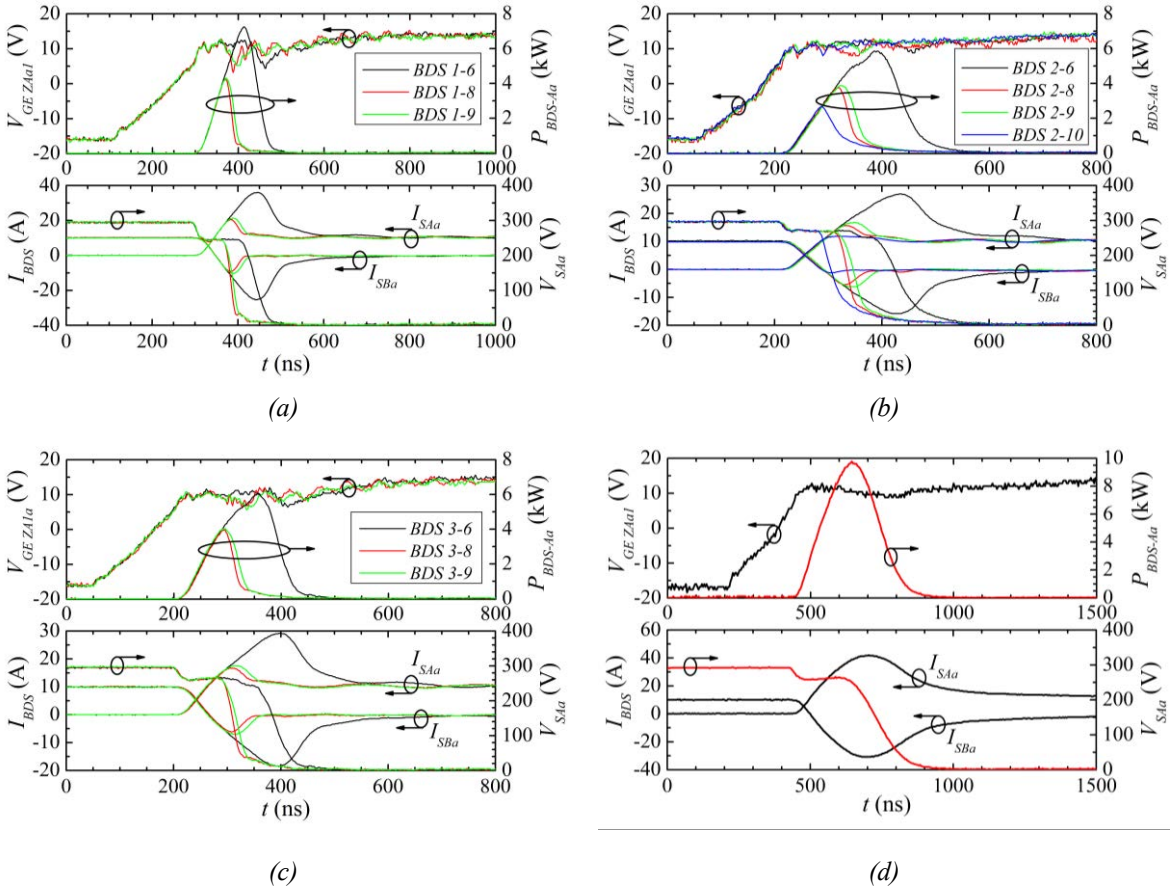


Figure 3-16 Experimental waveforms during the BDS-Aa turn-on at V_{ab} = 300 V, I_L = 10 A: a) BDS 1-6, 8, 9. b) BDS 2-6, 8, 9, 10. c) BDS 3-6, 8, 9. d) RB BDS

Figure 3-16b shows the commutation voltages and currents for *BDS 2-X* (IGBT *2* combined with diodes *6, 8, 9* and *10*) due to a hard turn-on switching. There is a remarkable difference between *BDS-Ba* current of *BDS 2-10* (built with a SiC diode) and *BDS 2-6* (built with a Si fast soft recovery diode). The effect of diode *10* (very low reverse recovery time and current) can be appreciated on the *BDS-Ba* current. The reason of this behaviour is due to the fact that Schottky diodes are unipolar devices. There is no minority carrier recombination so that the reverse recovery current is nearly negligible. The reverse recovery charge is quite low and results in a junction capacitance with almost no charge stored. This fact leads to a fast switching and an important power losses reduction as shown in Figure 3-16b. Therefore, no overshoot is exhibited in *BDS 2-10* current, whereas an important current peak of 15 A is undergone by *BDS 2-6* due to the addition of its large reverse recovery current to the *BDS 2-6* current. On the other hand, a moderate current peak is shown in *BDS 2-8* and *BDS 2-9* currents.

Figure 3-16c shows the commutation voltages and currents for *BDS 3-X* (IGBT *3* combined with diodes *6, 8 and 9*) due to a hard turn-on switching. The aforementioned discussion can be also applied for this type of BDS. *BDS 3-6* exhibits the largest power dissipation mainly due to the high reverse recovery current derived from diode *6* recovery characteristic.

Figure 3-16d shows the commutation voltages and currents for RB BDS due to a hard turn-on switching. The RB BDS shows a longer turn-on transition time compared to the BDSs built with diodes *8*, *9* and *10*, whereas it is similar to the BDSs combined with diode *6*. The internal diode of the RB-IGBT when it is recovered shows a long reverse recovery time and large reverse recovery current as depicted by I_{SBa} curve in Figure 3-16d. In fact, this characteristic is analogous to a normal p-n diode with very soft recovery behaviour.

When the *BDS-Aa* turn-off process is examined, it can be noted that it is not dependent on the diodes behaviour as observed in all current waveforms of Figure 3-17 since the diodes do not experiment any hard commutation. On the other hand, the influence of the IGBT type on the turn-off commutation can be appreciated between *BDS 1-X* (Figure 3-17a) and *BDS 2-X* (Figure 3-17b) or *BDS 3-X* (Figure 3-17c). The commutation process related to the *BDS 2-X* presents a faster turn-off time in comparison with *BDS 1-X* since *BDS 2-X* shows a shorter current tail and thus a faster fall time. The current tailing due to the minority carriers causes the turn-off speed to be slow. The slower current tail, the larger is the power dissipation as illustrated in Figure 3-17a. The RB BDS turn-off current shows an important current tail as depicted in Figure 3-17d. This fact has a remarkable consequence when the delay time of the step of the current commutation strategy is selected.

All *BDS-Aa* voltage hard turn-off switching waveforms show voltage overshoot due to the parasitic inductance of the test circuit. This overvoltage has also an impact on the turn-off losses.

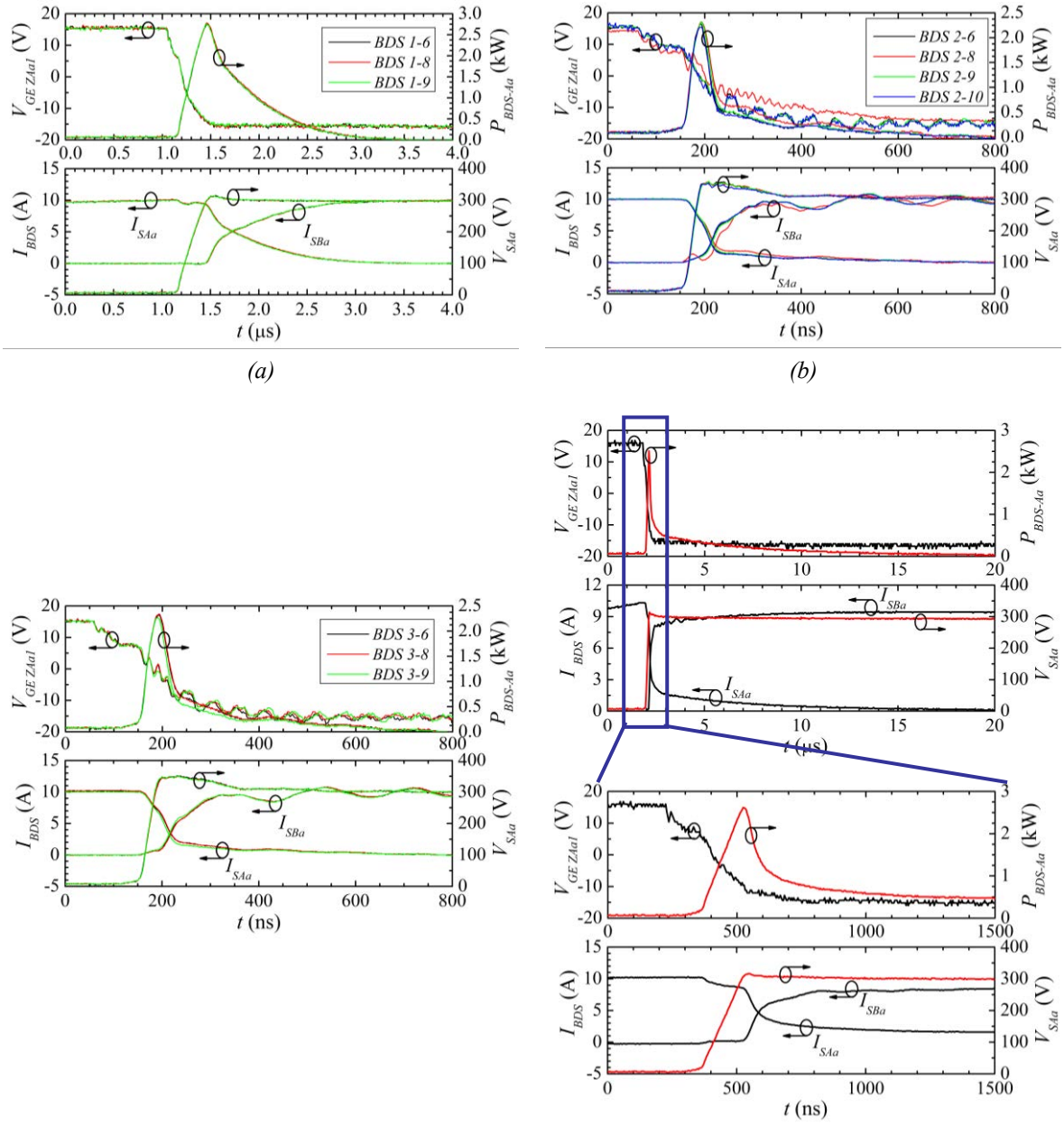


Figure 3-17 Experimental waveforms during the BDS-Aa turn-off at V_{ab} = 300 V, I_L = 10 A: a) BDS 1-6, 8, 9. b) BDS 2-6, 8, 9, 10. c) BDS 3-6, 8, 9. d) RB BDS

The hard turn-on and hard turn-off energy losses of the tested BDSs are summarised in Table 3-2.

IGBT	Diode	E_{on} [mJ]	E_{off} [mJ]	T_{on} [ns]	T_{off} [µs]	BDS Characteristics
1	6	0.64	1.76	160	1.6	Standard IGBT+ soft recovery diode
1	8	0.21	1.81	100	1.6	Standard IGBT + hyper fast recovery diode
1	9	0.23	1.76	100	1.6	Standard IGBT + ultra fast recovery diode
2	6	0.87	0.19	300	0.34	Ultra fast IGBT + soft recovery diode
2	8	0.31	0.24	220	0.34	Ultra fast IGBT + hyper fast recovery diode
2	9	0.35	0.205	220	0.34	Ultra fast IGBT + ultra fast recovery diode
2	10	0.2	0.18	220	0.34	Ultra fast IGBT + SiC Schottky diode
3	6	0.75	0.23	220	0.44	Ultra fast IGBT SC rated + soft recovery diode
3	8	0.26	0.24	170	0.44	Ultra fast IGBT SC rated + hyper fast recovery diode
3	9	0.3	0.21	170	0.44	Ultra fast IGBT SC rated + ultra fast recovery diode
RB-IGBT		2.15	2.6	420	15	RB-IGBT

Table 3-2 Switching characteristics of the discrete BDSs. Test conditions: Gate controls (G_{Aa1}, G_{Aa2}, G_{Ba1}, G_{Ba2})= ±15 V, R_{G1}=R_{G2}= 33 Ω, V_{ab} = 300 V, I_L = 10 A

The RB BDS shows the worst switching performance in terms of power losses, whereas *BDS 2-10* exhibits the best one (the lowest losses) for the considered test conditions. These results can be extrapolated for higher values of current since power losses increase with current.

Two conclusions can be inferred from the voltage and current hard turn-on and turn-off switching waveforms of the measured BDSs:

- The reverse recovery characteristics of the diodes have a direct influence on the BDS turn-on power losses as well as on the turn-on commutation time due to the

reverse recovery time. At room temperature, the SiC Schottky diode and a Si very fast recovery diode show a similar recovery performance.

- The effect of the IGBT tail current increases the turn-off energy losses and requires an increase in the delay time associated to the current commutation step strategy.

Regarding the soft switching performance of the BDSs under test, only the more extreme behaviours are shown in Figure 3-18. The power dissipation associated with the soft turn-on commutation shows very low losses values as appreciated in Figure 3-18a since the commutation is undergone with a low switching voltage. On the contrary, non-negligible power dissipation is exhibited by the soft turn-off commutation of *BDS 1-6* as depicted in Figure 3-18b. This is due to the fact that the large reverse recovery current of diode *6*, located in the *BDS-Ba*, is added to IGBT *1* current resulting in a high power dissipation. On the other hand, a completely different scenario is presented by *BDS 1-9* due to the better recovery characteristic of diode *9*, where low power dissipation is generated as observed in Figure 3-18b. The aforementioned comment is also valid for the RB-IGBT soft turn-off switching plotted in Figure 3-18c, where the effect of the internal diode of the RB-IGBT (placed in the *BDS-Ba*) on the power losses is still more outstanding than for *BDS 1-6*. This behaviour leads to very high power dissipation. Relative low power losses are observed when the RB-IGBT undergoes a soft turn-on commutation since it is performed at low current.

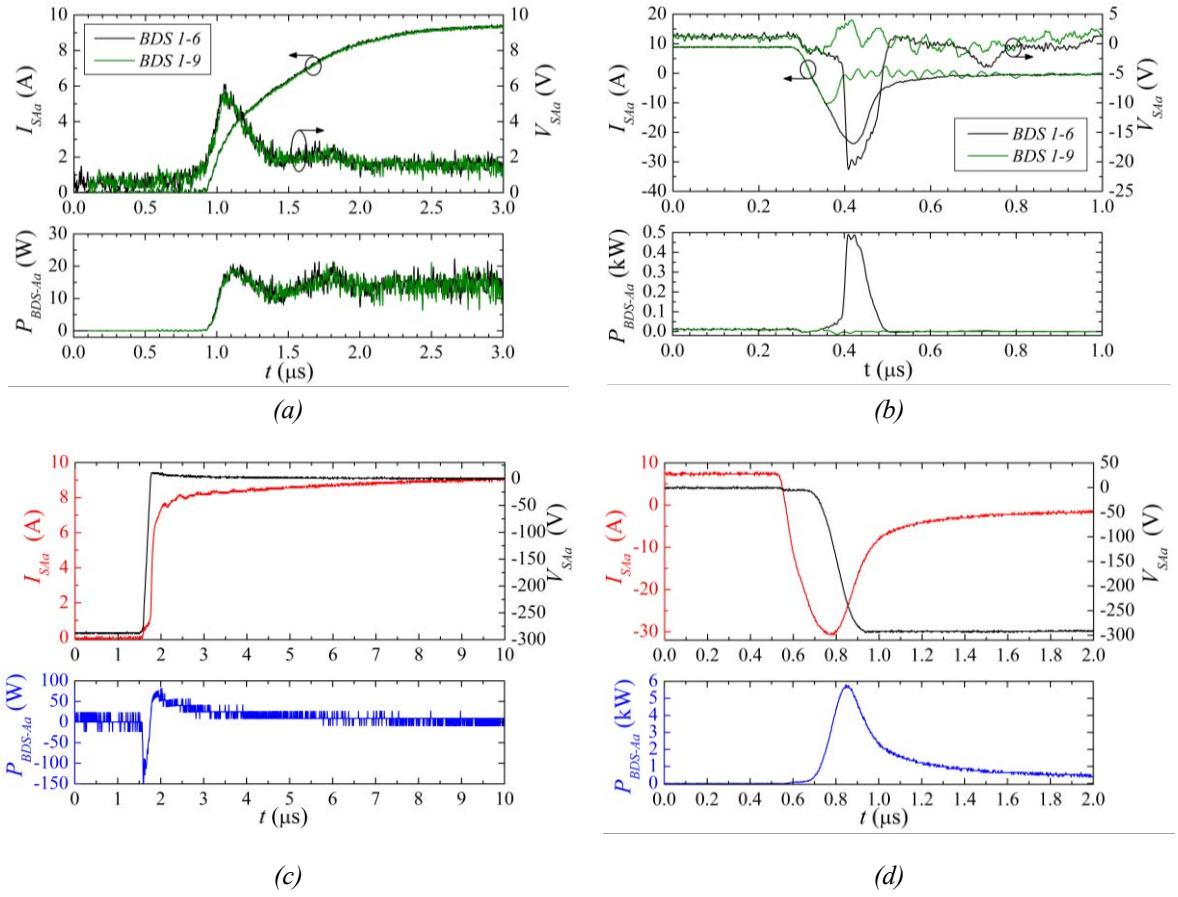


Figure 3-18 Experimental waveforms during a soft commutation process at V_{ab} = 300 V, I_L = 10 A: a) BDS 1-6, 9 turn-on. b) BDS 1-6, 9 turn-off. c) RB BDS turn-on. d) RB BDS turn-off

In conclusion, attention shall be paid with the soft commutation processes since the associated power losses can be no negligible as it could be in principle expect.

3.3.1. Dynamic Device Modelling

The dynamic device modelling methodology tries to cope with all operation conditions find in a typical 4.5 kW matrix converter, i.e. high and low voltages and high and low currents can be demanded to the test circuit to cover the entire device working envelope. This characterization scenario has been defined in order to determine the devices power losses models used in subsequent chapters devoted to matrix converters losses calculation. So, the procedure followed in section 3.3 is now extended for different V_{ab} applied voltages (100, 200, 250 and 300 V) and different test currents (5, 10, 15 and 20 A). As explained in chapter 2, different types of commutations [68] are involved in the power devices within the BDSs depending on the input phases relative voltages (represented by V_{ab} in the test circuit) and direction of the load current

(represented by I_L). All the possible commutation scenarios (hard and soft switching) obtained by means of the test circuit of Figure 3-11 are summarised in Table 2-2 of chapter 2.

The voltage and current switching waveforms at all test conditions for each kind of commutation and each BDS realisation are acquired and recorded by a scope. These experimental data are processed by means of different MATLAB scripts (more details can be found in the Appendix B). It should be pointed out that the delay and gain analysis performed for the current and voltage probes has been taken into account in the computation of the energy losses by means of the corresponding MATLAB scripts. The switching energy losses (E), are represented as a two variable function, i.e. measured device voltage (V) and measured device current (I) and marked by blue bullets as depicted in Figure 3-19 for *BDS 1-6*. Analogous plots are obtained for each type of BDS realisation.

The most common procedure for modelling the switching losses can be found in the literature [81, 82], where the switching losses are assumed to be linear with the commutation voltage and current at the switching instant as expressed in:

$$E_{sw} = E_{swR} \frac{V I}{V_R I_R} \tag{3.4}$$

where E_{SWR} is the switching energy at the reference voltage V_R and current I_R, values found typically in the device datasheet. This method is widely spread when the total average power losses of a three-phase MC are predicted [55] since its application is straightforward, but it could be less suitable when the switching losses of a particular power device within the converter need to be investigated and for this reason, the switching losses models proposed in this chapter rely on a full dynamic characterisation as illustrated in Figure 3-19. The obtained experimental data is fitted by a polynomial function of degree two as a function of current and voltage across the device as described in a generic way in:

$$E_{sw} = p_{00} + p_{10} I + p_{01} V + p_{20} I^2 + p_{12} IV + p_{02} V^2 \tag{3.5}$$

where p_{00}, p_{10}, p_{01}, p_{20}, p_{12} and p_{02} are the fitting polynomial coefficients. The result of this approach is represented in the switching energy surfaces depicted in Figure 3-19 for the *BDS 1-6* realisation. As sake of simplicity, results for *BDS 1-6* are depicted, but the switching energy surfaces of the others BDS devices under test have also been obtained. As it can be derived from Figure 3-19, the error between the experimental data points and the switching energy fitted expression is quite reasonable (less than 10%) in almost all the voltage – current domain of interest. On the other hand, as it can be appreciated in Figure 3-19a and Figure 3-19b, the error between the linear approach described by (3.4) and the experimental data can be relevant, mainly in the boundaries of the voltage – current domain (far from the reference values).

As it can be appreciated in Figure 3-19e and Figure 3-19f, energy losses associated with the soft switching processes are one or two orders of magnitude lower than the hard ones. Soft power losses are generally neglected in the practical implementation of a converter, but it should be done carefully. As already discussed, soft power dissipation cannot always be negligible since it mostly depends on the device characteristic and fabrication technology.

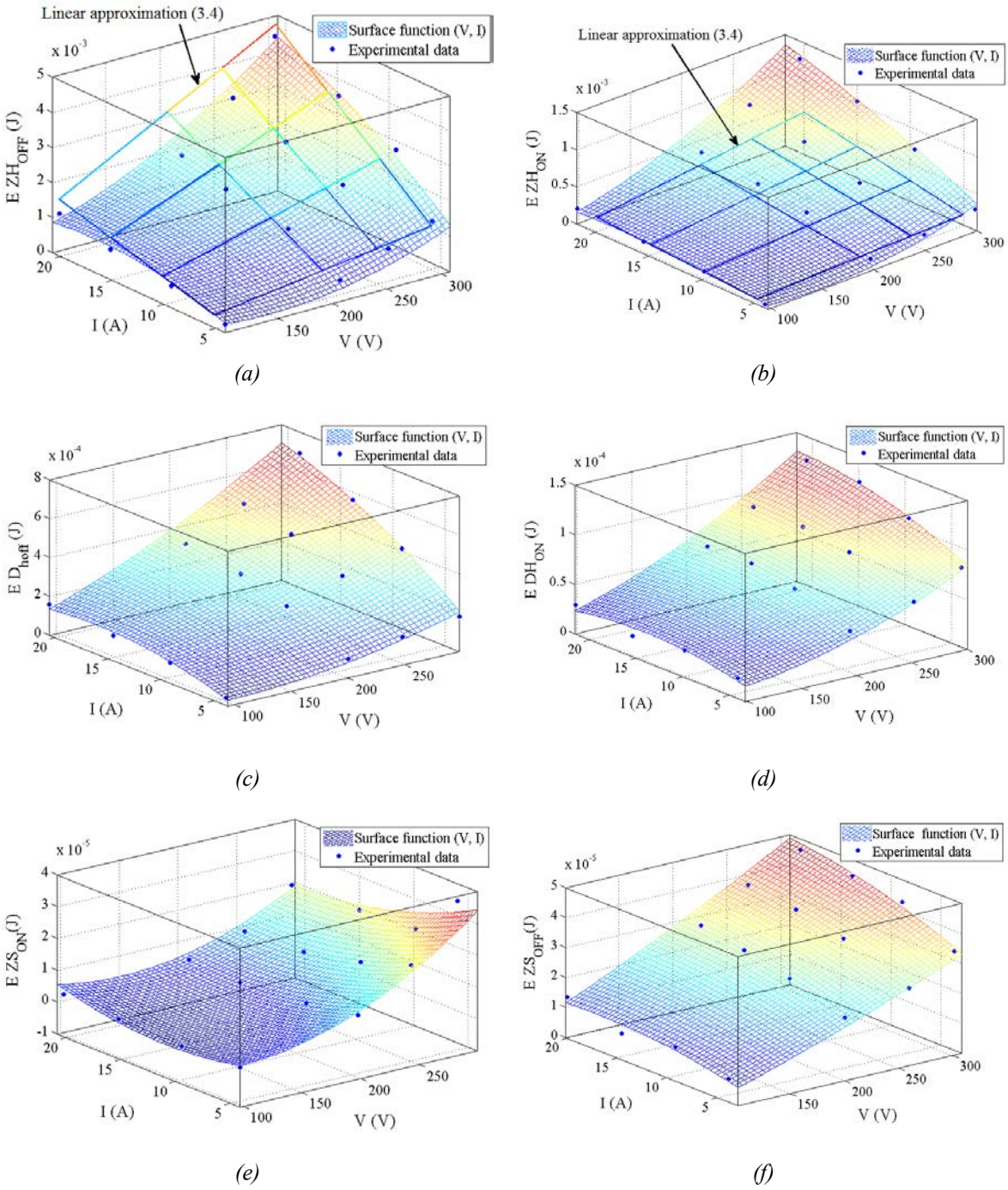


Figure 3-19 Energy losses associated to the BDS 1-6 at V_{ab} = 100, 200, 250 and 300 V and different I_L = 5, 10, 15 and 20 A. Experimental points, linear approximation (3.4) and polynomial fitting (3.5). a) IGBT hard turn-off. b) IGBT hard turn-on. c) Diode recovery. d) Diode hard turn-on. e) IGBT soft turn-on. f) IGBT soft turn-off

3.4. Summary

The target of this chapter is the static and dynamic device characterisation as well as the experimental evaluation of the switching losses of different BDS implementations in a true Matrix Converter operation. Hence, a switching test circuit based on a two-phase to one-phase MC has been implemented. It consists of a power stage circuit, BDS commutation cells, the control circuit and the voltage and current measurement probes. A BDS universal control circuit has been developed in order to generate the corresponding gate signals of the switching devices arranged in a CE, CC or RB BDS configuration. CE and RB BDSs have been built with different commercial power devices and tested. Three representative IGBTs of different switching speeds and a RB-IGBT have been selected as the controlled device. Likewise, three Si diodes types: soft recovery; ultra and hyper fast with soft recovery as well as a SiC Schottky diode have been considered to build the BDSs.

The device voltage and current hard turn/soft-on and hard/soft turn-off switching waveforms have been recorded and processed by means of MATLAB scripts in order to evaluate the corresponding switching losses and analyse the influence of the power devices on the commutation process between BDSs. In conclusion:

- the effect of the IGBT current tail is present at the turn-off phenomena (type I commutation). This fact causes low switching times and large turn-off switching power losses.
- the reverse recovery characteristics of the diode (the discrete diode in series with the IGBT and the internal diode of the RB-IGBT) determine the turn-on power losses and the turn-on transition time.

A summary of the BDS performance according to different types of power devices can be found in Table 3-3.

Configuration		**forward voltage drop**	**conduction losses**	**turn-on switching losses**	**turn-off switching losses**
IGBT	Diode				
Low $V_{CE(ON)}$ and low frequency operation	Soft recovery	low	low	high	high
	Fast recovery	moderate	moderate	low	high
High frequency operation	Soft recovery	moderate	moderate	high	low
	Very fast recovery	high	high	low	low
	SiC diode "zero I_{rr}"	moderate/high	moderate/ high	low	low
RB-IGBT		very low	very low	very high	very high

Table 3-3 Static and dynamic characteristics of different BDS realisations

The effect of the critical parameters of power devices on the commutation processes between BDSs has been identified. This will allow optimising the MC design in terms of electrical response and efficiency. In addition, the performed study will allow carrying out an accurate device dissipation modelling both in conduction and in commutation modes. In fact, this semiconductor loss characterisation will be applied in chapter 4 and 5 to estimate the device power losses of a Voltage Source Inverter (VSI) and a MC, respectively.

4. Power Losses Computation Method

The target of this chapter is the description, implementation and verification of a computation method addressed to evaluate the power losses of the power semiconductors that are part of power converters such as DC/AC voltage source inverters or AC/AC matrix converters. The method is mainly based on the static and dynamic characterisation of the power devices of the basic commutation cells of the converter, e. g. IGBT + freewheel diode for the voltage source inverter (VSI) or bidirectional switch (BDS) in case of the matrix converter (MC). In this chapter the power dissipation of a well-known VSI converter is evaluated by means of the proposed computation method in order to lay the basis of the MC losses estimation that will be analysed in detail in the next chapter. A straight forward application of the proposed method is the optimum selection of the power semiconductors to build the required commutation cells of the converter in terms of efficiency, cost and cooling system design.

4.1 Introduction

In DC/AC and AC/AC power electronics converters like VSIs and MCs respectively, controlled power devices (MOSFETs, IGBTs, RB-IGBTs, etc.) and diodes are operated as switches, alternating conduction, blocking and switching states in cycles. In any of these states, a power dissipation component is generated, which heats the semiconductor and adds to the total power losses of the device. In addition, the device junction temperature is also modified so that the maximum junction temperature must never be exceeded. Otherwise, the device will be damaged or its reliability will decrease. The device power dissipation is dependent on the operating conditions of the converter (output frequency, switching frequency, modulation strategy, voltage and current operation levels, load characteristics, etc.). Therefore, a calculation tool is required to cope with all the operating parameters in order to estimate the total power losses of a power semiconductor at any time of operation of the converter.

Devices' power losses information can be extracted from their datasheet [83] but usually not all the real operation conditions are considered in datasheet parameters. Another option is based on semiconductor simulations based on TCAD (technology computer aided design) physical models although these kind of tools (e.g. Synopsys or Silvaco software packages) are not always available for converter design engineers

since a deep semiconductor device physics ground is required to manage the simulations and to understand the results. In addition to this, these power losses estimations are typically time consuming (if several operating conditions are considered) and could be inaccurate since do not cover probably all the circuit constraints which will arise from the application. In [84] an analytical modelling of semiconductor losses in MC is presented. Conduction and switching losses are modelled by simple mathematical expressions based on the ideal behaviour of the device. The parameters of the losses model expressions are extracted from the device datasheet and they don't always match with the operation conditions of the considered final application. However, the present chapter proposes a method based on actual characterisation of power semiconductor data (in static as well as in dynamic operation) for different operating conditions in order to obtain accurate parameter values allowing the estimation of conduction and switching mode power dissipation in the devices of the commutation cells [85].

4.2 Description of the Semiconductor Power Losses Calculation Method

As it is well established in AC/DC and AC/AC power converters the output fundamental voltage and current waveforms repeat with a time period T. When this condition is reached the converter is in the electrical steady-state. Taking into account these considerations, the total average power losses $\overline{P}$ in a fundamental period for any device can be calculated as [86]:

$$\overline{P} = \frac{1}{T}\int_0^T p(t)\,dt \tag{4.1}$$

where $p(t)$ is the device instantaneous dissipated power and T is the fundamental output current period. The proposed method considers an approximation of the instantaneous power function $p(t)$ since it is difficult to be expressed analytically due to the complexity of the voltages and current waveforms in the converter operation. This approach lies in presupposing that the switching frequency of the converter (f_{sw}) is much higher than the converter output and input frequency (f_{out} and f_i). Consequently, it is assumed that at any considered time instant corresponds one full switching period (T_{sw}). Hence, the power losses of a device at any time t correspond to the average conduction

and switching losses undergone in such device during the $t+T_{sw}$ interval [87] as depicted in Figure 4-1. This approach results in working with simplified continuous time power losses functions and leads to approach the instantaneous power as:

$$p(t) \cong p'_{cond}(t) + p'_{sw}(t) = p'_{cond}(t) + p'_{on}(t) + p'_{off}(t) \tag{4.2}$$

where $p'_{cond}(t)$ and $p'_{sw}(t)$, are the average conduction losses and average switching losses at each switching period, respectively. The switching losses can be divided into turn-on losses $p'_{on}(t)$ and turn-off losses $p'_{off}(t)$ which are both caused during the commutation process of the controlled device and generally exhibit significant dissipation values in hard commutation type or low dissipation values in soft commutation type. On the other hand, the blocking losses may usually be neglected because of the small leakage current of the device in its off state.

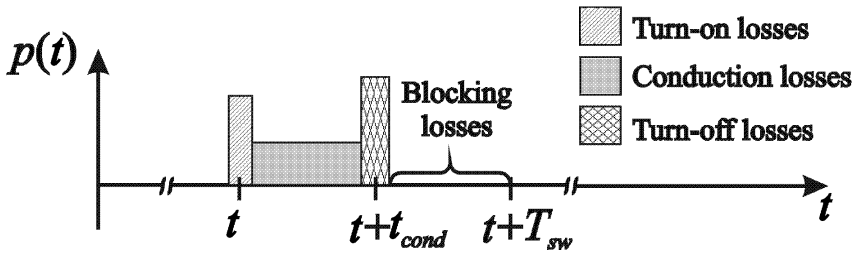


Figure 4-1 Schematic instantaneous power losses in a T_{sw} interval

Averaging (4.2) over a cycle of the output current, the total average power losses can be obtained:

$$\overline{P}(t) \cong \frac{1}{T}\int_0^T p'_{cond}(t)dt + \frac{1}{T}\int_0^T p'_{on}(t)dt + \frac{1}{T}\int_0^T p'_{off}(t)dt \tag{4.3}$$

The conduction losses are due to the voltage drop of each device $V(t)$ as the controlled switch or diode carries current $I(t)$ in the on state interval (t_{cond}). Thus, the average conduction losses in each switching period can be described as follows:

$$p'_{cond}(t) = \frac{1}{T_{sw}}\int_t^{t+T_{sw}} V(t)I(t)dt \cong \frac{1}{T_{sw}}\int_t^{t+t_{cond}} V(t)I(t)dt = V(t)I(t)\frac{t_{cond}}{T_{sw}} \tag{4.4}$$

$V(t)$ and $I(t)$ can be considered constant during the conduction time interval for inductive loads, if it is assumed that the T_{sw} cycle is infinitely small compared to T. In

addition, it can be considered that the device current is equal to the fundamental output current of the converter.

The switching power losses are associated to the power dissipation peaks generated during both switching transitions on-off and off-on. These power dissipation peaks correspond to the product of the device voltage drop and current during the switching transient (Δt_{on} during the turn-on transition and Δt_{off} during the turn-off transition). The area under the power dissipation waveform during the turn-on transition is defined as the dissipated turn-on energy (E_{on}). In analogous way, the dissipated turn-off energy (E_{off}) is described. The average turn-on and turn-off losses between t and $t+T_{sw}$ can be calculated as:

$$p'_{on}(t) = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} V(t)I(t)dt = \frac{1}{T_{sw}} \int_{t}^{t+\Delta t_{on}} V(t)I(t)dt \cong \frac{1}{T_{sw}} E_{on}(t) \tag{4.5}$$

$$p'_{off}(t) = \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} V(t)I(t)dt = \frac{1}{T_{sw}} \int_{t}^{t+\Delta t_{off}} V(t)I(t)dt \cong \frac{1}{T_{sw}} E_{off}(t) \tag{4.6}$$

Now, the total average power losses for a given power device are calculated by substituting expressions (4.4), (4.5) and (4.6) in (4.3):

$$\overline{P}(t) \cong \underbrace{\frac{1}{T}\int_{0}^{T} V(t)I(t)\frac{t_{cond}}{T_{sw}}dt}_{conduction losses} + \underbrace{\frac{1}{T}\int_{0}^{T} \frac{1}{T_{sw}} E_{on}(t)dt + \frac{1}{T}\int_{0}^{T} \frac{1}{T_{sw}} E_{off}(t)dt}_{switching losses} \tag{4.7}$$

The static and dynamic characterisation of the power devices will feed the conduction and switching losses terms of (4.7), respectively. The device characterisation was covered in the chapter 3.

Attention must be paid with the energy losses associated with the matrix converter case since they are voltage and current dependent at any time instant, and both vary throughout the T period [88]. In contrast, for the VSI converters, the losses are only current dependent since the commutation voltage is constant and imposed by the DC bus. A typical VSI converter is chosen to introduce the power losses estimation by means of the proposed computation method.

4.3 Power Losses Evaluation Method for a VSI

The schematic circuit of a VSI is depicted in Figure 4-2. Because of the symmetrical structure of the inverter circuit, the current and voltage characteristics for IGBT and diodes, which are time-shifted, will turn out to be identical. Therefore, it is enough to consider just one IGBT (for example Z_{1A}) and one diode (for example D_{2A}) to calculate the VSI power losses.

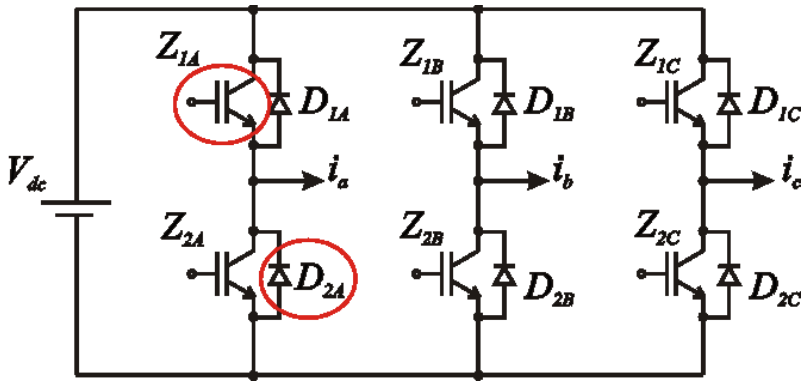


Figure 4-2 Three-phase VSI circuit schematic

In Figure 4-2, V_{dc} is the DC link voltage, $i_a(t)$, $i_b(t)$ and $i_c(t)$ are the output currents for each respective output phase. The current flows through Z_{1A} and through the opposite diode D_{2A} during the first half cycle of the fundamental output current (T) as shown in Figure 4-3. During the other half cycle, Z_{1A} is off, and only its parallel D_{1A} diode works. Consequently, it is only necessary to calculate the power losses during half a period of T, in order to obtain the total power losses of the IGBTs and the diodes of a VSI.

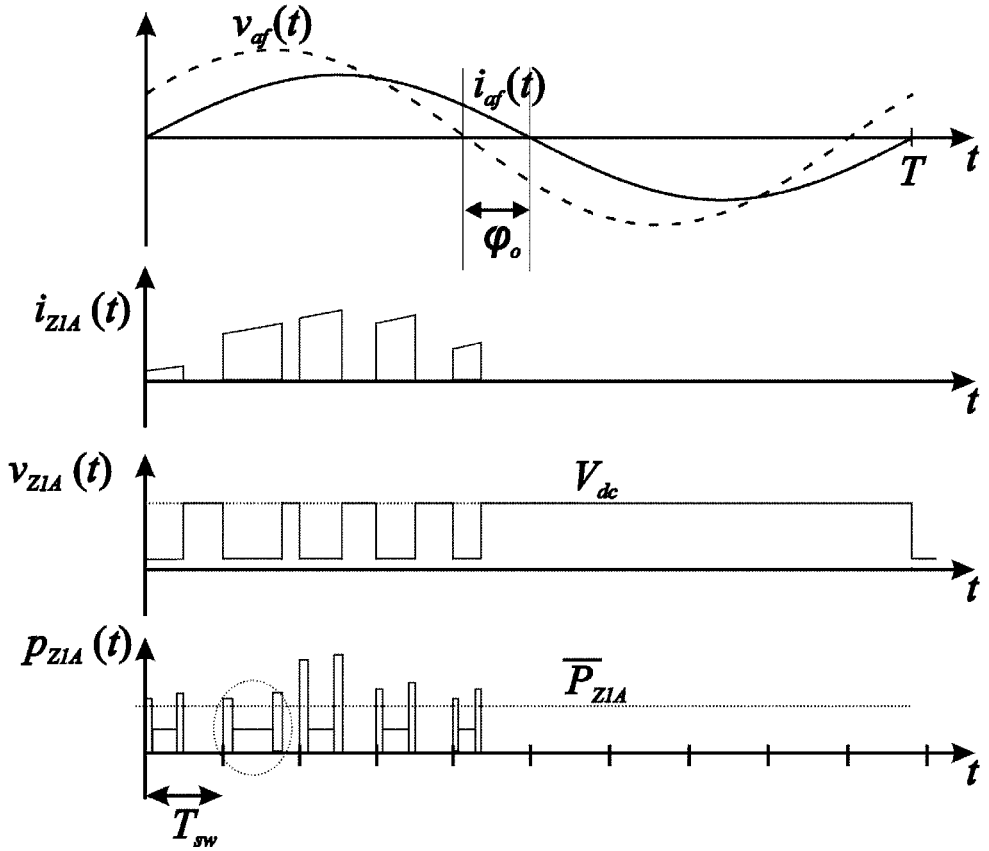


Figure 4-3 Schematic waveforms of Z1A IGBT within the converter a-phase

In Figure 4-3, $v_{af}(t)$ and $i_{af}(t)$ are the output fundamental *a*-phase corresponding to voltage and current respectively, φ_o is the load power factor, $v_{Z1A}(t)$ is voltage across IGBT Z_{1A}, $i_{Z1A}(t)$ is the current through IGBT Z_{1A}, $\overline{P}_{Z1A}$ is the total average Z_{1A} power dissipation. The Z_{1A} instantaneous dissipated power $p_{Z1A}(t)$ can be expressed following (4.2):

$$p_{Z1A}(t) \approx p_{cond/Z1A}(t) + p_{sw/Z1A}(t) = p_{cond/Z1A}(t) + p_{on/Z1A}(t) + p_{off/Z1A}(t) \qquad (4.8)$$

where $p_{cond/Z1A}(t)$, $p_{on/Z1A}(t)$ and $p_{off/Z1A}(t)$ are the average conduction, turn-on and turn-off losses in each switching period, respectively.

As it can be appreciated in Figure 4-3, other simplifications such as: linear modulation of the converter and negligible dead times have been assumed in order to calculate the power dissipation in both devices. In order to define the reference system taken into account in Figure 4-3, time $t = 0$ is defined when $i_{af}(t) = 0$ and takes a positive value.

4.3.1IGBT Conduction Losses

The conduction power losses of the IGBT are due to the forward voltage drop and by the current through it during the time it is active. Figure 4-4 represents the conduction dissipation in a T_{sw} cycle due to the IGBT on-state condition.

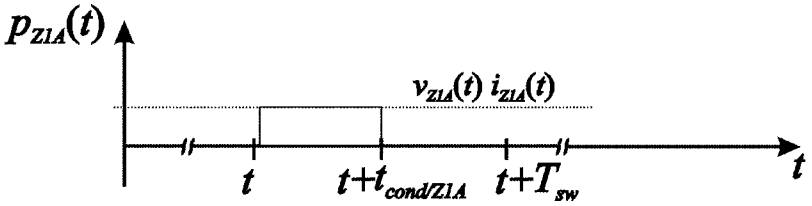


Figure 4-4 Schematic conduction losses in a T_{sw} period

where $t_{cond/Z1A} = T_{sw} D_Z(t)$ is the conduction time of the IGBT and $D_Z(t)$ is the IGBT duty cycle [89] that can be denoted by:

$$D_Z(t)=\frac{1}{2}\left[1+M\,sin(\omega_o t+\varphi_o)\right] \tag{4.9}$$

where M is the modulation depth index whose value is between 0 and 1, and ω_o is the output frequency pulsation. The average conduction losses in each switching period, $p_{cond/Z1A}(t)$, can be expressed by:

$$p_{cond/Z1A}(t)\approx\frac{1}{T_{sw}}\int_{t}^{t+T_{sw}} v_{Z1A}(t)\,i_{Z1A}(t)\,dt=\frac{1}{T_{sw}}\int_{t}^{t+t_{cond/Z1A}} v_{Z1A}(t)\,i_{Z1A}(t)\,dt=v_{Z1A}(t)\,i_{Z1A}(t)\,D_Z(t) \tag{4.10}$$

where $v_{Z1A}(t)$ is the Z_{1A} on-state voltage and $i_{Z1A}(t)$ can be considered to be equal to the fundamental output current $i_{af}(t)$ during the $t_{cond/Z1A}$ interval if it is assumed that the T_{sw} cycle is infinitely small compared to T. Thus, $i_{Z1A}(t)$ can be expressed as:

$$i_{Z1A}(t)\approx i_{af}(t)=I_M\sin(\omega_o t) \tag{4.11}$$

where I_M is the output current amplitude. The fundamental output current is assumed to be sinusoidal. $v_{Z1A}(t)$ is retrieved from the general expression (3.3) of chapter 3 so that it can be written for Z_{1A} as:

$$v_{Z1A}(t)=V_{t/Z}+a_Z\,i_{Z1A}^{b_Z}(t) \tag{4.12}$$

In short, the average conduction power losses in each T_{sw} cycle derived from equation (4.10) can be finally described as:

$$p_{cond/Z1A}(t) \approx I_M \sin(\omega_o t)\left[V_{t/Z} + a_Z I_M^{b_z} \sin(\omega_o t)\right] 0.5\left[1 + M\sin(\omega_o t + \varphi_o)\right] \quad (4.13)$$

Averaging (4.13) over a half cycle of the output current, the total average conduction power losses $\overline{P}_{cond/Z1A}$ are obtained.

4.3.2IGBT Switching Losses

The switching power losses are associated to the power dissipation peaks generated during both switching transitions on-off and off-on. These power dissipation peaks correspond to the commutation voltage across Z_{1A} and the switch current during the switching transient (Δt_{on} during the turn-on transition and Δt_{off} during the turn-off transition) as shown in Figure 4-5. Thus, the average turn-on losses between t and $t+T_{sw}$ $p_{on/Z1A}(t)$ can be calculated as:

$$p_{on/Z1A}(t) \approx \frac{1}{T_{sw}} \int_{t}^{t+\Delta t_{on}} v_{Z1A}(t)\, i_{Z1A}(t)\, dt = \frac{E_{on/Z1A}(t)}{T_{sw}} \quad (4.14)$$

where the dissipated turn-on energy $E_{on/Z1A}(t)$ is defined as the area under the power dissipation peak during the turn-on transition.

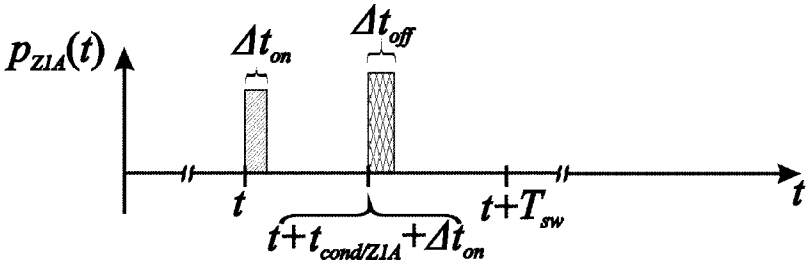


Figure 4-5 Schematic switching losses in a T_{sw} cycle

In analogous manner as the turn-on commutation, the average turn-off losses in a switching period $p_{off/Z1A}(t)$ can be expressed as:

$$p_{off/Z1A}(t) \approx \frac{1}{T_{sw}} \int_{t+t_{cond/Z1A}+\Delta t_{on}}^{t+t_{cond/Z1A}+\Delta t_{on}+\Delta t_{off}} v_{Z1A}(t)\, i_{Z1A}(t)\, dt = \frac{E_{off/Z1A}(t)}{T_{sw}} \quad (4.15)$$

where the dissipated turn-off energy $E_{off/Z1A}(t)$ is defined as the area under the power dissipation peak during the turn-off transition.

$E_{on/Z1A}(t)$ and $E_{off/Z1A}(t)$ are usually obtained by a curve fitting from measured data since energy depends only on the current. For the VSI converter, the initial or final commutation voltage value remains to a constant value near V_{dc} voltage. In contrast, in the matrix converter both energies are voltage and current dependent because there is not a constant DC link and the voltage across the devices evolves during an entire T period depending on the input phase voltages.

4.3.3 Total IGBT Power Losses

The instantaneous power losses of Z_{1A} can be now rewritten as:

$$p_{Z1A}(t) \approx v_{Z1A}(t)\, i_{Z1A}(t)\, D_Z(t) + \frac{E_{on/Z1A}(t)}{T_{sw}} + \frac{E_{off/Z1A}(t)}{T_{sw}} \tag{4.16}$$

The IGBT average power losses $\overline{P}_{Z1A}$ can be calculated by substituting expression (4.16) in (4.1):

$$\overline{P}_{Z1A} = \frac{1}{T}\int_0^T p_{Z1A}(t)\,dt = \underbrace{\frac{1}{T}\int_0^T (V_{t/Z} + a_Z\, i_{af}^{b_Z}(t))\, i_{af}(t)\, D_Z(t)\,dt}_{\overline{P}_{cond/Z1A}} + \underbrace{\frac{1}{T}\int_0^T \frac{E_{off/Z1A}(t)}{T_{sw}}dt}_{\overline{P}_{on/Z1A}} + \underbrace{\frac{1}{T}\int_0^T \frac{E_{off/Z1A}(t)}{T_{sw}}dt}_{\overline{P}_{off/Z1A}} \tag{4.17}$$

where $\overline{P}_{cond/Z1A}$, $\overline{P}_{on/Z1A}$ and $\overline{P}_{off/Z1A}$ are the average conduction, average turn-on and average turn-off power losses, respectively. In order to obtain the average value, it is only necessary to integrate over half output current period as it is derived from Figure 4-3. Finally, equation (4.17) is computed with MATLAB in order to obtain a numerical result as it is detailed in the implementation section.

4.3.4 Diode Conduction Losses

The schematic waveforms of the diode behaviour in a VSI are depicted in Figure 4-6. During the first half cycle of the output current, the diode D_{2A} takes over the current from Z_{1A}. During the other half cycle, the opposite diode (D_{1A}) is the operating diode. Lets defined the waveforms involved in the D_{2A} power dissipation: $v_{D2A}(t)$ is voltage across diode D_{2A}, $i_{D2A}(t)$ is the current through this diode, $p_{D2A}(t)$ is the D_{2A} instantaneous dissipated power and $\overline{P}_{D2A}$ is the total average power dissipation. The D_{2A}

instantaneous dissipated power $p_{D2A}(t)$ is due to the contribution of the conduction losses, the switching losses and the blocking losses. The turn-on and blocking losses have been neglected in this analysis because of their minor contribution to the total power dissipation [87]. In this way, there are only two kinds of power losses to be considered: the conduction and the turn-off losses. The turn-off losses are caused by the recovery characteristic of the diode.

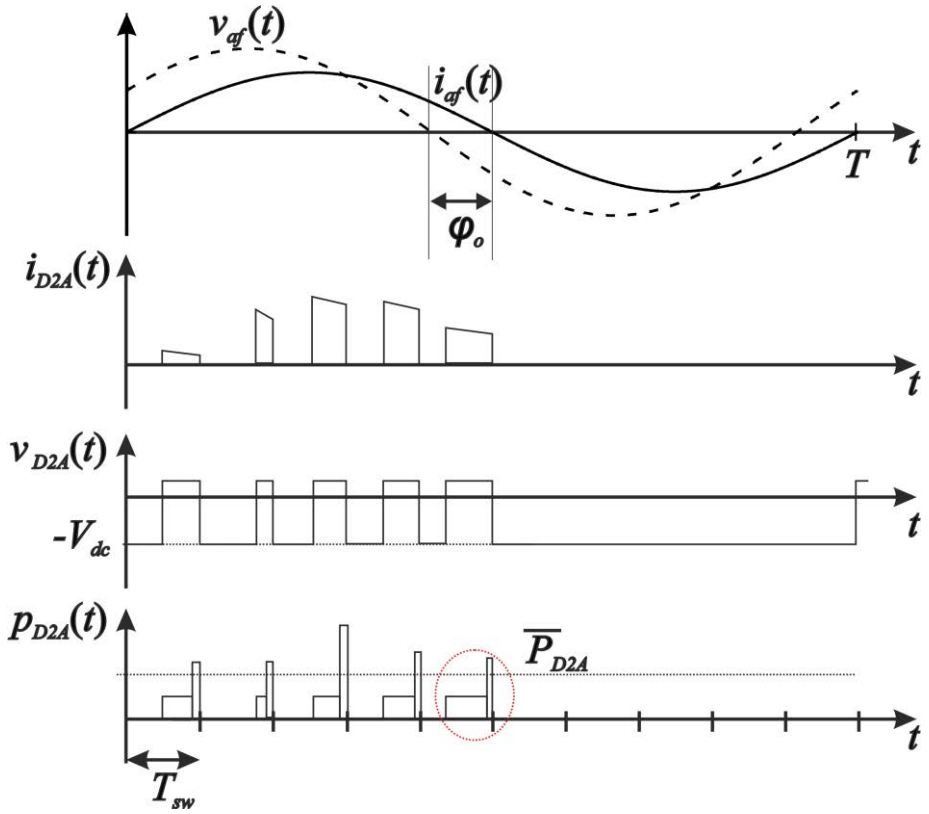


Figure 4-6 Schematic waveforms of D_{2A} diode within the converter a-phase

A detail of the D_{2A} schematic instantaneous dissipated power can be appreciated in Figure 4-7.

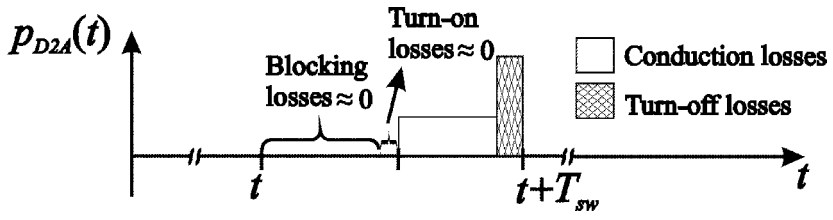


Figure 4-7 Schematic instantaneous power losses in a $t+T_{sw}$ interval

Assuming the same approach used for the IGBT, $p_{D2A}(t)$ can be described as:

$$p_{D2A}(t) \approx p_{cond/D2A}(t) + p_{sw/D2A}(t) = p_{cond/D2A}(t) + p_{off/D2A}(t) \tag{4.18}$$

where $p_{cond/D2A}(t)$ and $p_{off/D2A}(t)$ are the average conduction losses and turn-off losses in each switching period, respectively. They will be calculated following the same procedure as for the IGBT. All the diode nomenclature and approximations are analogous to the IGBT case.

The conduction power dissipation is caused by the on-state voltage drop of D_{2A} and the current carried by it during the time D_{2A} is active. The conduction losses due to the diode on-state behaviour are schematically depicted in Figure 4-8.

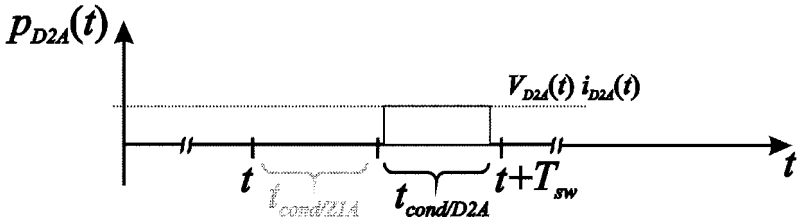


Figure 4-8 Schematic conduction losses in a T_{sw} period

where $t_{cond/D2A} = T_{sw}(1 - D_Z(t))$ is the conduction time of such diode and $(1 - D_Z(t))$ is the diode duty cycle which is generally defined as $D_D(t)$ [89].

$$D_D(t) = \frac{1}{2}\left[1 - M\sin(\omega_o t + \varphi_o)\right] \tag{4.19}$$

It can be assumed that IGBT and diode conduction times are larger than the switching transition times. Thus, the average conduction losses in each switching period $p_{cond/D2A}(t)$ can be expressed by:

$$p_{cond/D2A}(t) \approx \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} v_{D2A}(t)\, i_{D2A}(t)\, dt = \frac{1}{T_{sw}} \int_{t+t_{cond/Z1A}}^{t+t_{cond/Z1A}+t_{cond/D2A}} v_{D2A}(t)\, i_{D2A}(t)\, dt = v_{D2A}(t)\, i_{D2A}(t)\, D_D(t) \tag{4.20}$$

where $i_{D2A}(t)$ can be considered the fundamental output current $i_{af}(t)$ and $v_{D2A}(t)$ is the on-state voltage drop across the diode, which can be represented by analogous expressions than for the IGBT.

$$V_{D2A}(t) = V_{t/D} + a_D\, i_{D2A}^{b_D}(t) \tag{4.21}$$

$$i_{D2A}(t) \approx i_{af}(t) = I_M \sin(\omega_o t) \tag{4.22}$$

where $V_{t/D}$, a_D and b_D may be obtained by curve-fitting the measured on-state voltage versus current characteristic as explained in chapter 3.

In short, the average conduction power losses in each T_{sw} period $p_{cond/D2A}(t)$ can be expressed after substituting (4.21) and (4.22) in (4.20) as:

$$p_{cond/D2A}(t) \approx I_M \sin(\omega_o t)\left[V_{t/D} + a_D\, I_M^{b_D} \sin(\omega_o t)\right] 0.5\left[1 - M\sin(\omega_o t + \varphi_o)\right] \tag{4.23}$$

4.3.5 Diode Switching Losses

The turn-off losses during the on-off switching transition (Δt_{rec}) are due to the reverse recovery behaviour of the diode. Figure 4-9 illustrates the schematic turn-off instantaneous power dissipation within a switching cycle $p_{off/D2A}(t)$, which can be evaluated as:

$$p_{off/D2A}(t) \approx \frac{1}{T_{sw}} \int_{t+t_{cond/Z1A}+t_{cond/D2A}}^{t+t_{cond/Z1A}+t_{cond/D2A}+\Delta t_{rec}} v_{D2A}(t)\, i_{D2A}(t)\, dt = \frac{E_{off/D2A}(t)}{T_{sw}} \tag{4.24}$$

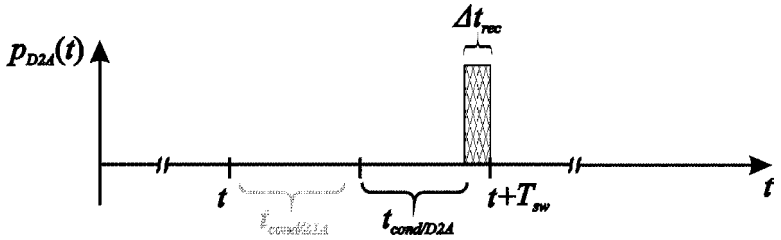


Figure 4-9 Schematic diode turn-off losses in the $t+T_{sw}$ interval

The diode energy losses are obtained by the same procedure applied for the IGBT as it is mentioned in the implementation section of this chapter.

4.3.6 Total Diode Power Losses

To sum up, the instantaneous power losses of D_{2A} can be approximated by:

$$p_{D2A}(t) \approx v_{D2A}(t)\, i_{D2A}(t)\, D_D(t) + \frac{E_{off/D2A}(t)}{T_{sw}} \tag{4.25}$$

Now, substituting expression (4.25) in (4.1), the diode average power losses ($\overline{P}_{D2A}$) result in:

$$\overline{P}_{D2A} = \frac{1}{T}\int_0^T p_{D2A}(t)\,dt = \underbrace{\frac{1}{T}\int_0^T (V_{t/D} + a_D\, i_{af}^{b_D}(t))\, i_{af}(t)\, D_D(t)\,dt}_{\overline{P}_{cond/D2A}} + \underbrace{\frac{1}{T}\int_0^T \frac{E_{off/D2A}(t)}{T_{sw}}\,dt}_{\overline{P}_{off/D2A}} \qquad (4.26)$$

where $\overline{P}_{cond/D2A}$ and $\overline{P}_{off/D2A}$ are the average conduction and the average turn-off power losses, respectively. In order to obtain the average value, it is only necessary to integrate over the half output current period as it is derived from Figure 4-6. Finally, equation (4.26) is computed with MATLAB in order to obtain a numerical result.

4.4 Implementation of the VSI Power Losses Calculation

Taking into consideration all these analytical expressions, which describe the IGBT and diode dissipated power, a numerical method to calculate the IGBT and diode power losses in a VSI is implemented using MATLAB. Once the presented approach is validated for the VSI, it will be extended to calculate the semiconductors power dissipation within a MC in the next chapters. Figure 4-10 illustrates the block diagram of the MATLAB script allowing the IGBT power losses computation, showing the input variables, losses components computation sub-blocks and output variables. An analogous block is built for the diode. The application-related parameters consist of: output current fundamental frequency (f_{out}); modulation depth index (M) [90]; rms output current amplitude (I_M); load power factor (cos φ_o) and switching frequency (f_{sw}). The inputs to the block are the on-state fitted parameters which are derived from the curve fitting of the device I-V characteristics (as explained in chapter 3) and the measured hard turn-on and turn-off energy losses ($E_{ON/Z1A}$) and ($E_{OFF/Z1A}$), respectively, as a function of the current (in the VSI case, the voltage across the device during the switching process is V_{dc}).

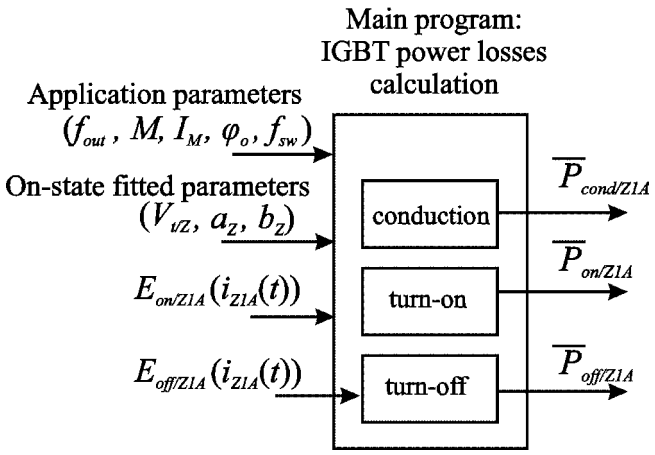


Figure 4-10 Block diagram of the power losses calculation script for a single IGBT within the VSI

The main program calls the conduction, turn-on and turn-off losses computation functions and the average value within the output period T of each power losses component is returned as an output. Each loss computation function performs first a one-dimensional fit of the measured energy losses (for instance Figure 4-11) to extract an energy loss value depending on the output current at each switching instant and second solves a numerical integration over the T period of the aforementioned expressions, (4.13) for the conduction losses, (4.14) and (4.15) for the switching losses, to calculate the corresponding average power dissipation.

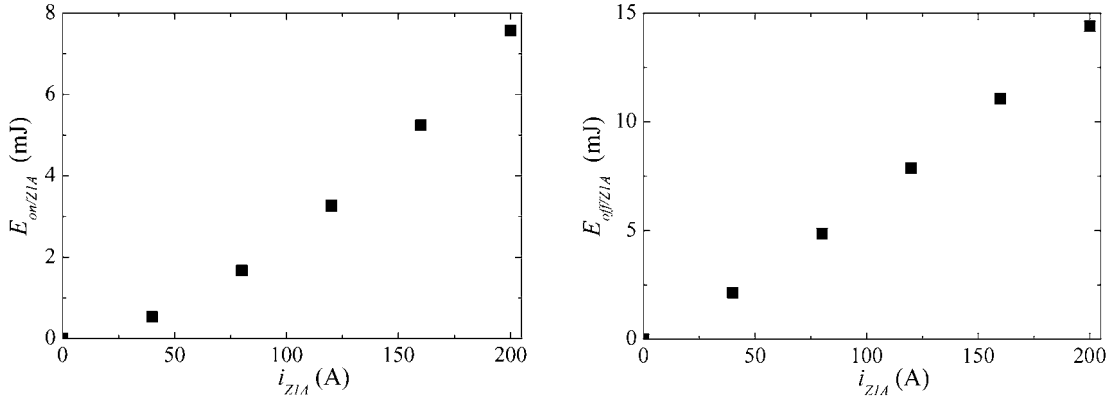


Figure 4-11 Measured data provided by [87]: a) $E_{on/Z1A}(t)$ versus $i_{Z1A}(t)$, b) $E_{off/Z1A}(t)$ versus $i_{Z1A}(t)$

The diode power calculation program consists of the conduction and turn-off functions as depicted in Figure 4-12. Both functions return the average conduction and average turn-off power losses, respectively.

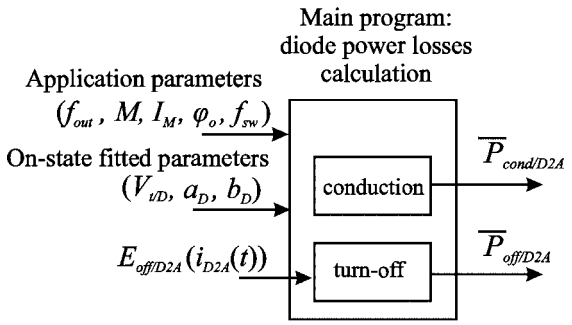


Figure 4-12 Block diagram of the power losses calculation script for a single diode within the VSI

Analogous to the IGBT case, once expressions (4.20) and (4.24) are obtained, integrating numerically over the T period, the average conduction and turn-off losses are determined.

4.4.1 Validation of the Power Losses Calculation Method

In order to validate the numerical method, the analysis of a VSI power losses carried out in [87] and based on analytical expressions is reproduced with the presented method. Measured turn-on and turn-off energy losses under certain test conditions as well as the modelling parameters of the IGBT and the diode switching losses can be found in [87] and are depicted in Table 4-1.

Application parameters			
Applied voltage	V_{dc}=320 V		
Output frequency	f_{out}=50 Hz		
Modulation depth	M=0.75		
Peak current	I_M=188.75 A		
Power factor	φ_o=0.74 rad		
Operating frequency	f_{sw}=20 kHz		
IGBT parameters		**Diode parameters**	
On-state	$V_{t/Z}$=0.875	On-state	$V_{t/D}$=0.80
	a_Z=0.028		a_D=0.005
	b_Z=0.745		b_D=1
Turn-on	h=1.21e^{-3} mJ	Turn-off	peak I_{rr}/I_f=1
	k=1.65		t_b=0.030μs
Turn-off	m=0.027 e^{-3} mJ		
	n=1.183		

Table 4-1 Test operating conditions and fitted parameters

The fitted parameters of Table 4-1 have been deduced from the following analytical expressions:

$$\begin{aligned} E_{on/Z1A}(t) &= h\, i_{Z1A}^{k}(t) \\ E_{off/Z1A}(t) &= m\, i_{Z1A}^{n}(t) \\ E_{off/D2A}(t) &= 0.5\, I_{rr}\, 0.5\, V_{dc}\, t_b \end{aligned} \tag{4.27}$$

where I_{rr} is the peak reverse recovery current, I_f is the forward current and t_b is the second half of the recovery time as it is defined in [91]. Table 4-2 summarises the comparison between the IGBT and diode power losses calculated through an analytical method that corresponds to [87] and the numerical method of this work.

	Power losses[W]	Analytical method	Numerical method	Deviation [%]
IGBT	Conduction	87.39	88.88	1.7
	Turn-on	37.01	37.40	1.05
	Turn-off	84.8	81.40	4
	Total losses	209.20	207.68	0.72
Diode	Conduction	25.33	22.88	9.67
	Turn-off	2.88	2.8	2.85
	Total losses	28.21	25.76	8.96

Table 4-2 Power losses comparison between the analytical method and the numerical implemented method

As it can be inferred from Table 4-2, the numerical method shows a reasonably good agreement with the method described in [87], with a maximum deviation below 10%. Nevertheless, the difference in the IGBT conduction losses between both methods is 1.5W and in case of the diode is 2.5W so there is a good match between them. In conclusion, the developed method derived from the instantaneous dissipated power approach of an IGBT and a diode as well as its implementation based on actual measured data can be extended for the more complex case of the MC.

4.5 Summary

The estimation of the power dissipation associated to the power devices within a power converter is a very important issue to take into account when the converter is designed. The survival of the converter depends on such estimation since an excessive dissipated heat in a power semiconductor could cause an irreversible damage in the component itself and drastically reduce the operative life of the converter. Thus, a computation method based on experimental values of the conduction and switching states of the device is presented to estimate their power losses within a VSI converter in first place. From this information, a numerical computation of the average power losses is performed, assuming that the switching frequency is higher than the fundamental one and that the instantaneous dissipated powers for each time t can be approximated by their mean value in the $t+T_{sw}$ switching period interval.

The power dissipation of a device is derived from the contribution of the conduction losses, the switching losses and the blocking losses. The switching losses can be divided into turn-on losses and turn-off losses which are both caused during the commutation process of the device and generally exhibit significant dissipation values. On the other hand, the blocking losses may usually be neglected because of the small leakage current in the off state of the device. The different power losses contributions are derived from their corresponding experimental waveforms. MATLAB is the tool used to numerically compute the devices power losses.

The implemented method has been successfully validated for the VSI case by comparing the power losses presented in reference [87] from analytical expressions with those computed using the numerical approach. In conclusion, the numerical method provides satisfactory results and it can be extended to the MC case. In the next step, chapter 5 will deal with the semiconductor power losses estimation within a typical three-phase to three-phase MC.

5. Evaluation of the Semiconductor Power Losses within Matrix Converters

Once the proposed losses computation method is validated with a VSI converter, it is now extended for the MC case. It is interesting for the converter designer having a tool to estimate the total average power losses associated with the power devices within a bidirectional switch as well as the entire converter depending on the operation parameters of the converter itself such as: modulation method, input and output frequency, input and output voltage, output current, switching frequency, load power factor, etc. Likewise, the power losses knowledge is required to carry out a proper thermal design of the converter leading to reasonable dimension of the thermal elements of the system i.e. heat-sink, fan, heat exchanger, etc. So, the proposed power losses computation method can become a useful tool to address all these issues. Moreover, the application of such a method will allow, for instance, adjusting the suitable switching frequency in order to avoid faults in the devices derived from thermal problems, selecting the proper power semiconductors for a given application.

Different modulation strategies can be applied to the MC to achieve sinusoidal output voltages and input currents as described in Appendix C. The modulation strategy dictates the instant time the bidirectional switch should commutate as well as its conduction time. This fact has a clear impact on the power losses so that two of the main practical solutions already used and demonstrated for the control of MCs, Venturini [92] and the double-sided space vector modulation (DS SVM) [18] are implemented to analyse their effect on the device power losses.

5.1 Matrix Converter Power Losses

The schematic circuit of a typical three-phase to three-phase MC acting as an induction motor drive in a possible application is depicted in Figure 5-1. $V_A(t)$, $V_B(t)$, $V_C(t)$ are the input phase voltages; $V_a(t)$, $V_b(t)$, $V_c(t)$ are the output phase voltages; $i_a(t)$, $i_b(t)$, $i_c(t)$ are the output phase currents with a time period T and S_{Aa} is the bidirectional switch connected between the input A-phase and the output a-phase. The study of the power losses is focused on the power device, in particular on the S_{Aa} bidirectional switch. Due to the symmetry of the MC topology and to the fact that we are analysing the sinusoidal regime of the converter, the same behaviour can be found

cyclically in the other IGBTs and diodes of other output phases. Concerning the configuration of the BDS, Figure 5-1 depicts a common emitter arrangement; analogous results can be obtained for the common collector configuration due to the symmetry of the BDS circuitry. Within the S_{Aa} BDS, it is only necessary to calculate the power losses during half a period T, for instance the positive one where Z_{Aa1} and D_{Aa1} are active, since the same behaviour will appear during the other half of the period, but involving the antiparallel IGBT and diode (Z_{Aa2} and D_{Aa2}). The different power losses expressions, which will appear along this section, follow analogous nomenclature as in the VSI case.

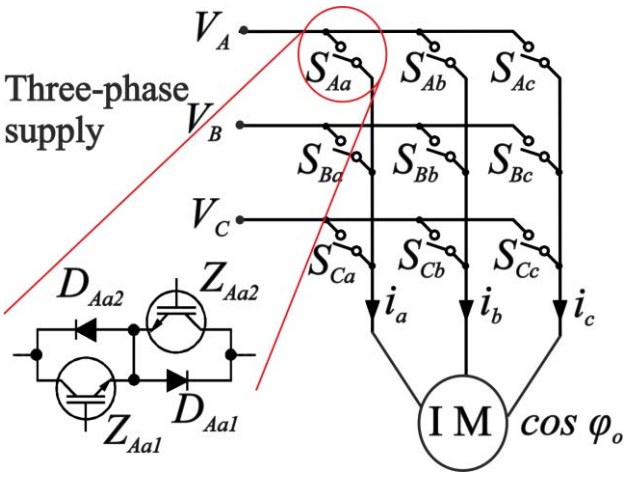


Figure 5-1 Typical three-phase to three-phase MC circuit topology implemented by nine BDSs (two IGBTs and two diodes in common emitter configuration) driving an AC machine of cos φ_o power factor

The basis of the MC power losses calculation follows the explanation given in chapter 4 section 4.2 as long as the converter switching frequency is much higher than the input and output frequencies. Accordingly to this, an estimated general expression for the instantaneous power of Z_{Aa1} can be formulated:

$$p_{ZAa1}(t) \approx p_{cond/ZAa1}(t) + p_{sw/ZAa1}(t) = p_{cond/ZAa1}(t) + p_{on/ZAa1}(t) + p_{off/ZAa1}(t) \qquad (5.1)$$

where $p_{cond/ZAa1}(t)$ are the average conduction power losses in each switching period, $p_{sw/ZAa1}(t)$ is defined as the average switching losses in each switching cycle, $p_{on/ZAa1}(t)$ and $p_{off/ZAa1}(t)$ are the average turn-on and turn-off losses in each switching cycle, respectively (due to hard and soft commutations).

The following assumptions have been also considered in order to calculate the power losses:

- blocking losses have been neglected due to the minor contribution on the total power losses.
- input voltages and output currents are sinusoidal and balanced, and contain negligible switching ripple.
- a four-step current commutation strategy is used.
- the Venturini and DS SVM modulations are the applied modulation algorithms.

5.1.1 Identification of the commutation types

The determination of the commutation regions (i.e. time interval where a type of switching is involved) is essential in order to evaluate the different components of the switching losses which take part in the Z_{Aa1} and D_{Aa1} instantaneous dissipated power. A schematic of the waveforms involved in the switching processes of Z_{Aa1} during the period T is shown in Figure 5-2. $V_{AB}(t)$ and $V_{AC}(t)$ are the A to B and A to C line to line input voltages, respectively, $v_{af}(t)$ and $i_{af}(t)$ are the a-phase voltage and current output fundamentals respectively, $v_{ZAa1}(t)$ and $i_{ZAa1}(t)$ are the instantaneous voltage across and current through IGBT Z_{Aa1}, $i_{DAa1}(t)$ current through diode D_{Aa1} and $\overline{P}_{ZAa1}$ is the total average Z_{Aa1} power dissipation. The Z_{Aa1} instantaneous dissipated power $p_{ZAa1}(t)$ is due to the contribution of the conduction and switching losses. All kind of commutation processes given in Z_{Aa1} can be identified in Figure 5-2. In this way, H_{OFF} region corresponds to the commutations characterised by a hard turn-off with $V_{AB}(t) > 0$ and $i_{af}(t) > 0$, H_{ON} region involves hard turn-on commutations with $V_{AC}(t) > 0$ and $i_{af}(t) > 0$, S_{ON} region denotes soft turn-on switching with $V_{AC}(t) < 0$ and $i_{af}(t) > 0$ and S_{OFF} region indicates soft turn-off processes of Z_{Aa1} with $V_{AB}(t) < 0$ and $i_{af}(t) > 0$. These commutation scenarios depend on the relative input voltages which are applied across a BDS and the direction of the current through itself as it was discussed in chapter 2. Thus, in the S_{Aa} case, $V_{AB}(t)$ and $V_{AC}(t)$ play an important role in the S_{Aa} commutation phenomena. During the first half output period, the current flows through a series combination of Z_{Aa1} and D_{Aa1} following the pattern, which is provided by the respective modulation strategies [73].

The voltage across Z_{Aa1} evolves with the input voltages during T period. As it is appreciated in Figure 5-2, in the instant t_1, $V_{AC}(t_1)$ voltage is being blocked by Z_{Aa1} during the turn-on transition and $V_{AB}(t_1)$ voltage is being blocked during the turn-off

transition. On the other hand, in the instant t_2 of Figure 5-2, no voltage can be blocked by Z_{Aa1} during the turn-on transition, since $V_{AC}(t_2)$ is negative. D_{Aa1} is standing $V_{AC}(t_2)$ voltage. Nevertheless, $V_{AB}(t_2)$ voltage is being blocked by Z_{Aa1} in the turn-off transition.

According to the voltage across S_{Aa} and the current through it, Z_{Aa1} exhibits the types of commutations throughout T period shown in Table 5-1. During the other half cycle, the Z_{Aa1} is *off*, and its complementary IGBT and diode (Z_{Aa2} and D_{Aa2}) carries the current from the load to the input supply.

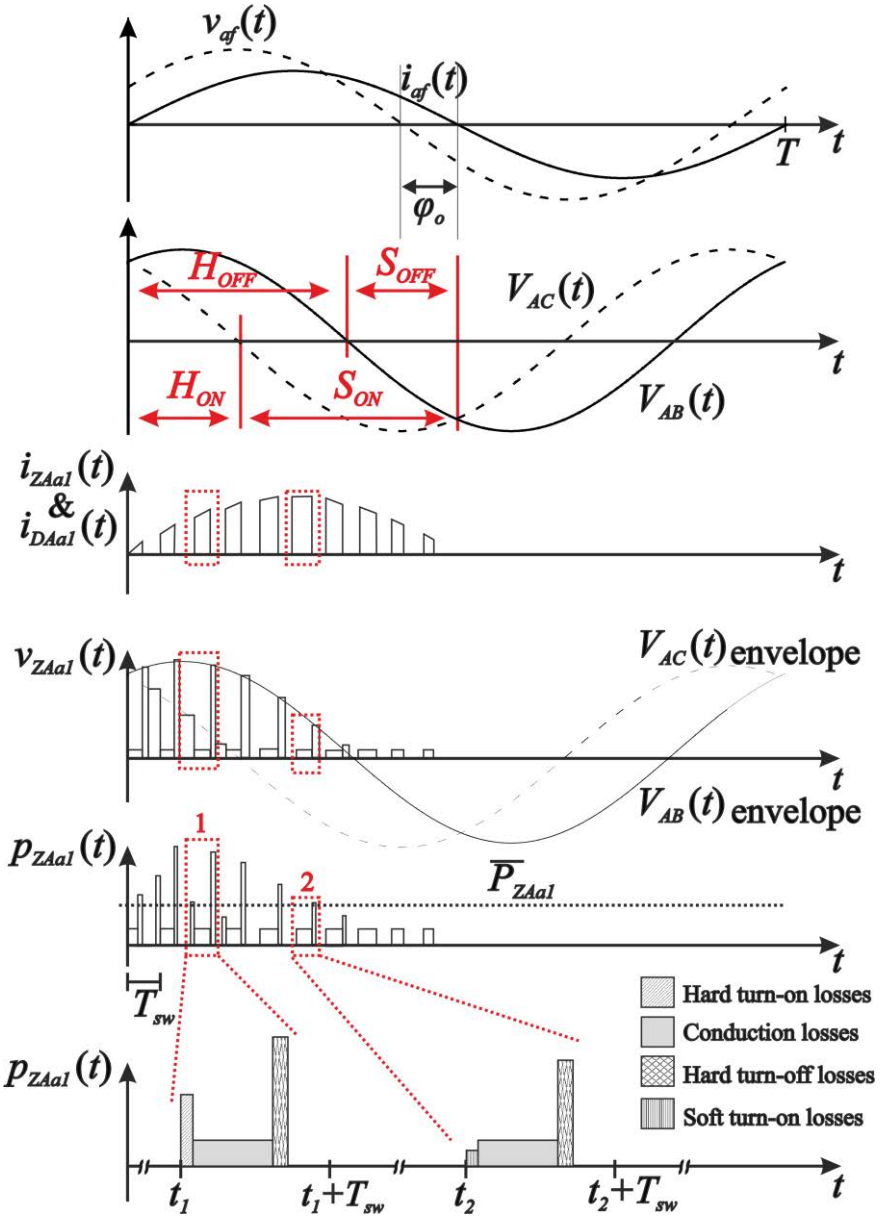


Figure 5-2 Schematic waveforms of the Z_{Aa1} commutation processes within T period

Commutation	Relative input voltages	Current direction	Commutation type
S_{Aa} BDS → S_{Ba} BDS	$V_{AB}(t) > 0$	$i_{af}(t) > 0$	H_{OFF}
	$V_{AB}(t) < 0$		S_{OFF}
S_{Ca} BDS → S_{Aa} BDS	$V_{AC}(t) > 0$		H_{ON}
	$V_{AC}(t) < 0$		S_{ON}

Table 5-1 Z_{Aa1} commutation processes

The identification of these commutation regions is essential in order to evaluate the different components of the switching losses which take part in the Z_{Aa1} instantaneous power losses.

5.1.2IGBT Conduction Losses

The output *a*-phase is connected to each input phase for a certain time during each switching interval. Hence, i_{SAa} (t), i_{SBa} (t), i_{SCa} (t) (current through S_{Aa}, S_{Ba} and S_{Ca} respectively) flow in turn to output *a*-phase during the switching cycle. The average conduction losses of Z_{Aa1} in each switching period can be calculated as:

$$p_{cond/ZAa1}(t) \approx \frac{1}{T_{sw}} \int_{t}^{t+T_{sw}} v_{ZAa1}(t) i_{ZAa1}(t) dt = \frac{1}{T_{sw}} \int_{t}^{t+t_{Aa}} v_{ZAa1}(t) i_{ZAa1}(t) dt = v_{ZAa1}(t) i_{SAa}(t) D_{Aa}(t) \tag{5.2}$$

where v_{ZAa1} (t) can be approached as the on-state voltage during the conduction interval, t_{Aa} is the time Z_{Aa1} is conducting, and D_{Aa} (t) is the duty cycle which can be approximated by the duty cycle of S_{Aa}. i_{SAa} (t) can be considered equal to the fundamental output current $i_{af}(t)$ whenever T is large compared to T_{sw} cycle. Integrating (5.2) during half an output current cycle, the total average conduction power losses in Z_{Aa1} is obtained. The IGBT average conduction losses per output *a*-phase can be calculated as the contribution of the devices connected to this phase (Z_{Aa1}, Z_{Ba1} and Z_{Ca1}).

5.1.3IGBT Switching Losses

The switching losses for the MC are dependent on the voltage across and current through the device as well as the applied current commutation strategy and the modulation method. As it is summarized in Table 5-1, different commutation types may

occur in the switching power device [68] when the current switches from one bidirectional switch to another one as represented in Figure 5-3. Thereby, if attention is paid in the S_{Ca} to S_{Aa} transition as illustrated in Figure 5-2 and zoomed in Figure 5-3a, $v_{ZAa1}(t_1)$ is roughly $V_{AC}(t_1)$ at t_1 instant. As a consequence of this, Z_{Aa1} involves a hard turn-on commutation (Figure 5-3c), while Z_{Ca1} involves a soft turn-off. Whereas $V_{AC}(t_1)$ voltage is positive, Z_{Aa1} device exhibits a hard turn-on commutation. On the contrary, when $V_{AC}(t_1)$ polarity is negative, a soft turn-on commutation is undergone by Z_{Aa1} since D_{Aa1} blocks all this voltage and hence the commutation is undergone at a very low voltage leading to low power dissipation.

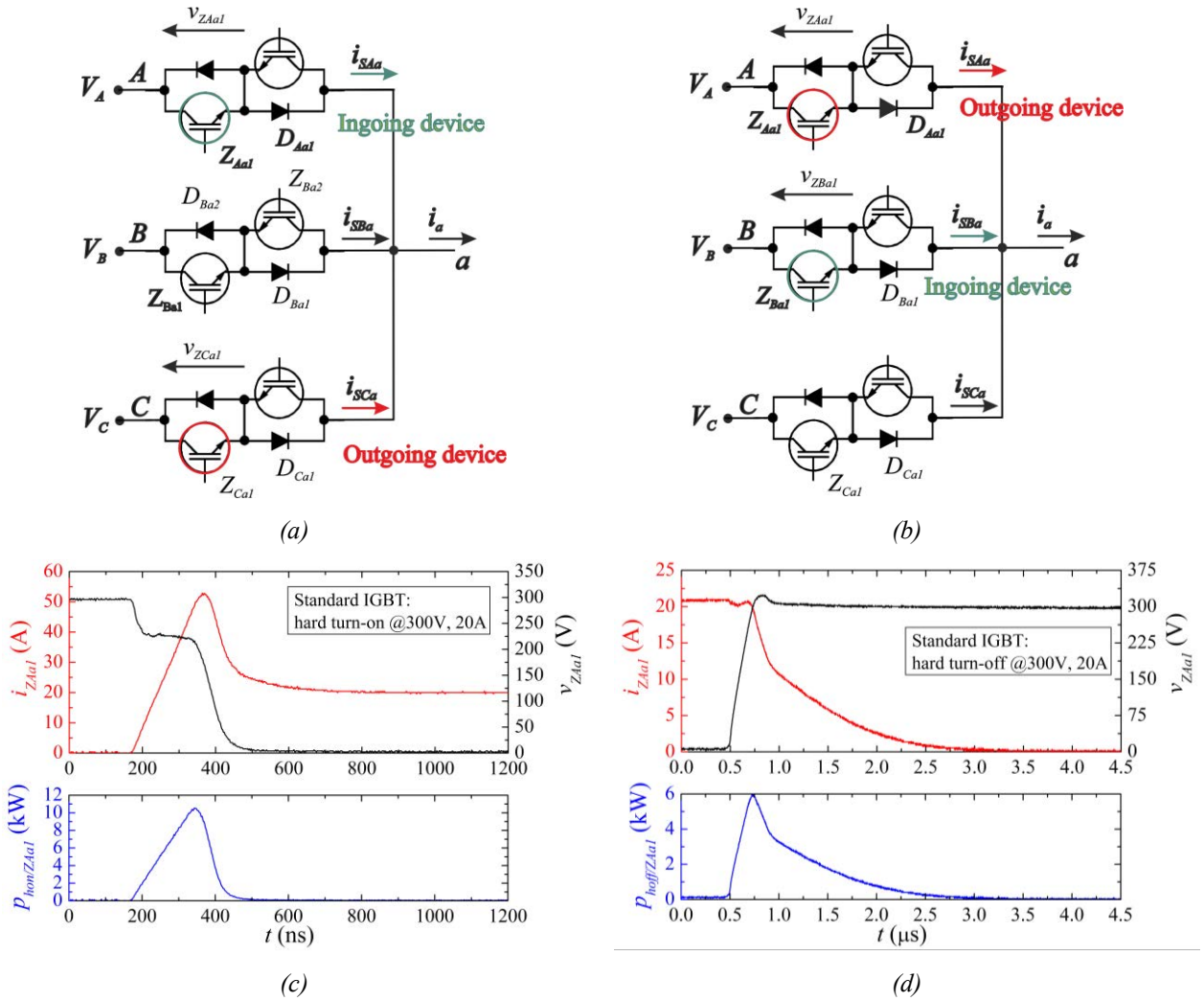
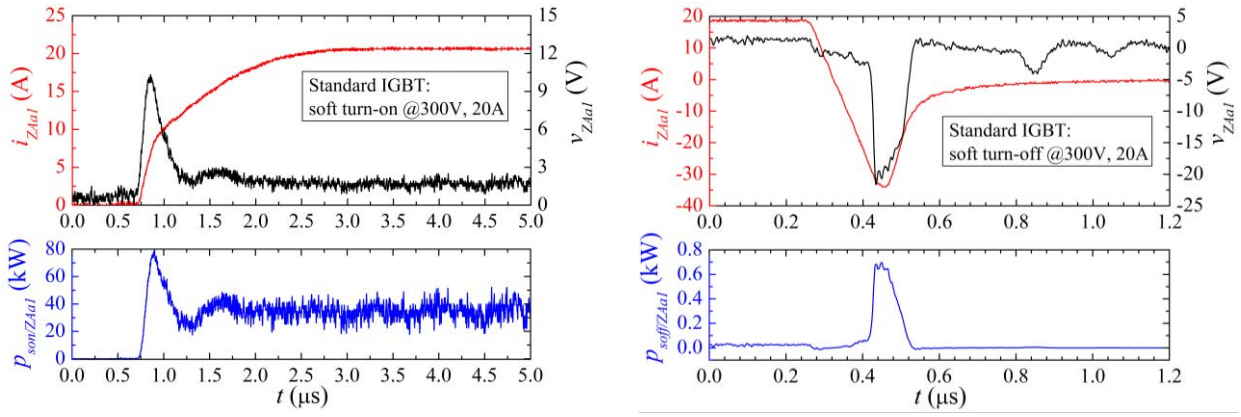


Figure 5-3 a) S_{Ca} to S_{Aa} commutation, b) S_{Aa} to S_{Ba} commutation, c) measured IGBT hard turn-on and d) hard turn-off switching waveforms and associated losses of BDS 1-6

On the other hand, at the instant of the switching transition from S_{Aa} to S_{Ba} as illustrated in Figure 5-3b, $v_{ZAa1}(t_1+t_{Aa}+\Delta t_{on})$ is approximately $V_{AB}(t_1+t_{Aa}+\Delta t_{on})$ voltage.

In this commutation instant, Z_{Aa1} involves a hard turn-off (Figure 5-3d), while Z_{Ba1} involves a soft turn-on. The hard turn-off commutation phenomenon is caused only if $V_{AB}(t_1)$ voltage is positive. When $V_{AB}(t)$ polarity is the opposite, a soft turn-off commutation is involved in Z_{Aa1} since the commutation takes place at low voltage as appreciated in Figure 5-4a. Therefore, this leads to very low power losses. On the other hand, when $V_{AC}(t)$ polarity is negative, a soft turn-off commutation is undergone in Z_{Aa1}. Moderate high power losses during a very short time are experimented by Z_{Aa1}.



(a) *(b)*

Figure 5-4 Measured IGBT switching waveforms and associated losses of BDS 1-6 a) Soft turn-on, b) soft turn-off

The target of this study is not only focused on hard switching phenomena [93] but also on the soft switching ones in order to analyse the influence of all components on the total power losses. Therefore, it is important to understand all BDS switching phenomena within a MC. This issue has been addressed with a MC simulation under true operation conditions [94]. The switching procedures of the IGBTs and diodes involved in the commutation are discussed in detail.

IGBT switching losses are formulated following the losses expressions derived from chapter 4, but for the MC case:

- $p_{hon/ZAa1}(t)$ are the average hard turn-on losses between t and $t+T_{sw}$. They can be calculated as:

$$p_{hon/ZAa1}(t) \approx \frac{1}{T_{sw}} \int_{t}^{t+\Delta t_{on}} v_{ZAa1}(t)\, i_{ZAa1}(t)\, dt = \frac{E_{hon/ZAa1}(V_{AC}(t), i_{af}(t))}{T_{sw}} \qquad (5.3)$$

$$for\ V_{AC}(t) > 0\ and\ i_{af}(t) > 0$$

where $E_{hon/ZAa1}$ is the dissipated hard turn-on energy.

- $p_{son/ZAa1}(t)$ are the average soft turn-on losses between t and $t+T_{sw}$. They can be calculated as:

$$p_{son/ZAa1}(t) \approx \frac{1}{T_{sw}} \int_{t}^{t+\Delta t_{on}} v_{ZAa1}(t)\, i_{ZAa1}(t)\, dt = \frac{E_{son/ZAa1}(V_{AC}(t), i_{af}(t))}{T_{sw}} \quad \text{for } V_{AC}(t) < 0 \text{ and } i_{af}(t) > 0 \tag{5.4}$$

where $E_{son/ZAa1}$ is the dissipated soft turn-on energy.

- $p_{hoff/ZAa1}(t)$ are the average hard turn-off losses between t and $t+T_{sw}$. They can be estimated as:

$$p_{hoff/ZAa1}(t) \approx \frac{1}{T_{sw}} \int_{t+t_{Aa}+\Delta t_{on}}^{t+t_{Aa}+\Delta t_{on}+\Delta t_{off}} v_{ZAa1}(t)\, i_{ZAa1}(t)\, dt = \frac{E_{hoff/ZAa1}(V_{AB}(t), i_{af}(t))}{T_{sw}} \quad \text{for } V_{AB}(t) > 0 \text{ and } i_{af}(t) > 0 \tag{5.5}$$

where $E_{hoff/ZAa1}$ is the dissipated hard turn-off energy.

- $p_{soff/ZAa1}(t)$ are the average soft turn-off losses between t and $t+T_{sw}$. They can be calculated as:

$$p_{soff/ZAa1}(t) \approx \frac{1}{T_{sw}} \int_{t+t_{Aa}+\Delta t_{on}}^{t+t_{Aa}+\Delta t_{on}+\Delta t_{off}} v_{ZAa1}(t)\, i_{ZAa1}(t)\, dt = \frac{E_{soff/ZAa1}(V_{AB}(t), i_{af}(t))}{T_{sw}} \quad \text{for } V_{AB}(t) < 0 \text{ and } i_{af}(t) > 0 \tag{5.6}$$

where $E_{soff/ZAa1}$ is the dissipated hard turn-on energy.

The analytical description presented for each power losses component of Z_{Aa1} can be also applied in analogous way to other IGBTs taking into account the corresponding voltage across and current through the device.

5.1.4Total IGBT Power Losses

At this time, the instantaneous power losses of Z_{Aa1} (5.1) can be rewritten as:

$$p_{ZAa1}(t) \approx v_{ZAa1}(t)\, i_{Aa}(t)\, D_{Aa}(t) + \frac{E_{hon/ZAa1}(t)}{T_{sw}} + \frac{E_{hoff/ZAa1}(t)}{T_{sw}} + \frac{E_{son/ZAa1}(t)}{T_{sw}} + \frac{E_{soff/ZAa1}(t)}{T_{sw}} \tag{5.7}$$

Finally, the IGBT average power losses ($\overline{P}_{ZAa1}$) can be calculated by substituting the obtained instantaneous power approach of Z_{Aa1} in expression (4.1):

$$\overline{P}_{ZAa1}=\frac{1}{T}\int_0^T p_{ZAa1}(t)\,dt=\underbrace{\frac{1}{T}\int_0^T v_{ZAa1}(t)\,i_{Aa}(t)\,D_{Aa}(t)\,dt}_{\overline{P}_{cond/ZAa1}}+\underbrace{\frac{1}{T}\int_0^T \frac{E_{hon/ZAa1}(t)}{T_{sw}}dt}_{\overline{P}_{hon/ZAa1}}+\underbrace{\frac{1}{T}\int_0^T \frac{E_{hoff/ZAa1}(t)}{T_{sw}}dt}_{\overline{P}_{hoff/ZAa1}}+$$
$$\underbrace{\frac{1}{T}\int_0^T \frac{E_{son/ZAa1}(t)}{T_{sw}}dt}_{\overline{P}_{son/ZAa1}}+\underbrace{\frac{1}{T}\int_0^T \frac{E_{soff/ZAa1}(t)}{T_{sw}}dt}_{\overline{P}_{soff/ZAa1}} \tag{5.8}$$

where $\overline{P}_{cond/ZAa1}$, $\overline{P}_{hon/ZAa1}$, $\overline{P}_{hoff/ZAa1}$, $\overline{P}_{son/ZAa1}$ and $\overline{P}_{soff/ZAa1}$ are the average conduction, hard turn-on, hard turn-off, soft turn-on and soft turn-off power losses, respectively.

5.1.5Diode Conduction Power Losses

The schematic waveforms of the diodes connected to *a*-phase (D_{Aa1}, D_{Ba1} and D_{Ca1}) are depicted in Figure 5-5. The D_{Aa1} instantaneous power dissipation $p_{DAa1}(t)$ is due to the contribution of the conduction losses, the switching losses and the blocking losses. Assuming the same approach used for the IGBT, D_{Aa1} instantaneous power losses can be described as:

$$p_{DAa1}(t)\approx p_{cond/DAa1}(t)+p_{sw/DAa1}(t)=p_{cond/DAa1}(t)+p_{on/DAa1}(t)+p_{off/DAa1}(t) \tag{5.9}$$

where $p_{cond/DAa1}(t)$ represents the average conduction losses in each switching period, $p_{sw/DAa1}(t)$ is defined as the average switching losses in each switching cycle, $p_{on/DAa1}(t)$ and $p_{off/DAa1}(t)$ are the average turn-on and turn-off losses in each switching cycle due to hard and soft commutations, respectively.

The average conduction losses of D_{Aa1}, $p_{cond/DAa1}(t)$, can be described as:

$$p_{cond/DAa1}(t)\approx\frac{1}{T_{sw}}\int_t^{t+T_{sw}} v_{DAa1}(t)\,i_{DAa1}(t)\,dt=\frac{1}{T_{sw}}\int_t^{t+t_{Aa}} v_{DAa1}(t)\,i_{DAa1}(t)\,dt=v_{DAa1}(t)\,i_{SAa}(t)\,D_{Aa}(t) \tag{5.10}$$

where $i_{DAa1}(t)$ and $v_{DAa1}(t)$ are the current through and the voltage across D_{Aa1}, respectively. $i_{SAa}(t)$ can be considered equal to the fundamental output current $i_{af}(t)$. The diode average conduction losses per output *a*-phase will be due to the contribution of the devices connected to this phase (D_{Aa1}, D_{Ba1} and D_{Ca1}).

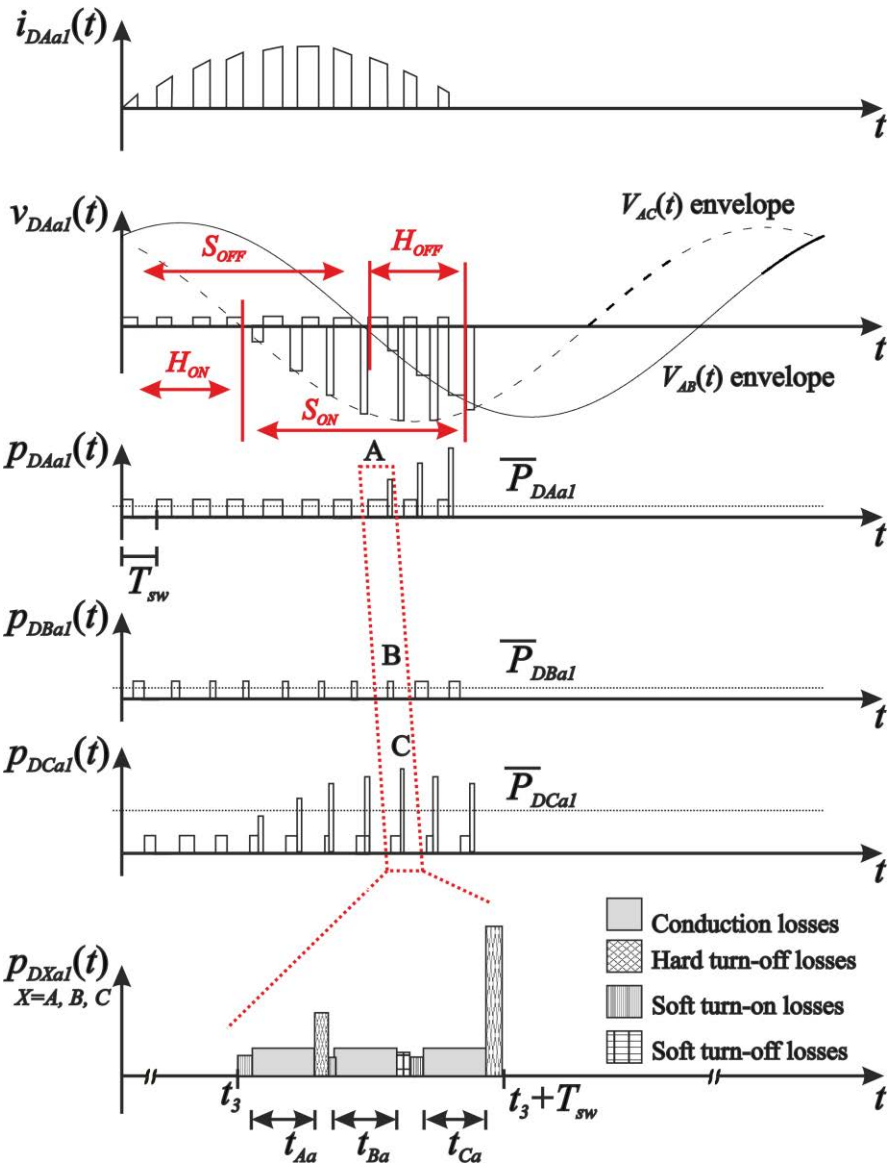


Figure 5-5 Schematic waveforms of the commutation processes within T period of the diodes connected to output a-phase

5.1.6Diode Switching Losses

As it is represented in detail in the waveforms of Figure 5-5, different kinds of commutations are involved in D_{Aa1}, D_{Ba1} and D_{Ca1}. $V_{DAa1}(t)$ evolves depending on the $V_{AB}(t)$ and $V_{AC}(t)$ voltages as shown in Figure 5-5. Thereby, if both voltages are positive,

the value of $V_{DAa1}(t)$ is almost negligible in the switching transitions, because the IGBT is able to block these voltages. But, if for instance $V_{AC}(t)$ has a negative value and a turn-on is demanded in S_{Aa}, D_{Aa1} is blocking such voltage since Z_{Aa1} cannot provide any reverse blocking capability. This type of commutation undergoes a soft turn-on in Z_{Aa1}, and hence low power losses are generated in D_{Aa1} as depicted in Figure 5-6. In this way, the average soft turn-on losses in each switching period, $p_{son/DAa1}(t)$ can be estimated by:

$$p_{son/DAa1}(t) \approx \frac{1}{T_{sw}} \int_{t}^{t+\Delta t_{on}} v_{DAa1}(t) i_{Aa}(t) dt = \frac{E_{son/DAa1}\left(V_{AC}(t), i_{af}(t)\right)}{T_{sw}} \quad \text{for } V_{AC}(t) < 0 \text{ and } i_{af}(t) > 0 \tag{5.11}$$

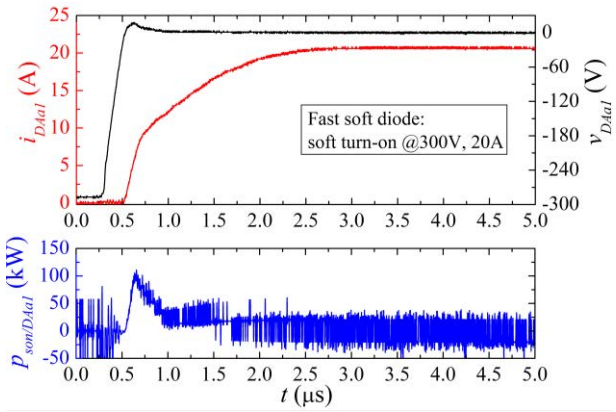
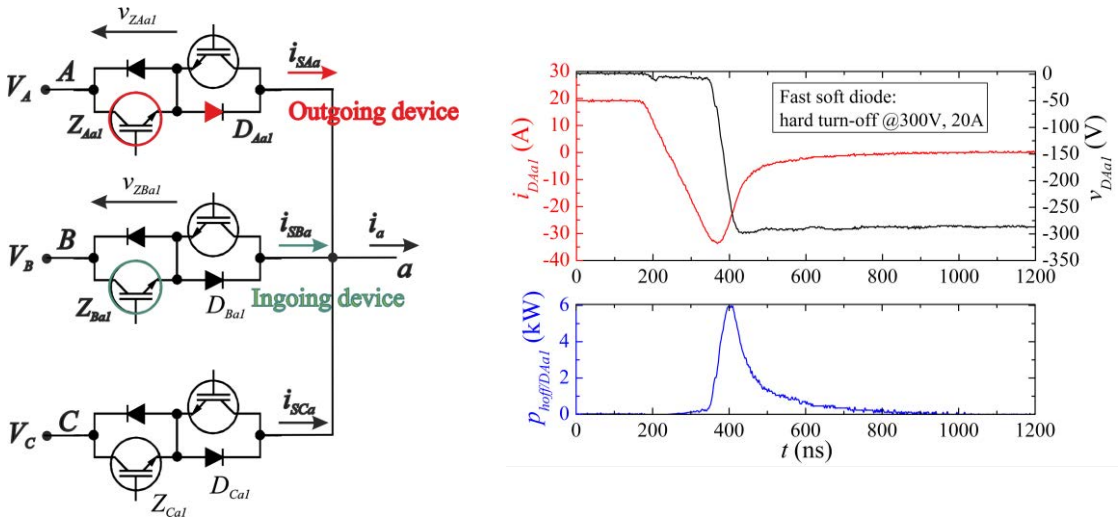


Figure 5-6 Measured diode soft turn-on switching waveforms and associated power losses of BDS 1-6

where $E_{son/DAa1}$ is the dissipated turn-on energy of D_{Aa1}. On the other hand, when $V_{AB}(t)$ has a negative polarity and a turn-off is demanded in S_{Aa} as sketched in Figure 5-7a, D_{Aa1} blocks such voltage till the next commutation comes. In this case, D_{Aa1} can exhibit large turn-off losses due to the reverse recovery characteristic of the diode.



(a) (b)

Figure 5-7 a) Diode turn-off in the S_{Aa} to S_{Ba} commutation process, b) measured hard turn-off switching waveforms and associated power losses of BDS 1-6

Taking in mind the example of commutation processes depicted in Figure 5-3, which occur at the instant $t = t_1$, no significant turn-off and turn-on losses associated to D_{Aa1}. D_{Ba1} and D_{Ca1} diodes are involved in such commutations. However, important turn-off losses are exhibited by D_{Aa1} in the transition from S_{Aa} to S_{Ba}, instant $t = t_3$ as shown in Figure 5-5 and zoomed in Figure 5-7. Previous to the commutation, it is assumed that $i_{SAa}(t)$ current flows through Z_{Aa1} and D_{Aa1} during t_{Aa} interval. When a commutation from S_{Aa} to S_{Ba} is demanded (Figure 5-7), the $i_{SBa}(t)$ current starts to flow through Z_{Ba1} and D_{Ba1}, meanwhile D_{Aa1} begins to recover the current and hence, high energy losses are generated in the device due to the reverse recovery current as illustrated in Figure 5-7b. D_{Aa1} diode exhibits a hard turn-off whereas $V_{AB}(t)$ voltage is negative. Thus, the average hard turn-off losses in the T_{sw} interval, $p_{hoff/DAa1}(t)$ can be expressed as:

$$p_{hoff/DAa1}(t) \approx \frac{1}{T_{sw}} \int_{t+t_{Aa}+\Delta t_{on}}^{t+t_{Aa}+\Delta t_{on}+\Delta t_{rec}} v_{DAa1}(t)\, i_{Aa}(t)\, dt = \frac{E_{hoff/DAa1}(V_{AB}(t), i_{af}(t))}{T_{sw}} \quad (5.12)$$

$$for\ V_{AB}(t) < 0\ and\ i_{af}(t) > 0$$

where $E_{hoff/DAa1}$ is the dissipated hard turn-off energy of D_{Aa1} and Δt_{rec} is the reverse recovery time. The area under the peak power dissipation during Δt_{rec} can also be named as the reverse recovery energy losses. When $V_{AB}(t)$ polarity is positive, D_{Aa1} turns off at

a low voltage and hence negligible power losses are involved. The average soft turn-off losses in the T_{sw} interval, $p_{soff/DAa1}(t)$ can be written as:

$$p_{soff/DAa1}(t) \approx \frac{1}{T_{sw}} \int_{t+t_{Aa}+\Delta t_{on}}^{t+t_{Aa}+\Delta t_{on}+\Delta t_{off}} v_{DAa1}(t)\, i_{Aa}(t)\, dt = \frac{E_{soff/DAa1}(V_{AB}(t), i_{af}(t))}{T_{sw}} \quad (5.13)$$
$$for\ V_{AB}(t) > 0\ and\ i_{af}(t) > 0$$

where $E_{soff/DAa1}$ is the dissipated soft turn-off energy of D_{Aa1}.

Figure 5-8 shows a pseudo hard turn-on commutation due to a low switching voltage and high switching current. The average hard turn-on losses in the T_{sw} interval, $p_{hon/DAa1}(t)$ can be observed in Figure 5-8 and written as:

$$p_{hon/DAa1}(t) \approx \frac{1}{T_{sw}} \int_{t+t_{Aa}}^{t+t_{Aa}+\Delta t_{on}} v_{DAa1}(t) i_{Aa}(t) dt = \frac{E_{hon/DAa1}(V_{AC}(t), i_{af}(t))}{T_{sw}} \quad (5.14)$$
$$for\ V_{AC}(t) > 0\ and\ i_{af}(t) > 0$$

where $E_{hon/DAa1}$ is the dissipated hard turn-on energy of D_{Aa1}.

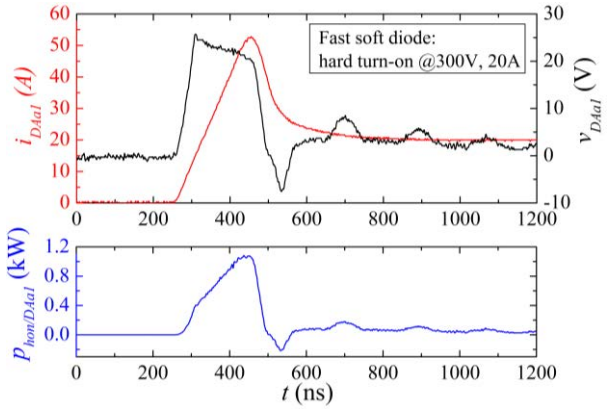


Figure 5-8 Measured diode hard turn-on switching waveforms and associated power losses of BDS 1-6

5.1.7 Total Diode Power Losses

To conclude, the instantaneous power losses of D_{Aa1} (5.9) can be finally described as:

$$p_{DAa1}(t) \approx v_{DAa1}(t)\, i_{Aa}(t)\, D_{Aa}(t) + \frac{E_{son/DAa1}(t)}{T_{sw}} + \frac{E_{hoff/DAa1}(t)}{T_{sw}} + \frac{E_{soff/DAa1}(t)}{T_{sw}} + \frac{E_{hon/DAa1}(t)}{T_{sw}} \tag{5.15}$$

The diode average power losses ($\overline{P}_{DAa1}$) can be calculated by substituting (5.15) in (4.1):

$$\overline{P}_{DAa1} = \frac{1}{T}\int_0^T p_{DAa1}(t)\,dt = \underbrace{\frac{1}{T}\int_0^T v_{DAa1}(t)\, i_{Aa}(t)\, D_{Aa}(t)\,dt}_{\overline{P}_{cond/DAa1}} + \underbrace{\frac{1}{T}\int_0^T \frac{E_{son/DAa1}(t)}{T_{sw}}dt}_{\overline{P}_{son/DAa1}} + \underbrace{\frac{1}{T}\int_0^T \frac{E_{hoff/DAa1}(t)}{T_{sw}}dt}_{\overline{P}_{hoff/DAa1}} + \underbrace{\frac{1}{T}\int_0^T \frac{E_{soff/DAa1}(t)}{T_{sw}}dt}_{\overline{P}_{soff/DAa1}} + \underbrace{\frac{1}{T}\int_0^T \frac{E_{hon/DAa1}(t)}{T_{sw}}dt}_{\overline{P}_{hon/DAa1}} \tag{5.16}$$

where $\overline{P}_{cond/DAa1}$, $\overline{P}_{son/DAa1}$, $\overline{P}_{soff/DAa1}$, $\overline{P}_{hoff/DAa1}$ and $\overline{P}_{hon/DAa1}$ are the average conduction, the average soft turn-on and soft turn-off, the average hard turn-off and hard turn-on, respectively.

5.2 Implementation of the MC Power Losses Calculation

The numerical method to calculate the IGBT and diode power losses in a VSI presented in previous chapters is now extended to calculate the MC power dissipation. The implementation of the losses calculation is focused in a BDS of the MC (S_{Aa} in particular), although it would be similar for other BDSs. The implementation will consist in translating the expressions which describe the different power losses components associated with the IGBT and the diode within the BDS in MATLAB scripts, taking into account the application parameters and the modulation algorithms. Figure 5-9 shows the inputs (parameters of the converter, static fitted parameters and energy losses measurements), losses functions (conduction, hard turn-on, hard turn-off, soft turn-on and soft turn-off) and outputs (average power losses of each power

dissipation component) that configure the IGBT power calculation block. Each losses function is derived from its corresponding expression in (5.8).

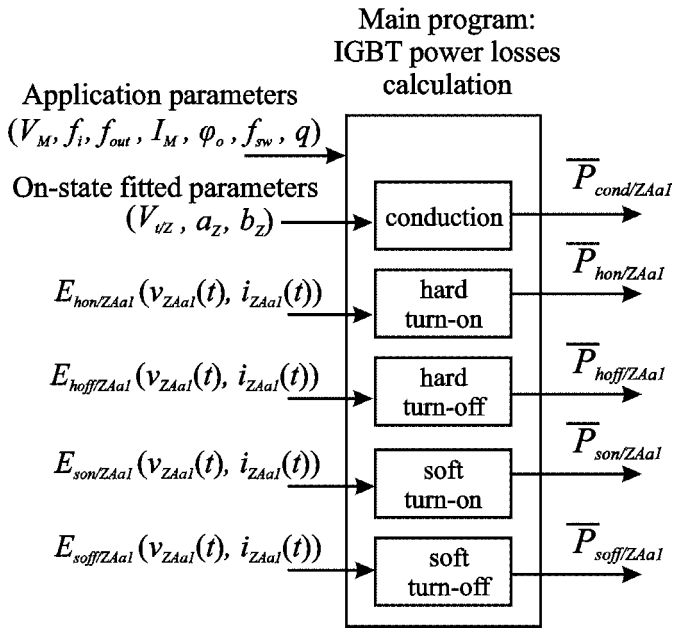


Figure 5-9 Block diagram of the power losses calculation script for a single IGBT within the MC

In a similar way, the diode power calculation scheme based on expression (5.16) is described in Figure 5-10.

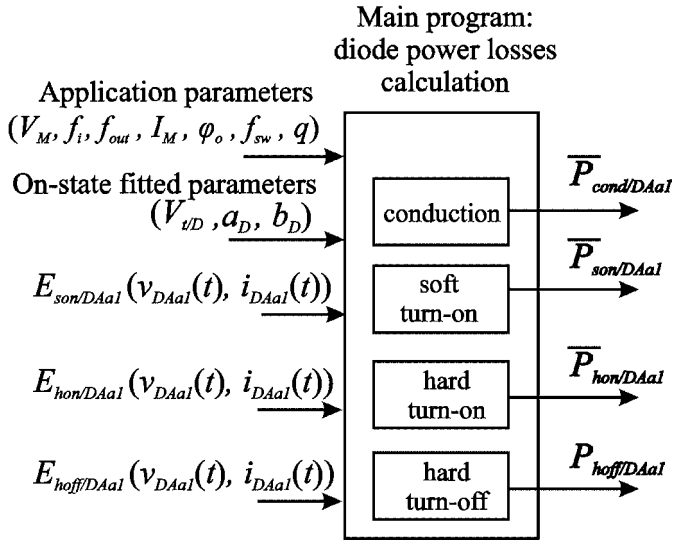


Figure 5-10 Block diagram of the power losses calculation script for a single diode within the MC

It is relevant the inclusion of different working parameters of the converter (input and output frequency, switching frequency, power factor, etc.) in the proposed computation method since they have a strong impact on the power losses. This will also

allow the converter designer to predict the power losses of the power semiconductors within the BDS in a true converter operation.

5.2.1 Description of the Power Losses Functions

Power losses components are split into conduction and switching functions:

5.2.1.1 Conduction Losses Function

The IGBT and diode conduction functions are based on (5.2) and (5.10) expressions, respectively. The device duty cycle is derived from the employed modulation strategy as shown in Figure 5-11 for Venturini and DS SVM modulations. Likewise, other modulation schemes can be considered (such as the optimum-amplitude Venturini [93] or the SVM with either one zero or two zero vectors in each switching period [73]), but the two selected algorithms represent the main practical solutions demonstrated for the control of MCs.

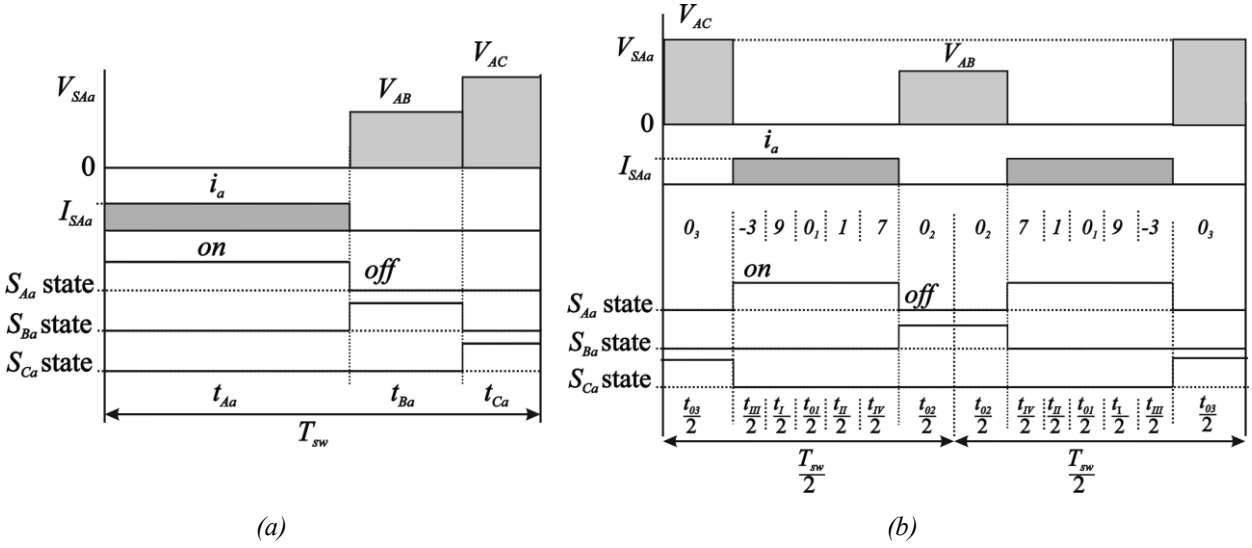


Figure 5-11 Schematic representation of the switching pattern for BDS S_{Aa} for a) Venturini modulation. b) double-side space vector modulation

A typical switching pattern of the BDSs (i.e. state of the BDSs, *on-off*, during a switching cycle) connected to output *a*-phase (S_{Aa}, S_{Ba} and S_{Ca}) based on Venturini modulation is depicted in Figure 5-11a, where I_{SAa} and V_{SAa} are the current and voltage across the S_{Aa} BDS, respectively, V_{SAa} is built from the relative input phase voltages (V_{AB} and V_{AC}). This switching pattern repeats through the matrix converter operation and, in fact, it defines the converter switching frequency (f_{sw}). t_{Aa} is derived from its duty cycle, m_{Aa}, which is calculated as explained in Appendix C. m_{Aa}, represents the

same concept as the aforementioned D_Z, i.e. a duty cycle. It is only a change in the nomenclature. The Venturini modulation limits the maximum voltage ratio q between input and output voltage amplitudes to a 50 %. On the other hand, Figure 5-11b depicts DS SVM switching pattern scheme. It has the particularity that a symmetric switching pattern is defined in each switching period as observed in Figure 5-11b where t_{01}, t_{02} and t_{03} are time intervals of the three zero switching patterns and t_I, t_{II}, t_{III} and t_{IV} are the time intervals of the four active switching configurations as explained in more detail in Appendix C. Comparing both switching patterns, one realises that more commutations are undergone by the DS SVM modulation than for Venturini. The maximum number of commutations for DS SVM can be two (two *turn-on's* and two *turn-off's*) and one commutation (one *turn-on* and one *turn-off*) for Venturini. This fact has an important impact on the losses as described in later in section 5.3.

5.2.1.2 Switching Losses Function

The switching losses functions, i.e. IGBT and diode soft turn-on, IGBT and diode soft turn-off, IGBT and diode hard turn-on, IGBT and diode hard turn-off, must deal with the identification of the type of commutation which is undergone by the device at each switching instant and with the evaluation of the switching losses surface with the corresponding voltage and current at each switching instant under the given commutation region. Figure 5-12 shows the block diagram for hard turn-on and hard turn-off losses functions. All the switching losses blocks are analogous among them, but each one is focused on one commutation losses type. Moreover, an external sub block, called modulation algorithm, dictates the time instants when the controlled device is *on* and *off* and the time the device is conducting. As represented in Figure 5-2 and Figure 5-5, the relative input phase voltages (V_{AB} and V_{AC}) and the direction of the output *a*-phase current are necessary to identify the device commutation type. For this reason, they are the inputs of the commutation type identification sub block.

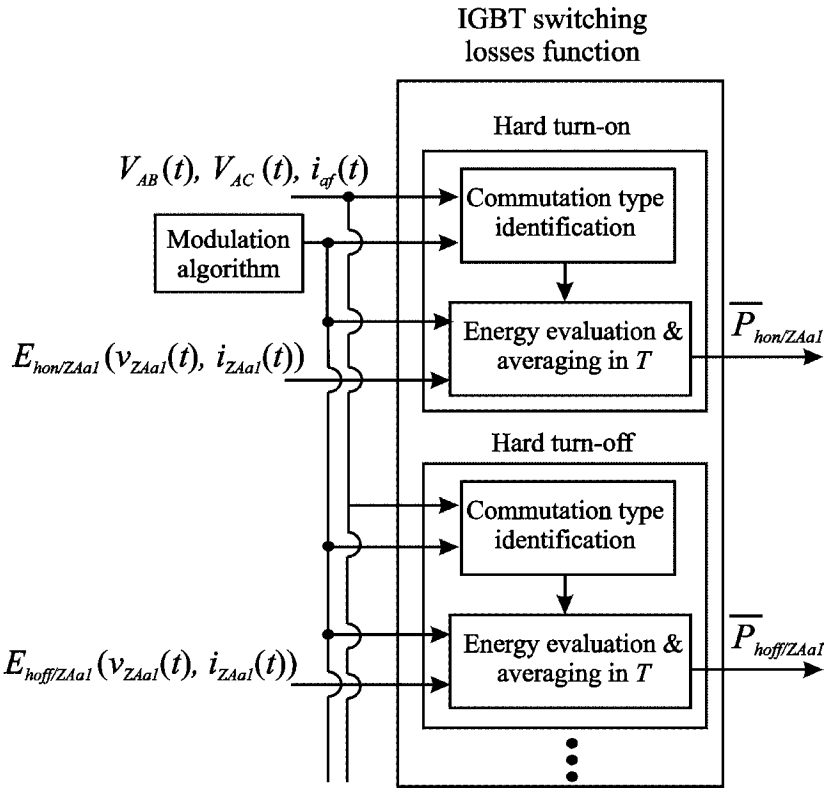


Figure 5-12 Block diagram of IGBT switching losses function

The implementation of the DS SVM modulation is not as straight forward as for the Venturini algorithm. An explanation of the DS SVM control algorithm is summed-up in Appendix C. Taking into account this; the block diagram of Figure 5-13 describes in detail how the DS SVM is implemented. Basically, it consists in two main blocks: first, there is a general computational block at converter level where the output reference voltage and input reference current sectors are determined; duty cycles are calculated; switching configurations are selected and finally the switching pattern is generated in such a manner that only one commutation is involved from one vector to the next one. Second, there is a device computational block which is focused on the power device (for instance Z_{Aa1} and D_{Aa1}). Firstly, this block selects over all switching sequences those that enable S_{Aa} switch, selects over all calculated duty cycles those which correspond to S_{Aa}, and determines throughout all the T period the voltage, current and the time instants the device undergoes a hard/soft turn-off or hard/soft turn-on. Once the time limits of each different commutation type are known, the corresponding switching energy losses can be estimated from the switching energy surfaces of chapter 3. Averaging the instantaneous hard turn-on power dissipation over T, the average hard turn-on power losses are calculated.

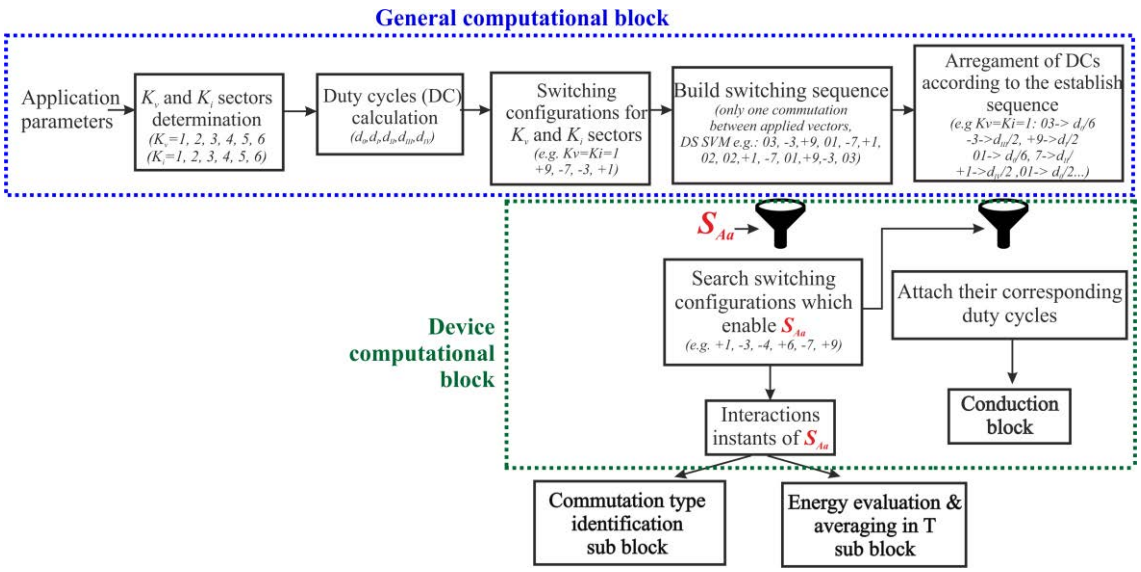


Figure 5-13 Detail of the modulation algorithm block for the DS SVM case

5.3 Losses Calculation and Analysis

In order to illustrate the potential utility of the proposed losses estimation method to evaluate the semiconductor power dissipation an example application of an AC induction motor variable speed drive is used. The induction motor drive is implemented by a three-phase to three-phase MC [95]. This losses analysis method under various modulation schemes (Venturini and DS SVM in this case) as well as different operating conditions results in a practical design tool to predict efficiency behaviour of the converter, to select the optimum power devices for a given application, to select the converter switching frequency, etc. Among the most critical operation conditions to consider in the converter design, let us mention: the motor speed by varying f_{out} and motor's supplied voltage with modulation ratio q; the motor power factor $\cos \varphi_0$; the switching frequency of the converter f_{sw}, etc. It is contemplated a three-phase 230 V – 50 Hz line input voltage and converter operation at f_{sw} between 10 kHz and 40 kHz. The *BDS 1-6* (IRG4PH50S IGBT and 20ETF12 diode) is arranged in a common emitter configuration as depicted in Figure 5-1. Then, *BDS 1-6s* are allocated in the two-phase to one-phase MC test circuit.

5.3.1 Losses Comparison between Venturini and DS SVM Modulation

The power losses comparison between Venturini and DS SVM modulation is performed under equal converter conditions, including a relative low voltage transfer ratio of 50 %, since this is the maximum value allowed in the Venturini modulation. The comparison between the power losses in Z_{Aa1} and D_{Aa1} under the aforementioned parameters are depicted from Figure 5-14 to Figure 5-17. $\overline{P}_{SAa}$, $\overline{P}_{cond/Z}$, $\overline{P}_{cond/D}$, $\overline{P}_{hon/Z}$, $\overline{P}_{hoff/Z}$, $\overline{P}_{hoff/D}$, $\overline{P}_{son/Z}$, $\overline{P}_{soff/Z}$ and $\overline{P}_{hon/D}$ correspond to the average losses of the whole BDS, IGBT conduction, diode conduction, IGBT hard turn-on, IGBT hard turn-off, diode recovery, IGBT soft turn-on, IGBT soft turn-off and hard turn-on diode, respectively. Figure 5-14 shows the IGBT and diode power dissipation when varying the switching frequency (f_{sw}) for the two different matrix converter modulation methods.

As expected, the higher the switching frequency, the higher are the total losses for both control methods, showing a practically linear dependence. Device conduction losses remain low and practically constant since the BDS is conducting at any time regardless of the modulation used in agreement with [96]. On the other hand, the DS SVM method is based on symmetric modulation patterns showing more commutations in each switching period than the Venturini modulation and, consequently exhibits higher switching losses. Concerning the IGBT soft switching losses, they are at least one order of magnitude lower than the hard commutation losses as shown in Figure 5-14 for both modulations, so that they are mostly not considered in practical designs.

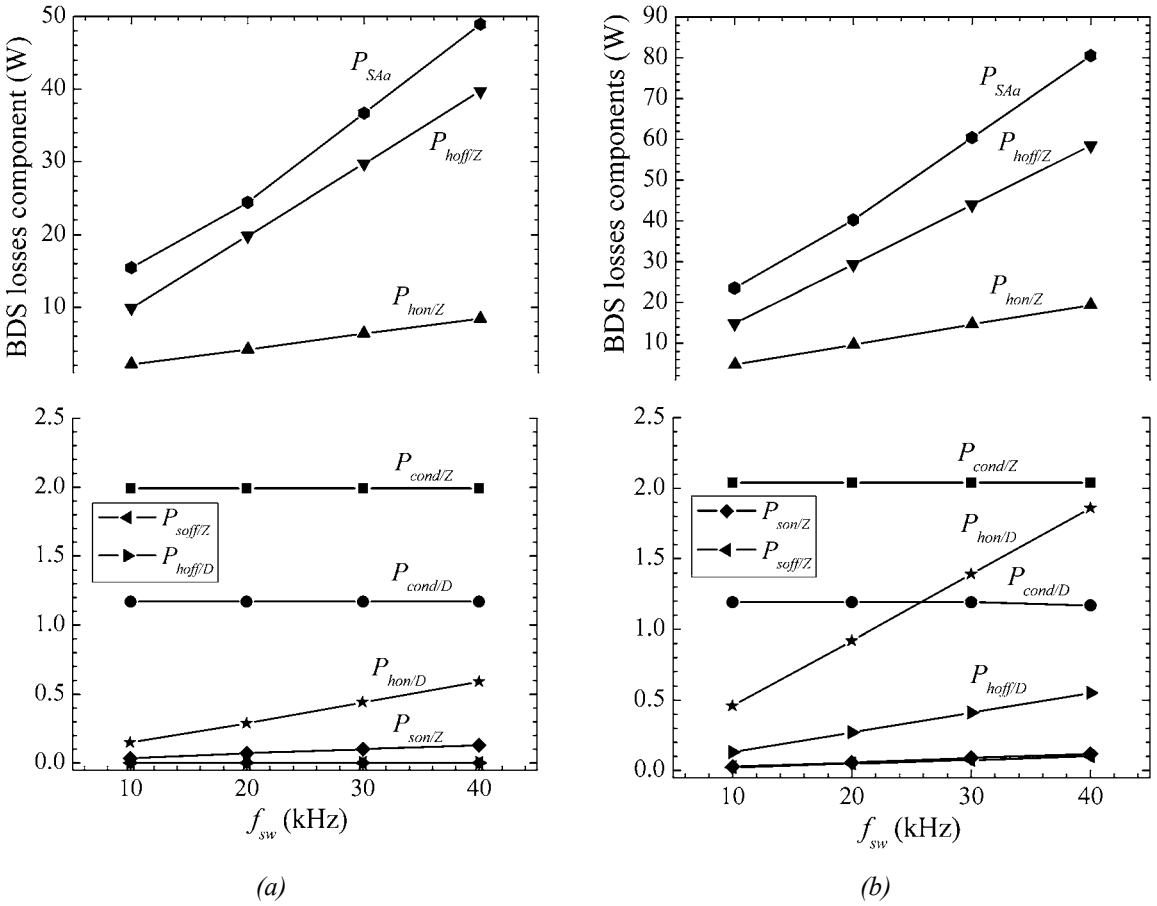


Figure 5-14 Comparison of Z_{Aa1} and D_{Aa1} power losses depending on the converter switching frequency. Operating conditions: f_i and f_{out} are 50 Hz, q is 0.5 and cos φ_o is 0.84. a) Venturini modulation. b) DS SVM modulation

5.3.2 Losses Analysis for the Relevant Application Parameters of the MC

All BDS losses components are computed for different working conditions of the MC as AC drive application at the same f_{sw} of 20 kHz and for the DS SVM control algorithm. Figure 5-15 shows power losses in Z_{Aa1} and D_{Aa1} for different AC machine references or qualities (i.e., different cos φ_o). In the present study, the losses are clearly dominated by the IGBT turn-off characteristics not only in Figure 5-15 but also in Figure 5-16 and Figure 5-17 as the used IGBT reference shows relatively low on-state voltage drop but significant turn-off switching energies (relatively slow turn-off time). Both, conduction and switching losses are affected by the load characteristics. This fact can be anticipated in Figure 5-2 where the IGBT (in this case) is involved in various commutation regions depending on the voltage across and current through the device at

the switching instant for a given cos φ_o. Whenever cos φ_o is modified, the commutation regions will also vary and different components of the losses will be exhibited by the IGBT or diode. This behaviour is translated in a reduction of the switching losses with cos φ_o as shown in Figure 5-15. As the load becomes more resistive the recovery losses in the diode ($P_{Hoff/D}$) in Figure 5-15 decrease since the free-wheeling behaviour is less relevant. On the other hand, conduction losses increase with cos φ_o and the highest value is found for cos φ_o = 1 since the output phase current is in phase with the output voltage.

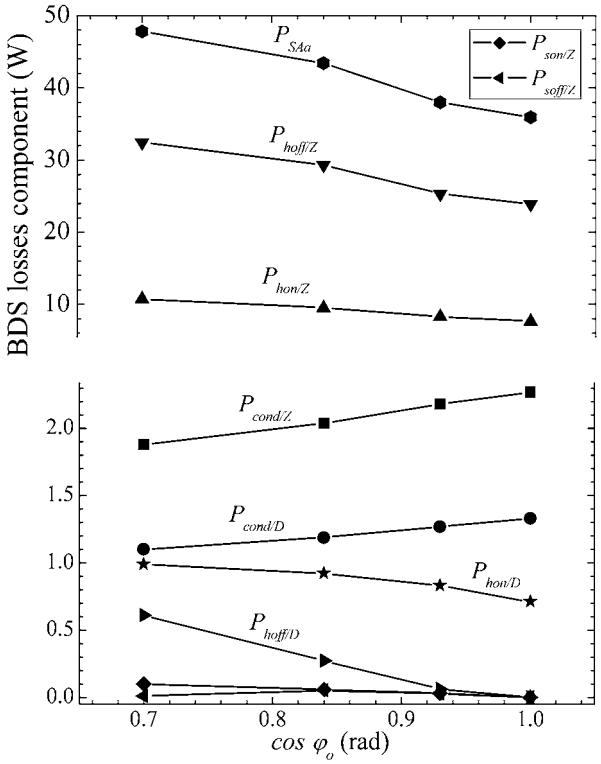


Figure 5-15 Comparison of Z_{Aa1} and D_{Aa1} power losses depending on cos φ_o. Operating conditions: f_i and f_{out} are 50 Hz, q is 0.5 and f_{sw} is 20 kHz.

In Figure 5-16, the losses calculations for different values of f_{out} are summarised. This analysis provides interesting results in the framework of AC drives where a variable speed in the AC machine is required. It is observed a maximum power dissipation in all hard switching losses components with $f_{out} = f_i$. This is due to the fact that the S_{Aa} switch is more active during the peak values of the input phase voltage and output current while in other cases S_{Aa} is switched *on* for smaller intervals.

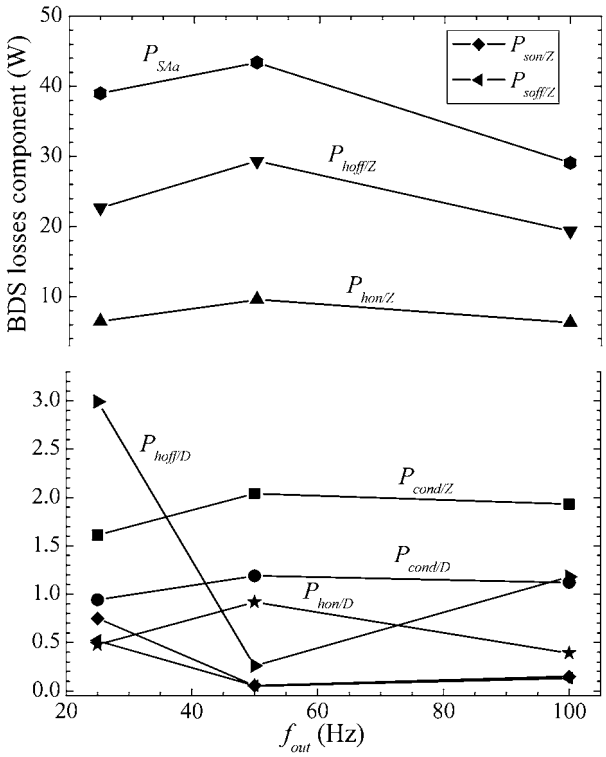


Figure 5-16 Comparison of Z_{Aa1} and D_{Aa1} power losses depending on f_{out}. Operating conditions: f_i is 50Hz, q is 0.5 cos φ_o is 0.84 and f_{sw} is 20 kHz

Figure 5-17 depicts the dependence of the voltage transfer ratio q on the losses. As it can be derived from Figure 5-17, conduction losses contribution varies linearly with q, whereas switching losses remain constant. This behaviour can be explained by the fact that the voltage level at the MC output is mainly controlled by the IGBTs duty-cycles for a given switching period and, consequently, higher output voltages are associated to longer device conduction times.

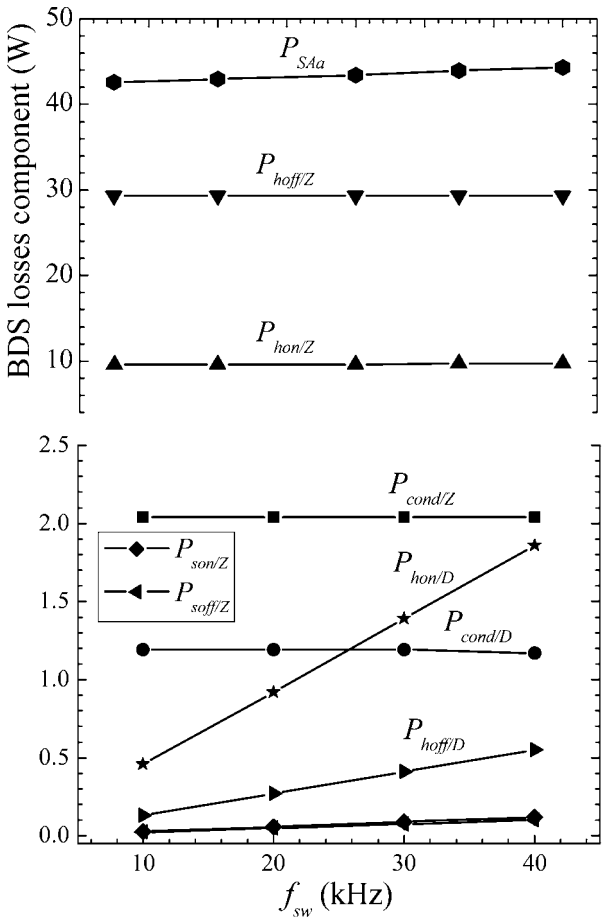


Figure 5-17 Comparison of Z_{Aa1} and D_{Aa1} power losses depending on q. Operating conditions: f_i and f_{out}.are 50 Hz, cos φ_o is 0.84 and f_{sw} is 20 kHz

5.3.3Losses Analysis for Different Power Devices Technologies

As discussed mainly in chapter 3, the BDS plays an important role in the practical implementation of MCs. Choosing the optimum power semiconductors in terms of efficiency, cost and the cooling system design is a challenge addressed in this section. Hence, it is essential to analyse the semiconductor power losses as a function of their characteristics and technologies in order to decide which device is suitable for a given application.

The total power dissipation of various BDSs types with the converter frequency is shown in Figure 5-18 for an application which requires a low working frequency. Due to this fact, the Venturini modulation fulfils better this requirement and thus, it is employed in the power losses calculation. The operational ranges of the BDSs depending on the f_{sw} can be established from Figure 5-18. Three ranges are defined to have an understandable discussion, low (f_{sw} < 5 kHz), mid (5 kHz < f_{sw} < 15 kHz) and

high (f_{sw} > 15 kHz) switching frequency. As it was expected for f_{sw} < 5 kHz, the "slow IGBT-slow Diode" combination (*BDS 1-6*) is the best one and the "fast IGBT-fast Diode" one (*BDS 4-9*) is the worst one from the power dissipation point of view. The prediction of the power losses of the crossed combinations (*BDS 1-9* and *BDS 4-6*) is more difficult, and in both cases a detailed analysis must be performed. *BDS 4-6* exhibits almost the same power losses as *BDS 1-9* (slightly lower). Between 5 KHz and 15 kHz, *BDS 4-6* and *BDS 4-9* show the best performance, due to the low turn-off losses of the high speed IGBT, in contrast to the other combinations where the slow IGBT dominates the switching behaviour. As the frequency rises till 20 kHz, the power dissipation difference between BDSs with fast and slow IGBT are even higher than at mid frequency, resulting that *BDS 4-6* and *BDS 4-9* are the best component combinations. It is also remarkable that the combination made of a high speed IGBT and fast soft diode (*BDS 4-6*), presents the best solution in the whole converter frequency range [97].

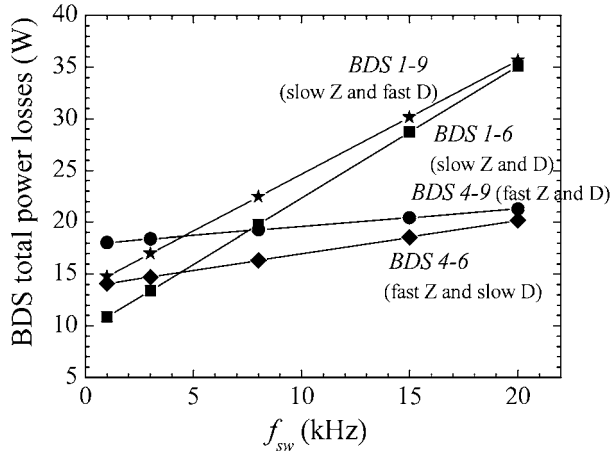


Figure 5-18 Comparison of BDS total power losses for different BDS combinations depending on f_{sw}. Operating conditions: f_i and f_{out} are 50 Hz, cos φ_o is 0.84

It is also interesting to take into account the relative contribution of each device within a BDS to the total power losses. Thus, the distribution of the power dissipation of each semiconductor in the analysed BDSs for different switching frequencies can be appreciated in Figure 5-19. A boundary red line can be helpful to remark both types of losses. As expected, the conduction losses of all BDS combinations at low f_{sw} are higher than the switching losses, because the on-state characteristics of the semiconductors weights more than the dynamic ones. An interesting result is that when f_{sw} rises, the

dominant losses are the switching ones for the combination *BDS 1-6* and *BDS 1-9*, but for *BDS 4-6* and *BDS 4-9* the conduction losses remain the dominant ones. This fact can be explained by the turn-off behaviour of both IGBTs as illustrated in Figure 4-15. The slow IGBT exhibits higher turn-off energy losses than the fast one. Another important point in the discussion concerns the diode power losses. As it can be appreciated in Figure 5-19a and Figure 5-19c, a little loss contribution due to the diode turn-off is presented in *BDS 1-6* and *BDS 4-6* combination, while these losses can be completely neglected for *BDS 1-9* and *BDS 4-6*, due to the ultra-fast diode switching behaviour.

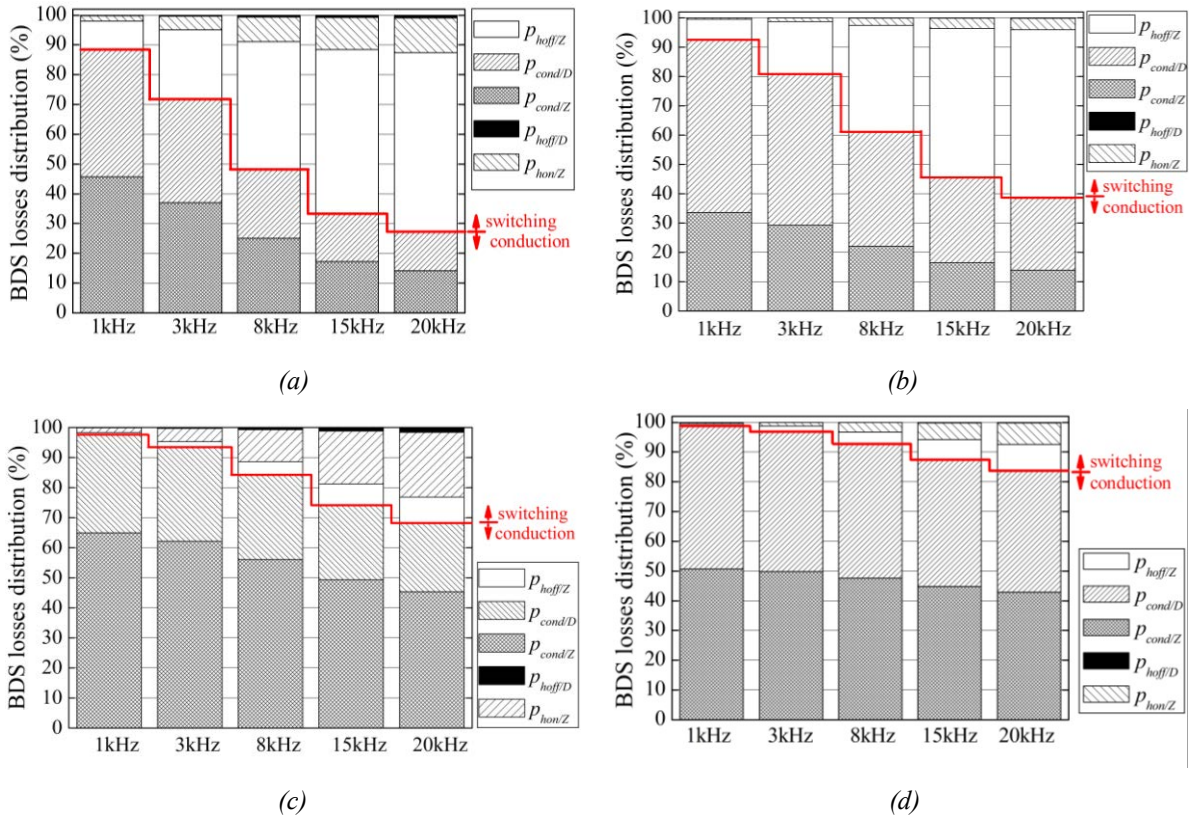


Figure 5-19 BDS power losses distribution depending on the operation mode. a) BDS 1-6. b) BDS 1-9. c) BDS 4-6. d) BDS 4-9

The diagrams of Figure 5-19, allow evaluating relative contributions between conduction and switching losses for a given BDS combination and switching frequency. Thus, at a first glance it is very easy to deduce which is the critical operation mode (conduction or switching) of the component to be optimised. The same basic information of Figure 5-19 can be also represented as it is shown in Figure 5-20, where the boundary line divides the total power losses contribution of each device (IGBT and diode) in a given BDS type for each switching frequency. It is noticeable from Figure

5-20, the negative influence on the power losses of the BDS combination with an ultra fast diode, since it represents a high percentage of the total BDS dissipation. This fact can help the MC designer to consider if this device is suitable for the BDS implementation.

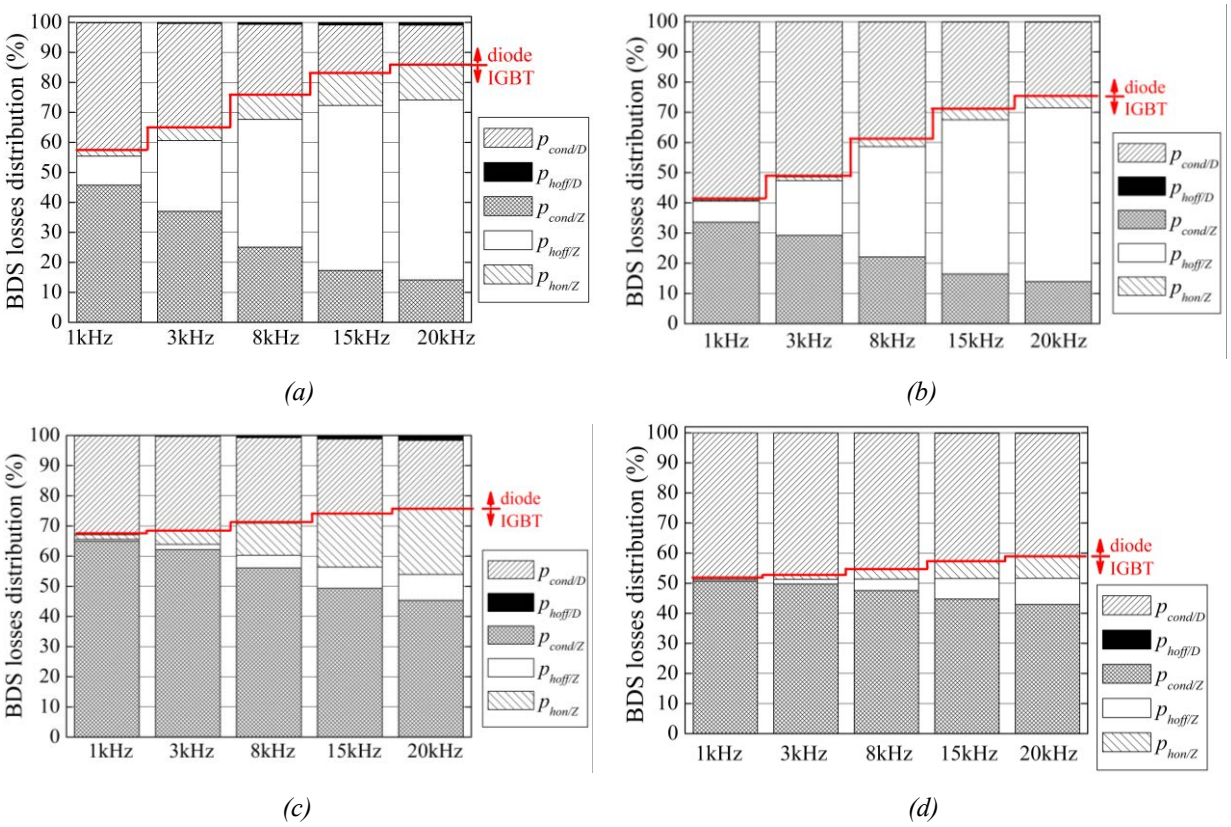


Figure 5-20 BDS power losses distribution depending on the power device. a) BDS 1-6. b) BDS 1-9. c) BDS 4-6. d) BDS 4-9

Now, the total power dissipation of *BDS 1-6*, *BDS 4-9*, *BDS 4-10* and the *RB BDS* are analysed with the converter frequency as shown in Figure 5-21 for an application which requires a high working frequency. Due to this fact, the DS SVM modulation fits better this requirement and thus, it is employed in the power losses calculation.

The BDS implemented with RB-IGBTs (*RB BDS*) shows the highest dissipation despite of its lowest conduction losses as depicted in Figure 5-21, even at relatively low switching frequencies around 10 kHz. However, its dynamic performance is worsened due to its poor dynamic behaviour, meaning that high power dissipation is involved in the turn-on and turn-off transitions of the RB-IGBT as it was deduced from its dynamic characterisation in chapter 3 and as it was depicted in Figure 3-15 and Figure 3-16. In contrast to this, the BDSs based on the high speed IGBT and ultra-fast Si and SiC

diodes (*BDS 4-9* and *BDS 4-10*, respectively) exhibit lower losses since they have a better dynamic performance such as a very low reverse recovery current of the SiC diodes and shorter turn-off transition time of the IGBT [98].

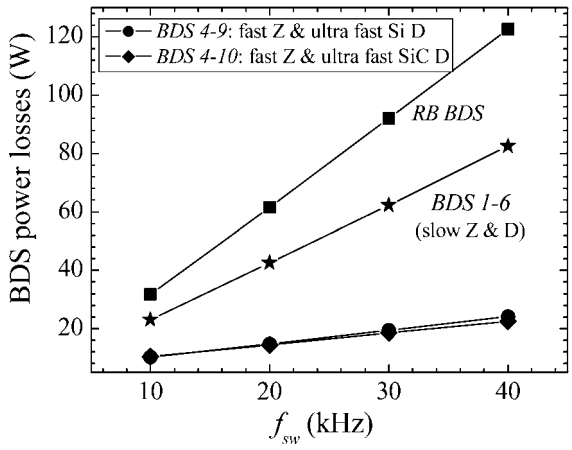


Figure 5-21 Comparison between total BDS power losses based on different devices in a MC working at different switching frequencies

The distribution of the power dissipation of each semiconductor in this sample group of BDSs depending on its fabrication technology and for different switching frequencies can be appreciated in Figure 5-22. As a general comment, the dominant losses are the switching ones in the f_{sw} range considered (10 – 40 kHz). On the other hand, the lowest conduction losses component appears in the RB BDS as depicted in Figure 5-22d. As in such BDSs current is flowing only in one device, their voltage drop is lower than in other BDS arrangements. The highest IGBT turn-off losses contribution arises from the BDS combination with the "standard speed" IGBT (IGBT *1*) as illustrated in Figure 5-22a. This IGBT shows a low forward voltage drop, but at the same time exhibits a slow turn-off transition generating in this way high switching losses. Another point in the discussion concerns the diode power losses. The SiC diode behaviour (Figure 5-22c) shows the highest conduction losses in comparison with the Si diodes. Conduction losses predominate at 10 kHz for the ultra-fast Si and SiC diodes as depicted in Figure 5-22b and in Figure 5-22c, respectively, since their on-state characteristics weights more than the dynamic ones. The hard turn-on and turn-off losses are the major components of the total losses of the *RB BDS* as illustrated in Figure 5-22d. The losses contribution of the internal diode states for the behaviour of the RB IGBT placed in *BDS-Ba* commutation cell. As inferred from Figure 5-21, the *RB BDS* seems not to be a

suitable candidate to implement a MC due to their high switching losses, although [99] demonstrates that applying a zero current switching strategy leads to a reasonable total switching losses and hence, it makes sense the use of RB-IGBTs.

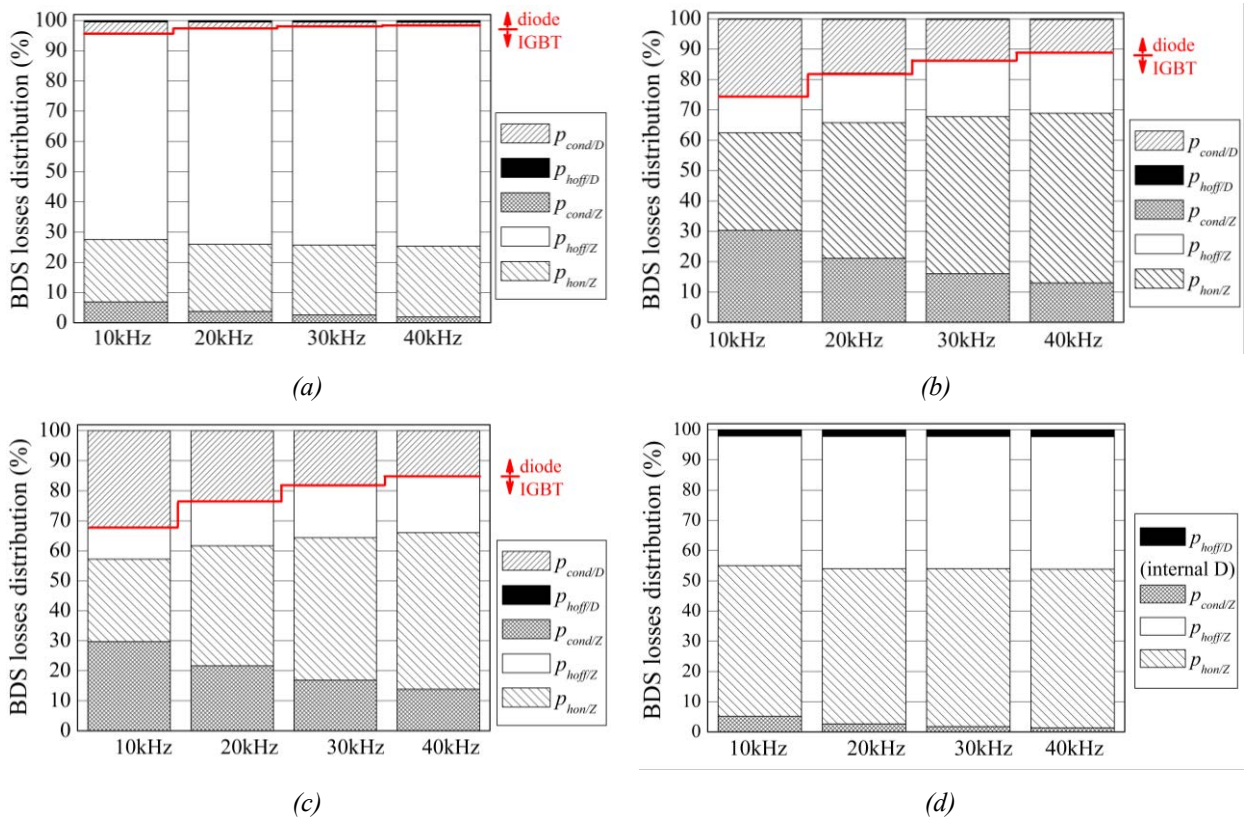


Figure 5-22 BDS power losses distribution depending on the power device. a) BDS 1-6. b) BDS 4-9. c) BDS 4-10. d) RB BDS

It is worth to point out that for evaluating the total MC power losses in the sinusoidal regime (for example for the thermal dissipation system design), the power losses of the IGBTs and diodes connected to the same output phase must be calculated, added and multiplied by three (the number of output phases in the converter). Therefore, the proposed power losses computation method, not only provides the total MC dissipation as described in previous work, but also the different losses components associated with each power device.

5.4 Summary

A method to evaluate accurately the semiconductor power losses has been introduced and validated by means of a VSI converter in chapter 4. The method has been extended to calculate the devices power losses of the BDS within AC/AC matrix converters (MC)

in chapter 5. MC power losses estimation is more complex that for the VSI case since energy losses are voltage and current dependent, and both vary throughout the period *T*.

A computational method is implemented by MATLAB scripts to process the obtained static and dynamic characterization data and together with the operation parameters of the converter (i.e. modulation method, switching frequency, input and output frequency, input and output voltage, power factor of the load) calculate the power dissipation of the power devices in a first place and the whole converter in a second place. The general block diagram of the device losses calculation is presented as well as a detailed description of the conduction and switching losses functions and the modulation algorithm block. It should be pointed out the difficulty to implement the DS SVM modulation since it should deal with a big number of switching configurations and should perform different computations such as to determine input current and output sectors, establish switching configurations, and calculate duty cycles). The modularity and rapidness of calculation of the method allows analysing the losses taking into account different operating conditions.

The analysis of the BDS power losses comprises two important aspects: the converter operation conditions and the power devices characteristics and technology.

a) Converter operation conditions:

- The Venturini and DS SVM modulation schemes have been implemented to analyse the semiconductor power losses.
- DS SVM modulation shows higher BDS total power losses than Venturini since a major number of commutations are undergone. For instance at f_{sw} = 40 kHz, BDS total power losses using the DS SVM are about 37 % larger than using Venturini.
- BDS total power losses increases nearly linear with increasing the f_{sw}. As it is well known, losses also increase with the output current.
- $cos\ \varphi_o$ modifies the commutation regions and hence, the components of the losses will be exhibited by the IGBT or diode.
- When $f_{out} = f_i$ a maximum power dissipation is observed in the BDS total losses. This fact discloses that the power devices losses within a BDS are not always evenly distributed among the BDSs connected to the same output phase.

- Device conduction losses contribution varies linearly with the voltage transfer ratio q since the duty-cycles are also larger for a given switching period. But, the BDS total losses remain almost the same.

b) Power semiconductors:

- *BDS 1-6* combination (slow Z and D) shows the lowest power dissipation at a relative low switching frequency (f_{sw} < 5 kHz). This combination should be discarded if a higher operating frequency is required.
- *BDS 4-9* (fast Z and ultra-fast Si D) and *BDS 4-10* (fast Z and SiC D) present very similar dynamic performance and exhibit almost the same power dissipation in the frequency range from 10 kHz to 40 kHz. Thus, it would be not justified to purchase the SiC diode whose cost is greater than the Si diode, and wait for a price reduction. On the other hand, in case of operating with a frequency higher than 40 kHz, it would be probable that the SiC diode was better suited than the Si diode for such application since it will exhibit lower losses.
- A priori, the RB BDS seems not to be a favourable option due to its high switching losses for the entire switching frequency range. But, for instance, the solution of commuting the RB-IGBTs at zero current can mitigate this handicap. In addition, less volume and compact MC can be built employing the RB-IGBT devices.

6. Bidirectional Switch Intelligent Power Module (BDS-IPM) for Matrix Converter Applications

In this chapter many of the results already presented in this work have been used for the development and practical implementation of a singular BDS. We come up with the concept of a bidirectional switch intelligent power module (BDS-IPM) [40] intended to make easier the practical assembly of Matrix Converters as well as increase the modularity of the converter itself. A brief introduction will highlight the benefits of such module. The structure of the BDS-IPM (power and control circuits) is explained in detail. Its main static and dynamic electrical characteristics are discussed, showing the performances of the module. Finally, the first results of three BDS-IPMs working together in a test matrix converter are also presented, validating the proposed approach in practical low and medium power applications. The features of the test matrix converter are described including the corresponding voltage and current transducers and a high level control circuit to compute the MC control algorithm.

6.1. Introduction to the BDS-IPM

Matrix Converters (MC) are more compact, light and versatile than standard AC-AC power converter solutions. The more relevant aspect of MCs compared with voltage source inverters (VSI) is the suppression of the intermediate DC voltage stage. This allows the elimination of the cumbersome bank of storage capacitors in the DC link. Consequently, MCs allow achieving higher levels of integration, higher-temperature operation (electrolytic capacitors are limited in working temperature) and natural bidirectional power flow (to regenerate energy back to the utility).

Nevertheless, the practical implementation of MCs requires a big number of bidirectional switches (BDSs) to connect any input line to any output line. As practical BDSs are implemented combining several unidirectional switches, a high number of power devices (diodes and switching devices) is required [101]. For example, nine BDSs, with eighteen switching devices and eighteen diodes are needed to implement a typical three-phase to three-phase MC. Using RB-IGBTs the total device count would be the half, i.e. eighteen devices. In any case the interconnection of all these devices is a complex task due to the high di/dt and dv/dt values involved in the power circuits, as well as the high number of control signals to be managed in a noisy environment. Thus,

any solution oriented to avoid these problems, which are also common to multi-level converters [102], is welcomed by the design engineers. To partially overcome these drawbacks, the entire power stage of three-phase to three-phase MCs has been proposed in single power modules [103]. Nevertheless, when using this solution, if only one of the thirty six or the eighteen (i.e. RB-IGBT implementation) power devices is destroyed, the whole module becomes useless. An alternate solution consists in using power modules integrating three BDSs (with six IGBTs and six diodes) configured as a three-phase to one-phase MC [104, 105]. Power modules implementing the power stage of a single BDS (two IGBTs and two diodes) can also be found as mentioned in chapter 1. In any case, all these power modules do not include any local control circuitry or intelligence, only the power stage.

As classical MC circuits do not show natural free-wheeling paths for the inductive load currents, the current commutation strategy between BDSs is quite relevant in order to ensure correct performances and high reliability. These algorithms determine from the high-level logic control, the signal of the BDSs (*on* / *off* signal), the right switching sequence of the different switching devices and delay times. The delays are mainly related to the characteristic switching times of the power devices as described in chapters 2 and 3, while the switching devices commutation sequence is mainly determined by the sign of the phase load current and the polarity of the voltage across the BDS. In any case, the determination of the switching devices commutation instants is not a major aspect for the high-level control block and this commutation strategy task can be associated to a local control circuitry. In [104] a specific control board to manage with the protections and commutation strategy of the nine BDSs of a complete MC is proposed.

The proposed intelligent power module [106] consists basically in a bidirectional switch function (bidirectional in current and voltage) with fast switching times and implementing the current commutation strategies required for safe commutation processes. The BDS-IPM includes the power transistors gate drivers, galvanic isolation between control and power stages, over-voltage protection devices, floating voltage power supplies and a local control circuitry providing the smart switching sequences for the current commutation strategy. In addition, its modular design allows the easy replacement of damaged BDSs in an entire MC and makes the power and signals interconnections easier. The module can be easily screwed to a heat-sink to allow a

suitable cooling and can be also used in other power converters requiring the bidirectional switch function.

6.2. Structure the BDS-IPM

The basic structure of the BDS module consists of a power substrate containing the power devices (diodes and IGBTs) connected in common emitter configuration and a board on top with the control circuits. Other configurations based on the common collector or RB-IGBTs are also feasible. From the user's point of view, the proposed module shows two power terminals (bidirectional switch function), two pins corresponding to the voltage power supply (shared with the high-level control circuits), the BDS logic control signal pin (BDS turn-on / turn-off) and other auxiliary control pins depending on the implemented commutation strategy (for example, the sign of the phase current).

6.2.1. BDS-IPM Block Diagram

Figure 6-1 shows the block diagram of the proposed BDS module prototype with its main elements and signals. The high-level control circuitry of a MC, determines the turn-on and turn-off instants of the BDSs using relatively complex modulation algorithms to fix the current and voltage target values in the load (for example the Venturini or space vector modulation ones). The MC high-level logic control signals are sent to the proposed modules where they are processed following a given commutation strategy ("four-step current commutation", "two-step current commutation", etc.) in order to determine the precise switching instants of the power switching devices involved in a commutation process between BDSs. In the present prototype, these logic signals are the BDS *on* / *off* control (i.e. *In*) and the sign of the output phase current (i.e. *Isign*) where the BDS is connected. The processing capability (intelligence) of the proposed module is given in the preliminary prototype by a low cost PIC microcontroller, although other programmable logic ICs can also be used. These local-control circuits share the same voltage reference as the high-level ones, and even the same power supply (*Vcc*). The processed BDS control signals (G_1 and G_2) are galvanically isolated using opto-couplers and they are sent to the power switching devices gate drivers. The floating voltage supply of these drivers is guaranteed by a high density integrated DC/DC converter supplied by *Vcc*. The gate control signal is finally

transferred to the power substrate which contains the power devices and other protection devices such as over-voltage transient suppressors and gate resistors.

As it can be observed in the power stage block of Figure 6-1, T_1 and T_2 corresponds to the power terminals. Moreover, the selected configuration of the IGBTs and diodes is the common-emitter one, because both IGBTs share the same reference terminal for their control (the common-emitter). This fact allows applying positive and negative gate-to-emitter voltages to both IGBTs using a single two-output DC/DC converter as floating voltage supply. This point can be observed more in detail in Figure 6-2.

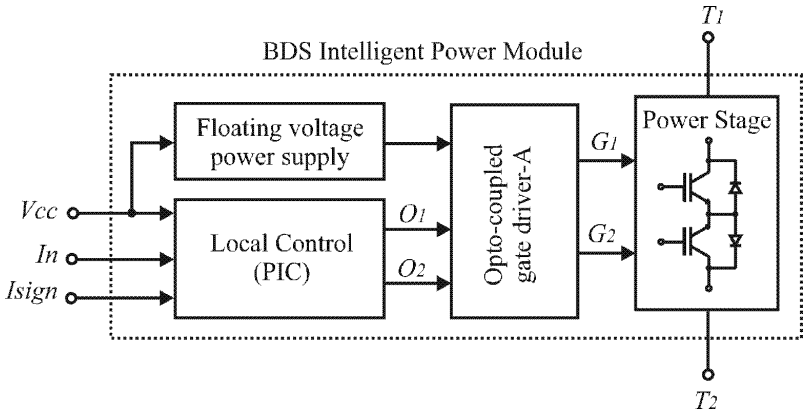


Figure 6-1 Block diagram of the proposed intelligent power module integrating a bidirectional switch

6.2.2. Detailed BDS-IPM Schematic

A more detailed scheme of the implemented BDS module prototype is depicted in Figure 6-2. As mentioned before, the local-control circuit is based on the PIC12F675 microcontroller. It receives the *on* / *off* control signal of the BDS (*In*) from the high level controller (DSP or microcontroller) and the sign of the output phase current signal (*Isign*). Both variables, *In* and *Isign*, are 0 / 5 V logic signals referenced to *Ref1*. Around the PIC microcontroller, auxiliary passive components are included in SMD format (20 MHz quartz oscillator and decoupling capacitors). The algorithm implemented in the PIC generates the two control signals corresponding to the two switching devices assembled in the power stage from the *In* and *Isign* signals. This algorithm is a simplified version of the well-known "four step" current commutation strategy [60] and has already been described in reference [106]. The two 0 / 5 V output signals of the PIC (O_1 and O_2) are sent to two Agilent HCPL-J312 opto-drivers. These components combine an optocoupler with an IGBT gate driver circuit in the same package. The driver decoupling capacitors required to ensure the IGBT input capacitance charging

and discharging processes, are also assembled in SMD format. Both driver output signals (G_1 and G_2) are finally sent to the BDS power stage. Between the drivers and the IGBTs gate terminals, the gate resistors (*Rg1* and *Rg2*) are physically placed in the power substrate. The gate resistors are responsible of the switching speed of the IGBTs and their final value will influence not only the switching losses of the converter, but also the required delays implemented by the commutation strategy algorithm. On the same power substrate, a transient voltage suppressor (TVS) device is connected between gate and emitter terminals of each IGBT (*Dz1* and *Dz2*) in order to protect their gate structure.

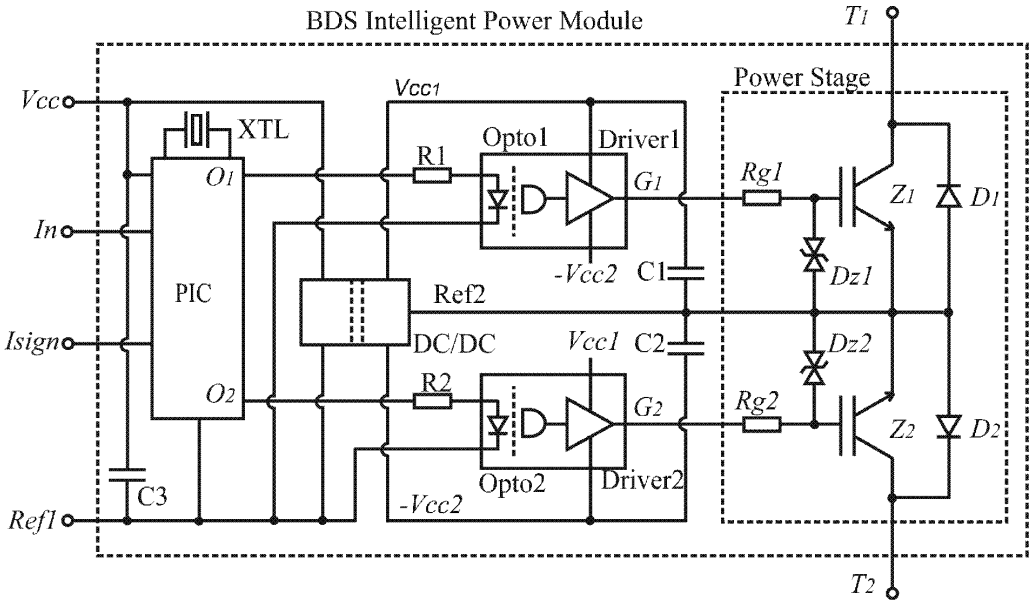


Figure 6-2 Schematic circuit of the bidirectional switch power module

As stated before, the BDS power stage of the initial prototype is connected in common emitter configuration. This scheme has been preferred instead of the common collector one, in order to simplify the requirements for the floating voltage power supplies required by the drivers. Using a single insulated voltage supply with two symmetric outputs *(+Vcc1* and *-Vcc2*), the gate-to-emitter control voltages of both IGBTs of the BDS can sweep between the positive and negative voltages (+15 V and -15 V). The TDS0515 DC/DC converter from Traco company is selected in the present implementation.

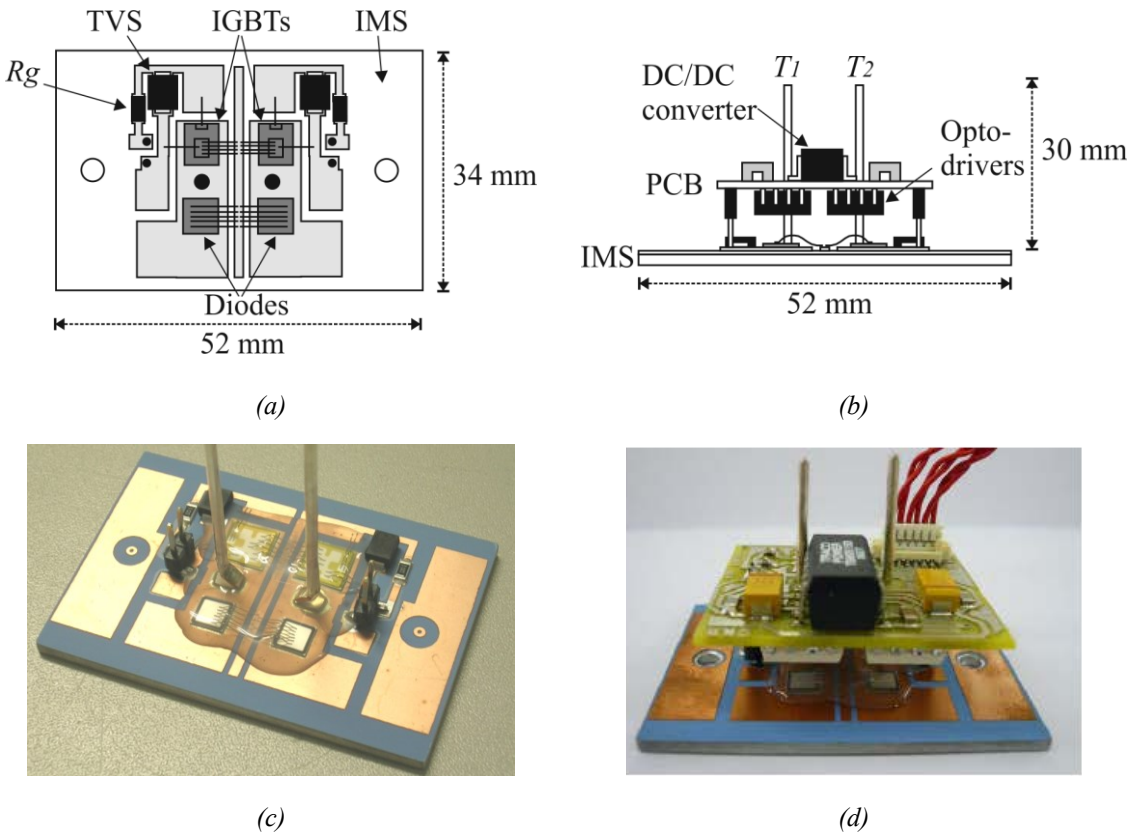


Figure 6-3 Structure and dimensions of the BDS module. a) Scheck top view of the IMS substrate showing the two pairs of IGBT and diode chips, gate resistors and TVS protection devices. b) Scheck lateral view showing the IMS substrate on the bottom with the power stage and the PCB with the control circuitry on top. c) Realisation of the power stage of a BDS module. d) Picture of a whole assembly of BDS module prototype including the power and control stage.

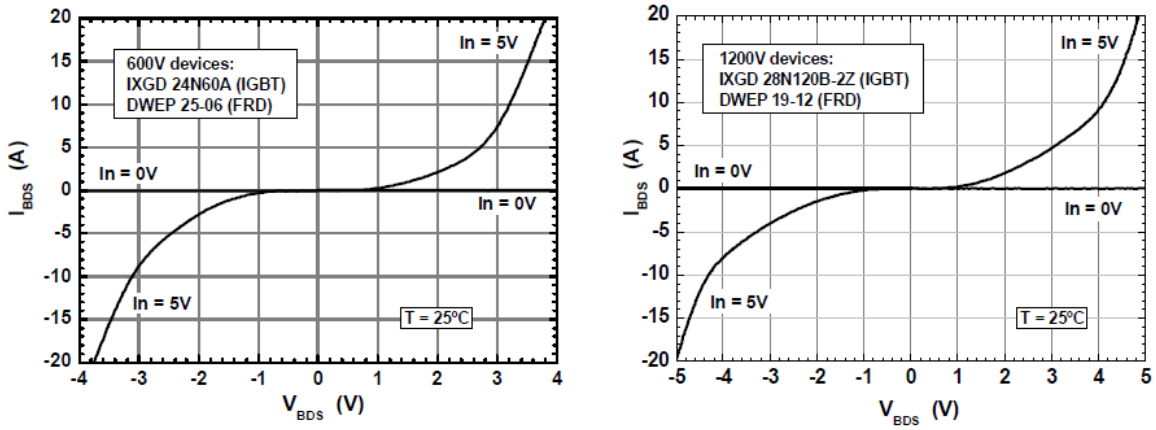
Figure 6-3 shows two drawings and a picture of the practical module prototype. The lateral view of Figure 6-3b shows the Insulated Metal Substrate (IMS) on the bottom of the assembly with the IGBTs and diodes soldered in bare-die format. This improves their thermal behaviour as the additional thermal resistance of the package (SMD, for example) is eliminated. The power devices are connected with 127 µm Aluminium bond-wires, as it can also be observed in the top-view of the substrate of Figure 6-3a, and they are protected in the prototypes with a silicone glob-top as appreciated in the power stage realisation of Figure 6-3c. Figure 6-3d shows a picture of the whole assembly with the control board on top of the IMS. The DC/DC converter and their decoupling capacitors, the power terminals T_1 and T_2 and the signal connector can be clearly appreciated on the top side of the PCB. The bottom side of the control PCB (Figure 6-3b) also accommodates the two opto-drivers and the PIC microcontroller (which is behind the opto-drivers and cannot be observed).

6.3. BDS-IPM Electrical Characteristics

6.3.1. BDS-IPM Static Characteristics

Two power stages have been implemented using 600 V and 1200 V breakdown voltage devices. IXGD 28N120B-2Z IGBTs and the DWEP 19-12 diodes, both 1200 V devices, are selected from the power devices under test of Table 3-1 in chapter 3. They fulfil the trade-off between relative low on-state voltage and fast dynamic response IGBT together with a soft recovery characteristic diode. Likewise, 600 V devices, IXGD 24N60A IGBTs and the DWEP 25-06 diodes are also integrated in a power module in order to compare both realisations. Figure 6-4 shows the I-V static output characteristics of both BDSs at 25 ºC. The first point to stress from these figures is the bidirectional current capability of the module when the input control signal is activated (*In* = 5 V), and the bidirectional voltage withstanding capability when the BDS is off (*In* = 0 V).

The second relevant point derived from the I-V curves is the relatively high value of the forward voltage drop compared with that of standard unidirectional power switches. This is also a predictable result as the BDS voltage drop comes from the series association of the IGBT and diode on-state voltages. Obviously, this effect is more pronounced for higher breakdown voltage devices, i.e. 4.8 V at 20 A for the 1200 V BDS instead of the 3.8 V at the same current shown by the 600 V BDS. In conclusion, the conduction power losses of the BDSs constitute one of the critical points of MC application.



(a) *(b)*

Figure 6-4 Static I-V characteristics of the BDS showing its voltage and current bidirectional capability. a) I-V curves using 600V devices. b) I-V curves using 1200V devices.

6.3.2. BDS-IPM Dynamic Characteristics

Another critical point of MCs is the current commutation process between BDSs. When a conducting BDS has to be turned-off, the appropriate non-conducting BDS has to be previously turned-on to allow circulating the inductive output current of the MC. More or less complex and performing commutation strategies have been developed and many references about this topic can be found in the literature [5], but for the BDS prototypes developed in this work, the four-step strategy (probably the most spread one) has been implemented in the PIC microcontrollers of the module local control. As the current commutation processes involve always two BDSs, the analysis of all the switching phenomena associated to such processes can be tackled with the switching test circuit of Figure 6-5 which was previously introduced and described in chapter 3. The voltage source V_{ab} is adjusted to reproduce the voltage difference between both BDS when they are connected to their respective phases in an n-phase grid. On the other side, the inductance L_L represents the load (of inductive nature in almost all practical applications). The sign of output current is positive when the current flows towards the load.

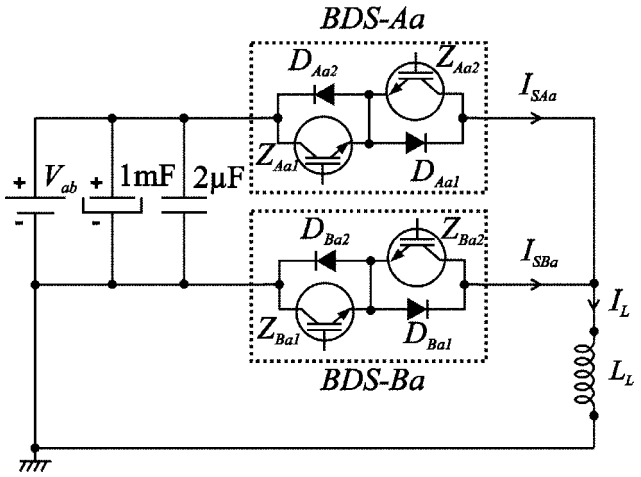


Figure 6-5 Schematic of the switching test circuit used to validate the commutation processes between BDS modules.

The different waveforms of Figure 6-6 show the evolution of the main control signals of the BDSs represented in Figure 6-5 when a pulse is applied to the input signal of *BDS-Aa* for positive (*Isign-A* = 5 V) and negative (*Isign-A* = 0 V) output phase currents. Figure 6-6a and Figure 6-6c correspond to the commutation scenario with $I_L > 0$, and Figure 6-6b and Figure 6-6d with $I_L < 0$. In Figure 6-6a and Figure 6-6b are represented

the logic control signals of *BDS-Aa* (*In-A* and *Isign-A*) and the gate-to-emitter voltages of both IGBTs of *BDS-Aa* (*GAa1* and *GAa2*). It should be noted that *In-A*, *Isign-A*, *GAa1* and *GAa2* are signals represented in Figure 6-2 particularised for *BDS-Aa* case. It is not shown in Figure 6 6a as a matter of availability of the scope channels, but an opposite control signal to *BDS-Aa* is applied to *BDS-Ba* in order to switch the BDS off. Figure 6-6c and Figure 6-6d show the evolution of the four gate to emitter voltages involved in the commutation processes. The four-step commutation strategy has been extensively explained in the literature [60]. The way it is implemented can be followed in Figure 6-6a and Figure 6-6c for *BDS-Aa* to *BDS-Ba* commutation and assuming a positive I_L. Prior to the commutation instant:

- *BDS-Aa* is conducting through the Z_{Aa1} IGBT and the D_{Aa1} diode in series with it.
- Z_{Aa2} is gated-on but it is not conducting, since $I_L > 0$.
- Z_{Ba1} and Z_{Ba2} are gated-off.

When *In-A* is set to *off*:

- the non-conducting Z_{Aa2} of the active BDS is turned-off, *GAa2* signal is *off*.
- the incoming conducting Z_{Ba1} is turned-on, *GBa1* signal is gated *on*.
- the active Z_{Aa1} IGBT of *BDS-Aa* is turned-off, *GAa1* signal is *off*, so that *BDS-Ba* begins to conduct the current.
- Finally, the inactive device Z_{Ba2} is turned-on, *GBa2* signal is active, in order to allow bidirectional current capability.

The commutation scenario with I_L negative can be also examined from the signals of Figure 6-6 in a similar way than for I_L positive.

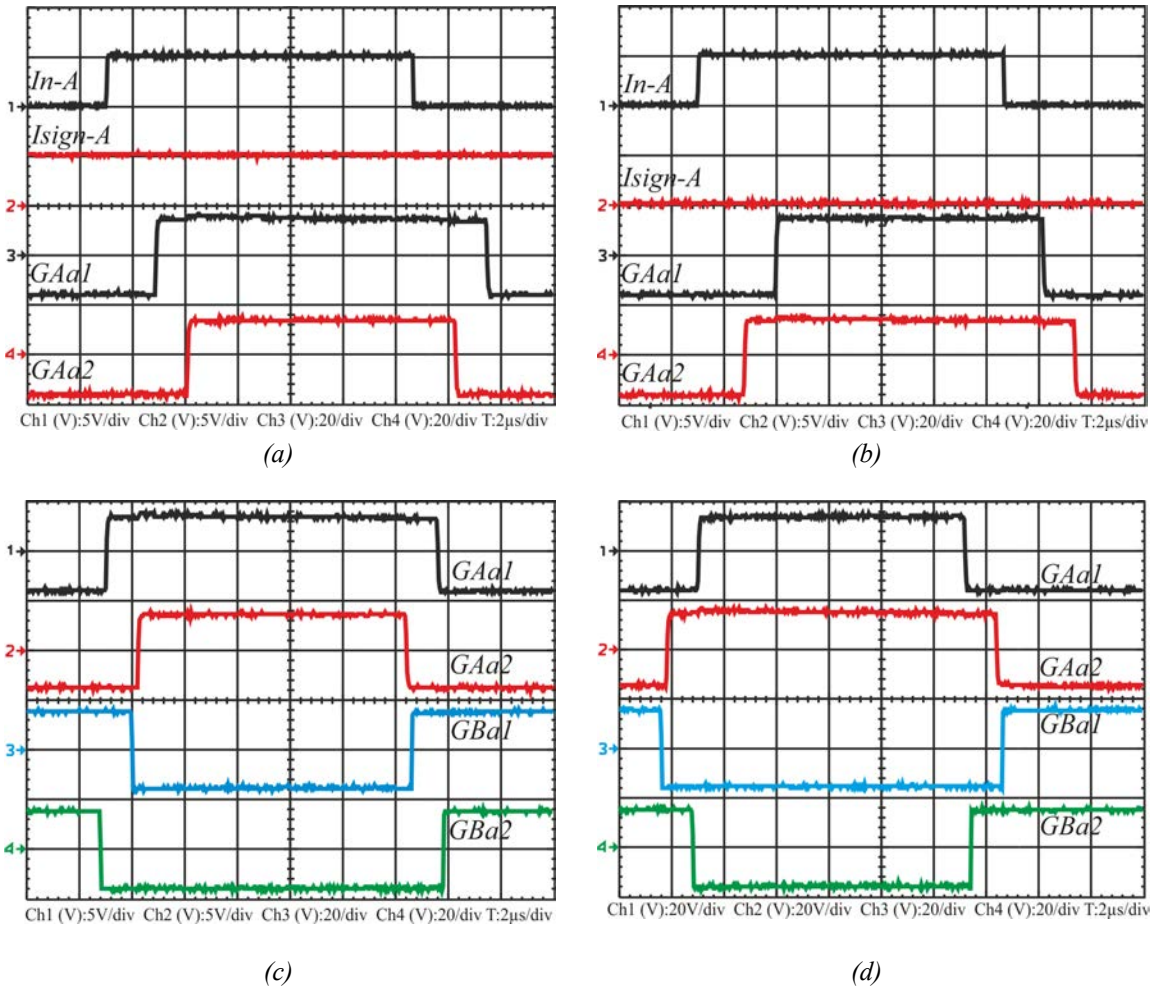


Figure 6-6 Control signals showing the generation of the commutation sequence of the IGBTs depending on the sign of the phase current. a) Gate voltages of BDS-Aa for $I_L > 0$. b) Gate voltages of BDS-Aa for $I_L < 0$. c) Gate voltages of BDS-Aa and BDS-Ba, $I_L > 0$. d) Gate voltages for BDS-Aa and BDS-Ba, $I_L < 0$.

Two BDS modules (using the mentioned 1200 V power devices) are tested in the switching circuit of Figure 6-5 at 25 A and an applied voltage of 300 V. The evolution of the currents and voltages across both BDSs as well as the associated power losses of *BDS-Aa* are shown in Figure 6-7. The commutation processes depicted in Figure 6-7a occur when *In* signal is set *on* and I_L is positive. The result of *BDS-Ba* to *BDS-Aa* commutation (Figure 6-7a) is characterised by a hard turn-on in Z_{Aa1} and by a soft turn-off in the opposite device (Z_{Ba1}). As explained in chapter 3, the turn-off recovery feature of the opposite diode (D_{Ba1}) is appreciated in I_{SAa} current as added peak current. On the other hand, when *In* signal is set *off* and I_L is positive, the commutation processes depicted in Figure 6-7b happen. A hard turn-off is undergone by Z_{Aa1} and a soft turn-on

by Z_{Ba1}. The typical voltage overshot described in chapter 3 is appreciated in the *BDS-Aa* voltage waveform in Figure 6-7b.

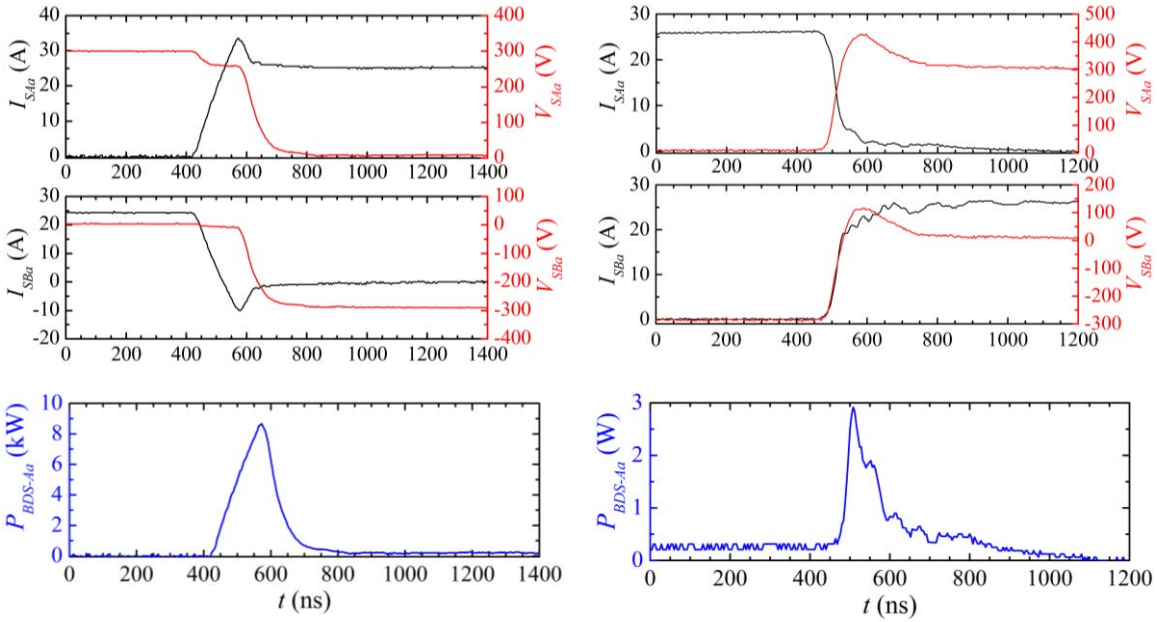


Figure 6-7 Characteristic current and voltage switching waveforms of a BDS module (1200 V rated devices) at V_{ab} = 300 V, I_L = 25 A. a) Hard turn-on commutation type. b) Hard turn-off commutation type.

Table 6-1 summarises the main switching parameters of the fabricated BDS module prototype.

IGBT	Diode	E_{on} [mJ]	E_{off} [mJ]	T_{on} [ns]	T_{off} [ns]	BDS Characteristics
4	7	1.19	0.28	334	264	High speed IGBT + fast recovery diode

Table 6-1 Switching characteristics of the BDS module prototype at V_{ab} = 300 V, I_L = 25 A

The knowledge of T_{on} and T_{off} times is relevant to set the suitable delay or commutation times in the current commutation strategy, e. g. the four-step. It should be noted that the commutation time has an important impact on the distortion of the output waveforms as reported in [107, 108].

6.4. Application Example of the BDS-IPM: Three-Phase to One-Phase Matrix Converter

In order to validate the proposed BDS intelligent power module in real operation conditions, a three-phase to one-phase test MC has been implemented using three of those modules. The test converter corresponds to the structure find in one of the output phases of a more conventional three-phase to three-phase MC. The test MC is made of two blocks: the power and high level control circuits. The design and the functionality of the test converter, including the power circuit (voltage and current measurement, current direction detection circuit and protection circuit) and the high level control circuit are described in detail. Afterwards, the real operation of the BDS-IPMs under an applied three phase input voltage and at a certain level of current is also shown.

6.4.1. Test Converter Power Circuit

The power stage of the test converter includes the BDS intelligent power modules, the input filter, the protection circuit, the current direction detection and the voltage and current measuring circuit as shown in Figure 6-8. The elements of the test converter are defined:

- Three-phase input grid with four wires: one wire *N* for neutral, three others for *R*, *S*, and *T* phases. The input voltage is set between 0 to 480 V generated in a variable transformer connected to the 380 V three-phase grid.
- *FA*, *FB* and *FC* are the input protection fuses in order to avoid short circuit and overload current conditions in each corresponding input phase.
- Input LC filter is connected between the input grid and the test converter (a detailed electrical diagram is depicted in Figure 6-9a).
- *VT-A*, *VT-B* and *VT-C* are the voltage transducers (LEM LV 25-P [109]) to measure each input phase (*VA*, *VB* and *VC*) which are required by the modulation algorithm.
- Protection circuit based on a diode-clamp circuit (a detailed electrical diagram is depicted in Figure 6-9b).
- *BDS-Aa*, *BDS-Ba* and *BDS-Ca* are the BDS intelligent power modules which connect their respective input phases with the *a*-output phase.

- *CT-A*, *CT-B* and *CT-C* are the phase current transducers (LEM LAH 25-NP [110]) which are used for monitoring, measurement (I_{SAa}, I_{SBa} and I_{SCa}) and protection purposes.

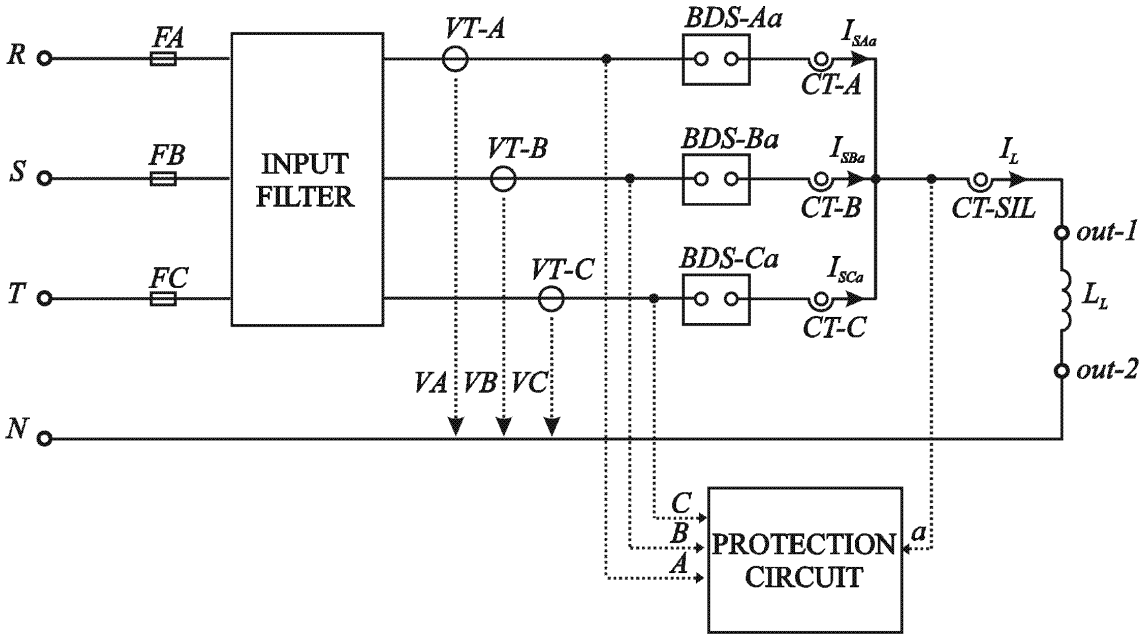
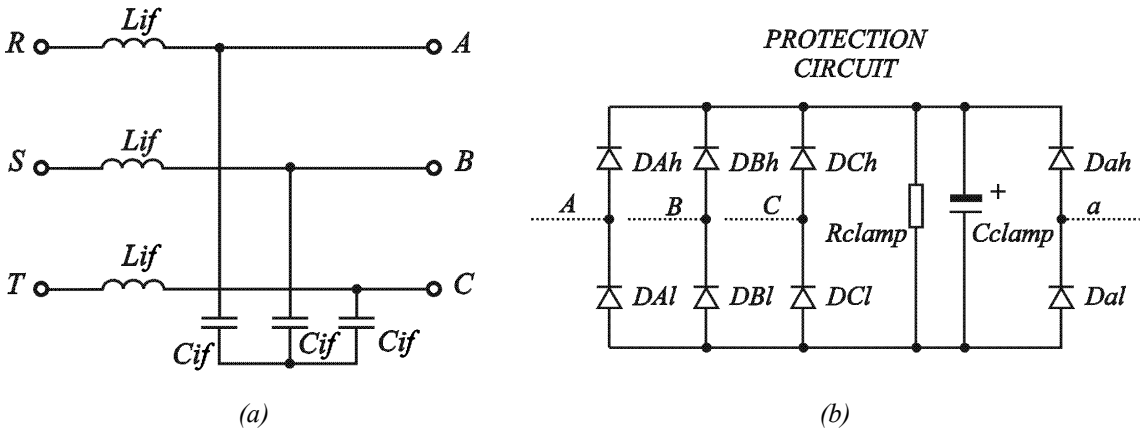


Figure 6-8 Diagram of the power circuit of the three-phase to one-phase test MC

- *CT-SIL* is another current transducer (LEM LAH 25-NP) in series with the load dedicated to obtain the sign of the output current (I_L).
- A passive inductive load (50 mH – 5 Ω) is connected between the MC output line and the neutral point.



(a) *(b)*

Figure 6-9 Schematic circuit of a) input L-C filter in star connection with inductances: 200 µH and capacitances: 100 nF. b) protection circuit

Figure 6-10 shows the used signals by the components allocated in the power circuit of the test converter. In red, the signals sent to the high level control board such as the voltage and current transducers outputs (*M-VA*, *M-VB*, *M-VC*, *M-IA*, *M-IB*, *M-IC* and *M-I*). In green, the signals sent from the high level control board to BDS modules such as BDS control signal (*SA*, *SB* and *SC* with their corresponding references) and sign of the current (*Isign*). The reference signals of the transducer are not shown for the sake of simplicity. More details are given in the following sections.

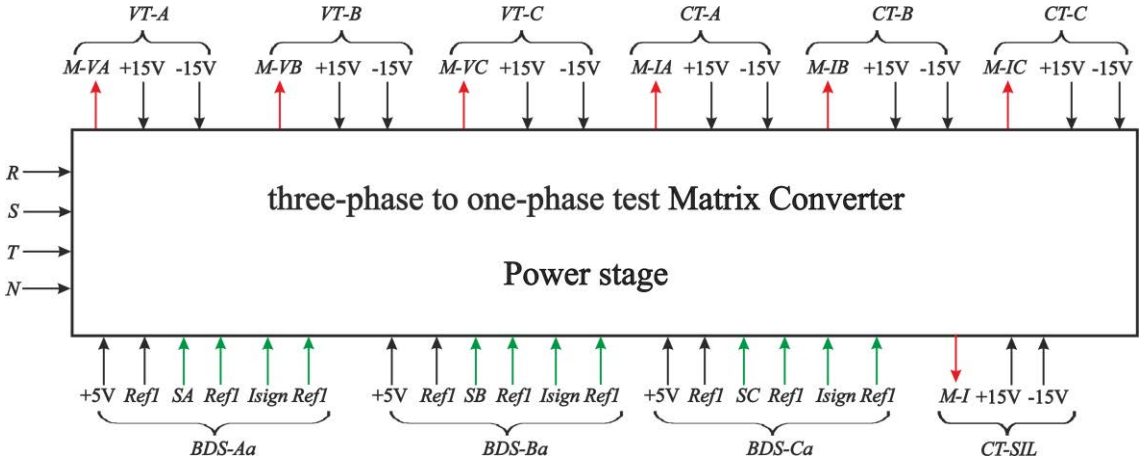


Figure 6-10 Signal diagram of the power stage

The power circuit PCB of the test converter is depicted in Figure 6-11. Several of the elements described in Figure 6-8 can be identified in Figure 6-11. Those highlighted with a continuous box are placed at the top side of the PCB whilst the components at the bottom are highlighted with a discontinuous box.

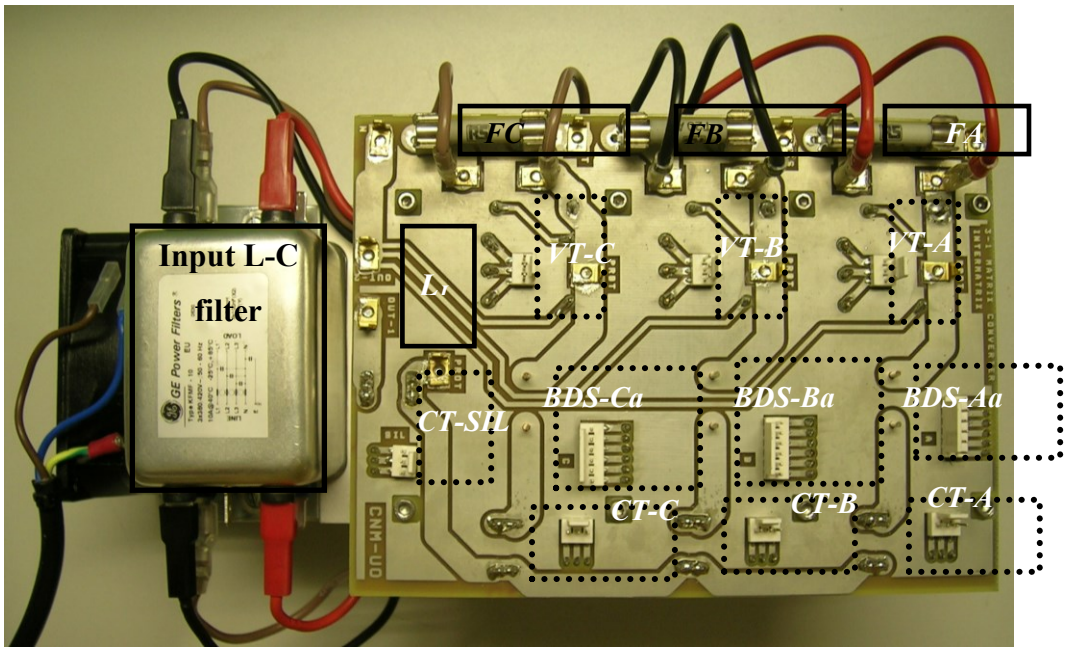


Figure 6-11 Top view of the power circuit of the three-phase to one-phase test MC

A double sided FR4 PCB with 105 µm thick Copper tracks is considered for implementing the power circuit where high current and high voltage areas are present. Likewise, the PCB layout is designed in such a way to obtain low stray inductances and to cope with the desirable current capability. It is important to have low stray inductance in order to minimise the voltage spikes generated due to the switching devices turn-off during the BDS commutation. The PCB Copper width for the current path is calculated according to [111] so that a current capability of 15 A can be safely achieve

The assembly of the power stage board and the BDS modules on the heat-sink is depicted in Figure 6-12. The purpose of the heat-sink is to transfer heat from the BDS modules to the ambient air. In order to enhance this process, a forced convection is used with a fan assembled on the heat-sink.

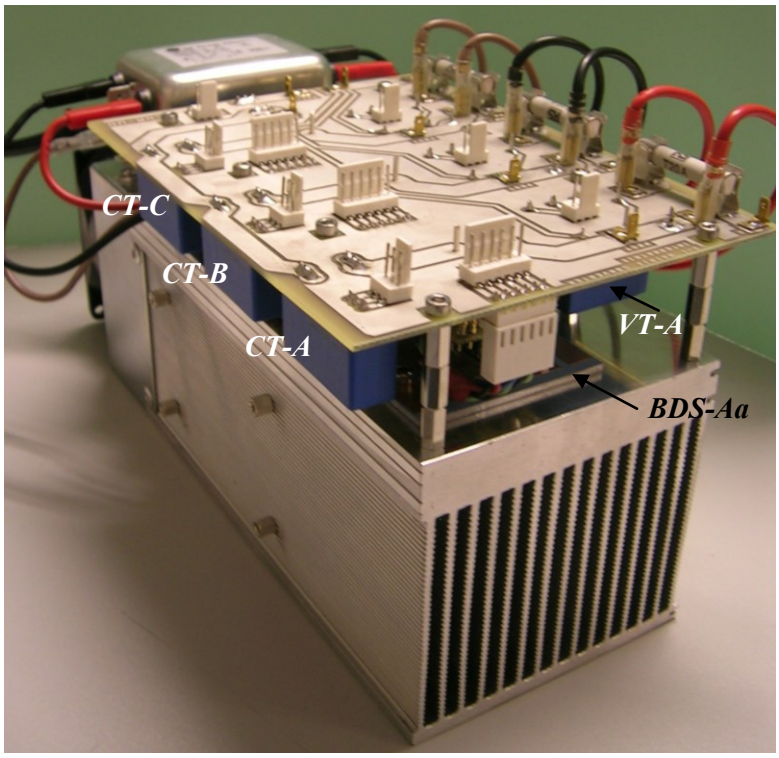


Figure 6-12 View of the heat-sink and the BDS modules

6.4.2. Measurement Circuit and Techniques

The voltage transducer LV 25-P [109] and the current transducer LAH 25-NP [110] both based in the Hall effect and manufactured by LEM are used to measure the voltage at the input phases with respect to the neutral point, the current through each BDS module and the output phase current. Figure 6-13 depicts the schematic circuit of both transducers. Both types of transducers provide a galvanic isolation between the primary circuit (high power) and secondary circuit (measuring circuit). In addition, they exhibit many features such as: an excellent accuracy, wide frequency bandwidth and high immunity to external interference.

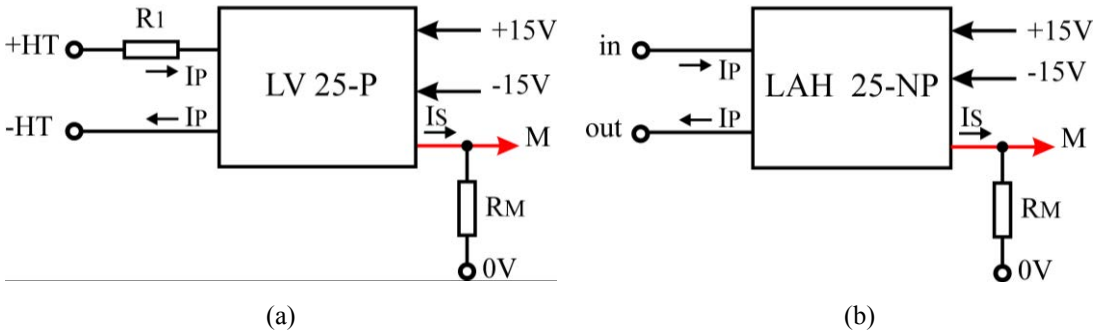


Figure 6-13 Schematic circuit of a) voltage transducer. b) current transducer

Figure 6-13a shows the voltage measurement circuit. For instance, *A* input phase voltage should be measured. So, *+HT* terminal is connected to input phase *A*, *-HT* is connected to the neutral point, an external resistance R_1 (1 kΩ) is connected in series with the primary circuit. The primary current (*IP*) which flows through R_1 is proportional to the measured voltage. The measured current leads to a secondary current (*IS*) with a conversion ratio of 2500:1000. The secondary current flows through a measuring resistance (R_M of 180 Ω) generating a voltage signal (*M-VA*) which is sent to an ADC channel of the high level control board. Before reaching the ADC, *M-VA* signal should be connected to a conditioning circuit and anti-aliasing low pass filter (Figure 6-14) in order to match to the level signal of the ADC input. The conditioning circuit is based on an inverter op-amp (operational amplifier). The gain of the anti-aliasing low pass filter is -1 and the output follows equation (6.1). Therefore, the resulting output signal will take a value between 0 and 5 V centred in the reference voltage value (2.5 V) and will be sent to the corresponding ADC channel.

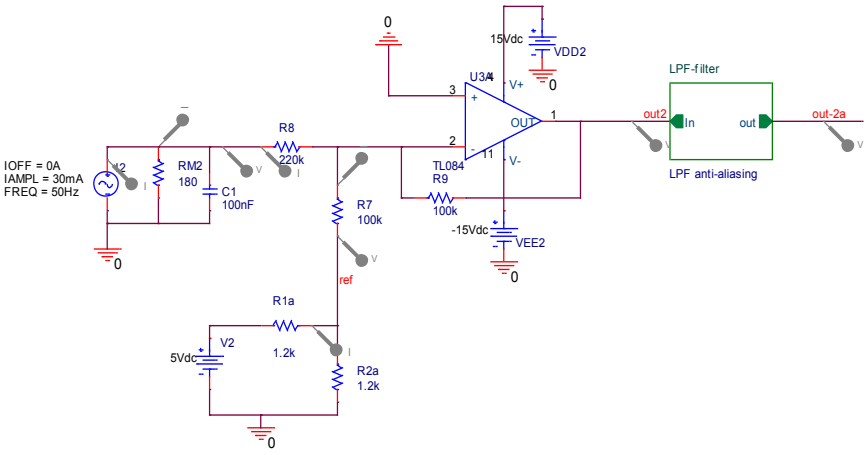


Figure 6-14 Schematic of the voltage transducer conditioning circuit

$$out\_voltage\_transducer = \frac{R9}{R8}V_M + \frac{R9}{R7}Vref \qquad (6.1)$$

The voltage measuring circuits of *B* and *C* input phases are implemented in the same way as described for *A* input phase.

The schematic of the current measurement circuit is shown in Figure 6-13b. For instance, the current through *BDS-Aa* should be measured. Thus, the primary terminals of the transducer are connected in series with *BDS-Aa*. The measured current results in a

secondary current with a conversion ratio of 1:1000. The secondary current flows through a measuring resistance (R_M) of value 220 Ω generating a voltage signal (*M-CTA*) which is sent to the ADC channel. As described in the voltage transducer case, the transducer output voltage should be conditioned in order to adapt the signal level to the ADC input channel. This task is performed by the circuit of Figure 6-15. A gain and voltage level adapter stage based on an inverter op-amp is implemented followed by an anti-aliasing low pass filter with a gain of -1. The output signal follows equation (6.2). The resulting signal will be a value between 0 and 5 V centred in 2.5 V which is sent to the ADC channel on the high level control block.

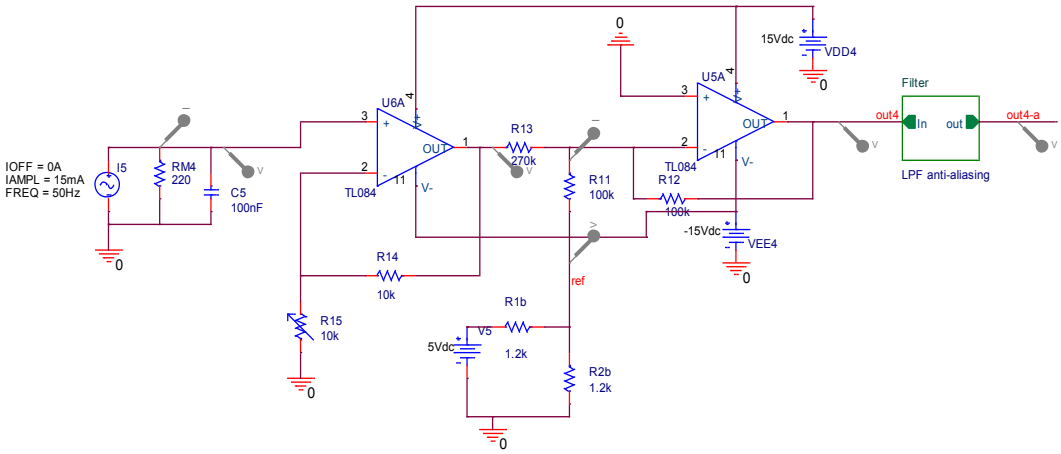


Figure 6-15 Schematic of the current transducer conditioning circuit

$$out\_current\_transducer = \frac{R12}{R13}\left(1+\frac{R14}{R15}\right)V_M + \frac{R12}{R11}Vref \qquad (6.2)$$

6.4.3. Current Direction Detection Circuit

The sign of the output phase current must be known by the BDS module in order to establish a safe current commutation based on the four-step commutation strategy described in chapter 2.

CT-SIL current transducer is located in series with the load in order to measure the output phase current. The measured current feeds an ultra-fast comparator which provides the output current direction. Figure 6-16 shows the schematic circuit which detects the current direction. The comparator used (TL3016ID) is designed to interface directly to TTL logic so that no extra conditioning electronics is needed. Hence, the comparator output signal is straight forward transmitted to the BDS modules connected

to that output phase. The comparator features a high speed operation as well as good precision and accuracy. An accurate detection of the output current direction is required in order to carry on a correct switching operation between the BDSs.

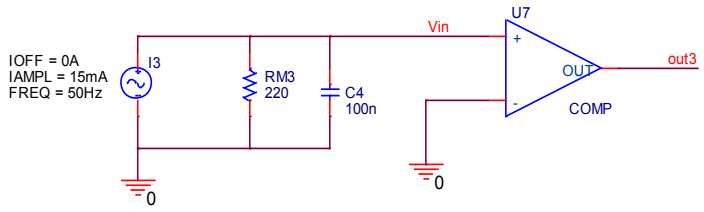


Figure 6-16 Schematic of the current direction detection circuit

6.4.4. Protection Circuit

Between the three-phase to one-phase test MC inputs and output, a diode-clamp circuit is introduced to protect the test converter from possible fault modes since no free-wheeling paths for the load current are available [105]. Thus, this protection circuit must prevent the test converter from overvoltages caused either at the input side by line perturbations or at the output side by an overcurrent fault during converter shutdown. The energy stored in the inductor load has to be discharged without any dangerous overvoltage. Therefore, a clamp capacitor (*Cclamp*) is required to take the energy stored in the inductance of the load without exceeding the maximum voltage rating of the devices. Then, the voltage is discharged through the clamp resistor (*Rclamp*). Figure 6-9b shows the schematic circuit of the protection circuit. *Rclamp* = 20 kΩ and *Cclamp* = 22 µF are the chosen values to implement the diode-clamp circuit.

6.4.5. High Level Control Circuit

The high level control board houses mainly the conditioning circuits of the voltage and current transducers, the current sign detection circuit and the digital signal controller (DSC) which is the core of the control circuit. The DSC chip, also known as dsPIC (manufactured by Microchip [112]), integrates the control attributes of a Microcontroller (MCU) with the computation and throughput capabilities of a Digital Signal Processor (DSP). The ds-PIC30F4012 chip is selected in order to implement the control of the test MC. Some of the features of this device are summarised in Table 6-2:

Device	Pins	Program Mem. Bytes/ Instructions	SRAM Bytes	EEPROM Bytes	Timer 16-bit	Input Cap	Output Comp/Std PWM	Motor Control PWM	10-bit A/D 1 Msps	Quad Enc	UART	SPI	I²C™	CAN
dsPIC30F4012	28	48K/16K	2048	1024	5	4	2	6 ch	6 ch	Yes	1	1	1	1

Table 6-2 Main features of dsPIC30F4012

The architecture of ds-PIC30F4012 enables a C compiler optimized instruction set which results in a save of program code space. In addition, this device can be in-circuit serial programming and debugging making easy the validation of the code.

Figure 6-17 illustrates the block diagram of the implemented high level control board. The computer hosts the MPLAB® Integrated Development Environment (IDE) software. It allows editing, building and debugging in an easy way the code of the MC control. Then, the MPLAB ICD 2 is the hardware which enables the communication between the dsPIC device and the PC via an USB connection. MPLAB ICD 2 can operate as in-circuit debugger and as in-circuit serial programmer. Running under MPLAB IDE, MPLAB ICD 2 can debug assembler (ASM) or C source code, watch and modify variables, single step and set breakpoints.

The voltage signals required to implement the control algorithm are provided by the measurement circuits of the input phase voltages. The current signals required to monitor the current phases are provided by the measurement circuits of the phase currents. Once these signals are conditioned, they are transferred to the six analog input channels of the 10-bit high speed ADC (Analog to Digital Converter) module of the dsPIC device. The values of the input voltages are needed to compute the duty cycle of each BDS control signal (*SA*, *SB* and *SC*) according to the classical Venturini modulation algorithm [113]. As the goal of this converter is to validate for the first time the operation of several BDS modules together in the same MC, a simple modulation algorithm has been preferred, although additional tests implementing other modulation algorithms are foreseen in the future. The source code for the control of the test matrix converter has been developed in C language for the Universidad de Oviedo (UO) in the framework of collaboration with IMB-CNM (InterMatrix Project). The sign of the output phase current is provided by comparing the *M-I* value. The resulting output logic signal (*Isign*) is sent to the three BDS modules in order to implement the four-step current commutation technique.

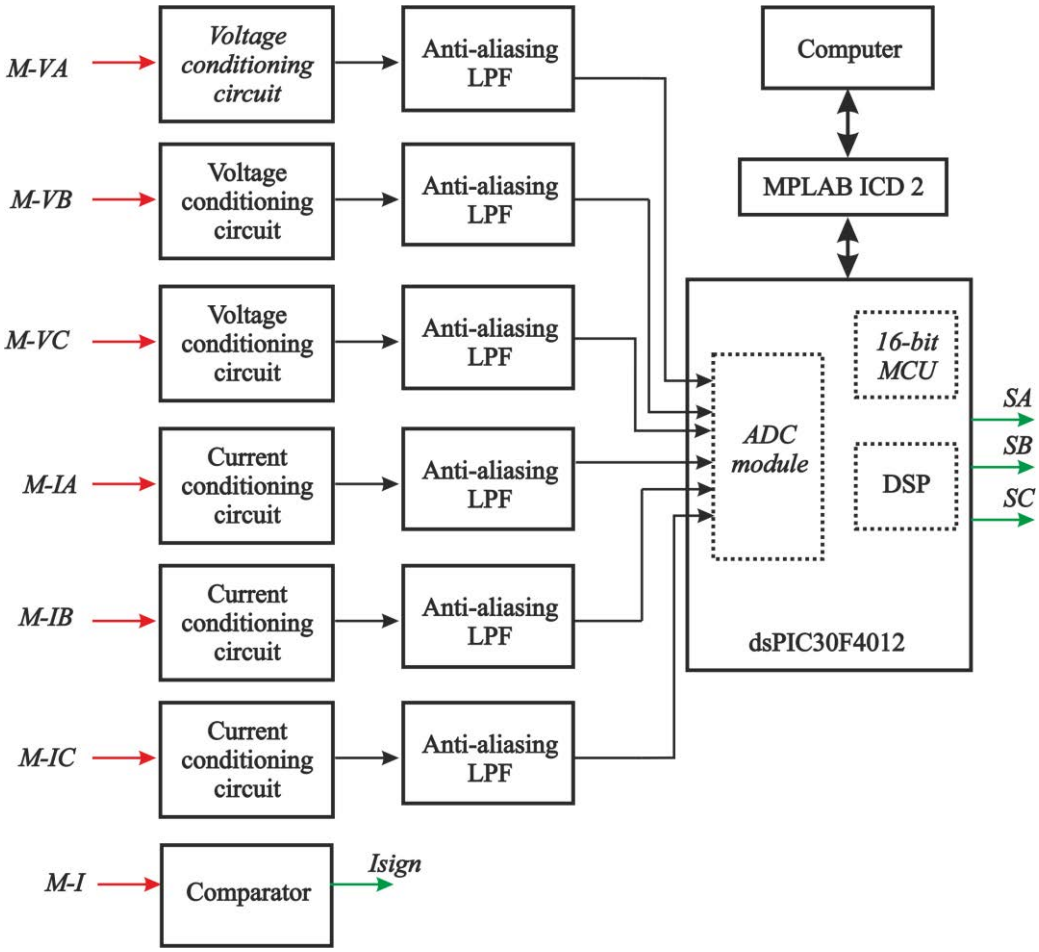


Figure 6-17 Block diagram of the high level control board

Figure 6-18 illustrates the top layer of the high level control board of the three-phase to one-phase test MC. The control board is placed above the power circuit board by means of spacers and screwed at the top to make the whole a rigid structure as shown in Figure 6-19. There is a safety distance between the power circuit PCB (high voltage) and the control PCB (low voltage) in order to avoid any electrical breakdown due to high voltage differences.

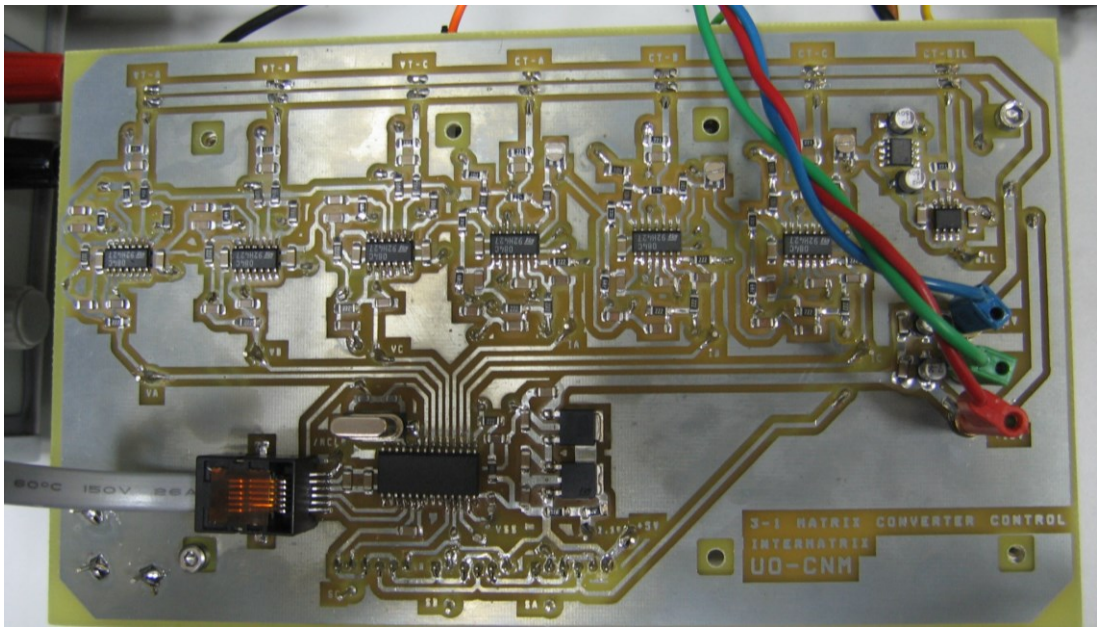


Figure 6-18 Fabricated control board of the three-phase to one-phase test MC

The signal connectors of the current transducers as well as of the control BDSs can be appreciated in the power PCB of picture Figure 6-19.

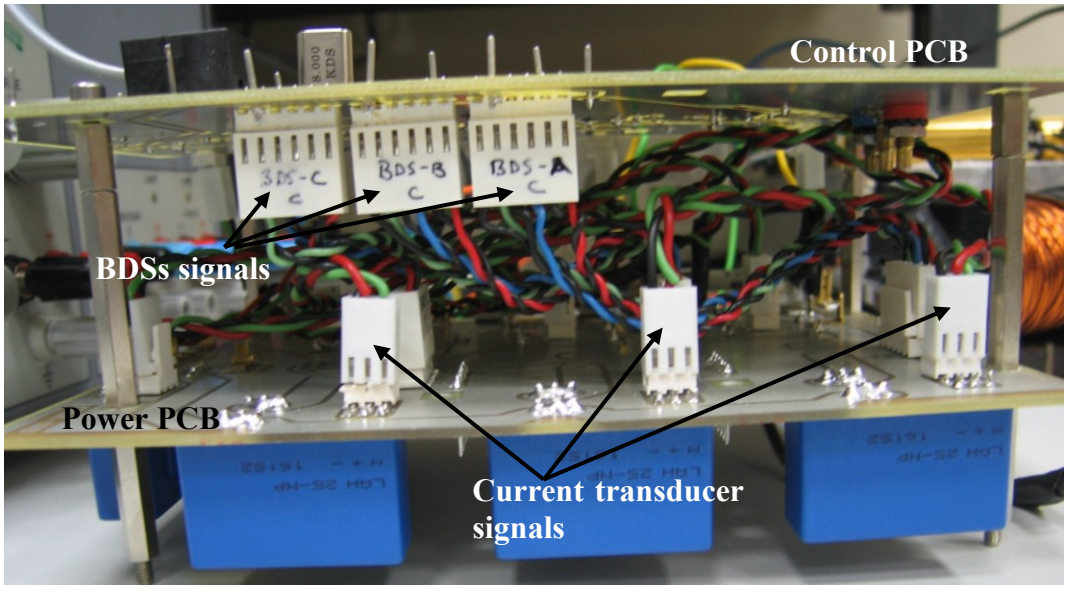


Figure 6-19 Mechanical and electrical assembly between the control and the power boards

It should be noticed that in general, the overall structure of a high level control implementation for the MC is based on a digital signal processor and a field programmable gate array (FPGA). In our implementation, part of the control performance which is closer to the BDS functionality (strategy current commutation) is

carried out by the proposed intelligent BDS module. This fact allows the development of a less complex MC control board and represents a step forward towards the feasibility of intelligent BDS components for the implementation of a MC and others converters with a power bidirectional requirement.

6.4.6. Experimental Behaviour of the BDS-IPMs in a Test MC

The most characteristic waveforms of the test MC under real operation conditions when the 3-phase input voltages show 200 V amplitude is depicted in Figure 6-20. The "chopped" output voltage waveform can be observed on the top of Figure 6-20. This voltage induces the output current waveform through the load shown in the second plot, with a 100 Hz frequency and 5 A peak-to-peak amplitude. The sign of the output current logic signal is also represented placed on top of the current signal itself. The high level control board computes and sends directly the 0 – 5 V logic control signals to the inputs of the BDSs (*SA*, *SB* and *SC* respectively). These three signals can be observed at the bottom of Figure 6-20. Additional tests are ongoing in order to increase the output current, the output voltage and the switching frequency, although the preliminary results shown in Figure 6-20 demonstrate the suitability of the proposed approach.

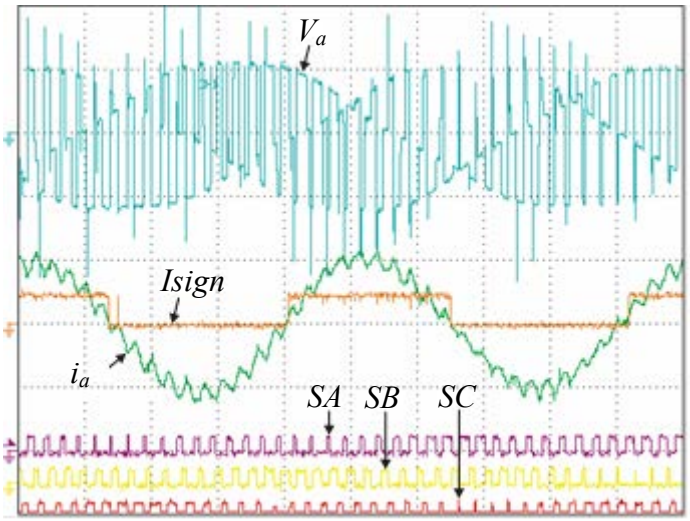


Figure 6-20 Characteristic waveforms of the test MC. Switching frequency 2 kHz. Input voltages 200 V – 50 Hz, i_a output current 5 A peak-peak – 100 Hz. i_a: 2.3 A/div. V_a: 200 V/div. Time: 2 ms/div.

6.5. Summary

This chapter shows the structure, main characteristics and an application example of a new intelligent power module prototype implementing the bidirectional switch (BDS) function, in order to make easier the realisation of matrix converters. The power stage of the module is based on two IGBTs and two diodes in common emitter configuration. This configuration allows obtaining positive and negative gate control voltages using only a double-output insulated power supply for the entire BDS. Others power stages of the BDS based on SiC devices (diodes and transistors) or two RB-IGBTs arranged in anti-parallel can be also implemented.

The prototype presented is intended for low and medium power applications and is based on an insulated metal substrate (IMS), containing the power semiconductor devices (bare die) and other auxiliary components (transient voltage suppressors, gate resistors, etc.). On top of the IMS, the control board includes a local control device (a PIC microcontroller in the presented prototype) to manage the input control signals and to establish the commutation strategy, the gate drivers of the power stage IGBTs and their floating voltage power supplies (a high density DC/DC converter).

Two power stage substrates have been developed using 600V and 1200V devices respectively. Their I-V static curves show the four-quadrant operation capability of the BDS and the relatively high values of forward voltage drop, a common problem to all BDSs based on the combination of unidirectional switches. Concerning the switching operation, it has been shown how the module safely implements the four-step commutation strategy from the control BDS and the sign of current logic signals. The total commutation time observed at the gate-to-emitter voltages is 3μs. The corresponding commutation waveforms of the BDS (current and voltage) have been obtained in the switching test-bench of chapter 3 under high relative power conditions (300 V and 25 A), showing the expected behaviour.

Finally, the design and the functionality of the three-phase to one-phase test converter, including the power circuit, voltage and current measurement circuit, current direction circuit, protection circuit and the high level control circuit have been described in detail. The first results of three BDS intelligent power modules operating in the aforementioned test matrix converter have also been shown.

As the present work has been mainly addressed to validate the global approach of integrating the BDS function in an intelligent power module, additional efforts will be necessary in the future to improve this basic idea. Ongoing works will deal with the improvement of both, the power and control stages of the module. Concerning the power stage, ceramic substrates (DCB) are under study to increase the power capability of the modules. Temperature sensors will be also included at this level. On the other hand, the control board is being improved by using gate drivers with short circuit protection capability, enhanced commutation strategies oriented to minimise the commutation times and to improve the operation in the current reversal region, and optimised management of the fault conditions (protection against IGBT short-circuits, BDS over-voltages, power substrate over-temperatures, etc.).

7. Summary and Conclusion

The Matrix Converter (MC) is a single-stage converter which carries out a direct AC-AC conversion by means of a matrix of bidirectional switches (BDS) to connect each input phase to each output phase at a relatively high switching rate. This topology doesn't require bulky passive storage components (i.e., electrolytic capacitors) as in more conventional converter topologies, providing a very compact and efficient solution for direct AC-AC industrial systems demanding bidirectional power flow capability, in particular in the renewable energies and smart-grid fields (wind turbines, static transformers, etc.). Nevertheless, some technical problems arise for the practical implementation of MC in field applications. Many of them are related with the big number of semiconductor power devices involved in the structure, their control, assembly, protection, and thermal management.

BDS power modules are the key elements to enable the medium and high power MC applications due to their inherent four-quadrant operation as an AC power switch, in which the power is able to flow from the input source to the load and vice-versa. BDSs are implemented by the combination of power devices, typically two IGBTs and two diodes in common emitter or common collector arrangement. This means that for a three-phase to three-phase MC, eighteen IGBTs and eighteen diodes are required and their switching processes occur under variable current and voltage levels, becoming very difficult to model and describe. Consequently, very critical topics such as power losses prediction are difficult to undertake.

In this framework, the main aim of this work was the analysis of the commutation processes in BDSs, the prediction of their power dissipation in typical MC operation and the development of a new controlled bidirectional switch module which integrates the power stage functionality with the intelligence in one component to enhance the modularity and feasibility of MC applications.

First of all it is important to understand how the bidirectional switches within the MC behave. A SPICE simulation work of a simplified two-phase to single-phase MC was performed in order to analyse the commutation phenomena involved between BDSs. Hard and soft commutations are undergone by the different power devices depending on the voltage across the BDS and the direction of the current through it.

Understanding the details of the switching processes allow an optimum definition of the commutation strategies within BDSs and modelling of the switching power losses.

The static and dynamic characteristics of several BDSs implemented with discrete devices of different technologies, have been analysed. A switching test circuit based on the aforementioned two-phase to single-phase MC has been fabricated for this purpose. In this test MC it is possible to test BDSs in common emitter configuration, BDSs based on reverse-blocking IGBTs (RB-IGBTs) as well as BDSs integrated in power modules sharing the same power stage and control board. Based on the extracted measured data of the BDSs devices, their conduction and their switching losses have been accurately modelled. It has been shown that switching losses cannot be considered linear function of the voltage and current. When this widely spread approach is accounted an important error is made. In this sense, we proposed the two-dimensional polynomial fitting of the switching energy losses as the most suitable method for describing their dependence with voltage and current across the device. It has been also found that soft switching losses cannot be directly neglected since they strongly depend on the fabrication technology of the power device (for example, for the RB-IGBT). Hence, a proper analysis should be performed to consider or not negligible the soft switching losses.

This research work has also described the implementation of a computational method to evaluate the conduction and switching losses (hard and soft types) of the power devices within the bidirectional switch when they are operating in a MC. Based on the conduction and switching losses models, the power losses of the semiconductor devices are calculated depending on different operating condition of the MC such as the modulation algorithm, the output frequency, the output to input voltage ratio (i.e. modulation index), the load power factor and the switching frequency. Likewise, a power losses analysis of several BDSs built with power devices from different technologies has been also carried out. All these studies have resulted in a practical tool to help the converter designer to select the optimum power devices for a given application, and to predict in an accurate way the semiconductor power losses in order to size and implement the suitable cooling system. These are the main examples of the outcome of the implemented losses calculation method, but the proposed approach has a big potential for analysing other aspects related with BDS and MC implementation, such as the analysis of the impact of different control and modulation strategies on the power losses.

Finally in this work, an integrated bidirectional switch intelligent power module (BDS-IPM) prototype was designed, built and tested in order to take a step forward in the practical implementation of matrix converters. This power module is not limited to this application, and it is suitable for any application demanding a bidirectional power flow capability and being part of an intelligent power system. The BDS-IPM is itself a complex power electronics system since many disciplines converge in it: power semiconductor devices, thermal / power management, device level control (i.e. gate drive circuits) and high level control (i.e. current commutation strategy implementation, active protection issues). Some of these aspects have been only partially analysed and they need additional efforts for obtaining optimum results, consequently, a lot of interesting and fascinating work is still pending to try to improve the BDS-IPM capability.

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A. Lists of Acronyms and Symbols

A.1 List of Acronyms

AC	Alternating Current
ADC	Analog to Digital Converter
BDS	Bidirectional Switch
BDS-IPM	Bidirectional Switch Intelligent Power Module
BJT	Bipolar Junction Transistor
BN	Boron Nitride
CC	Common Collector
CE	Common Emitter
DB	Diode Bridge
DC	Direct Current
DSC	Digital Signal Controller
DSP	Digital Signal Processor
FRED	Fast Recovery Epitaxy Diode
GaAs	Gallium Arsenide
GaN	Gallium Nitride
HEMT	High-Electron-Mobility Transistor
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IMS	Insulated Metal Substrate
J-FET	Junction- Field Effect Transistor
LPF	Low Pass Filter
MC	Matrix Converter
MCU	Microcontroller
MCT	MOS-Controlled Thyristor
MOSFET	Metal-Oxide-Semiconductor-Field-Effect-Transistor
NTC	Negative Temperature Coefficient
RB-IGBT	Reverse Blocking Insulated Gate Bipolar Transistor
SBD	Schottky Barrier Diode

Si	Silicon
SiC	Silicon Carbide
TCAD	Technology Computer Aided Design
VSI	Voltage Source Inverter
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
PCB	Print Circuit Board

A.2 List of Symbols

a_{device}	Fitted parameter provided from I/V characteristic (conduction resistance)
b_{device}	Fitted parameter provided from I/V characteristic
d_{01}, d_{02}, d_{03}	Duty-cycle of the three zero switch configurations
d_I, d_{II}, $d_{III,}$ d_{IV}	Duty-cycle of the four active switch configurations
D_{device}	Device IGBT duty cycle
DS SVM	Double-sided space vector modulation
E_{off}	Turn-off energy losses
E_{on}	Turn-on energy losses
$E_{hoff/device}$	IGBT or diode dissipated hard turn-off energy
$E_{hon/device}$	IGBT or diode dissipated hard turn-on energy
$E_{soff/device}$	IGBT or diode dissipated soft turn-off energy
$E_{son/device}$	IGBT or diode dissipated soft turn-on energy
f_{out}	Output voltage frequency
f_{sw}	Switching frequency
i_a	Output a-phase current
i_{af}	Output fundamental a-phase current
i_A, i_B, i_C	Input a,b,c-phase currents
i_{Aa}	Current through S_{Aa} BDS
i_b	Output b-phase current
i_{Ba}	Current through S_{Ba} BDS
i_c	Output c-phase current

i_{Ca}	Current through S_{Ca} BDS
i_{ZA1}	Current through Z_{1A} IGBT
I_M	Output current amplitude
I_C	Collector current
I_L	Load current
I_{rr}	Maximum reverse current
q	Voltage transfer ratio
Q_{rr}	Reverse recovery charge
M	Modulation depth index
p	Instantaneous dissipated power
$p_{cond/device}$	Instantaneous conduction dissipated power
$p_{hoff/device}$	Instantaneous hard turn-off dissipated power
$p_{hon/device}$	Instantaneous hard turn-on dissipated power
$p_{soff/device}$	Instantaneous soft turn-off dissipated power
$p_{son/device}$	Instantaneous soft turn-on dissipated power
$p_{sw/device}$	Instantaneous switching dissipated power
$\overline{P}$	Total average power losses
r_{CE}	IGBT on-state resistance
R_G	Gate resistance
r_{TO}	Diode on-state resistance
S_{Kj}	Bidirectional switch which connects *K (=A, B, C)* input phase with *j (=a,b,c)* output phase
t_I, t_{II}, t_{III}, t_{IV}, t_{01}, t_{02}, t_{03}	Time interval of the switching configuration
$t_{cond/device}$	Conduction time of a device
$t_{d(off)}$	Turn-off delay time
$t_{d(on)}$	Turn-on delay time
t_f	Fall time
t_{rr}	Reverse-recovery time
T	Output current period
T_{sw}	Switching period
$V_{t/device}$	Fitted parameter provided from I/V characteristic (threshold voltage)

v_a, v_b, v_c	Output a,b,c-phase voltages
V_A	Input a-phase voltage
V_B	Input b-phase voltage
V_C	Input c-phase voltage
v_{ZA1}	Voltage across Z_{1A} IGBT
$V_{CEO}/V_{CE(ON)}$	Collector-to-Emitter saturation voltage (i.e. on-state voltage)
V_{GE}	Gate-to-Emitter voltage
$V_{GE(th)}$	Gate threshold voltage
V_{GG}^{+}/V_{GG}^{-}	Positive/Negative Gate drive voltage
$V_{t/D}/V_{t/Z}$	Diode/IGBT on-state voltage
V_{TO}	Diode on state voltage
I_i	Magnitude of the input voltage vector
V_o	Magnitude of the output voltage vector
α_o	Direction of the reference output vector
$\tilde{\alpha}_o$	The angle of the reference output vector within the sector
β_i	Direction of the reference input vector
$\tilde{\beta}_i$	The angle of the reference input vector within the sector
Δt_{off}	Turn-off transition time
Δt_{on}	Turn-on transition time
φ_i	Displacement angle of input currents with respect to input voltages
φ_o	Output current displacement angle
ω_i	Input frequency pulsation
ω_o	Output frequency pulsation

B. Switching Energy Losses Calculation

This appendix describes how the switching losses are calculated from the switching current and voltage waveforms provided by the MC test circuit of Figure 3-10. These experimental data is processed by means of several MATLAB scripts in order to obtain the switching dissipation associated to the power devices within the BDS.

B.1 IGBT

Figure B-1 represents, read_IGBT_x script, a general basic module which receives the IGBT measured switching current and voltage signals, $i_{ZAa1}(t)$ and $v_{ZAa1}(t)$, for a given test current and voltage and calculates the energy dissipation associated to the corresponding commutation type once the commutation interval ($t_{off1} - t_{off2}$ as shown in Figure B-2 in case of the turn-off) is determined. The *x* of read_IGBT_x function stands for the kind of commutation (*hoff*, *hon*, *soff* and *son*).

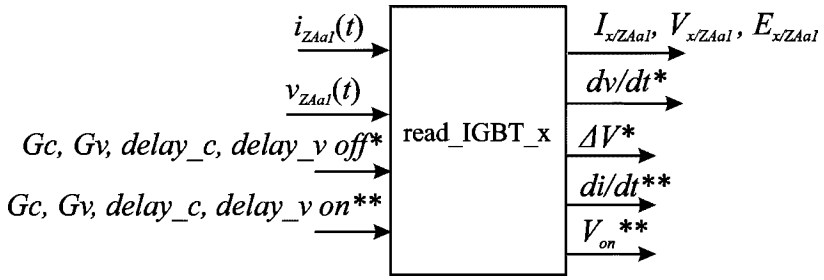
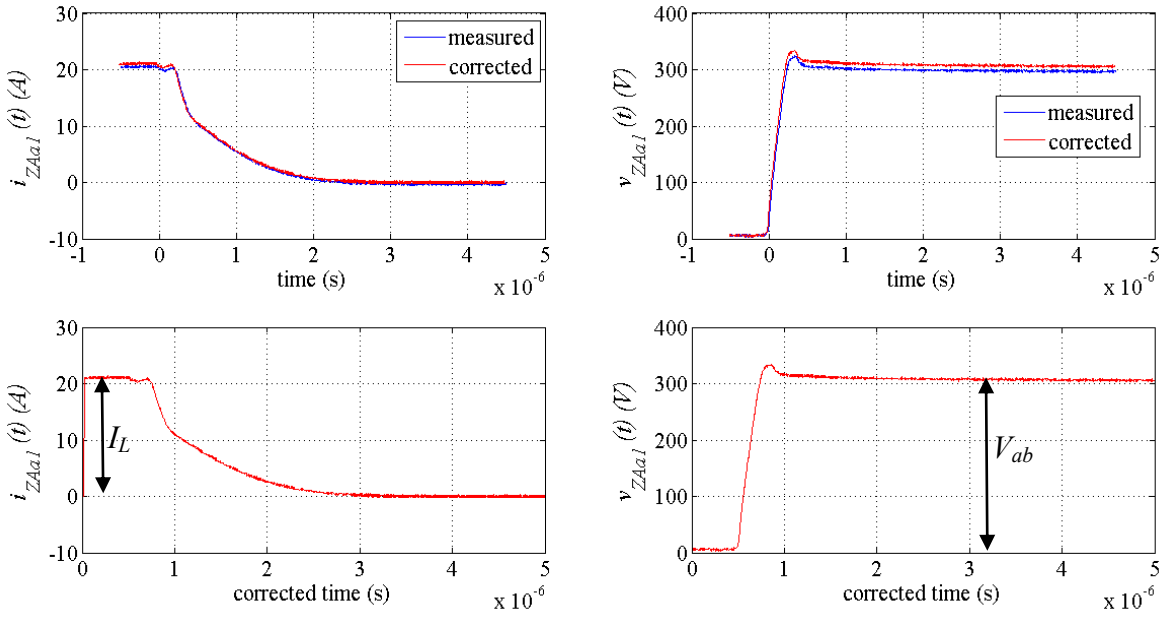


Figure B-1 Block diagram of the read_IGBT_x script

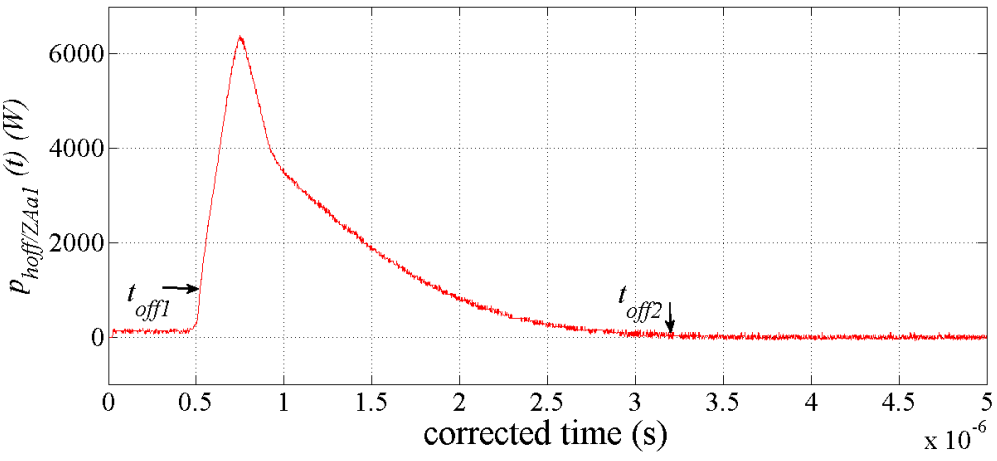
where *Gc*, Gv, *delay_c* and *delay_v* are the current probe gain correction, the differential voltage probe gain correction, the current probe time delay correction and differential voltage probe time delay correction, respectively. This set of compensation parameters are determined for the *on* and for the *off* transition as examined in chapter 3. Prior to calculate the energy losses, current and voltage waveforms are corrected in amplitude and time by means of the compensation parameters. $E_{x/ZAa1}$, $I_{x/ZAa1}$ and $V_{x/ZAa1}$ are the calculated energy losses, the current and voltage at the switching instant, respectively. *dv/dt** is the *dv/dt* value which is exhibited by the IGBT voltage during the *off* transition. ΔV* is the overvoltage generated by the parasitic inductances of the circuit during the turn-off. *di/dt*** is the *di/dt* value which is exhibited by the IGBT current during the *on* transition. V_{on}* is the IGBT on-state voltage.

* Symbol is introduced in read_IGBT_x to represent a specific output for the hard turn-off commutation, whereas ** stands one for the hard turn-on commutation. The script output for the soft commutations is only the $E_{x/ZAa1}$, $I_{x/ZAa1}$ and $V_{x/ZAa1}$ values.

An example of measured and processed switching current and voltage waveforms when the IGBT within *BDS 1*-6 undergoes a hard turn-off commutation can be appreciated in Figure B-2.



(a)



(b)

Figure B-2 a) Hard turn-off measured and corrected switching current and voltage signals at V_{ab} = 300 V and I_L = 20 A within BDS 1-6 . b) Hard turn-off instantaneous power dissipation.

where t_{off1} is defined as the time when the $v_{ZAa1}(t)$ voltage rise to 10% of the V_{ab} test voltage and t_{off2} is the time when $i_{ZAa1}(t)$ current falls to 5% of its load value. ΔV is

defined as the value between the maximum $v_{ZAa1}(t)$ voltage and the V_{ab} test voltage. *dv/dt* is defined as the ratio between the $v_{ZAa1}(t)$ voltage rise from 10% to 90% of V_{ab} and its corresponding time as depicted in Figure B-3.

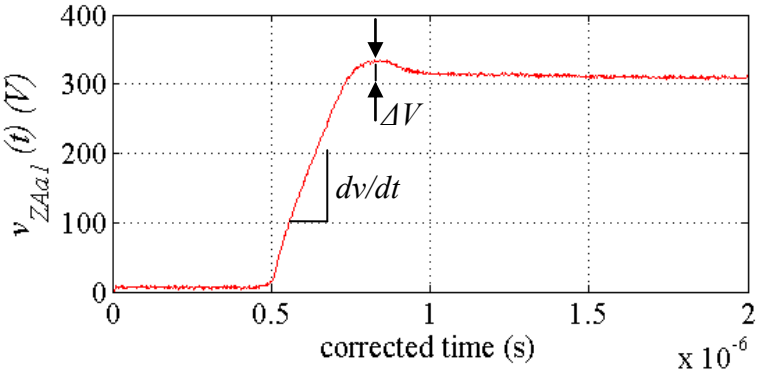
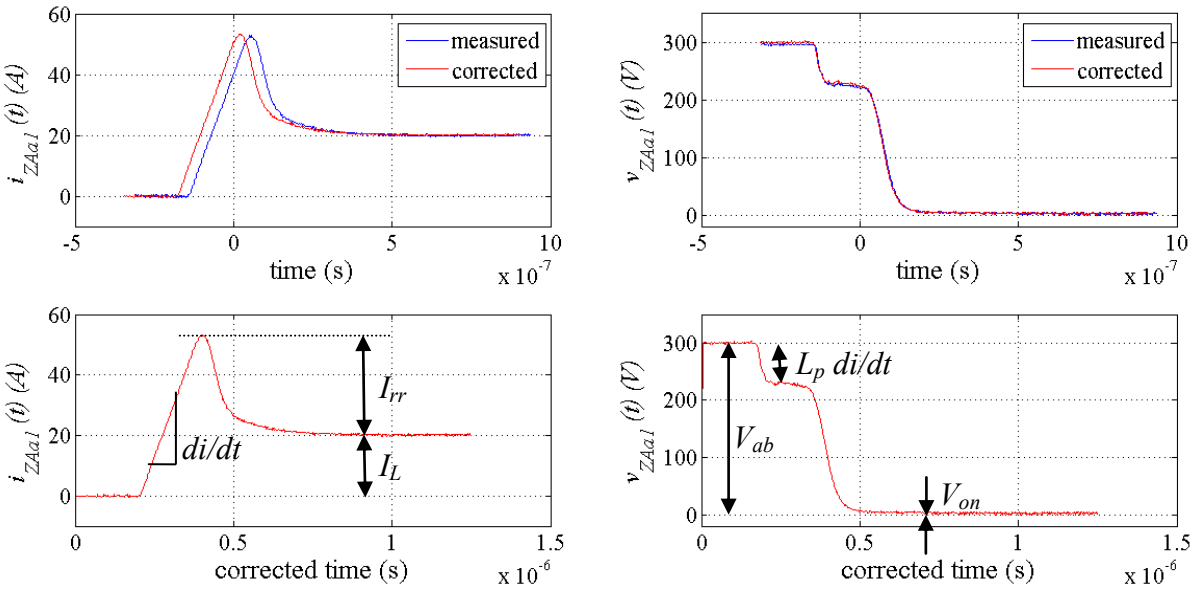
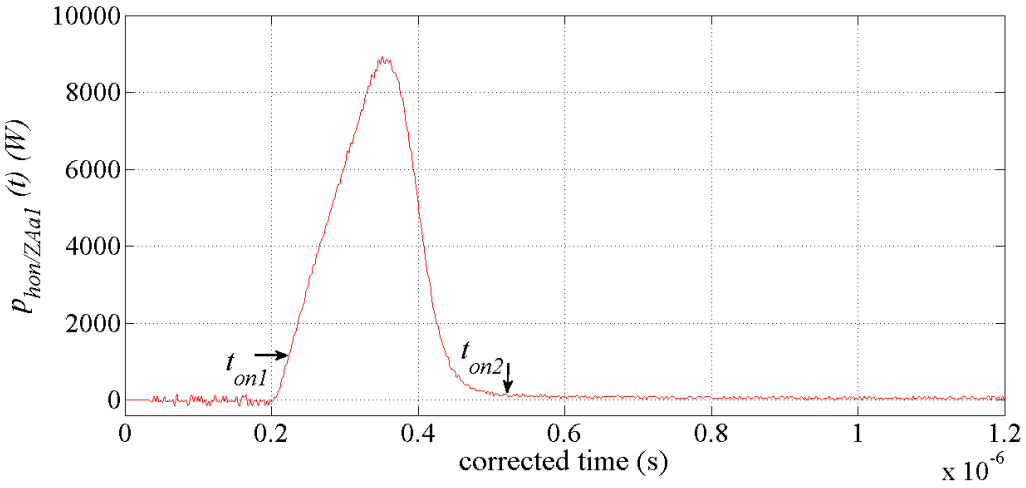


Figure B-3 Turn-off switching voltage zooming

The experimental hard turn-on current and voltage switching waveforms as well as the correction signals are depicted in Figure B-4.



(a)



(b)

Figure B-4 a) Hard turn-on measured and corrected switching current and voltage signals at V_{ab} = 300 V and I_L = 20 A within BDS 1-6. b) Hard turn-on instantaneous power dissipation.

where t_{on1} is defined as the time when $i_{ZAa1}(t)$ current has reached 10% of its load value and t_{on2} is the time when the $v_{ZAa1}(t)$ voltage falls 5% of the V_{ab} test voltage. I_{rr} is the reverse recovery current of the diode already introduced in chapter 3. *di/dt* is defined as the rate between the $i_{ZAa1}(t)$ current rise from 10% to 90% of load current and its corresponding time as depicted in Figure B-4. L_p is the parasitic inductance associated to the test circuit.

Figure B-5 calls the aforementioned read_IGBT_hoff script (particularized for the IGBT hard turn-off case) as many times as required to calculate the IGBT hard turn-off energy losses for a wide range of voltage and current, covering the whole operating conditions of a medium power rate MC: applied voltages (100, 200, 250 and 300 V) and different test currents (5, 10, 15 and 20 A).

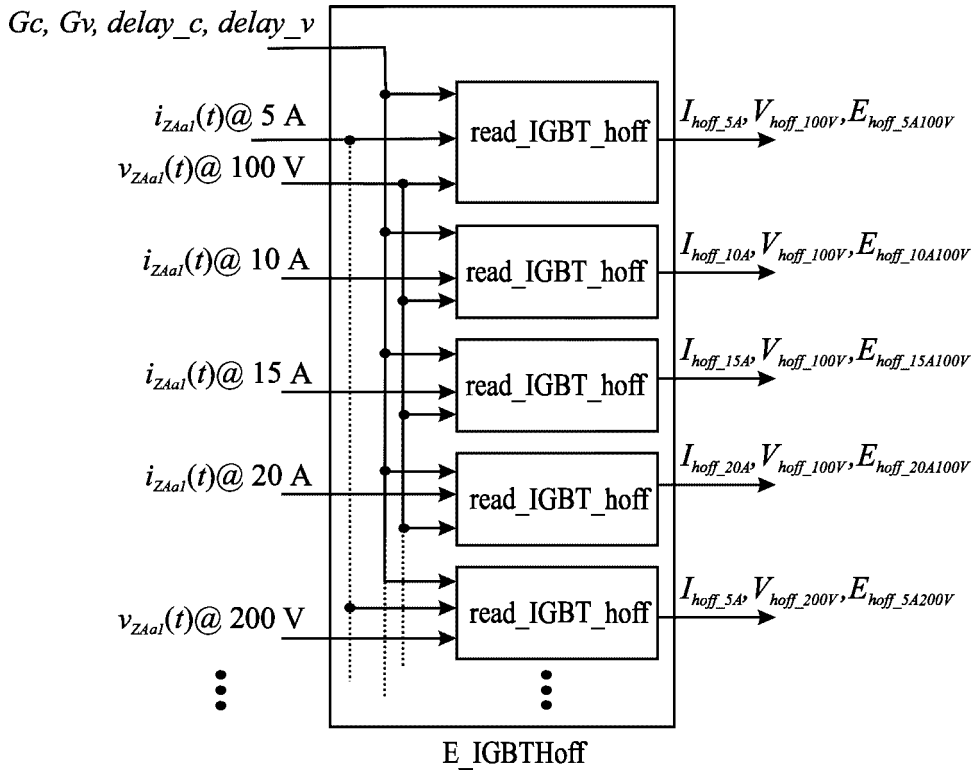


Figure B-5 Block diagram of the IGBT hard turn-off energy losses calculation

An analogous block diagram as shown in Figure B-5 is implemented for the rest of kind of commutations undergone by the IGBT, i.e. E_IGBTHon, E_IGBTSon and E_IGBTSoff. As a result, the different switching energy losses shown in Figure 3-18 are obtained. Moreover, these blocks are run for the different combinations of BDSs under analysis. So, as it can be noted an important number of operations shall be performed in a repetitive mode. Hence, MATLAB suits perfect this kind of task since suitable functions can be programmed and called any time are needed to implement such calculations automatically.

B.2 Diode

Similar to the IGBT case, the read_diode_y block (Figure B-6) deals with processing the diode switching current and voltage waveforms in order to calculate the diode energy losses. The *y* of read_diode_y function stands for the kind of commutation (*hoff*, *hon* and *son*).

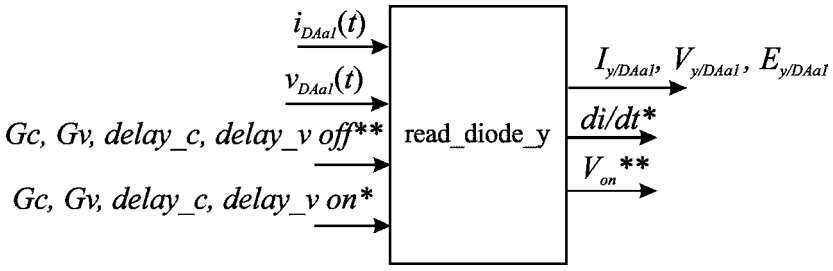
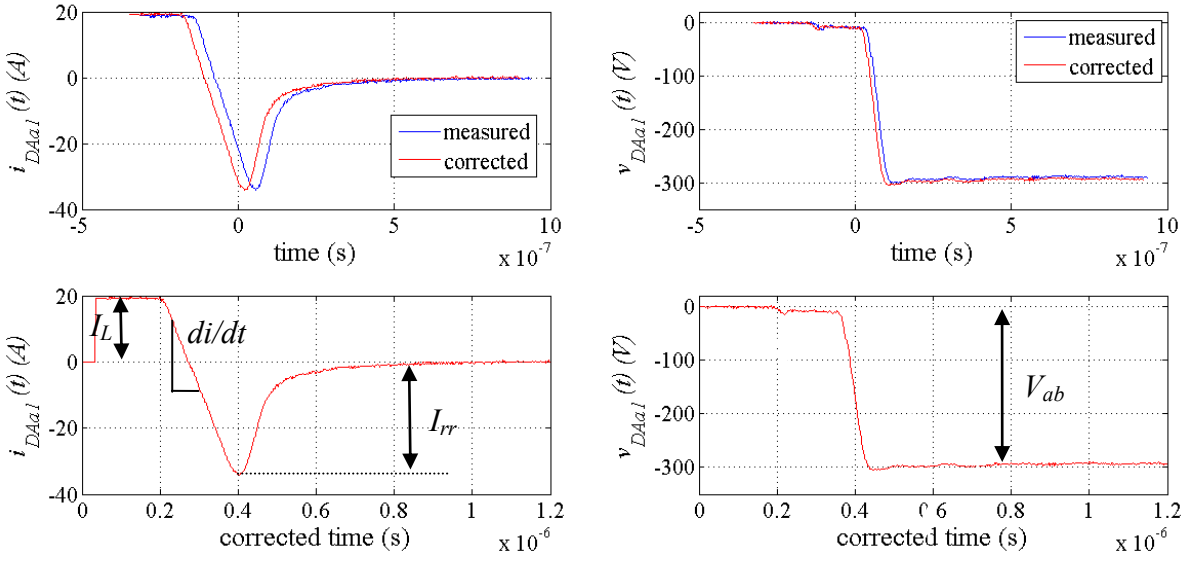
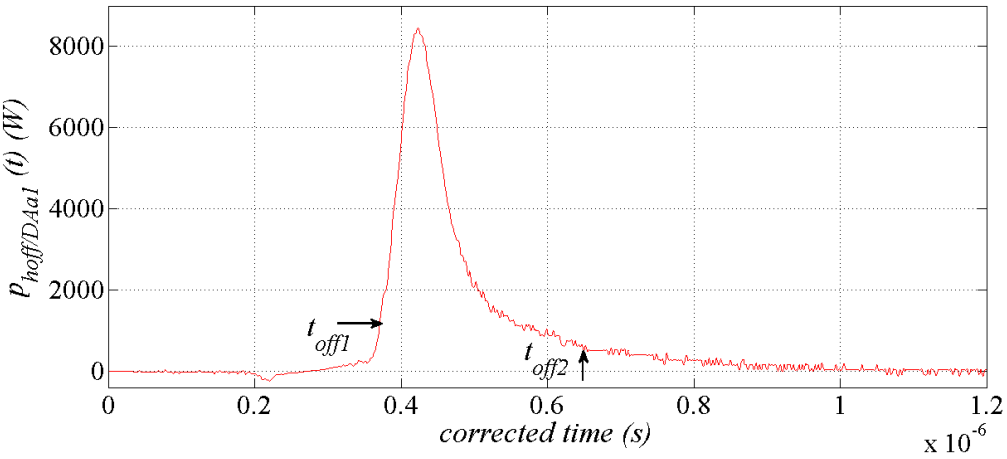


Figure B-6 Block diagram of the read_diode_y script

Attention should be paid with the diode compensation parameters. Although they have the same value as the IGBT ones, the *off* parameters in the IGBT are the *on* parameters in the diode case. This is due to the fact that the probes tests were performed by measuring the current and voltage of the IGBT as a reference.



(a)



(b)

Figure B-7 a) Hard turn-off measured and corrected switching current and voltage signals at V_{ab} = 300 V and I_L = 20 A within BDS 1-6. b) Hard turn-off instantaneous power dissipation.

The turn-off switching interval is defined as in the IGBT case, thus t_{off1} and t_{off2} of Figure B-7 are determined equal to the turn-off IGBT case.

An analogous block to Figure B-5 is also implemented, but to compute diode energy losses and using the read_diode_y script.

C. Matrix Converter Modulation Methods

C1. Venturini Algorithm

The Venturini method allows the generation of a desired set of three-phase output voltages by selecting each of the input phases in sequence for defined periods of time. The duration of these time intervals (i.e. the duty cycle) for the nine bidirectional switches is calculated by ensuring that the average value of the output voltages within each switching cycle tracks the desired reference output waveform and willing to have unity input factor [113].

The duty cycle of each bidirectional switch can be calculated by [114]. It presents two solutions depending on the maximum achievable voltage ratio. Assuming unity displacement factor, for a maximum voltage transfer ratio (q) of 50% the modulation duty cycle can be expressed in a compact way as:

$$D_{Kj} \approx \frac{1}{3}\left[1+\frac{2V_K V_j}{V_{im}^2}\right](q=50\%) \;\; for\; K=A,B,C \; and \; j=a,b,c \tag{C.1}$$

where A, B and C are the input phases, a, b and c are the output phases and V_{im} is the input voltage amplitude. If the optimum-amplitude Venturini method [92] is applied, a maximum voltage transfer ratio of 87% is achieved. For this q, the modulation duty cycle can be written by:

$$\begin{aligned} &D_{Kj} \approx \frac{1}{3}\left[1+\frac{2V_K V_j}{V_{im}^2}+\frac{4q}{3\sqrt{3}}\sin(\omega_i t+\beta_K)\sin(3\omega_i t)\right](q=87\%) \\ &for\; K=A,B,C \; and \; j=a,b,c \\ &\beta_K = 0, 2\pi/3, 4\pi/3 \;\; for\; K=A,B,C \end{aligned} \tag{C.2}$$

where ω_i is the input frequency pulsation.

C2. DS SVM Algorithm

The SVM method is based on the instantaneous space vector representation of output reference voltages and input reference currents as represented in (C.1) and (C.2), respectively.

$$\vec{v}_o = \frac{3}{3}\left(v_a + v_b\, e^{j\,2\pi/3} + v_c\, e^{j\,4\pi/3}\right) = V_o\, e^{j\,\alpha_o} \qquad \text{(C.1)}$$

$$\vec{i}_i = \frac{3}{3}\left(i_A + i_B\, e^{j\,2\pi/3} + i_C\, e^{j\,4\pi/3}\right) = I_i\, e^{j\,\beta_i} \qquad \text{(C.2)}$$

where V_o, I_i and α_o, β_i are the magnitudes and phase angles of the corresponding output voltage and input current vectors, respectively. The output voltage vector is generated from the three-phase reference output voltages (v_a, v_b and v_c) while the input current vector is based on the inputs phase currents (i_A, i_B and i_C).

Controlling the state of each bidirectional switch allows obtaining the desirable output voltages and the input currents. A total of twenty-seven possible switching combinations fulfil the three-phase MC constraints (i.e. only one of the three switches connected to a single output can be in on state at any instant), but only twenty-one can be employed in the SVM algorithm [18], eighteen combinations called stationary vectors and three called zero voltage vectors. All possible combinations are summarised in Table C-1. The ones involving the BDS S_{Aa}, target of our analysis, are highlighted.

Each switching configuration defines both an output voltage reference vector and an input current reference vector. The procedure of the SVM modulation strategy consists basically in two steps: selection of the target output voltage ($\vec{v}_o$) and target input current ($\vec{i}_i$) vectors at any switching instant among the eighteen stationary vectors as shown in Figure C-1 [115] and calculation of the duty cycles of their adjacent target vectors (i.e. $\vec{v}_o', \vec{v}_o'', \vec{i}_i', \vec{i}_i''$) as illustrated in Figure C-1. Besides, $\tilde{\alpha}_o$ and $\tilde{\beta}_i$ are the angles of the output voltage and input current vectors, respectively, resulting from the bisecting line of the corresponding sectors as they are depicted in Figure C-1. The output voltage vector and the input current vector lie in one of the six output voltage and input current sectors, K_v and K_i, respectively as shown in Figure C-1.

Switching configuration	Enable BDSs			V_o	α_o	I_i	β_i
+1	$\boldsymbol{S_{Aa}}$	S_{Bb}	S_{Bc}	2/3 v_{AB}	0	2/sqr(3) i_a	-π/6
-1	S_{Ba}	S_{Ab}	S_{Ac}	-2/3 v_{AB}	0	-2/sqr(3) i_a	-π/6
+2	S_{Ba}	S_{Cb}	S_{Cc}	2/3 v_{BC}	0	2/sqr(3) i_a	π/2
-2	S_{Ca}	S_{Bb}	S_{Bc}	-2/3 v_{BC}	0	-2/sqr(3) i_a	π/2
+3	S_{Ca}	S_{Ab}	S_{Ac}	2/3 v_{CA}	0	-2/sqr(3) i_a	7π/6
-3	$\boldsymbol{S_{Aa}}$	S_{Bc}	S_{Cc}	-2/3 v_{CA}	0	-2/sqr(3) i_a	7π/6
+4	S_{Ba}	S_{Ab}	S_{Bc}	2/3 v_{AB}	2π/3	2/sqr(3) i_b	-π/6
-4	$\boldsymbol{S_{Aa}}$	S_{Bb}	S_{Ac}	-2/3 v_{AB}	2π/3	-2/sqr(3) i_b	-π/6
+5	S_{Ca}	S_{Bb}	S_{Cc}	2/3 v_{BC}	2π/3	2/sqr(3) i_b	π/2
-5	S_{Ba}	S_{Cb}	S_{Bc}	-2/3 v_{BC}	2π/3	-2/sqr(3) i_b	π/2
+6	$\boldsymbol{S_{Aa}}$	S_{Cb}	S_{Cc}	2/3 v_{CA}	2π/3	2/sqr(3) i_b	7π/6
-6	S_{Ca}	S_{Ab}	S_{Cc}	-2/3 v_{CA}	2π/3	-2/sqr(3) i_b	7π/6
+7	S_{Ba}	S_{Bb}	S_{Ac}	2/3 v_{AB}	4π/3	2/sqr(3) i_c	-π/6
-7	$\boldsymbol{S_{Aa}}$	S_{Ab}	S_{Bc}	-2/3 v_{AB}	4π/3	-2/sqr(3) i_c	-π/6
+8	S_{Ca}	S_{Cb}	S_{Bc}	2/3 v_{BC}	4π/3	2/sqr(3) i_c	π/2
-8	S_{Ba}	S_{Bb}	S_{Cc}	-2/3 v_{BC}	4π/3	-2/sqr(3) i_c	π/2
+9	$\boldsymbol{S_{Aa}}$	S_{Ab}	S_{Cc}	2/3 v_{CA}	4π/3	2/sqr(3) i_c	7π/6
-9	S_{Ca}	S_{Cb}	S_{Ac}	-2/3 v_{CA}	4π/3	-2/sqr(3) i_c	7π/6
0_1	$\boldsymbol{S_{Aa}}$	S_{Ab}	S_{Ac}	0	-	0	-
0_2	S_{Ba}	S_{Bb}	S_{Bc}	0	-	0	-
0_3	S_{Ca}	S_{Cb}	S_{Cc}	0	-	0	-

Table C-1 Switching configurations derived from the SVM for three-phase to three-phase MC [18]. The ones involving S_{Aa} BDS are red coloured

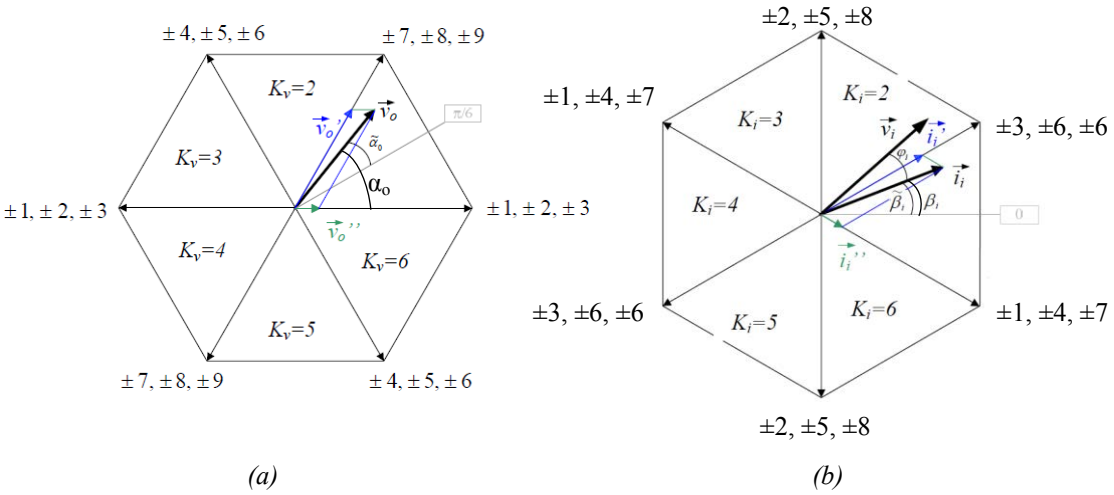


Figure C-2 Active configurations to build the a) Output reference voltage vector. b) input reference current vector

The selection of the switching configurations for each combination within the K_v and K_i sectors can be obtained by considering Table C-2. The combinations where BDS S_{Aa} is involved are highlighted. In order to identify the four general switching configurations which are valid for any combination of input and output sectors, *I*, *II*, *III* and *IV* symbols are also introduced in Table C-2. Four active configurations are required and applied during a certain time within each switching period in order to achieve unity input power factor (i.e. $\varphi_i = 0$, where φ_i is the phase angle between the input current vector and the input voltage vector) and maximum output to input voltage ratio. The corresponding duty-cycles can be determined using:

$$d_I = \frac{2}{\sqrt{3}} q \frac{\cos\left(\tilde{\alpha}_o - \frac{\pi}{3}\right)\cos\left(\tilde{\beta}_i - \frac{\pi}{3}\right)}{\cos(\varphi_i)} \qquad \text{(C.3)}$$

$$d_{II} = \frac{2}{\sqrt{3}} q \frac{\cos\left(\tilde{\alpha}_o - \frac{\pi}{3}\right)\cos\left(\tilde{\beta}_i + \frac{\pi}{3}\right)}{\cos(\varphi_i)} \qquad \text{(C.4)}$$

$$d_{III} = \frac{2}{\sqrt{3}} q \frac{\cos\left(\tilde{\alpha}_o + \frac{\pi}{3}\right)\cos\left(\tilde{\beta}_i - \frac{\pi}{3}\right)}{\cos(\varphi_i)} \qquad \text{(C.5)}$$

$$d_{IV} = \frac{2}{\sqrt{3}} q \frac{\cos\left(\tilde{\alpha}_o + \frac{\pi}{3}\right)\cos\left(\tilde{\beta}_i + \frac{\pi}{3}\right)}{\cos(\varphi_i)} \qquad \text{(C.6)}$$

$$d_0 = 1 - \left(d_I + d_{II} + d_{III} + d_{IV}\right) \qquad \text{(C.7)}$$

where d_I, d_{II}, d_{III} and d_{IV} are the duty-cycles of the four active switch configurations. d_0 is the duty-cycle for the zero switching configuration, which is introduced to complete the switching period. As already mentioned in chapter 5, a DS SVM with the inclusion of three zero vectors in each switching period is considered for the power losses analysis. The duty-cycle for each zero configuration, 0_1, 0_2 and 0_3 can be calculated by:

$$d_{01} = d_{02} = d_{03} = \frac{d_0}{3} \qquad \text{(C.8)}$$

However, the vector control does not establish a specific sequence of the vectors to be activated during the period. Table C-2 only determines the ones that are to be applied. Therefore, there is a degree of freedom when applying and establishing the order of MC vectors. The order shall fulfil that only one commutation of the input phase voltage is given between the applied vectors in order to reduce switching losses [116]. Table C-3 summarises the vector DS SVM sequence regarding S_{Aa} (in this study case) which meets the aforementioned requirement. All these vector sequences have been implemented by means of a MATLAB script in the modulation control block (Figure 5-13) and their corresponding conduction times calculated from (C.3) to (C.8).

$K_v \setminus K_i$	1	2	3	4	5	6	
1	**+9**	-8	+7	-9	+8	-7	*I*
	-7	**+9**	-8	+7	-9	+8	*II*
	-3	+2	-1	+3	+3	**+1**	*III*
	+1	**-3**	+2	-1	-1	-2	*IV*
2	-6	+5	**-4**	**+6**	-5	+4	*I*
	+4	-6	+5	**-4**	**+6**	-5	*II*
	+9	-8	+7	-9	+8	**-7**	*III*
	-7	**+9**	-8	+7	-9	+8	*IV*
3	+3	-2	**+1**	**-3**	+2	-1	*I*
	-1	+3	-2	**+1**	**-3**	+2	*II*
	-6	+5	**-4**	**+6**	-5	+4	*III*
	+4	-6	+5	**-4**	+6	-5	*IV*
4	-9	+8	**-7**	**+9**	-8	+7	*I*
	+7	-9	+8	**-7**	**+9**	-8	*II*
	+3	-3	**+1**	**-3**	+2	-1	*III*
	-1	+3	-2	**+1**	-3	+2	*IV*
5	+6	-5	+4	-6	+5	**-4**	*I*
	-4	**+6**	-5	+4	-6	+5	*II*
	-9	+8	**-7**	**+9**	-8	+7	*III*
	+7	-9	+8	**-7**	**+9**	-8	*IV*
6	**-3**	+2	-1	+3	-2	**+1**	*I*
	+1	**-3**	+2	-1	+3	-2	*II*
	+6	-5	+4	-6	+5	**-4**	*III*
	-4	**+6**	-5	+4	-6	+5	*IV*

Table C-3 Selection of the switching configurations depending on K_v and K_i sectors of the MC references [18]. The ones involving S_{Aa} BDS are red coloured

sector K_v	sector K_i	DS SVM sequence							
1	1	0_3	-3	+9	0_1	-7	+1	0_2	
1	2	0_2	-8	+2	0_3	-3	+9	0_1	
1	3	0_1	-1	+7	0_2	-8	+2	0_3	*Symmetry*
1	4	0_2	+7	-1	0_1	+3	-9	0_3	
1	5	0_1	+3	-9	0_3	+8	-2	0_2	
1	6	0_1	-7	+1	0_2	-2	+8	0_3	
2	1	0_2	+4	-7	0_1	+9	-6	0_3	
2	2	0_1	+9	-6	0_3	+5	-8	0_2	
2	3	0_1	-4	+7	0_2	-8	+5	0_3	*Symmetry*
2	4	0_2	+7	-4	0_1	+6	-9	0_3	
2	5	0_2	-5	+8	0_3	-9	+6	0_1	
2	6	0_3	+8	-5	0_2	+4	-7	0_1	
3	1	0_2	+4	-1	0_1	+3	-6	0_3	
3	2	0_1	+3	-6	0_3	+5	-2	0_2	
3	3	0_3	+5	-2	0_2	+1	-4	0_1	*Symmetry*
3	4	0_3	-3	+6	0_1	-4	+1	0_2	
3	5	0_2	-5	+2	0_3	-3	+6	0_1	
3	6	0_3	+2	-5	0_2	+4	-1	0_1	
4	1	0_2	+7	-1	0_1	+3	-9	0_3	
4	2	0_1	+3	-9	0_3	+8	-2	0_2	
4	3	0_1	-7	+1	0_2	-2	+8	0_3	*Symmetry*
4	4	0_2	+1	-7	0_1	+9	-3	0_3	
4	5	0_2	-8	+2	0_3	-3	+9	0_1	
4	6	0_1	-1	+7	0_2	-8	+2	0_3	
5	1	0_2	+7	-4	0_1	+6	-9	0_3	
5	2	0_2	-5	+8	0_3	-9	+6	0_1	
5	3	0_3	+8	-5	0_2	+4	-7	0_1	*Symmetry*
5	4	0_2	+4	-7	0_1	+9	-6	0_3	
5	5	0_1	+9	-6	0_3	+5	-8	0_2	
5	6	0_1	-4	+7	0_2	-8	+5	0_3	
6	1	0_3	-3	+6	0_1	-4	+1	0_2	
6	2	0_2	-5	+2	0_3	-3	+6	0_1	
6	3	0_3	+2	-5	0_2	+4	-1	0_1	*Symmetry*
6	4	0_2	+4	-1	0_1	+3	-6	0_3	

6	5	0_1	+3	-6	0_3	+5	-2	0_2
6	6	0_3	+5	-2	0_2	+1	-4	0_1

Table C-4 Vector DS SVM sequence depending on K_v and K_i sectors of the MC for S_{Aa} device