Universitat Autònoma de Barcelona

Improving the performance of an all-Si based thermoelectric micro/nanogenerator

Inci Dönmez Noyan

Improving the performance of an all-Si based thermoelectric micro/nanogenerator

İnci Dönmez Noyan

Physics Department
Universitat Autònoma de Barcelona

A thesis submitted for the degree of
Doctor of Philosophy (PhD) in Materials Science
under the supervision of:

Dr. Luis Antonio Fonseca Chácharo
Dr. Carlos Alberto Calaza Cabanas

Tutor: Dr. Aitor Lopeandía Fernández

PhD Thesis - 2018

Abstract

This thesis presents the development of a thermoelectric microgenerator (µTEG) with the aim of powering low power wireless sensor nodes for Internet of Things applications. The proposed µTEG is fabricated by means of silicon micromachining technologies and makes use of silicon (Si) and silicon/germanium (SiGe) nanowire (NW) arrays as thermoelectric material.

Specific technological routes are designed to increase the power density of the µTEG. Particularly, this thesis has been focused on increasing the power density through i) thermal and electrical optimization of the thermoelectric microplatform, ii) integration of a heat exchanger on the proposed µTEGs. The thermal performance of the µTEG is enhanced by reducing the parasitic thermal losses between the hot and cold ends which ended up in %34 decrease of the thermal conductance. The electrical performance, on the other hand is improved tremendously by lowering the device internal resistance 7 to 20 times. Both has been achieved through the redesign of the architecture and processing steps for µTEG. Even though the power densities obtained from the optimized µTEGs are close to meet the expectations for low power sensor nodes (10-100 $\mu W/cm^2$), further improvement is aimed by the integration of a heat exchanger. Two different routes with different heat flow directions have been designed for the integration of a heat exchanger. With the integration of the heat exchanger, a significant amount of improvement has been observed for all tested µTEGs based on different thermoelectric materials (Si NWs, SiGe NWs and Si microbeams). µTEGs with integrated heat exchanger were able to harvest 41.2 (Si NWs), 45.2 (SiGe NWs) and 34.5 $\mu W/cm^2$ (Si microbeams) when they were placed on a waste heat source of 100 °C. This is 50-1000 times more than for similar devices without heat exchanger at the same hot plate temperature.

Results obtained in this thesis are well positioned compared with the state-of-the-art µTEGs. In addition, this thesis, together with the one performed in collaboration at IREC, reports for first time on the performance of SiGe NWs based µTEG.

Resumen

Esta tesis presenta el desarrollo de un microgenerador termoeléctrico (µTEG) con el objetivo de alimentar nodos sensores inalámbricos de bajo consumo para aplicaciones en la Internet de las Cosas. El µTEG propuesto se ha fabricado mediante tecnologías de micromecanizado de silicio y haciendo uso de formaciones de nanohilos de silicio (Si) y de silicio/germanio (SiGe) como material termoeléctrico.

Se han definido rutas tecnológicas de fabricación adecuadas para aumentar la densidad de potencia del µTEG. En particular, esta tesis se ha centrado en aumentar dicha potencia a partir de i) la optimización térmica y eléctrica de la microplataforma termoeléctrica, y ii) integrando un intercambiador de calor en los µTEGs propuestos. Las prestaciones térmicas del µTEG se han mejorado reduciendo las pérdidas parásitas de calor entre las partes calientes y frías de la microplataforma, lo que ha resultado en una reducción del 34% en la conductancia térmica. Las prestaciones eléctricas, por otro lado, han mejorado aún más importantemente al reducir la resistencia interna del dispositivo entre 7 y 20 veces. Ambos logros se han conseguido mediante el rediseño de la arquitectura y de algunos de los procesos de fabricación del µTEG. Aunque las densidades de potencia obtenidas para los µTEG optimizados se acercan a las necesidades de nodos sensores de bajo consumo (10-100 $\mu W/cm^2$), se ha intentado mejorar su comportamiento mediante la integración de un intercambiador de calor. Para dicha integración se han ensayado dos rutas diferentes, en función de la dirección del flujo de calor en el dispositivo. En cualquier caso, se ha podido observar un incremento significativo de prestaciones para todos los µTEGs considerados (Si NWs, SiGe NWs y Si microbeams). Los µTEGs con intercambiador de calor integrado han sido capaces de colectar densidades de potencia de 41.2 (Si NWs), 45.2 (SiGe NWs) and 34.5 $\mu W/cm^2$ (Si microbeams) cuando

se han dispuesto sobre placas calientes a 100 °C de temperatura. Esto supone un incremento de 50-1000 veces con respecto a dispositivos similares sin el intercambiador de calor en esas mismas condiciones.

Los resultados obtenidos en esta tesis están bien posicionados en relación al estado del arte de µTEGs. Además, esta tesis, junto con otra también llevada a cabo en colaboración con el IREC, reportan por primera vez µTEGs basados en nanohilos de SiGe.

Acknowledgements

I consider it my privilege to acknowledge the help, assistance and support of the many individuals without whom this thesis would not have been possible.

First and foremost, I would like to thank my advisor Dr. Luis Fonseca for his invaluable guidance and being a continuous source of support, patience, knowledge and influence for me. He has routinely gone beyond his duty to struggle against my concerns, visa problems, and have instilled great confidence in both myself and my work. I could not have imagined having a better advisor and mentor for my Ph.D. study.

Also, I would like to thank Dr. Carlos Calaza for co-supervising my thesis and Dr. Andrej Stranz for the fruitful discussions. I have enjoyed the opportunity to learn from their knowledge and experience. I am also indebted to Dr. Aitor Lopeandía Fernández for being the tutor of my thesis and for all his help since the beginning of my Ph.D. studies.

I find it very difficult to express my gratitude for Dr. Marc Salleras, the smartest and most adventurous colleague and friend that one person could ask for. Marc has provided me extensive personal and professional guidance and taught me more than I could ever give him credit for here. Moltes gràcies per tot!

I would not have been able to complete this work as I wanted without my dear companion Marc Dolcet, who has contributed a lot during the last year of this thesis work. We have shared many laughs and memories, and I really enjoyed the conversations we had during the breakfast breaks.

Perla, my dearest friend, thank you for sharing this journey with me. You were always there with a listening ear, supporting me in every aspect of my life. Thanks for the time that we spent both in

and out. Roberto, I am profoundly grateful for your friendship and kindness. Sole, thank you for cheering us up even in hard times (and also for 'mate'). I would also like to thank my friends: Kutlu, Ceren, Civan, Cami, Mar, Irene, Onur, Gulçin, Başak, Xavi, Marina, Laura and Federico for making my life in Barcelona much more pleasant.

Thanks to IMB-CNM cleanroom staff for their painstaking efforts in fabricating the microgenerator and effectiveness in alleviating the challenges that I faced during the experimental research. I am especially indebted to Marta Duch and Marta Gerbolés for their valuable assistance and help. I feel so lucky to have a chance to work with them in Microsystems Lab. I would also like to thank Ana Sánchez, Roser Mas, Miguel Zabala, Javier Sanchez, Xavier Borrisé, Sara Duran and Alberto Moreno for their collaborations. I would also like to thank mechanical workshop for their efforts in fabricating various pieces when I needed. Additionally, I would like to acknowledge IMB-CNM administrative staff for their guidance throughout these years.

I have had an opportunity to collaborate with amazing researchers from IREC, Barcelona. I am specially indebted to Dr. Gerard Gadea and Dr. Mercè Pacios for their time, understanding and fun/useful conversations we had. I would also like to acknowledge Dr. Albert Tarancón and Dr. Álex Morata for their enthusiasm and valuable comments.

I would also like to thank Humberto Mata Rodríguez and Loreta Gutiérrez from D+T Microelectrónica, A.I.E for their overwhelming efforts to solve my paperwork problems, I greatly appreciate it.

I am eternally grateful to my parents and my parents-in-law for their unremitting encouragement, support and guidance. I also wish to thank my sisters: Merve, Melike and Aslı for being awesome and to my nieces: Ada and İdil for bringing joy to my life. Finally, I wish to thank my loving, supportive, encouraging, and patient husband Alican who provides me unending inspiration. This dissertation stands as a testament to your unconditional love and support.

Contents

Abstract i

Resumen iii

Acknowledgement v

Nomenclature xiii

Scope of the Thesis xv

1 Introduction 1
- 1.1 Thermoelectric effect . . . 3
- 1.2 Thermoelectric materials . . . 5
  - 1.2.1 Thermoelectric materials efficiency . . . 5
  - 1.2.2 Literature review on thermoelectric materials 8
    - 1.2.2.1 Si and SiGe nanostructures as thermoelectric materials . . . 10
- 1.3 Thermoelectric devices . . . 14
  - 1.3.1 Thermoelectric devices efficiency . . . 16
  - 1.3.2 Literature review on thermoelectric devices . . 18
    - 1.2.3.1 Miniaturized thermoelectric devices . 19

2 Experimental methods 23
- 2.1 Overview . . . 23
- 2.2 Strategy of the µTEG Fabrication . . . 23
  - 2.2.1 Silicon technology processing for µTEG . . . 25
  - 2.2.2 Si and SiGe NW growth . . . 28
    - 2.2.2.1 Overview . . . 28
    - 2.2.2.2 Galvanic displacement . . . 29

2.2.2.3 CVD-VLS growth 31
2.3 Thermoelectric characterization 33
2.3.1 Contact resistance 34
2.3.2 Temperature coefficient of resistance 36
2.3.3 Thermal conductance of the platforms 38
2.3.4 Seebeck coefficient 39
2.3.5 Thermoelectric power 40

3 An optimized all-Si based thermoelectric microgenerator 43
3.1 Overview 43
3.2 Thermoelectric microgenerator design 43
3.2.1 Platform thermal response optimization . . . 45
3.2.2 Platform electrical response optimization . . . 49
3.2.3 Other design considerations 55
3.3 Thermoelectric microgenerator fabrication: microplatform definition and NWs integration 58
3.4 Thermoelectric microgenerator characterization . . . 64
3.4.1 Thermal conductance 64
3.4.2 Seebeck coefficient 71
3.4.3 Thermoelectric power 76
3.5 Discussion & summary 83

4 Integration of a heat exchanger on a µTEG 89
4.1 Overview 89
4.2 Preliminary studies 90
4.2.1 Forced convection 90
4.2.2 Cold-finger approach 95
4.3 Routes for the integration of a heat exchanger 97
4.3.1 Top approach 99
4.3.2 Bottom approach 104
4.4 Simulations with the assembled heat exchanger . . . 106
4.5 Thermoelectric power characterization with the assembled heat exchanger 113
4.6 Discussion & summary 119

Conclusions 125

Ongoing & Future Work 129

Scientific Contributions **133**

Appendix **138**

A Test structures for single NW characterization **139**

B Studies to increase the fabrication yield **143**
B.1 Cleaving of the wafer 143
B.2 Stress analysis of the device layers 147

Bibliography **151**

Nomenclature

Abbreviations

µTEG	Thermoelectric microgenerator
APCVD	Atmospheric-Pressure Chemical Vapor Deposition
CQFP	Ceramic Quad Flat Pack
CVD	Chemical Vapor Deposition
DRIE	Deep Reactive Ion Etching
FEM	Finite Element Method
FIB	Focused Ion Beam
HCl	Hydrochloric acid
HF	Hydroflouric acid
IMB-CNM	Institute of Microelectronics of Barcelona, CSIC
IoT	Internet of Things
IREC	Catalonia Institute for Energy Research
KOH	Potassium hydroxide
LPCVD	Low-Pressure Chemical Vapor Deposition
MACE	Metal-assisted Chemical Etching
MEMS	Micro-Electro-Mechanical Systems
NW	Nanowire

PCB	Printed Circuit Board
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PMMA	Poly(methyl methacrylate)
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
SEM	Scanning Electron MIcroscope
Si	Silicon
SiGe	Silicon-Germanium
SNAP	Superlattice Nanowire Pattern Transfer
SOI	Silicon-on-Insulator
TCR	Temperature Coefficient of Resistance
TEG	Thermoelectric Generator
TLM	Transmission Line Model
VLS	Vapor-Liquid-Solid

Symbols

β	Thomson coefficient	V/K
η	Efficiency	%
Π	Peltier coefficient	V
ρ_c	Specific contact resistivity	Ωcm^2
σ	Electrical conductivity	S/cm
d	Nanowire diameter	nm
E_s	Young´s modulus (of Si)	130 GPa
I	Electric Current	A

K	Thermal conductance	W/K
k	Thermal conductivity	W/mK
L_T	Transfer length	μm
P	Power	W
PD	Power density	$\mu W/cm^2$
R	Electrical resistance	Ω
R_c	Contact resistance	Ω
R_s	Sheet resistance	Ω/sq
S	Seebeck coefficient	V/K
$T, \Delta T$	Temperature, Temperature difference	K
$V, \Delta V$	Voltage, Voltage difference	V
v_s	Poisson´s ratio (of Si)	0.28
W	Width	m
ZT	Figure of merit (device)	
zT	Figure of merit (material)	
TCR	Temperature Coefficient of Resistance	ppm/K

Scope of the thesis

This thesis presents a thermoelectric microgenerator (µTEG) fabricated using silicon micromachining technologies that makes use of silicon and silicon/germanium nanowires as thermoelectric material. The aim of the proposed all-Si µTEG is to harvest electricity when placed on a waste heat source by means of Seebeck effect.

Particularly, our efforts have been focused on increasing the power output through i) thermal and electrical optimization of the thermoelectric microplatform, ii) integration of a heat exchanger on the proposed µTEGs. Attained improvements from both the microplatform optimization and heat exchanger integration are presented.

The organization of this thesis is as follows:

Chapter 1 introduces the basics of the thermoelectricity, including thermoelectric effect and efficiency. Literature review on the state-of-the art of thermoelectric materials and devices is presented, paying attention to the Si nanowires based thermoelectric generation.

In **Chapter 2**, experimental methods used for the growth of nanowires and the device characterization techniques are described.

The Si nanowires based µTEG is presented in **Chapter 3**, including optimization of the microplatform design and microfabrication steps as well as the µTEG performance characterization. First results on the µTEG with SiGe nanowires are also discussed.

Chapter 4 focuses on the first proof-of-concept integration of heat exchanger on microplatforms. Different routes are described, their contribution to resulting performance presented both with simulations and experiments.

After discussing the results and further work planned in relation to the topic in **Conclusion** and **Future Work**, two appendixes are

added to the thesis. **Appendix A** describes the labor invested in the development of test structures for single nanowire characterization. In **Appendix B**, the efforts to increase the fabricating yield of our µTEG are presented. These studies include the use of mechanical cleaving instead of wafer dicing to eliminate the breaking of a fragile structures on the device as well as the analysis of the stress of the specific layers deposited during the fabrication process.

Chapter 1

Introduction

Internet of Things (IoT) has started to spread rapidly in the last few years and is expected to gain further recognition as *the Next Industrial Revolution*. IoT basically refers to a system where items in the physical world embedded with sensors can communicate with the others via internet connection. According to BI Intelligence, there will be more than 55 billion IoT devices on Earth by 2025 [1]. Several environments will benefit from IoT, including, connected home, healthcare, smart environments, food services, transportation etc. Figure 1.1 summarizes the main application areas of IoT together with some examples.

For successful realization of IoT devices on several applications, they should be smart, autonomous, miniaturized, and they should have low-energy wireless communication capabilities to be able to collect data from all kinds of locations. Currently, most of the IoT devices are being powered by batteries which limit their operational lifetime. Replacing the battery will disturb the operation, increase the cost, and most importantly, it will end up with significant environmental implications. The use of environmental energy harvesting can self-power IoT sensors, it can extend the battery lifetime or even eliminate the need for the batteries. Considering the low-power requirements for wireless sensor nodes of IoT (10-100 $\mu W/cm^2$), the efforts are focused on microsystem based energy harvesting [4]. Micro-Electro-Mechanical Systems (MEMS) based energy harvesting has been attracting profound interest in the research and scientific community since its technology allows mass production, miniaturization

Application	Examples
 Wearables	Monitor and maintain human health and wellness; disease management, increased fitness, higher productivity
 Homes	Energy management, safety and security, chore automation, usage-based design of appliances
 Vehicles	Condition based maintenance, safer/smarter transportation, usage-based design, pre-sales analytics
 Cities	Public spaces and infrastructure in urban settings; adaptive traffic control, smart meters, environmental monitoring, resource management
 Factories	Places with repetitive work routines, including hospitals and farms; operating efficiencies, optimizing equipment use and inventory
 Healthcare	Enhanced patient experience, reduced errors, in-home medical devices, improved disease management,
 Retails	Inventory optimization, smart customer relationship, faster/efficient logistics and supply chains
 Offices	Energy management and security in office buildings; improved productivity, mobile employees
 Education	Smart devices to share the knowledge, self-directed learning, interactive education
 Agriculture	Sensor based field and resource mapping, remote monitoring, predictive analytics

Figure 1.1: Main application areas of Internet of Things together with some application examples. Adapted from [2], [3].

and easy integration with electronics [5]. In addition, the repeatability and high reliability of MEMS batch fabrication processes reduce the unit cost which can clearly contribute positively to their use for IoT devices.

Thermal energy is one of the environmentally available energy sources which can be harvested through thermoelectric generators. Thermoelectric generators can convert heat into electricity with long operational lifetimes and reliability, and they don´t include any moving parts. Considering the excessive amount of waste heat that is produced in our daily life, harvesting at least some of this waste heat means a tremendous amount of power that can be used for several applications.

This thesis reports an all-Si based thermoelectric microgenerator (µTEG) fabricated using MEMS technology with the aim of powering low power wireless sensor nodes for IoT applications. Specific technological routes are designed to increase the power density of the µTEG which will be detailed in the following chapters. This chapter intends to explain the basic thermoelectric effects together with a short literature review on thermoelectric materials and devices.

1.1 Thermoelectric effect

Thermoelectric effect refers to a phenomenon in which temperature difference generates electricity or vice versa. There exist three reversible thermoelectric effects: Seebeck effect, Peltier effect and Thomson effect. They are dubbed reversible as opposed to Joule effect, which is irreversible, although not always considered a thermoelectric effect in itself, but a loss mechanism.

In 1821, Johann Thomas Seebeck discovered that a circuit made out of two dissimilar conductors (standard thermocouple configuration, depicted in Figure 1.2) would deflect a compass needle if their junctions are maintained at different temperatures. Initially, he interpreted his discovery as magnetism caused by temperature difference. Later it was realized what he found out was the new source of electric current. Applying a temperature differences to a material leads to diffusion of charge carriers from the hot side to the cold side. This diffusion creates an electric field which in turn builds up a thermally

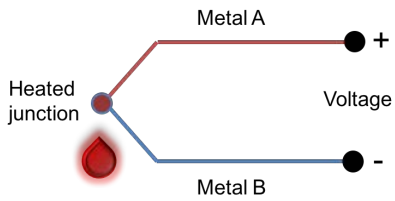

Figure 1.2: The schematic of a basic thermocouple.

induced voltage across the material, which is

$$V = S\Delta T \tag{1.1}$$

In the thermocouple configuration, the voltage developed across both materials, V, is proportional to the temperature difference, ΔT, and the ratio between them is the differential Seebeck Coefficient of materials A and B ($S_A - S_B$). The sign of the Seebeck coefficient depends on the sign of the majority charge carriers present in the material. Therefore, it is positive for p-type and negative for n-type semiconductors or metals.

The second thermoelectric effect was discovered in 1834 by Jean Peltier using the same experimental setup that was used for the demonstration of Seebeck effect. Instead of establishing a temperature gradient between the junctions, the current was applied through the circuit ending up heating or cooling at the junction. It was found that the rate of heat ejection or absorption (q) was proportional to the applied electric current (I), and the constant of proportionality is defined by a coefficient named Peltier Coefficient, Π.

$$\Pi = \frac{q}{I} \tag{1.2}$$

The last of the thermoelectric effects, Thomson Effect, relates the rate of generation of reversible heat q when a current passes through a single conductor along which there is a temperature difference of ΔT. Thomson Coefficient is defined by β in the following formula:

$$q = \beta I \Delta T \tag{1.3}$$

The units of β is the same with the Seebeck coefficient (V/K), and it is usually neglected for thermoelectric devices.

Seebeck, Peltier and Thomson effects are interrelated fundamentally by the The Thomson relations based on the use of classical thermodynamics of equilibrium reversible processes in the form:

$$\Pi = ST \tag{1.4}$$

$$\beta = T\frac{dS}{dT} \tag{1.5}$$

1.2 Thermoelectric materials

Standard thermocouples are composed of two alternating n-type and p-type semiconductor elements. These thermoelements are classified with respect to their efficiencies defined by their material properties. This section aims to explain briefly the relationships between the factors affecting their performances/efficiencies. Next, literature reports on good thermoelectric materials will be shortly reviewed with an emphasis on silicon (Si) and silicon-germanium (SiGe) as thermoelectric materials.

1.2.1 Thermoelectric materials efficiency

The efficiency of a thermoelectric material is defined by its dimensionless figure of merit, zT, which is a function of several parameters:

$$zT = \frac{S^2\sigma}{k}T \tag{1.6}$$

where σ is electrical conductivity, S is Seebeck coefficient and k is thermal conductivity of the material. The term $S^2\sigma$ is referred as thermoelectric power factor. Thermoelectric figure of merit is defined with respect to mean operating temperature (T). Obviously, a material should have a large Seebeck coefficient and electrical conductivity as well as low thermal conductivity to have a high figure of merit.

Seebeck coefficient is a sum of electrical (S_e) and phonon-drag (S_{ph}) contributions. The first contribution is a result of different charge carrier contribution rates at different temperature, while the latter arises from lattice vibrations that are carrying the heat. When

a temperature difference is applied across the material, phonons interact with charge carriers and contribute positively to their movements through the cold end.

Similar to Seebeck coefficient, thermal conductivity is also composed of two components. Lattice thermal conductivity, k_l, is the dominant contribution and is related to ability of phonons to conduct heat. Electrical thermal conductivity, k_e, on the other hand, arises from the ability of charge carriers to conduct heat.

Another parameter affecting the thermoelectric efficiency is electrical conductivity, σ, which is the measure of a material´s ability to allow the transport of an electric charge. Metals have the highest electrical conductivity while semiconductors are occupying an intermediate position in terms of electrical conductivity with carrier concentration values between 10^{16}-10^{22}cm^{-3}. Insulators, on the other hand, have very low electrical conductivity which is assumed as zero under normal conditions.

It is also important to note the effect of temperature on the thermoelectric properties. With increased temperature, the phonon-drag contribution of Seebeck coefficient decreases. Increased temperature also decreases the lattice thermal conductivity due to increased phonon-phonon scattering. Phonon-electron scattering also increases with temperature which ends up in low electrical conductivity for highly doped semiconductor. Therefore, an optimum temperature for each thermoelectric material should be defined for the desired thermoelectric applications.

To increase the thermoelectric efficiency, it is necessary to optimize a variety of conflicting properties. As can be seen from Eqn. 1.6, maximum zT can be achieved by manipulating the material properties to have high Seebeck coefficient, high electrical conductivity and low thermal conducitivity.

Seebeck coefficient and electrical conductivity relate to the carrier concentration by the following equations:

$$S = \frac{8\pi^2(k_B)^2}{3eh^2} m^* T \Big(\frac{\Pi}{3n}\Big)^{\frac{2}{3}} \tag{1.7}$$

$$1/\rho = \sigma = ne\mu \tag{1.8}$$

where n is the carrier concentration and m^* is the effective mass of

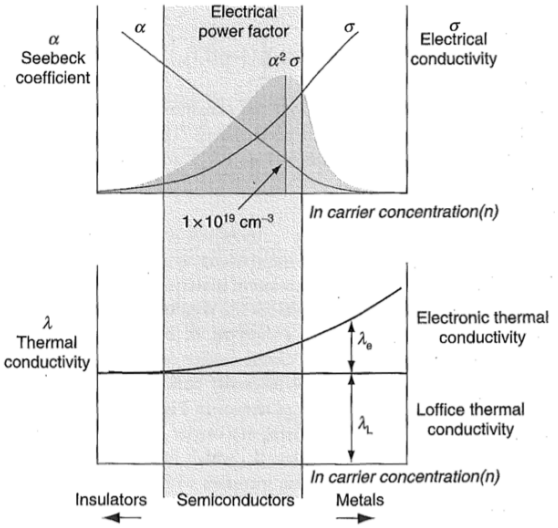

Figure 1.3: Schematic dependence of Seebeck coefficient, thermal conductivity, electrical conductivity and power factor on free carrier concentration. Taken from [7].

the carrier. Figure 1.3 can be correlated with Eqn. 1.7 to claim that Seebeck coefficient decreases as the carrier concentration increases. On the other hand, low carrier concentration results in low electrical conductivity (Eqn. 1.8) which is not desired in order to have a high figure of merit. Therefore, it is very critical to compromise between large Seebeck coefficient and high electrical conductivity to achieve maximum zT. This maximum usually occurs at carrier concentrations between 10^{19} and 10^{21} carriers per cm^3 [6].

Considering abovementioned parameters, semiconductors are the best candidates as thermoelectric materials. zT is linked to thermoelectric efficiency because it modulates the maximum attainable fraction of the Carnot efficiency for a given temperature difference. More information is given in Section 1.3.1. To refer a material as a good thermoelectric material, its dimensionless figure-of-merit (zT) should be higher than 0.5. [7]

1.2.2 Literature review on thermoelectric materials

From the previous section it is clear that the selection of materials for thermoelectric power generation involves the search for materials of high figure of merit (zT). In addition to that, thermoelectric materials should be capable of operating over a wide temperature range as much as possible, they should have reliable mechanical, metallurgical and thermal characteristics that allow their use in practical applications. The following recollection of thermoelectric materials options is neither exhaustive nor enters into an in-depth description of them. It only aims at showing the material families that are currently used and researched as well as the avenues for improving thermoelectric performance or applicability. The interested reader is advised to explore the cited references and the regularly published reviews on thermoelectric materials [8]–[14].

Several thermoelectric materials have been investigated for decades to improve the efficiency of the system using high zT materials. In the 1950s, generator efficiencies had reached 5% and cooling from ambient to below 0 °C was demonstrated using Bi_2Te_3 as thermoelectric material. Since then, Bi_2Te_3 has been the most extensively studied and applied material for thermoelectric applications. Another high zT thermoelectric material is PbTe which is used for space applications as well as SiGe for radioisotope thermoelectric generators [15]. Several materials have been reported with high zT values due to their intrinsically low thermal conductivities such as Cu_2S, $Yb_{14}MnSb_{11}$, Ag_9TlTe_5, $AgSbTe_2$, BiCuSeO and SnSe. Figure 1.4 displays the state of the art thermoelectric materials with high figures of merit. Thermoelectric materials can be divided into three groups according to the optimal working temperatures; low, medium and high temperatures. Bi_2Te_3-based materials are stable up to 550 K so that they are mostly functional for low temperature applications. In the middle temperature range (550 to 900 K), different materials exist such as PbTe, $Bi_{0.875}Ba$, clathrates, skutterudites and TAGS. For the high temperature applications above 900 K, SiGe, Cu_2Se, Zintl compounds and Half-Heusler alloys are considered to be the most efficient materials. Oxides and silicides are aimed at enabling heat conversion at elevated temperatures. Further to their stability, they

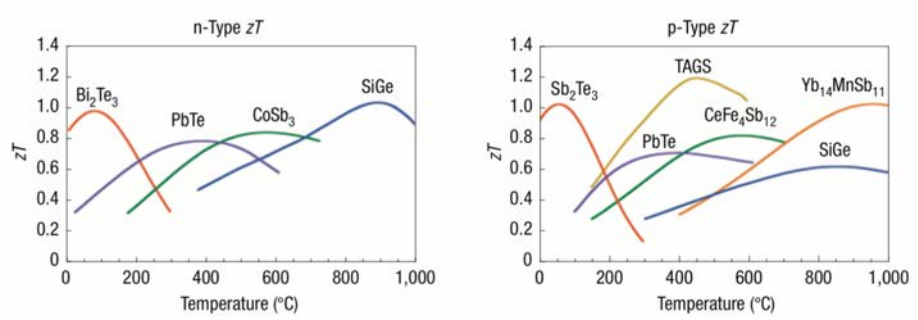

Figure 1.4: Figure of merit (zT) of state-of-the-art commercial materials for thermoelectric power generation. Taken from [6].

are attractive also on view of their low cost and nontoxicity [14], [16], [17]. Silicides are also of wider interest because of their prospective compatibility with integrated technology, which would make them suitable candidates for microharvesting.

In the mid-90s, zT values higher than 1 were achieved thanks to breakthroughs in two different research approaches: exploring new materials with complex crystalline structures and resourcing to some dimensional engineering of the materials. New materials such as skutterudites and clathrates include loosely bonded atoms which cause phonon scattering with almost negligible impact on the electron transport [18]. For the latter approach, Dresselhaus and coworkers found that dimensional restriction can lead to a much enhanced efficiency over bulk thermoelectrics [19], [20]. They proposed that the use of nanostructures allows tuning the zT through new methods such as quantum confinement, modulation doping, and the enhanced influence of interfaces and surfaces. Once more, a successful strategy to increase zT has been introducing additional scattering mechanisms for phonons. Hierarchical structures have been designed including all-length scale structures to scatter broad spectrum of heat carrying phonons, as depicted in Figure 1.5. On the other hand, the predicted positive effect of the extreme dimensions reduction on Seebeck coefficient by quantum confinement of carriers has not been proved unambiguously in any material system experimentally.

Recently, organic and hybrid materials have been reported to exhibit figure of merits that are approaching to those of inorganic materials. Their optimization into devices have been studied especially

Figure 1.5: Some of the different phonon scattering mechanisms. Adapted from [25].

for low temperature wearable microgenerators [21]. Organometallic polymers have demonstrated the highest organic thermoelectric generator performance so far, with an attained power output of about 1 $\mu W/cm^2$ under a 30 K temperature difference [22]. However, these polymers require traditional cross-plane geometries and they are poorly processable. Organic and hybrid materials that are easily processable in large amounts such as carbon nanotubes (CNTs) loaded organic matrices [23] and PEDOT-based polymers [24] are being investigated intensely and are expected to perform better in the near future.

1.2.2.1 Si and SiGe nanostructures as thermoelectric materials

Lately, interest in thermoelectrics has gained momentum thanks to the advances in tailoring material properties by nanostructuring. As a matter of course, different materials have been studied, especially the ones which are not promising in their bulk form. In particular, silicon (Si) has been studied since it is cheap, abundant, non-toxic and extremely technologically enabling material. In its bulk form, Si has a high power factor ($S^2\sigma$) but also very high thermal conductivity (148 W/mK), which makes it a bad thermoelectric material with very low zT values (below 0.01). Therefore, efforts have been focused on lowering its thermal conductivity by introducing scattering mechanisms for phonons. This could be achieved by introducing second

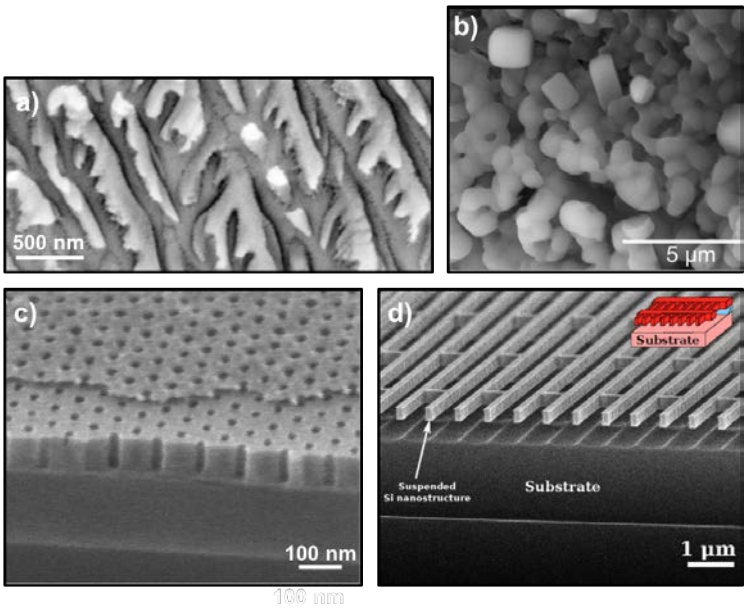

Figure 1.6: Different Si nanostructures fabricated to enhance their thermoelectric properties: nanoporous Si (a) [30], Si quantum dots (b) [35], holey Si (c) [33], suspended Si nanostructures (d) [34].

phase precipitates into Si, which has been reviewed lately by Narducci et al. [26] or nanostructuring. Several Si nanostructure geometries have been investigated in order to increase the zT by lowering its thermal conductivity. Thin layers of Si have been demonstrated as an efficient thermoelectric material [27], [28]. Very low thermal conductivities have been achieved using porous Si structures (0.1 W/mK at RT) [29], however, these structures exhibit very poor electrical conductivities which resulted in zT values similar to those of bulk Si [29], [30]. To control the thermal conductivity of a material independently from its electrical conductivity, Yu et al. [31] reported Si nanomesh structures that are periodically structured. Similar structures (called as *holey Si* by the authors) were demonstrated in Refs [32], [33] in which arrays of periodic holes were fabricated by block copolymer lithography. Pennelli et al. [34] proposed a thermoelectric generator using top-down fabricated Si nanostructures as thermoelectric materials. Some of the Si nanostructures fabricated for thermoelectric characterization/application purposes can be seen from Figure 1.6.

Papers by Boukai et al. [36] and Hochbaum et al. [37] have been the pioneers of the field by claiming that rough Si nanowires (NWs) can have zT of 0.6 at room temperature and 1 at lower temperatures. They independently argued that the reason of this high figure of merit is phonon scattering from the rough Si NW surfaces which caused almost 100 times decrease in the thermal conductivity of the NWs. Figure 1.7 demonstrates the length scale where the decrease of the thermal conductivity is taking place, in the vicinity of a 100 nm or below (already evident for thicker SiGe NW). Since then, even though the same zT values could not be achieved, a variety of studies have been reported addressing the enhancement of thermoelectric performance using Si NWs. Studies reporting the top-down fabrication of Si NW arrays are generally aiming at a vertical architecture for NWs arrangement using different techniques such as lithography which is followed by reactive ion etching [38]–[44], electroless etching [37] and metal-assisted chemical etching (MACE) [45]–[48]. For the application of vertical Si NW arrays into microgenerators, the mostly encountered adversity is to achieve a good thermal and electrical contact for the top side of the NWs. To overcome this problem and to provide mechanical stability to NW arrays, filler materials such as silicon dioxide (SiO_2) and polyimide have been used to fill the gap between the NWs [40], [49]–[51]. Top-down techniques have also been demonstrated to fabricate NWs with planar geometries using e-beam lithography [52]–[57] and controlled etching and filling of recessed regions (CEFRR) [58]–[61] techniques. Bottom-up approaches are based on the growth of NWs by means of chemical vapor deposition (CVD). The mostly used CVD growth method for Si and SiGe NWS is vapor-liquid-solid (VLS), which enables the massive integration and low-cost production of NWs with respect to top down approaches. However, bottom-up approaches usually require complex procedures for the positioning of NWs inside the thermoelectric device. This problem is overcome by the monolithic integration of VLS-grown Si NWs into thermoelectric microgenerators which was first proposed by Davila et al. [62]. This thesis intends to further improve the power output obtained by such approach by optimizing the microgenerator design, and to show the first attempt to integrate SiGe NWs into the optimized microgenerator.

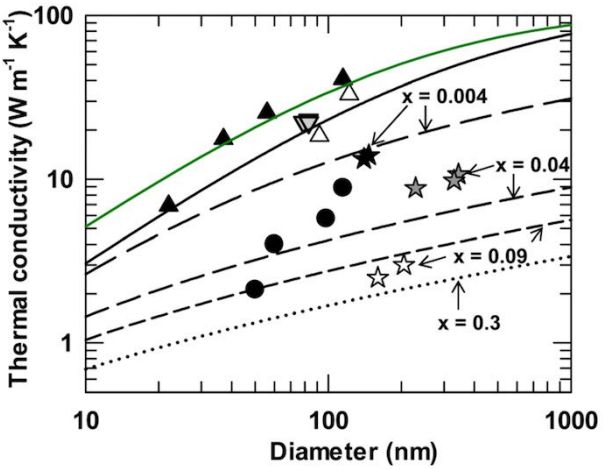

Figure 1.7: Thermal conductivity as a function of diameter for Si and $Si_{1-x}Ge_x$ nanowires. Except for those labeled in the figure, the data are for Si nanowires. The symbols are for VLS Si nanowires (black triangles), RIE patterned Si nanowires (gray down triangles), electroless etched Si nanowires (black circles), Si nanowires (unfilled triangles) and $Si_{1-x}Ge_x$ nanowires. Green and black lines are the calculations for Si and SiGe NWs, respectively. Taken from [63].

Regarding SiGe, it is already reported as a highly efficient thermoelectric material in its bulk form and has been used first in a number of space applications such as multihundred watt generators used on the LES 8/9 and the Voyager spacecrafts [64]. The high efficiency of SiGe arises from its reduced thermal conductivity due to the alloy-induced scattering of phonons. The use of SiGe low-dimensional structures aims to further decrease the thermal conductivity by enhanced phonon boundary scattering effect and integrate them into microdevices. Similar structures such as nanowires, nanomeshes, nanotubes have been demonstrated to have lower thermal conductivities [65], [66]. Si/SiGe superlattice structures have also been theoretically proposed and fabricated [67].

1.3 Thermoelectric devices

A typical thermoelectric device consists of a given number of materials junctions, each one formed from two different semiconductor materials, one containing hole-charge carriers (p-type) and the other electron-charge carriers (n-type). These semiconductor materials are referred as the two legs of a thermocouple, and these thermocouples are connected electrically in series and thermally in parallel.

Thermoelectric devices can be categorized as thermoelectric coolers and thermoelectric generators. Basic thermocouples for both applications are illustrated in Figure 1.8. When a DC voltage is applied to the module terminals (current flowing from positive terminal to the negative terminal), electrons in the n-type element are attracted by positive pole of the supply voltage while holes in the p-type element are attracted by negative potential of the supply voltage and move in an opposite direction to the electron flow. The movement of charge carriers convey the heat away from the junction which results in cooling of the junction. This is called *thermoelectric cooling* (or heating, depends on the current direction), and it is mainly influenced by Peltier Effect. Currently, thermoelectric cooling devices are widely used in a variety of applications as refrigerators and air conditioners. They also serve for cooling the heat-producing device to keep it in normal operation, reducing the thermal noise and leakage current of electronic components.

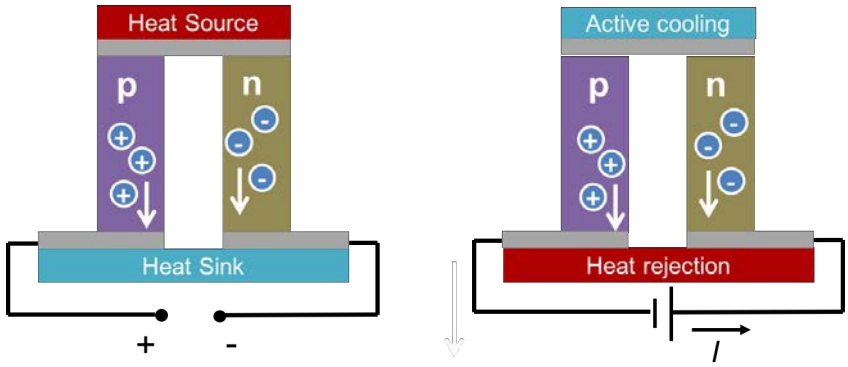

Figure 1.8: Thermocouple composed of an n-type (negative thermopower and electron carriers) and a p-type (positive thermopower and hole carriers) semiconductor material connected through metallic electrical contact pads. Thermoelectric generation (left) and cooling (right) modes are displayed.

A thermoelectric device can also be used to generate power if a temperature difference is applied between the two ends of a thermocouple. This process is called *thermoelectric generation*, and is the main focus of this thesis. Heat source at the junction causes carriers to flow away from the junction and built up a voltage to the module terminals due to Seebeck Effect.

The advantages of thermoelectric devices are compactness, quietness and robustness (no moving parts), and being applicable for any size of heating/cooling source. Moreover, energy in the form of waste heat (0% efficiency) that would normally be lost may be converted into useful electrical energy (7–8% efficiency) using a thermoelectric power generator [68].

Thermodynamics of heat engines leads to lots of energy being wasted in form of low-grade heat. About two-thirds of energy is lost as waste heat in different scenarios of energy usage or conversion. Thermoelectricity offers a way to recover part of that waste heat back into the system in form of electricity. This is a way of greening industrial processes, or even energy conversion plants, saving extra consumption of fossil fuels and reducing the corresponding emissions. Thermoelectric generators devoted to energy recovery can be of medium size, large size and even gigantic size. Efficiency in

those applications, ranging from automotive to waste heat recovery from industrial plants, is important, but also other considerations related to the bill of materials (affordability, availability, environmentally friendliness) matter a lot: in the end a competitive €/W value is needed to give such technology a chance. A different application, harvesting, aims at getting convenience electricity from a heat source in order to be able to power an electric device in a situation where there is no access to the grid, e.g. charging a mobile from a campfire. In these cases, the size of the thermoelectric generator will depend on the device power requirements. A particular harvesting scenario, which is the one this thesis focuses in, is converting heat into electricity at the (sub)milliwatt scale to provide full power autonomy to sensing nodes deployed within wireless sensor networks. In order to deploy such sensors unobtrusively in IoT scenarios the nodes should be of small size, which also points to a small size for the microharvesters. This prospective situation of billions of small devices also has materials and technological constraints to sort out.

The efficiency of a thermoelectric device will be briefly explained in this section. Next, the recent works on the thermoelectric microgenerators will be emphasized.

1.3.1 Thermoelectric devices efficiency

The efficiency of a thermoelectric device not only depends on the materials figure of merit but also on the thermoelectric device itself. As previously commented, a thermoelectric device generally includes two alternating thermoelements which are connected thermally in parallel and electrically in series. The efficiency of a thermoelectric device (η) is defined as heat-to-electricity conversion and expressed by the formula:

$$\eta = \frac{P_{el}}{Q_{in}} \tag{1.9}$$

where P_{el} is the electrical output power dissipated at external load (R_{load}), and Q_{in} is the heat absorbed by the device. Q_{in} has contributions from the thermal conductance of the device (Eqn. 1.10), Peltier cooling (Eqn. 1.11) and Joule heating (Eqn. 1.12) as described above:

(Thomson contribution is neglected)

$$Q_1 = K(T_h - T_c) = kA\frac{\Delta T}{L} \tag{1.10}$$

$$Q_2 = \Pi I = ST_hI \tag{1.11}$$

$$Q_3 = -\frac{1}{2}R_{int}I^2 \tag{1.12}$$

where k is the thermal conductivity, K is the thermal conductance of the device, R_{int} is the device internal resistance, and S and Π are the Seebeck and Peltier coefficients, respectively. Considering that the maximum power output is achieved when the $R_{load} = R_{int}$:

$$P_{el} = \frac{V^2}{4R_{int}} = \frac{S^2\Delta T^2}{4R_{int}} \tag{1.13}$$

Therefore, efficiency of a thermoelectric device can be rewritten as:

$$n = \frac{\dfrac{S^2\Delta T^2}{4R_{int}}}{kA\dfrac{\Delta T}{L} + ST_hI - \dfrac{1}{2}R_{int}I^2} \tag{1.14}$$

After some math,

$$n = \frac{T_h - T_c}{T_h}\frac{\sqrt{1+ZT_m}-1}{\sqrt{1+ZT_m}+\dfrac{T_c}{T_h}} \tag{1.15}$$

where $T_m = (T_c + T_h)/2$. The efficiency of a thermoelectric device is determined by ZT, which is different from the materials figure of merit, zT, with a capital Z. ZT includes the loss mechanisms in the device such as thermal and electrical contact resistances of the interconnects. To minimize the loss mechanisms through the whole device assembly, metallization should be perfectly electrically conducting and should be stable at high temperatures. In addition, the geometry of the thermoelectric legs should be carefully designed to optimize the total thermal conductance of the device. Thermal resistance between the boundaries of the components is also critical to minimize the losses. Figure 1.9 demonstrates the power generation

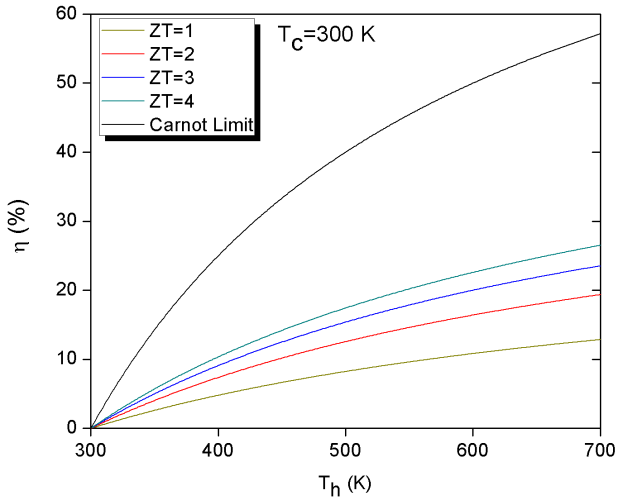

Figure 1.9: Power generation efficiency with respect to temperature of the hot side plotted for Carnot limit and different ZT values. Cold side temperature is taken as 300 K.

efficiencies with respect to hot side temperature for different ZT values calculated by Eqn. 1.15. Even though high ZT values larger than 1 are included in the graph (which would require even larger zT to account for device losses), the achieved efficiencies are far from the Carnot efficiency, which is $(T_h - T_c)/T_h$. It is worth noting that the device approach of this thesis will concurrently improve both zT (by thermoelectric material nanostructuring) and ZT (by reducing internal thermal and electric contact resistances due to monolithic integration).

1.3.2 Literature review on thermoelectric devices

Thermoelectric generators have been applied over a wide range of power outputs from microwatt conversion of body heat to power a wristwatch [69] up to hundreds of watts conversion of heat from a nuclear reactor for space applications [15]. Low power applications from the miniaturized thermoelectric generators will be summarized in the next section. Regarding the high power generation, thermoelectric

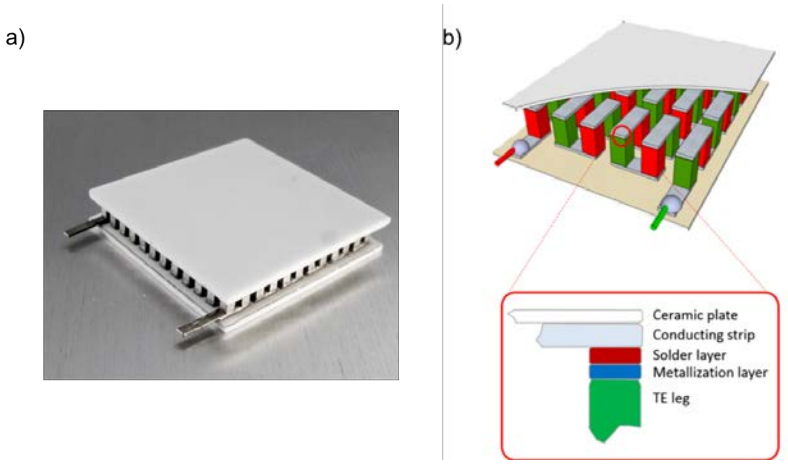

Figure 1.10: a) Typical bulk thermoelectric module from Kryotherm. b) The configuration of a thermoelectric module and the stacking layers between thermoelectric leg and the conducting strip [71].

generators are usually used for waste heat recovery [70]. These bulk TEGs are usually composed of individually mounted thermoelectric legs of 1 mm in size made of Bi_2Te_3 related semiconductor materials. They can generate up to tens of watts at maximum hot plate temperatures around 250 °C. Typical bulk TEG configuration can be seen from Figure 1.10. Since this thesis focuses on low power harvesting, more detailed review is presented on miniaturized thermoelectric generators.

1.3.2.1 Miniaturized thermoelectric devices

With the emerging applications of Internet of Things, small and low power sensors which are provided energy by harvesting have started to become essential. However, there are certain difficulties and limitations in making highly miniaturized thermoelectric modules because of the fragile nature of the mostly used thermoelectric materials. In addition, the number of p/n couples fitting in a limited space available makes it impossible to obtain relatively high output voltage for power generation.

Micro and nanotechnologies are called to play a key role in the fabrication of miniaturized TEGs since they allow mass production with significant reduction in size. Although no longer in production,

Seiko [69] and Citizen [72] developed wristwatches powered by thermoelectrics. Two companies developed commercial thermoelectric microgenerators taking advantage of thin film technologies. Micropelt was the first company to deploy ready-to-use microcoolers and microgenerators in the market. They were using wafer level technology to mass produce thermoelectric microgenerators (µTEGs) with $(Bi, Sb)_2(Te, Se)_3$ compound semiconductor thin films, however, they are reported as insolvent as of December 2015. The Nextreme company (bought by Laird technologies in 2013) used Bi_2Te_3–Sb_2Te_3 staggered superlattices for n- and p-type thermoelectric legs. Both of these commercial products exhibited vertical TEG architectures in which thermoelectric legs stand like pillars on the substrate surface, and the same holds for the applied or generated temperature gradient. Therefore, the heat flow is perpendicular to the substrate surface. In the horizontal/planar architecture, thermoelectric legs are oriented parallel to the substrate surface, and the temperature gradient is applied or re-adapted along the substrate surface.

Taking advantage of the microfabrication techniques, new technologies with promising performance levels are in development which allow the use of common, abundant materials in the form of low dimensional structures such as thin films and nanowires. Si has been intensively studied since it is abundant, cheap and it can be easily integrated into current microfabrication technologies. Regarding Si thin films, planar configuration with horizontal gradients has been shown to be more effective since larger ΔTs can be achieved when the heat flow is parallel to the thin film. Perez-Marin et al. [27] reported µTEG based on 100 nm thick single crystalline Si layers, which exhibited power density of 4.5 µW/cm^2 at an imposed ΔT of 5K across the structure. Infineon Technologies and TUM reported power density of 6.21 µW/cm^2 for ΔT of 10 K across the chip using 400 nm thick Si layers as thermoelectric material [28]. In that study, an external ΔT is applied by placing the chips between heatable thermochuck and a Peltier cooler.

Motivated from high zT values reported by Boukai and Hochbaum et al. [36], [37], several research groups have been working on implementing Si NWs into µTEGs to test its applicability in low power generation devices. Figure 1.11 shows some of the approaches reported for Si NW based µTEGs. Li et al., [39] reports on a vertical

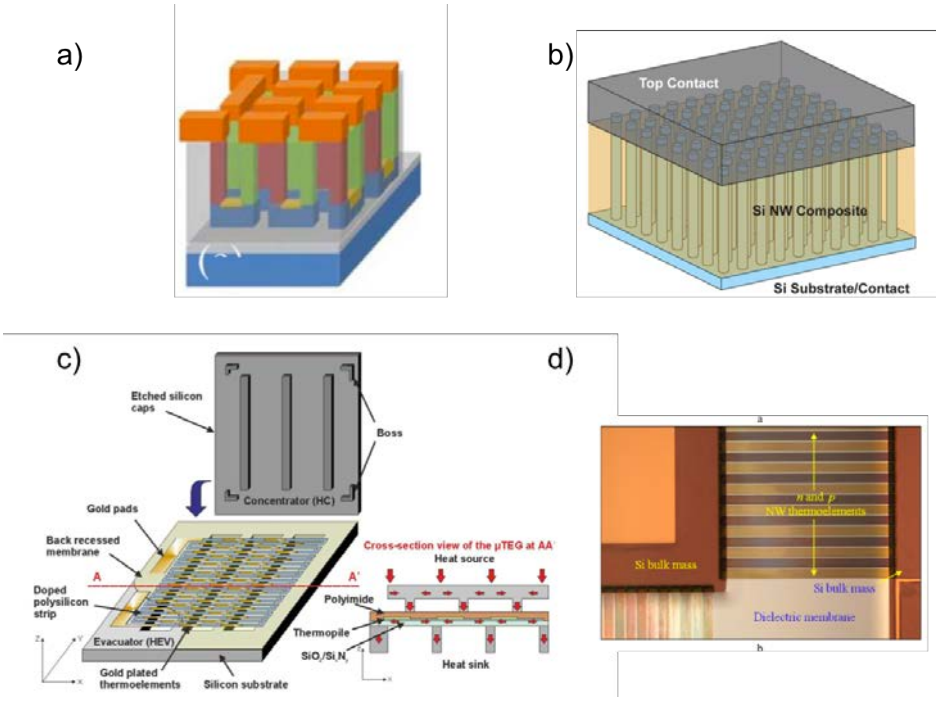

Figure 1.11: Different top down approaches for vertical (a-b) [39], [40] and planar (c-d) [73], [74] Si NWs based µTEGs.

µTEG with 1 µm tall Si NWs arrays, which consists of 540x540 wires in a device area of 5x5 mm^2. A low power output of 1.4 nW for an estimated ΔT of 0.12 K across the Si NWs (ΔT of 70 K across the experimental setup) is observed due to high wire and contact resistances. Similar vertical approach has been reported by Curtin et al.[40] with similar Si NW height, however, the gap between the NWs are filled with spin on glass to have a low thermal conductivity Si NW/spin on glass composite. With this approach, they achieved 29.3 µW of power output for a heater-imposed ΔT of 56 K from a device area of 50x50 µm. Researchers at Imperial College [46] demonstrated two sided Si NW array/bulk TEG which is capable to produce 3.5 µW at an external temperature difference of 37 K.

Regarding planar architectures, Ziouche et al. [73] recently reported high thermal resistance µTEG that can generate a maximal output power of 12.3 $\mu W/cm^2$ for an input heat of 2 W/cm^2. In another study [74], stacked 950 µm long top-down polysilicon Si NWs

demonstrated a Seebeck voltage of 500 mV from the preliminary measurements when µTEG is placed on a hot plate at 50 °C. Another recent study is the investigation of Si NW based µTEG on a flexible substrate which is reported by Choi et al. [38]. In this study, strain dependence of the thermoelectric performance is also discussed. Low thermoelectric performance is reported (1.3 nW at an applied ΔT=52.1 K) due to high internal electrical resistance.

Aforementioned studies (both vertical and planar architectures) are based on *top-down* fabrication of the thermoelectric materials. The first implementation of *bottom-up* Si NWs into planar µTEGs has been reported by Davila et al. [62], [75]. This work follows the same approach, however, optimization of the µTEG performance is studied as well as the heat exchanger integration.

SiGe has been integrated into µTEGs as thin films by Infineon and IMEC [28], [76]. In [28], poly SiGe based µTEG produced 2.73 µW/cm^2 when an external ΔT of 8.5 K is applied. Ref. [76] reports on a power output of 0.45 µW for an external temperature difference of 29 K. There is only one attempt from Imperial College [77] to demonstrate SiGe NW arrays output power. However, in that study, Si bulk or Si NWs are used as a n-type leg while including SiGe NW arrays as a p-type leg built by MACE process. The attained power outputs (and power densities) were very low (1 nW for ΔT of 2-3 K), which was attributed to high internal electrical resistances. This thesis, and another one performed in collaboration at IREC, reports for first time on the performance of SiGe NWs based µTEGs.

Chapter 2

Experimental methods

2.1 Overview

In this chapter, the route of the fabrication process of the µTEG is briefly described. A detailed description and optimization steps will be explained in Chapter 3. Next, experimental procedure for the integration of Si and SiGe NWs in the predefined trenches of the fabricated µTEG is explained. Finally, experimental techniques and setups used for the characterization of the µTEG are presented. A more detailed fabrication description including the optimization steps considered in this thesis will be explained in Chapter 3. Experimental details on the heat exchanger integration will be presented in Chapter 4 together with the other details/characterizations of the assembled µTEG.

2.2 Strategy of the µTEG Fabrication

The idea behind the proposed thermoelectric microgenerator (µTEG), which is merging top-down silicon micromachining technology with bottom-up silicon nanowire (Si NW) growth, was first presented by Davila et al.[62], [75], [78]. One of the main objectives of this thesis is to improve the design of the µTEG to prevent parasitic heat losses and increase the power output.

A basic sketch of the fabrication route of a single thermocouple can be seen in Figure 2.1. Top-down micromachining techniques on

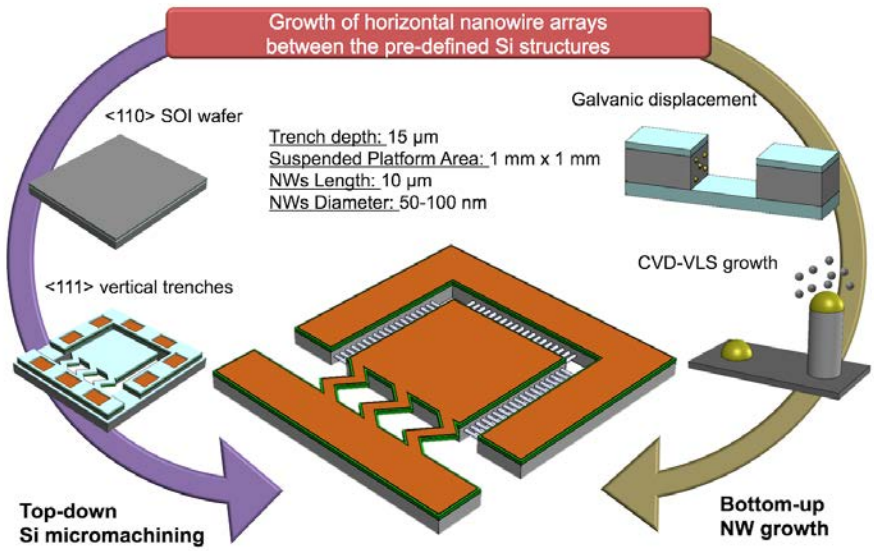

Figure 2.1: Schematic of the fabrication route for a single thermocouple with typical dimensions involved.

silicon on insulator (SOI) substrates are used to fabricate a microplatform composed of a suspended Si platform surrounded by a bulk Si rim. When placed on a waste heat source, the suspended platform and the bulk Si rim act as a cold side and a hot side of the generator, respectively. After completing the fabrication of the microplatform, p-type Si and SiGe NW arrays have been integrated laterally by a bottom-up Vapor-Liquid-Solid (VLS) method between the isolated suspended platform and the bulk Si rim on top of a SOI substrate.

For technological simplicity, our planar µTEG is fabricated employing a uni-leg architecture, in which the thermocouple is formed by a semiconductor thermoelectric material (p-type Si or SiGe NW arrays) and a metal layer. The proposed architecture for the single thermocouple is easily scalable to parallel or serial connections in order to increase the current or voltage, respectively, of the final microgenerator (Figure 2.2).

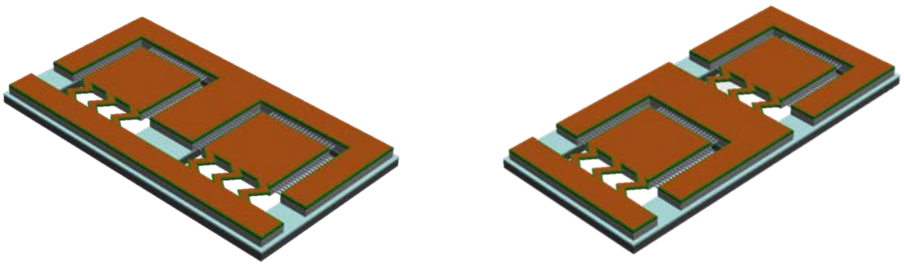

Figure 2.2: Parallel (left) and series (right) connection of devices to increase the power output.

2.2.1 Silicon technology processing for µTEG

The structural core of our planar microthermoelectric device is fabricated using standard microelectronic methods, lithography and thin film processes, combined with micromachining steps. In case the reader is not familiar with such silicon processing steps, they are briefly described in the following paragraphs:

Lithography: By means of this technique a wafer level 2D pattern containing microfeatures is replicated on a photosensitive resist layer spun on a silicon substrate. Such features are reproduced in chrome in a glass or quartz mask that is put above the resist coated wafer in contact or at a close distance to faithfully transfer optically those motives after being shone with UV light. After this exposure, the resist is then chemically developed and those areas that received no light remain in the wafer (in case the photoresist used is of 'positive' nature; the opposite effect is achieved if using a 'negative' resist). In addition to the device features, ancillary alignment motives are also transferred in order to serve as a reference for the alignment of subsequent masks. The reiteration of different mask levels and corresponding patterns configure the device architecture. Figure 2.3 illustrates the lithography and patterning steps.

Patterning: The resist pattern on top of a given thin film layer is then used as an etch mask when the wafer is exposed to a wet bath or a dry (plasma based) process that is tailored to remove the layer that is kept unprotected by the resist, and whose etch progresses at an adequate differential rate with respect the etch of the resist

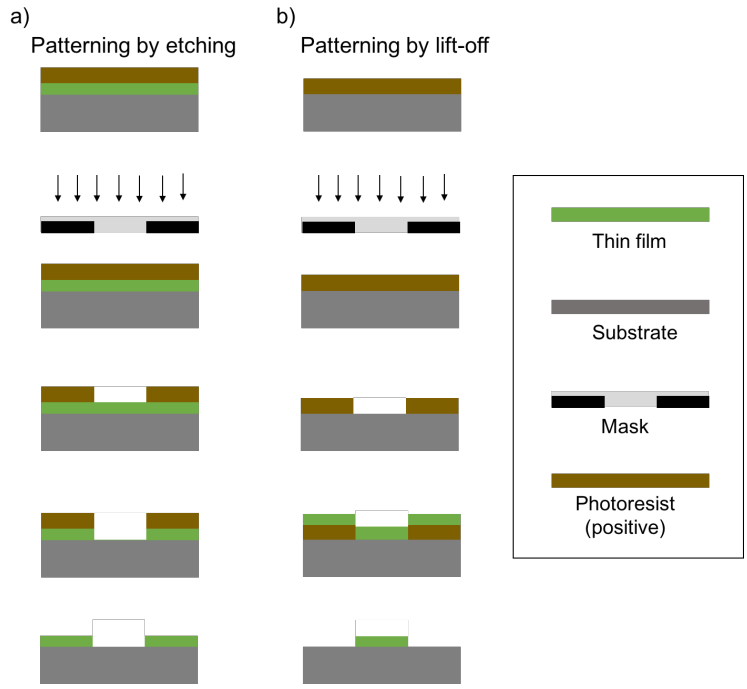

Figure 2.3: Photolithography and pattern definition by means of a) wet/dry etching and b) lift-off. Illustration shows the case with positive photoresist.

mask itself (attending to the different thickness of both layer and resist). The resist remnants after the process are eliminated (ashed) using a O_2 plasma. Usually, the resist is patterned on top of the layer on which the pattern wants to be reproduced. In the particular case of a lift-off (Figure 2.3b), the order is reversed: the resist is deposited and patterned first, and then the layer is placed on top of it. The resist is then chemically removed (using a dissolvent and ultrasounds), a process that lifts from the wafer the portions of the layers attached to the resist. In order to obtain the desired effect, the resist should reflect the negative pattern intended for the layer. Also due to the chemical and mechanical nature of the removal process, a much thicker resist than the layer itself is recommended.

Wet etch: As mentioned above, different wet etchings are tailored for different layers by preparing solutions that contain chemical species that react with the target layer by forming soluble com-

pounds. A wet etch usually progresses isotropically, meaning that the etch evolves laterally as well as in depth.

Dry etch: Alternatively, a given layer can be etched away by means of a plasma process that increases the reactivity of etchant gases that react with the target layer producing volatile compounds. A dry etch usually has a physical directional component (kinetic milling of the layer by impinging of ions). The resulting etch profile is more vertical than when using a wet etchant.

Thin film processes: the layers to be etched need to be laid on the wafers first. This can be achieved through different means. One is making some species, normally in gas phase, to react with the silicon itself (or previous layers) like the oxidation of silicon or polysilicon layers. Such processes usually require high enough temperatures. If the involved species contain all the precursors needed for the layer in mind, this can be obtained in the process atmosphere itself and be chemically deposited in the substrate. The temperature required is usually lower, and although the process can take place at atmospheric pressure (APCVD), it is common to do it at low pressure (LPCVD). If part of the thermal energy needed to activate the reaction of the precursors is provided electrically by means of a plasma enhanced process (PECVD), the deposition can take place at even lower temperatures, making the process compatible with the presence of materials, like metals, with lower temperature stability. Metals themselves are usually deposited by means of sputtering techniques, in which inert ions as Ar are directed by a plasma towards a target of the material (metal) to be deposited. The metal is etched from the target and ends up deposited as a film on the opposing substrate. It is usually a low temperature process.

Micromachining: When instead of vertically patterning a given thin layer, it is removed in a way that a self-standing structure is formed, we are talking about micromachining. If such process takes place by removing laterally a sacrificial layer, the process is called surface micromachining. If the removed layer is partly the silicon itself, usually in a quasi-vertical fashion, the process is called bulk micromachining. This silicon etch can proceed both by wet means or dry processes. In this thesis both are used for defining the microgenerator. For wet etching a KOH anisotropic etchant has been

used. KOH etches silicon but the etch rate depends on local atom densities. That means that more 'dense' planes as (111) are etched much slower than (100) ones, so that the silicon is carved following crystallographic patterns. Resist is not a good mask for such processes, dielectric layers such as oxide and nitride are needed instead. A dry approach, deep reactive ion etching (DRIE), can be used to remove silicon away defining high aspect ratio walls/holes. Usually DRIE uses the so called Bosch process, in which an etch step and a passivation step (local polymer deposition) are subsequently repeated by cycling different specialty gases as many times as needed leaving behind deep vertical scalloped walls. The whole thickness of a silicon wafer can be etched in this way. If this is the case, a thick resist may not be enough as a mask. Alternative materials that are more slowly etched away are needed, such as aluminum or a thick oxide.

A detailed description of the µTEG microfabrication process is given in Chapter 3. Next section describes the experimental details on the bottom-up growth of NWs.

2.2.2 Si and SiGe NW growth

2.2.2.1 Overview

The µTEG reported in this thesis requires the horizontal integration of the Si-based NW arrays, which can be achieved by techniques such as electron beam lithography [53], [55], superlattice nanowire pattern transfer (SNAP) [36], conventional KrF lithography [44], [79] and chemical vapor deposition (CVD) [80]–[82]. Although the latter is less accurate, it allows high-level control over NW composition, direction, diameter, crystal structure and doping. Also as a bottom-up method, it does not require top-down patterning after ultra-fine-pitch lithography. Its scalability, easy application, and high growth rates also make CVD the most preferred method for growth of Si-based NWs.

The following subsections describe the NW growth using the optimized conditions of CVD-VLS process. It is important to note that optimization of the growth process has been conducted at IREC and detailed in Ref [83].

2.2.2.2 Galvanic displacement

The VLS mechanism is assisted by a metal catalyst which is deposited by a galvanic displacement method. Gold (Au) is selected as a metal catalyst for the growth of NW arrays for the following reasons [38], [84]:

- Au can be selectively seeded, which is a critical requirement for the proposed microgenerator. NW arrays should only grow on the predefined trenches to be used as thermoelectric material. Growth of NWs is not desired on the rest of the device to prevent unwanted electrical/thermal contributions.
- Since the eutectic temperature of Au-Si alloy is low (363°C), it allows the nanowire growth at moderate temperatures.
- High solubility of Si and Si/Ge in Au-Si eutectic alloy enables a fast growth in comparison to other catalyst materials.
- Au is extremely stable in ambient conditions.

The approach used for the deposition of Au nanoparticles is called galvanic displacement method, which is a type of electroless deposition method that takes place under aqueous, room temperature conditions. The mechanism of galvanic displacement on Si surface is presented in Figure 2.4. It occurs by simultaneous redox processes that result in charge exchange on Si surface.

Those simultaneous redox reactions leading to the deposition of Au nanoparticles on a Si surface are as following:

$$\mathrm{Si(s) + 6\,F^-(aq) \longrightarrow {SiF_6}^{2-} + 2\,e^-}$$
$$\mathrm{{Au}^{3+}(aq) + 3\,e^- \longrightarrow Au(s)}$$

Where (aq) and (s) represent aqueous and solid phases, respectively. When Si is exposed to a hydrofluoric acid (HF) containing solution, it dissolves as silicon hexafluoride (SiF_6) and avoids the formation of silicon oxide (SiO_2) on the surface. At the same time, Au is deposited on the Si surface with a known size and density that is determined by solution properties.

For the deposition of Au nanoparticles in this thesis, Au microemulsions are prepared by mixing an aqueous solution with an

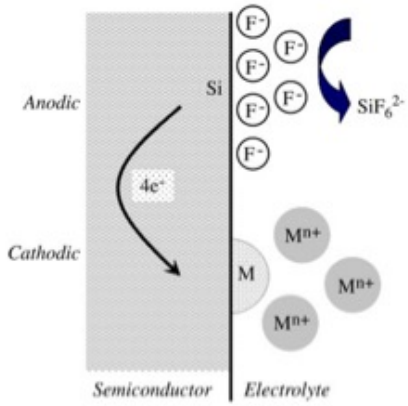

Figure 2.4: Galvanic displacement mechanism on a Si surface [84].

organic phase. The aqueous solution consists of deionized (DI) water with 0.01 M Sodium tetrachloroaurate(III) dihydrate ($NaAuCl_4$) and 0.2 M HF. The organic phase, on the other hand, is composed of n-heptane with 0.33 M sodium bis(2-ethylhexyl) sulfosuccinate (AOT, a surfactant). The ratio of DI water to surfactant is represented by R, and it directly affects the size distribution and dispersion homogeneity of Au nanoparticles [81], [83]. For the NWs synthesized for this thesis, R is optimized to be 168 which is achieved by mixing the same amount of volumes of both aqueous and organic solutions.

The process starts with immersing the chips in HF (5%) for 5 min to remove the native oxide on the Si trench walls. Chips are then rinsed with DI water, isopropanol (IPA) and dried with compressed nitrogen (N_2). Next, they are dipped in sonicated microemulsions which are prepared by mixing and aqueous solution with an organic phase with the proportions described in the above paragraph. Dipping time is critical to obtain a homogeneous distribution of nanoparticles especially in deep trenches. Even though a dipping time of 30 s is enough to obtain homogeneously distributed nanoparticles on bare Si substrates, 10 min is required to reach the bottom of the trenches (15 µm deep vertical walls) of the proposed µTEG. Following each dipping, the chips are subsequently immersed in cleaning baths of acetone, DI water and IPA, and dried gently with compressed N_2. At this point, Au forms a disordered pattern formed by agglomerated crystallites. To obtain well-defined particles, the samples are

then annealed in air at 400°C for 30 min using both heating and cooling ramps of 20°C min^{-1}. The galvanic displacement method employed is the same for both Si and SiGe NWs.

2.2.2.3 CVD-VLS growth

The VLS growth is a bottom-up 1D crystal growth mechanism that is assisted by a metal catalyst. It usually occurs at high temperatures, therefore processes such as chemical vapor deposition (CVD), molecular beam epitaxy [85], laser ablation [86] and carbothermal reduction [87] are generally used. In this thesis, the CVD technique is used for VLS growth of NWs.

Previous studies show that NWs grow preferentially perpendicular to (111) surfaces [82], [88]. Taking advantage of this, (110) surface oriented SOI wafers (hence with vertical (111) surfaces) are chosen as substrates to grow NWs laterally. Figure 2.5 describes the VLS mechanism for the lateral NW growth between the predefined trenches of the microgenerator with vertical (111) surfaces. The concept of growing NWS as a bridge between the pre-fabricated microdevices has been introduced before [62], [82], [89], [90]. When samples are exposed to a vapor precursor at high temperature, metal catalyst nanoparticles start to adsorb the vapor components of the precursor and form a liquid alloy. With time, the alloy becomes supersaturated and drives the precipitation of the component at the liquid-solid interface to minimize the free energy of the alloy system. This starts crystal NW growth and continues while vapor components are supplied [91]. When NW reaches the opposite trench wall, it welds to the trench wall and continues its growth in the other <111> direction [82]. Since the mechanism involves a vapor phase (precursor), a liquid phase (catalyst alloy), and a solid phase (precipitated NWs) at the same time, it is called VLS mechanism.

The most common precursors used for Si growth by CVD are halide precursors such as silicon tetrachloride ($SiCl_4$) or hydride sources such as silane (SiH_4) and disilane (Si_2H_6). In the preceding study by Davila et al., $SiCl_4$ was employed as Si source for Si NW growth by CVD-VLS. In this thesis, on the other hand, SiH_4 is chosen instead of $SiCl_4$ since it allows the growth at lower temperatures.

For CVD-VLS growth of Si NWs, silane (SiH_4) is used as a pre-

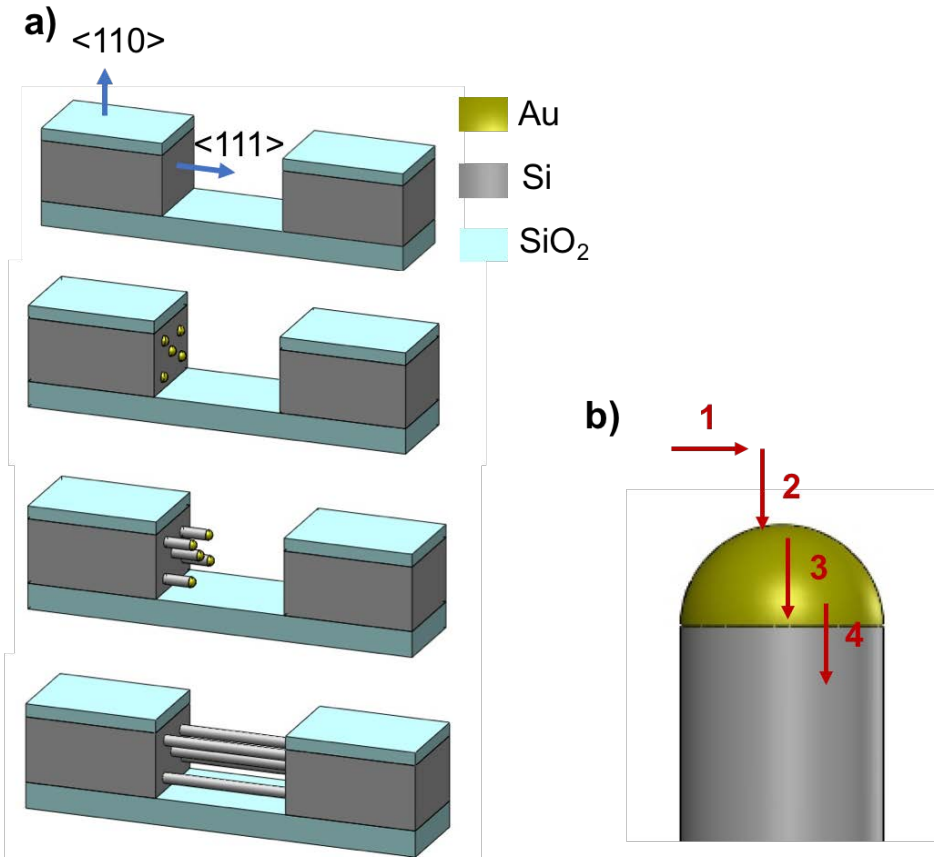

Figure 2.5: a) Schematic illustration of Si NW arrays growth from a vapor source between the predefined (111) walls. b) Closer view on the VLS mechanism steps: (1) mass transport in the gas phase; (2) precursor (SiH_4) adsorption on vapor–liquid surface and chemical reaction at the interface; (3) Si diffusion in the Au-Si liquid phase; and (4) Si atoms supersaturation in the alloy and incorporation in the crystal lattice.

cursor while SiH_4 and germane (GeH_4) are used together for SiGe NWs. Hydrogen (H_2) is used as a carrier gas during the growth. Diborane (B_2H_6) is used as a precursor for in-situ p-doping of both type of NWs. Hydrochloric acid (HCl), on the other hand, is used to hinder gold migration and controlling the morphology of the NWs. Several factors are affecting the final morphology of the NWs such as Au NP distribution and morphology, growth pressure and temperature, which have been studied in detail by IREC [83]. Table 2.1 summarizes the optimum parameters that are used for the growth and the resulting NW properties.

Table 2.1: VLS-CVD growth parameters and resulting properties of Si and SiGe NWs. Adapted from Ref [83].

Parameter	**Si NWs**	**SiGe NWs**
Temperature	630 °C	650 °C
Pressure	2.5 Torr	2.5 Torr
HCl flow	30 sccm	30 sccm
H_2 flow	1085 sccm	1257 sccm
SiH_4 - H_2 flow	15 sccm	200 sccm
GeH_4 - H_2 flow	-	$8 \cdot 10^{-1}$ sccm
B_2H_6 - H_2 flow	$3.8 \cdot 10^{-3}$ sccm	$3.8 \cdot 10^{-3}$ sccm
Property	**Si NWs**	**SiGe NWs**
NW diameter	112 ± 31 nm	64 ± 11 nm
NW density	3.9 NWs/µm^2	4.9 NWs/µm^2

2.3 Thermoelectric characterization

This section aims to briefly describe the characterization techniques together with the setups used. Prior to characterization of the devices, samples are packaged and wire bonded. Figure 2.6 shows the basic diagram for the wire bonding and the chip after packaging. Ceramic quad flat packages (CQFP) from Kyocera are used for the encapsulation of the samples (Drawing number PB-12941-C). These packages contain 44 flat leads and a 7.62 mm x 7.62 mm wide die

cavity. Thermally conductive electrically insulating epoxy (EPO-TEK®H70E) is used to attach the devices onto the packages. This epoxy is stable up to 440°C which makes it adequate considering that the characterization temperatures will be lower than 350°C.

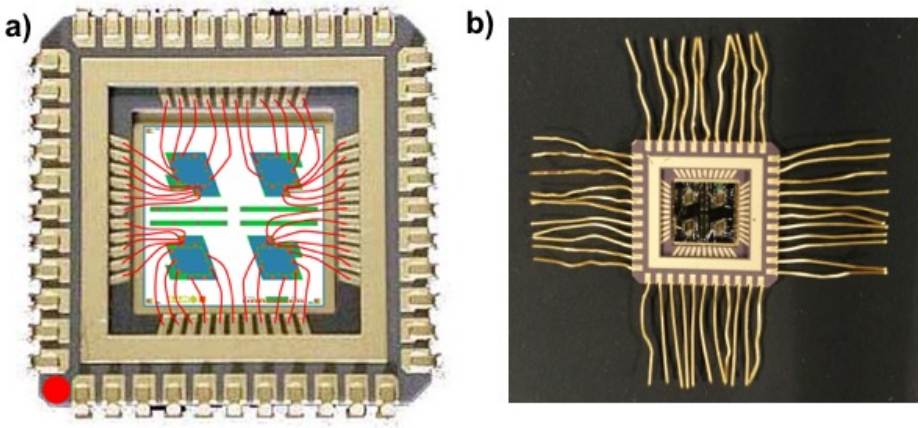

Figure 2.6: a) Schematic of a chip placed inside the package including wire bonding diagram. b) Encapsulated and wire bonded chip.

2.3.1 Contact resistance

As discussed in Chapter 1, it is very important to decrease the device internal resistance to increase the efficiency of thermoelectric generator. Optimizations in process flow are conducted in this thesis to decrease the contact resistance and will be detailed in the following chapter.

Measurement of the contact resistance between the device Si layer of the SOI substrate and the metal is conducted using the transmission line model (TLM) configuration. On each chip, TLM structures are fabricated together with the devices using the same mask set. The sketch of the TLM test structure can be seen in Figure 2.7a. These structures are composed of rectangles (adjacent pads) with the same size and thicknesses. The only difference is the distance between each structure which helps the accurate measurement of contact resistance.

Measurements are done by applying a voltage between several pairs of adjacent pads in a row and measuring the current flow. They

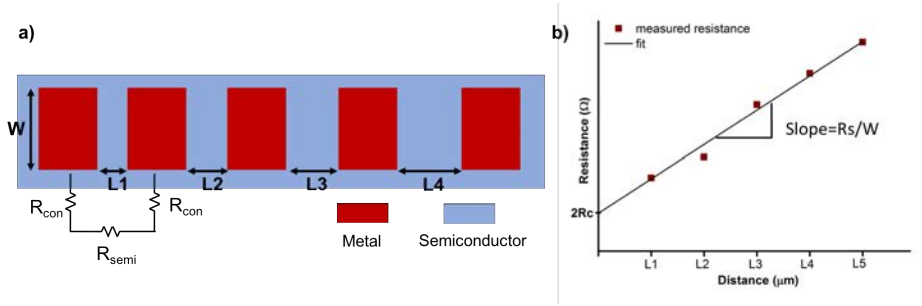

Figure 2.7: a) The TLM test structure and b) the plot of the measured resistance as a function of the pads distance. R_c and R_s stand for contact resistance and sheet resistance, respectively.

are done in a 4 wire configuration, using an HP4155 semiconductor parameter analyzer and a Karlsuss PA200 semiautomatic probe station (Figure 2.8).

The resistance between two adjacent pads is the series combination of 3 resistors: metal to semiconductor (R_{con}), through the semiconductor (R_{semi}), and back into metal(R_{con}):

$$R_{total} = R_{semi} + 2R_{con} \tag{2.1}$$

$$R_{semi} = R_s \frac{L}{W} \tag{2.2}$$

$$R_{total} = R_s \frac{L}{W} + 2R_{con} \tag{2.3}$$

$$R_{con} = \frac{R_s L_T}{W} = \frac{\rho_c}{L_T W} \tag{2.4}$$

Using the equations above, it is possible to obtain R_{con} by extrapolating the Resistance vs distance graph to $L = 0$ (See Figure 2.7b). In addition, the sheet resistance (R_s) of the semiconductor can be calculated from the slope of the line. Using these two values, we

can obtain the transfer length, L_T, which is the distance along the contact for which the voltage drops to $1/e$ of its value. It is also defined as effective length of the contact. Since current crowding occurs when TLM geometry is used, usual contact length cannot be used to calculate the contact resistivity (ρ_c).

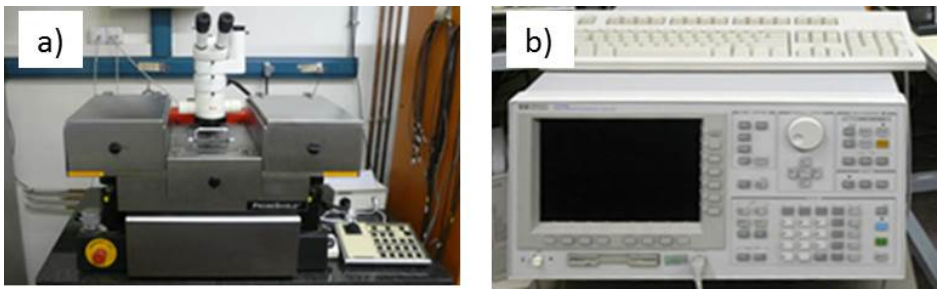

Figure 2.8: a) Karlsuss PA200 semiautomatic probe station and b) HP4155 semiconductor parameter analyzer used for 4-wire measurements.

2.3.2 Temperature coefficient of resistance

Temperature coefficient of resistance, or TCR, is one of the main parameters used to characterize a resistor, and allows its use as a thermometer. It defines the relative resistance change with respect to ambient temperature change, and it is usually expressed in ppm/°C (parts per million per centigrade degree). TCR being a positive number means that resistance increases with increasing temperature which is the case for pure metals. For elements like carbon, germanium etc. this coefficient is a negative number, meaning that resistance decreases with increasing ambient temperature. TCR can be calculated using the following formula:

$$R = R_{ref}(1 + \alpha(T - T_{ref})) \tag{2.5}$$

where R is the resistance at temperature T, R_{ref} is the resistance at reference temperature T_{ref}, and α is the temperature coefficient of resistance for the material.

The TCR of the metals used in this thesis is determined by placing the samples inside an oven and collecting the resistance data both during heating and cooling. Since cooling is slower than the heating

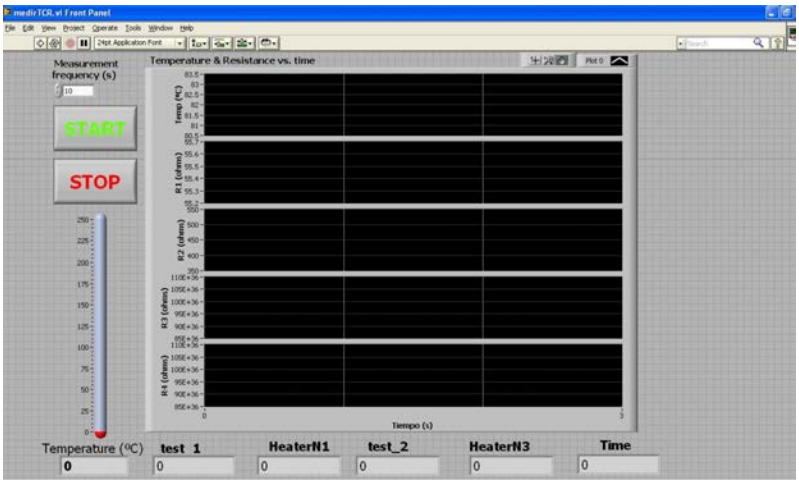

Figure 2.9: LabVIEW program interface developed for TCR measurements.

of the oven and hence better thermal equilibrium is achieved, more accurate data is obtained during cooling.

Measurements are done in 4-wires configuration with the setup shown in Figure 2.10. Since the temperature range used for the measurements is between 20°C and 250°C, any kind of soldering in the setup is avoided. Instead, high temperature stable cables are used with mechanical clamps which are isolated using Kapton®film to avoid any short circuits. Temperature of the oven is measured using a thermocouple connected to a Keithley®740 system scanning thermometer, and the resistance data is recorded using a multimeter data acquisition unit (Keithley®2700). Automated tests are performed by connecting both thermometer and multimeter to a computer using a GPIB (General Purpose Interface Bus) to a computer. A program developed with LabVIEW (National Instruments™) collects the data as shown in Figure 2.9. Resistance vs temperature graphs obtained by these measurements are then used to calculate TCR of the metals using Eqn. 2.5.

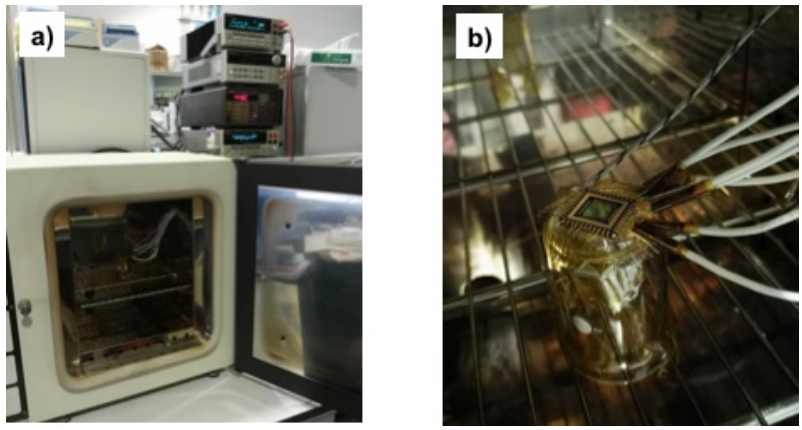

Figure 2.10: a) Oven and measurement set-up used for TCR, thermal conductance and Seebeck coefficient measurements. b) Closer view of the chip connected to high temperature stable cables inside the oven. Oven is kept at room temperature for thermal conductance measurements while TCR and Seebeck measurements are applied during heating the oven.

2.3.3 Thermal conductance of the platforms

Thermal conductance measurements are done in this thesis to evaluate the improvement attained in the thermal isolation of the suspended microplatform through its reengineered mechanical supports. Since these supports are thermal paths in parallel to the NWs, a strategy has been followed to decrease their thermal conductance to not impair the ΔT perceived by the NWs arrays and hence the thermocouple performance. These tests are done on devices that include a heater on the isolated platform. The measurement is conducted by Joule heating of the platform forcing a controlled current through the heater using the source meter Keithley®2400. In other words, a known amount of power is dissipated on the isolated platform using the heater and the developed temperature difference between platform and silicon rim is measured simultaneously. To be able to measure this temperature difference (ΔT), the heater has been previously calibrated as a thermometer by measuring its TCR as explained in the previous section. The temperature of the silicon rim is either measured with a second resistance or it is assumed to be equal to the ambient temperature.

Since our aim is to compare the thermal isolation of the microplat-

forms themselves, encapsulated chips without NWs are used for the measurements.

2.3.4 Seebeck coefficient

Similar to thermal conductance measurements, Seebeck coefficients are also measured by calibrating the heater as a thermometer and dissipating power on it to achieve a ΔT between microplatform and silicon rim. An additional multimeter (Keithley®2700) is connected to the internal and external collectors of the device to measure the open circuit voltage (Voc) developed at two ends of the NWs. Measurements are done by placing the encapsulated chip inside the oven, and forcing different ΔTs (2.5, 5, 7.5, 10, 12.5 K) at different ambient temperatures (RT, 50°C, 100°C, 150°C, 200°C, 250°C). The Seebeck coefficient can be calculated from the slope of Voc vs ΔT curve for each ambient temperature. The LabVIEW program interface developed for the Seebeck coefficient and thermal conductance measurements can be seen in Figure 2.11.

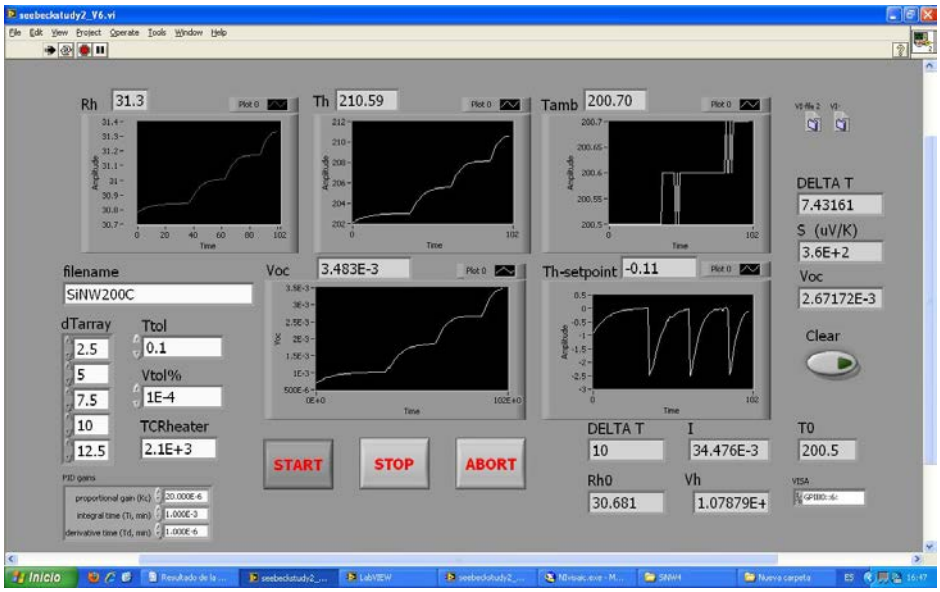

Figure 2.11: LabVIEW program interface developed for thermal conductance and Seebeck coefficient measurements.

2.3.5 Thermoelectric power

For the measurement of thermoelectric power, the closest approach to the real-life harvesting operation is applied. Devices are placed on a hot plate and a temperature difference is built up between the bulk Si rim (hot side) and the thermally isolated platform (cold-side).

A Linkam THMS 350V is used as a heating stage which allows working both in ambient and in vacuum conditions at temperatures ranging from -196°C (with a nitrogen cooling system, not used in this thesis) to 350°C. This stage includes 8 in-chamber connector pins that can carry electrical signals to external measurement devices. For that purpose, most of the chips used for this measurement are encapsulated and wire-bonded previously. Alternatively, for measuring devices that are not encapsulated, a probing stage has been built and micropositioners are used for connections (Figure 2.12). A Dino-Lite USB microscope is also included in the setup with its imaging software for the proper placement of the micropositioner tips on the devices. In all cases, chips are mounted on the heating stage using Omegatherm "201" high temperature and high thermal conductivity paste. A glass slip cover can also be placed on top of the heating stage to ensure isolation when required (encapsulated chips).

I-V and power curves are collected using two multimeter data acquisition units (Keithley®2700 and HP 34401A) and a source meter unit (Keithley®2400). They are connected to the computer together with the temperature controller (TMS94V) of the Linkam heating stage through GPIB communication. Multimeters are used to measure the Voc developed across the NWs and the resistance of the thermometer on the bulk Si rim and the heater on the suspended platform. By introducing the TCR values of the metals to the interface, this resistance is directly converted to temperature. The source meter unit is used to measure I-V characteristics, starting at V=0, then increasing the voltage until we reach the pre-measured Voc. Measurements are repeated for each temperature after stabilizing the set point temperature during the selected holding time (usually 1 min).

Figure 2.13 shows the automated program developed for thermoelectric power measurements using LabVIEW. It includes a temperature controller to read and operate the temperature of the hot plate. Minimum and maximum temperatures, temperature step, heating

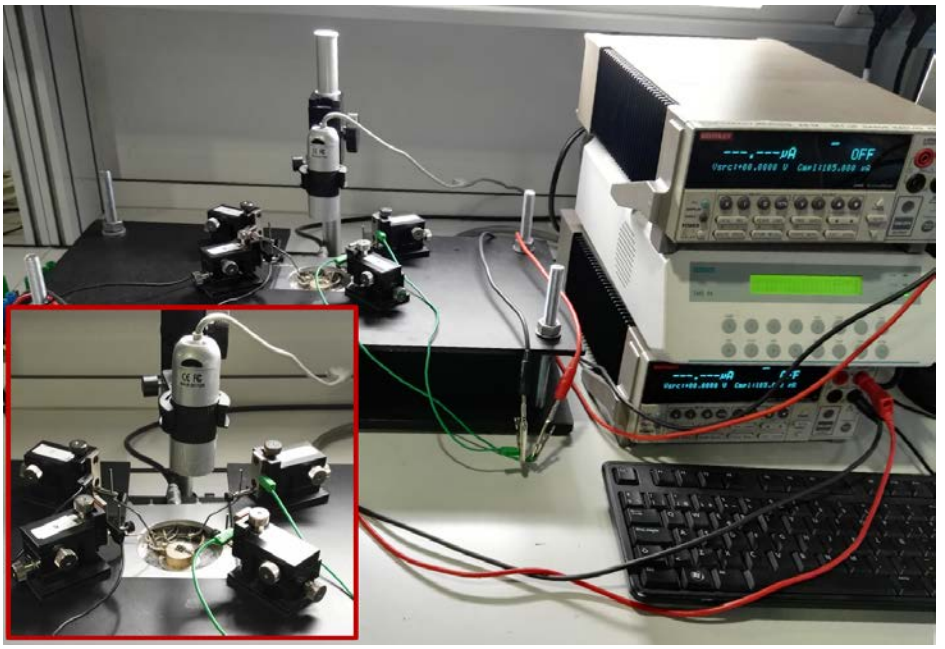

Figure 2.12: Setup used for the thermoelectric power measurements. Inset shows a closer view of Linkam heating stage.

rate and holding time at each temperature can be set through the program. It also measures NW resistance, Voc, temperature of the thermometer on bulk Si rim simultaneously. I-V and power curves (I·V) can also be obtained at each temperature that is set before starting the measurement.

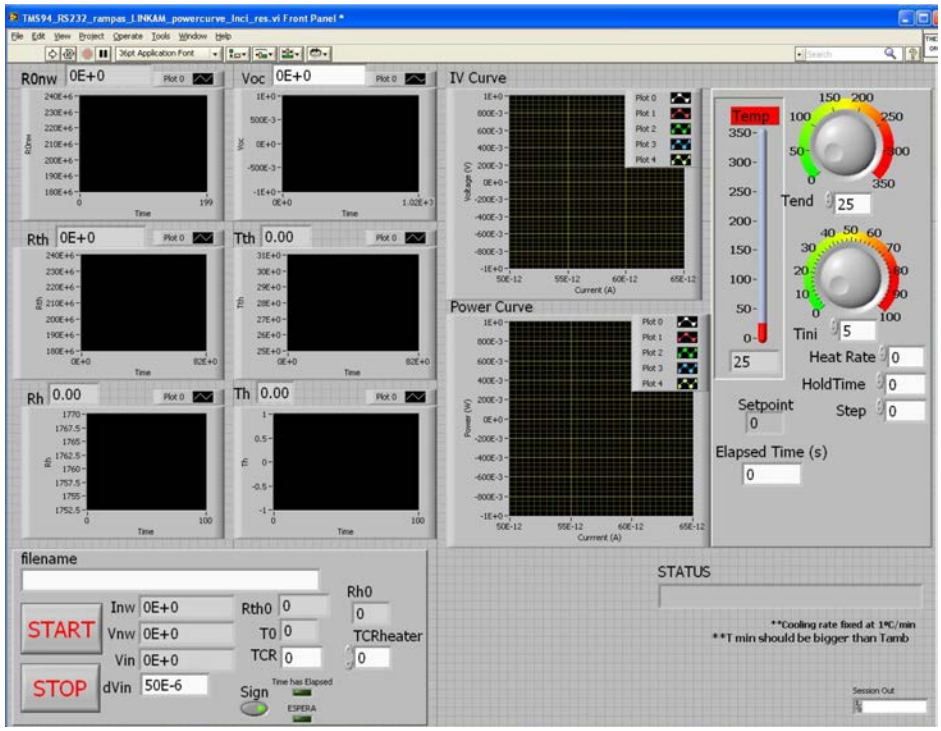

Figure 2.13: LabVIEW program developed for thermoelectric power measurements. Measurements of hot side and cold side temperatures and NW resistance can also be performed simultaneously.

Chapter 3

An optimized all-Si based thermoelectric microgenerator

3.1 Overview

This chapter presents the optimized design for an all-Si based thermoelectric microgenerator (µTEG) using Si and SiGe nanowire (NW) arrays as thermoelectric materials. In the next section, microfabrication process amendments to improve thermal and electrical performances of the microgenerator are explained together with design considerations in terms of device architecture. Next, microfabrication process steps for µTEG are described in detail. Finally, thermoelectric characterizations of the thermoelectric microgenerators (µTEGs) are presented and trade-offs of the different design parameters are studied.

3.2 Thermoelectric microgenerator design

Maximizing materials zT by optimizing the thermoelectric coefficients is not enough to have an efficient thermoelectric generator. A thermoelectric device should be considered as a whole together with its metallization, heat sink-heat source, and has to be engineered carefully to minimize loss mechanisms. This section focuses

on fabrication process amendments designed for the enhancement of µTEG thermal performance by basically improving the temperature difference attainable between the two active Si parts and decreasing the device internal electrical resistance.

Figure 3.1 shows the colored SEM images of the µTEGs with different designs to clarify the functions of different device parts.The 1^{st} generation design presented herein refers to the device design conducted by Davila et al.[78] (Figure 3.1a), whereas the 2^{nd} generation design stands for the design of the µTEG after the optimizations realized within the scope of this thesis (Figure 3.1b). Both of them include a built-in heater (green) to be used as a temperature sensor and to dissipate power for test purposes, and internal/external collectors (yellow/orange) to measure the Seebeck voltage and device resistance, and hence the final thermoelectric power output. In the 2^{nd} generation design, an additional thermometer is included (red) to be able to measure the temperature of the bulk Si rim. In the 1^{st} generation design, the suspended platform has an interdigitated structure to increase the area to be filled with NWs. In the 2^{nd} generation design, on the other hand, a square shape has been chosen to ease the heat exchanger integration, which will be explained in Chapter 4.

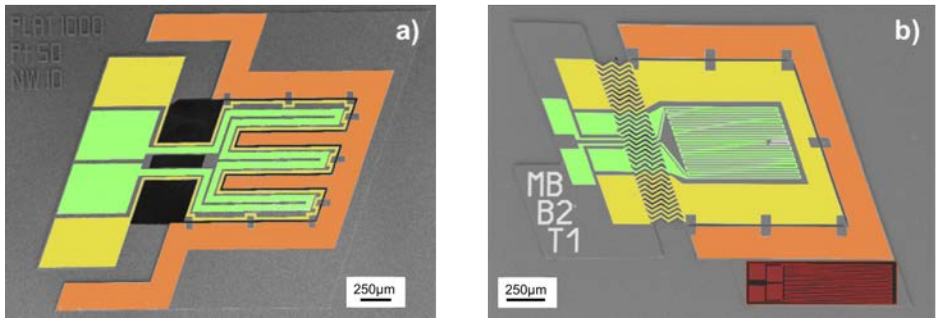

Figure 3.1: SEM images of the a) 1^{st} generation and b) 2^{nd} generation µTEG designs. Images are colored to clarify functions of each structure: built-in heater (green), internal collector (yellow), external collector (orange), and thermometer (red).

3.2.1 Platform thermal response optimization

The efforts to optimize the thermal performance of the microplatform have been focused on minimizing the thermal parasitic losses between the hot and cold ends of the microplatform. SEM images in Figure 3.2 presents the structural differences between three designs of microplatforms emphasizing the different physical connection between the thermally isolated suspended platform and the bulk Si rim. To be able to evaluate the improvements attained in the optimized design, devices with the 1^{st} generation design have also been produced and used as a reference. All devices feature a built-in heater on the isolated platform and they all have a trench area 10 µm wide to be filled with NWs.

In the 1^{st} generation device (Figure 3.2a), bulk Si bridges linked the suspended platform to the bulk Si rim to act as a mechanical support and as a holder for the electrical connections placed on top. However, the high thermal conductivity of bulk Si reduces the microplatform thermal isolation and limits the device ability to obtain a large temperature difference from a waste heat source. To be able to develop a large temperature difference with the presence of high thermally conducting supports, significantly long and narrow bridge supports are needed which require larger device area and reduce the power density (because of the larger area involved and the increased electrical resistance of metals). Therefore, in this thesis, a new technological route has been developed to replace these bulk Si bridging supports by a thin dielectric membrane (Figure 3.2b and c), which features a lower thermal conductance because of the membrane material conductivity and the thin membrane form factor. With this new arrangement, the hot and cold Si parts are closer to be only ideally connected through the thermocouple active materials, i.e. NWs and metals, avoiding the high thermal conductance bulk silicon supports that were limiting the device performance. It is important to mention here that there are also smaller bulk Si beams on the corners of the suspended platform to keep it stable before the NW growth. These beams are later cut by focused ion beam as explained in the microfabrication section of this chapter.

The definition of the membrane requires a dedicated processing step since the Si beneath the dielectric thin film needs to be removed.

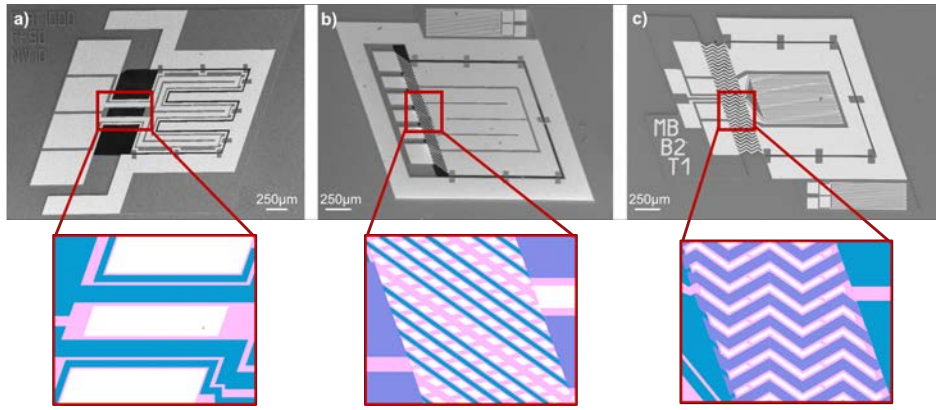

Figure 3.2: SEM images of the microplatforms with different designs. a) 1^{st} generation design with a bulk Si bridge. b) Intermediate design replacing the bulk Si bridge with a thin dielectric membrane. c) 2^{nd} generation design which enables to effectively remove Si under the thin nitride membrane. Zoomed schematics of the bulk bridge and membranes are extracted from the mask layout.

For reasons that will be clear in the following section, this removal is done from the top side rather than from the bottom one. This points to an open membrane geometry with a particular angled design and the use of Si wet etch. In this way, the etchant will also remove laterally the Si when progressing down the Si areas exposed through the holes, and the membrane will be freed in a reasonable processing time. A potassium hydroxide (KOH) solution with a concentration of 40% at 80 °C is used as an anisotropic wet etchant. The design of the membrane itself and of the device as a whole makes use of the dependence of the KOH etch rate on the different Si crystallographic planes.

The geometry of the intermediate design (Figure 3.2b) is composed of a criscrossing pattern of wide and narrow nitride support lines. The wide ones will host the metal lines on top and the narrow ones will contribute to the mechanical stiffness of the membrane. The angled arrangement of the lines is defined so that the sides exposed are aligned to vertical Si walls that correspond to fast KOH etching planes. A short etch is enough to etch most of the bulk Si under the membrane leaving residual remaining Si islands under the nitride intersections. Those Si islands can be observed in Figure 3.3a,

which is taken after the wet anisotropic Si etch step to define the membrane. Since the Si islands are isolated, they don't create a continuous parasitic thermal path. However, they may create another problem after the integration of NWs. NWs grow also from these islands (Figure 3.3b), which is undesired because they might result in connecting the metal lines on the membrane which have different functions (e.g, connecting the heater to the internal collector should be prevented to be able to use the heater for characterization purposes). In order to prevent this, the membrane structure has been redesigned with a saw pattern, with again proper angles to enable fast Si lateral removal (Figure 3.2c). With this new zigzag shaped membrane design, it is possible to remove all the Si under the membrane area with an etching time of 30 min. Different etching stages of the Si under the membrane can be seen from the optical microscope images of Figure 3.4. A wet isotropic etch would also provide the lateral etching needed for the membrane release. However, this approach will be not adequate since this etch will equally affect any other exposed silicon areas. It is worth noticing that the proposed device requires the other three sides of the microplatform to be aligned to vertical <111> walls (preferential orientation for NWs growth). If those trenches are already defined by the time the membrane etch takes place, an isotropic etch will destroy them. On the other hand, the KOH etch rate for <111> walls is so slow that they are not significantly etched during the membrane definition. In fact, the etch helps to improve the surface quality and orientation of these walls. Alternatively, if the <111> vertical walls are not yet present, an extended membrane etch will naturally define them where they need to be. During the redesign of the membrane, width of the metal lines is also increased (from 5 to 15 µm) to decrease the electrical resistance.

The performance of thin dielectric membrane supports has been analyzed by thermal conductance measurements, and a significant amount of reduction of thermal conductance is observed for the microplatforms with a dielectric membrane compared to the ones with bulk Si supports. The characterization of the thermal conduction for different design parameters is explained in Section 3.4.1.

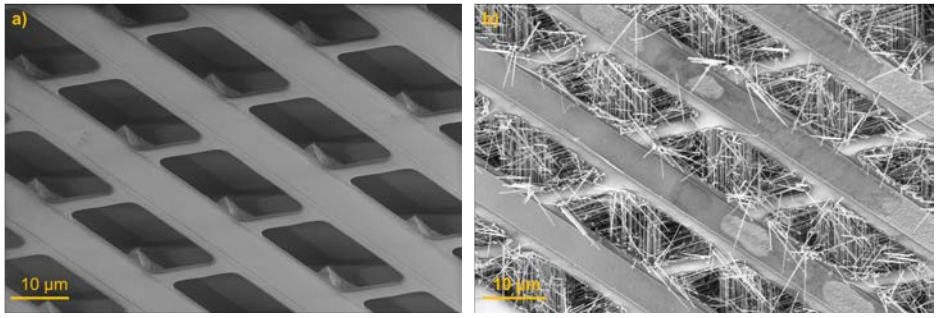

Figure 3.3: SEM images of the membrane with an intermediate design. a) Tilted SEM image showing the bulk Si islands remained under the membrane. b) The same membrane after Si NW growth, producing possible parasitic NW connections between the metal lines of the membrane.

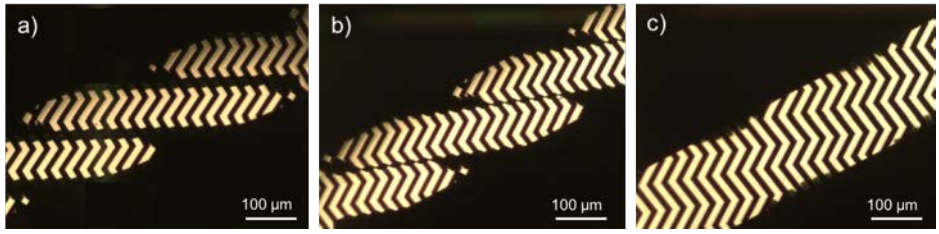

Figure 3.4: Backlight illuminated optical microscope images of the membrane during different stages of KOH etch. Images belong to samples after 20 min (a), 25 min (b), and 30 min (c) of etching.

3.2.2 Platform electrical response optimization

To be able to gain maximum power output from the µTEG, electrical resistances of both thermoelectric material and microplatform should be minimized. In this thesis, process optimizations and redesign considerations are employed to decrease the device internal resistance. There are different parameters contributing to total internal resistance of a µTEG:

$$R_{total} = R_{NWs} + R_{metal} + R_{contact(NW-Si)} + R_{contact(metal-Si)} \quad (3.1)$$

- $\mathbf{R_{NWs}}$ is the electrical resistance of nanowires and it depends on NW doping and density, which are optimized by IREC, and also their length. Boron doping level of NWs is estimated to be 3-8.10^{19} cm^{-3} for both Si and SiGe NWs. NW density is optimized as 3.9 NWs/μm^2 and 4.9 NWs/μm^2 for Si and SiGe NWs, respectively. Electrical resistance of NW arrays depends on the total trench area filled with NWs which is discussed in the characterization section of this chapter. Doping and density are process parameters, NW length is the only parameter affecting electric performance that can be changed by device design.

- $\mathbf{R_{metal}}$ is the metal resistance which can be reduced by designing the metal lines of the collectors wider and shorter. Since the dielectric membrane explained in the previous section offers much lower thermal conductance, it could be made wide, allowing wider and shorter metal legs with a much lower electrical resistance. In the new design, the resistance of the metal lines is decreased by a factor of 4-5 compared to the metal lines of the initial design.

- $\mathbf{R_{contact(NW-Si)}}$ is the contact resistance between the substrate and NWs. In this thesis, test structures are designed and fabricated for the measurement of NW-Si contact resistance. They enable to grow individual NWs with different lengths. Area-specific contact resistance is extracted from transmission line method (TLM) measurements and found to be 1-9.4 Ωcm^2, which is only 7% of the total NW resistance [83]. Such obtained

low contact resistance is in accordance with the quasi-epitaxial growth enabled by vapor-liquid-solid (VLS) mechanism.

- $\mathbf{R_{contact(metal-Si)}}$ is the metal-Si contact resistance which has been the limiting factor for the 1^{st} generation design of the µTEG. In this thesis, efforts are focused to decrease metal-Si contact resistance by adding additional process steps and studying different materials as metals.

R_{NWs} and $R_{contact(NW-Si)}$ are given (and controlled) by the way and by the conditions the NWs are grown. R_{metal} and $R_{contact(metal-Si)}$ are mediated by material choices, physical and geometrical design, and, especially for $R_{contact(metal-Si)}$, by processing conditions. In the following paragraphs the optimization of such processing conditions is discussed. In any case, low resistance ohmic contacts should be guaranteed to enable an easy charge flow. To determine this, I-V measurements are applied on TLM structures using a 4-wire configuration. As can be seen from Figure 3.5, depositing metal (150 nm W for this case) on a p-type Si substrate without any pre- or post-processing results in a non-linear rectifying contact behaviour which is not desired for the current application. This problem of rectification was not reported for the 1^{st} generation devices, it came out with the new set of wafers even though they have high doping levels (2-4x10^{19}). After annealing the sample using Rapid Thermal Annealing (RTA) system at 800 °C for 5 min under nitrogen (N_2) ambient, resistance decreases but still a non-linear contact is observed. Finally, when the same annealing conditions are applied on a previously B-doped wafer (implantation dose and energy of 5.10^{15} at/cm^2 and 50 KeV, respectively), a low-resistance ohmic behavior is observed. It is shown that both doping of the substrate and annealing after the metal deposition are needed to establish low-resistance and stable ohmic contacts.

After verifying the need of both doping and annealing to achieve an ohmic contact, next step is to choose the best suitable material to be used as a metal in those conditions. For that purpose, tungsten (W), titanium/tungsten (Ti/W), and titanium nitride/tungsten (TiN/W) are deposited on the Si wafers that are equally doped with the abovementioned parameters. These layers were chosen to investigate the formation of silicide layers ($TiSi_2$, WSi_2) on the contact

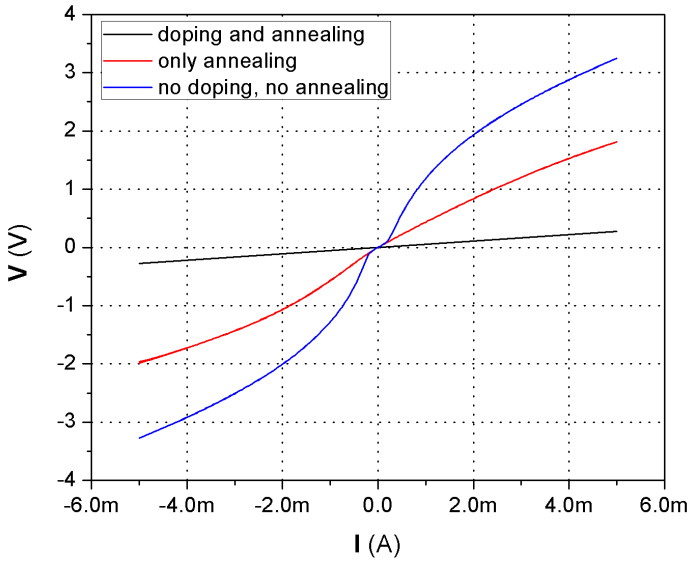

Figure 3.5: I-V curves measured from the same TLM structures. The metal used as a contact was 150 nm thick W. Annealing is applied using RTA at 800 °C for 5 min under (N_2) ambient.

resistance. After their deposition and patterning via lift-off process, all samples are similarly annealed with RTA at 800 °C for 5 min under N_2 ambient. As can be seen from Figure 3.6a, all three material combinations exhibit a linear ohmic behaviour with significantly lower resistance for the Ti/W. Resistances measured from the two equally placed TLM structures with the layers of TiN/W, W, and Ti/W are found to be 59 Ω, 54 Ω, and 29 Ω, respectively. Therefore, Ti/W is chosen to be used as an adhesion/metal layers for the proposed µTEG.

Figure 3.6b shows the effect of annealing temperature on the resistance. For this study, samples with Ti/W metal are exposed to RTA at different maximum temperatures. The rest of the parameters for RTA such as heating/cooling rate and annealing time are kept constant. Samples that are annealed at 700 °C and 800 °C have lower resistances than the sample annealed at 600 °C. Since the resistances of the samples annealed at 700 °C and 800 °C are almost

equal, 700 °C is chosen the be the optimized annealing temperature for this work. RTA process is applied under N_2 ambient for the measurements shown in this section. However, RTA was also applied under a vacuum ambient, and the results were found to be equal. Different annealing times were also studied (from 30 s to 5 min), and 30 s was selected for the process time since the obtained resistances were equal.

In this thesis, metal-Si contact resistances are calculated using the TLM method explained in Section 2.4.1. Additional parameters, such as sheet resistance of the semiconductor (R_s) and transfer length (L_T, that allows calculating an area independent specific contact resistivity) can also be derived from the same graph. It is clearly visible from Figure 3.7 that the contact resistance between TiW/Si is smaller than the contact resistance between W/Si. Calculated values for the abovementioned parameters are listed in Table 3.1.

Table 3.1: Parameters extracted from Figure 3.7 for different metal/Si contacts.

Parameter	**Ti+W (30+200 nm)**	**W (230 nm)**
R_c (Ω)	1.06	4.04
R_s (Ω/sq)	33.15	51.73
L_T (µm)	4.80	11.71
ρ_c (Ωcm^2)	$7.6{\cdot}10^{-6}$	$7.1{\cdot}10^{-5}$

Based on the abovementioned optimizations of the device internal resistance, total µTEG resistance is decreased to 10-40 Ω from 50-500 Ω.

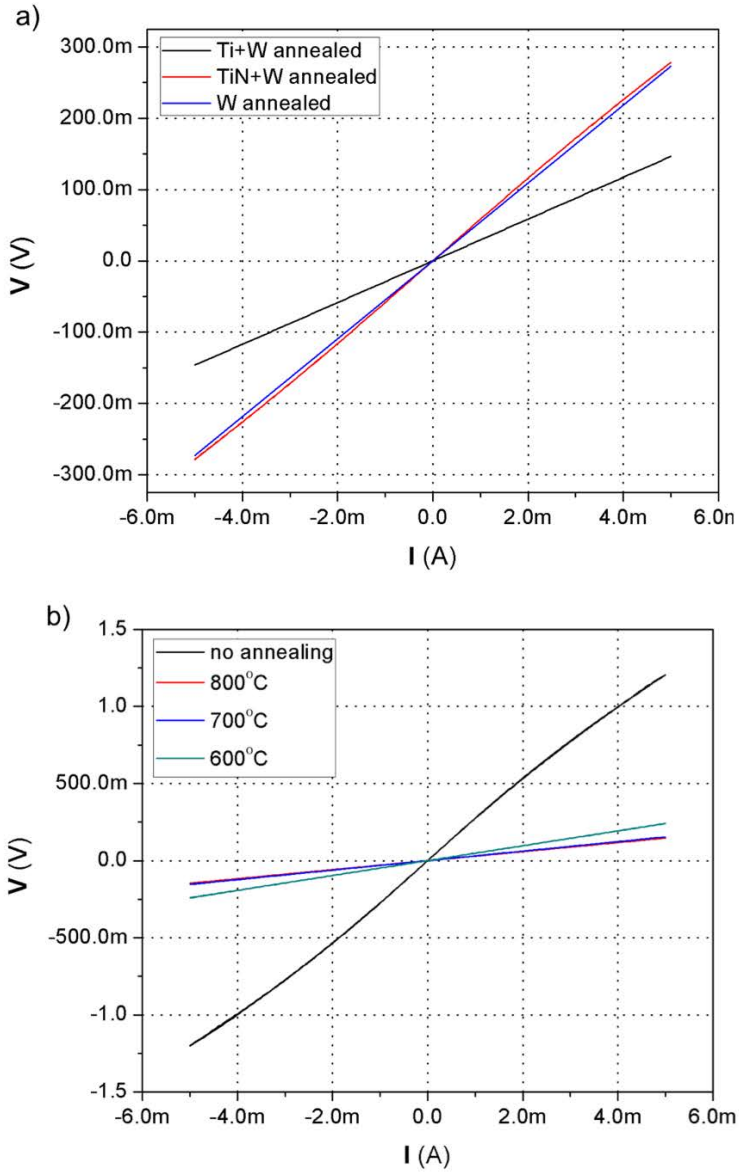

Figure 3.6: a) I-V curves measured from the same TLM structures of different material combinations processed under the same conditions (doping of the substrate and annealing of the metal). b) The effect of annealing temperature on the resistance for the sample with Ti/W.

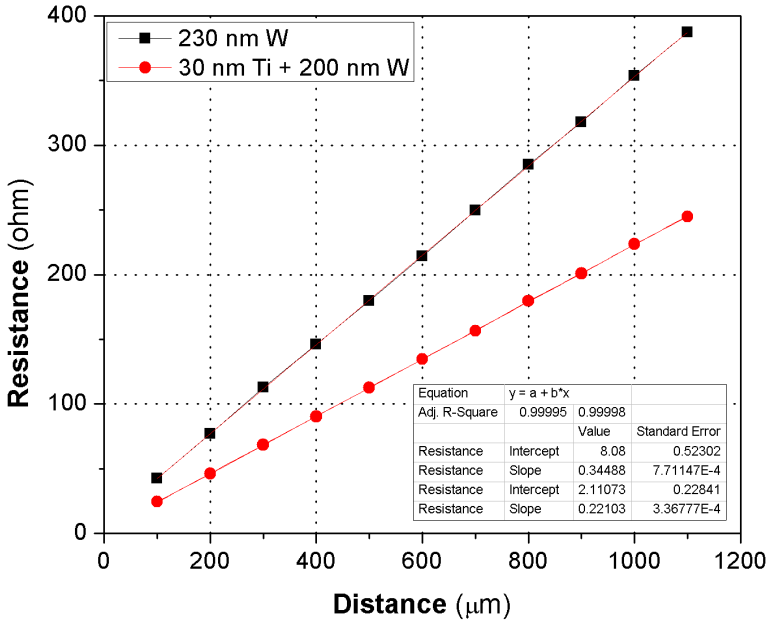

Figure 3.7: Total resistance vs distance plots measured using TLM structures for samples with different metal layers (Ti/W and W).

3.2.3 Other design considerations

A set of different layouts have been included in the mask set designed for all-silicon µTEGs (2^{nd} generation devices) to test the effect of device architecture on the final power output. All devices share a common area of 1mm^2 for the thermally isolated suspended platform. Devices with different lengths for the support bridge (thin nitride membrane) (100 µm and 200 µm) and with different number of consecutive trenches to be bridged by NWs (1-4) have been included in the mask set. The trench width is designed to be 10 µm due to the constraints of the NW growth method. The trench depth is defined by the thickness of the Si device layer of SOI substrate, which is chosen to be 15 µm to accommodate a large number of NWs. Figure 3.8 shows corners of the multiple trenches that are used to increase the effective NW length and hence the thermal isolation between the platforms. Midway silicon bars (3 to 6 µm) are used to define 10 µm wide consecutive trenches. Additional Si bars are also connecting the thermally isolated platform to bulk Si rim to provide robustness to the device before NW growth. These bars are cut using focused ion beam (FIB) after the NW growth to prevent these parasitic thermal paths between hot and cold areas of the device.

Three different metal designs are also considered on the thermally isolated platform for different purposes (Figure 3.9). The first of them is metal A (MA) which is composed of a continuous metal layer to be used as an internal collector for the harvesting measurements. These devices are used for the thermoelectric power characterization in this thesis. Second metal design (MB) consists a built-in heater to be used as a temperature sensor or to dissipate a power for testing purposes. This heater is fabricated on top of the nitride layer and separated from the internal collector. Thermal conductance and Seebeck coefficient measurements presented in this thesis are conducted using this type of devices. Finally, metal C design (MC) includes a metal square in the middle of the platform which is isolated from the Si device and internal collector for the heat exchanger integration purposes.

Standard chips feature 4 isolated devices. Serial and parallel connections of multiple devices have also been included in the design to enhance the power output by means of increasing voltage (V) and current (I), respectively (Figure 3.10). All chips include TLM

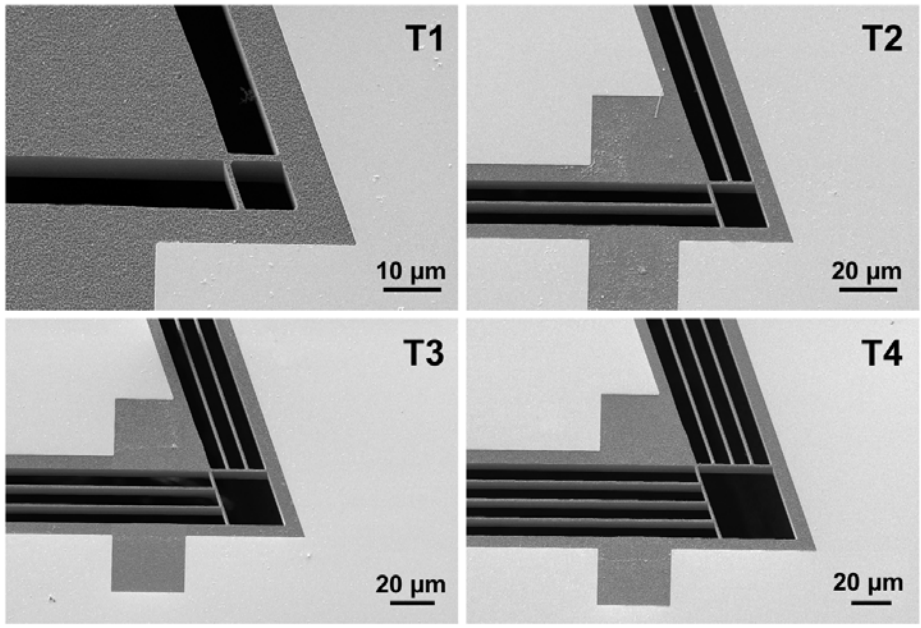

Figure 3.8: SEM images of the silicon structures used to increase the effective nanowire length, from 10 µm (T1) to 40 µm (T4), with successive trenches to be filled with Si and SiGe NWs.

structures on the unused areas to measure the metal/silicon contact resistance as explained in Section 2.4.1. All devices also include integrated thermoresistors to measure the temperature on the bulk Si rim.

In order to assess the nanostructured Si performance compared to regular bulk Si, devices with micron-sized Si beams have been also designed and fabricated. Figure 3.11 shows the µTEG with a 10 µm wide trench filled with a bulk Si micron-sized beams. The micron-sized beams are obtained after an anisotropic etch with KOH of the Si device layer of the SOI wafer, the same step that is used to free the self-standing dielectric supporting membrane mentioned before. Devices with different trench occupancies are fabricated. Since the beams are opened by anisotropic etch, resulting beams have a pyramidal shape arising from the oblique planes with a slow etch rate. Taking this into account, final trench occupancies for different devices are calculated to be 6.2%, 11%, 20.6% and 39.8%.

In summary, the device architecture features designed to test the

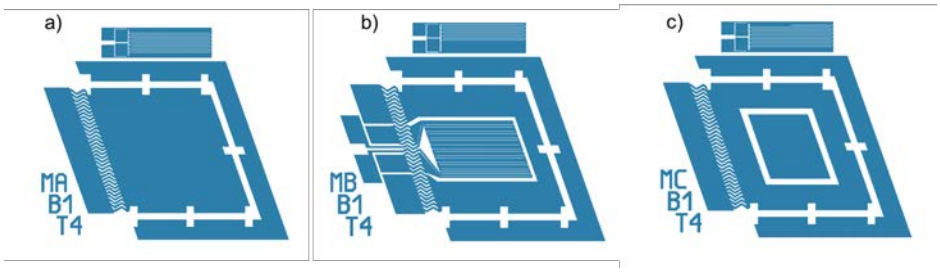

Figure 3.9: Metal designs for µTEG a) Metal A, which is designed to be used for harvesting, b) metal B, in which a heater is integrated for characterization purposes, c) metal C, designed to be used for heat exchanger integration studies.

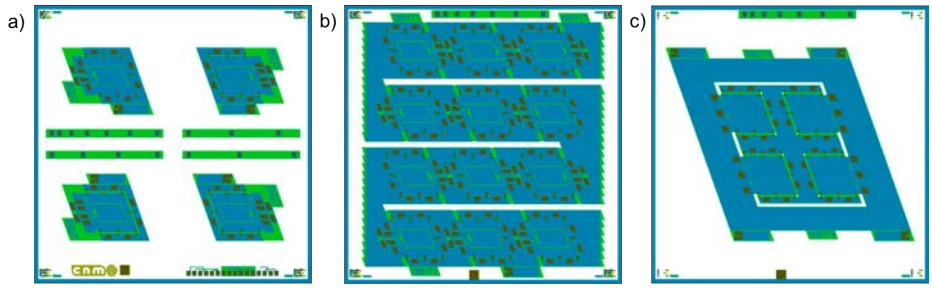

Figure 3.10: Different chip designs included in the wafer layout. a) Standard design with 4 individual devices, b) series connection of 12 devices, c) parallel connection of 4 devices.

influence of certain parameters can be listed as below:

- Harvesters with long bulk bridges and with thin dielectric membranes of different lengths
- Harvesters with different numbers of trenches (from 1 to 4) to be filled by NWs
- Harvesters with different metal structures on the isolated platform for test and heat exchanger purposes
- Harvesters with prefixed percentages of bulk (micron-sized) silicon beam connecting platform and rim

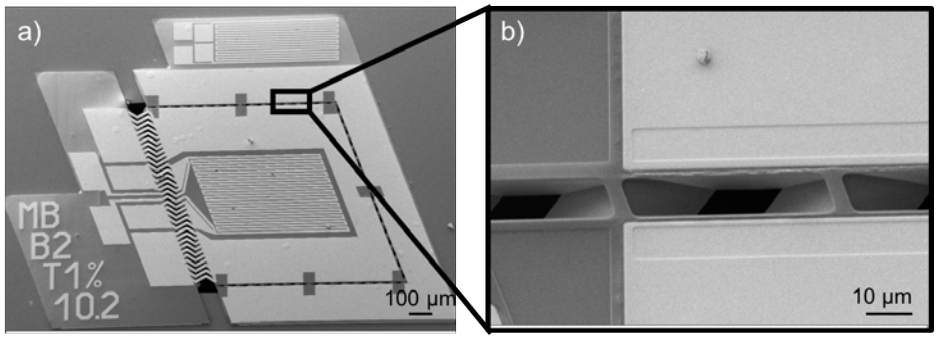

Figure 3.11: a) µTEG with a single trench filled with Si microbeams. b) Closer view to the trench area emphasizing the bulk Si beams with a pyramidal shape opened by KOH.

3.3 Thermoelectric microgenerator fabrication: microplatform definition and NWs integration

This section presents the microfabrication process steps for the proposed µTEG. All top-down fabrication processes of the Si microplatform are conducted at the Cleanroom Facilities of IMB-CNM (CSIC).

Design considerations explained in previous section have led to the definition of the technological sequences of top-down micro and nanofabrication steps which require the fabrication of a set of 5 photolithographic masks to structure the different device layers. The mask set used to fabricate the microplatform is briefly described in Figure 3.12.

Figure 3.13 illustrates the microfabrication steps for the proposed µTEG. Silicon-on-Insulator (SOI) wafers with (110) orientation are used as substrates for the fabrication of the µTEG. The reason of choosing this orientation is that the vertical walls of the microplatform can then be aligned to <111> planes, which is the preferred orientation to grow directional NWs by CVD-VLS. Our SOI wafers are composed of 15 µm of device Si layer, 1.5 µm buried oxide layer and 500 µm of bulk Si layer. Wafers are highly doped with boron (B) and the resistivity of the wafers was in the range of 0.003-0.005 Ωcm.

The fabrication process starts with a deposition of 300 nm thick silicon nitride (Si_3N_4) layer by Low-Pressure Chemical Vapor De-

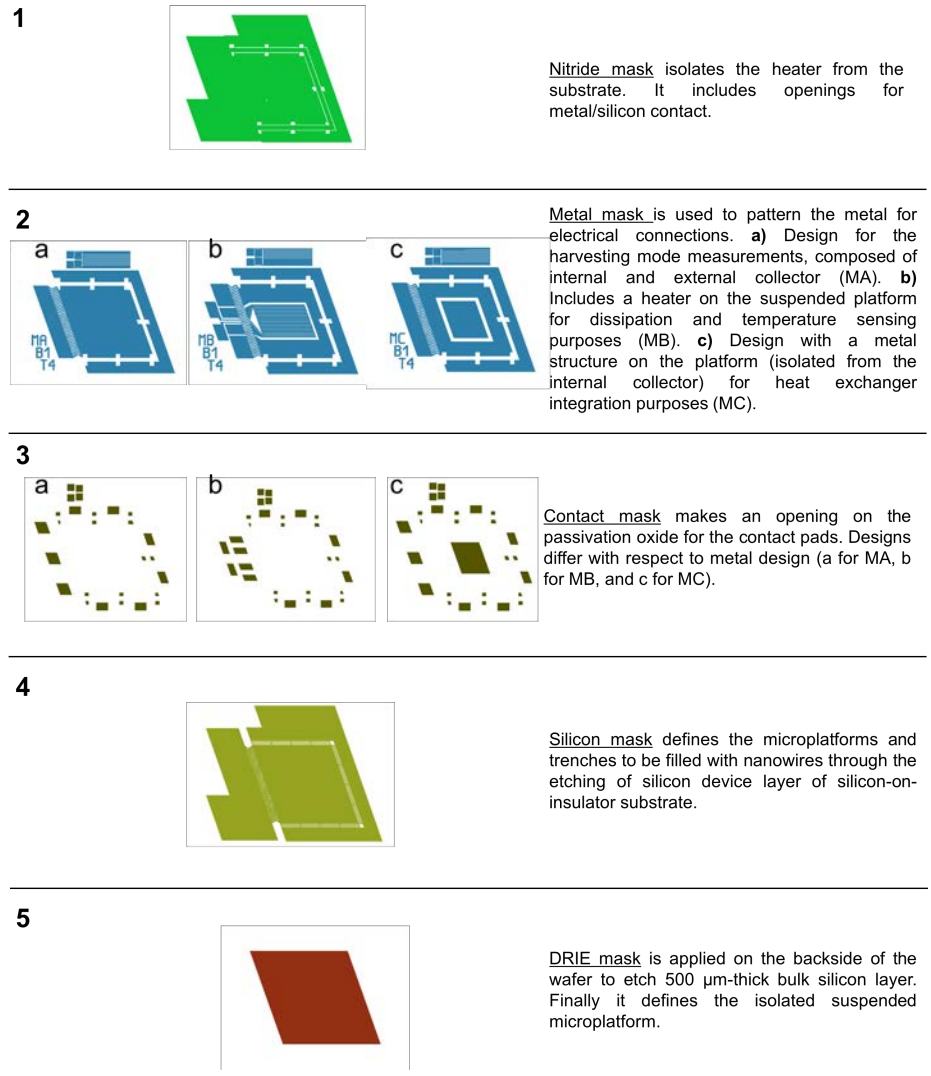

Figure 3.12: Mask layout for each photolithography step in the fabrication sequence with a brief explanation. Depending on the nature of the photoresist used (positive or negative), masks are redesigned in dark or bright field so that areas where the layer should remain or where should be removed are drawn. In our case, resist is positive so that masks 1, 2 and 3 show in color the remaining material, while 3 and 5 show where the involved material layer will be removed.

position system (LPCVD). After patterning with photolithography (*Nitride Mask*) and dry etch, this layer serves as both an insulating layer between the metal heater and Si device layers and as a support for metallic connections eventually bridging the platform and rim. It is important to note that LPCVD deposition is done on both sides of the wafer. Then, ion implantation of boron (B) is applied on the wafer with an implantation dose and energy of 5.10^{15} at/cm^2 and 50 KeV, respectively. The reason of applying the ion implantation after the nitride lithography step is to use the nitride as a mask of doping. By this way, we are protecting the trench areas of the wafer from doping since it might introduce defects that complicates the control of KOH wet etching step. Next, 30 nm of titanium (Ti) layer is sputtered as an adhesion layer followed by a subsequent sputtering of 200 nm of tungsten (W) layer. Metal layers are patterned with a lift-off process (*Metal Mask*). Then, wafers are exposed to rapid thermal annealing (RTA) under nitrogen gas (N_2) with a maximum temperature of 700 °C during 30 s to achieve an ohmic contact between the metal and device Si layer of SOI. Since we want to deposit the gold (Au) nanoparticles only on the trench walls, we need to protect the rest of the device. As discussed in Section 2.3.1, Au nanoparticles do not assemble on the oxide surface. Therefore, 1 µm thick high density silicon oxide (SiO_2) layer is deposited on the top surface of the device. Two masks are involved in the process of patterning the oxide. The first mask (*Contact Mask*) is used to thin this SiO_2 layer on the contact pads. The reason for that is to be able at the end to clear the oxide on the pads while leaving passivated the rest of the device. With the help of a different mask (*Silicon Mask*), next lithography is done and the previously deposited 1 µm thick SiO_2 and 300 nm thick Si_3N_4 are etched clearing the Si areas that will be later on etched by KOH. On the backside of the wafer, 3.5 µm thick high density SiO_2 is deposited on the LPCVD nitride layer, to be used as an etching mask during Deep-Reactive Ion Etching process (DRIE). After photolithography with the *DRIE Mask*, the handle wafer of our SOI (500 µm thick Si) is etched by the sequential exposure of SF_6 and C_4H_8 gases. The process continues with the thinning of the SOI buried oxide layer from 1 µm to 500 nm. Then, wafers undergo a dicing step to cut the wafer into chips of 7x7 mm^2. Before dicing, the wafer is protected by a photoresist. It should be noted that the

platform on the device layer is not suspended yet.

To suspend and thermally isolate the central platform, an anisotropic KOH wet etch step is applied. This step is very critical since it shapes the final microplatform by both defining the <111> trenches and by removing the Si below the low conductance nitride membrane with the metallic connections, the latter being the limiting one in terms of etch time. Definition of the fast and slow etch planes should be carefully designed as explained in the thermal optimization part of this chapter. Before starting the KOH process, samples are dipped in hydrofluoric acid (HF) 5% solution for 20 s to etch the native oxide layer on the Si trench walls. After the HF step, samples are subsequently etched with KOH solution with a concentration of 40% and temperature of 80 °C for 30 min. Timing should be arranged in a way that it should completely etch the Si under the membrane and the one in the trench areas where the NWs will grow, but it should not start etching the device Si layer of the suspended platform. Figure 3.14 shows the evolution of etching with respect to time in the microplatform support area. It is enough to disconnect the bulk Si under the membrane and to make sure that the gap distance is enough to prevent any unwanted connection by spurious NWs. Going beyond may endanger the device. The reason is that inhomogeneities in etching rate of DRIE at wafer scale might result in overthinning of the buried oxide layer of SOI. Since KOH partially removes SiO_2, this may lead to etching of the suspended platform by KOH as shown in Figure 3.14. After successful KOH etching, samples are rinsed with deionized (DI) water for 5 min and then placed into hydrochloric acid (HCl) for 10 min to clean the possible remaining potassium ions by the formation of potassium chloride (KCl). Finally, samples are again rinsed with DI water and IPA, and dried under air.

After releasing the membrane with KOH, samples are ready for galvanic displacement and NW growth. At this stage, only the Si at the walls of the device active area should be exposed; the rest of surface Si and metals should be still passivated (metal pads with a thinner oxide than the rest, as explained). NWs are grown between the predefined trenches using the CVD-VLS parameters explained in Section 2.2.2, and contact pads are cleared of any remaining thin oxide while keeping the rest of the device still passivated. Figure 3.15 shows the µTEG after the integration of Si NWs. To be able to

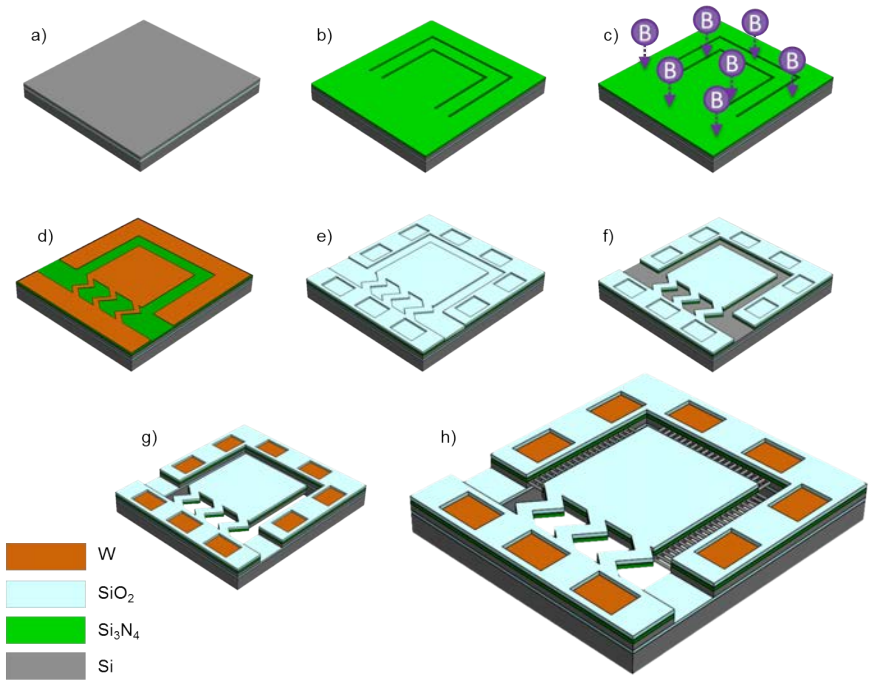

Figure 3.13: Schematical representation of the microfabrication steps of 2^{nd} generation µTEG. a) Starting SOI substrate, b) nitride deposition and patterning, c) doping of Si device layer of SOI using the nitride as a mask, d) deposition and patterning of metal layer via lift-off, e) passivation deposition and lithography for thinning the oxide on the contact layer, f) photolithography and dry etch of oxide to make the opening for KOH, g) backside DRIE for opening the bulk cavity and KOH to release the suspended microplatform, h) final image of the µTEG after the integration of NWs.

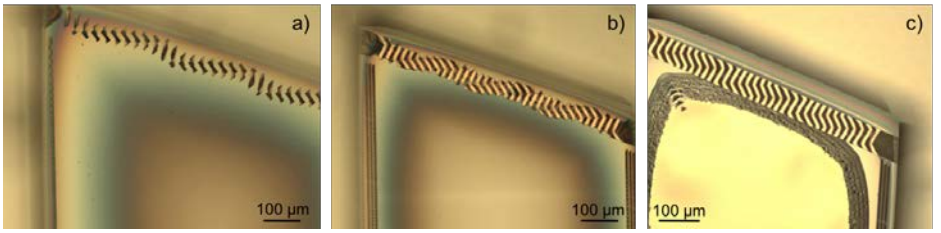

Figure 3.14: Optical images of different stages of KOH etch. a) Under-etched device, there are still Si bulk connections under the membrane. b) Properly etched device, membrane is completely released. c) Over-etched device, KOH started to etch device Si of SOI.

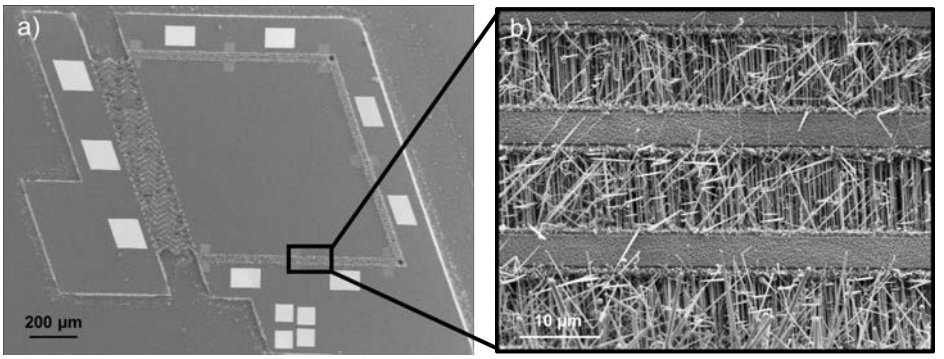

Figure 3.15: a) The final µTEG with 3 trenches (T3) after the integration of Si NWs. White areas are the contact openings to make the measurements, the rest of the device is covered by passivation b) Closer SEM image of the trench area filled with Si NWs.

keep the integrity of the suspended platform before the NW growth, supporting Si beams were introduced across the trenches between the corners of the suspended platform and the bulk Si rim. Since trenches are also defined by anisotropic KOH etch, these supporting beams are opening with a pyramidal shape due to the presence of <111> oblique planes blocking the etch. Figure 3.16a shows SEM image of one of these corners after KOH on the device with 3 trenches. After growing the NWs, these supports are cut by FIB to prevent thermal losses through the highly thermal conducting bulk Si beams (Figure 3.16b).

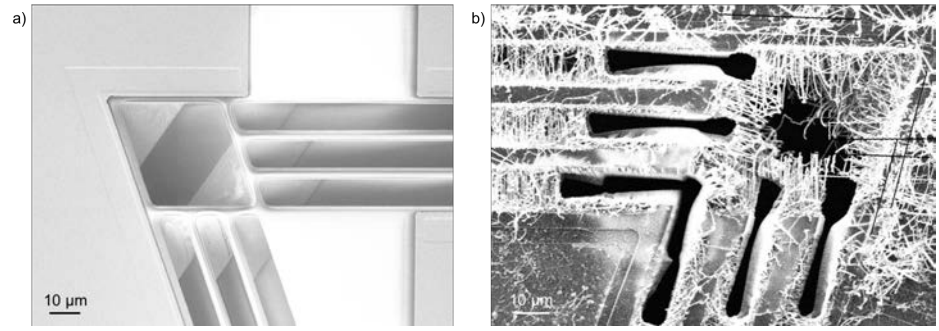

Figure 3.16: SEM images of a) supporting Si beams between the corners of suspended platform and bulk Si rim for the device with 3 trenches after opening by KOH and b) similar corner with NWs grown and Si support beams cut by FIB.

3.4 Thermoelectric microgenerator characterization

3.4.1 Thermal conductance

A set of different devices are used to evaluate the effect of device architecture on platform thermal isolation. The devices used for the thermal conductance measurements feature a built-in-heater which is isolated from the SOI device Si layer by Si_3N_4.

Platform thermal isolation is assessed by measuring the total thermal conductance between the bulk Si rim and the isolated platform. Thermal conductance is measured by forcing a controlled temperature difference by Joule heating of the platform heater. In other words, a known amount of power is dissipated on the isolated platform using the heater and the resulting temperature difference is measured simultaneously. To be able to measure the temperature difference, the heater was previously calibrated as a thermometer by measuring its temperature coefficient of resistance (TCR). TCR values of the heaters (Ti/W) were measured as explained in Section 2.3.2, and found to be 1148 $\pm$ 5 ppm/°C (Figure 3.17). In the first few measurements the temperature of the rim was confirmed to stay at room temperature by measuring a second thermometer present in that area.

First of all, microplatforms with both former bulk Si (1^{st} genera-

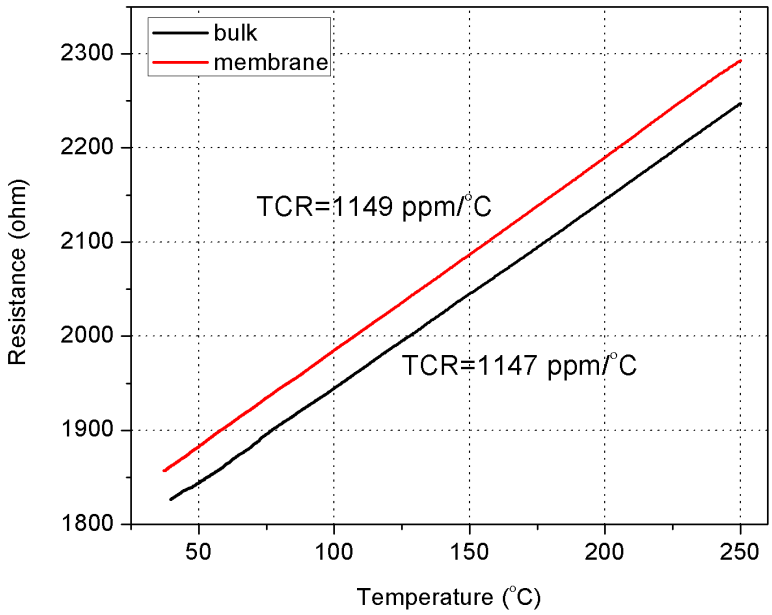

Figure 3.17: Resistance vs temperature plots of the heaters used for the thermal conductance measurements. As expected, similar values were found for both type of platform supports (bulk Si *1st generation* and membrane *2nd generation*)

tion) and new thin dielectric membrane (2^{nd} generation) supports are fabricated and measured. Both devices have a 200 µm long bridges/membranes as a mechanical support for the metal connections. They also feature a single 10 µm wide single trench (T1) between the isolated platform and surrounding bulk rim. Figure 3.18 shows the temperature reached in the isolated platform as a function of the power dissipated in the heater element. It can be clearly seen that the thermal isolation provided by the new membrane bridge outperforms that of the bulk bridge supports. Thermal conductance is decreased by 34%, from 2.01 to 1.33 mW/K, pointing out that bulk bridge conductance is an important contribution to thermal conductance in 1^{st} generation designs, limiting their performance. It should be kept in mind that in both generations, we still have additional bulk Si beams on the corners of the suspended platform to keep it leveled before the NW growth.

The influence of length of the membrane support on thermal conductance has also been studied using a set of two devices with 100 µm and 200 µm long dielectric membranes (B1, B2) with a single trench design (T1). Figure 3.19 shows the temperature reached in the isolated platform as a function of the power dissipated in the heater element. The very small change observed in total thermal conductance, from 1.34 mW/K to 1.33 mW/K by doubling the membrane length (i.e. nitride and metals contributions), confirms that the main contribution to thermal conductance in the microplatforms is linked to the extra Si bars in the corners to hold in place the platform (or to link the trenches to be filled with NWs in more than one trench devices), as anticipated in the previous measurement. Since these bars are cut by FIB after the NW growth, final µTEG will have much lower thermal conductance microplatform-wise.

As explained in the previous section, four different trench designs (T1-T4) are considered between the isolated platform and bulk Si rim to increase the effective NW length anticipating that longer NW will lead to better thermal isolation (and a higher temperature difference) due to their larger thermal resistance. The influence of the number of trenches is analyzed using four devices with the same dielectric membrane length (100 µm) but with different number of trenches. Figure 3.20 presents the temperature reached in the isolated platform with respect to the power dissipated in the heater. As anticipated, thermal

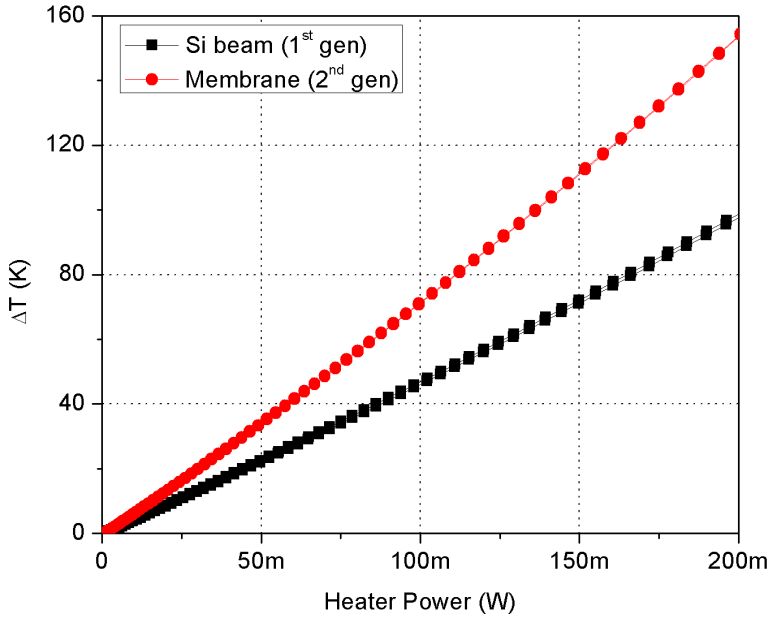

Figure 3.18: Temperature increase in the platform as a function of dissipated power for devices with bulk Si supports (1^{st} generation design) and Si_3N_4 membrane (2^{nd} generation design). Both devices have 200 µm long supports and a single trench (T1).

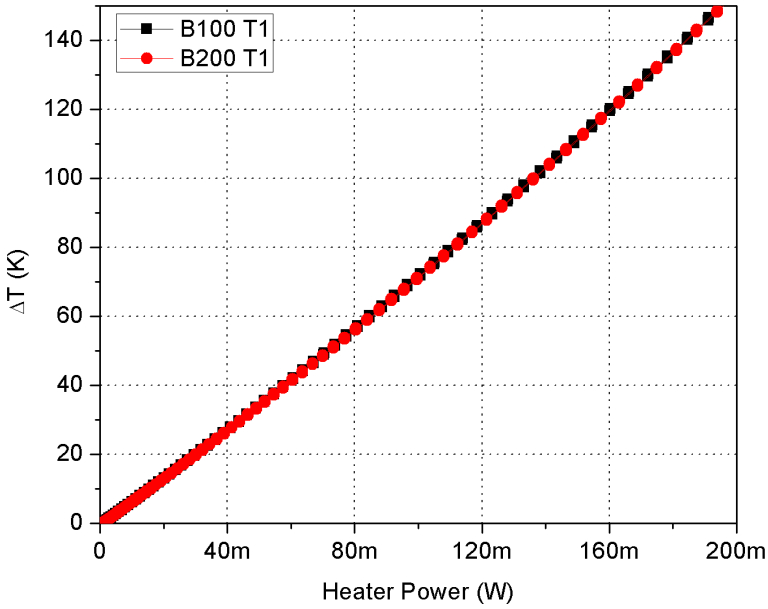

Figure 3.19: Temperature increase in the platform as a function of dissipated power for 2^{nd} generation devices with 100 µm (B1) and 200 µm (B2) long Si_3N_4 membrane and a single trench.

conductance decreases significantly when increasing the number of trenches. Thermal conductance values are 1.34 mW/K, 1.29 mW/K, 1.20 mW/K, and 0.99 mW/K for the microplatforms with the trench numbers of 1 (T1), 2 (T2), 3 (T3) and 4 (T4), respectively. It is obvious that if we increase the number of trenches, we will improve the thermal isolation. These devices had no NW. Once these trenches are filled with NWs, thermal conductance of µTEG will also depend on other parameters such as NW thermal conductivity, NW size and density etc, but the same consideration will hold: more trenches will lead to better thermal performance and a higher Seebeck voltage. In any case, it will be meaningless increasing the number of trenches beyond the point their thermal conductance is below the one of the membrane support. In addition, it is important to keep in mind that the electrical resistance of NW arrays is also expected to increase with an increasing number of trenches which will impact negatively on the power delivered by the µTEG. All these parameters should be taken into account in order to establish the optimum number of trenches.

It is important to note that these measurements are done in air ambient, therefore they are affected by heat transfer via convection and radiation. The effect of radiation is expected to be negligible considering the rather low temperature of the measurements. However, the effect of air convection is expected to be significant, therefore the platform conductance itself should be lower than the values presented here but the same trend should follow.

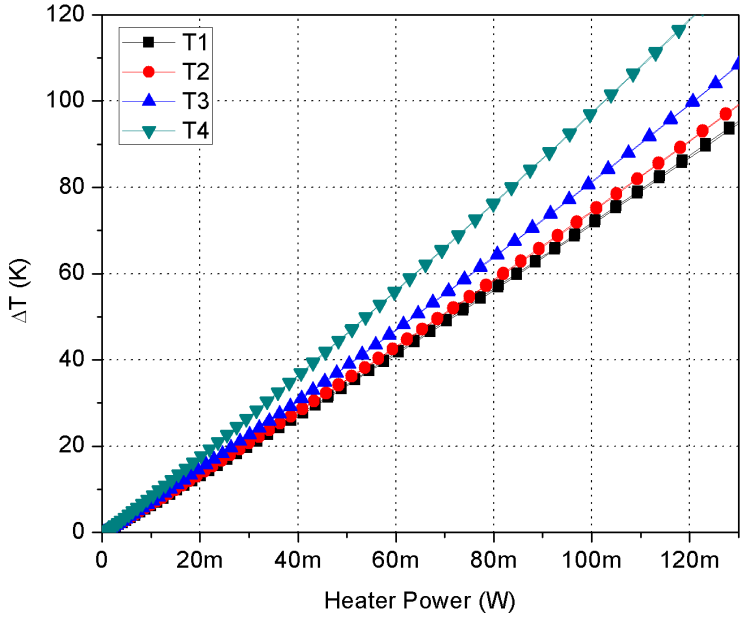

Figure 3.20: Temperature increase in the platform with respect to heat dissipated on the heater for the 2^{nd} generation devices with different trench numbers.

3.4.2 Seebeck coefficient

Seebeck coefficient measurements are performed for the different Si-based thermoelectric materials considered. Similarly to thermal conductance measurements, no other test structures than the devices themselves are used. Different ΔTs are forced actuating the heater in the platform and the Seebeck voltage measured between the internal and external collector is recorded. These measurements are repeated at various ambient/operation temperatures as explained in Section 2.3.4. In order to determine the attained ΔTs, the heater is used as thermometer. Devices used for the Seebeck coefficient measurements for NWs and TCR of the heater metal (W) are presented in Figure 3.21.

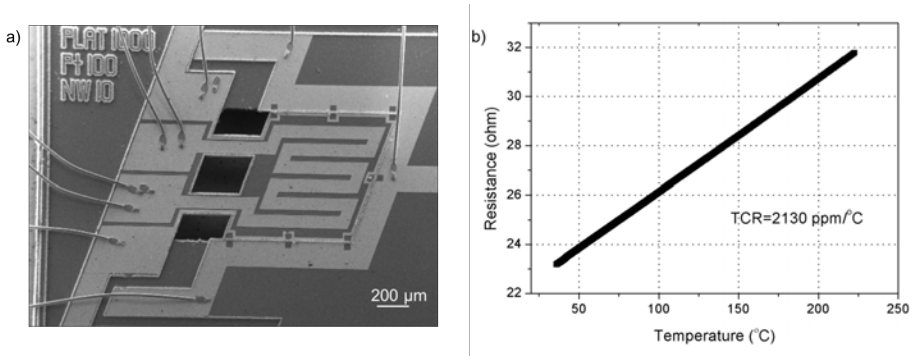

Figure 3.21: a) SEM image of the devices used for the Seebeck coefficient characterization of NWs b) Resistance vs temperature graph of the heater used for the measurements

Si NWs and microbeams

Figure 3.22 shows the measured Seebeck voltage of Si NWs with respect to the temperature difference between the hot and cold sides at different ambient temperatures. All the measured voltage vs temperature plots are linearly fitted. The slope of each line represents the Seebeck coefficient for the defined ambient temperature. As presented in Figure 3.22b, the extracted Seebeck coefficients increase with the ambient temperature (from 125 µV/K (RT) to 385 µV/K (250 °C)).

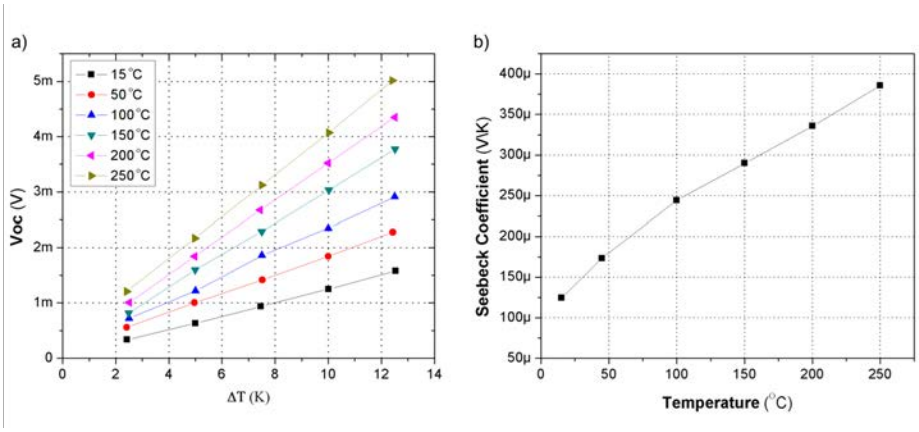

Figure 3.22: Seebeck measurements for Si NWs a) Seebeck voltages measured with respect to temperature difference between the hot and cold sides at different ambient temperatures. b) Extracted Seebeck coefficients with respect to temperature.

As explained in Section 3.2.3, devices with distributed Si microbeams are also fabricated to be able to compare micron-sized Si beams with Si NWs. For that purpose, the same measurements are performed on the devices with Si microbeams as thermoelectric material. Calibration of the heater as a temperature sensor is also done by measuring its TCR for the specific device used for the measurements. It can be seen from Figure 3.23 that Seebeck coefficient of microbeams is increasing with temperature as well. However, the increase is much smaller when compared to Si NWs (from 205 µV/K (RT) to 245 µV/K (250 °C)).

Figure 3.24 compares the Seebeck coefficient data of this thesis with the similar works in literature taking into account bulk and NW material. Considering the doping level assumed for Si NWs of this work (3-8·10^{19}cm^{-3})[83], the data obtained agrees well with the literature. For Si NWs, a larger magnitude and steeper trend of S is observed with temperature with respect to bulk Si. This may be explained by the suppression of the phonon drag effect for the low dimensional structures. It is known that the total Seebeck coefficient (S_T) results both from the intrinsic diffusion of charge carriers (S_d) from the hot to the cold side as well as a drag imposed on the carriers by the accompanying diffusion of phonons (S_{ph}). Usually at low

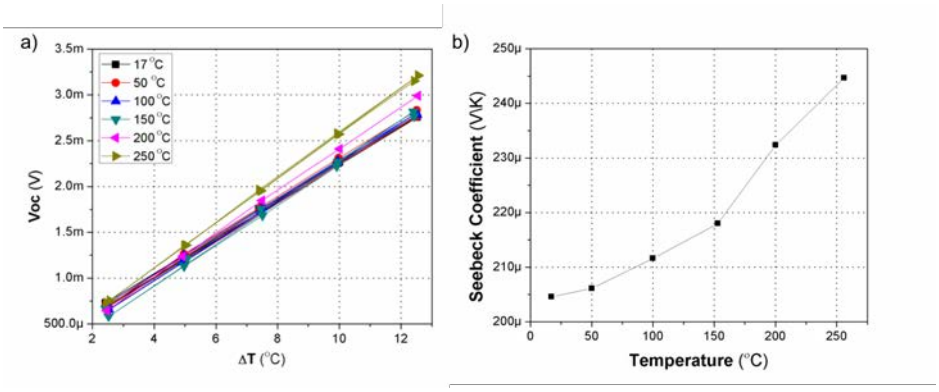

Figure 3.23: Seebeck measurements for Si microbeams a) Seebeck voltages measured with respect to temperature difference between the hot and cold sides at different ambient temperatures. b) Extracted Seebeck coefficients with respect to temperature.

temperatures S_{ph} is considered to be low and sometimes neglected. For bulk materials, electrical conductivity decreases with increased temperature which results in increased S_d. However, phonon drag at high temperatures increases the electrical conductivity and hence balances the total Seebeck coefficient (S_T). This is the reason why more or less constant S_T is observed for the bulk materials. In low dimensional structures such as NWs, on the other hand, due to the scattering of phonons from the surfaces, phonon drag is suppressed and cannot affect the S_T significantly. Studies reporting this effect imply that the phonon drag suppression has the same underlying mechanism than reduced thermal conductivity in NWs. Thus, in the NWs with diameters lower than 100 nm, strong surface scattering suppresses S_{ph}, so that a sharp increase of Seebeck coefficient is observed which is actually the S_d component of the Seebeck coefficient. According to Krali et al. [92], this effect is much more enhanced for highly doped NWs. Detailed analysis and discussion on the phonon-drag suppression in Si NWs is beyond the scope of this thesis and can be found in Refs [93], [94].

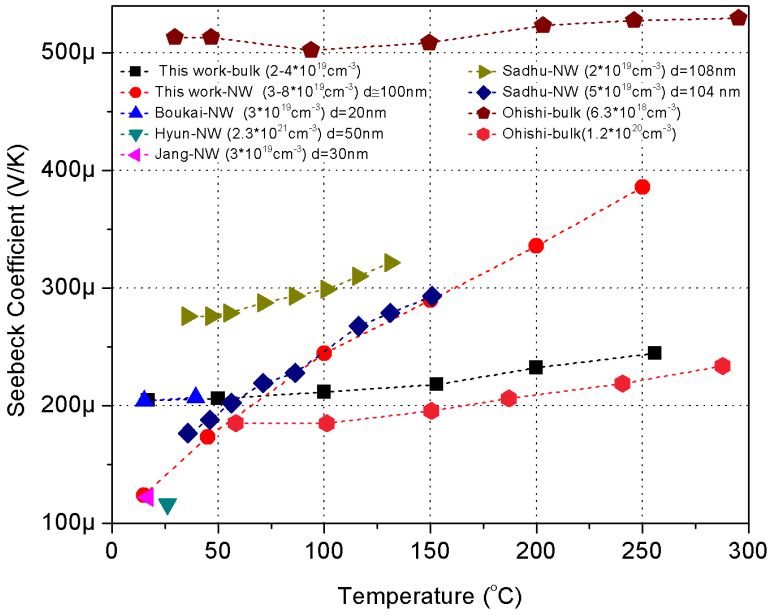

Figure 3.24: Comparison of this work results with the literature [44], [36], [95], [79], [96], [93], showing agreement on the Seebeck coefficient evolution with temperature for bulk and NW material.

SiGe NWs

Figure 3.25a shows the variation of the Seebeck coefficient of SiGe NWs as a function of temperature together with the similar data from the literature. A similar trend of rapidly increasing Seebeck coefficient is observed with Si NWs with slightly lower Seebeck coefficient values than for Si NWs, from 90 to 235 µV/K. It is worth mentioning that for SiGe, the increase of Seebeck coefficient with temperature is not specific of NWs as in the Si case. In SiGe mixed crystals, the phonon mean free paths are already so short that the phonon drag component of the Seebeck coefficient is negligible and only the electronic part remains [97].

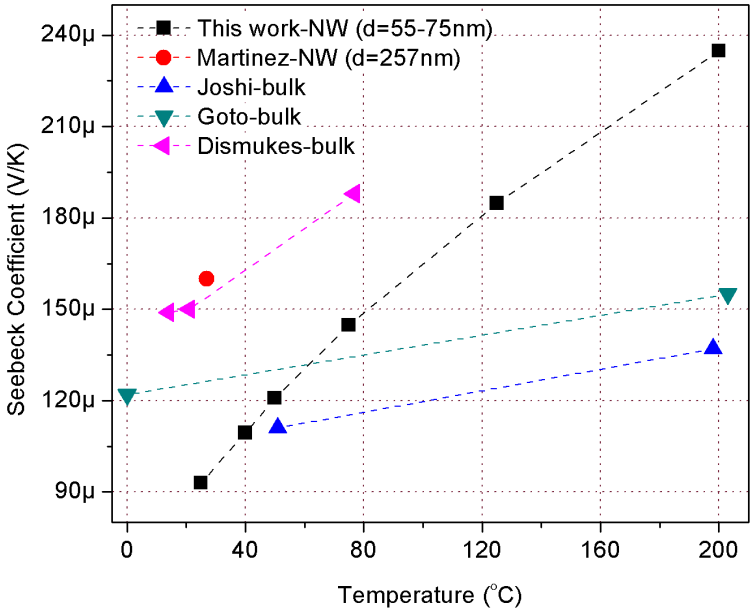

Figure 3.25: Comparison of SiGe NW Seebeck coefficient values obtained in this work with the literature [98]–[101].

3.4.3 Thermoelectric power

In order to characterize the microgenerators performance as energy harvesters, I-V (and power) measurements are made on packaged chips placed on top of a thermal chuck using a silver paste to enhance the thermal contact between both surfaces. While the bottom part of the device is at a high temperature, the top of the device is cooled by natural convection. Measurements are conducted in a 2-wire configuration to mimic the performance in a real application scenario.

Si NWs are grown on both 1^{st} and 2^{nd} generation microplatforms to be able to compare and emphasize the power output obtained in 2^{nd} generation devices. SiGe NWs, on the other hand, are only grown on 2^{nd} generation microplatforms to be able to compare with Si NWs.

Si NWs-based µTEGs

First, the improvement attained in the power output resulting from the optimizations discussed in the previous sections is evidenced by comparing the initial (1^{st} generation) design with the optimized (2^{nd} generation) design. Figure 3.26 compares the power curves obtained from Si NW-based µTEG with both generations of designs under natural convection conditions and hot plate temperatures up to 300 °C with 50 °C steps. Both devices have three trenches (T3), and same conditions are applied to both devices for Si NW growth. Even though the 1^{st} generation interdigitated platform structure (Figure 3.26a, top), which has more perimeter filled with Si NWs, is replaced by a square platform, higher power densities are achieved in the 2^{nd} generation platform. Power increased from 500 pW to 13 nW in the 2^{nd} generation µTEG, which is attributed to replacing narrow bulk Si bridges by the thin dielectric membrane and to decreasing the electrical resistance by proper doping/annealing steps and metal layout redesign taking advantage of the wider membrane support.

Table 3.2 compares the Seebeck voltages, device internal resistances and power densities of both generation µTEGs with single and three trench devices at a hot plate temperature of 200 °C. Power densities are calculated assuming a single device area of 2 mm^2. Temperature differences between the hot and cold ends of the device (ΔTs) are extracted using the measured Seebeck coefficient values

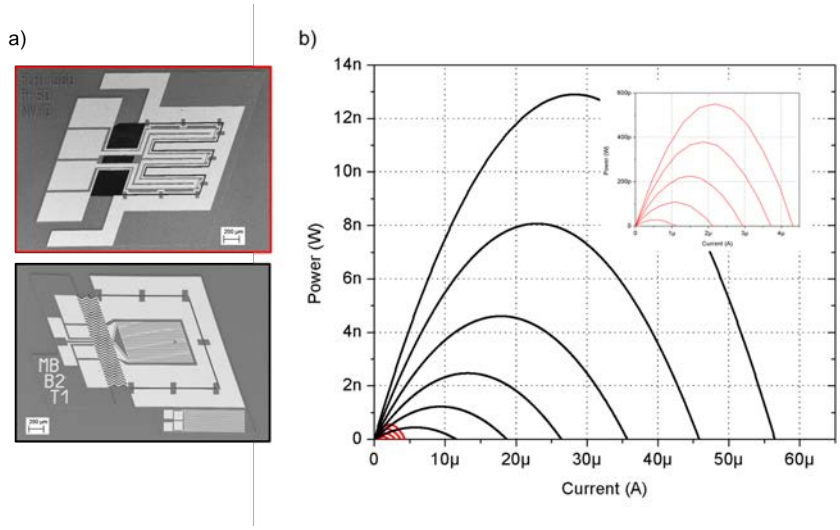

Figure 3.26: a) SEM images of the devices with bulk Si support (1^{st} generation, top), and thin dielectric membrane support (2^{nd} generation, bottom). b) Power curves obtained at different hot plate temperatures (50 to 300 ^{o}C in 50 ^{o}C steps) for two packaged devices with three trenches filled by Si NWs: 2^{nd} generation (black) and 1^{st} generation (red, detailed in the inset).

Table 3.2: Comparison of the 1^{st} generation and 2^{nd} generation Si NWs-based µTEGs in terms of their Seebeck voltages, device internal resistances and power densities at hot plate temperature of 200 °C for a 2 mm^2 device. Devices with single (T1) and three (T3) trenches are presented.

	T1 1^{st} gen	T1 2^{nd} gen	T3 1^{st} gen	T3 2^{nd} gen
V_{oc} (mV)	0.29	0.36	0.30	0.52
ΔT(K)	0.86	1.07	0.9	1.54
R_{device} (Ω)	89.5	5.1	102.3	15.1
Max. Power Density (nW/cm^2)	11	335	11.2	230

explained in the previous section (See Figure 3.25). Replacing the bulk Si beam bridge with a thin dielectric membrane resulted in 25% to 75% increase in the Seebeck voltage for the 2^{nd} generation µTEG. Electrical optimizations of the platform (mainly metal/Si contact resistance) significantly decreased the device internal resistance in the 2^{nd} generation devices (7-20 times less device resistance compared to initial design). As a result of thermal and electrical improvements of the microplatform, a tremendous improvement of 25-35 times power output is obtained from the proposed µTEG.

Next, the effect of the number of trenches on Seebeck voltage and thermoelectric power is studied. Voltage curves of the Si NW-based 2^{nd} generation µTEG with respect to hot plate temperature is given in Figure 3.27. As expected, the obtained voltage increases with increasing trench number, ie. effective Si NW length. A maximum Seebeck voltage of 1.12 mV is obtained from the device with 4 trenches at a hot plate temperature of 300 °C.

Obtained power values from the same devices do not follow the same trend than Seebeck voltages (Figure 3.28). Since $P_{max} = V^2/4R$ for a load resistance matched device, internal electric resistance of the device also plays an important role on the final power output. As can be seen from Figure 3.28, the increase of the device resistance for the four devices is aligned but not linearly dependent on the effective length of the NWs ensemble (i.e. number of trenches). Factors contributing to this non-linearity might be inhomogeneity in overall NW

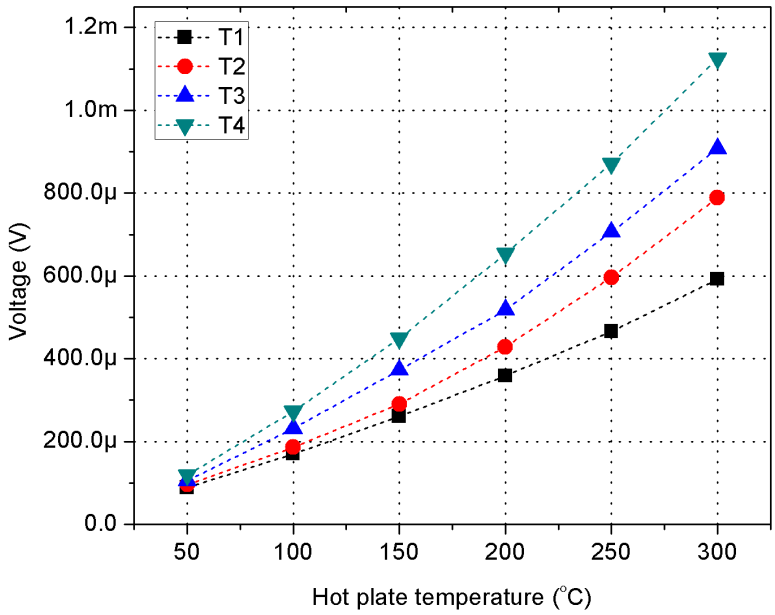

Figure 3.27: Seebeck voltages measured from Si NWs based µTEGs with different trench numbers while heating the base of the device.

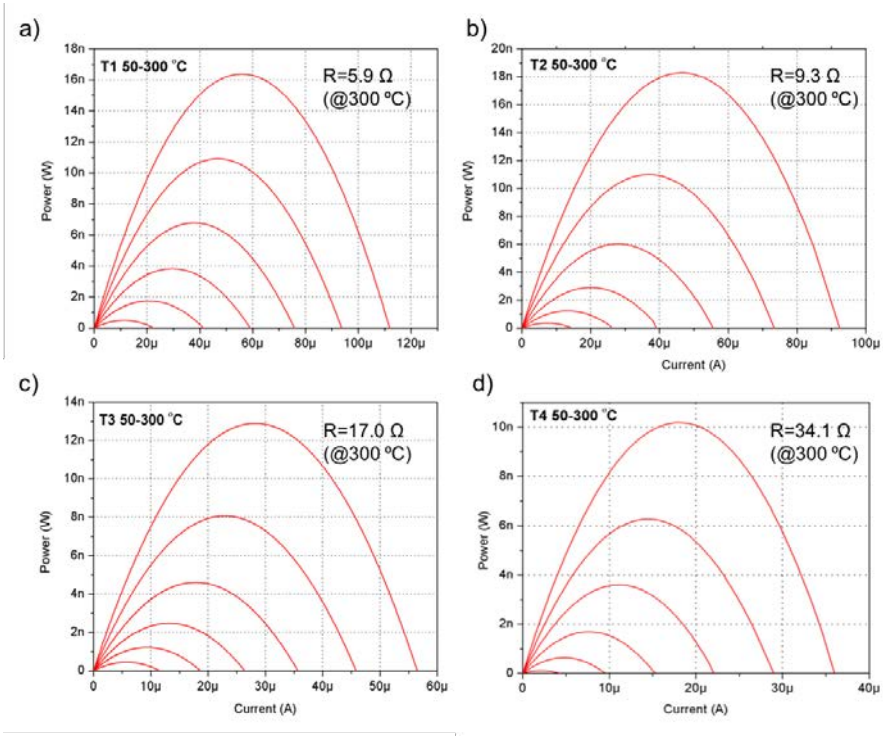

Figure 3.28: Thermoelectric power curves measured for 2^{nd} generation devices of T1 (a), T2 (b), T3 (c) and T4 (d) at different temperatures (50 to 300 °C with 50 °C steps). Device resistances are also included for each device at hot plate temperature of 300 °C.

density and NW geometrical distribution, which depends on the galvanic displacement step of the growth. Obtained maximum power outputs are 16.3 nW, 18.3 nW, 12.8 nW and 10.1 nW for the devices with 1,2, 3 and 4 trenches when the hot plate temperature is 300 °C.

SiGe NWs-based µTEGs

Regarding the performance of µTEGs with SiGe NW arrays, a significant increase of the Seebeck voltage is observed due to the lower thermal conductivity of SiGe NWs with respect to Si NWs. Considering the Ge composition of 20% - 30% in this thesis, thermal conductivity of the SiGe NWs should be less than 15 W/mK [102]. Thermal conductivity of the Si NWs presented in this thesis, on the other hand, was found to be in the range of 25-33 W/mK [83]. More-

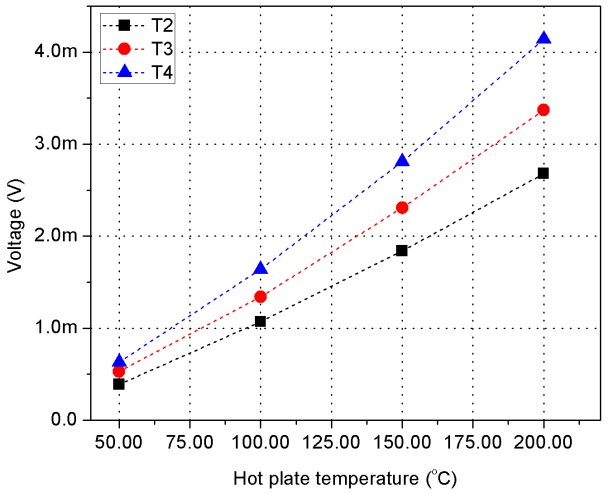

Figure 3.29: Seebeck voltages obtained from SiGe NWs based µTEGs with respect to hot plate temperature.

over, the diameter of SiGe NWs (55-75 nm) is lower than that of Si NWs (80-140 nm) in this work (as shown in Table 2.1 of Chapter 2), which eventually indicates lower thermal conductance of the platform with SiGe NWs.

Seebeck voltages obtained from SiGe NWs-based µTEGs are shown in Figure 3.29. A maximum Seebeck voltage of 4.14 mV is obtained from the device with four trenches at hot plate temperature of 200 °C. However, as can be seen from Figure 3.30, the maximum power is attained from the device with three trenches (145 nW) due to the lower internal resistance of that specific device with respect to others. Since all the components of device internal resistance are the same but the NW resistance, the non-linearity is again attributed to variations in NW distribution. Table 3.3 summarizes the harvesting parameters for SiGe NWs based µTEGs. A maximum ΔT of 17.6 K is obtained from the device with four trenches, which is the one exhibiting higher Seebeck voltage, when the hot plate temperature is set to 200 °C.

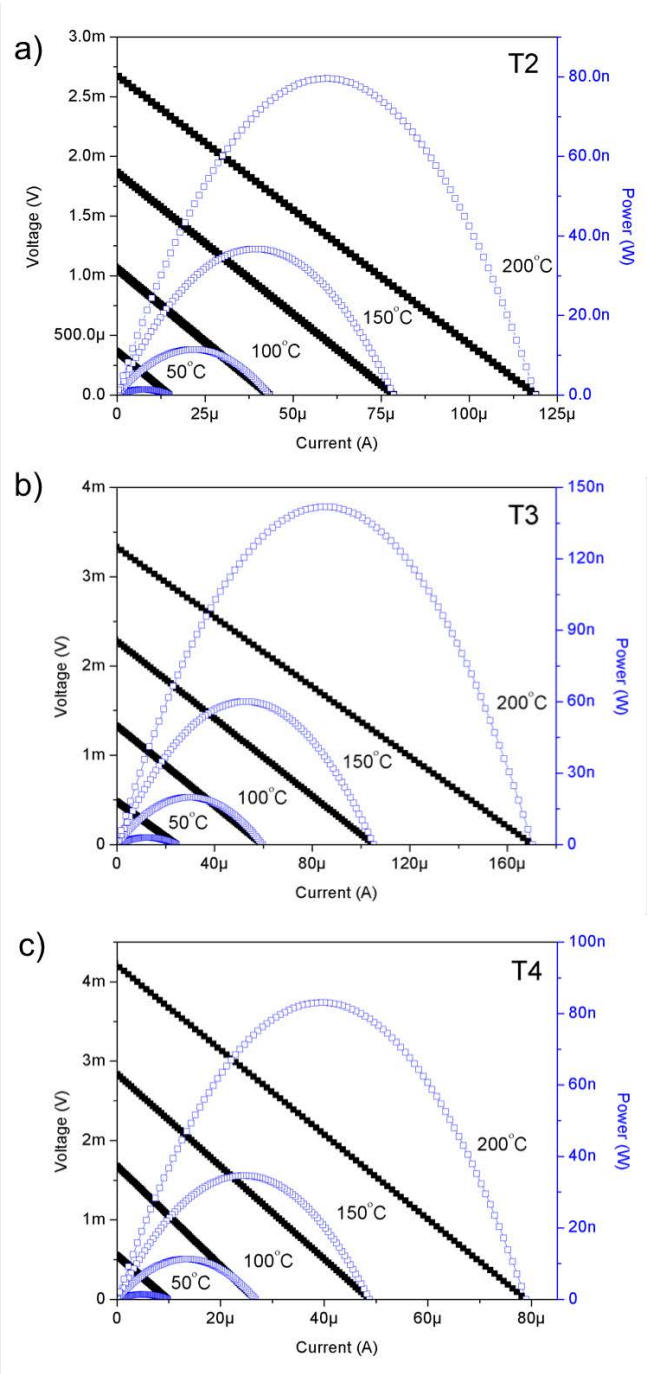

Figure 3.30: I-V and power curves obtained from SiGe NWs based µTEGs at different substrate temperatures (50 to 200 °C in 50 °C steps).

Table 3.3: Harvesting parameters of SiGe NWs-based µTEG with different trench numbers when hot plate temperature is at 200 °C for a 2 mm^2 device.

	T2	T3	T4
V_{oc} (mV)	2.7	3.4	4.2
$\Delta T(K)$	11.5	14.3	17.6
R_{device} (Ω)	22.5	19.5	53.3
Max. Power Density ($\mu W/cm^2$)	4.0	7.1	4.1

3.5 Discussion & summary

In this work, µTEGs that were first presented by D. Davila [78] (mentioned as 1^{st} generation in this work) have been redesigned (mentioned as 2^{nd} generation) to improve the resulting power densities. Two main approaches have been followed during the optimization of the microplatform:

- The thermal performance of the µTEG is enhanced by improving the temperature difference attainable between the two separated Si regions (one of them a suspended platform), which are designed to be the hot and cold ends of the µTEG. In the 1^{st} generation design, bulk Si supports were linking these isolated Si regions to provide a mechanical support for the electrical connections to the suspended platform. However, this was limiting the device performance due to their high parasitic thermal conductance. In this work, the bulk Si supports have been replaced with low thermal conductivity open membranes (Si_3N_4) by introducing the specific design and microfabrication processing amendments. With this new arrangement, the hot and cold Si parts are thermally linked mostly through the thermocouple active materials, i.e. NWs and metals, decreasing any parasitic thermal losses.

- The electrical performance of the µTEG is enhanced by decreasing the device internal resistance. The microplatform has

been redesigned to have lower metal resistances on the collectors, and additional process steps are employed to minimize the metal/Si contact resistance. Different metal layers have been tested together with a proper combination of additional doping of the Si substrate and annealing the metal/Si layer to achieve a low resistance ohmic contact.

Figure 3.31 compares the maximum power densities obtained from the 1^{st} generation µTEGs with Si NWs (T3 beam Si), 2^{nd} generation with Si NWs (T3 membrane Si), and 2^{nd} generation with SiGe NWs (T3 membrane SiGe). All devices have three trenches that are filled with NWs (i.e. NW effective length is 30 µm.). It can be clearly concluded that 2^{nd} generation SiGe NWs-based µTEGs yielded much higher power densities compared to the ones with Si NWs due to their low thermal conductivity which allows attaining higher temperature differences between the cold and hot ends of the µTEG. Even though the power densities attained from Si NWs- based µTEGs with both generations look similar at that plot scale, more than 20 times improvement is obtained by 2^{nd} generation µTEG just by optimizing the microplatform design.

Figure 3.32 helps to explain the mechanism beyond the improved power densities and shows the room left for improvement. Figure 3.32a presents the ΔT obtained between the hot and cold ends of the µTEG with respect to hot plate temperature in which the difference arises only from the *thermal contributions*. The only difference between the 1^{st} and 2^{nd} generation µTEGs with Si NWs is originated by the replacement of the bulk Si beam supports by low thermal conductivity dielectric membrane. Therefore, the main contribution which leads to the difference in power density between the generations is the thermal resistance of the platform. Comparing the 2^{nd} generation µTEGs with Si and SiGe NWs, higher ΔTs obtained for the latter are due to the much lower thermal conductivity of SiGe NWs.

Variations of maximum power densities with respect to the attained Seebeck voltage between the two ends of the microplatform is presented in Figure 3.32b. The highest power density is obtained from the Si NWs-based 2^{nd} generation µTEG when the same Seebeck voltage is considered for all three cases. To be able to attain higher power densities from the same Seebeck voltage, the internal

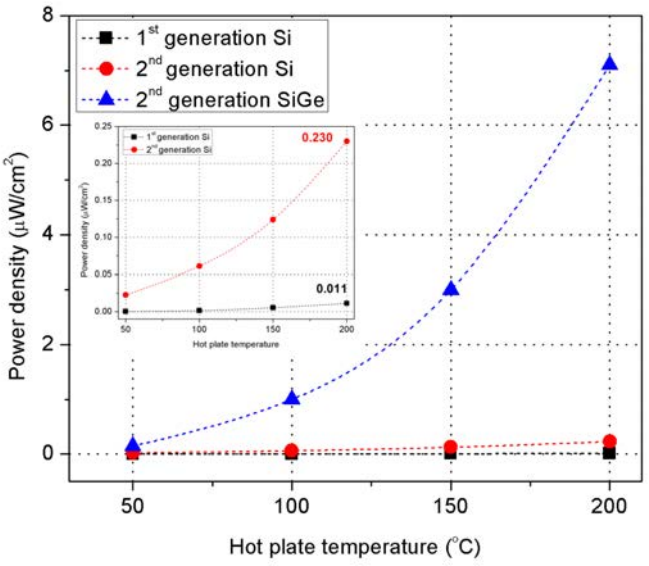

Figure 3.31: Comparison of power densities of different µTEGs (1^{st} generation with Si NWs, 2^{nd} generation with Si NWs, and 2^{nd} generation with SiGe NWs) with respect to hot plate temperature. All devices comprise three trenches (T3) that are filled with NWs.

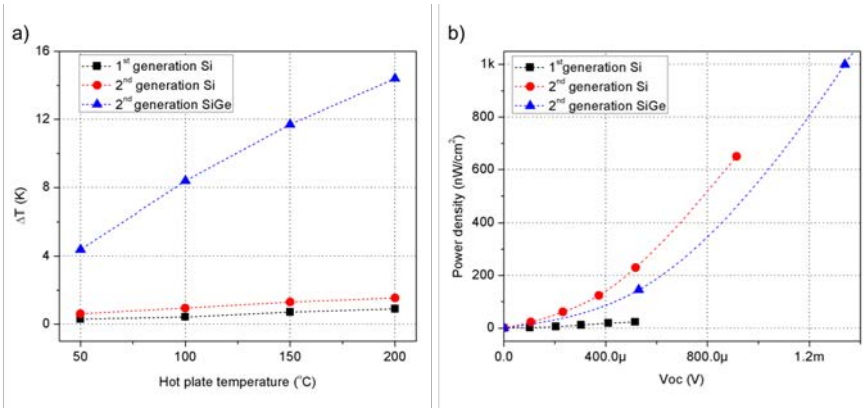

Figure 3.32: a) Temperature differences attained by Si and SiGe NWs based µTEGs with respect to hot plate temperature. ΔTs are calculated by V_{oc} and Seebeck coefficient measurements. b) Power density vs Seebeck voltage curves for different µTEGs.

resistance should be lower. When the same Si NWs are grown on both generation of devices (same Seebeck coefficient), higher power densities are obtained from the 2^{nd} generation devices due to its decreased internal resistance. Comparing 2^{nd} generation devices with Si and SiGe NWs, higher power densities are obtained from Si NWs-based µTEG for the same Seebeck voltage since Si NWs have lower electrical resistance.

Figure 3.33 shows the variations of maximum power densities with respect to the attained ΔT between the two ends of the microplatform. In this graph, the difference between the power densities for the same ΔTs arise from the *electrical contributions* (Seebeck coefficient and electrical resistance). Comparing the µTEGs with Si NWs, a significant increase of the power densities is observed for the 2^{nd} generation µTEG. This is due to the substantial decrease of the device internal resistance presented in this Chapter. However, the power densities obtained for a given attained ΔT are far lower for the SiGe NWs based µTEGs when compared to Si NWs based µTEGs. This is due to much lower Seebeck coefficient and to the higher resistance of SiGe NWs arrays. Within the framework of the collaboration with IREC, efforts to decrease the SiGe NW arrays resistance by further doping during the growth are underway. This will further increase the performance of SiGe NWs as far as the extra

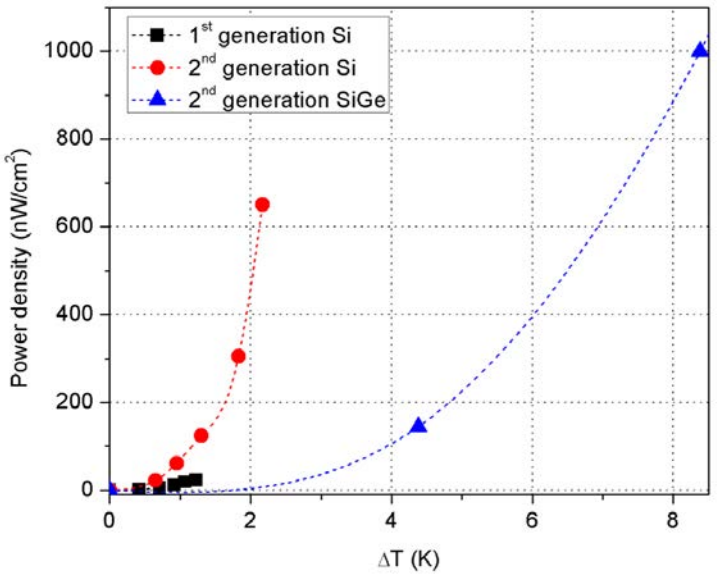

Figure 3.33: Variation of power density with respect to ΔT attained in different µTEGs.

doping do not affect negatively their Seebeck coefficient. The harvesting parameters of these three devices are also listed in table 3.4 to be able to differentiate them more clearly. Considering the main focus of this thesis, optimizing the thermoelectric microplatform, a tremendous improvement can be observed just by comparing 1^{st} and 2^{nd} generation designs with Si NWs.

It is shown that SiGe NWs based µTEGs can harvest 7.1 µW/cm^2 when there is a waste heat source available with a temperature of 200 °C. Since the required power density for many sensing applications is in the range of 10-100 µW/cm^2, we are close to meet expectations. However, ways to further improve the power density have been studied and will be presented in the following chapter (especially for Si NWs-based µTEGs). Certainly, what needs to be improved is the attainable ΔT. The thermal resistance to the ambient of a bare small surface is so high that under natural convection our device is only capturing a minimum fraction of the total temperature difference be-

Table 3.4: Harvesting parameters for different µTEGs with three trenches when the hot plate temperature is 200 °C for a 2 mm^2 device.

	Si NW 1^{st} gen	Si NW 2^{nd} gen	SiGe NW 2^{nd} gen
R_{device} (Ω)	117.6	15.06	19.5
V_{oc} (mV)	0.31	0.52	3.37
$\Delta T(K)$	0.92	1.54	14.4
Max. Power Density (nW/cm^2)	11.2	230	7100

tween the heat source and the ambient.

Chapter 4

Integration of a heat exchanger on a µTEG

4.1 Overview

Most of the studies reporting thermoelectric microgenerators (µTEGs) measure their performance by applying a temperature difference (ΔT) to the system by means of actively dissipating a power on it or artificially applying a fixed temperature on both ends of the device. In a real application case, such as the harvesting the energy from a waste heat source, an internal ΔT is stablished in the µTEG under given operation ambient conditions. To achieve a high ΔT across the thermoelectric materials (i.e. to maximize the power output), optimizing the heat sink and heat source of the generator is necessary. Particularly for µTEGs, it is difficult to create reasonable ΔTs due to the small size of the device (smaller thermal resistances), and therefore the integration of a heat exchanger is crucial for the thermal management of the system. Integration of a heat exchanger on top of a micron-sized device is also challenging especially for planar µTEGs, which mostly include a fragile suspended platform.

In this thesis, different routes have been designed for the integration of a heat exchanger onto our all-Si planar µTEG to maximize the power output. Some researchers have conducted measurements/simulations of vertical µTEGs including a heat spreader or a heat sink [49]–[51]. Yuan et al.[103], recently reported on a high thermal resistance planar µTEG using the Si substrate as heat con-

centrator and evacuator on both hot and cold ends of the device. Yang et al.[104] presented the measurements for a planar µTEG in which the bulk Si substrate is cooled by a heat sink and a fan. In that work, the suspended platform is heated by a heat source from a distance to prevent breaking it. Researchers from Singapore coated a heat-sink layer on the cold side of the planar µTEG to effectively disperse heat from the cold side of the device to ambient air [105]. To the best of our knowledge, the work of this thesis is the first attempt to define the routes for the heat exchanger integration on a planar µTEG using commercial heat sinks and considering both possible direction for the heat flow. Performance of the all-Si based µTEG is reported under operational conditions both with and without the heat exchanger.

Next section presents the preliminary experimental studies on increasing the heat dissipation to the ambient by applying a forced convection or a cold-finger approach. Next, the routes for the integration of a heat exchanger on the proposed µTEG are detailed together with the components used for the integration. Simulations of the temperature distribution across the assembly as well as the power outputs are conducted to compare the performances of two approaches. Finally, thermoelectric power measurements are carried out on µTEGs with and without heat exchanger.

4.2 Preliminary studies

Before starting to design the routes and components for the integration of a heat exchanger, preliminary experimental studies are conducted to examine its possible effect on the device performance. For that purpose, the suspended platform of the presented µTEG, considered as the cold side, is tentatively further cooled down by the application of forced convection or a soft physical contact with high thermally conducting material element (i.e. cold-finger approach).

4.2.1 Forced convection

Convection is a mechanism of heat transfer originated from the physical movement of a surrounding fluid (usually water or air). Depending on how the movement of fluid is initiated, convection can

be classified as natural or forced convection. In natural convection, the fluid closer to heat source warms up and rises, giving its place to colder fluid. In forced convection, the fluid is forced to move in the direction determined by external forces such as a pump or a fan.

The positive attribute of forced convection compared to natural convection is the increased amount of heat transfer. The overall heat transfer is usually expressed as:

$$Q = UA(T_1 - T_2) \tag{4.1}$$

where Q is the overall heat transfer rate, U is the overall heat transfer coefficient, A is the exposed surface area, and $(T_1 - T_2)$ is the temperature difference between the solid surface and surrounding fluid. It can be seen from this equation that the heat transfer rate is directly proportional to the heat transfer coefficient. If we assume the surface and temperature difference to be constant, the greater the heat transfer coefficient, the greater the heat transfer rate. The heat transfer coefficient depends on the type of fluid, its flow properties such as velocity and viscosity, and other flow and temperature dependent properties. In a forced convection scenario, the heat transfer coefficient and hence the total heat transfer rate is higher since the velocity of the surrounding air is increased by a fan or a pump. However, unless the movement of the fluid is provided by the application scenario itself, a force convection situation requires additional parts and energy to operate those parts, so it is hardly feasible to include it for the proposed generator approach. In this section, forced convection on the devices is tested only for mimicking the positive effect of the presence of a heat transfer promoter, such as a heat exchanger.

For the forced convection studies, a silicone tube with approximately 4 mm in diameter is positioned vertically 5 cm above the device, pointing downwards, and a pressure of 0.2 bar is applied to let the air flow. In such a case the heat exchange between the suspended platform and the ambient is enhanced, and therefore lower platform temperatures are expected, which leads to larger thermal differences across the NWs.

The temperatures of the bulk Si rim and the suspended microplatform under natural and forced convection are shown in Figure 4.1. These temperatures are measured by calibrating the thermometer on

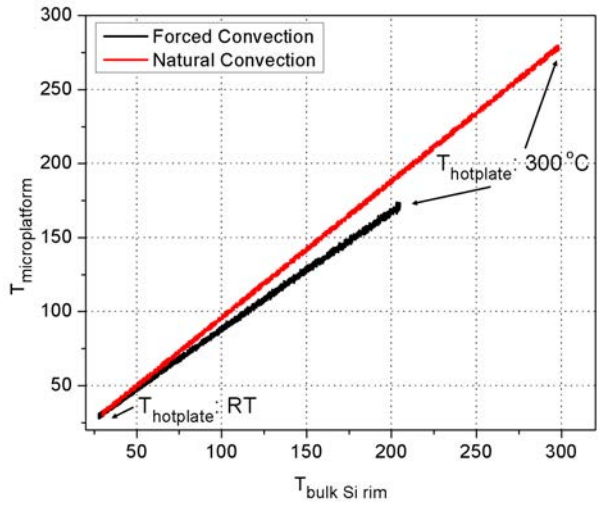

Figure 4.1: Temperatures of the bulk Si rim and the suspended microplatform under natural and forced convection at a hot plate temperature of 300 °C. Under forced convection both microplatform and rim get colder but the resulting ΔT is larger than under natural convection.

the bulk Si and the heater on the suspended microplatform, respectively. As can be seen from the figure, even though the hot plate temperature is at 300 °C, the maximum temperatures attained on the device are around 200 °C when the forced convection is applied. This study is conducted on T1 test structures using Si microbeams as thermoelectric material. It is important to note that the ΔTs observed would not be strictly the temperature differences across the NWs: they correspond to the differences between the average temperatures of the heater and the thermometer on the suspended and bulk Si parts, and such averages cover an area larger then the one in close proximity to NWs.

The effect of the forced convection on Seebeck voltages of the Si NW-based µTEGs is shown in Figure 4.2. Since the heat transfer is higher in the forced convection mode, the temperature differences experimented by the NWs are higher. This ends up in a Seebeck voltage increment of 2 to 9 times, with the higher impact on the devices with higher number of trenches. The same trend is observed

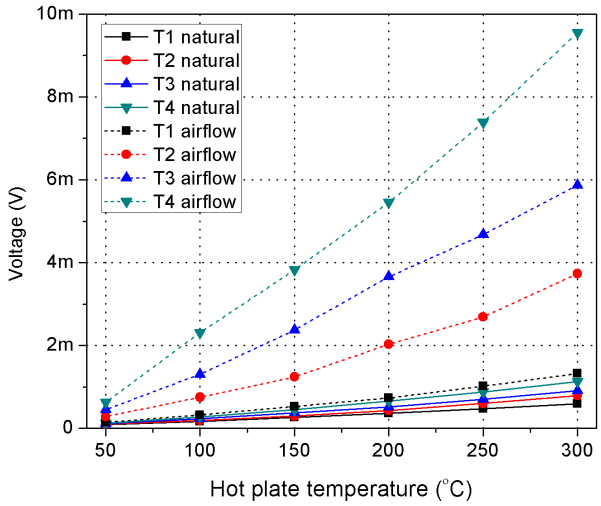

Figure 4.2: Seebeck voltages obtained from Si NWs based µTEG with respect to hot plate temperature under natural or forced convection conditions.

for the power outputs (Figure 4.3). A maximum power output of 690 nW is observed from the device with 4 trenches when the hot plate temperature is 300 °C. Since the forced convection is applied with a tube of 4 mm diameter in the direction of the suspended platform, it is more possible to cool it down effectively when there is a larger distance between the suspended platform and bulk Si rim. Table 4.1 compares the harvesting parameters of the same µTEG under natural or forced convection ambients. The same effective device area is used for the devices with different number of trenches to calculate the power densities.

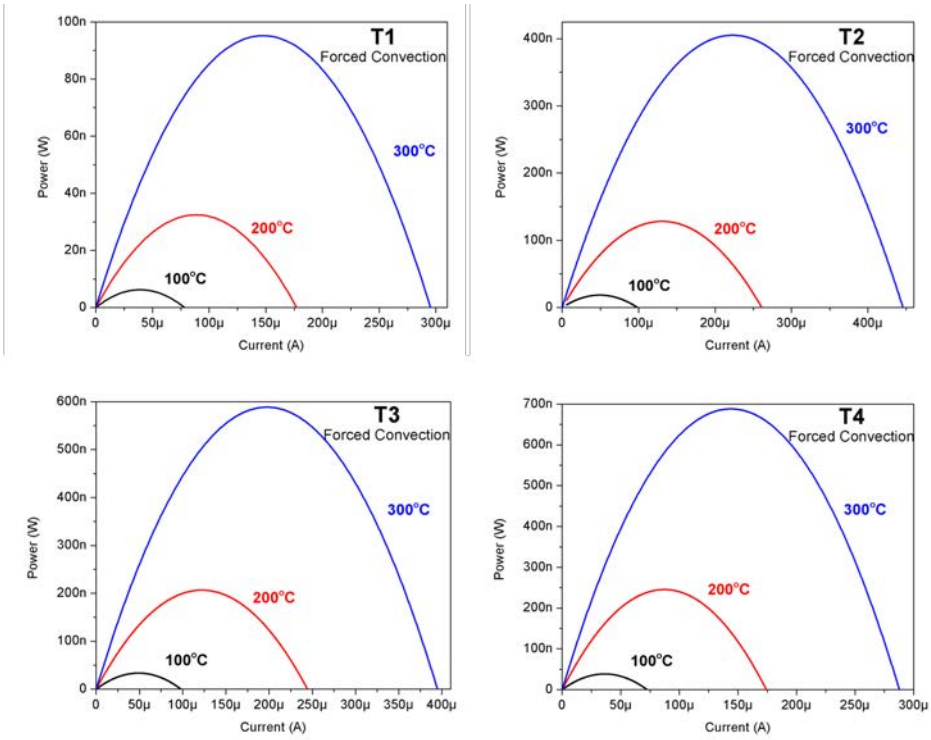

Figure 4.3: Power curves obtained from Si NWs based µTEG under forced convection with respect to hot plate temperatures of 100 °C, 200 °C and 300 °C. Devices with different number of trenches are presented (T1-T4)

Table 4.1: Performance comparison of the µTEGs with different number of trenches filled with Si NWs under natural and forced convection ambient. Measurements are conducted when the hot plate temperature is at 300 °C. Power densities are calculated for a device area of 2 mm^2.

	Natural convection			**Forced convection**		
Device	Voc (mV)	Power density ($\mu W/cm^2$)	Resistance (Ω)	Voc (mV)	Power density ($\mu W/cm^2$)	Resistance (Ω)
T1	0.6	0.82	5.9	1.32	4.75	4.6
T2	0.79	0.92	9.3	3.74	20.3	8.7
T3	0.91	0.64	17.0	5.87	29.4	14.3
T4	1.12	0.51	34.1	9.55	34.4	33.1

4.2.2 Cold-finger approach

In order to demonstrate the positive effect that a heat exchanger may have once implemented in the µTEG, another experimental approach called cold-finger is studied. In this set of experiments, a metallic probe dipped in thermal paste is placed on top of the thermally isolated microplatform with the help of a micromanipulator to reduce the thermal resistance from such platform to ambient. This approach is studied on the devices with (more robust) Si microbeams as thermoelectric active material.

The optical microscopy image of the device just after removing the probe from the suspended microplatform can be seen in Figure 4.4a. The probe was dipped in electrically insulating thermally conducting paste before contacting the center of the platform. Figure 4.4b shows the voltage change when a cold-finger is applied. Voltage increases rapidly after touching the platform with the probe. If we increase the force slightly, voltage continues to increase since it reduces the conductive thermal path and hence the thermal resistance. After removing the probe, previous voltage values are recovered.

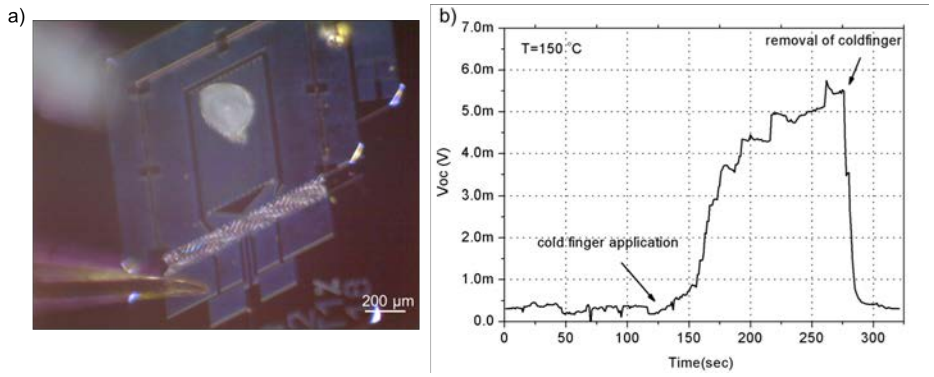

Figure 4.4: a) Optical microscopy image of the device just after the removal of the cold-finger. A drop of remaining thermal paste can be seen on top of the suspended (thermally isolated) microplatform of the device. b) Seebeck voltage change when the cold-finger is applied on the microplatform. Measurement is done using the Si microbeams based µTEG (area occupation=6.2 %) when the hot plate temperature is kept at 150 °C. The voltage evolution from probe application to removal is due to the exertion of an increasing force with the help of the micromanipulator.

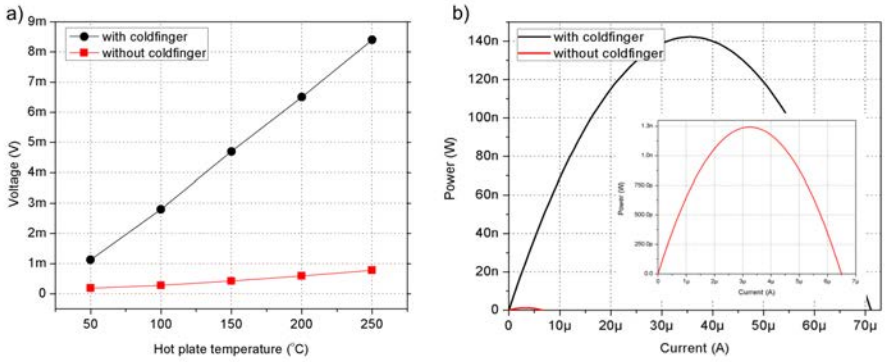

Figure 4.5: a) Seebeck voltages vs hot plate temperature curves obtained from the same Si microbeams device (area occupation= 6.2%) with and without cold-finger. b) Power curves obtained at a hot plate temperature of 250 ^{o}C for the same Si microbeams device with (black) and without (red, detailed in the inset) cold-finger placed on top of the suspended microplatform.

Figure 4.5 displays the increase in the generated Seebeck voltage and thermoelectric power when there is a contact with the cold-finger. In terms of Seebeck voltage, 6 to 12 times improvement is observed with the cold-finger depending on hot plate temperature, the higher the hot plate temperature, the larger the improvement. For a given hot plate temperature the cold-finger approach produces better results than forced convection, since a solid probe removes heat more effectively from the microplatform, and does it locally, without affecting the Si rim temperature. Power curves are also compared for the same device with and without cold-finger, and found to be two orders of magnitude larger (1.3 nW vs. 142 nW @ 250 °C, corresponding to a power density of 7.1 µW/cm^2), which makes sense since the power is directly proportional to the square of Seebeck voltage. It also proves that the electrical resistance of the devices remained unchanged during the measurements. It is important to note that cold finger studies are conducted on the devices with Si beams filling the trenches instead of NWs. Larger powers can be generated from the µTEGs based on NWs due to enhanced thermoelectric properties.

4.3 Routes for the integration of a heat exchanger

After observing a significant amount of increase in the power generated by applying a forced convection or a cold finger, our efforts have been focused on defining the routes for the integration of a heat exchanger (an aluminum mini heat sink) on the proposed µTEGs. Up to now, all harvesting measurements have been performed by placing the devices on a hot plate, which makes the bulk Si part of the device act as a hot side of the µTEG. Therefore, the suspended microplatform has been the cold side of the µTEG. For the approaches studied for the heat exchanger integration, both directions of the heat flow have been however considered. The same heat flow direction than in harvesting measurements (bulk Si rim as the hot side, suspended microplatform as a cold side) is applied for the integration route called as *top approach*. In the alternative *bottom approach*, however, the aim is to heat the suspended microplatform with a hot plate and to cool down the bulk Si with a heat sink. Both approaches will be discussed in the following sections.

Since the proposed µTEG has a planar layout built around a suspended platform, the heat sink can not be directly placed on top of this fragile platform. Additional components are included in the assembly to prevent the application of an excessive force on the suspended platform. Thermal conductivities and dimensions of these components are also critical to optimize the heat flow. In addition, to be able to measure the performance of the µTEG once assembled, a printed circuit board (PCB) is designed and connected electrically to the µTEG by wire bonding. The PCB is made of FR-4 which is a composite material composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant. The decomposition temperature of the FR-4 is around 300 °C [106]. Figure 4.6 shows the PCB layout (designed by Marc Dolcet, from the CNM Thermoelectrics Group), and the image after wire bonding the chip inside the PCB. The same PCB layout is used for both approaches.

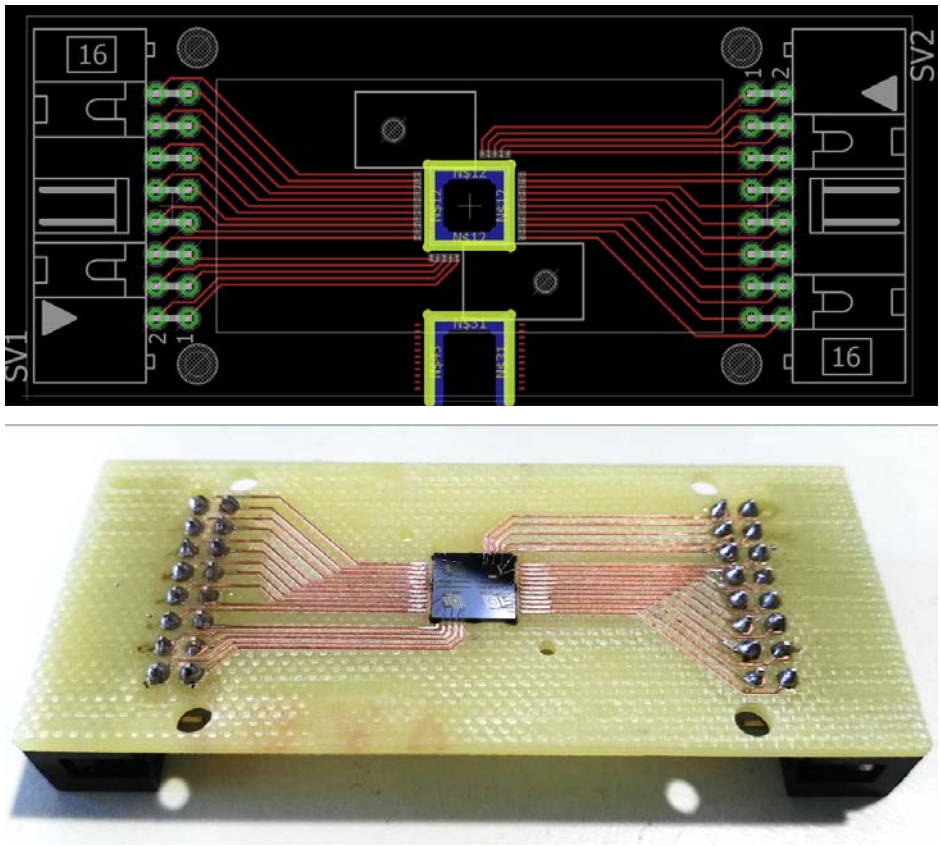

Figure 4.6: PCB layout designed with Eagle software (top), and image of the µTEG chip (featuring four devices) placed inside the cavity of the PCB and wire bonded to Cu interconnects on the board (bottom).

4.3.1 Top approach

In the top approach, the assembly is designed in a way that the bulk Si rim acts as the hot side and the suspended platform acts as the cold side. The reason of naming this route as a top approach is because the suspended platform is contacted from its the top side.

Figure 4.7 shows the components of the assembly together with their functions. The first component of the assembly is a 500 µm thick *copper (Cu) plate* (4x2 cm^2, 500 µm thick) with 4 holes (1.5 mm in diameter) for the alignment with the other components using pins. On the Cu plate, a smaller *square Cu piece* (6x6 mm^2, 1 mm thick) is attached using a solvent based alcoholic paste. Alignment of this Cu piece is done by using the *perforated PCB*, which exhibits a matching cavity and also includes the aligning holes. These Cu components are used to transfer the heat from the hot plate to the bulk Si rim of the device due to their high thermal conductivity. The PCB is fixed to these bottom Cu components with a silver-based epoxy (EPO-TEK®H70E). Then, the attached components are placed inside the oven at 120 °C for 15 min to cure the epoxy. The same curing step is repeated after each application of an epoxy. Next, the µTEG is placed inside the cavity of the PCB and fixed. It is important to note that the chip should be consistently touching the Cu piece, therefore, an epoxy is used to ensure the thermal contact between the hot plate/Cu plates and the chip. Next, wire bonding is done between the contact pads of the µTEG chip and the Cu tracks on the PCB.

The *heat sink adapter* is the component used to direct the heat flow from the suspended microplatform to the heat sink. It includes a brass piece (8x8 mm^2, 500 µm thick) with 4 holes (each with 600 µm diameter) filled with Cu wires. To prevent the heat sink from exerting an excessive force on the suspended microplatform through the heat sink adapter, a *spacer* is placed between the heat sink and the device resting only on the bulk Si areas of the latter. Since the heat should flow preferably from the suspended microplatform to the heat sink with the help of the heat sink adapter (which is detailed in the paragraph below), any direct heat flow between the bulk Si rim and heat sink, through the spacer and skipping the NWs, should be prevented as much as possible. For that purpose, polymethyl methacrylate (PMMA) is chosen as a spacer material due to its low

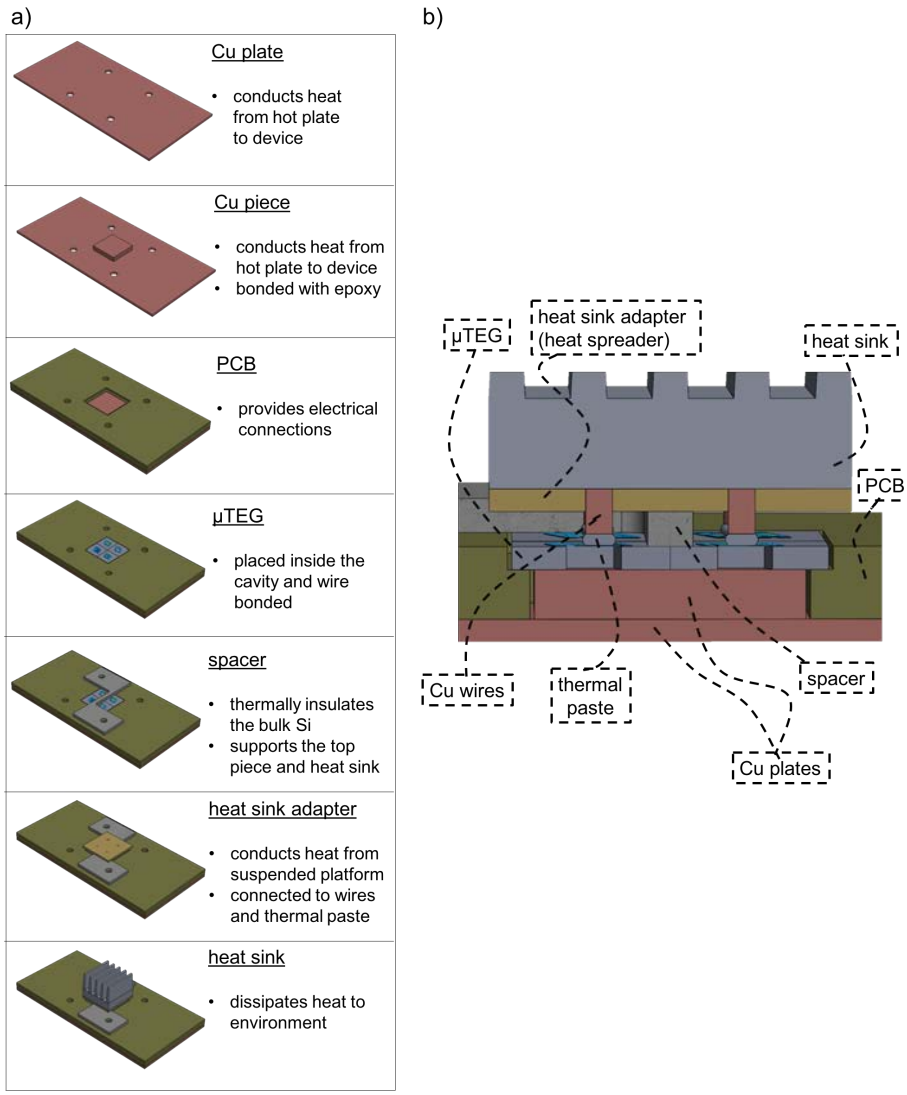

Figure 4.7: a) Schematic of the heat exchanger integration route for the top approach including the components and their main functions. b) Cross sectional schematic of the assembly indicating the different components involved.

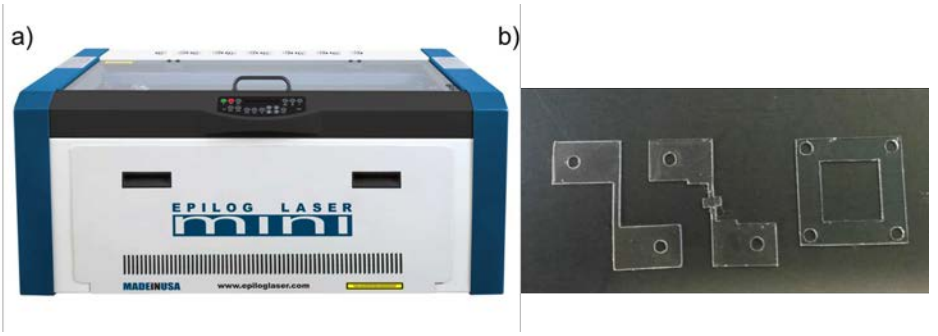

Figure 4.8: a) Epilog Mini 24 laser cutter used for the fabrication of PMMA pieces. b) PMMA pieces cut by laser. S-shaped pieces are used as spacer while the square shaped pieced is used for the alignment of the heat sink adapter.

thermal conductivity of around 0.19-0.22 W/mK [107], [108] and its easy and cheap fabrication. A laser cutter (Epilog Mini 24) is used to cut the 500 µm thick PMMA piece into an *S-shaped* spacer, which is also aligned with the rest of the components using the alignment pins. The obtained pieces by laser cutting are shown in Figure 4.8 together with the equipment itself. S-shaped pieces are used as spacers while the square shaped piece is used for the alignment of heat sink adapter on top of the spacer.

For the preparation of the heat sink adapter component, 4 Cu wires (0.6 mm in diameter) are placed inside the holes of the brass piece. Wires are fixed to the brass piece with an epoxy. Next, the tips of the wires are polished to have the same length for each with the help of an ancillary PMMA stencil, which is removed after the polishing. Figure 4.9a shows the preparation steps for the heat sink adapter. The height of the protruding wires is set to 375 µm which ends up in a 125 µm gap between the wire tip and the suspended microplatform (considering the spacer thickness of 500 µm). To fill these gaps without applying too much pressure on the microplatforms, the tips of the wires are dipped in thermal paste which usually has a thickness of between 150-250 µm. Since the wire diameter is about half of the size of the suspended microplatform, we have enough clearance to tolerate some squeeze out of the thermal paste. The paste should not overflow over the NWs area, though, since this will produce a thermal shortcut. Optical microscopy images of one of the wires

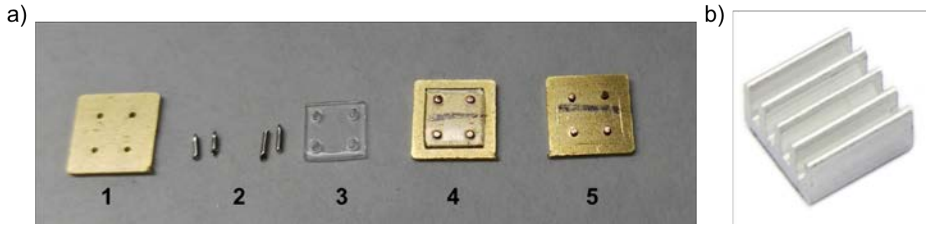

Figure 4.9: a) Steps of the fabrication of heat sink adapter. Brass piece (1), Cu wires (2), PMMA stencil (3), brass/wires/PMMA just after polishing the wires (4), final heat sink adapter (5). b) Aluminum mini heat sink.

dipped into thermal paste and of the test device after removing the heat sink can be seen in Figure 4.10. Even though a certain amount of squeeze out is observed, the microplatform area is big enough to keep the droplet within its borders. At this stage the functionality of the heater located in the platform can be sacrificed since the aim of the assembly is to undergo harvesting measurements. However, the heater can still be used to measure the platform temperature if it is properly passivated.

The last step of the integration is to place the *aluminum (Al) heat sink* on top of the heat sink adapter using a thermal paste in between to secure them in place with an appropriate thermal contact. The mini heat sink has the dimensions of 8x8x6 mm^3. Figure 4.11 shows the final image of a assembly.

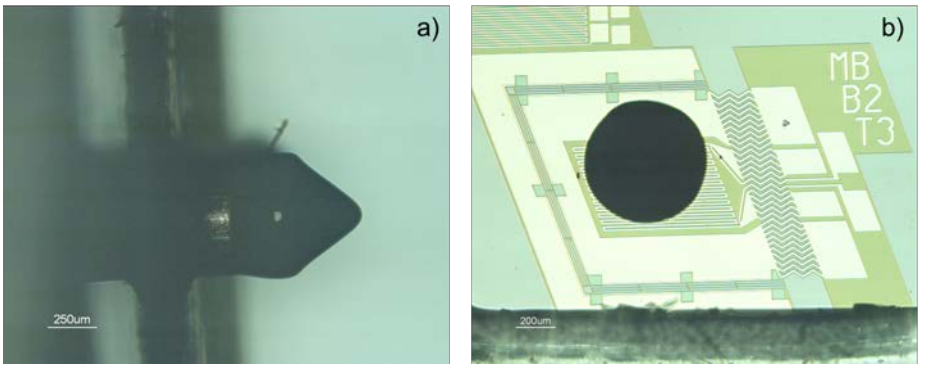

Figure 4.10: Optical microscope images of a) the Cu wire dipped in a thermal paste and b) the test device after removing the heat sink adapter with wires and thermal paste from top of it. The wire is properly aligned on top of the microplatform.

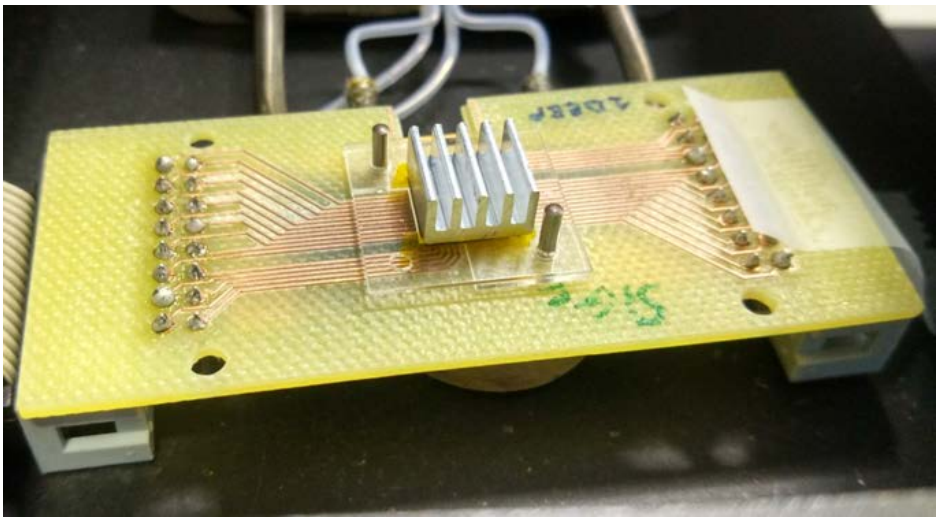

Figure 4.11: An image of the final assembly built following the top approach.

4.3.2 Bottom approach

An additional route is designed to see what happens if we change the heat flow direction. This approach is called bottom approach since the suspended microplatforms are thermally contacted from their bottom side. This time, heat is directly transferred from the hot plate to the suspended microplatforms with the help of Cu wires, and the heat sink cools down the bulk Si part of the device from the top side.

Figure 4.12 presents the components along with their functions in the assembly. The first component of the assembly is the same than the one used for the top approach, which is a Cu plate with 4 holes. Instead of placing a small bare Cu piece on top of the bigger Cu plate, a Cu piece with 4 holes filled with Cu wires is glued. The preparation of this piece is similar to the one followed to obtain the heat sink adapter of the top approach, the only differences being the starting material of the base piece (Cu instead of brass) and its dimensions (6x6 mm^2 instead of 8x8 mm^2). Wires diameter is 600 µm and their length is arranged with respect to the resulting working distance when the chip is encased in the PCB. The component dimensions are arranged in a way that if fits inside the PCB cavity and the distance between the wires and the platform lays between 150-250 µm to accommodate the thermal paste that will assure a good thermal contact. Once the Cu wires are then dipped in that thermal paste, directing the heat flow from the hot plate to the suspended microplatform, the µTEG is placed inside the cavity of the PCB.

After making the electrical connections via wire bonding, an S-shaped spacer is placed on top the device. The geometry is the same than the one of the PMMA spacer used for the top approach. However, since we want to conduct heat from the bulk Si rim to the heat sink this time, this piece is made of brass instead of PMMA. Brass and Cu pieces used in both approaches are fabricated by local provider PANTUR using micro laser cutting technologies. Finally, the Al mini heat sink is placed on top of the spacer using a thermal paste in between.

An image of the final assembly for the bottom approach can be seen in Figure 4.13. In this approach, it is difficult to observe if the Cu wires are touching the suspended microplatform or not. For that

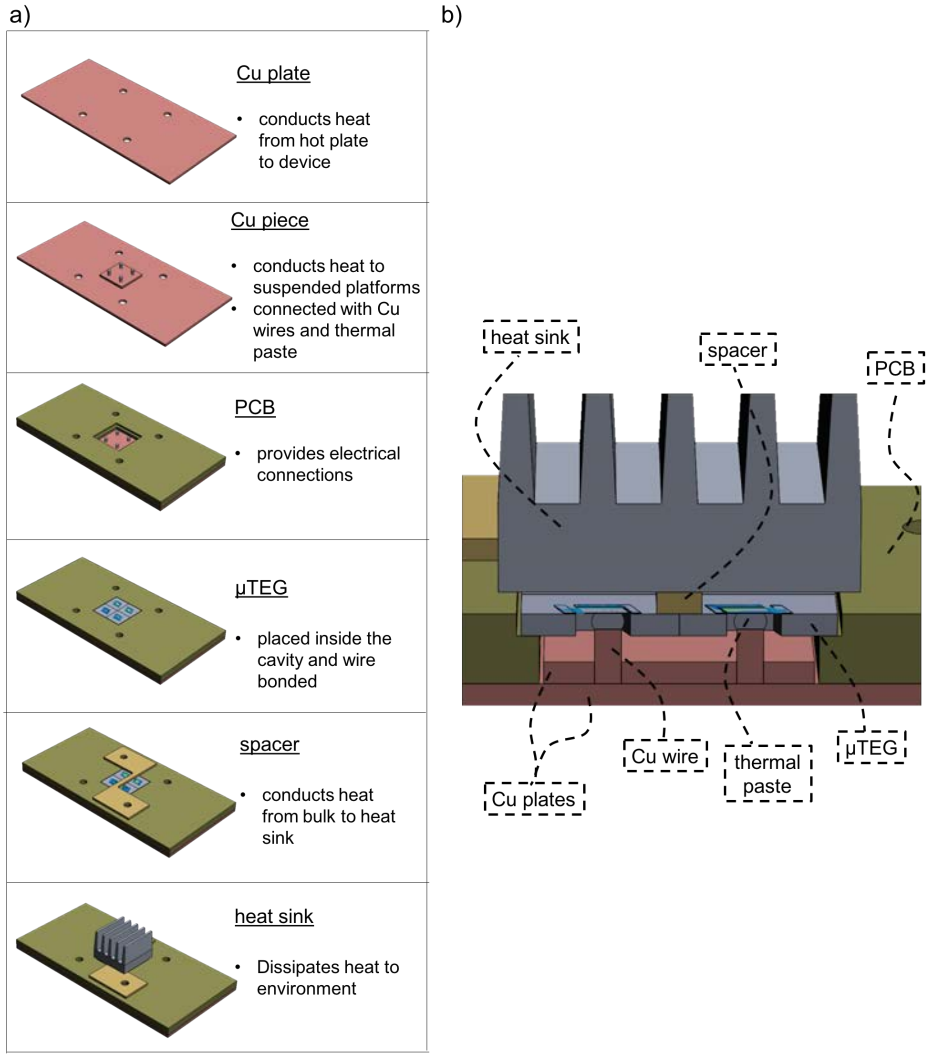

Figure 4.12: a) Schematic of the heat exchanger integration route for the bottom approach including the components and their main functions. b) Cross sectional schematic of the assembly indicating the different components involved.

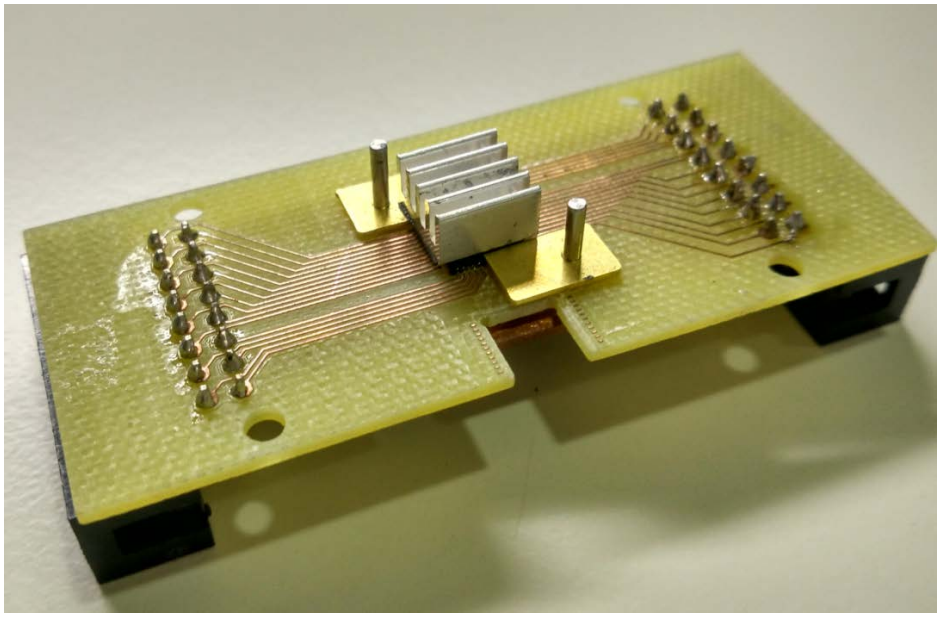

Figure 4.13: An image of the final assembly using the bottom approach.

purpose, an additional cavity is opened on the side of the PCB to rehearse the alignment and fitting of the components.

4.4 Simulations with the assembled heat exchanger

During the planning of the routes for the integration of a heat exchanger, simulations have been conducted to anticipate their thermal and electrical performances. COMSOL Multiphysics 5.2 finite element analysis software is used for the simulations. Final physical implementation of both routes are sketched in real dimensions using Solidworks 2014 and imported into COMSOL software.

The relevant parameters of thermoelectric active materials used for the simulations are listed in Table 4.2. Properties of the other materials (Cu, Si_3N_4, SiO_2, FR-4 and PMMA) are added from the material library of the software. Simulating thousands of NWs bridging the trenches requires too many meshing elements and memory. To prevent this, a meta-material is introduced between the trenches,

Table 4.2: Parameters used for the simulations.

Parameter	**Si NW**	**Si bulk**	**W**	**TIM**[a]
Electrical conductivity σ (S/m)	2000*occ[b]	2000	7e^{6}	-
Thermal conductivity k (W/mK)	(25e-3*(1-occ)+ 25*occ)	150	174	5
Seebeck Coefficient S (V/K)	250e^{-6}	210e^{-6}	5e^{-6}	-

[a] Thermal interface material.
[b] Area occupation of NWs, which is 0.05 for the presented work.

the properties of which are introduced by combining air and NW properties. The electrical and thermal conductivity of the meta-material is extracted considering that the NWs occupy nearly 5% of the total trench area (mentioned as *occ* in the Table 4.2). Since these simulations aim to compare the two approaches (bottom and top approaches), it is considered to be enough to appraise only the Si NWs based µTEGs.

First, the temperature distribution in the overall system has been simulated using the heat transfer module of the simulation software. The boundary conditions applied to the model are setting the bottom temperature to different working temperatures and to apply natural convection conditions with an ambient temperature of 293 K on the exposed surfaces. Three different architectures have been simulated using the same conditions: without heat sink, with heat sink using the top approach, and with heat sink using the bottom approach. For the device without heat sink, convective heat flux is applied on the bare suspended microplatform. For the assemblies with heat exchanger, convective heat flux is applied on both vertical walls and horizontal plates of the heat sink fins.

Figure 4.14 shows the temperature distribution maps when the hot plate temperature is set to 373 K. It has been observed that from the µTEG itself we could only get a maximum ΔT of 0.5 K

out of 80 K of temperature difference between the hot plate and the ambient (4.14a). For the heat exchanger integrated µTEGs, on the other hand, ΔT has been increased to 10 and 23 K by using bottom and top approaches, respectively (4.14b). For all the cases, maximum ΔT is observed on T4 devices.

Next, the heat transfer module interface is coupled to electric currents to be able to extract the thermoelectric power from the µTEGs. Seebeck voltage (V_{oc}) is determined after the obtained ΔT by the heat transfer module using the Seebeck coefficient of Table 4.2. Similar to the thermoelectric power measurements presented in previous chapters, sweep of the voltage is applied on the internal collectors of each device (from 0V to V_{oc}), and the current values for each applied voltage are extracted from the external collectors. Seebeck voltage vs hot plate temperature curves obtained from the µTEG with 1 and 4 trenches are given in Figure 4.15. It is clearly visible that the top approach performs better than the bottom approach. The voltage obtained from the top approach is about 2-2.5 times higher than the voltage obtained from the bottom approach for the same device bottom temperature and number of trenches. The reason is that the thermal contact between the hot plate and the bulk Si part of the device in the top approach is much better than the thermal contact between the heat exchanger and the bulk Si part in the bottom approach. In the first case the contact area is large, involving all the bottom Si surface available while in the second the contact is done only in a limited area (thin and long part of the thermally conducting S-shaped spacer). This constraint on shape and limited area was due to the need to preserve enough space for wire connections along two sides of the chip. The same spacer geometry was used for the top approach, but since in that case it was made of low thermally conducting PMMA and the objective was to decrease the heat conduction as much as possible, it is better to have less area.

Figure 4.16 compares the power obtained from a finite element model for 3 cases: without heat exchanger, with heat exchanger using bottom approach, and with heat exchanger using top approach. As anticipated, a better thermal isolation and hence better ΔTs and Seebeck voltages are obtained for devices with a larger number of trenches, also when the heat sink is present. In terms of thermopower, there is no evident trend following the Seebeck voltage linearity for

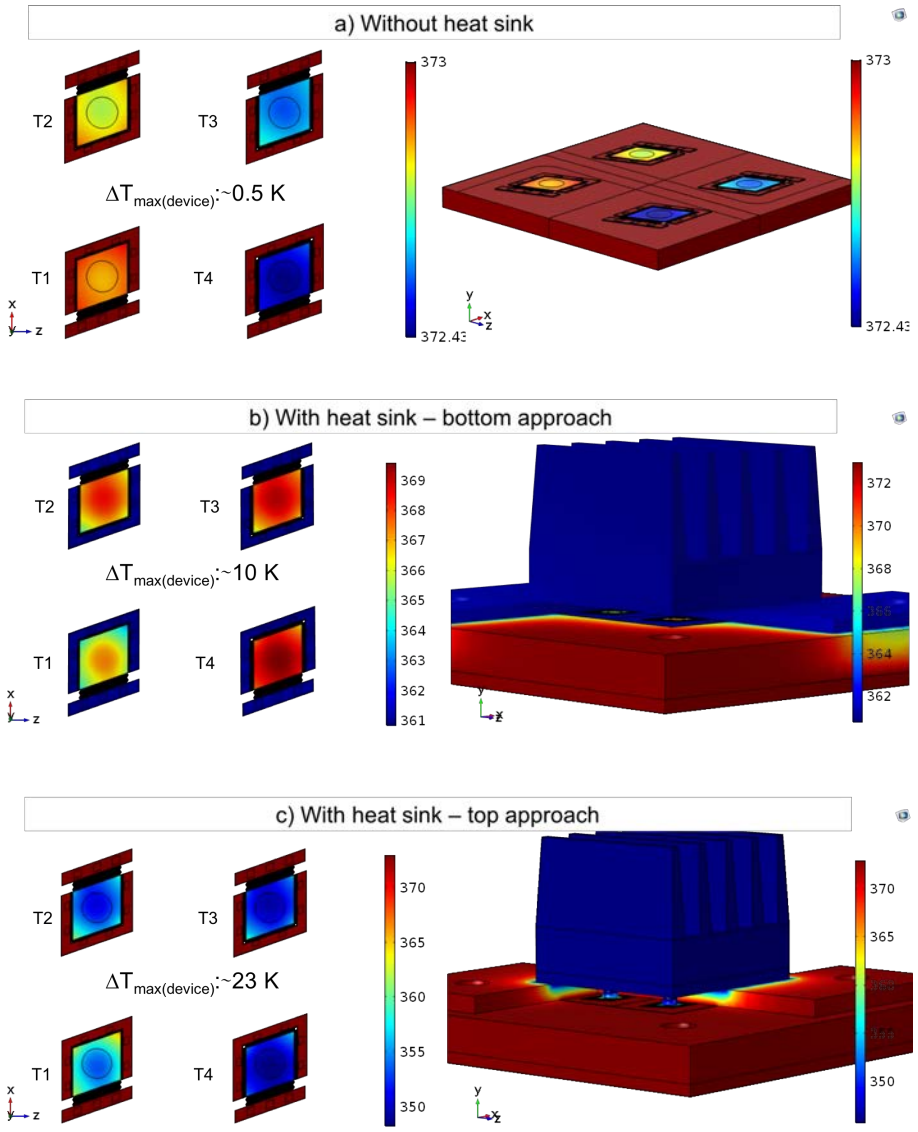

Figure 4.14: a) Temperature distribution of a µTEG obtained from a finite element model without heat sink. Temperature distributions applying the same conditions on a similar µTEG with heat sink using b) bottom and c) top approaches. Images on the left represents the temperature distribution at chip level (at the suspended platform plane) for the four chips present, differing in the number of trenches (T1-T4), while the ones on the right represent the temperature distributions of the whole 3D assemblies. The chip bottom temperature is fixed at 373 K while the top surfaces experiment a natural convection in an ambient temperature of 293 K.

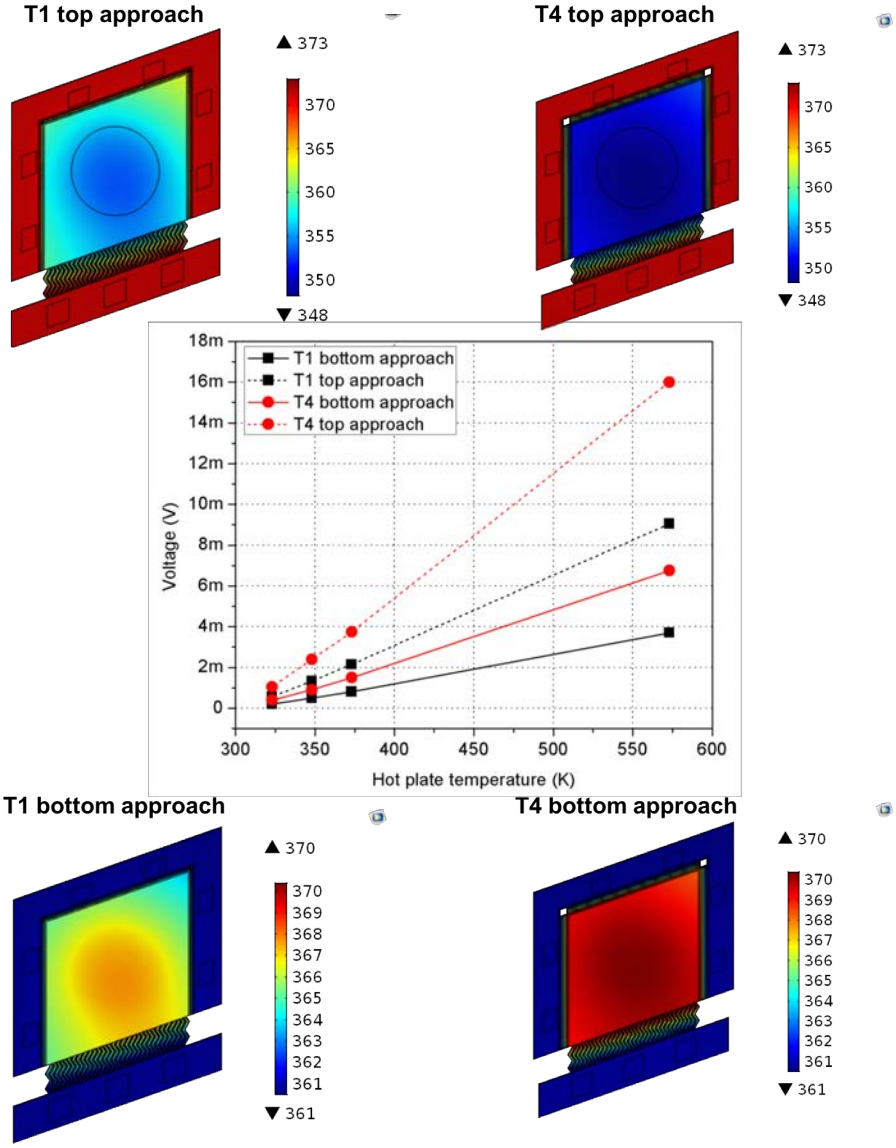

Figure 4.15: Comparison of top and bottom approaches in terms of Seebeck voltage with respect to hot plate temperature (center). Data is extracted from the simulations of the µTEG with 1 (T1) and 4 trenches (T4). Temperature profiles of single thermocouples with 1 and 4 trenches for both approaches, top approach (top) and bottom approach (bottom), for a hot plate temperature of 373 K are also shown.

Table 4.3: Electrical resistance (R), Seebeck voltage (V_{oc}), and maximum power (P_{max}) of the devices obtained by the finite element model for three different cases. The harvesting simulations are conducted when the device bottom temperature (hot plate temperature is kept at 373 K).

		without heat sink		**bottom approach**		**top approach**	
	R (Ω)	Voc (mV)	Pmax (nW)	Voc (mV)	Pmax (nW)	Voc (mV)	Pmax (nW)
T1	2.7	0.032	0.093	0.81	61	2.12	420
T2	4.9	0.063	0.201	1.10	69	2.98	454
T3	7.1	0.092	0.302	1.37	66	3.44	418
T4	9.3	0.121	0.396	1.50	60	3.74	375

the cases with a heat exchanger. As explained in previous chapters, the positive effect of more trenches in terms of V_{oc} is counterbalanced in terms of power by a higher electric resistance. When a heat sink is used, most of the attained ΔT is due to its presence rather than to the thermal properties of the Si NWs. This is why the detrimental electrical effect of having longer NWs is more determinant and may be made evident sooner (lower number of trenches) when the heat exchanger is integrated. For the case without heat exchanger, the attained ΔT results from the thermal properties of NWs itself, therefore, T4 results in longer effective NW length and hence higher ΔT. In any case, power obtained from the top approach assembly is almost 7 times higher than the bottom approach which is expected due to its more than 2 times higher Seebeck voltage (Figure 4.16). Using the given parameters in Table 4.2, maximum power is obtained from the µTEGs with 2 trenches (T2) from both approaches.

Table 4.3 lists the electrical resistance (R), Seebeck voltage (V_{oc}), and maximum power (P_{max}) of the devices obtained by the simulations for three different cases. Maximum powers extracted from the simulations of Si NWs based single µTEG with heat sink integrated by bottom and top approaches are 69 and 454 nWs, respectively. It is important to note that NW density (mentioned as area occupation in this section), NW doping and thermal conductivity directly impact on the thermal and electrical properties of NW arrays and hence the maximum power outputs. An analytical study about the dependence of maximum power on these parameters is given in Ref [74].

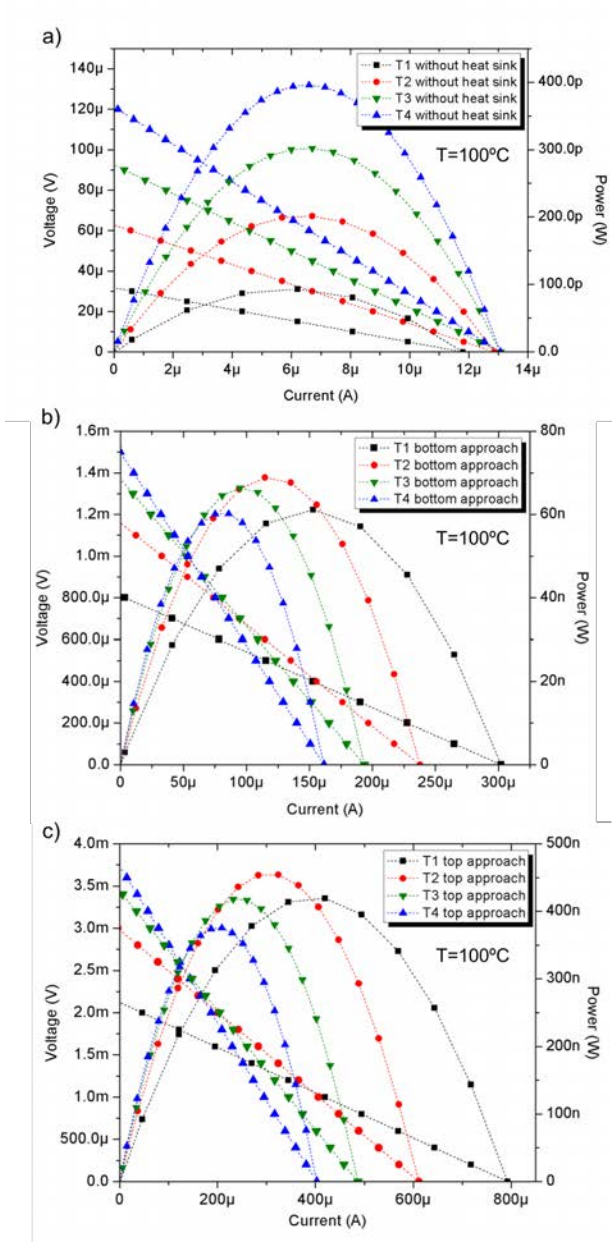

Figure 4.16: I-V and power curves obtained from a finite element model of a Si NWs based µTEGs a) without heat sink, and with heat sink integrated by b) bottom and c) top approaches. Simulations are conducted for the µTEGs with different number of trenches when the device bottom temperature (hot plate temperature) is kept at 373 K (100 °C).

4.5 Thermoelectric power characterization with the assembled heat exchanger

In this section, thermoelectric power measurements of the Si and SiGe NWs based µTEGs with and without heat sink integration are reported. All the measurements presented in this section belong to the membrane supported 2^{nd} generation devices. Since it is evidenced from the simulations that the top approach is significantly more effective than the bottom approach, our efforts have been focused on the integration of a heat sink using the top approach. The setup used for the measurement is given in Figure 4.17. An additional control PCB is designed to connect the PCB of the assembly to the measurement units. Harvesting mode measurements are applied by placing the assembly on the Linkam heating stage at different temperatures. Since the assembly includes a PMMA spacer layer, the temperature of the measurements is limited to 100 °C. No forced convection is applied, all the measurements have been made in a natural convection environment.

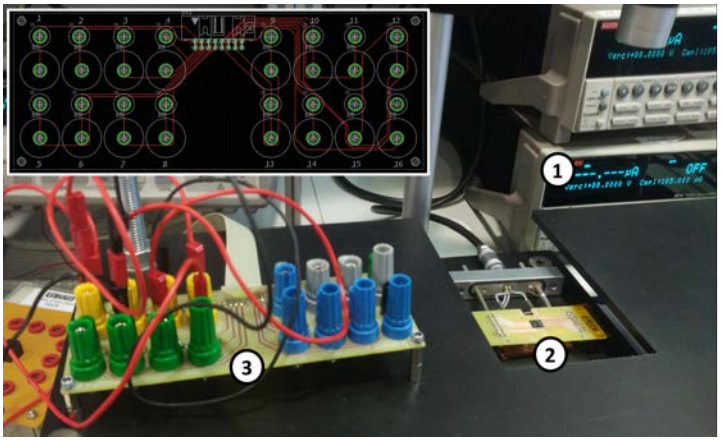

Figure 4.17: Setup used for the measurements. 1) Measurement units, 2) assembly placed on top of the Linkam heating stage (image doesn´t stand for the final assembly), 3) control PCB for the electrical connection between the assembly and the measurement units. The inset shows the layout of the control PCB.

Assembled heat exchanger on Si NWs-based µTEGs

First, harvesting measurements are conducted on the Si NWs-based µTEGs to be able to investigate the improvement attained with the integration of a heat exchanger. As explained, the previously described top approach route is followed for the integration due to its easier implementation and higher efficiency. The same µTEG is used for the measurements with and without heat sink. This µTEG has a lower power output than similar ones presented in Chapter 3 due to the Si support beams on the corners of the suspended microplatform. In Chapter 3, these beams are cut by FIB to be able to obtain the power only from the NW arrays. In this section, they are left as we consider that their detrimental thermal effect will be diluted by the effectiveness of the heat exchanger to obtain larger temperature differences.

Figure 4.18 shows the Seebeck voltage vs hot plate temperature curves for the µTEGs with different number of trenches. Three different conditions are presented: without heat sink, with heat sink and with heat sink + pressing. For both of the cases with heat sink, a tremendous improvement is observed compared to the case without heat sink, resulting from the lower thermal resistance between the cold side of the device and the ambient. Ideally, the highest Seebeck voltage should be obtained from T4, however, no clear trend of improvement is observed from T1 to T4. In this case, different factors affecting the contact between the components of the assembly may be the cause. One of the most significant of these effects is the thickness of the thermal paste. Since the thermal paste is applied manually on the Cu wires, the thickness of the thermal paste changes in the range of 150-250 µm, and hence it is not connecting equally on all four devices. This ends up in different thermal resistances at the interface and different ΔTs between the two ends of the NWs. As can be seen from Figure 4.18, T4 ended up in lower voltages compared to others. After the measurement, the assembly was demounted and the area covered by the thermal paste was observed to be smaller for T4.

Another uncertainty comes from the application of an epoxy between the metal components that may compromise the overall flatness, which might result in nonlinear temperature distribution between the devices. Efforts are being focused on optimizing these

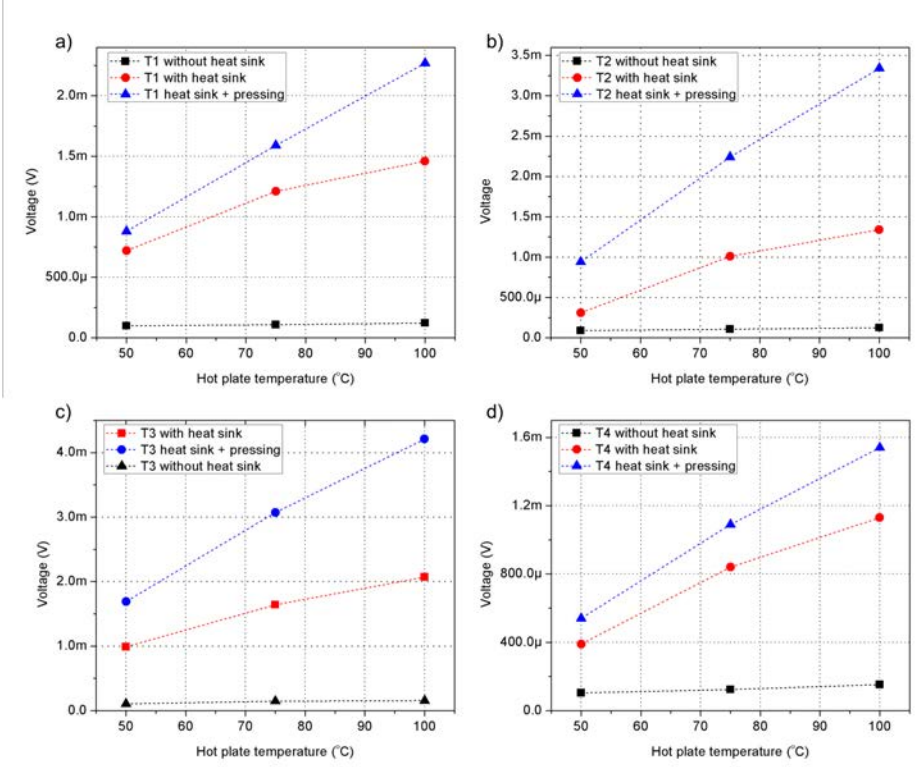

Figure 4.18: Seebeck voltage vs hot plate temperature graphs for Si NWs-based µTEGs with different number of trenches (T1-T4). Figures are presented for three different cases: without heat sink, with heat sink and with heat sink + pressing.

uncertainties to be able to apply the same conditions on all devices. In the case of heat sink + pressing, the pressing is applied passively by placing an additional Cu plate (4x7 mm^2, 500µm thick) on top of the assembly. The extra weight of this piece helps to remove the air bubbles of the thermal paste and decrease the thickness of the thermal paste between the suspended platform and the Cu wires. This application does not harm the suspended platform since the Cu wires cannot reach physically to the suspended platform thanks to the PMMA spacer in between. Voltages obtained from T2 and T3 devices are similar to the simulations which means that the interfaces between the components for these devices are closer to the ideal.

Table 4.4 demonstrates the effect of the heat sink integration on

Table 4.4: Seebeck voltage (Voc) and power density (PD) values of the Si NWs based µTEGs with one and three trenches. Measurements are conducted when the hot plate temperature is at 100 °C. A 2 mm^2 device area is considered.

	T1		T3	
	Voc (mV)	PD (µW/cm^2)	Voc (mV)	PD (µW/cm^2)
without heat sink	0.12	0.061	0.16	0.087
with heat sink	1.46	10.4	2.07	12.5
with heat sink + pressing	2.27	21.5	4.21	41.6

the Seebeck voltage and the power density. The devices with single (T1) and three trenches (T3) are presented for the a hot plate temperature of 100 °C. The maximum power densities obtained are 21.5 (T1), 14.3 (T2), 41.6 (T3) and 7.3 (T4) µW/cm^2 at that temperature. The low performance of T4 device is not only due to its higher electric resistance, but also to aforementioned thermal contacting problems.

Assembled heat exchanger on SiGe NWs-based µTEGs

The abovementioned approach is repeated using the SiGe NWs based µTEGs. In this case, Seebeck voltages without the integration of heat sink are higher than for Si NWs based µTEGs but lower than for the SiGe NWs based µTEGs presented in Chapter 3. Again, the reason of these lower voltages is the presence of bulk Si beam supports on the corners of the platform, which were preserved for the heat sink integration test instead of being cut by FIB. As can be seen from Figure 4.19, significantly higher Seebeck voltages and power values are observed with the heat sink integration. Additional application of a pressure also improved the performance of the µTEG. The data is given for the devices from T1 to T3, since T4 was not functional before the integration of the assembly. Power curves of the T3 device with different heat sink application are presented in Figure 4.19d, and a maximum power output of 903 nW is obtained when the hot plate temperature is kept at 100 °C.

Power densities obtained from the devices with heat sink are 1.4 (T1), 4.5 (T2) and 18.9 (T3) µW/cm^2 when the hot plate is set to 100 °C. With the application of a pressure by placing a Cu plate on top of the assembly, T1 was not functional anymore. The power

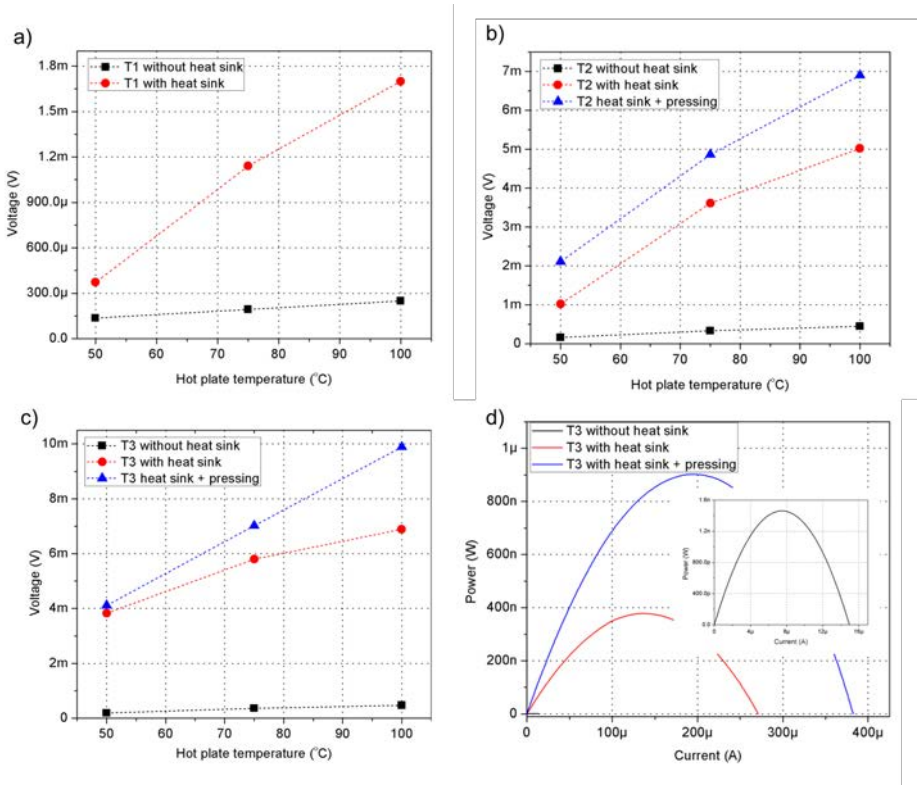

Figure 4.19: a)-c) Seebeck voltage vs hot plate temperature graphs for SiGe NWs based µTEGs with different number of trenches (T1-T3). Figures are presented for three different cases: without heat sink, with heat sink and with heat sink + pressing. d) Power curves obtained from T3 for those three different cases at a hot plate temperature of 100 °C.

densities increased to 9.6 and 45.2 µW/cm^2 for the devices with two (T2) and three (T3) trenches, when the pressure is applied keeping the same hot plate temperature.

Assembled heat exchanger on Si microbeams-based µTEGs

As pointed out in Section 3.2.3, µTEGs with microbeams are also designed and fabricated to be able to compare the performances of micron-sized Si beams with the Si NWs. Different number of beams are fabricated inside the (single) trench area yielding different area occupancies, which in the end determine the thermoelectric power output. From the volumetric shape of the beams defined after the anisotropic KOH process, final trench occupancies for different devices are calculated to be 6.2%, 11%, 20.6% and 39.8%.

Power curves obtained from the device with area occupation of 11% are given in Figure 4.20. A three orders of magnitude increase is obtained in the power output (from ∼650 pW to ∼690 nW for a single thermocouple, i.e. from 32.5 nW/cm^2 to 34.5 µW/cm^2) by integrating a heat sink on the µTEG and applying a small amount of pressure by placing a Cu plate on the assembly. It is worth noticing that being a T1 device, the obtained power density favorably compares to Si and SiGe NWs devices with low number of trenches. In this way, it is shown that even with high thermal conductivity Si beams, it is possible to obtain high power densities by optimizing its area occupation and electrical properties. Additional mask set design including lower area occupancies of Si microbeams is under development.

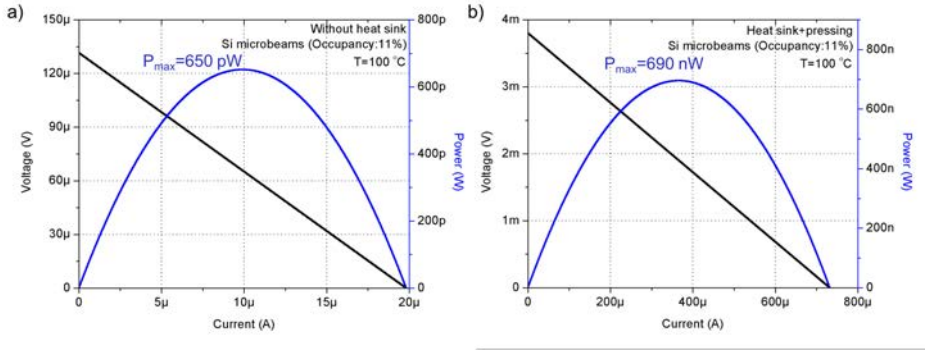

Figure 4.20: I-V and power curves obtained from the Si microbeams based µTEG with the beam area occupation of 11%. Measurements are conducted a) without and b) with heat exchanger at a hot plate temperature of 100 °C and a three order magnitude increase is obtained.

4.6 Discussion & summary

This chapter is motivated by investigating the possible ways to further increase the power output obtained from an all-Si based µTEGs presented in Chapter 3. To achieve this goal, two preliminary experimental studies have been conducted first:

- *Forced convection* has been applied to increase the heat transfer rate between the device and the surrounding air by speeding the airflow on top of the device. It has been confirmed that it is possible to achieve higher Seebeck voltages (2 to 9 times improvement when increasing the effective length of NWs as shown in Figure 4.2) and power densities (up to 34.4 µW/cm^2 at 300 °C from a T4 Si NWs-based µTEG). These values can be improved by further increasing the airflow.

- *A cold-finger approach* has also been investigated to demonstrate the effect of a physical heat exchanger once implemented on the µTEG. In this approach, the suspended microplatform has been contacted with a probe dipped into thermal paste to reduce the thermal resistance between the microplatform and the air. Measurements conducted on T1 Si microbeams based µTEGs have shown that it is possible improving the Seebeck

voltage 6 to 12 times for increasing hot plate temperatures as shown in Figure 4.5, and a two orders of magnitude increase in the power density has been harvested at 250 ° for such device. It is worth noticing than an equivalent device to the one than improved 12 times its Seebeck voltage, only improved by a factor 2 when forced convection was applied instead, so physical contact proves more effective.

After verifying experimentally the significant improvement brought by the abovementioned studies, two different routes have been designed for the integration of a heat exchanger. In the *top approach*, the same heat flow direction is maintained as in the case of the harvesting measurements in Chapter 3 (bulk Si rim acting as the hot side, suspended microplatform being the cold side). The heat flow direction is reversed for the *bottom approach*, in which the suspended microplatform is heated with the help of different components while the bulk Si rim is cooled with the help of the heat sink. Next, both approaches have been compared by simulating their Seebeck voltages and thermoelectric powers using a finite element method. It has been concluded that the top approach performs much better than the bottom approach (almost 2.5 times higher Seebeck voltages). Taking into consideration its easier implementation and higher efficiency, experimental studies have been oriented on the integration of a heat exchanger using the top approach.

Harvesting measurements have been performed on the µTEGs with the heat exchanger integrated via top approach. A significant amount of improvement has been observed for all tested µTEGs based on different thermoelectric materials (Si NWs, SiGe NWs and Si microbeams). Maximum power densities obtained from heat exchanger integrated µTEGs based on NWs are 41.2 (Si NWs) and 45.2 µW/cm^2 (SiGe NWs) for a T3 device and a hot plate temperature of 100 °C. For Si NW based µTEG, the power density with the heat exchanger integrated assembly is more than two orders of magnitude larger compared to the same µTEG without heat exchanger. Even µTEGs based on micro sized Si beams are able to offer 34.5 µW/cm^2 for a T1 device. When the attainable working ΔT is mostly secured by the presence of an adequately assembled heat sink, the thermal properties of the thermoelectric material itself seem to become less determinant than the electric ones (its Seebeck coefficient and electrical resistance). In

any case, it is important to note that we cannot strictly compare the µTEGs with a heat exchanger for different thermoelectric materials with a heat exchanger since its integration is not yet optimized and the conditions applied on each device are not guaranteed to be the same yet. However, we can clearly conclude that in all cases there is an enormous increase in the thermoelectric performance, and that tens of $\mu W/cm^2$ are achievable. Optimization of the heat exchanger integration is an ongoing work. Materials limiting the measurement temperature are being replaced with high temperature stable materials as well as the replacement of the heat sink adapter with a micromachined uniform single piece (See *Future Work* section of this thesis).

Table 4.5 compares the results obtained in this work with state-of-the-art µTEGs. Power densities are calculated by dividing the maximum power output values by the device area in each case. P_{max}/couple values are calculated by dividing maximum power output of the µTEG to the number of thermocouples that it includes.

Even though numerous thermoelectric materials are currently being studied in terms of their thermoelectric performances, only few of them could be integrated into actual µTEGs. Among these, the number of µTEGs that could be converted into a commercially available product is even lower, and not much successful to date. All of the companies producing µTEGs are using V-VI semiconductor compounds as thermoelectric material, there is no report on the commercial use of Si-based µTEGs yet. As expected, power densities and factors obtained from V-VI semiconductors-based µTEGs are higher compared to their Si-based counterparts due to their superior thermoelectric properties. However, it can be clearly concluded that the Si NWs-based µTEG presented in this work is very well positioned among the other Si-based µTEGs. Especially the power obtained per thermocouple in this work is higher than most of its counterparts and it can even compete with the V-VI semiconductor compounds.

With respect to SiGe, the work conducted during this thesis (also in a collaboration with IREC) reports for the first time the fabrication and characterization of SiGe NWs-based µTEGs. The work presented in this thesis reports the highest power per couple compared to the ones from IMEC and Infineon using poly SiGe thin films. Generally speaking, it is difficult to compare the reported power densities since

Table 4.5: Comparison of the results obtained in this work with the state-of-the-art thermoelectric microgenerators

Company/ Group	**TE Material**	**ΔT (K)**	**N^o of couples**	**P_{max}/A (µW/cm^2)**	**P_{max}/couple (nW)**	**Ref.**
Nextreme (Laird) [a]	$(Bi,Sb)_2Te_3$	10	NA	1.4-1.5e^{-}4	NA	[109]
RMT [a]	BiTe	70	NA	8-16e^4	NA	[110]
Fraunhofer	$(Bi,Sb)_2Te_3$	5	12	60	60	[111]
DTS	$Bi_2(Sb,Se)Te_3$	20	2250	31.3	9	[112]
Micropelt [ab]	Bi_2Te_3	10	540	1e^4	2700	[113]
FBK	Cu/Ni	22	180	1.1	4	[114]
NCHU	p/n poly Si strips	1	24	5.4e^{-6}	2e^{-5}	[115]
HSG-IMIT & Kundo	mono Si/Al	10	1000	9.1	1.5	[116]
UAB	mono Si thin film	5	20	4.5	NA	[27]
Infineon	poly Si	10	15782	6.21	0.027	[28]
A*STAR	poly Si	5	125144	1.3	0.01	[105]
Infineon	poly Si-Ge	8.5	15782	2.73	0.012	[28]
IMEC	poly Si-Ge	10	1766	1.07	0.045	[76]
NUS	Si NWs (DRIE)	70	162	1.9	3	[117]
Imperial College	Si NWs (MACE)	37	1	14	3.5e^3	[46]
CNM-IREC	Si NWs (VLS)	50	1	23	230	[75]
This work	**Si NWs (VLS)**	**2.1**	**1**	**0.9**	**18.3**	
This work	**SiGe NWs (VLS)**	**14.3**	**1**	**7.1**	**142**	
This work	**Si NWs (VLS)** [c]	**17.3**	**1**	**41.2**	**824**	
This work	**SiGe NWs (VLS)**[c]	**53.5**	**1**	**45.2**	**903**	
This work	**Si microbeams** [c]	**18**	**1**	**34.5**	**690**	

[a] Information taken from the data sheets.
[b] Reported as insolvent as of December 2015.
[c] Data for the heat exchanger integrated assembly.

the data given belongs to different ΔTs, and those ΔTs may be also of different nature (internal/external with respect to the device, naturally developed/artificially imposed). The results obtained during this work are very promising, and point to a high potential to be applied into considered applications even without the integration of a heat exchanger. With the emergence of more low power devices, Si (and SiGe) based thermoelectric generation is expected to participate in the market.

It is possible to further increase the performance reported in this work by both optimizing the NW properties (doping, roughness, size and density distribution, etc.) and the microplatform design (decreasing the device area, reducing internal losses, etc.). Optimizations regarding the microplatform design have already begun and will be mentioned in the *Future Work* part of this thesis.

Conclusions

The study presented throughout this thesis deals with the optimization of a planar thermoelectric microgenerator (µTEG) based on the use of Si and SiGe nanowire arrays as thermoelectric material. Dense arrays of such nanowires (NWs) are monolithically integrated by means of VLS-CVD into a silicon micromachined device composed of a suspended microplatform and a surrounding bulk Si rim. Compared to a preceding study following the same approach, a significant reduction in device thermal conductance and electrical resistance is obtained which yields higher power outputs.

The thermal performance of the µTEG, which is linked to the attainable ΔT, is enhanced by revising the architecture reducing the parasitic thermal losses between the hot and cold ends of the µTEG. This is achieved by replacing the bulk Si connection that serves as a support for the metal lines through the suspended microplatform with a thin dielectric membrane. The thermal conductance of the platform is decreased by 34% with this new arrangement. In addition, the effect of other design features, such as membrane length and number of trenches, on the thermal conductance is investigated. Within the current device design limits, the latter has a much larger impact (the more trenches, the better platform thermal performance). The electrical performance of the µTEG is also enhanced by decreasing the device internal resistance. The microplatform is redesigned to have lower metal resistances on the collectors, and additional processing steps are employed to minimize the metal/Si contact resistance. As a result, device internal resistance decreased 7 to 20 times compared to the preceding µTEG.

Optimized µTEGs with different number of trenches (T1 to T4) filled with NWs are characterized to investigate the effect of NW length on the Seebeck voltage and power output. Even though the

highest Seebeck voltage is obtained from the µTEG with the highest number of trenches (T4), the same trend is not observed for the power output since the electrical resistance of NWs also increases with their effective length (i.e. number of trenches). Maximum power densities of 0.34 and 7.1 µW/cm^2 are obtained from Si and SiGe NW based µTEGs, respectively, when they are placed on a waste heat source of 200 °C under natural convection conditions. It is worth noticing that the optimized Si NW device exhibits 21 times more power than the preceding version for the aforementioned conditions. SiGe NWs were more electrically resistive than Si NWs and exhibited a lower Seebeck coefficient, so the above result is a clear consequence of the much lower thermal conductance of the former. Also, it points to the fact that optimized SiGe NW offer the chance of obtaining even higher power outputs.

Even though the power outputs obtained from SiGe NWs based µTEGs are convenient for powering small wireless nodes (if heat sources at 200 °C or higher are available), ways to further improve the power density have been studied. One important limitation of µTEGs is the quite moderate temperature differences that develop across the thermoelectric material when placed on a waste heat source due to the small size of the device. The thermal resistance to the ambient of a bare small surface is so high that under natural convection the device is only capturing a minimum fraction of the total temperature difference existing between the heat source and the ambient. Since most of the literature report the performance of a µTEG when there is a fixed temperature on both ends of the thermoelectric material, this thesis aimed to emphasize the importance of being able to create reasonable temperature differences in harvesting applications (without forcing an external temperature difference). Therefore, routes for the integration of a heat exchanger on the proposed planar µTEGs are designed, simulated and characterized. With the integration of the heat exchanger, a significant amount of improvement has been observed for all tested µTEGs based on different thermoelectric materials (Si NWs, SiGe NWs and Si microbeams). µTEGs with integrated heat exchanger were able to harvest 41.2 (Si NWs), 45.2 (SiGe NWs) and 34.5 µW/cm^2 (Si microbeams) when they were placed on a waste heat source of 100 °C. This is 50-1000 times more than for similar devices without heat exchanger at the same hot plate tem-

perature. Clearly, the presence of the heat exchanger changes the device internal balance of thermal resistances in a way that makes the thermal conductivity of the thermoelectric material less relevant, while making electrical parameters (Seebeck coefficient and electrical resistance) to gain importance.

In summary, the work developed in this thesis focuses on two technological approaches to improve the power outputs of a μTEG: i) electrical and thermal optimization of the microplatform, ii) integration of a heat exchanger to minimize the thermal resistance between the μTEG and the ambient. Results obtained in this thesis are well positioned compared with the state-of-the-art μTEGs. In addition, this thesis, together with the one performed in collaboration at IREC, reports for first time on the performance of SiGe NWs based μTEGs.

Ongoing & Future Work

Thermoelectric Microgenerator

A new parallel project has been initiated during the last year of this thesis which aims to further increase the power output per chip. For that purpose, similar devices have been designed with smaller device area to be able to include larger number of devices per chip. Figure 4.21 shows a single thermocouple element following the same approach as the one presented in this thesis: a planar unileg thermoelectric microgenerator based on the monolithic integration of dense arrays of silicon and silicon/germanium nanowires as the thermoelectric material. The suspended microplatform area is designed to be 5 times smaller (1 mm^2 to 0.2 mm^2) with 15 µm wide trenches located only on one side of the suspended microplatform.

To be able to harvest high power output by increasing the voltage and current, devices with series and parallel configurations are designed. The same approach was used in the work of this thesis,

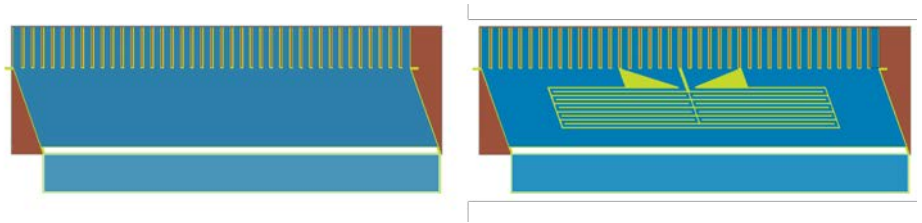

Figure 4.21: New thermoelement design with smaller suspended microplatform area and different configuration for the suspended membrane. The red area shows the DRIE mask to open the suspended platform. A regular design for thermoelectric harvesting purposes (left), and a design with a built-in heater for test purposes (right).

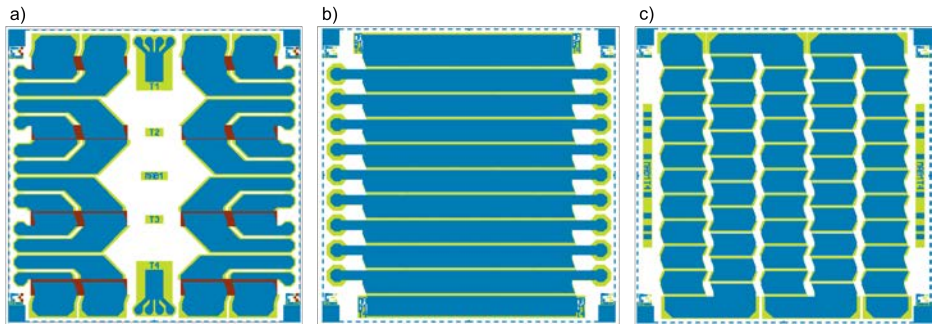

Figure 4.22: Different chip designs for the new layout. a) Standard design with 16 individual devices, b) combination of 5 parallel and 10 series devices, c) series connection of 50 devices.

however, less number of thermoelements were included (4 in a regular chip, 4 in parallel connected chip, 12 in a series connected chip). With this new configuration, a better geometrical approach is considered to evaluate the chip area more effectively. Both of the connected chips include 50 thermoelements as well as a regular chip containing 16 thermoelements.

One limitation of the current microgenerator is the need of the post-process for cutting the bulk Si beams on the corners of the trenches (between the suspended microplaform and bulk Si) that helps to keep the structures leveled before the nanowire growth. In the current approach, these beams are cut by FIB after NW growth to eliminate the associated thermal parasitic losses and this process takes time and slows down the testing of the chips. Studies for further improvements on this issue have been initiated such as replacing these beams by low thermally conducting supports.

Another aspect to cover in the near future regarding the microgenerator might be the implementation of different nanostructured materials in similar devices using the already maturated design/fabrication knowledge. Si microbeams fabricated using standard lithography techniques might be of interest when several thermoelements are connected in series or parallel. In addition, high surface area nanomeshes and nanoporous structures, or even thin films, might be applied as possible thermoelectric materials.

Heat Exchanger

Regarding the integration of heat exchanger, efforts should focus on the optimization of the route for the integration and selecting high temperature stable components to be able to make measurements, and operate, at higher temperatures. Regarding the first case, the non-uniformity of the thermal paste thickness (since it is applied manually) resulted in different pressures on the devices and different thermal resistances between the platform and heat sink. In addition, manual attachment and polishing of the Cu wires compromise the proper leveling of the top components on the devices. These problems might be prevented either by automating the thermal paste application or designing the new components to eliminate the variations caused by the manual operations. For the latter case, low temperature components should be replaced by high temperature stable components to be able to conduct high temperature measurements. Currently, a PMMA piece is included in the assembly due to its fast and cheap production. However, PMMA limits the measurement temperature up to 100 °C. Studies have been already initiated to replace PMMA by high temperature stable 3D printed Zirconia pieces which have low thermal conductivity and can be designed to make the assembly more robust. Additionally, studies for the replacement of the heat sink adapter with a micromachined uniform single piece defining air cavities over most of the Si rim have already been initiated. With these modifications, operation temperature can be increased safely.

Scientific Contributions

Journal Articles

- I. Donmez Noyan, G. Gadea, M. Salleras, M. Pacios, C. Calaza, A. Stranz, M. Dolcet, À. Morata, A. Tarancon, and L. Fonseca, "**SiGe nanowire arrays based thermoelectric micro/nanogenerator**," *In Preparation* (2018).

- I. Donmez Noyan, M. Dolcet, M. Salleras, A. Stranz, C. Calaza and L. Fonseca, "**Integration of a heat exchanger on an all-Si thermoelectric micro/nanogenerator**," *In Preparation* (2018).

- J. D. Santos, M. Salleras, I. Donmez, G. Gadea, C. Calaza, A. Morata, A. Tarancón, and L. Fonseca, "**Power response of a planar thermoelectric microgenerator based on silicon nanowires at different convection regimes**," *Energy Harvesting and Systems* vol.3 no.4 (2016).

- C. Calaza, L. Fonseca, M. Salleras, I. Donmez, A. Tarancón, À. Morata, J. D. Santos, and G. Gadea, "**Thermal test of an improved platform for silicon nanowire-based thermoelectric micro-generators**," *Journal of Electronic Materials* vol. 45, no. 3, pp. 1689–1694 (2016).

- L. Fonseca, J. D. Santos, A. Roncaglia, D. Narducci, C. Calaza, M. Salleras, I. Donmez, A. Tarancon, À. Morata, G. Gadea, L. Belsito and L. Zulian, "**Smart integration of silicon nanowire arrays in all-silicon thermoelectric micro-nanogenerators**," *Semiconductor Science and Technology* vol. 31, no. 084001 (2016).

Conference Proceedings

- I. Donmez, M. Salleras, C. Calaza, G. Gadea, À. Morata, A. Tarancón, L. Fonseca, "**Improved thermal and electrical design for an all-Si thermoelectric micropower source**," *Proceedings of SPIE* vol.10246 no.102460Y (2017).

- C. Calaza, I. Donmez, M. Salleras, G. Gadea, J. D. Santos, À. Morata, A. Tarancón, and L. Fonseca, "**Optimization of power output in planar thermoelectric microgenerators based on Si nanowires**," *Journal of Physics: Conference Series* vol.773 pp.12026 (2016).

- I. Donmez, M. Salleras, C. Calaza, J. D. Santos, G. Gadea, À. Morata, D. Dávila, A. Tarancón, and L. Fonseca, "**Interdigitated design of a thermoelectric microgenerator based on silicon nanowire arrays**," *Proceedings of SPIE* vol.9517 no.95172C (2015).

- L. Fonseca, I. Donmez, M. Salleras, C. Calaza, G. Gadea, J. D. Santos, A. Morata, and A. Tarancón, "**Improved thermal isolation of silicon suspended platforms for an all-silicon thermoelectric microgenerator based on large scale integration of Si nanowires as thermoelectric material**," *Journal of Physics: Conference Series* vol.660 pp.12113 (2015).

Conference Contributions

- *Authors:* I. Donmez, M. Dolcet, M. Salleras, A. Stranz, C. Calaza, L. Fonseca, G. Gadea, M. Pacios, À. Morata, A. Tarancón

  Title: **Integration of a heat exchanger on an all Si-based thermoelectric micro/nanogenerator**

  Congress: International and European Conference on Thermoelectrics, ICT/ECT 2018, Caen, France

  Type: Poster

- *Authors:* L. Fonseca, I. Donmez, M. Dolcet, A. Stranz, M. Salleras, G. Gadea, M. Pacios, A. Morata, A. Tarancón

Title: **Research on thermoelectric microgenerators based on Si and SiGe nanowires as thermoelectric material**

Congress: JNRSE 2018, Besançon, France

Type: Oral

- *Authors:* I. Donmez, M. Salleras, C. Calaza, G. Gadea, À. Morata, A. Tarancón, L. Fonseca

  Title: **Improved thermal and electrical design for an all-Si thermoelectric micropower source**

  Congress: SPIE Microtechnologies 2017, Barcelona, Spain

  Type: Oral

- *Authors:* G. Gadea, I. Donmez, M. Pacios, M. Salleras, C. Calaza, À. Morata, L. Fonseca, A. Tarancón

  Title: **Integration of silicon-germanium nanowires in micro-thermoelectric generators**

  Congress: European Conference on Thermoelectrics, ECT 2017, Padua, Italy

  Type: Oral

- *Authors:* L. Fonseca, C. Calaza, I. Donmez, M. Salleras, A. Stranz, G. Gadea, À. Morata, A. Tarancón

  Title: **All-silicon thermoelectric microgenerator with improved design**

  Congress: Iberian Thermoelectric Workshop, ITW 2017, Porto, Portugal

  Type: Oral

- *Authors:* C. Calaza, I. Donmez, M. Salleras, G. Gadea, À. Morata, A. Tarancón, L. Fonseca

  Title: **Optimization of power output in planar thermoelectric microgenerators based on Si NWs**

  Congress: PowerMEMS 2016, Paris, France

  Type: Oral

- *Authors:* L. Fonseca, C. Calaza, M. Salleras, I. Donmez, A. Tarancón, À. Morata, J. D. Santos, G. Gadea

  Title: **Integration path for an all-silicon MEMS based thermoelectric micro and nanogenerator**

  Congress: European Materials Research Society, E-MRS 2016 Spring Meeting, Lille, France

  Type: Oral

- *Authors:* G. Gadea, À. Morata, J.D. Santos, I. Donmez, C. Calaza, M. Salleras, D. Dávila, L. Fonseca, A. Tarancón

  Title: **Silicon nanowires for thermoelectric harvesting applications: growth, integration and characterization**

  Congress: European Materials Research Society, E-MRS 2016 Spring Meeting, Lille, France

  Type: Oral

- *Authors:* L. Fonseca , I. Donmez, M. Salleras, C. Calaza, G. Gadea, J. D. Santos, À. Morata, A. Tarancón, L. Belsito, A. Roncaglia, L. Zullian, D. Narducci

  Title: **Smart integration of Si NWs arrays in all-silicon thermoelectric micro-nano-generators**

  Congress: Smart Systems Integration 2016, Munich, Germany

  Type: Poster

- *Authors:* J. D. Santos, M. Salleras, I. Donmez, G. Gadea, C. Calaza, À. Morata, A. Tarancón, L. Fonseca

  Title: **Power response of planar microgenerators with different lengths of silicon nanowires**

  Congress: International/Asian Conference on Thermoelectrics, ICT/ACT 2016, Wuhan, China

  Type: Oral

- *Authors:* I. Donmez, M. Salleras, C. Calaza, J. D. Santos, G. Gadea, À. Morata, D. Dávila, A. Tarancón, L. Fonseca

  Title: **Interdigitated design of a thermoelectric microgenerator based on silicon nanowire arrays**

  Congress: SPIE Microtechnologies 2015, Barcelona, Spain

  Type: Oral

- *Authors:* L. Fonseca, I. Donmez, M. Salleras, C. Calaza, G. Gadea, J. D. Santos, À. Morata, A. Tarancón

  Title: **Improved thermal isolation of silicon suspended platforms for an all-silicon thermoelectric microgenerator based on large scale integration of Si nanowires as thermoelectric material**

  Congress: PowerMEMS 2015, Boston, MA, USA

  Type: Poster

- *Authors:* G. Gadea, J.D. Santos, À. Morata, I. Donmez, C. Calaza, M. Salleras, D. Dávila, L. Fonseca, A. Tarancón

  Title: **Integration and optimization of silicon nanowires in a thermoelectric generator**

  Congress: EUROMAT Conference 2015, Warsaw, Poland

  Type: Oral

Appendix A

Test structures for single NW characterization

Measuring the thermal and electrical properties of low-dimensional structures has been a challenge due to the lack of conventional test equipment that are usable for low-dimensional nanostructures. During this thesis work, test microplatforms have been designed and fabricated for the characterization of some nanowire (NW) properties.

Only Seebeck coefficient has been obtained from NWs in array form using the TEG microplatform themselves as explained in Chapter 3. However, it is not possible to determine other material properties very precisely from such NW arrays. Since there are thousands of NWs connected in parallel in a single thermocouple, their density and statistical NW diameter distribution play an important role on the final properties. For instance, NW diameter variation (50-120 nm) ends up in different thermal conductivity values for each NW. Being NW arrays non-practical to extract material properties, individual NWs should be characterized to calculate the material figure of merit. The test microplatforms fabricated in this work are used for the characterization of single NWs in terms of their thermal and electrical conductivity, and for evaluating NW-Si thermal and electrical contact resistance in a still ongoing work [83].

Figure A.1a shows the schematic of the mask layout for a single chip of test platforms. Each chip is composed of 780 hexagons and a few TLM structures for metal/Si contact resistance measurement.

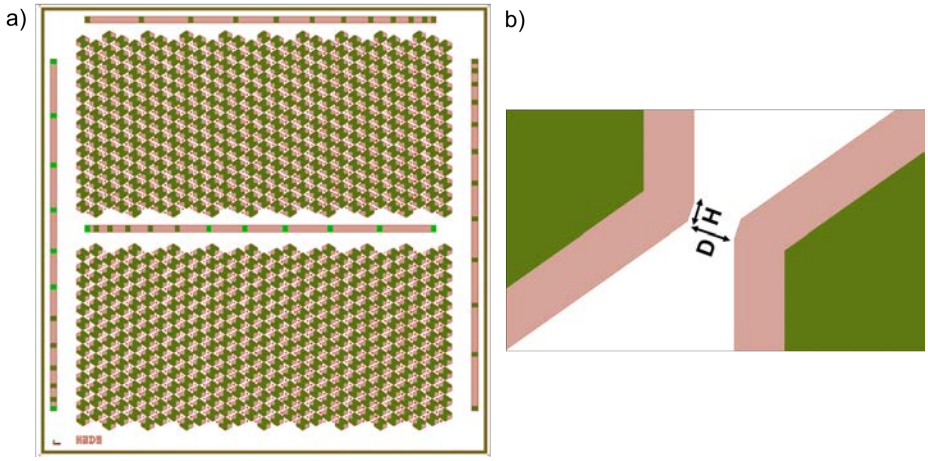

Figure A.1: a) Layout of a single chip including two arrays of hexagon test structures and a few longitudinal TLM structures. b) A closer schematic showing the opposing corners of two hexagons aligned to <111> planes, where single NWs will be grown. D and H are the distances between the hexagons (hence the NW length) and hexagon corner widths, respectively.

Hexagon structures are designed to have <111> planes on the corners to allow the directional growth of NWs between the corners of two adjacent hexagons. As can be seen from Figure A.1b, different distances (D - 2, 5, 10, 15, and 20 µm) and corner widths (H - 2 and 5 µm) are introduced in the design for different measurement purposes.

The fabrication sequence involving two photolithographic levels is presented in Figure A.2. Silicon-on-insulator (SOI) wafers are used as starting substrates with 500 µm of bulk Si layer, 2 µm of buried oxide layer and 3 µm of device Si layer. As for µTEGs, wafers are of (110) orientation so that subsequent processing is able to define vertical <111> planes where to successfully grow NWs. The fabrication process starts with the ion implantation of the substrate with boron using the same conditions applied for the µTEGs to improve the final quality of metal/Si contacts. Then, a first photolithographic mask is used to define four metal areas in each hexagon via a lift-off process of a 30 nm Ti/200 nm W bilayer deposited by sputtering. Samples are then rapid thermally annealed at 700 °C during 30 s to ensure an ohmic contact. Next, 1 µm of passivation oxide is deposited in a plasma enhanced chemical vapor deposition system. This layer is

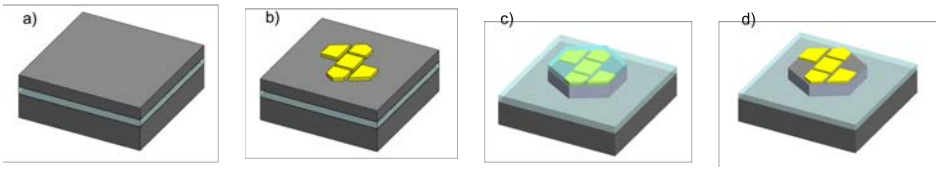

Figure A.2: Schematical representation of the microfabrication steps of hexagon test structures. a) Starting SOI wafer, b) metal (Ti+W) deposition and patterning, c) passivation oxide deposition and reactive ion etching of oxide and device layer of the SOI, d) final microstructure of a single hexagon after etching the passivation (to be done after Si NWs growth).

used both as a protection of the metal layer during Si NWs growth and as a hard mask for the reactive ion etching of the 3 µm thick device Si layer, for which a second photolithographic mask is used. In this way, the final hexagon structures are defined, which are electrically isolated from each other by the buried oxide layer of the SOI wafer. Finally, the wafer is diced into chips of 1x1 cm^2.

Figure A.3a shows a scanning electron microscope (SEM) image of the hexagons including the metal pads that allow to make 4 wire measurements. Figure A.3b shows a single Si NW grown between the <111> walls bridging two hexagons. Single NWs are grown using the same CVD-VLS conditions than for the µTEGs. However, a colloidal deposition method is used for depositing the required gold nanoparticles instead of the galvanic displacement method previously explained. This colloidal method provides a much less dense particle distribution precluding the formation of arrays. The probability of obtaining Si NWs in the area of interest is, of course, reduced but their singularity is promoted. Increasing the chances of getting bridging single NWs in the right place is the reason behind having so many hexagons per chip. Details of the growth method and preliminary characterization results obtained with these test microplatforms can be found in Ref [83].

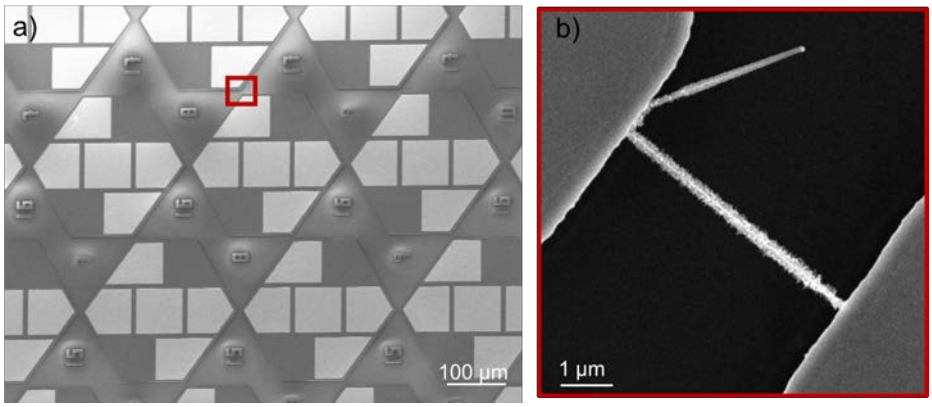

Figure A.3: a) SEM image of the fabricated hexagon structures. b) Close up image showing a single Si NW grown in between the <111> walls of two hexagon structures. A thinner Si device layer and a sparser gold nanoparticles distribution were used for minimizing the chances of having multiple bridging NWs.

Appendix B

Studies to increase the fabrication yield

B.1 Cleaving of the wafer

In the fabrication sequence of the µTEG explained in Section 3.3, it is stated that the wafer is diced into chips and KOH step is applied at chip level. The reason of dicing before KOH is to avoid breaking of the thin nitride membrane during the dicing since DI water is dispensed on the wafer to wash away particles (Si dust) and to provide lubrication and cooling. Generally, the wafer is protected with photoresist to minimize the damage that might appear on the devices during the dicing process. Both water jetting while dicing and pre-coating the wafer might harm the fragile nitride membrane and decrease the fabrication yield. To prevent this, wafers are diced before releasing the membrane and KOH process is applied at chip level after dicing. Even though the etch is not done one by one with individual chips (usually 10 chips simultaneously), it requires much longer times compared to etching the whole wafer at a time.

To overcome the abovementioned problems, an alternative to dicing has been studied during this thesis. The aim was to be able to mechanically cleave the chips easily without needing any protection on the wafer. For this purpose, the backside DRIE mask has been slightly modified to include the cleaving lines enclosing the chips. These lines are also etched during the DRIE step for the etching of the bulk Si of SOI wafer. Different line widths are included in the

mask to examine the optimum width for the etch so that it could be cleaved easily. It is known that DRIE process progresses slower on the smaller openings. Therefore, these narrow lines were not expected to be etched totally during the etch of large area cavities under the suspended platform. These lines were aimed to be used for easy cleaving of the wafer without damaging the chips. In this way, KOH process could be applied at wafer level.

Figure B.1 shows the DRIE mask designed for the cleaving test. In order to be able to decide on the optimum depth of the etch for the cleaving, lines with different widths are included from 5 to 120 µm (to be compared with the typical 1 mm side dimension of the µTEG cavities). If they were too wide, the attained etched depth would be too large, thus weakening prematurely the wafer. If they were too narrow, the etch would be too shallow and it could be difficult to cleave them without damaging the devices.

DRIE etch uniformity can also be seen from Figure B.1. DRIE process is conducted using Alcatel-AMS 110 deep-reactive ion etching system, and the etch time is defined as 1 h 22 min to etch 500 µm of Si. The etch depth is measured after the DRIE etch from the cavities under the suspended microplatform using the confocal microscope. The etch process is set to etch the 500 µm thick Si bulk of the SOI wafer, however, non-uniformity of the etch is resulted in etching the borders of the wafer slower than the center of the wafer.

Cross-sectional SEM images taken from the edges of the chips with different line widths can be seen from Figure B.2. The images are taken after the cleaving to be able to observe the etch depth of DRIE process. The areas between the green cursors feature the scalloping effect produced by the DRIE process. Therefore, the height of these areas shows how deep the etch progress for the lines with different widths for the same etching time. Etch depths with respect to line widths are represented in Figure B.3. It has been observed that the etch depth is starting to saturate for line widths of about 80-90 µm.

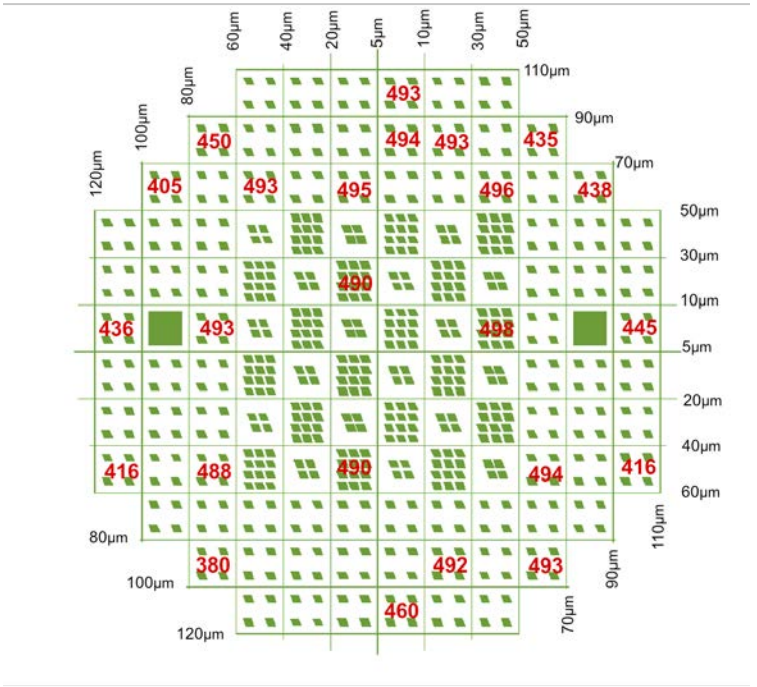

Figure B.1: DRIE mask layout including the cavities from the original mask and the cleaving lines on the edges of each chip. The width of each line is indicated. The numbers in red show the average DRIE etch depth in the cavities from that specific chip.

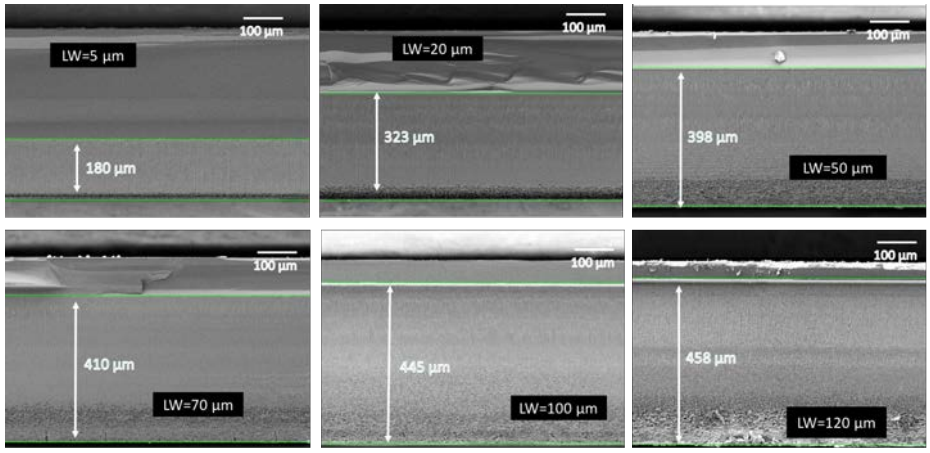

Figure B.2: Cross-sectional SEM images taken from the cleaved edges of the chips with different line widths. Line widths are displayed as LW on each image

KOH has been applied on this first trial wafer after DRIE process. After etching with KOH during 30 min using special wafer holders to protect the backside of the wafer, the wafer came out in 3-4 pieces, which were broken following the widest cleaving lines. However, the etch was performed successfully and the Si under the nitride membrane was totally opened. Cleaving of these pieces into chips following the lines was achieved quite easily without damaging the devices. Under the light of this information, the next step is to design the mask with a narrower line width to prevent breaking of the wafer during KOH step.

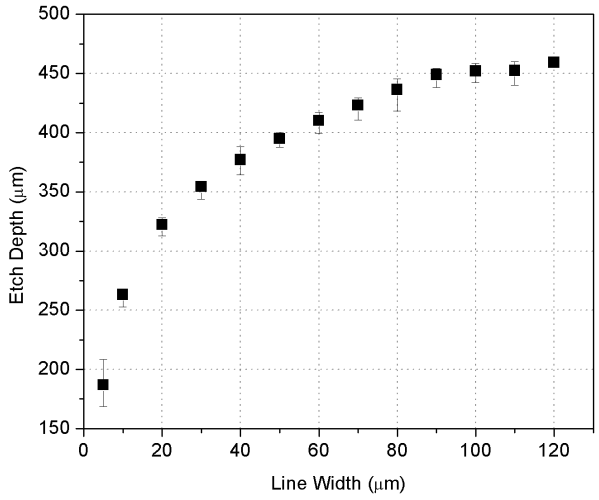

Figure B.3: Etch depth measured from the SEM images for different cleaving line widths.

B.2 Stress analysis of the device layers

During the fabrication of the μTEG, some of the wafers were broken at intermediate steps of fabrication. This could occur due to inattentive handling during the fabrication processing steps and/or the presence of high stress in the wafers. In one of the fabrication runs including 4 wafers, all wafers were broken and the responsible crack started from the same point. This raised doubts about the contribution of aforementioned causes and a stress analysis on the wafers has been conducted for the following fabrications.

Stress in thin films results from two significant contributions; thermal and intrinsic stress. Thermal stress arises from the deposition temperature. If the deposition takes place at high temperatures (higher than room temperature), differences in thermal expansion coefficients of the substrate and the thin film cause a thermal stress when they cool down. Deposition of thin films (oxide and nitride layers) during this thesis are realized at high temperatures. For the nitride layer, low-pressure CVD system is used which is known the result in high stress thin films due to its high deposition temperatures

(*ca* 800 °). For the deposition of oxide layers, plasma-enhanced CVD system is used to be able to make depositions at lower temperatures with the help of the plasma (*ca* 400 °).

The Stoney formula is generally used to calculate the stress in thin films:

$$\sigma = \frac{E_s}{6(1-v_s)} \frac{h_s^2}{h_f} \left(\frac{1}{R} - \frac{1}{R_0} \right) \tag{B.1}$$

where E_s is the Young´s modulus, v_s is the Poisson´s ratio (assumed as 0.28 for this study), h_s is the thickness of the substrate, and h_f is the thickness of the thin film. R_0 and R are the radii of curvature before and after the deposition of the thin film, respectively. The Stoney formula requires the following assumptions [118], [119]:

- the thicknesses of the both the substrate and the thin film are uniform and isotropic;
- the thickness of the thin film is smaller than the thickness of the substrate;
- the deformations and the rotations are infinitesimal;
- the radius of curvature is equal in all directions (spherical deformation);
- the stress and the radius of curvature are constant over the plate system´s surface.

This formula is applied frequently even though the last two requirements are often violated in practice.

To be able to determine the film stress, curvatures of the substrate both before and after the film deposition are measured using Sensofar confocal microscope.The total scan length of the initial wafer profiles was 7.5 cm taken at 90° increments. This was done to map the changes in curvature over a large portion of the wafer surface. The scan speed and the sampling rate were chosen to ensure clean data and to keep the total number of data points within a reasonable size (1 point/µm.) If the curvature plot obtained from the measurement (measured distance along the substrate vs height of the substrate) is

defined by the function $y = f(x)$, the local radius of curvature can be determined using the following formula:

$$R(x) = \frac{(1 + y'^2)^{3/2}}{y''} \tag{B.2}$$

where y' and y'' are the first and second order derivatives of y, respectively.

Figure B.4 demonstrates the steps of calculation of the stress for a thin film. The function $y = f(x)$ is defined by applying the 5^{th} degree polynomial fit on the curvature graph obtained from the confocal microscope (Figure B.4a-c). This allows for the curvature to be calculated at any radial position. Next, first and second order derivatives of the fit are obtained by a numerical method and inserted into Eqn. B.2 to calculate the radius of curvature at each point both before and after the thin film deposition (Figure B.4b-d). Finally, stress at each point of the thin film is calculated using Eqn. B.1, assuming E_s value of 230 GPa for (100) oriented Si wafers [120] (Figure B.4e). These steps are repeated after each layer deposition to determine the stress of both thin film and the substrate.

Figure B.5 shows the curvatures of the wafers at the initial steps of the fabrication. Figure B.5a corresponds to a test (bulk) wafer to be able to calculate the stress of the LPCVD nitride (Si_3N_4) layer. Since it has been deposited on both sides of the wafer, the backside nitride layer is etched using a RIE process. The stress of the 300 nm thick LPCVD nitride layer is calculated to be 976 MPa (tensile) following the above mentioned method. This stress can be modified by changing the ratio of precursors (and hence the stoichiometry of the resulting nitride thin film) during the deposition and it is in agreement with the stress values reported in the literature [121]. Figure B.5b studies the effect of the doping on the nitride thin film stress. Since our fabrication requires local doping of the SOI wafer, the idea was to decrease the stress by including the nitride layer during the doping step. It has been observed that keeping the nitride on both sides while doping only the top side decreased the curvature compared to leaving nitride without doping only on one side. However, when nitride at both sides are doped, smaller curvatures were obtained (See steps 3 and 4 of Figure B.5b). The stress of doped nitride layer is calculated to be 484 MPa, which is almost half of the stress of the

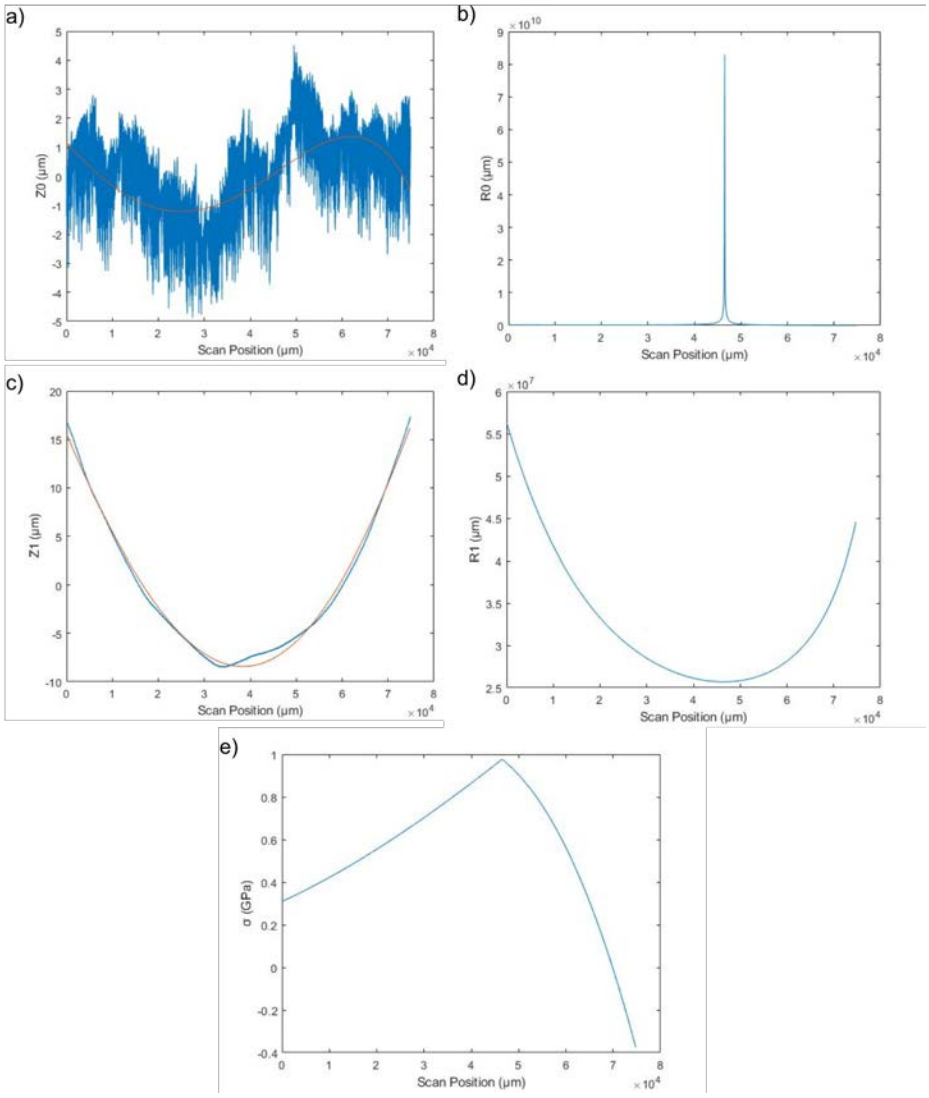

Figure B.4: Representative steps of the stress calculation for thin films. Curvature graphs obtained from confocal microscope before (a) and after (c) the deposition and fitting with 5^{th} degree polynomial. Radius of curvature plots calculated before (b) and after (d) the thin film deposition. e) Stress calculated by inserting calculated radius of curvatures and the material constants into Stoney´s equation.

undoped nitride layer.

Since our fabrication processes are carried out starting with SOI wafers, a compressive stress is observed due to the 1.5 µm thick buried oxide between the device layer and bulk Si of the SOI. The curvature of the SOI wafer is shown in Figure B.5c. It is not possible to determine the stress of the starting SOI wafers since we don´t have the initial curvature data (R_0), but this large curvature reflects the high possibility of breaking the wafer during the fabrication steps. This curvature remains the same after the symmetric deposition of nitride layer. Normally, we deposit 3.5 µm thick passivation oxide on the backside of our wafers as a mask for DRIE etching of bulk Si of SOI wafer. It happens that this step decreased the curvature of the wafer significantly (See step 3 of Figure B.5c). However, this process took place at the final step of the fabrication which increased the risk of breaking the wafer in the mid-steps such as the passivation oxide deposition on the top side that will increase the curvature of the wafer in the same direction. For this reason, the fabrication sequence is modified to deposit this DRIE mask oxide at the initial steps (after the nitride deposition). A compressive stress of 169 MPa is calculated for this 3.5 µm thick oxide layer deposited using PECVD. Curvature measurements are also applied at each step of the fabrication, however, no significant stress involvement is observed. This amendment in processing steps eliminated the breaking of the wafers due to the high starting stress of the wafers.

The curvatures of SOI wafers with different buried oxide/device layer thickness combinations were also measured and presented in Figure B.6. All curvatures are bowed concave downwards because of the compressive intrinsic stress of buried oxide, resulting in a negative curvature. The highest curvature is observed at the center of the wafer, the slight shifts in the figure is due to the different scan starting positions. As stated before, it is not possible to determine the exact stress values using Stoney´s formula on account of the lack of initial curvature information. There is no regular trend of curvature following the buried oxide/device layer thickness combinations since all measured SOI wafers have different doping levels and crystal orientations. However, the lowest curvature is obtained from the case with the thinnest buried oxide/thickest device layer thickness combination.

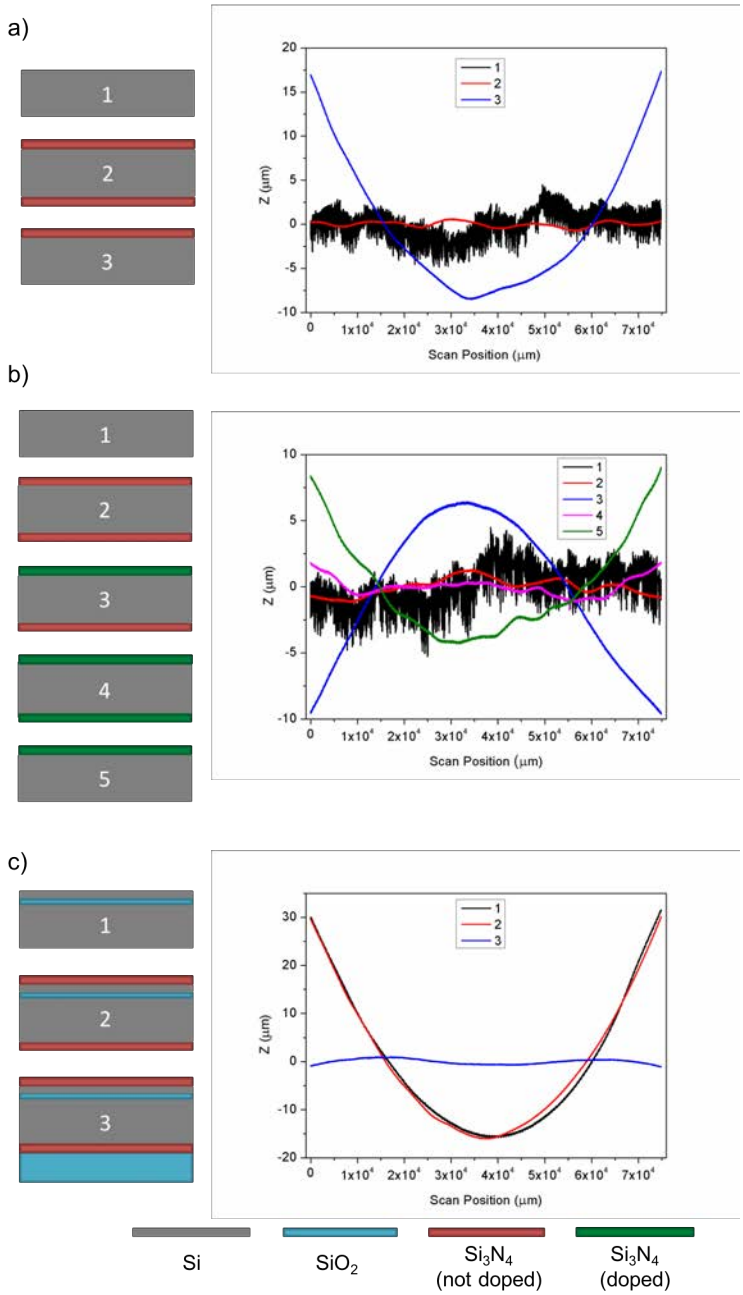

Figure B.5: Schematics of the layers present (left) and corresponding curvature measurements (right).

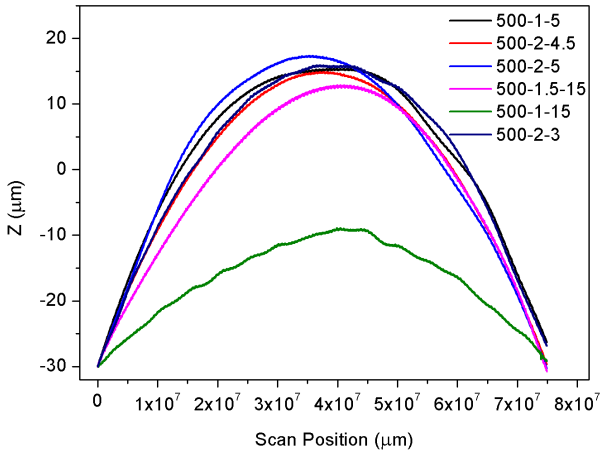

Figure B.6: Curvatures of the SOI wafers with different buried oxide/device layer combinations. Numbers in the label correspond to Si bulk thickness-buried oxide thickness-device layer thickness.

Bibliography

[1] P. Newman, "The internet of Things 2018," BI Intelligence, Tech. Rep., 2018.

[2] McKinsey&Company, "The Internet of Things:Mapping the value beyond the hype," Tech. Rep., 2015.

[3] GSM Association, "Understanding the Internet of Things (IoT)," Tech. Rep., 2014.

[4] R. J. Vullers, R. van Schaijk, I. Doms, C. Van Hoof, and R. Mertens, "Micropower energy harvesting," *Solid-State Electronics*, vol. 53, pp. 684–693, 2009.

[5] J. I. Fondazione and B. Kessler, "Microsystem based Energy Harvesting (EH-MEMS): Powering pervasivity of the Internet of Things (IoT) A review with focus on mechanical vibrations," *Journal of King Saud University - Science (Article in Press)*, 2017.

[6] G. Snyder and E. Toberer, "Complex thermoelectric materials," *Nature Materials*, vol. 7, pp. 105–114, 2008.

[7] D. M. Rowe, *Thermoelectrics Handbook:Macro to Nano*. Taylor&Francis Group, 2006.

[8] A. V. Shevelkov, "Thermoelectric Power Generation by Clathrates," in *Thermoelectrics for power generation*, 2016, pp. 239–261.

[9] L. M. Cowen, J. Atoyo, M. J. Carnie, D. Baran, and B. C. Schroeder, "Organic Materials for Thermoelectric Energy Generation," *ECS Journal of Solid State Science and Technology*, vol. 6, no. 3, pp. 3080–3088, 2017.

[10] O. Caballero-Calero and R. D'Agosta, "Review—Towards the Next Generation of Thermoelectric Materials: Tailoring Electronic and Phononic Properties of Nanomaterials," *ECS Journal of Solid State Science and Technology*, vol. 6, no. 3, pp. 3065–3079, 2017.

[11] M. Rull-Bravo, A. Moure, J. F. Fernández, and M. Martín-González, "Skutterudites as thermoelectric materials: revisited," *RSC Adv.*, vol. 5, pp. 41 653–41 667, 2015.

[12] Z. H. Ge, L. D. Zhao, D. Wu, X. Liu, B. P. Zhang, J. F. Li, and J. He, "Low-cost, abundant binary sulfides as promising thermoelectric materials," *Materials Today*, vol. 19, no. 4, pp. 227–239, 2016.

[13] H. Wang, W. Su, J. Liu, and C. Wang, "Recent development of n-type perovskite thermoelectrics," *Journal of Materiomics*, vol. 2, pp. 225–236, 2016.

[14] W. Liu, K. Yin, Q. Zhang, C. Uher, and X. Tang, "Eco-friendly high-performance silicide thermoelectric materials," *National Science Review*, vol. 0, pp. 1–16, 2017.

[15] R. L. Cataldo and G. L. Bennett, "U.S. Space Radioisotope Power Systems and Applications: Past, Present and Future," NASA Glenn Research Center, Tech. Rep., 2011.

[16] J. Loureiro, N. Neves, R. Barros, T. Mateus, R. Santos, S. Filonovich, S. Reparaz, C. M. Sotomayor-Torres, F. Wyczisk, L. Divay, R. Martins, and I. Ferreira, "Transparent aluminium zinc oxide thin films with enhanced thermoelectric properties," *Journal of Materials Chemistry A*, vol. 2, pp. 6649–6655, 2014.

[17] P. Fan, Y. Z. Li, Z. H. Zheng, Q. Y. Lin, J. T. Luo, G. X. Liang, M. Q. Zhang, and M. C. Chen, "Thermoelectric properties optimization of Al-doped ZnO thin films prepared by reactive sputtering Zn-Al alloy target," *Applied Surface Science*, vol. 284, pp. 145–149, 2013.

[18] J. Yang, L. Xi, W. Qiu, L. Wu, X. Shi, L. Chen, J. Yang, W. Zhang, C. Uher, and D. J. Singh, "On the tuning of electrical and thermal transport in thermoelectrics: an integrated theory–experiment perspective," *npj-Computational Materials*, vol. 2, no. 15015, 2016.

[19] M. S. Dresselhaus, G. Chen, M. Y. Tang, R. Yang, H. Lee, D. Wang, Z. Ren, J. P. Fleurial, and P. Gogna, "New directions for low-dimensional thermoelectric materials," *Advanced Materials*, vol. 19, pp. 1043–1053, 2007.

[20] I. D. Hicks and M. S. Dresselhaus, "Thermoelectric figure of merit of a one-dimensional conductor," *Physical Review B*, vol. 47, no. 15, 1993.

[21] B. Russ, A. Glaudell, J. J. Urban, M. L. Chabinyc, and R. A. Segalman, "Organic thermoelectric materials for energy harvesting and temperature control," *Nature Reviews Materials*, vol. 1, pp. 1–14, 2016.

[22] Y. Sun, P. Sheng, C. Di, F. Jiao, W. Xu, D. Qiu, and D. Zhu, "Organic thermoelectric materials and devices based on p- and n-type poly(metal 1,1,2,2-ethenetetrathiolate)s," *Advanced Materials*, vol. 24, no. 14, p. 1781, 2012.

[23] C. A. Hewitt, A. B. Kaiser, S. Roth, M. Craps, R. Czerw, and D. L. Carroll, "Multilayered carbon nanotube/polymer composite based thermoelectric fabrics," *Nano Letters*, vol. 12, 13071310, 2012.

[24] O. Bubnova, Z. U. Khan, A. Malti, S. Braun, M. Fahlman, M. Berggren, and X. Crispin, "Optimization of the thermoelectric figure of merit in the conducting polymer poly(3,4-ethylenedioxythiophene)," *Nature Materials*, vol. 10, pp. 429–433, 2011.

[25] X. Zhang and L.-D. Zhao, "Thermoelectric materials: Energy conversion between heat and electricity," *Journal of Materiomics*, vol. 1, pp. 92–105, 2015.

[26] D. Narducci, S. Frabboni, and X. Zianni, "Silicon de novo: energy filtering and enhanced thermoelectric performances of nanocrystalline silicon and silicon alloys," *Journal of Materials Chemistry C*, vol. 3, pp. 12 176–12 185, 2015.

[27] A. P. Perez-Marín, A. F. Lopeandía, L. Abad, P. Ferrando-Villaba, G. Garcia, A. M. Lopez, F. X. Muñoz-Pascual, and J. Rodríguez-Viejo, "Micropower thermoelectric generator from thin Si membranes," *Nano Energy*, vol. 4, pp. 73–80, 2014.

[28] M. Strasser, R. Aigner, C. Lauterbach, T. F. Sturm, M. Franosch, and G. Wachutka, "Micromachined CMOS thermoelectric generators as on-chip power supply," *Sensors and Actuators A*, vol. 114, pp. 362–370, 2004.

[29] G. Gesele, J. Linsmeier, V. Drach, J. Fricke, and R. Arens-Fischer, "Temperature-dependent thermal conductivity of porous silicon," *Journal of Physics D: Applied Physics*, vol. 30, no. 3097, pp. 2911–2911, 1997.

[30] J. Boor, D. S. Kim, X. Ao, M. Becker, N. F. Hinsche, I. Mertig, P. Zahn, and V. Schmidt, "Thermoelectric properties of porous silicon," *Applied Physics A*, vol. 107, no. 4, pp. 789–794, 2012.

[31] J. K. Yu, S. Mitrovic, D. Tham, J. Varghese, and J. R. Heath, "Reduction of thermal conductivity in phononic nanomesh structures," *Nature Nanotechnology*, vol. 5, pp. 718–721, 2010.

[32] J. Tang, H. T. Wang, D. H. Lee, M. Fardy, Z. Huo, T. P. Russell, and P. Yang, "Holey silicon as an efficient thermoelectric material," *Nano Letters*, vol. 10, no. 10, pp. 4279–4283, 2010.

[33] J. Lim, H. T. Wang, J. Tang, S. C. Andrews, H. So, J. Lee, D. H. Lee, T. P. Russell, and P. Yang, "Simultaneous thermoelectric property measurement and incoherent phonon transport in holey silicon," *ACS Nano*, vol. 10, no. 1, pp. 124–132, 2016.

[34] G. Pennelli and M. Macucci, "High-power thermoelectric generators based on nanostructured silicon," *Semiconductor Science and Technology*, vol. 31, no. 054001, 2016.

[35] S. P. Ashby, T. Bian, H. Ning, M. J. Reece, and Y. Chao, "Thermal Diffusivity of SPS Pressed Silicon Powders and the Potential for Using Bottom–Up Silicon Quantum Dots as a Starting Material," *Journal of Electronic Materials*, vol. 44, no. 6, pp. 1931–1935, 2015.

[36] A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J. K. Yu, W. A. Goddard, and J. R. Heath, "Silicon nanowires as efficient thermoelectric materials," *Nature*, vol. 451, pp. 168–171, 2008.

[37] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, "Enhanced thermoelectric performance of rough silicon nanowires," *Nature*, vol. 451, pp. 163–168, 2008.

[38] J. Choi, K. Cho, and S. Kim, "Flexible Thermoelectric Generators Composed of n-and p-Type Silicon Nanowires Fabricated by Top-Down Method," *Advanced Energy Materials*, vol. 7, no. 1602138, 2017.

[39] Y. Li, K. Buddharaju, N. Singh, G. Q. Lo, and S. J. Lee, "Chip-level thermoelectric power generators based on high-density silicon nanowire array prepared with top-down CMOS technology," *IEEE Electron Device Letters*, vol. 32, no. 5, pp. 674–676, 2011.

[40] B. M. Curtin, E. W. Fang, and J. E. Bowers, "Highly ordered vertical silicon nanowire array composite thin films for thermoelectric devices," *Journal of Electronic Materials*, vol. 1408, 2012.

[41] B. M. Curtin and J. E. Bowers, "Thermoelectric Properties of Silicon Nanowire Array and Spin-on Glass Composites Fabricated with CMOS-compatible Techniques," in *Materials Research Society Symposia Proceedings*, 2012.

[42] M. Jang, Y. Park, Y. Hyun, M. Jun, S.-J. Choi, T. Zyung, and J.-D. Kim, "Top-Down Processed Silicon Nanowires for Thermoelectric Applications," *Journal of Nanoscience and Nanotechnology*, vol. 12, pp. 3552–3554, 2012.

[43] A. Stranz, J. Kähler, S. Merzsch, A. Waag, and E. Peiner, "Nanowire silicon as a material for thermoelectric energy conversion," *Microsystem Technologies*, vol. 18, pp. 857–862, 2012.

[44] S. J. Kim, W. C. Choi, T. H. Zyung, and M. G. Jang, "Thermoelectric properties of 50-nm-wide n- and p- type silicon nanowires," *Applied Physics A*, vol. 120, pp. 265–269, 2015.

[45] E. Dimaggio and G. Pennelli, "Potentialities of silicon nanowire forests for thermoelectric generation," *Nanotechnology - Accepted Manuscript*, 2018.

[46] B. Xu, W. Khouri, and K. Fobelets, "Two-Sided silicon nanowire array/bulk thermoelectric power generator," *IEEE Electron Device Letters*, vol. 35, no. 5, pp. 596–598, 2014.

[47] B. Xu and K. Fobelets, "Spin-on-doping for output power improvement of silicon nanowire array based thermoelectric power generators," *Journal of Applied Physics*, vol. 115, no. 214306, 2014.

[48] T. Zhang, S.-l. Wu, R.-t. Zheng, and G.-a. Cheng, "Significant reduction of thermal conductivity in silicon nanowire arrays," *Nanotechnology*, vol. 24, no. 505718, 2013.

[49] K. Y. Lee, D. Brown, S. Kumar, and G. W. Woodruff, "Performance Evaluation of Silicon Nanowire Arrays Based Thermoelectric Generators," *14th IEEE ITHERM Conference*, no. 1394, 2014.

[50] K. Y. Lee, D. Brown, and S. Kumar, "Silicon Nanowire Arrays Based On-Chip Thermoelectric Generators," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 5, no. 8, pp. 1100–1107, 2015.

[51] Y. Li, K. Buddharaju, N. Singh, and S. J. Lee, "Top-down silicon nanowire-based thermoelectric generator: Design and characterization," *Journal of Electronic Materials*, vol. 41, no. 6, pp. 989–992, 2012.

[52] M. Totaro, P. Bruschi, and G. Pennelli, "Top down fabricated silicon nanowire networks for thermoelectric applications," *Microelectronic Engineering*, vol. 97, pp. 157–161, 2012.

[53] G. Pennelli and M. Piotto, "Fabrication and characterization of silicon nanowires with triangular cross section," *Journal of Applied Physics*, vol. 100, no. 054507, 2006.

[54] G. Pennelli, M. Totaro, M. Piotto, and P. Bruschi, "Seebeck coefficient of nanowires interconnected into large area networks," *Nano Letters*, vol. 13, 25922597, 2013.

[55] G. Pennelli, "Top down fabrication of long silicon nanowire devices by means of lateral oxidation," *Microelectronic Engineering*, vol. 86, pp. 2139–2143, 2009.

[56] G. Pennelli, M. Totaro, and M. Piotto, "Selective doping of silicon nanowires by means of electron beam stimulated oxide etching," *Nano Letters*, vol. 12, 10961101, 2012.

[57] T. Watanabe, S. Asada, T. Xu, S. Hashimoto, S. Ohba, Y. Himeda, R. Yamato, H. Zhang, M. Tomita, T. Matsukawa, Y. Kamakura, and H. Ikeda, "A scalable Si-based micro thermoelectric generator," in *IEEE Electron Devices Technology and Manufacturing Conference, EDTM 2017 Proceedings*, 2017.

[58] G. F. Cerofolini, M. Ferri, E. Romano, F. Suriano, G. P. Veronese, S. Solmi, and D. Narducci, "Crossbar architecture for tera-scale integration," *Semiconductor Science and Technology*, vol. 26, no. 045005, 2011.

[59] G. F. Cerofolini, M. Ferri, E. Romano, A. Roncaglia, E. Selezneva, A. Arcari, F. Suriano, G. P. Veronese, S. Solmi, and D. Narducci, "Industrially Scalable Process for Silicon Nanowires for Seebeck Generation," *Proceedings of the 8th European Conference on Thermoelectrics (ECT)*, pp. 147–151, 2010.

[60] G. F. Cerofolini, M. Ferri, E. Romano, F. Suriano, G. P. Veronese, S. Solmi, and D. Narducci, "Terascale integration via a redesign of the crossbar based on a vertical arrangement of poly-Si nanowires," *Semiconductor Science and Technology*, vol. 25, no. 095011, 2010.

[61] M. Ferri, F. Suriano, A. Roncaglia, S. Solmi, G. F. Cerofolini, E. Romano, and D. Narducci, "Ultradense silicon nanowire arrays produced via top-down planar technology," *Microelectronic Engineering*, vol. 88, pp. 877–881, 2011.

[62] D. Dávila, A. Tarancón, D. Kendig, M. Fernández-Regúlez, N. Sabaté, M. Salleras, C. Calaza, C. Cané, I. Gràcia, E. Figueras, J. Santander, A. San Paulo, A. Shakouri, and L. Fonseca, "Planar thermoelectric microgenerators based on silicon nanowires," *Journal of Electronic Materials*, vol. 40, no. 5, pp. 851–855, 2011.

[63] D. G. Cahill, P. V. Braun, G. Chen, D. R. Clarke, S. Fan, K. E. Goodson, P. Keblinski, W. P. King, G. D. Mahan, A. Majumdar, H. J. Maris, S. R. Phillpot, E. Pop, and L. Shi, "Nanoscale thermal transport. II. 2003-2012," *Applied Physics Reviews*, vol. 1, no. 011305, 2014.

[64] D. M. Rowe, "Applications of nuclear-powered thermoelectric generators in space," *Applied Energy*, vol. 40, p. 241 271, 1991.

[65] J. A. Perez-Taborda, M. Muñoz Rojo, J. Maiz, N. Neophytou, and M. Martin-Gonzalez, "Ultra-low thermal conductivities in large-area Si-Ge nanomeshes for thermoelectric applications," *Scientific Reports*, vol. 6, no. 32778, 2016.

[66] H. Lee, D. Vashaee, D. Z. Wang, M. S. Dresselhaus, Z. F. Ren, and G. Chen, "Effects of nanoscale porosity on thermoelectric properties of SiGe," *Journal of Applied Physics*, vol. 107, no. 094308, 2010.

[67] C. K. Liu, C. K. Yu, H. C. Chien, S. L. Kuo, C. Y. Hsu, M. J. Dai, G. L. Luo, S. C. Huang, and M. J. Huang, "Thermal conductivity of Si/SiGe superlattice films," *Journal of Applied Physics*, vol. 104, no. 114301, 2008.

[68] T. M. Tritt and M. A. Subramanian, "Thermoelectric Materials, Phenomena, and Applications: A Bird's Eye View," *MRS Bulletin*, vol. 31, pp. 188–194, 2006.

[69] M. Kishi, H. Nemoto, T. Hamao, M. Yamamoto, S. Sudou, M. Mandai, and S. Yamamoto, "Micro thermoelectric modules and their application to wristwatches as an energy source," in *Eighteenth International Conference on Thermoelectrics (ICT) Proceedings,*, 1999, pp. 301–307.

[70] S. B. Riffat and X. Ma, "Thermoelectrics: A review of present and potential applications," *Applied Thermal Engineering*, vol. 23, pp. 913–935, 2003.

[71] W. Liu, Q. Jie, H. S. Kim, and Z. Ren, "Current progress and future challenges in thermoelectric power generation: From materials to devices," *Acta Materialia*, vol. 87, pp. 357–376, 2015.

[72] J. P. Carmo, L. M. Gonçalves, and J. H. Correia, "Micro and nanodevices for thermoelectric converters," *Scanning Probe Microscopy in Nanoscience and Nanotechnology*, vol. 2, pp. 791–812, 2010.

[73] K. Ziouche, Z. Yuan, P. Lejeune, T. Lasri, D. Leclercq, and Z. Bougrioua, "Silicon-Based Monolithic Planar Micro Thermoelectric Generator Using Bonding Technology," *Journal of Microelectromechanical Systems*, vol. 26, no. 1, pp. 45–47, 2017.

[74] L. Fonseca, J. D. Santos, A. Roncaglia, D. Narducci, C. Calaza, M. Salleras, I. Donmez, A. Tarancon, A. Morata, G. Gadea, L. Belsito, and L. Zulian, "Smart integration of silicon nanowire arrays in all-silicon thermoelectric micro-nanogenerators," *Semiconductor Science and Technology*, vol. 31, no. 084001, 2016.

[75] D. Dávila, A. Tarancón, C. Calaza, M. Salleras, M. Fernández-Regúlez, A. San Paulo, and L. Fonseca, "Monolithically integrated thermoelectric energy harvester based on silicon nanowire arrays for powering micro/nanodevices," *Nano Energy*, vol. 1, pp. 812–819, 2012.

[76] J. Su, V. Leonov, M. Goedbloed, Y. Van Andel, M. C. De Nooijer, R. Elfrink, Z. Wang, and R. J. Vullers, "A batch process micromachined thermoelectric energy harvester: Fabrication and characterization," *Journal of Micromechanics and Microengineering*, vol. 20, no. 104005, 2010.

[77] B. Xu, C. Li, M. Myronov, and K. Fobelets, "n-Si–p-Si(1-x)Gex nanowire arrays for thermoelectric power generation," *Solid State Electronics*, vol. 83, pp. 107–112, 2013.

[78] Davila D., "Monolithic integration of VLS silicon nanowires into planar thermoelectric microgenerators," PhD thesis, Universitat Autonoma de Barcelona, 2011.

[79] Y. Hyun, Y. Park, W. Choi, J. Kim, T. Zyung, and M. Jang, "Evaluation of Seebeck coefficients in n- and p-type silicon nanowires fabricated by complementary metal-oxide-semiconductor technology," *Nanotechnology*, vol. 23, no. 405707, 2012.

[80] D. Dávila, A. Tarancón, C. Calaza, M. Salleras, M. Fernández-Regúlez, A. S. Paulo, and L. Fonseca, "Improved thermal behavior of multiple linked arrays of silicon nanowires integrated into planar thermoelectric microgenerators," *Journal of Electronic Materials*, vol. 42, no. 7, pp. 1918–1925, 2013.

[81] G. Gadea, A. Morata, J. D. Santos, D. Davila, C. Calaza, M. Salleras, L. Fonseca, and A. Tarancon, "Towards a full integration of vertically aligned silicon nanowires in MEMS using silane as a precursor," *Nanotechnology*, vol. 26, no. 195302, 2015.

[82] M. S. Islam, S. Sharma, T. I. Kamins, and R. S. Williams, "A novel interconnection technique for manufacturing nanowire devices," *Applied Physics A: Materials Science and Processing*, vol. 80, pp. 1133–1140, 2005.

[83] G. Gadea, "Integration of Si/Si-Ge nanostructures in microthermoelectric generators," PhD thesis, University of Barcelona, 2017.

[84] C. Carraro, R. Maboudian, and L. Magagnin, "Metallization and nanostructuring of semiconductor surfaces by galvanic displacement processes," *Surface Science Reports*, vol. 62, pp. 499–525, 2007.

[85] L. Schubert, P. Werner, N. D. Zakharov, G. Gerth, F. Kolb, Long L., Gösele U., and Tan T.Y., "Silicon nanowhiskers grown on Si substrates by molecular-beam epitaxy," *Applied Physics Letters*, vol. 84, no. 24, pp. 4968–4970, 2004.

[86] N. Wang, Y. Cai, and R. Q. Zhang, "Growth of nanowires," *Materials Science and Engineering R: Reports*, vol. 60, pp. 1–51, 2008.

[87] M. O. Orlandi, P. H. Suman, R. A. Silva, and E. P. S. Arlindo, "Carbothermal Reduction Synthesis: An Alternative Approach to Obtain Single-Crystalline Metal Oxide Nanostructures," in *Recent Advances in Complex Functional Materials*, E. Longo and F. La Porta, Eds., Springer International Publishing, 2017.

[88] T. Kamins, R. Williams, D. Basile, T. Hesjedal, and J. Harris, "Ti-catalyzed Si nanowires by chemical vapor deposition: Microscopy and growth mechanisms," *Journal of Applied Physics*, vol. 89, no. 2, pp. 1008–1016, 2001.

[89] S. Wagesreither, E. Bertagnolli, S. Kawase, Y. Isono, and A. Lugstein, "Electrostatic actuated strain engineering in monolithically integrated VLS grown silicon nanowires," *Nanotechnology*, vol. 25, no. 455705, 2014.

[90] M. Fernandez-Regulez, M. Sansa, M. Serra-Garcia, E. Gil-Santos, J. Tamayo, F. Perez-Murano, and A. San Paulo, "Horizontally patterned Si nanowire growth for nanomechanical devices," *Nanotechnology*, vol. 24, no. 095303, 2013.

[91] H.-J. Choi, *Semiconductor Nanostructures for Optoelectronic Devices*, Gyu-Chul Yi, Ed. Springer Berlin Heidelberg, 2012.

[92] E. Krali and Z. A. K. Durrani, "Seebeck coefficient in silicon nanowire arrays," *Applied Physics Letters*, vol. 102, no. 143102, 2013.

[93] J. Sadhu, H. Tian, J. Ma, B. Azeredo, J. Kim, K. Balasundaram, C. Zhang, X. Li, P. M. Ferreira, and S. Sinha, "Quenched phonon drag in silicon nanowires reveals significant effect in the bulk at room temperature," *Nano Letters*, vol. 15, no. 5, pp. 3159–3165, 2015.

[94] J. Sadhu Swaroop, "Effect of Phonon Transport on the Seebeck Coefficient and Thermal Conductivity of A," PhD thesis, University of Illinois at Urbana-Champaign, 2014.

[95] A. Stranz, J. Kähler, A. Waag, and E. Peiner, "Thermoelectric properties of high-doped silicon from room temperature to 900 K," *Journal of Electronic Materials*, vol. 42, no. 7, pp. 2381–2387, 2013.

[96] M. Jang, Y. Park, M. Jun, Y. Hyun, S. J. Choi, and T. Zyung, "The Characteristics of Seebeck Coefficient in Silicon Nanowires Manufactured by CMOS Compatible Process," *Nanoscale Research Letters*, vol. 5, pp. 1654–1657, 2010.

[97] G. A. Slack and M. A. Hussain, "The maximum possible conversion efficiency of silicongermanium thermoelectric generators," *Journal of Applied Physics*, vol. 70, no. 5, pp. 2694–2718, 1991.

[98] J. A. Martinez, P. P. Provencio, S. T. Picraux, J. P. Sullivan, and B. S. Swartzentruber, "Enhanced thermoelectric figure of merit in SiGe alloy nanowires by boundary and hole-phonon scattering," *Journal of Applied Physics*, vol. 110, no. 074317, 2011.

[99] J. P. Dismukes, L. Ekstrom, E. F. Steigmeier, I. Kudman, and D. S. Beers, "Thermal and electrical properties of heavily doped Ge-Si alloys up to 1300°K," *Journal of Applied Physics*, vol. 35, pp. 2899–2907, 1964.

[100] G. Joshi, H. Lee, Y. Lan, X. Wang, G. Zhu, D. Wang, R. W. Gould, D. C. Cuff, M. Y. Tang, M. S. Dresselhaus, G. Chen, and Z. Ren, "Enhanced Thermoelectric Figure-of-Merit in Nanostructured p-type Silicon Germanium Bulk Alloys," *Nano Letters*, vol. 8, no. 12, pp. 4670–4674, 2008.

[101] T. Goto, J. H. Li, T. Hirai, Y. Maeda, R. Kato, and A. Maesono, "Measurements of the Seebeck coefficient of thermoelectric materials by an AC method," *International Journal of Thermophysics*, vol. 18, no. 2, pp. 569–577, 1997.

[102] P. D. Maycock, "Thermal conductivity of silicon, germanium, III-V compounds and III-V alloys," *Solid State Electronics*, vol. 10, pp. 161–168, 1967.

[103] Z. Yuan, K. Ziouche, Z. Bougrioua, P. Lejeune, T. Lasri, and D. Leclercq, "A planar micro thermoelectric generator with high thermal resistance," *Sensors and Actuators, A: Physical*, vol. 221, pp. 67–76, 2015.

[104] M. Z. Yang, C. C. Wu, C. L. Dai, and W. J. Tsai, "Energy harvesting thermoelectric generators manufactured using the complementary metal oxide semiconductor process," *Sensors*, vol. 13, pp. 2359–2367, 2013.

[105] J. Xie, C. Lee, and H. Feng, "Design, Fabrication, and Characterization of CMOS MEMS-Based Thermoelectric Power Generators," *Journal of Microelectromechanical Systems*, vol. 19, no. 2, pp. 317–324, 2010.

[106] Multi CB, "FR4 Standard (Data Sheet)," Tech. Rep., 2016.

[107] B. B. Kadhim, F. K. Farhan, B. Daram Balwa, and W. A. Shakir, "Thermal Properties of (TiO2 -ZnO) / PMMA Nanocomposites," *Science and Technology*, vol. 7, no. 1, pp. 1–3, 2017.

[108] M. J. Assael, S. Botsios, K. Gialou, and I. N. Metaxa, "Thermal conductivity of polymethyl methacrylate (PMMA) and borosilicate crown glass BK7," *International Journal of Thermophysics*, vol. 26, no. 5, pp. 1595–1605, 2005.

[109] Nextreme Thermal Solutions, *eTEG HV56 power generator (Data Sheet)*. [Online]. Available: `http://www.mouser.com/ds/2/292/Nextreme_eTEG_HV56_Data_Sheet-3613.pdf`.

[110] RMT Ltd., *1MD03-002-04 (Data Sheet)*, 2012. [Online]. Available: `http://www.rmtltd.ru/datasheets/1md03002.pdf`.

[111] H. Böttner, J. Nurnus, A. Gavrikov, G. Kühner, M. Jägle, C. Künzel, D. Eberhard, G. Plescher, A. Schubert, and K. H. Schlereth, "New thermoelectric components using microsystems technologies," *Journal of Microelectromechanical Systems*, vol. 13, no. 3, pp. 414–420, 2004.

[112] M. Stordeur and I. Stark, "Low Power Thermoelectric Generator -self-sufficient energy supply for micro systems," in *16th International Conference on Thermoelectric*, 1997, pp. 575–577.

[113] Micropelt Energy Harvesting, "MPG-D751 (Data Sheet)," Tech. Rep., 2014.

[114] S. Pelegrini, A. Adami, C. Collini, P. Conci, L. Lorenzelli, A. A. Pasa, and F. B. Kessler, "Simulation, design and fabrication of a planar micro thermoelectric generator," *Proceedings of SPIE, Smart Sensors, Actuators, and MEMS VI*, vol. 876322, no. 17, 2013.

[115] P. H. Kao, P. J. Shih, C. L. Dai, and M. C. Liu, "Fabrication and characterization of CMOS-MEMS thermoelectric micro generators," *Sensors*, vol. 10, pp. 1315–1325, 2010.

[116] H. Glosch, M. Ashauer, U. Pfeiffer, and W. Lang, "A thermoelectric converter for energy supply," *Sensors and Actuators*, vol. 74, pp. 246–250, 1999.

[117] Y. Li, K. Buddharaju, B. C. Tinh, N. Singh, and S. J. Lee, "Improved vertical silicon nanowire based thermoelectric power generator with polyimide filling," *IEEE Electron Device Letters*, vol. 33, no. 5, pp. 715–717, 2012.

[118] M. R. Ardigo, M. Ahmed, and A. Besnard, "Stoney Formula: Investigation of Curvature Measurements by Optical Profilometer," *Advanced Materials Research, Trans Tech Publications,*, vol. 996, pp. 361–366, 2014.

[119] X. Feng, Y. Huang, and A. J. Rosakis, "On the Stoney Formula for a Thin Film/Substrate System With Nonuniform Substrate Thickness," *Transactions of the ASME*, vol. 74, pp. 1276–1281, 2007.

[120] M. A. Hopcroft, W. D. Nix, and T. W. Kenny, "What is the Young's modulus of silicon?" *Journal of Microelectromechanical Systems*, vol. 19, no. 2, pp. 229–238, 2010.

[121] P. Temple-Boyer, C. Rossi, E. Saint-Etienne, and E. Scheid, "Residual stress in low pressure chemical vapor deposition SiNx films deposited from silane and ammonia," *J. Vac. Sci. Technol. A*, vol. 16, no. 4, pp. 2003–2007, 1998.