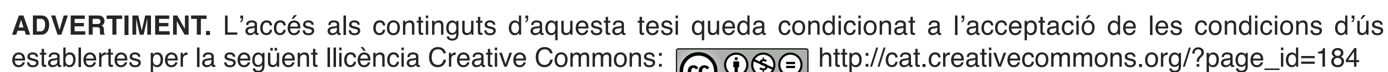
ADVERTIMENT. L'accés als continguts d'aquesta tesi queda condicionat a l'acceptació de les condicions d'ús establertes per la següent llicència Creative Commons:  http://cat.creativecommons.org/?page_id=184

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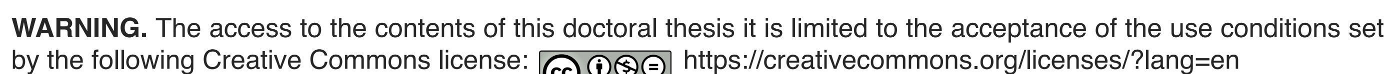
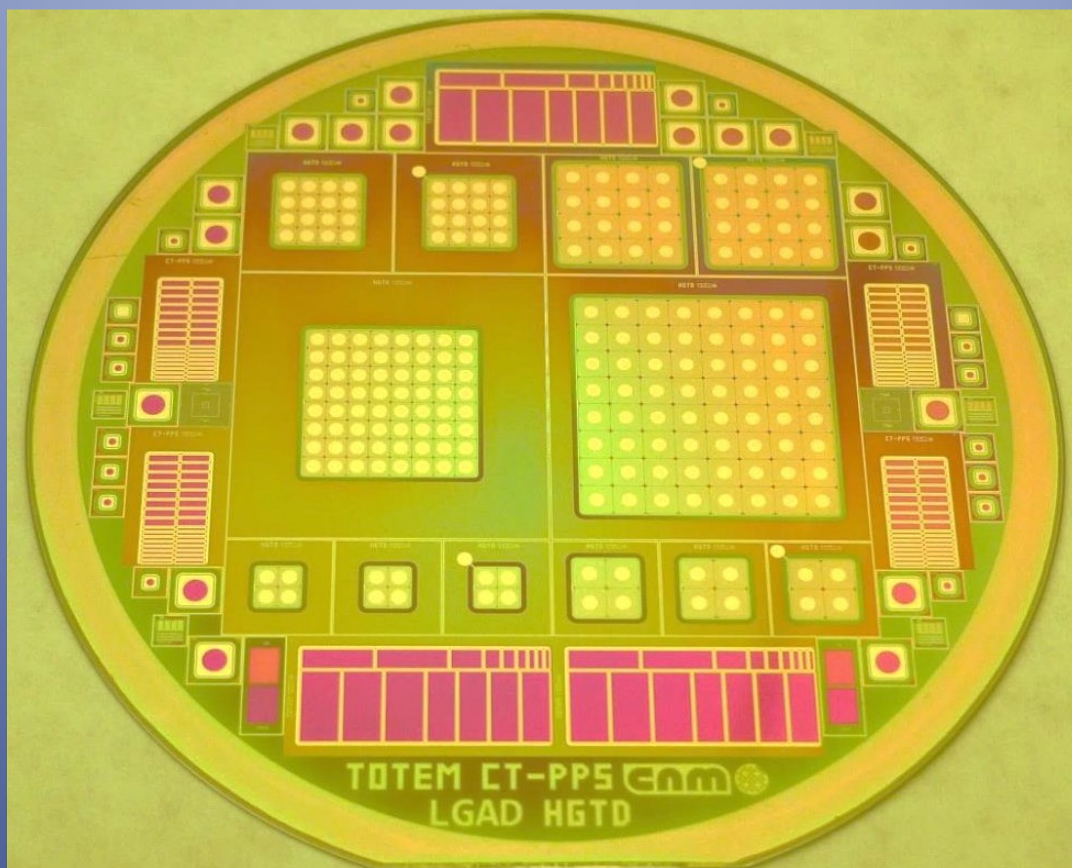
WARNING. The access to the contents of this doctoral thesis it is limited to the acceptance of the use conditions set by the following Creative Commons license:  https://creativecommons.org/licenses/?lang=en



Thin LGAD timing detectors for the ATLAS experiment

Maria del Mar Carulla Areste

May 2019

Thin LGAD timing detectors for the ATLAS experiment

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CERTIFICA:

que la memoria de la presente tesis doctoral titulada "Thin LGAD timing detectors for the ATLAS experiment" presentada por Maria del Mar Carulla Areste para optar al grado de Doctor en Física por la Universidad Autónoma de Barcelona ha sido realizada bajo su dirección dentro del Instituto de Microelectrónica de Barcelona del Consejo Superior de Investigaciones Científicas.

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CERTIFY:

That the present manuscript entitled "*Thin LGAD timing detectors for the ATLAS experiment*" has been written by the Ph. D. candidate **Maria del Mar Carulla Areste** under his supervision, in order to fulfill the requirements for the PhD degree in Physics.

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March 2019

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David Flores Gual

"...Even the largest avalanche is triggered by small things..."
Vernor Vinge "The Coming Technological Singularity: How to Survive in the Post-Human Era"

A Pilu, Amaia, Marisa y en especial a mi madre, que me enseñaron a luchar, tenerme en pie durante la tormenta y dar lo mejor de mí.

Per la Berta. Per que segueixis lluitant i canviant el nostre món.

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and doubts about the measurements they carried out.

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1. INTRODUCTION

The Large Hadron Collider (LHC) with its 27 kilometer in circumference is the world's largest and most powerful particle accelerator. The LHC was designed to collide protons at 14 TeV energy at the center-of-mass. The design luminosity is 10^{34} cm^{-2} s^{-1}, which is achieved with 2808 circulating bunches, each with ~ 10^{11} protons. Bunches are spaced by 25ns, corresponding to a collision rate of 40 MHz at each of the four interaction points.

The main priority of the European Strategy for Particle Physics is the exploitation of the full potential of the LHC. An upgrade of the LHC to the high-luminosity LHC (HL-LHC) was planned for this purpose. The HL-LHC will require an upgrade of the machine and detectors with a view to collecting ten times more data than in the initial design, by around 2030. The major challenges for the high-luminosity phase are the occupancy, pile-up, high data rates, and radiation tolerance of the detectors. The increase in occupancy will be mitigated using higher granularity. Fast timing detectors with time resolution in the range of 30 ps will be used to reduce pile-up. Furthermore, precision timing will provide additional physics capabilities.

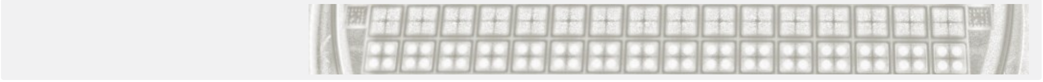
The purpose of the present thesis is the design, development and study of silicon detectors with high granularity and 30 ps time resolution suitable for the upgrade of the A Toroidal LHC Apparatus (ATLAS) experiment in the HL-LHC phase. Low Gain Avalanche Detectors (LGAD) have been proposed by CNM within the RD50 collaboration as timing detectors for the Endcap Timing Layer (ETL) of ATLAS experiment. Three different strategies have been studied in order to fulfil the high granularity, time resolution and radiation hardness specifications of devices for the ETL. The first strategy has consisted in detectors thickness reduction to decrease its collection time, rise time and intrinsic Landau noise. The second strategy has been the minimization of the capacitance developing strips and pixels with gain. Finally, the last strategy has lied in the use of other dopants to reduce radiation effects as boron removal.

The structure of the thesis is as follows: chapter 2 introduces the major issues in the LHC upgrade, the CERN experiments, the required specifications of particle detectors for the HL-LHC phase, their working principles, the measurement of time resolution, the microscopic and macroscopic radiation effects, and the state of the

art in timing detectors; chapter 3 presents the technological and electrical simulation of the designed devices after the calibration of the technological simulation with the process characterization; chapter 4 gives an outline of the different device processes; chapter 5 presents the obtained results of unirradiated and irradiated devices; chapter 6 condenses the simulation, production and results of inverse Low Gain Avalanche Detectors (i-LGAD), and chapter 7 reports the conclusions and future work of the measured devices.

This thesis has made use of process technologies developed at IMB-CNM. Those technologies are confidential. As a consequence, the doping profiles are considered confidential, and consequently they are represented in arbitrary units.

2. Detectors for High Energy Physics



The major issues in the LHC upgrade, the CERN experiments, the required specifications of particle detectors for the HL-LHC phase, their working principles, the measurement of time resolution, the microscopic and macroscopic radiation effects, and the state of the art in timing detectors are introduced in this chapter.

2.1. HL-LHC

The high-luminosity phase of CERN's Large Hadron Collider (HL-LHC) is foreseen to start in 2026. The instantaneous luminosity should reach up to $7.5 \cdot 10^{34}$ cm^{-2} s^{-1}, compared to the current nominal value of $2 \cdot 10^{34}$ cm^{-2} s^{-1} [1]. The probability of proton-proton interaction per bunch crossing will be increased using a low emittance and finely tuned beam optics. The beam bunches will be packed with a nominal value of $1.15 \cdot 10^{11}$ protons per bunch. Thus, significant upgrades of the accelerator and detectors will take place during these periods in order to withstand the high-radiation environment and the large increase in the number of collisions per bunch crossing. Fig. 2. 1 shows the LHC accelerator and detectors upgrade plan since 2011 to 2038.

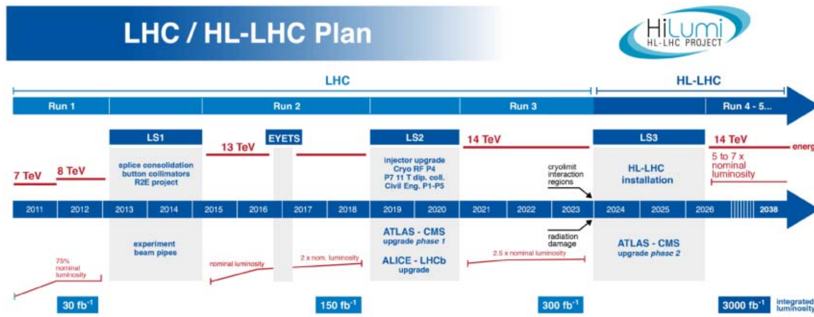


Fig. 2. 1. The upgrade accomplished over the past seven years and the plans for the next two decades.

2.1.1. Pile-up

Proton-proton collision in addition to the collision of interest, collectively referred to as pile-up (μ), present a serious challenge to physics analysis at the LHC. Fig. 2. 2. a) shows the recorded proton-proton collision of the high pile-up fill of Run2. The pile-up during Run2 was of 50 at ATLAS and CMS experiments [2]; meanwhile the expected pile-up during the HL-LHC upgrade will be in the range of 200.

The collision of interest, primary vertices (PV), is characterised by having high momentum particles coming out of it, while the other unwanted collisions contain low momentum particles as it is shown in Fig. 2. 2. b) [3]. The identification of PV is becoming significantly difficult due to the pile-up increase, especially in the forward direction. In the nominal collision scheme, the interaction region will be spread over 50 mm (RMS) along the beam axis and an average of 1.6 collisions per millimetre will be produced for a pile-up of 200 [4]. The resolution on the longitudinal track impact parameter (z_0) should be better than the average distance between interaction points (0.6 mm for the HL-LHC). For $|\eta|>2$ the z_0 resolution provided by the Inner Tracker (ITk) is of the order of a few millimetres [5].

The use of the spread in time of the different interactions during a single bunch crossing reduces the pile-up value. Collisions within one bunch have a time spread of ~180 ps, thus precise timing information of the order of 30 ps allows to unfold the tracks into 6 packages thereby virtually reducing a pile-up value of 200 to values of μ = 40 [6]. Fig. 2. 3 exhibits ATLAS, CMS and LHCb simulation of primary vertices. While 3D reconstructed vertices give the same position for

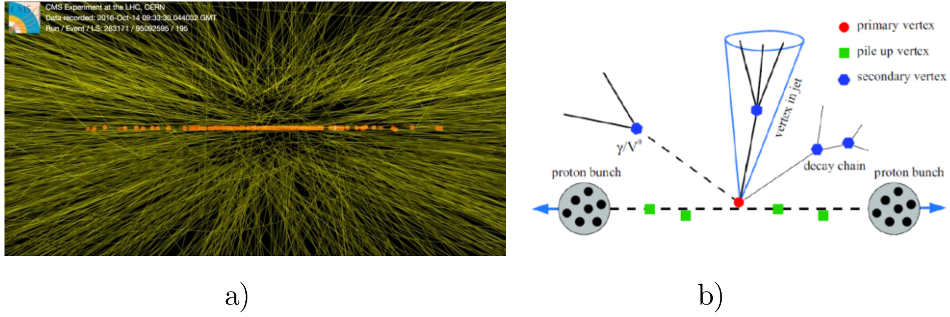


Fig. 2. 2. Proton-proton collisions at a center-of-mass energy of 13 TeV recorded during the high pile-up fill of Run 2 a), draft representation of a PV with a high momentum, a secondary vertex and pile-up vertex b).Taken from [3].

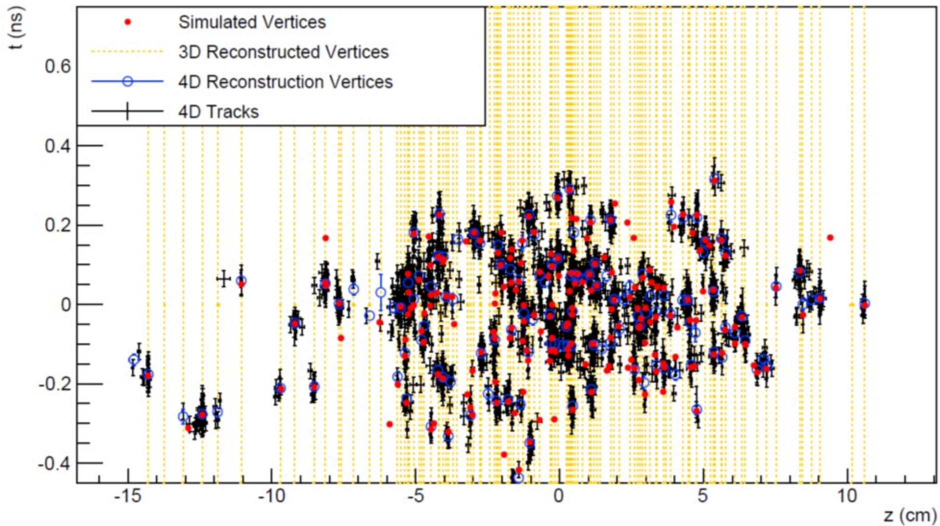


Fig. 2. 3. Simulated PV where the x-axes show the PV position resolved by 3D tracking while the new timing information (y-axes) resolves the vertices in 4D. Remaining charged particles from pile-up can be effectively cleaned. Taken from [7].

different vertices, the 4D reconstructed vertices (3D + timing information) resolve further the 3D tracks and pile-up is decreased [7].

Thus timing information would disentangle overlapping events and eliminate false event assignments exploiting the full potential of the luminosity capability of HL-LHC.

Timing information can be available at different stages in the reconstruction of an event. The timing information can be associated at each hit of the track or at each track rather than each hit. Fig. 2. 4. a) shows a schematic diagram where the effect of time information at each point of the track is clear. In this method, the timing

and 3D tracking information are included in the low level trigger of the experiment. A precise real-time determination of the 3D tracking and timing information is achieve using a system which is based on a massively parallel "artificial retina" [8] algorithm implemented in commercial FPGAs [9]. Those hits that are not compatible with the expected time of passage of the particles are rejected.

On the other hand, the association of timing information at each track during the event reconstruction are performed on dedicated timing layer, which are located inside or outside the tracker volume [10]. Thus, the use of the measured time information on the timing layers allows the disentangling of two events, which are overlapped in space, as it is shown in Fig. 2. 4. b). This method reduces the demands of the read-out and processing electronics. It also minimizes the changes on the main tracker hardware. Thus, the association of timing information at each track is the proposed solution for the HL-LHC upgrade.

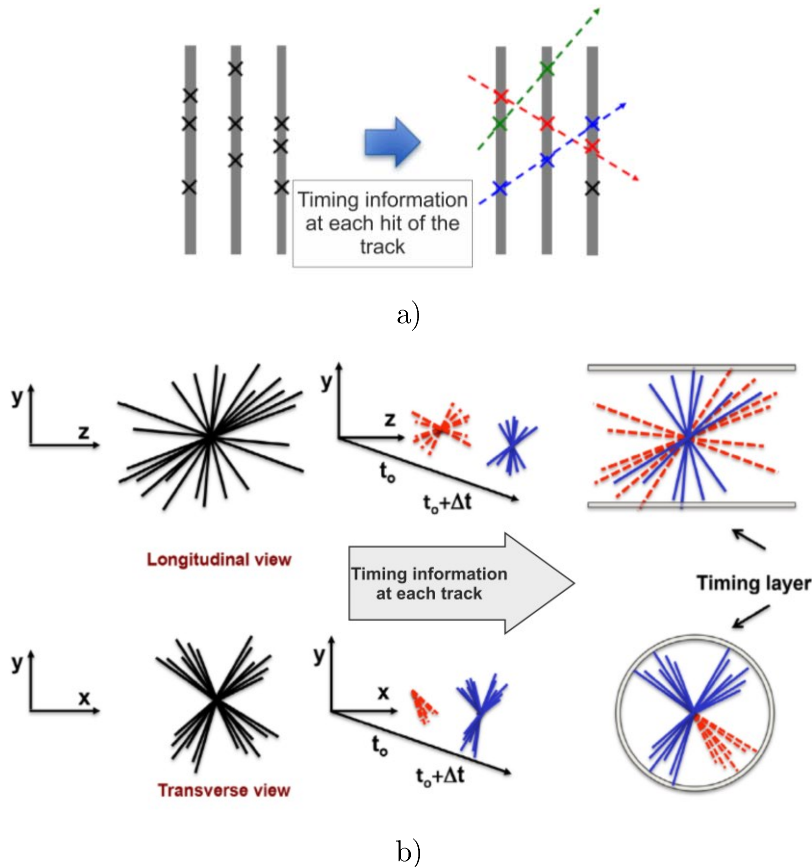


Fig. 2. 4. The track reconstruction of the obtained pattern of hits in 3 tracking layers (left) is resolved adding the timing information of each hit to the spatial information (right), a). Taken from [9]. Schematic diagram of two overlapping events (left), they are disantangled when the time information of each track is added to the tracks (right), b).

2.1.2. Radiation Hardness

Another important issue to take into account on the detector development is the radiation damage that detectors are going to face at the end of the HL-LHC phase. Simulations are used to predict the magnitude and composition of radiation as a function of luminosity. An example of the predictions of expected radiation levels for HL-LHC conditions in the ATLAS detector is given in Fig. 2. 5, where the distribution of absorbed dose over the ATLAS detector for an integrated luminosity of 3000/fb is shown [11], [12]. Thus, detectors at low radii and large pseudorapidity will require major optimizations in order to stand fluences 10 times larger than in LHC. As a consequence, the signal collection will be degraded in such environment. Since 2001, the RD50 collaboration "Radiation hard semiconductor devices for high luminosity colliders" is working on the development of radiation hard semiconductor detectors for the HL-LHC phase [13]. Drawing on their knowledge of the radiation effects, the RD50 thoroughly investigates device and material engineering approaches along with the optimization of operational conditions in order to increase radiation hardness and improve detector performance under any conditions.

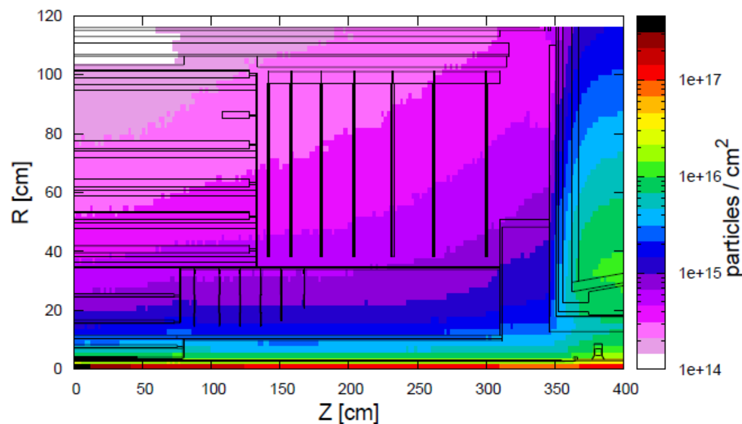


Fig. 2. 5. Radiation fluence distribution at ATLAS detector of 1 MeV neq fluences normalised to 3000/fb. R is the transverse distance from the beamline and Z is the distance along the beamline from the IP at Z=0. Taken from [12].

The different strategies to improve the radiation hardness of the detectors are:

- The use of high resistivity p-type substrates to avoid type inversion after hadron irradiation of the n-type substrates, as well as to reduce the required voltage to fully deplete the detector [14]. An exhaustive understanding and development of the n-on-p detectors have been achieved

over the past years. Structures as p-type implants between strips/pixels and floating guard rings have been developed in order to avoid shortcuts between strips/pixels, as well as to increase the voltage capability of detectors, respectively.

- The study of new geometries of 3D detectors. The charges induced in the 3D detectors by ionizing radiation are collected by cylindrical columns etched into the bulk [15]. This type of sensors shows a superior performance after fluences up to $3 \cdot 10^{16}$ $n_{eq} \cdot cm^{-2}$ [16]. 3D sensors have been installed in the ATLAS IBL. 3D detectors are currently the most promising option for the innermost pixel detector layers for ATLAS Phase II [17]–[19].
- Based on the observation of charge multiplication in highly irradiated sensors operated at high voltage as well as the superior performance of 3D detectors with short drift distances, a thin detector with short drift distances, similar to 3D distances, and intrinsic multiplication, namely Low Gain Avalanche Detectors (LGAD), has been proposed as radiation hard timing detectors [20].

2.2. CERN Experiments

There are four major experiments at the LHC, as it is shown in Fig. 2. 6. Two are general-purpose high transverse momentum experiments (high-p_T), ATLAS and CMS, which perform precision studies of the Standard Model (including the new field of Higgs properties), as well as they search for physics beyond the Standard Model. The Large Hadron Collider beauty experiment (LHCb) specializes in investigating the slight differences between matter and antimatter by studying the beauty quark. The LHC also accelerates heavy ions (Pb^{82+}). Typically it is run with Pb-Pb or Pb-p collisions for one month at the end of each year. The dedicated experiment for this physics is ALICE, although by now all experiments participate. The ATLAS and CMS experiments are introduced in this section, along with the detector subsystems and the specifications needed for the timing detectors in both experiments.

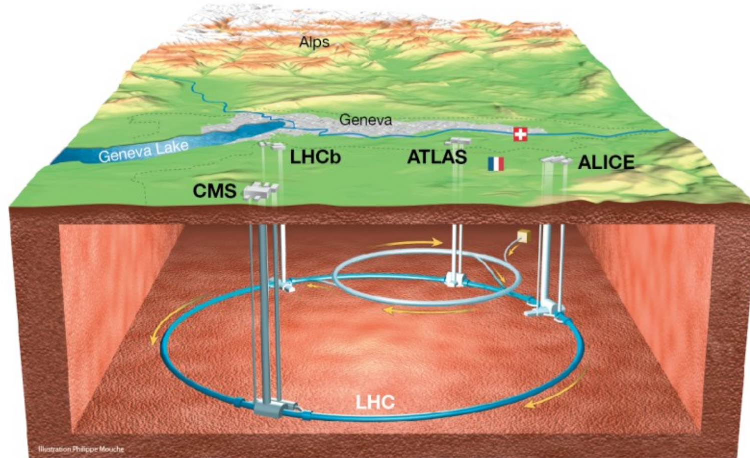


Fig. 2. 6. View of the 4 LHC detectors: ALICE, ATLAS, CMS and LHCb.

2.2.1. ATLAS

ATLAS is one of two general-purpose detectors at the LHC. It investigates a wide range of physics, from the search for the Higgs boson to extra dimensions and particles that could make up dark matter. Although it has the same scientific goals as the CMS experiment, it uses different technical solutions and a different magnet-system design.

Proton-proton collision at the centre of the ATLAS detector is studied with six different detecting subsystems arranged in layers around the collision point. These subsystems record the paths, momentum, and energy of the particles, allowing them to be individually identified.

The overall ATLAS detector layout is shown in Fig. 2. 7. It is composed of the Inner Tracker Detector (ITk), the Liquid Argon (LAr) electromagnetic calorimeter, the hadronic calorimeter (Scintillating Tile hadronic barrel detectors, TileCal, and the Hadronic End-cap Calorimeter, HEC), the muon system, and the forward detectors.

The ITk for the Phase-II upgrade of ATLAS was designed to measure the transverse momentum and direction of isolated particles (in particular muons and electrons), to reconstruct the vertices of pile-up events and to associate the vertex with the hard interaction.

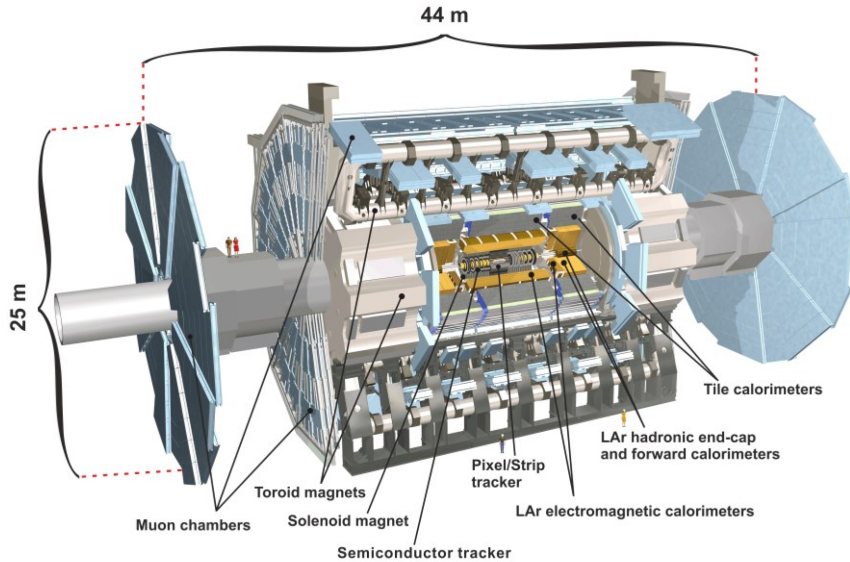


Fig. 2. 7. Schematic view of the ATLAS detector with the various sub-systems. The dimensions of the detector are 25 m in height and 44 m in length. The overall weight of the detector is about 7000 tons.

The detectors of the ATLAS Calorimeter system, including the LAr e-m calorimeters, the TileCal, and the HEC, maintain their required performance under HL-LHC conditions, and as a result they do not need replacement. On the other hand, the performance of the Liquid Argon Forward Calorimeters (FCals) will be degraded by the high energy and particle density in the LAr detector elements under HL-LHC conditions, and consequently its replacement with a high-granularity sFCal is foreseen in the reference scenario. This replacement, together with the installation of a new High Granularity Timing Detector (HGTD) in front of the LAr Calorimeter end-caps, will allow a mitigation of pile-up effects in the forward and end-cap regions [4], [21].

2.2.1.1. HGTD

As aforementioned, pile-up suppression is one of the main challenges at the HL-LHC. In the forward region, the resolution attains a few millimeters depending on the transverse momentum (p_T) and up to 7 collision vertices could be merged into a single one.

In this context, A High Granularity Timing Detector (HGTD) is proposed to measure the arrival time of charged particles in order to assign them to different collision vertices. With an expected time resolution of approximately 30 ps for

minimum-ionizing particles (MIP), in contrast to 180 ps RMS spread of collisions in the nominal configuration, this device should be able to assign a collision vertex to each particle. Timing information is complementary to the spatial and p_T information provided by the tracker and calorimeters, making it a unique new tool to enhance the pile-up mitigation capabilities of the ATLAS detector in the endcaps and forward regions.

The HGTD covers the pseudorapidity ($|\eta|$) region from about 2.4 to 4.3, partially occupying spaces in the ATLAS endcaps that presently contain the Minimum Bias Trigger Scintillators (MBTS) and moderator, as illustrated in Fig. 2. 8. The detector will be located at about $z = \pm$ 3.5 m from the interaction region, just outside the Inner Tracker (ITk) volume and in front of the forward calorimeters and the EM endcap inner wheels. Fig. 2. 8 shows a photo of the HGTD location.

The space allocated to the HGTD for the ATLAS HL-LHC upgrade is quitelimited, which defines some of the HGTD geometrical parameters. The space in z axis goes from position z = 3450 mm to position z = 3545 mm. As agreed upon recently by the ATLAS Technical Coordination and ITk, a 50 mm moderator will be installed in front of the endcap calorimeters to protect the ITk and the HGTD from the back-scattered neutrons from the endcap calorimeter. Thus, the available space for the full detector, including supports and front and rear covers, is 75 mm. The problem of the space constraints is one of the reasons for choosing silicon-based detectors as baseline. Table 2. 1 presents the main characteristics of the HGTD. An overall layout of the HGTD is shown in Fig. 2. 9.

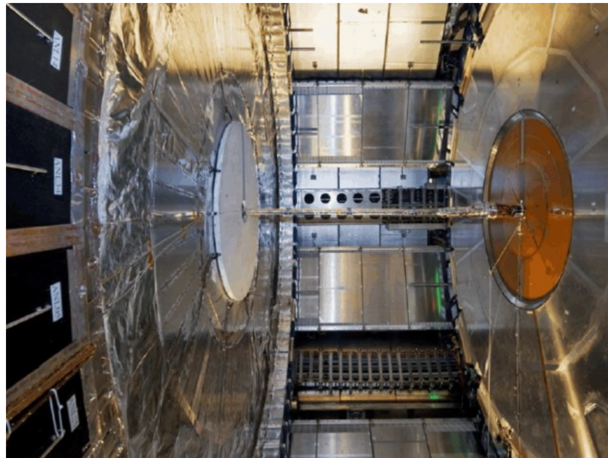


Fig. 2. 8. A photo of the current ATLAS layout (opened for maintenance), showing the gap between the ATLAS endcap calorimeter on the left and the tracking detectors on the right, where the HGTD will be installed. Currently the space is occupied by the MBTS (white disk, in front of the endcap calorimeter).

Table 2. 1: Main parameters of the HGTD	
Pseudorapidity coverage	$2.4 < \|\eta\| < 4.2$
Position of active layers	$3435 < z < 3485$ mm
Radial extension (active area)	110 – 1100 mm (120 mm -640 mm)
Number of layers	3 per side
Time resolution	30 ps/mip
Sensor size	1.3 x 1.3 mm^2
Number of channels	6.3 M
Number of Si modules (2x4 cm^2 each)	13952
Number of ASICs (2x2 cm^2 each)	27904
Total active area (Si sensors)	11.16 m^2

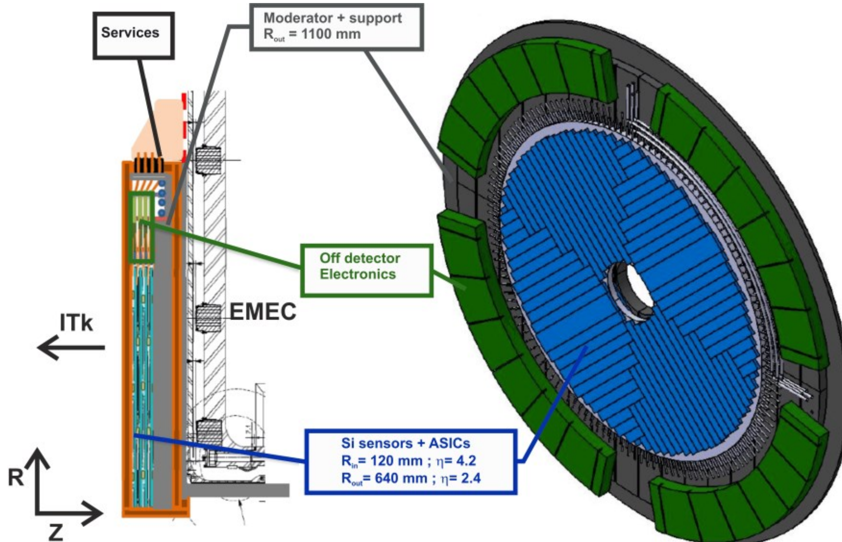


Fig. 2. 9. Illustration of the HGTD detector. On the left, the detector installed in front of the endcap calorimeter cryostat. On the right, the different components of the HGTD. The central blue parts correspond to the active area. The green blocks correspond to the off-detector electronics. The grey cylinder behind is the moderator needed to shield the back-scattered neutrons from the endcap calorimeter. Taken from [1]

2.2.1.2. The ATLAS Forward Proton (AFP) project

The main purpose of AFP detectors is to study hard diffraction and search for new physics using proton spectrometry. The AFP detectors are placed about 210m from the ATLAS Interaction Point (IP), because diffractive protons are usually scattered at very small angles. The purpose of the spectrometer is to tag and measure the momentum and emission angle of very forward protons that remain close to the LHC beam line [4]. Each AFP arm contains two Roman pot (RP) stations [22], at 205 m and 217 m. Roman Pots are cylinders that allow the displacement of detectors into the LHC beam pipe so they sit a few mm from the beam during measurements and they are move inside the RP afterwards. Tracking detectors are placed in each pot, while a compact time-of-flight (ToF) detector is only installed in the station at 217m. The time-of-flight measurement of the forward protons is required to reject pile-up background. A schematic not-to-scale drawing of the AFP detector is depicted in Fig. 2. 10. [23].

Fig. 2. 10. Scheme showing the AFP detector, where the position of the protons is measured by the tracker detectors, and their ToF system measures their ToF in order to identify their original vertex of the protons. Taken from [23].

Each Roman Pot station houses a set of 4 Silicon tracker (SiT) planes. The tracker devices are based on silicon hybrid detectors: 3D pixel sensors [15], [24], [25] are coupled to the FE-I4 read-out chip [26]. The ToF system consists of 16 L-shaped quartz bars (LQbars) installed in each of the far Roman Pot stations on both sides and a Micro-Channel Plate Photo-Multiplier (MCP-PMT), which detects the Cherenkov photons at the end of the bars [27].

There are concerns about how high luminosity affects cross talk between channels. The timing resolution in a given train can potentially be degraded if a neighboring train also has a proton. Furthermore, the LQbars lose their transparency in near UV after the exposure and the glue doesn't stand the radiation. Thus, LGAD detectors were proposed to replace the actual AFP ToF system.

2.2.2. CMS

The Compact Muon Solenoid (CMS) is a general-purpose detector at the LHC. Although it has the same scientific goals as the ATLAS experiment, it uses different technical solutions and a different magnet-system design [28].

2.2.2.1. CMS TOTEM-Precision Proton Spectrometer

LHC collides bunches of protons into one another. When two bunches are focused magnetically to cross each other in the center of detectors such as CMS and ATLAS, only 30 or so protons actually collide. The rest continue to fly through the LHC unimpeded until the next time that two bunches cross.

But if two protons travelling in opposite directions pass very close to one another, photons radiated from each proton can collide and produce new particles. The two parent protons remain completely intact, continuing their path in the LHC, but the photon-photon interaction removes a fraction of their initial energy and causes them to be slightly deflected from their original trajectories. By identifying the deflected protons, It can determine whether such photon interactions took place [29].

A new project called the CMS-TOTEM Precision Proton Spectrometer (CT-PPS) has now taken up the challenge of making photon-photon physics possible at the LHC when operating at nominal luminosity [30]. CT-PPS uses two sets of detectors, tracking and ToF detectors, placed on each side of the CMS IP [31]–[33]. Strips and 3D detectors are installed for tracking inside 2 RPs at 214 m and 220 m from the CMS IP. Although different technologies are used nowadays as timing detectors, diamond detectors were chosen for ToF detectors and four layers of diamond sensors were installed inside horizontal RP stations at 216 m from CMS IP during 2016. LGAD detectors with customized pad segmentation to suit the hit density distribution were proposed as ToF detectors for CT-PPS. One diamond layer was replaced by the LGAD device for the CT-PPS experiment during 2017.

2.2.2.2. Endcaps Timing Layer (ETL)

Analogous to the HGTD, an endcap timing layer must be installed in the CMS Endcaps to mitigate pile-up. The Endcaps timing layer is situated between the tracker and the calorimeter and covers the pseudorapidity ($|\eta|$) region from about 1.5 to 3.0. At this pseudorapidity, detectors should withstand a radiation fluence of $2 \cdot 10^{15}$ n_{eq}/cm^2. More detailed information can be consulted in reference [34].

2.3. Particle Detectors

Semiconductor detectors are basically ionization chambers with an ionizing energy lower than a gas detector. The structure and signal formation in silicon detectors are explained in the next section.

2.3.1. Silicon detectors

Silicon strip, pixel or voxel detectors are extremely useful in many different fields. Their small size, high granularity, low intrinsic noise and the possibility of making them radiation resistant under special treatment, render them a high-resolution detector of exceptional versatility. They are currently being used in many particle physics experiments as vertex detectors. Important applications in other fields, like medicine (Compton cameras), art, material science and engineering, complete the large-scope applications [35].

Silicon sensors are diodes with a pn-junction, which is depleted applying a reverse bias from external electrodes. Then the depleted zone acts as a solid state ionization chamber. In such a reverse biased diode, only a very small thermally generated current is flowing and a large electric field is built up in the depleted region. If an incident particle stops in the detector, the particle energy can be measured (spectroscopy); if a particle crosses the detector, it is only possible to determine whether or not a particle has passed (tracking). Therefore, the momentum of the particle is extracted from the reconstruction of the trace of the particle under the magnetic field. Tracking is the main application of silicon detectors in high energy physics.

Electron-hole pairs are created in the diode by photons and ionizing particles. A minimum ionizing particle (MIP) traversing a silicon detector of 300µm thickness create a most probable value of 24000 electron-hole pairs (about 80 e-h pairs per µm) [36] . If the detector is fully depleted, all the generated electrons and holes are drifted by the electric field to the electrodes, inducing a signal on them.

2.3.1.1. Capacitance

Pn-diodes are manufactured on low doped p-type bulk silicon material with a shallow high doped n^+ implant on the surface, creating the junction. A thin p-doped implant on the backside surface acts as an ohmic contact. Both implantations are contacted by metal layers. When a reverse bias (V) is applied to the bulk with a doping concentration N_A, it starts to deplete from the pn-junction till the space charge region reach the p-type ohmic contact of the backside at a

depth d and an electric field builds up in the depleted region.

A depleted diode forms a parallel plate capacitor. The depletion-layer capacitance per unit area is defined as $C_D = dQ_D/dV = \varepsilon_s/W_D$, where dQ_D is the incremental depletion charge on each side of the junction upon an incremental change of the applied voltage dV. For one-sided abrupt junctions, the capacitance per unit area is given by

$$C_D = \frac{\varepsilon_s}{W_D} = \sqrt{\frac{q\varepsilon_s N_A}{2}}\left(V_{bi} - V - \frac{2kT}{q}\right)^{-1/2} \qquad \text{Eq. 2. 1}$$

It is straightforward from parallel plate capacitor equation that once the detector is full depleted the capacitance remains constant because both the area and depth do not change. Rearranging the equation leads to a more useful equation:

$$\frac{1}{C_D^2} = \frac{2}{q\varepsilon_s N_A}\left(V_{bi} - V - \frac{2kT}{q}\right) \qquad \text{Eq. 2. 2}$$

It is clear from the last equation that by plotting $1/C_D^2$ versus V, a straight line should result from a one-sided abrupt junction [37]. The slope gives the impurity concentration of the substrate (N_A), as it can be observed in Fig. 2. 11. Besides, the full depletion of the device can be obtained using the RD50 collaboration convention. The $1/C_D^2$ data points are fitted to two linear curves, as it is shown in Fig. 2. 11. The intersection of these two linear curves defines the full depletion voltage (V_{FD}) of the detector.

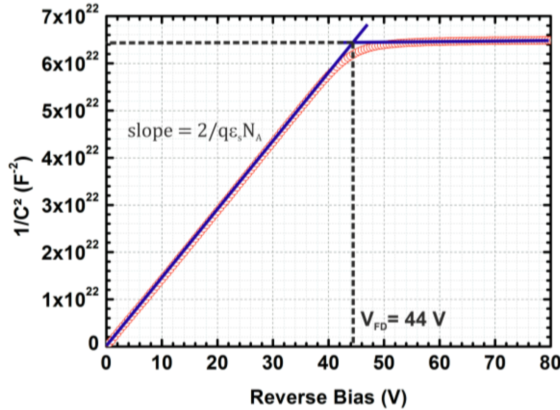


Fig. 2. 11. Plot of the $1/C_D^2$ vs reverse bias for 300 µm thick detector where the full depletion voltage (V_{FD}) is indicated.

2.3.1.2. Charge collection and signal formation

Carrier transport in a silicon detector is carried out through diffusion or drift. Diffusion is driven by a concentration gradient, while carriers are drifted to the electrodes due to the build-up electric field.

A sufficient amount of energetic radiation impinging the sensor volume creates electron-hole pairs along its path. Electron-hole pairs created in the depleted volume of the sensor are drifted under the influence of the electric field to the correspondent electrodes as shown in Fig. 2. 12, while those pairs created in the non-depleted volume are diffused to a lower gradient.

When a charge is created inside the sensitive volume, an induced charge is created on the electrodes. Once the charge starts moving towards the electrode, the induced charge in the electrode changes over time and a signal current is detected. Thus, the signal current begins when the charges start moving.

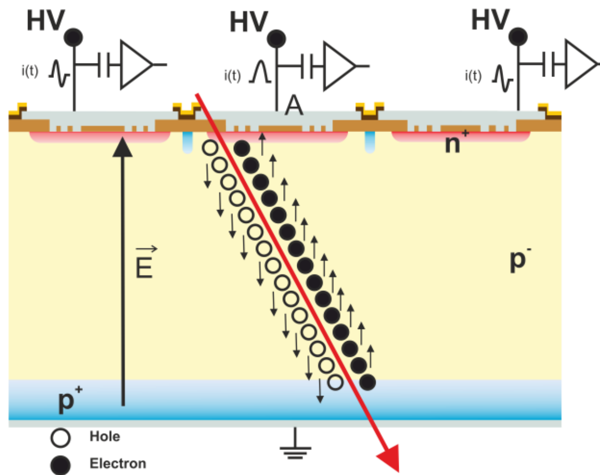


Fig. 2. 12. The particle impinges a fully depleted p-i-n diode, creating electron-hole pairs along its path. The electrode A collects all the charge, while a current with a bipolar shape is induced in the neighboring electrodes.

From Shockey-Ramo's theorem [38], [39], the induced charge on electrode A, which is at unit potential on the other grounded electrodes, is

$$i_A = qv_x \frac{\partial V_{q1}}{dx} = qv_x \frac{\partial \phi}{dx} = -q\vec{v} \cdot \overrightarrow{E_Q} \quad \text{Eq. 2. 3}$$

where $\overrightarrow{E_Q}$ is the weighting field and ϕ is the weighting potential that describes the coupling of a charge to the electrode A. The weighting potential and field apply to a specific electrode are obtained setting the potential of the electrode to 1 and

setting all other electrodes to 0. The weighting field just depends on geometry and determines how charge motion couples to a specific electrode. Meanwhile, the electric field determines the charge trajectory and velocity. Only in two-electrode configurations the electric field and the weighting field show the same form.

2.4. Time-of-arrival measurement

As aforementioned in section 2.1.1, precise information of the time-of-arrival of a particle is crucial to reject background pile-up. When timing information is the major purpose, detector pulses are often handled differently than when accurate pulse height measurement is the object. The best timing performance is obtained for the fastest detectors, because the charge is collected most rapidly on them. For detectors with equal charge collection time, those that generate the greatest number of electron-hole pairs per pulse will demonstrate superior timing properties [40].

The easiest and most direct time pick-off method is to sense the time that the pulse crosses a fixed threshold level. Such leading edge (LE) timing methods are in common use and can be quite effective, especially in situations in which the dynamic range of the input pulses is not large. On the contrary, a constant fraction discriminator (CFD) is the best option as a pick-off method, when the dynamic range of the input pulses is large, as it will be shown. In the next sections the different contributions on the time resolution and the CFD pick-off method are introduced.

2.4.1. Time resolution

Effects that change the shape of the signal and each step in the read-out process introduce uncertainties in the time-of-arrival. The schematic diagram of the main components of a measuring ToF system is presented in Fig. 2. 13. The sensor output signal is read out by a preamplifier [41]. After, the preamplifier output is compared to a threshold (V_{th}) or a CFD to determine the ToA (t_0). Finally, the comparator or discriminator output is digitized in a time-to-digital converter (TDC). Thus, the time resolution is the sum of the time walk ($\sigma_{time\ walk}$), Landau noise ($\sigma_{Landau\ noise}$), jitter (σ_{jitter}), signal distortion ($\sigma_{distortion}$) and TDC effects (σ_{TDC}), as it is shown in Eq. 2. 4.

$$\sigma_t^2 = \sigma_{time\ walk}^2 + \sigma_{Landau\ noise}^2 + \sigma_{jitter}^2 + \sigma_{distortion}^2 + \sigma_{TDC}^2 \qquad \text{Eq. 2. 4}$$

Those uncertainties related to the variable amplitudes of input pulses are called time walk. The time walk uncertainty is shown in Fig. 2. 14, where two pulses with identical shape and time of occurrence cross the threshold level at different times. Thus, the variation in signal amplitude will broaden the timing distribution. The time walk is defined as the RMS of the time at which the signal crosses the threshold (t_d), as shown in Eq. 2. 5

$$\sigma_{time\,walk} = [t_d]_{RMS} = \left[\frac{V_{th}}{S/t_{rise}}\right]_{RMS} \propto \left[\frac{N \cdot \sigma_N}{dV/dt}\right]_{RMS} \qquad \text{Eq. 2. 5}$$

where S is the signal amplitude, t_{rise} is the rise time of the signal, σ_n is the system noise and dV/dt is the slew rate.

As it can be seen in Fig. 2. 14, time walk decreases if the threshold level is reduced. Therefore, time walk can be minimized as it will be shown in section 2.4.2.

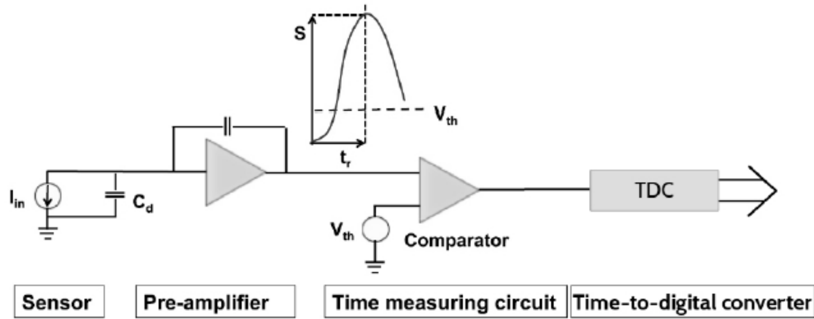


Fig. 2. 13. Scheme of the ToA measuring system, where the sensor is represented by a capacitor with a current source in parallel. Taken from [41]

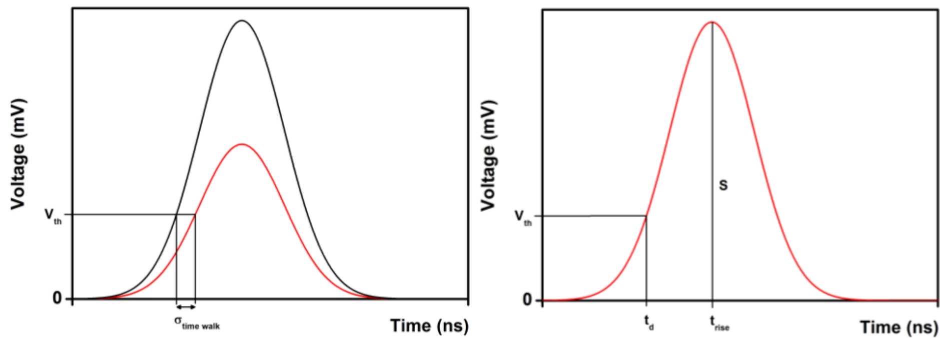


Fig. 2. 14. Time walk in leading edge triggering. Two pulses with identical shape and time of occurrence but different amplitude are seen to cross the trigger level at different times.

The signal produced by a MIP crossing a sensor varies on an event-by-event due to the fact that the created charge distribution follows a Landau-Vavilov distribution. Therefore, these event-by-event variations cause a change in the signal amplitude. As aforementioned, those uncertainties related to the variable amplitudes of input pulses are taken into account in the time walk term ($\sigma_{\text{time walk}}$). Additionally, for each event, the amount of energy loss per unit of length is not uniform. These fluctuations, which are specific of each event, cause irregularities in the induced signal of each event. These irregularities in the induced signal are known as Landau noise ($\sigma_{\text{Landau noise}}$). The Landau noise depends on how MIPs lost their energy in silicon detectors. Reducing the detectors thickness decreases the energy loss of MIPs [36], as well as the Landau noise [10].

Effects which give uncertainties in the arrival time, when the input pulse amplitude is constant, are usually called sources of time jitter (σ_{jitter}). Fig. 2. 15 shows the leading edge of a pulse fed into a threshold discriminator, a leading-edge triggering [35] . The instantaneous signal level is modulated by noise, where the variations are indicated by the shaded band. Because of these fluctuations, the time of threshold crossing fluctuates. The timing variance or jitter is

$$\sigma_t = \frac{\sigma_n}{\left({}^{dV}/_{dt}\right)_{V_{th}}} \approx \frac{1}{{}^{S}/_{N}} t_r \qquad \text{Eq. 2. 6}$$

where σ_n is the rms noise and the slew rate dV/dt is evaluated at the trigger level V_{th}. As it can be appreciated the jitter will increase if the slope of the leading edge of the pulse is decreased. In other words, time jitter can be reduced by fixing the threshold level, where the slew rate is maxim, as well as by decreasing the time rise.

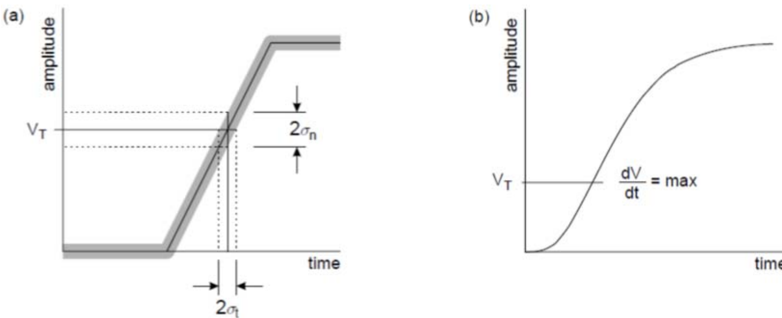


Fig. 2. 15. Fluctuation in signal amplitude crossing a threshold translate into timing fluctuations. With real pulses the slope changes with amplitude, so minimum timing jitter occurs with the trigger level at the maximum slope. Taken from [42].

Furthermore, sensors can introduce variations on the signal shape as a function of the hit position, which produce uncertainties in the time resolution known as signal distortion ($\sigma_{distortion}$). The induced current is proportional to the carriers drift velocity and the weighting field, as shown Eq. 2. 3. These variables should be homogenous on sensors for timing applications and they do not depend on the hit position. To achieve the required uniformity, in the first place, the sensors are designed to reach a high electric field (E > 30 kV/cm) right after their depletion, in order to saturate the carriers drift velocity ($v_{sat} \sim 1 \cdot 10^7$ cm/s). In the second place, the width of the electrodes is as big as the pitch and infinite, when they are compared to the sensor thickness.

The storage of the timing information is typically done in a TDC (time-to-digital converter), where the time of the leading edge of the discriminator signal is digitized and place in a time bin of width Δt, given by the TDC least significant bit. This process adds a contribution to the timing uncertainty equal to $\Delta t/\sqrt{12}$. This error does not depend on the sensor characteristics and its contribution to the overall resolution is small.

Finally, it is worth to mention that the best timing performance is achieved if the input pulses are confined to a very narrow range in signal amplitude, because only sources of time jitter contribute to uncertainty. However, practical applications require the processing of pulses of different amplitudes, and the additional contribution of walk will worsen the overall time resolution of the system [40], [42]. Therefore, the discrimination point should be as low as possible to minimize the sensitivity of leading edge triggering to time walk. However, the discrimination point should be in a region of steep slope on the pulse leading edge to minimize uncertainties due to jitter. Compromise in these requirements often leads to optimum time resolution for levels that are set at about 10-20% of the average pulse amplitude.

2.4.2. Constant fraction discriminator

It is empirically found that the best leading edge timing characteristics are obtained when the timing discriminator is set at about 10-20% of the pulse amplitude. These observations have led to the development of a time pick-off method that produces an output signal at a fixed time after the leading edge of the pulse has reached a constant fraction of the peak pulse amplitude. This point is independent of pulse amplitude for all pulses of constant shape.

The discriminator compares the input pulse, which is delayed (t_d), with the fractional pulses, which is inverted. The time for which both pulses are equal, is the

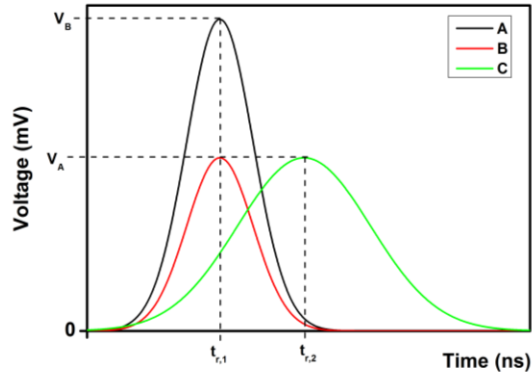
output time of the discriminator. This process is the same thing as building a bipolar pulse, which is the sum of the delayed input pulse (t_d) with the desired fractional pulse, which is inverted. The time when this pulse crosses the zero axes is independent of the pulse amplitude and corresponds to the time at which the pulse reaches the fraction of its final amplitude.

Using the constant fraction technique, time walk due to rise time and amplitude variations of the input signal is minimized by proper selection of the shaping delay, t_d. Jitter is minimized by proper selection of the attenuation factor, f.

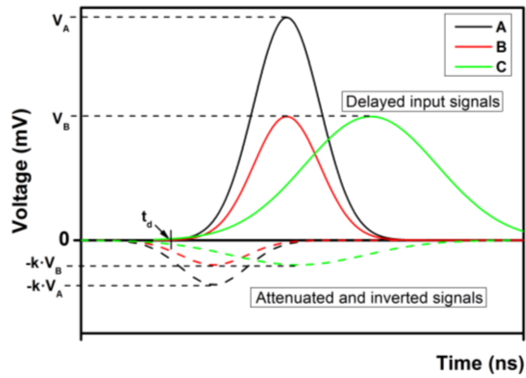
The time of zero crossing occurs while the attenuated input signal is at its full amplitude. Fig. 2. 16 shows the signal formation in an ideal CFD for True Constant Fraction (TCF) timing. The amplitude independence of the zero crossing time is depicted for input signals A and B, which have the same rise time but different amplitudes. From signals B and C the zero crossing time is seen to be dependent on the rise time of the input signal [43].

The zero crossing time occurs after the input signal has reached its maximum amplitude. The shaping delay must be sufficiently short to force the zero crossing time to occur during the time that the attenuated signal is at its peak.

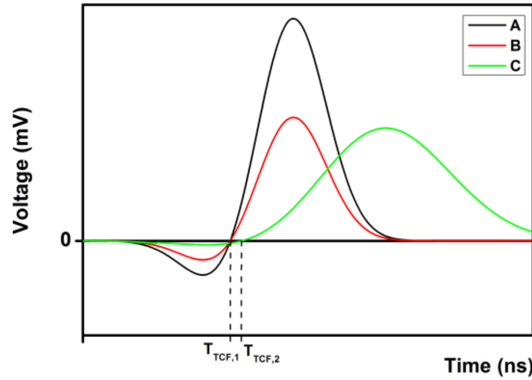
TCF timing is most effective when used with input signals having a wide range of amplitudes but having a narrow range of rise times and pulse widths. Any remaining walk effect can be attributed to the charge sensitivity of the zero crossing detector and the limitations of the devices used to form the constant fraction signal.



a)



b)



c)

Fig. 2. 16. Signal formation in a constant fraction discriminator for TCF timing of two signal pulses with same t_r and different amplitude (A and B) and one signal with same amplitude as pulse B but longer time rise than B (C).

2.5. Timing Detectors

Fast time-of-flight detectors with expected time resolution in the range of 10 ps and space resolution < 1mm are interesting in many fields: HEP, medical and industrial applications. They can be used in muon collider studies, ToF spectrometry, and particle and vertex identification in colliders.

Several sensor and detector technologies are considered to achieve a timing performance in the range of 20 ps for MIP. In this section the state of the art of timing detectors, which are used in HEP, is reviewed. As it will be shown, solid state timing detectors have the important advantage of being very thin and allowing fine granularity. Solid state detectors, as diamond and silicon detectors, make it possible to stack three or more detectors, which improves the time resolution by the square root of the number of layers.

2.5.1. Cherenkov gas detector

Cherenkov gas detectors consist in an L–shaped vessel containing a gas acting as a radiator. The vessel is filled with C_4F_{10}. The incident protons produce Cherenkov photons in C_4F_{10} that are reflected and focused to the window center of the MCP-PMT (Microchannel Plate-Photomultiplier Tube) by the UV enhanced concave mirror, as it is shown in Fig. 2. 17. a) [44]. The MCP-PMT has a photocathode material with a low work function that liberates an electron when a photon hits the cathode, and the electron is accelerated and guided by electric fields to hit a secondary-emission electrode. Hit after hit, the signal is multiplied and the MCP-PMT transforms the individual photon hits into an electronic pulse to be collected and processed, as it is shown in Fig. 2. 17. b).

Time resolution obtained for the Cherenkov gas detector at the test beam is 15 ps per proton [44]. As a drawback, the quantum efficiency of the photocathode is degraded with radiation. However, the quantum efficiency degradation is corrected by increasing the gas pressure, which results in a raise in the number of Cherenkov photons. The gain of MCP-PMT also decreases with radiation. Despite that, the gain is recovered increasing the high voltage. Another disadvantage is the fact that the vessel cannot be segmented, and consequently the granularity of the detector is too low.

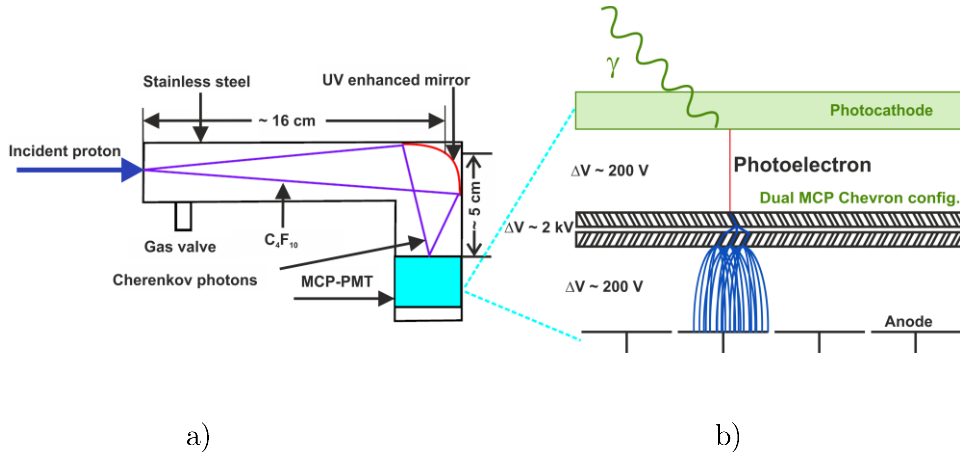
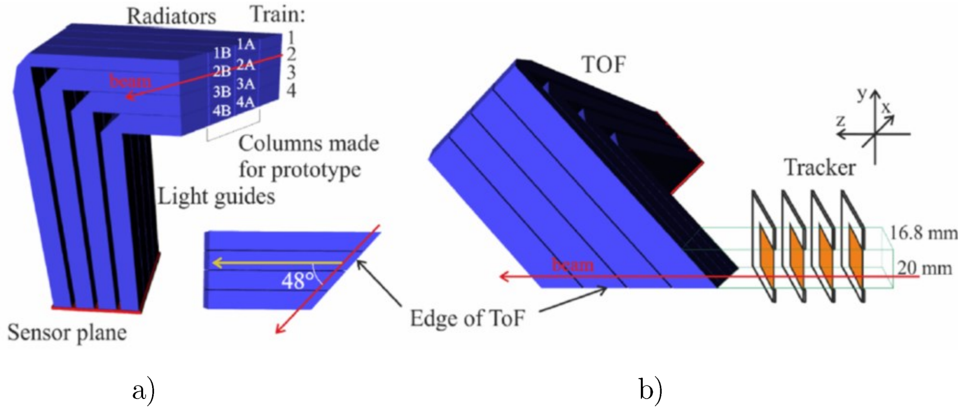


Fig. 2. 17. Illustration of the Cherenkov gas detector a). Sketch of the Multichannel Plate- Photomultiplier Tube with a Chevron configuration b). Taken from [44].

2.5.2. Quartz Cherenkov

Albrow et al. [45] developed particle detectors based on fused silica Cherenkov radiators read out with MCP-PMT for high precision timing. Quartz Cherenkov detector consists of a 4x4 matrix of L-shaped bars made of fused silica. Each bar serves both as a Cherenkov radiator and light guide towards a fast MCP-PMT device [46]. The radiators are tilted at an angle of 48º with respect to the beam, which corresponds to the Cherenkov angle for the fused silica. The bars are produced from 2 pieces and glued by UV transparent glue. All the surfaces of the bars are polished and only the area of the 45º cut on the outside of the right angle joint of the radiator and light guide parts are aluminized to meet the reflection conditions. A sketch of the fused silica bars is illustrated in Fig. 2. 18. The shape of the fused silica bars is due to the limited space inside the Roman Pot.

Irradiation tests of the bar materials were performed by Komarek et al. [47], where a loss in the transmission of UV light was obtained in bar materials (fused silica bars and glue). In addition to the reduction in transparency in both materials, the glue does not withstand the radiation.



a) b)

Fig. 2. 18. Illustration of the fused silica bars where the trains and the radiators are labelled a). Illustration of the quartz bars position with respect to the tracker inside the Roman Pot b). Figures taken from reference [45].

While Cherenkov based detectors have intrinsically better time resolution and are more mature timing technologies, they have some important drawbacks. In the existing device implementation, the quartz detector is segmented in elements of 3 x 3 mm^2, which implies a large rate of double hits in the same bar per bunch crossing, approaching 50% in the sensors close to the beam. Two hits in the same channel cannot be resolved. Finer granularity near the beam is required to improve the detector performance.

The amount of material introduced by the quartz detector itself is not negligible. The probability that a proton has a nuclear interaction in one detector is between 7.2% and 14.6%. Given that the timing detector is located downstream of the pixel detectors, these interactions do not affect the track measurement. However, they may smear the time measurement introducing another source of inefficiency [48].

2.5.3. LYSO crystal

Scintillating LYSO (Cerium-doped Lutetium Yttrium Orthosilicat) crystals coupled to Silicon Photomultiplier devices (SiPM) are well known time-of-flight detectors used in Positron Emission Tomography (PET) to improve the image signal-to-noise ratio. The HEP community takes advantage of the advancements of this technology in the medical imaging field to use it in vertex reconstruction.

When a charged particle enters the LYSO crystal, it interacts and begins the shower, producing scintillation light. The scintillation light travels from the point of interaction to the SiPM, where the photons are converted into an electrical

signal. A representation of the crystal coupled to the SiPM is shown in Fig. 2. 19. a). A SiPM consists of a matrix of microcells all connected in parallel. Each microcell is a Geiger-Mode avalanche photodiode working beyond the breakdown voltage, which integrates a resistor (R_Q) for passive quenching. A cross-section and top view of a SiPM are presented in Fig. 2. 19. b) and c), respectively.

It has been demonstrated that 3mm LYSO crystal, read out with an SiPM, can achieve a time resolution in the range of 20 ps for charged particles [49]. The radiation hardness of LYSO crystals against gamma rays [50], neutrons [51] and protons [52] has been found to satisfy the radiation hardness required at the HL-LHC. But the SiPM shows a vast decrease in the signal-to-noise ratio (SNR) after proton irradiation to $2 \cdot 10^{14}$ n_{eq}/cm^2 [53]. Thus, LYSO crystals are proposed for the barrel timing layer where the expected radiation fluence is lower than the forward end-cap.

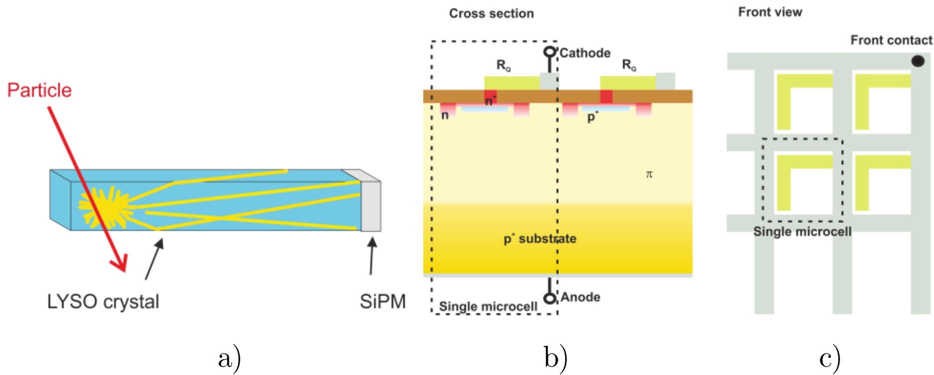


Fig. 2. 19. Illustration of the LySO(Ce) scintillator and the SiPM readout a), cross-section of a SiPM b), and top view of a SiPM c).

SiPM can be used as a direct particle detector with an excellent time resolution, but their gain sensitivity to temperature and bias voltage, crosstalk, high noise and low radiation resistance make them not an optimum choice for hard radiation environments. An excellent detector to carry out tracking and timing will be Avalanche Photodiodes (APD) working in the lineal mode with enough gain to improve the SNR without worsening the noise level and avoiding the problems of high gain as crosstalk. At the same time, the detector structure must be suited to detect charged particles and work in hard radiation environments. This is the idea of Low Gain Avalanche Detectors (LGAD), as it will be presented in section LGAD 2.5.5.1.

2.5.4. Diamond sensors

Detectors based on CVD diamond have several advantages over other semiconductor detectors, e.g. silicon detectors: their radiation hardness, low noise level, etc. A high resistivity ($> 10^{11}\ \Omega \cdot$ cm) coupled to a large electronic gap (5.48 eV) results in a lower noise level and an almost negligible leakage current even at room temperature. But a large electronic gap also means that the amount of charge in the detector is lower than in silicon ones, 36 e-h pairs per micrometer [54]. Then the use of low noise amplifiers is mandatory to obtain a good S/N ratio and time resolution. Time resolution in the range of 100 ps per layer has been achieved with single crystal diamond detectors for relativistic protons [55].

2.5.5. Silicon sensors

Silicon detectors are commonly used as tracking detector with micrometric space resolution or as spectrometers [40], but they can also be used as a timing detector. In order to achieve a sub-nanosecond time resolution, intrinsic fluctuations of the charge collection time inside the sensor must be minimized. This can be achieved by designing pixel geometry with a uniform weighting field and by saturating the carrier drift velocity in the whole sensor volume. Under this assumption, the jitter of the detector is in the range of 100 ps per layer for a 100 µm thick silicon pixel [56].

As aforementioned in section 2.5.3, SiPM detectors can be used as a direct particle detector with an excellent time resolution, but they are not optimized for hard radiation environments. On the other hand, Avalanche Photodiodes (APD) detectors working on lineal mode improve the time resolution avoiding the drawbacks of high gain. It is in this context that Low Gain Avalanche Detectors (LGAD) have been developed and characterized. The idea of LGAD detectors has been the development of customized APD detectors, which are used as direct particle detectors, increasing their lineal mode and optimizing their radiation hardness. During the last four years the RD50 collaboration has worked in the development and characterization of LGAD sensors with lower time resolution and better radiation hardness than standard p-i-n diodes, in a view to withstanding the foreseen fluence of HL-LHC.

2.5.5.1. LGAD

LGAD detectors are customized Reach-Through Avalanche Photodiodes (APD) for particle tracking and Time-of-Arrival measurement. The difference between LGAD

and standard APD detectors is that LGAD detectors are optimized to detect charged particles with a gain in the range of ten. LGAD works in the lineal mode in all the bias range, therefore detectors do not need a quenching system, there is no crosstalk between pixels, and the signal does not exceed the dynamic range of readout electronics.

The first LGAD diode detectors were produced at IMB-CNM's clean room facilities [57], by diffusing a p-type layer just below the n^+ electrode, as shown in the schematic cross section of Fig. 2. 20. b). Thus, an $n^+/p/p^-$ junction is created along the center of the electrodes. Under reverse bias conditions, a high electric field is generated in this localized region, which triggers the impact ionization caused by electrons reaching the n^+ electrode. The main technological parameters of the p-type multiplication layer are the implantation dose and the final depth. An optimum and uniform multiplication layer is pivotal in ensuring a high voltage capability and enough uniform gain to obtain a pulse shape with a good time resolution. As shown in previous studies [20], [58], [59], modification of 10% in the boron implant dose can induce enormous changes on the gain and breakdown voltage values.

Two common termination structures used in power devices to avoid the breakdown at the edge cylindrical junction, namely Junction Termination Extension (JTE) and Field Plate (FP), have been implemented at the edge of the main planar junction [60]. A detailed explanation of these termination structures is presented in section 3.1.1.2. A complete study of the edge termination for an LGAD is reported in reference [20], [58].

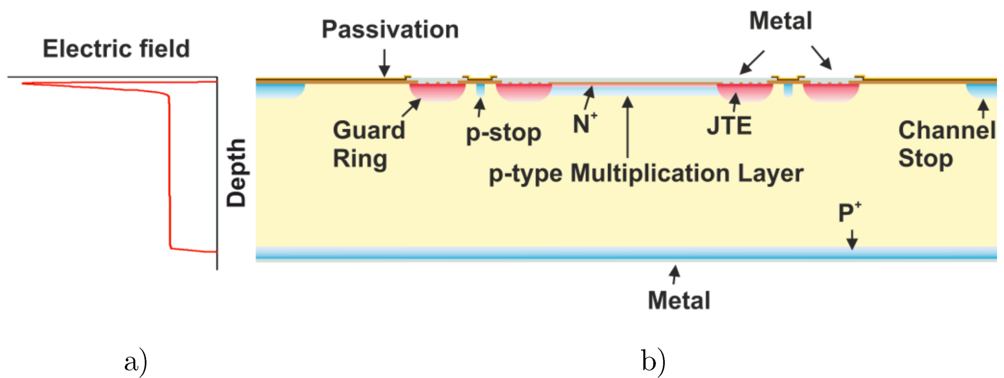


Fig. 2. 20. Electric field cutline in the multiplication region a). Schematic cross-section of an LGAD structure on 285 µm thick high resistivity p-type wafer b).

2.6. Radiation Damage

Another aspect that must be taken into account is the radiation resistance of the LGADs. During the HL-LHC operation they will have to withstand fluences between $2 \cdot 10^{15}$ n_{eq}/cm^2 and $1 \cdot 10^{16}$ n_{eq}/cm^2, depending on the pseudorapidity they cover. A straightforward explanation of the radiation damage in detectors will be given in this section.

Silicon devices are affected by two basic radiation damage mechanisms: ionization damage and displacement damage. Both mechanisms are important in detectors. While some devices are more sensitive to ionization effects, others are dominated by displacement damage.

2.6.1. Ionizing Damage

The energy absorbed by ionization in insulating layers as SiO_2, creates electron-hole pairs, which diffuse or drift to other locations where they are trapped. While electrons move to the most positive electrode, holes move by a complex and slow hopping mechanism, which promotes the probability of trapping in the oxide volume with an associated fixed positive charge. The holes that reach the oxide-silicon interface can be captured by interface traps, which are a consequence of the lattice mismatch at the oxide-silicon interface or impurities trapped at the oxide-silicon interface. Hole trapping results in an increase of the oxide positive charge. This charge build-up saturates at a value close to $2 \cdot 10^{12}$ cm^{-3} after a dose of about 100kRad. In summary, ionizing damage introduces oxide charges and interface traps, which strongly influence the break-down voltage, the inter-electrode isolation and capacitance, and might also impact the charge collection properties of silicon detectors.

2.6.2. Displacement Damage

Displacement damage occurs when a sufficient amount of energy is transferred from an incident energetic particle to a lattice atom, resulting in a dislodgement of the atom from its normal location. The silicon atom initially displaced by an incoming particle is known as the primary knock-on atom (PKA) or the primary recoil. Lattice defects are produced by PKAs and any later-generation energetic recoils that they create.

In the simplest scenario, the initially created defects are vacancies and interstitials, where a vacancy is the absence of an atom from its normal lattice position and an

interstitial is a dislodged atom that resides in a non-lattice position. A vacancy and a nearby interstitial are known as a Frenkel pair. A common defect produced in semiconductors is the divacancy, which is formed by two adjacent vacancies. Larger groups of vacancies and defect-impurity complexes may also be created. Defect-impurity complexes are combinations of vacancies or interstitials with impurities. When defects created by incident radiation are relatively far distant from each other, they are known as point defects. Radiation-induced defects may also be produced close to each other and form a local region of disorder known as defect clusters. Energetic incident particle on silicon create either isolated and clustered defects or solely point defects, depending on their mass and energy.

All the effects of displacement damage on the electrical and optical properties of silicon and devices can be understood in terms of energy levels introduced in the bandgap. Those radiation-induced levels result in the following effects: an increase of thermal generation of electron-hole pairs through a level near midgap, a recombination of electron-hole pairs in recombination centers, a temporary trapping of carriers at a typically shallow level, a compensation of donors or acceptors by radiation-induced centers, a tunneling of carrier through a potential barrier by means of defect levels, a decrease in carrier mobility caused by defects that act as scattering centers, type inversion due to carrier removal, and an enhancement of the thermal generation of electron-hole pairs in the presence of a sufficiently high electric field. Table 2. 2 and Fig. 2. 21 offer a review of the most relevant defects in silicon, as well as their properties and effects in detector characteristics [61]. More detailed information about defects and characterization methods can be consulted in references [61], [62] and references therein.

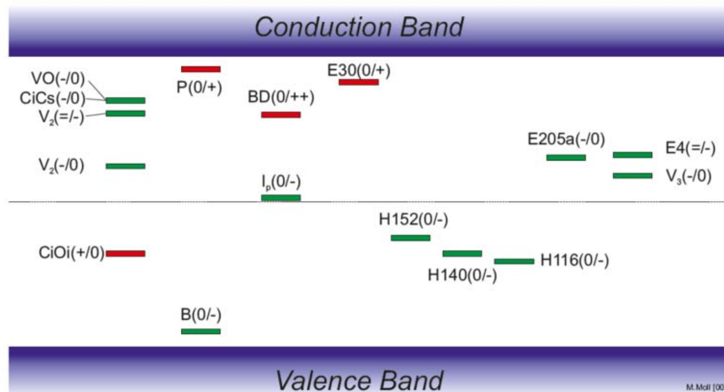


Fig. 2. 21. Schematic representation of a selection of defect levels generated by radiation in the silicon band gap. Donors are indicated in red while acceptors are given in green. Figure taken from [62].

Table 2. 2: Electrical properties of point and extended defects relevant for detector operation. Table taken from [62].

Defect	Transition	Level(s) [eV]	$\sigma_{e,h}$ [cm²]	Comment
E(30K)	(0/+)	$E_C - 0.1$	$\sigma_e=2.3\times10^{-14}$	Donor level, contributes in full concentration with positive space charge to N_{eff}, strongly generated after charged particle irradiation with linear fluence dependence.
BD_A **BD_B**	(0/++) (+/++)	$E_C - 0.225$ $E_C - 0.15$	$\sigma_e=2.3\times10^{-14}$ $\sigma_e=2.7\times10^{-12}$	Point defect, TDD2, bistable donor existing in configuration A and B, strongly generated in O rich material, contributing in full concentration to positive space charge.
I_p	(+/0) (0/-)	$E_V + 0.23$ $E_C - 0.545$	$\sigma_h=(0.5\text{-}9)\times10^{-15}$ $\sigma_e=1.7\times10^{-15}$ $\sigma_h=9\times10^{-14}$	Not identified point defect generated via second order process (quadratic fluence dependence), strongly generated in O lean material, acceptor level contributing to current and N_{eff}.
E_{75} **E4** **E5**	(-/0) (=/-) (-/0)	$E_C - 0.075$ $E_C - 0.359$ $E_C - 0.458$	$\sigma_e=3.7\times10^{-15}$ $\sigma_e=2.15\times10^{-15}$ $\sigma_e=2.4\times10^{-15}$ $\sigma_h=2.15\times10^{-13}$	Tri-Vacancy (V_3), bistable defect existing in 2 configurations: FFC(E_{75}) and PHR (E4,E5), E5 is contributing to leakage current, linear fluence dependence.
H(116K) **H(140K)** **H(152K)**	(0/-) (0/-) (0/-)	$E_V + 0.33$ $E_V + 0.36$ $E_V + 0.42$	$\sigma_h=4\times10^{-14}$ $\sigma_h=2.5\times10^{-15}$ $\sigma_h=2.3\times10^{-14}$	Linear fluence dependence, contributing in full concentration negative space charge, responsible of reverse annealing.
B_iO_i	(0/+)	$E_C - 0.23$		Dominant Boron related defect (electron trap) in oxygen rich Silicon, created during acceptor removal.

In summary, displacement damage creates new energy levels which alter the performance of detectors. Macroscopic radiation-induced effects observed in silicon detectors are: leakage current increase, effective space charge increase, charge trapping, acceptor and donor removal, and double junction effect. Those effects will be explained in detail in the next sections.

2.6.2.1. Increase of the carrier thermal generation

Radiation-induced defect levels close to midgap are very efficient charge carrier generation centers that lead to an increase of the leakage current of silicon detectors.

After exposure to highly energetic particles with sufficient energy to produce defect clusters, the radiation induced increase of the leakage current is proportional to the particle fluence, regardless of the type, resistivity and impurity content of the used silicon material. Thus the leakage current after irradiation is

$$I_{det} = I_0 + \alpha \cdot \Phi \cdot V \qquad \text{Eq. 2. 7}$$

where I_0 is the leakage current before irradiation, α is a damage coefficient dependent on particle type and fluence, Φ is the particle fluence, and V is the detector volume. The value of α is $2 \cdot 10^{-17}$ A/cm for standard p-i-n detectors, which are irradiated to 1 MeV neutrons [61].

Leakage current is strongly dependent on temperature, as it can be seen in Eq. 2. 8.

$$I(T) \propto T^2 e^{-E_{eff}/2k_B T} \qquad \text{Eq. 2. 8}$$

where E_{eff} = 1.214 ± 0.014 eV [63]. Even after rather low fluences, the generation current dominates. A way to reduce the leakage current of irradiated detectors is the reduction of the temperature. Thus, the measurement of irradiated detectors is performed at low temperatures, usually -20 ºC, in order to avoid saturation of the electronics, high noise, and power dissipation.

2.6.2.2. Change of the Effective Doping Concentration

The radiation induced defects lead to a change in the effective space charge N_{eff}, which is reflected in a change of the depletion voltage V_{FD} of the detector. The depletion voltage is given by

$$V_{FD} = \frac{q\,|N_{eff}|d^2}{2\varepsilon_{Si}} \qquad \text{Eq. 2. 9}$$

where d is the thickness of the device, q the elementary charge and ε_{Si} the permittivity of silicon. The last equation assumes that the space charge is constant over the volume of the damaged detector, but this is not always the case [64].

2.6.2.3. Temporary trapping

The electron-hole pairs created by ionizing radiation in the depleted bulk of the detector are drifted towards the electrodes, generating the sensor signal, as seen in section 2.3.1.2. If a charge carrier is trapped into a defect level and not released within the signal collection time of the detector, the charge is lost and the signal reduced.

Trapping depends on particle fluence: the higher defect concentration, the more charge carriers get trapped. Therefore, the signal height or the Charge Collection Efficiency (CCE) decreases with increasing radiation fluence. The charge inside the sensor is described by

$$Q(t) = Q_0 \cdot e^{(-t/\tau_{eff})} \qquad \text{Eq. 2. 10}$$

where Q_0 is the charge generated in the sensor and τ_{eff} is the effective trapping time. A linear dependence of the inverse effective trapping time on the particle fluence is observed and described as

$$1/\tau_{eff} = 1/\tau_{eff,0} + \beta\Phi \qquad \text{Eq. 2. 11}$$

where β is the effective trapping damage constant and $\tau_{eff,0}$ the effective carrier lifetime before irradiation. The effective trapping damage for electrons and holes has been measured for various silicon materials (Float Zone , Diffusion Oxygenated Float Zone, Magnetic Czochralski, and Epitaxial) and different heavy particle irradiations, obtaining similar results of β: 4 to 6×10^{-16} cm^2/ns for electrons and 5 to 8×10^{-16} cm^2/ns for holes [65]–[67].

2.6.2.4. Acceptor and Donor removal

During nonionizing radiation, the acceptor's (donor's) impurities are dislodged from their electrically active position in the silicon cell. Those impurities can interact with vacancies, divacancies, interstitials and bigger complexes, creating an impurity complex where the acceptors (donors) are not electrically active anymore. The negative (positive) space charge contributed by the shallow dopants is therefore lost and the overall space charge is altered.

The removal of phosphorus and boron by irradiation with fast neutrons has been

studied and measured by Wunstorf et al. [68]. The donors' (acceptors') removal shows an exponential decrease with the fluence as

$$N_{D(A)}(\Phi) = N_{D(A),0}e^{-c_{D(A)}\cdot\Phi} \qquad \text{Eq. 2. 12}$$

where the removal coefficients in high resitivity materials were determined to be $c_D = 2.4\times10^{-13}$ cm^2 for phosphorous and $c_A = 2.0\times10^{-13}$ cm^2 for boron.

Donegani et al. [69], [70] measured a peak related to the defect B_iO_i in p-type proton irradiated sensors using Thermally Stimulated Current spectroscopy (TSC). Boron dislodged from its substitutional position and located in an interstitial position interacts with interstitial oxygen because it is energetically more favourable. This is the cause of the Boron removal. Thus, the reduction of interstitial oxygen O_i in the substrate will reduce the boron removal.

2.6.2.5. The double junction effect

Eq. 2. 9 assumes a constant and homogeneously distributed over the sensor bulk space charge. The electric field is assumed to be a linear function of the depth in the sensor, but this is not actually the case. Only for non-irradiated detectors or low irradiation fluences can the space charge be assumed to be constant throughout the depleted volume. Detectors irradiated to higher fluences show a strong electric field that starts to grow from the back electrode when raising the reverse bias over the sensor, while a field growing form the front side is observed at the same time. The formation of the double peak field is explained by a polarization effect [64].

The Transient Current Technique (TCT) allows to characterize and visualize the electric field distribution [71]. Experimental measurements and more detailed explanation of the double junction effect can be consulted in reference [64], [72].

It is assumed that the double junction effect is also responsible for the gain decrease on LGADs. At a given reverse voltage, the increase of the electric field peak on the back side of the sensor must produce a decrease of the electric field peak on the front side, as it can be seen in Fig. 2. 22.

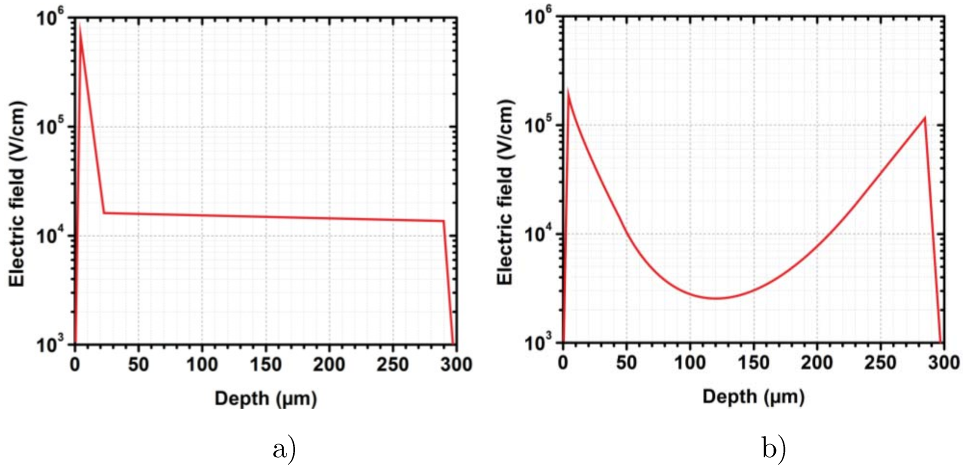
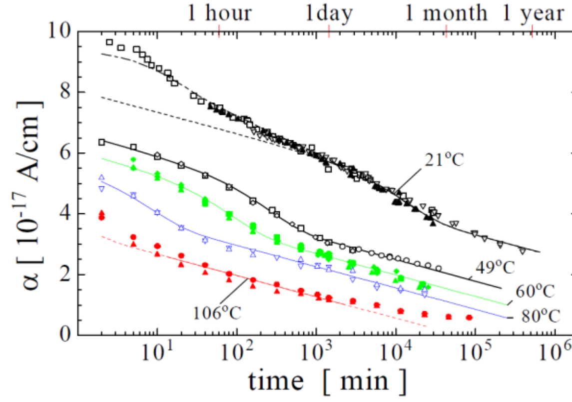


Fig. 2. 22. Schematic representation of the electric field distribution in non-irradiated LGAD a) and the double junction effect in irradiated LGAD b).

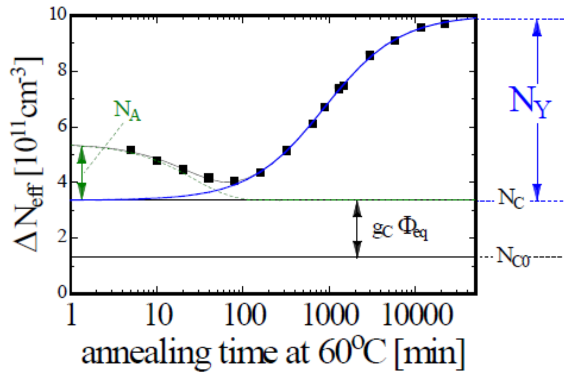
2.6.3. Annealing

The effects caused by radiation can be reduced with time, temperature or carrier injection annealing. Annealing of the leakage current, depletion voltage and trapping has been studied by the HEP community over the last decades.

The evolution of current related damage factor α as a function of the annealing time at different temperatures, ranging from 21 ºC to 106 ºC, was measured in reference [73] for irradiated detectors produced from materials with different resistivities and oxygen concentrations. Fig. 2. 23. a) shows the decreasing behavior of α with increasing annealing time.



a)



b)

Fig. 2. 23. current related damage factor α as a function of the accumulated annealing time at different temperatures a). Evolution of the effective doping concentration as a function of the annealing time at 60ºC b). Figures a) and b) are taken from [61] and [62] respectively.

The effective doping concentration also decreases as a function of annealing time until 80 minutes, as it can be seen in Fig. 2. 23. b), [62]. After that annealing time, the effective doping concentration shows a reverse annealing effect and start increasing. The annealing beneficial time at 60 ºC is 80 minutes, which becomes the annealing usually used by the HEP community.

Finally, the effective trapping damage constant also depends on the annealing time after irradiation, as it is shown in Fig. 2. 24. While a reduction in β_e with annealing time is observed, an increase of trapping with time has been measured in holes [74].

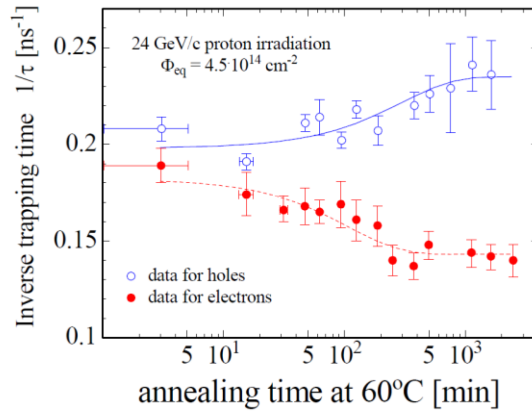
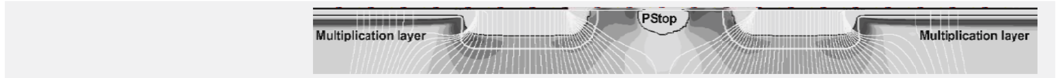


Fig. 2. 24. Inverse trapping time evolution as a function of the annealing time at 60ºC. Taken from [74].

3. TECHNOLOGICAL AND ELECTRICAL OPTIMIZED DESIGNS



The designs of silicon radiation detectors for the new timing layers of the ATLAS and CMS experiments are introduced in this chapter.

Before the production of new devices starts at IMB-CNM's clean room, the design of the new sensors must guarantee that they are going to fulfill the specifications. Technology Computer Aided Design (TCAD) is a category of software tools for modeling both semiconductor fabrication and semiconductor device operation, which allows us to validate the optimum design of the device before the expensive fabrication begins. The performance of detectors can be optimized for their final purpose with these tools.

In order to achieve a better design of the new devices, It is important to calibrate the LGAD process simulation. SPROCESS is the Synopsys TCAD tool for simulating the LGAD technological process. The experimental doping profiles, obtained by Second Ion Mass Spectrometry (SIMS), are compared with the simulated doping profile to tune the simulation. Once the technological simulation is calibrated, the electrical performances of detectors are simulated with Synopsys TCAD (SDEVICE) to compare them with the experimental measurements. Finally, the designs of the new HGTD, CT-PPS, AC-LGAD detectors are optimized using SDEVICE, in order to find the parameters with which the detectors achieve their maximum voltage capability.

3.1. LGAD technological process simulation

Physically-based process simulators predict the structures that result from specified process sequences. This is done by solving systems of equations that describe the physics and chemistry of semiconductor processes using the Finite Element Method [75]. The process to be simulated must be defined by specifying the initial geometry of the structure, sequence of process steps (oxidation, implantation, diffusion, etching, deposition) and physical models to be used.

In this section, the LGAD layout, process simulation with SPROCESS, and physical models are explained.

3.1.1. LGAD layout

LGAD detectors are processed on high resistivity (HR) p-type doped with boron silicon wafers using planar technology. P-type substrates are used because, unlike n-type substrates, they do not invert the substrate type after irradiation due to donor removal and defect formation. Different protection structures have been used to improve the voltage capability of LGADs, as shown in Fig. 3. 1. The LGAD is divided in two regions: the active region, where all the generated electrons are collected by the n^+ electrode, and the periphery, which protects the main planar junction (n^+/p) and guarantees that the depletion region does not reach the detector edge. In the following sections the main structures are briefly explained.

3.1.1.1. P-stop

The major issue in HR p-type substrates is that positive charges are created during oxidation at the oxide/silicon interface. These positive charges attract electrons from the bulk to the silicon surface just below the oxide, creating an n-type layer. The inversion layer reduces the resistance between pixels and strips and short-circuits the n^+ electrodes. This effect is relevant in substrates with low doping concentration. The p-stop is a p-type implant surrounding the n^+ electrode, which interrupts the inversion layer and isolates the n^+ electrodes [76], [77]. The implementation of the p-stop structure in devices requires an additional photolithography step. The concentration of boron in the p-stop must be high enough to counteract the inversion layer, but not too high, since an excessive concentration would create an intense electric field at the edges of the p-stop that cause microdischarges in the leakage current, electronic noise and early breakdown.

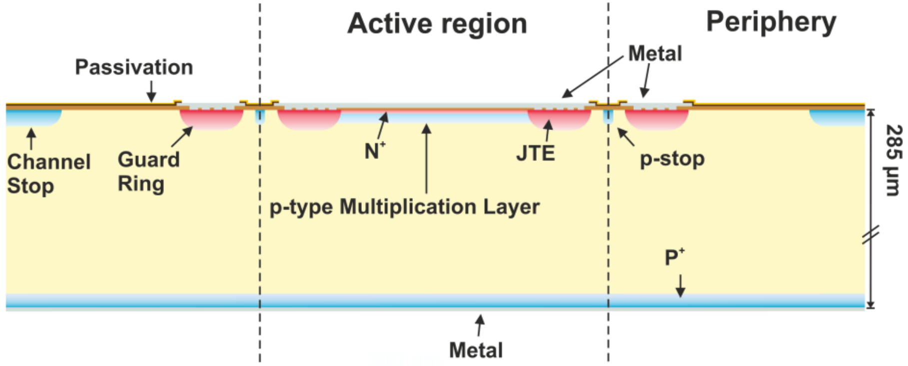


Fig. 3. 1. LGAD cross-section representation. In blue are represented the Boron implants and in red the phosphorus implants. The different protection structures and implants are indicated: p-stop, channel stop, JTE, guard ring, p^+ electrode, n^+ electrode.

Similar to the p-stop, the channel stop structure is also implemented using the same mask level. It is also a p-doped implant near the dicing path, which stops the progress of depletion along the surface. Then, the depletion region does not reach the damaged edge of the detector, avoiding an increase in the leakage current due to both the dislocations and traps introduced during the dicing of the detector. The channel stop and p-stop are depicted in the cross-section representation of the LGAD (Fig. 3. 1.).

3.1.1.2. Junction Termination Extension and Field Plate

When impurities are implanted, part of them is not active because they are not located in a substitutional site of the silicon cell. In order to diffuse the impurities to a substitutional position, a thermal process is carried out. The diffusion is done in all directions into the substrate. That means that the impurities diffuse into both the depth and the lateral of the substrate. The transversal diffusion of the impurities creates both cylindrical and spherical junctions at the edge of the main planar junction, where the electric field is higher than the electric field in the planar junction. Thus the electric field at the edge reaches the critic electric field earlier at the edge than at the planar junction [60]. As a consequence, the breakdown voltages of both cylindrical and spherical junctions are lower than that of a planar junction. Although the spherical junction is avoided designing round vertex, the cylindrical junction cannot be avoided with designing rules. A common protection structure, which changes the electric field distribution, avoiding premature breakdown at the edge of a planar junction, is the Junction Termination Extension (JTE) [60] . The JTE is an n-type diffusion, which is implanted along

the edge of the n^+ electrode and diffused deeper into the substrate than the n^+ electrode. The breakdown voltage at the edge of the JTE is higher than at the n^+ electrode, since the radius of the cylindrical junction between the JTE and the substrate is larger than between the n^+ and the substrate. The JTE implant requires another mask level to be implanted after the p-stop level.

Another protection structure used to increase the breakdown voltage is the field plate (FP). The FP is the extension of the contact metal from the n^+ over the field oxide at the edge of the junction, as shown in Fig. 3. 2. When a positive bias is applied at the metal contact to deplete the device bulk, electrons are attracted to the surface, causing an expansion of the depletion region at the surface, as indicated by line B in Fig. 3. 2. Thus, the field plate decreases the electric field at the cylindrical junction.

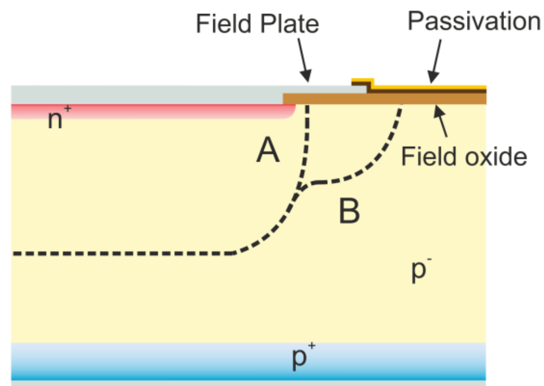


Fig. 3. 2. Representation of a planar junction with a metal field plate over the field oxide. Depletion regions of the same planar junction without and with field plate are indicated by A and B lines, respectively

3.1.1.3. Guard Ring

The Guard Ring (GR) is another structure which protects the planar junction from an early breakdown. The GR can be biased or left floating. When the GR and the main planar junction are biased simultaneously at the same voltage, the leakage current generated at the periphery of the detector is collected by the GR. This method is an elegant solution to reduce the thermal noise at the main planar junction. The guard ring can be left floating, as well. Although, the guard ring is floating and no voltage is applied, the potential of the guard ring is non-zero due to the punch-through mechanism, but it is lower than at the main n^+ electrode. In this case, the electrons from the peripheral generation current are collected by the floating GR and flow from there into the biased n^+ electrode [78]. As a consequence, the thermal noise related to the whole periphery is also collected by

the n^+ electrode. Thus, the GR of LGAD detectors is biased to reduce the noise at the main planar junction.

If the spacing between the guard ring and the n^+ is too close, the electric field increases at the edge of both the guard ring and the main junction, due to the punch-through, causing the breakdown of the device. On the contrary, if the guard ring is too far from the main junction, the guard ring does not change the electric field and the breakdown takes place at edge of the main junction. The optimum location of the guard ring was determined by TCAD simulation in previous studies [58], [59].

The guard ring is implemented at the same mask level as the JTE. The standard width of the guard ring, in order to facilitate the wire bonding, is 120 µm but it is not mandatory to have the same width along the ring. As it will be shown in the CT-PPS layout, the guard ring can be narrow at the edge closer to the beam, in order to minimize the periphery of the device at this region.

3.1.2. Technological process

The process simulation starts with the definition of the initial grid, the wafer type, orientation and resistivity. As aforementioned, the TCAD uses the Finite Element Method to solve the physic models of the structure. The definition of a good grid is crucial, in order to avoid convergence problems during the simulation. Remeshing strategies at structure boundaries and interface, in order to refine the grid, are implemented in the simulation.

After the initialization of the grid and the definition of the wafer specifications, the growth of 0.8 µm field oxide, using a wet oxidation, is simulated following the clean room recipe. Afterwards, the following process flow is simulated:

- Photolithography of the p-stop level, boron implantation and posterior diffusion of the implanted boron.
- Photolithography of the JTE level, phosphorus implantation and posterior diffusion of the implanted phosphorus.
- Photolithography of the PWell level (multiplication layer), boron implantation and posterior diffusion.
- Photolithography of the n^+ level, phosphorus implantation and diffusion of the implanted phosphorus.
- Contact opening

- Metallization and photolithography of the metal level
- Passivation and photolithography of the passivation level.

A diagram of the process flow is presented in Fig. 3. 3. The doping profile of boron and phosphorus after the last diffusion of the n^+ electrode is not affected by the following processes, contact opening, metallization and passivation, because they are done at low temperature.

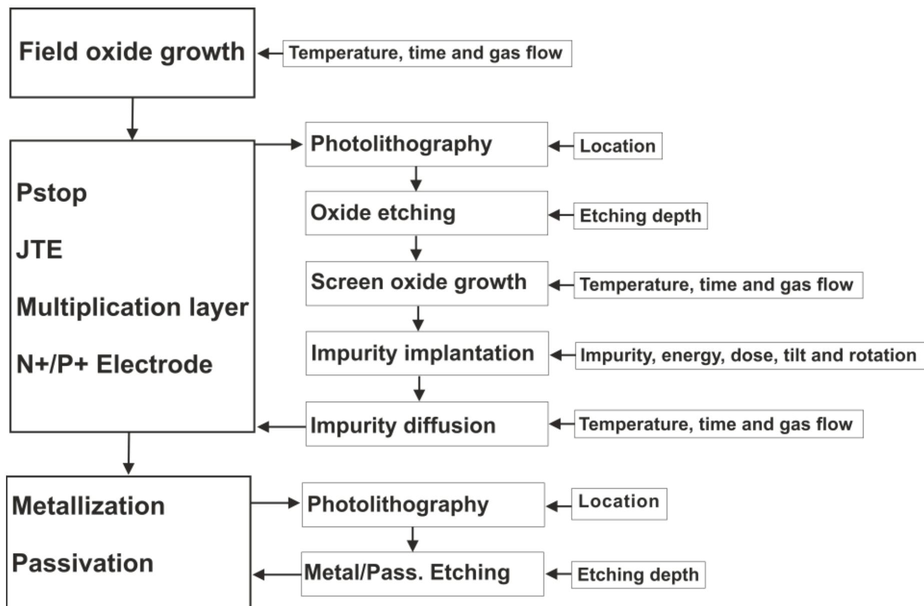


Fig. 3. 3. Schematic diagram of the LGAD process flow

3.1.3. Physic models

The simulation is done selecting the advanced calibration file, which is a selection of models and parameters for an accurate process simulation. The relevant physic models of the advanced calibration file are summarized in Table 3. 1. More detailed information about the advanced calibration file can be consulted in references [79], [80].

Dopants are diffused in silicon via silicon point defects; vacancies (V) and interstitials (I). An excellent explanation of the different dopant-point defects mechanism can be found in references [81]–[84]. Observed effects as the Oxidation Enhanced Diffussion (OED), the Oxidation Retarded Diffusion (ORD), the Transient Enhanced Diffusion (TED), are explained by the dopant-point defect

diffusion. The ChargedReact diffusion model is the most general transport model in Sentaurus Process. The model has an immobile substitutional dopant and two mobile charged dopant-defect pair species (V and I). The diffusion of dopants is simulated through dopant-defect pairs.

Table 3. 1: Physic models switched on with advanced calibration file

Diffusion model	ChargedReact
Activation model	Transient
Surface recombination model	Pair Segregation
Implant data	coimplantation

Dopant cluster models govern the dopant activation during thermal annealing. The Transient cluster model is switched on by default in the advanced calibrations. In this model, dopants can be bound in clusters of only one species. The Transient cluster model gives satisfactory results in many situations.

In the pair segregation surface recombination model, when a dopant-defect pair diffuses to the interface between semiconductor and oxide, the dopant may enter the oxide, whereas the point defect remains on the silicon side of the interface. The point defects released in silicon may have any charge state.

The coimplantation model takes into account the lowering in the channeling tail of the analytic implantation due to the damage present in silicon after the first implantation without an annealing step in between implantations.

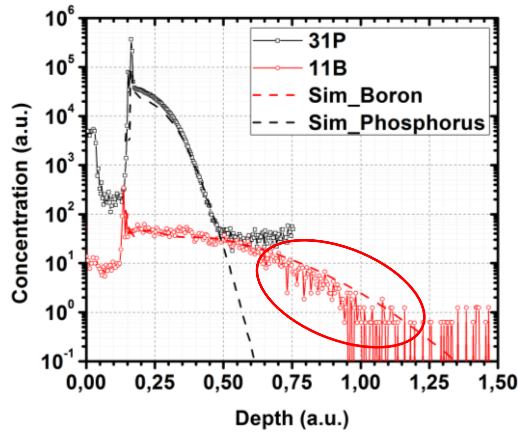
Generally, the TCAD default diffusion parameters are used for the simulation, although the diffusion parameters for Gallium are taken from Pichler [85], which gives an exhaustive overview on the publications of impurity diffusion and activation in silicon.

3.1.4. Calibration of LGAD simulations with the experimental doping profiles

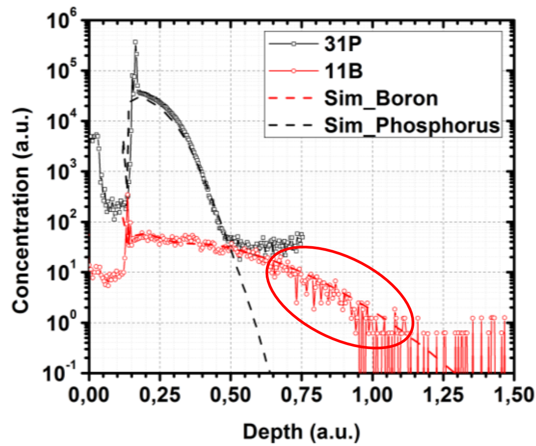
SIMS data are crucial to calibrate the process. This data provides information about the diffusivity and segregation of the dopant. The SIMS consists in a beam of energetic heavy ions, which erodes away the surface, while secondary ions produced in the sputtering process are mass analyzed and detected [86]. SIMS is a

destructive technique but it has better resolution than other profiling techniques as the spreading resistances.

After the definition of the LGAD process simulation, a fine-tuning of some parameters is peformed to match the simulated profile with the experimental doping profile obtained by SIMS. This fine-tuning consists in the adjustment of the segregation parameters and the diffusion factors. Fig. 3. 4. a) shows the experimental phosphorus and boron profiles of an LGAD in open symbols and solid lines, while the simulated profiles are plotted in dashed lines, before the fine-tuning. The plots are shown in arbitrary units due to the confidentiality of this information. As it can be seen, the tail of the simulated boron profile is longer than the tail of the experimental boron profile. In order to reduce this boron tail, the diffusion coefficient of the B^-I^- is increased. Fig. 3. 4. b) presents the boron and phosphorus profiles after the fine-tuning of the diffusion parameters.



a)



b)

Fig. 3. 4. Comparison between the Boron and phosphorus doping profiles obtained by simulation with the experimental profiles obtained by SIMS before fine tuning a) and after fine tuning of the parameters b)

Once the LGAD process simulation is well calibrated, it becomes a valuable tool to simulate different LGAD designs and thicknesses, e.g. HGTD and CT-PPS detectors, before their fabrication.

3.1.5. Radiation hardness strategies for LGAD detectors

Recent studies on LGAD show that the multiplication layer of neutron irradiated devices is affected by boron removal, which consequently decreases the gain of detectors [87]. Therefore, the timing resolution of the detectors is worsen by neutron radiation. This boron removal is caused by interstitial oxygen present in

the substrate [69], [70]. As mentioned before, the reduction of interstitial oxygen in the silicon substrates and the use of p-type dopants with a constant removal better than boron, as multiplication layer, are the proposed options to improve the radiation hardness of LGAD detectors.

The first option to counteract the boron removal is the implantation of carbon. The effect of carbon was studied previously for the RD48-ROSE collaboration [14]. Carbon is a non-electrically active impurity in silicon, which easily combines with interstitial oxygen O_i, reducing the concentration of O_i in the substrate. This reduction could reduce the boron removal, which causes the gain decrease in LGADs devices. Thus, an LGAD process with a carbon implantation on the whole device surface, called carbon spray, is designed and simulated for the production of new detectors.

The second option consists in the use of gallium as a dopant of the multiplication layer. Gallium is a p-type dopant which was extensively studied and used in solar cells. Different studies show the low acceptor removal constant of gallium, when it is compared to boron after electron irradiation [88]–[93]. Thus, the replacement of boron by gallium impurities in the multiplication layer is proposed for the new process.

In this section, the calibration of LGAD simulations with gallium impurities in the multiplication layer is presented. Following, the LGAD process with carbon spray is introduced as well.

3.1.5.1. Gallium technology process simulation

A new process with gallium implanted multiplication layers has been developed, in order to make LGADs more radiation resistance.

Gallium is a well-known diffuser in silicon, which presents a diffusivity in oxide that exceeds the other dopants diffusivity by orders of magnitude [94]. In the oxide-silicon interface, gallium tends to pile-up at the silicon side, but due to its fast diffusion through silicon oxide, the concentration of gallium at the silicon side decreases. Dopants diffuse slower in oxide than in silicon. Then, silicon oxide blocks the out-diffusion of dopants, which is the case of boron and phosphorus, but it is not the gallium case. Oxide does not act as a mask to block the out-diffusion of gallium. Thus, the thermal diffusion process of gallium should not use the silicon oxide as a mask.

First, the gallium implantation process has been simulated by TRIM and GEANT4, in order to obtain the optimum gallium implantation energy. TRIM and GEANT4 are Monte Carlo computer program that calculates the interactions of

energetic ions with matter. Results of the final average penetration depth of gallium into silicon are plotted in Fig. 3. 5. Three gallium implantation energies (160keV, 180keV, and 200 keV) were simulated. The implantation through a 38nm screen oxide, which is used to protect the processed surface, and a tilt of 7º, in order to avoid impurity channeling, are taken into account in the GEANT4 simulation.

Although an implantation energy of 160 keV is enough to penetrate into the silicon bulk, the highest gallium implantation energy available (195 keV) is chosen, in order to implant gallium impurities as deep as possible.

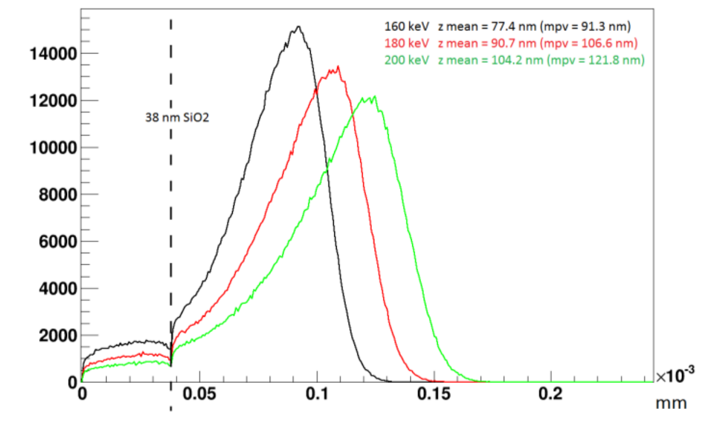


Fig. 3. 5. Gallium implantation range into silicon through a screen oxide of 38nm for three implantation energies; 160 keV, 180 keV, and 200 keV. (S. Esteban private communication).

Another important issue related to the technological process is the design of the thermal step, which activates and diffuses the implanted gallium. This step is performed by oxidation processes for standard boron doped LGAD detectors, but gallium activation and diffusion should be done by thermal processes in inert ambient (N_2), in order to avoid the diffusion of gallium through the oxide.

Physic models used for gallium simulation are the same ones used for standard LGAD simulation. Differences between processes are the gallium implantation and the following diffusion of gallium. Before the initialization of the process, the new dopant (gallium) must be defined, as well as the main characteristics of the new impurity must be set in SPROCESS. The process flow is the same as the flow presented in section 3.1.2.The simulation was done for five gallium implantation doses, which are called as Dose1, Dose2, Dose3, Dose4 and Dose5. In the next section, the comparison between experimental data and simulation is presented and discussed.

3.1.5.1.1. Calibration of Gallium simulation with experimental doping profiles

As aforementioned, the diffusion coefficients of gallium are taken from Pichler [85], changing the self-interstitials fraction to 0.95 [95]. SIMS doping profiles for gallium implantation (Dose2) are compared with the obtained ones by simulation in Fig. 3. 6. a). As it can be seen, the tail of the gallium simulation is longer than the tail of the experimental profile. Lowering the self-interstitials fraction to 0.65, as indicated by Tan et al. [96], together with an increase of the factor of $Ga^{-}V^{-}$ pairs reduce the gallium tail of the simulation, as shown in Fig. 3. 6. b). This calibration gives us a good match between experimental and simulated doping profiles.

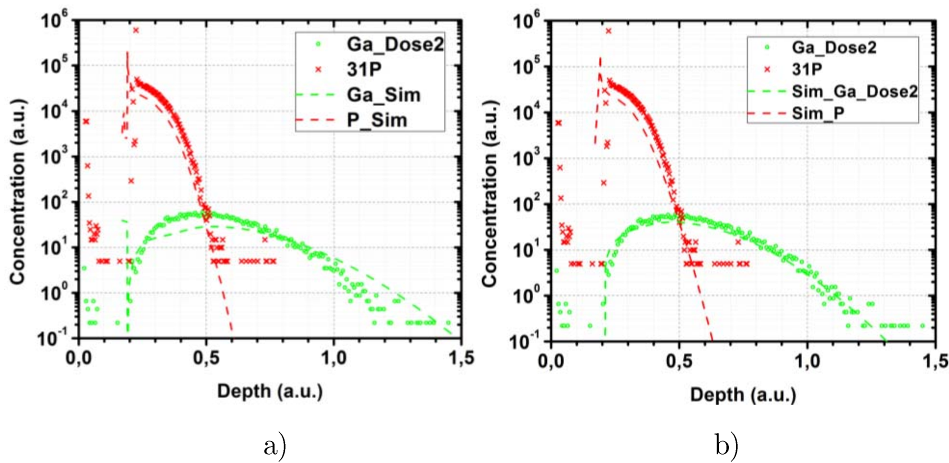


Fig. 3. 6. Comparison between the gallium and phosphorus doping profiles obtained by simulation with the experimental profiles obtained by SIMS, before the calibration a) and after the fine-tuning of the parameters b).

3.1.5.2. Carbon technological process simulation

Carbon is an electrically neutral impurity in silicon. Interstitial carbon (C_i) is highly mobile. These form C_i-O_i complexes after electron irradiation of the carbon doped CZ wafers [97]. Therefore, the concentration of O_i after irradiation is expected to decrease in presence of C_i. The carbon concentration should be in the same order of magnitude as the oxygen concentration. The oxygen concentration in float zone silicon wafers is less than 10^{16} at/cm^3 [98]. Thus, a carbon concentration in the range of 10^{16} at/cm^3 would be enough to suppress the O_i concentration after irradiation.

Furthermore, the introduced substitutional carbon is a sink of interstitials, which

decreases the concentration of interstitials. At high concentrations of substitutional carbon, the diffusion of boron and phosphorus are reduced due to the suppression of interstitials [81], [83], [85], [99], [100]. Therefore, it is crucial to verify that the implantation dose and energy of carbon does not change the phosphorus and boron doping profiles. In this section, the results of technological LGAD process simulations with carbon spray are presented.

Carbon can be implanted on the entire detector surface due to its electrical neutrality in silicon. Consequently, there is no need of a new mask level. Fig. 3. 7. presents the carbon and boron profiles obtained by simulation, where carbon is implanted through a 15 nm pedestal oxide on the whole wafer surface at the beginning of the LGAD process. Fig. 3. 7. a) shows the carbon profile for an implantation dose of $5 \cdot 10^{13}$ cm^{-2} and energy of 150 keV. In this case, the carbon is diffused 35 μm deep into the bulk. Although the carbon concentration is lower than the boron concentration at the multiplication layer, it is higher than the oxygen concentration in the silicon wafers. On the other hand, the carbon concentration for an implantation dose and energy of $4 \cdot 10^{14}$ cm^{-2} and 70 keV is equal to the boron concentration, as shown in Fig. 3. 7. b). Both implantation doses are enough to suppress the formation of B_i-O_i. At the same time, they are sufficiently low to avoid the formation of carbon clusters, which reduce the diffusion of boron and phosphorus [97], [101], [102]. Thus, the lowest implantation dose is chosen as the implantation dose for the carbon spray.

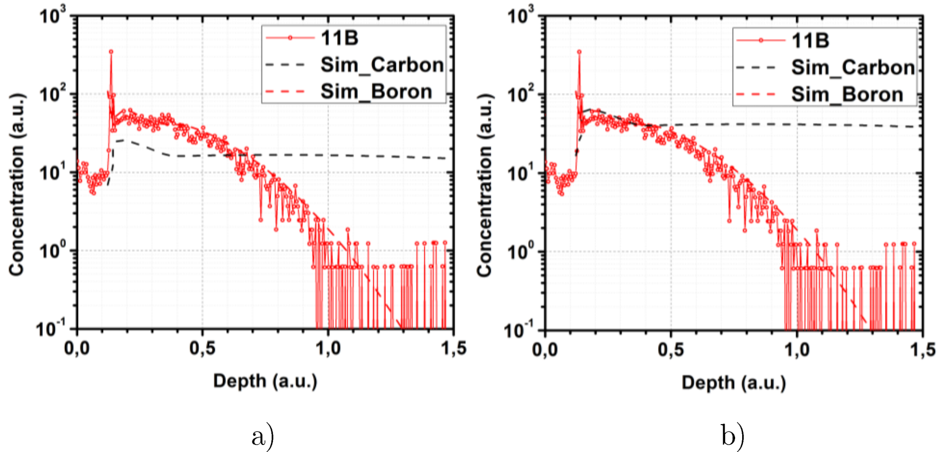


Fig. 3. 7. Carbon and boron profiles. The implantation dose and energy of carbon are $5 \cdot 10^{13}$ cm^{-2} and 150 keV a); and $4 \cdot 10^{14}$ cm^{-2} and 70 keV b).

3.2. LGAD electrical simulation

Sentaurus Device (SDEVICE) simulates numerically the electrical behavior of a single semiconductor device or several devices in a circuit. Terminal currents, voltages, and charges are computed based on a set of physical equations that describes the carrier distribution and conduction mechanisms. After the process simulation of LGAD detectors, the SDEVICE simulation is performed in the previous simulated devices. In the following sections, the IV, CV and gain of processed devices are simulated by SDEVICE and compared with the experimental results. Physic models, which were used in SDEVICE simulations, are presented in Appendix A. Finally, optimum design parameters of the new devices are found by simulation, before the new process starts at the clean room facility.

3.2.1. Multiplication region simulation

The simulation of a detector is divided in three regions: the multiplication region, the core or active region and the termination or periphery region. The multiplication region gives us the maximum voltage capability of the device, despite the design of the core region edge and the termination. The core region is the active part of the detector, which detects and multiplies the charged particles crossing this region of the detector. The termination region has two purposes. The first purpose is to protect from premature breakdown the core region, while guarantees the maximum voltage capability of the device. The second purpose is to prevent the space charge region from reaching the damaged edge of the detector.

The electrical characteristics and the charge collection process are simulated in the multiplication region of 300 µm thick LGAD detectors. In the next sections, the IV, CV and gain simulations are compared with the experimental data. Afterwards, the simulation of LGAD microstrips detectors, where the multiplication layer is segmented, is presented. The design and study of the termination region of LGAD detectors was done in previous studies [58], [59], and as a consequence, the termination of thick LGAD detectors is not discussed in the present work.

As it will be seen in the following sections, only a part of the given region is simulated, in order to minimize the number of points, where the equations are solved, speeding up the simulation. An area factor is introduced in the commands line to take into account this reduction and reproduce the characteristics of the whole detector area.

3.2.1.1. IV and CV

The structure, electrodes and physical models must be defined before starting the electrical simulation. In order to simulate the current as a function of the applied voltage, a quasistationary command is used to ramp the cathode (n^+ electrode) from 0V to 1000V, while the anode (p^+ electrode) is grounded. The simulation is carried out at 20 ºC for two different doses of the multiplication layer; $1.8 \cdot 10^{13}$ cm^{-2} and $2.0 \cdot 10^{13}$ cm^{-2} called as low and high dose, respectively. The simulation is done for all avalanche models available in SDEVICE: van Overstraeten, Lackner, UniBo and UniBo2. The avalanche model, which adjusts better to the experimental data, is the van Overstraeten one as it can be seen in the comparison between simulation and experimental data in Fig. 3. 8. Thus, the van Overstraeten model is the model set for the electrical simulations. Once the avalanche model is set in SDEVICE, the simulation of the current as a function of the reverse applied voltage is performed. Fig. 3. 9. a) presents the comparison between the simulation and the experimental data of the current in open symbols and dashed lines, respectively. The simulation agrees with the experimental data. In the low dose simulation, the difference between leakage currents becomes important due to edge and surface effects that are not taken into account in the simulation.

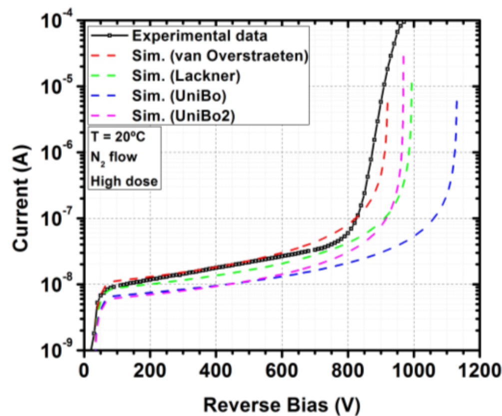
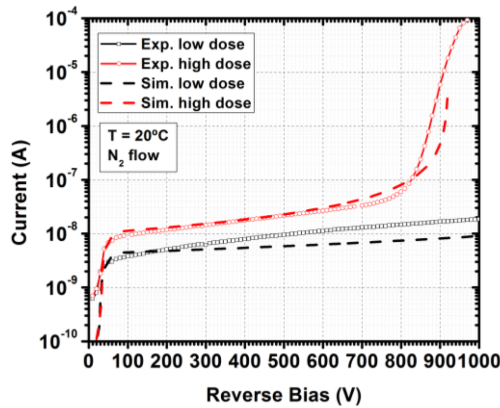
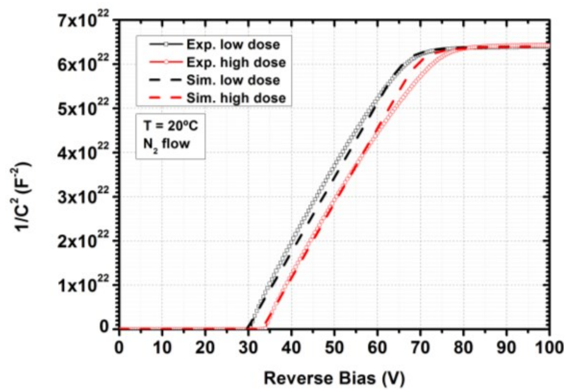


Fig. 3. 8. Comparison between the experimental data in open symbols and the simulation with different avalanche models in dashed lines.



a)



b)

Fig. 3. 9. Comparison between the experimental data in open symbols and the simulation in dashed lines of the IV a) and CV b) for 300 µm LGAD.

The simulation of the capacitance must be performed using the mixed mode. The mixed mode allows to simulate a circuit with multiple devices and components (e.g. resistors, capacitors, voltage sources, etc.), and extract the voltage, current, capacitance at each node of the circuit. First of all, a device section has to be introduced in the command lines, where the structure, physical models and electrodes are defined. The nodes of the circuit are defined in the system section of the commands lines. Once the device with a node in the cathode and another node in the anode are fixed, the SDEVICE computes the complex admittance, which specifies the current response at a given node to a small voltage signal applied at another node. The capacitance is calculated from the complex part of the admittance.

The plot of $1/C^2$ versus the reverse bias, which is obtained by simulation, is compared with the experimental data taken at 20 ºC and in dry ambient (N_2 flow)

in Fig. 3. 9. b). This plot gives us important information of detectors: the full depletion voltage and a rough estimation of the gain as well. LGAD detectors have a first slope between 0 V and 30 V, a second slope between 30 V and 70 V, and a third slope for voltages higher than 70 V. The first LGAD slope, which is named foot, is related to the multiplication layer concentration. The range of this slope gives a rough estimation of the gain. The experimental data for low implantation dose, which is presented in Fig. 3. 9. b) in black open symbols, exhibits a slope that extends up to 30V. In other words, 30 V is the required voltage to fully deplete the multiplication layer and it is indicated as V_{MD}. In the same example, a high implantation dose of the multiplication layer is plotted in red open symbols. This LGAD with a high dose implant shows a full depletion of the multiplication layer in the range of 34 V. Then, this device has a higher gain than the device with low implantation dose. Once the multiplication layer is fully depleted at 30 V (34 V), the space charge quickly spreads across the bulk until 65 V (70 V), where the device with low (high) implantation dose is fully depleted. The concentration of the substrate set in the simulation is calculated from this slope, as it is explained in section 2.3.1.1. After the full depletion of the detector, the capacitance remains constant. The simulated data is represented in black and red dashed lines. As it can be seen in Fig. 3. 9. b), the simulation reproduces the same foot as the experimental data for both implantation doses. The full depletion for both implantation doses is equal to the experimental data as well. Thus, these results guarantee that the electrical simulation of the new devices, using the same process, will reproduce the experimental data.

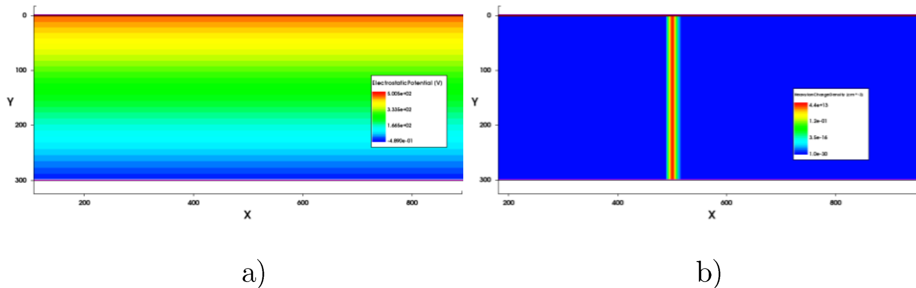
3.2.1.2. Heavy ion

Another LGAD characteristic, we are interested to define before the production, is the gain. The gain measurement in the laboratory consists in the impinging of Minimum Ionizing Particles (MIP) on the full depleted detector. When a MIP crosses the detector, it creates electron-hole pairs along its track. The pulse shape of the collected charge is recorded and analyzed afterwards. The most probable value (MPV) of the charge for all the recorded pulses is calculated. The same process is repeated with a detector without gain (p-i-n) and the most probable value (MPV) of the charge is extracted from the pulses. The gain is calculated as the ratio between LGAD MPV of the charge and p-i-n MPV of the charge.

In order to simulate the gain of an LGAD detector, first of all the structure should be over-depleted. Once the detector is over-depleted, a MIP is simulated across the detector obtaining the induced current as a function of the time. The same process

is repeated for a p-i-n detector. Afterwards, the gain is calculated as the ratio of the collected charge of an LGAD to a p-i-n. SDEVICE allows the simulation of a heavy ion penetrating the device structure, which loses energy creating a trail of electron-hole pairs along its track. The position of the impinging particle, the time when the particle penetrates the detector, the shape of the spatial distribution, the length of the track and the created charge per micrometer must be specified in the heavyion command. In all heavy ion simulations, the MIP is located at the middle of the detector with a normal incidence, crossing the whole thickness of the detector. The spatial distribution of the track is simulated as a Gaussian distribution with a standard deviation equal to 1 µm. The amount of electron-hole pairs created per micrometer depends on the thickness of the silicon. Eighty e-h pairs per micrometer are created for 300 µm thick silicon, as it is shown in data collected by Bichsel [103].

As mentioned before, the structure, electrodes and physical models must be defined in the command lines before defining the solve command. Then, the detector is reverse biased to a certain voltage with a quasistationary in the solve command. Fig. 3. 10. a) shows the equipotential lines of an LGAD reverse biased at 500V. Once the virtual device reaches the specified voltage, the transient simulation starts, simulating the MIP crossing the device at a given time (1 ns) of the transient simulation, as it can be seen in Fig. 3. 10. b).



a) b)

Fig. 3. 10. Simulation of the equipotential voltage distribution for a reverse biased LGAD at 500V a). Simulation of a MIP crossing the reverse biased device b).

The transient simulation gives the evolution of the created electron-hole pairs at a given voltage. This simulation is repeated at different voltages, in order to obtain the dependence of the gain with the voltage. The current as a function of the time and the reverse applied voltage is plotted in

Fig. 3. 11. a). The contribution of the multiplied charge at the pulse shape is clear, when the signal of an LGAD is compared to the signal of a p-i-n, which is plotted

in

Fig. 3. 11. b). Finally, the collected charge is extracted integrating the pulses from 0s to 60ns and the gain is calculated as the ration between the collected charge of an LGAD and a p-i-n. Fig. 3. 12. presents the simulation of the gain in dashed line and the measured gain in open symbols. As it can be seen in the figure, the simulation agrees with the experimental data.

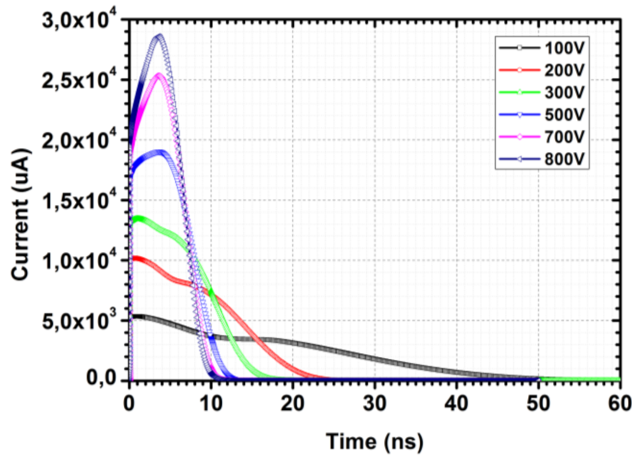


Fig. 3. 11. a) Current as a function of the time and the reverse bias for an LGAD.

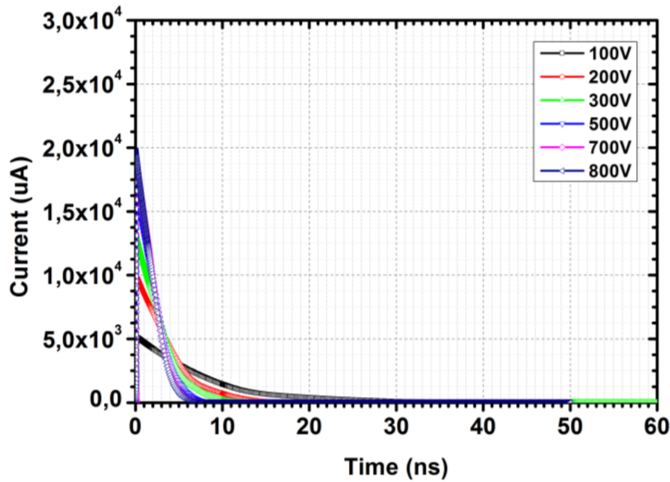


Fig. 3. 11. b) Current as a function of the time and the reverse bias for a p-i-n.

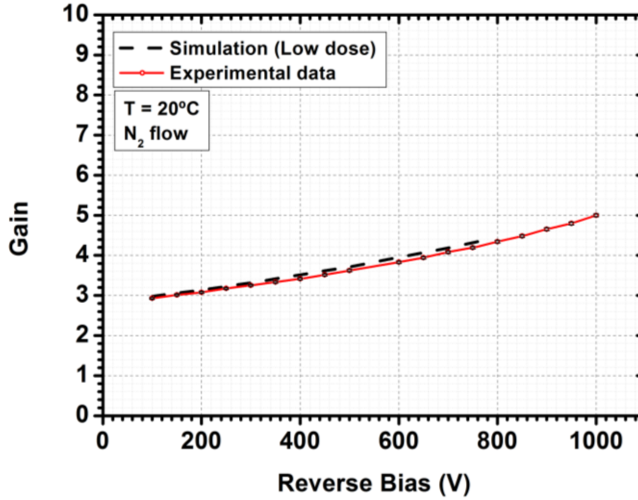


Fig. 3. 12. Gain as a function of the reverse bias of a simulated LGAD in black dashed line and measured on an LGAD in red open symbols.

3.2.1.3. Segmentation of the multiplication layer

LGAD microstrips detectors are also designed in the same mask set. Fig. 3. 13. a) presents the microstrips layout, where the guard ring surrounds the microstrips. The n^+ electrode is segmented in strips of 32 µm and 112 µm widths with a pitch of 80 µm and 160 µm, respectively. The multiplication layer is also segmented in a smaller size than microstrips area. Thus, the n^+ electrode of each microstrip overhangs its own multiplication layer, as it can be seen in the cross-section in Fig. 3. 13. b). The simulated core region has five microstrips and a p-stop between them as shown in the cross-section of the simulated core region. The electrical simulation is performed grounding the strips and ramping up the voltage of the anode (p^+ electrode) to 1000V. The simulation also takes into account the positive charges in the silicon oxide interface with a concentration in the range of 10^{11} cm^{-2}.

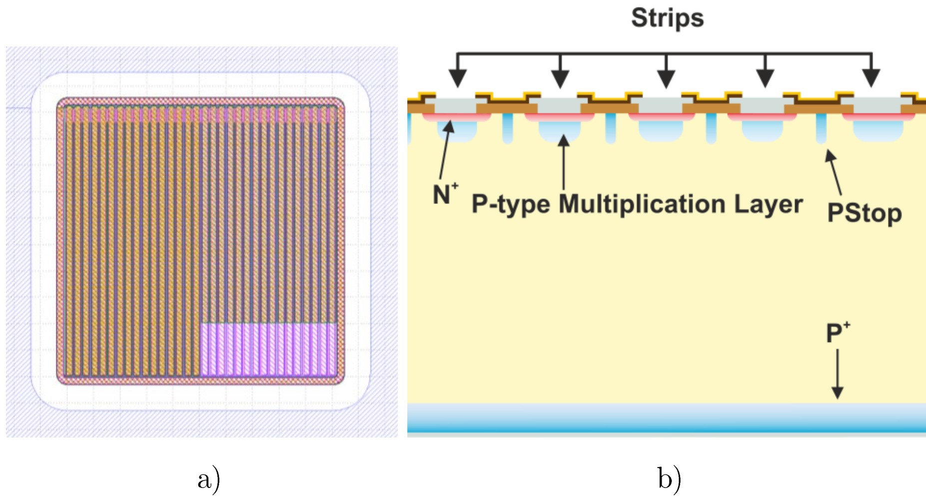
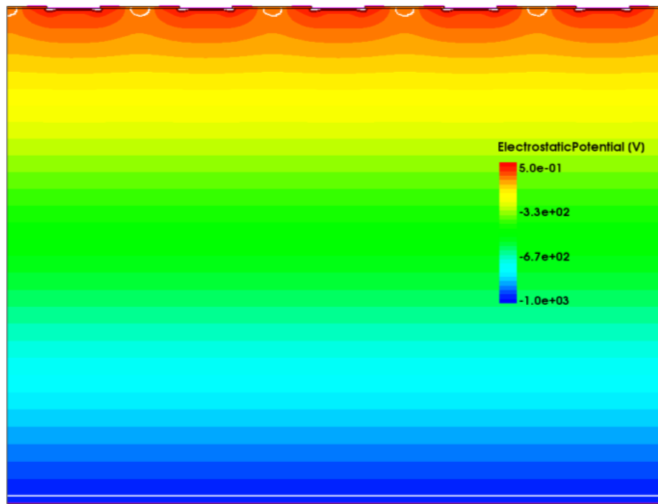


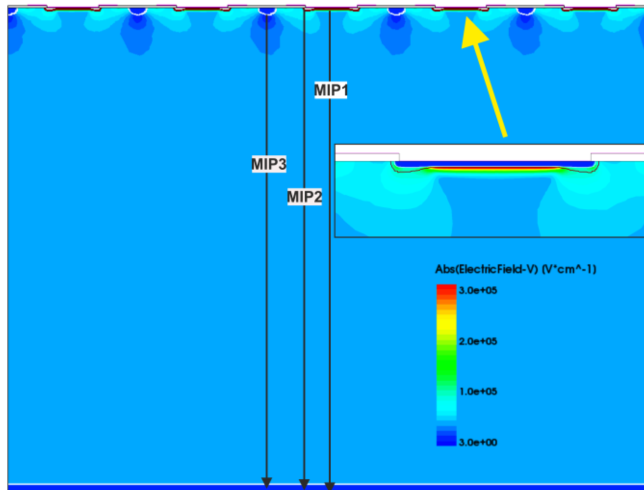
Fig. 3. 13. Microstrips LGAD layout a). Cross-section of the simulated core region of the microstrips LGAD b).

The grounded neighboring strips are close enough to each other to reduce the voltage drop between strips as it is shown in Fig. 3. 14. a), where the simulated electrostatic potential distribution at 1000 V of the core region is presented. Thus, the protection of the strip edges with a JTE is not required anymore.

Furthermore, the plot of the electric field distribution at 1000 V is also obtained from the electrical simulation. Weak points, where the device is going to break due to the high electric field, are easily detected with the plot of the electric field distribution. Fig. 3. 14. b) presents the electric field distribution of the strips at 1000V. The maximum electric field is located at the n^{+}/p junction in the middle of the strip. It can be seen that the electric field is not uniform along the detector width. Particles crossing the detector will see different electric field depending on where they pass through the device. Thus, the gain depends on the position of the particle track. Three positions with the highest difference between them are chosen to simulate the pass of a MIP through the detector. They are indicated as MIP1, MIP2 and MIP3 in Fig. 3. 14. b).



a)



b)

Fig. 3. 14. Simulation of the electrostatic potential distribution at 1000 V a). Distribution of the electric field at 1000 V b). The locations of the three simulated MIPs are also indicated on the picture.

Cutlines of the electric field in these three studied positions are done before the MIP simulation. The comparisons between electric field cutlines for both microstrips widths are presented in Fig. 3. 15. a) and b). MIP1 cutline, which is placed in the middle of the strip, has the highest electric field peak, as shown in Fig. 3. 15. in black symbols. The electric field peak at MIP2 cutline is almost three orders of magnitude lower than MIP1, while MIP3 cutline does not show any peak of the electric field. Both sizes of strips show the same distinction between

positions.

The gain also shows these dissimilarities in the position, as it can be seen in Fig. 3. 16. MIPs crossing the strip right through the edge of the strip or between strips are

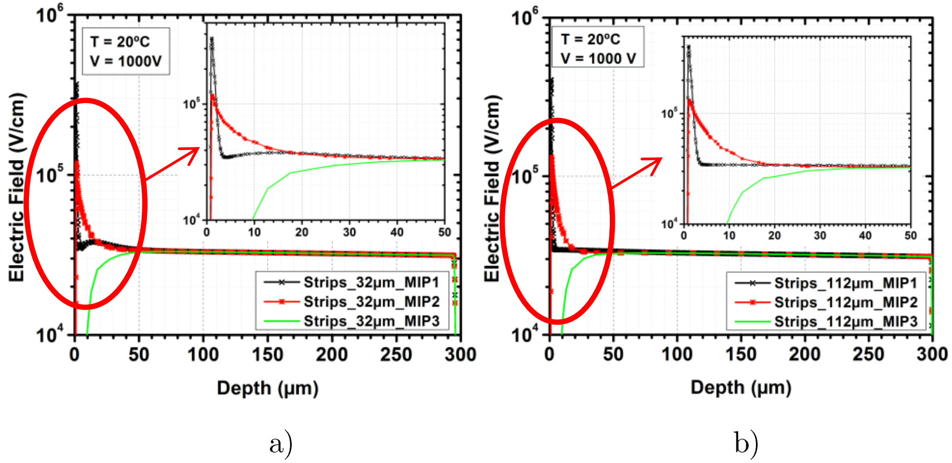


Fig. 3. 15. Cutline of the electric field distribution at 1000 V at MIP1, MIP2 and MIP3 positions for 32 μm wide strips a) and 112 μm wide strips b).

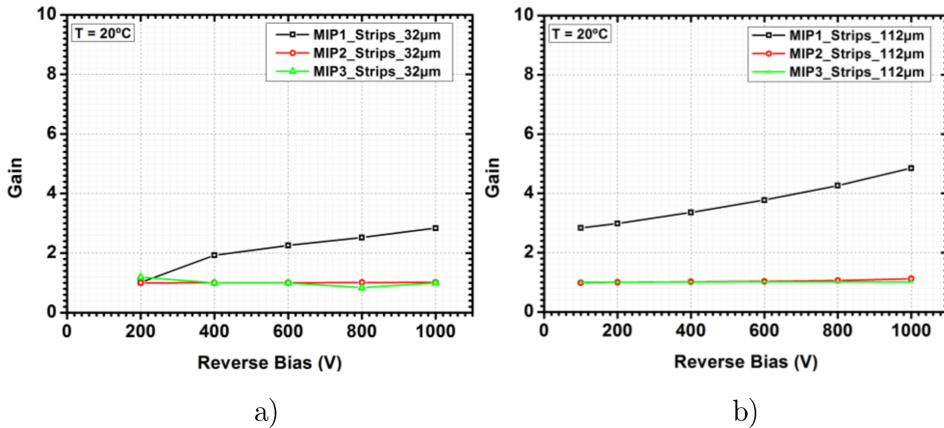


Fig. 3. 16. Plot of the gain as a function of the reverse bias and the track position for 32 μm a) and 112 μm wide microstrips LGAD b).

not multiplied. Comparing the gain between 32μm and 112μm wide strips, it looks like narrow strips have less gain than wide strips. This gain decrease could be related to the transverse diffusion of carriers. The created electrons are drifted to the multiplication region but they are also transversely diffused. The charge cloud is spread transversely with an root mean square (rms) width

$$\sigma_y = \sqrt{2\frac{kT}{e}\frac{d^2}{V_b}} \qquad \text{Eq. 3. 1}$$

which is independent of mobility, giving the same result for electrons and holes. For a 300 µm thick detector at room temperature and 1000 V the transverse diffusion is $\sigma_y \approx 2.2$ µm. Then, the total width of the electrons cloud is approximately 4.4 µm. Furthermore, the electric field lines are not straight which causes that part of the electrons does not go through the multiplication region, decreasing the number of collected charge as well as the gain. Fig. 3. 17. shows the electron density distribution in the detector after a MIP crosses the strip. Electric field lines are also plotted on the electron density distribution. Part of the electrons is deflected to the non-multiplication region for narrow strips, as it can be seen inFig. 3. 17. a). At the same time, electrons do not alter their course for wide strips and all of them go through the multiplication region, as it can be seen in Fig. 3. 17. b).

In order to solve the limitations of segmented LGAD, there is another microstrips and pixel design which does not require the segmentation of the multiplication. Thus, the gain is homogeny along the detector. This device is the inverse LGAD (i-LGAD) detector and will be presented in chapter 6.

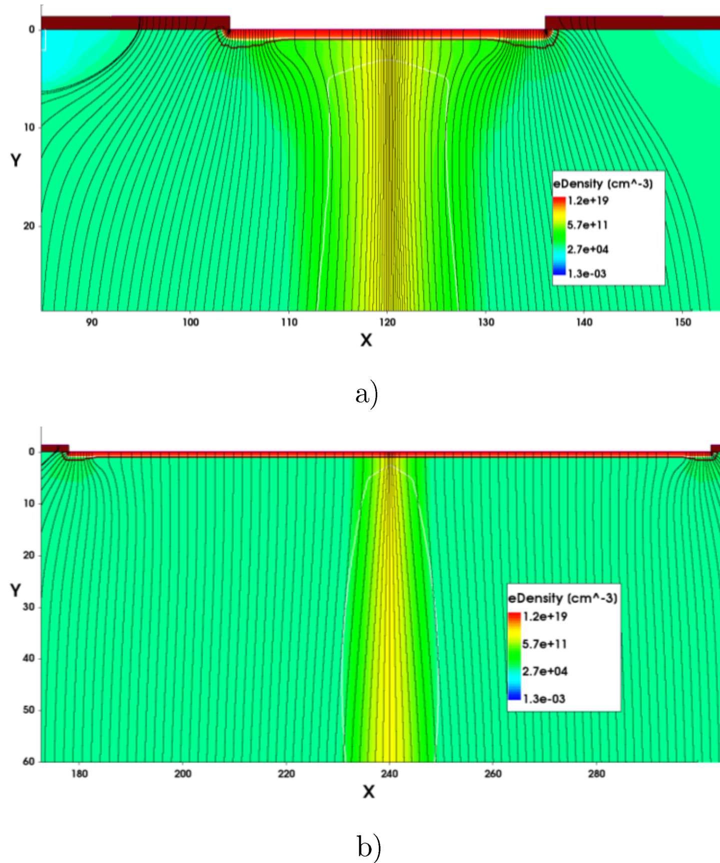


Fig. 3. 17. Electron density distribution and electric field lines for a 32 µm wide strips a) and 112 µm wide strips b).

3.2.1.4. Core and Termination region simulation

The optimum design for 285 µm thick LGAD was studied and reported before in references [58], [59]. The process and design have been settled since then. The main structures are: the JTE, the guard ring, the field plate at the n^+ electrode and the field plate at the guard ring. They will be used in the new device designs, but adapting their values to the new thickness and experiment requirements.

3.2.2. Design of new devices

Once the simulation tools are calibrated, designs of new Low Gain Avalanche Detector are simulated, in order to validate the sensor performances before the fabrication. The new devices have to fulfil with the specifications of each experiment as well as they must assure the breakdown of the device in the main

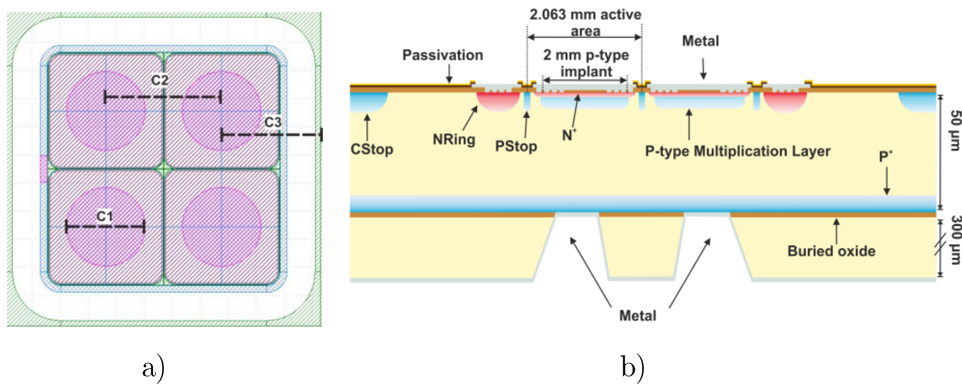
planar junction. The designed devices for the HGTD and CT-PPS experiments and the critical parameters are presented in the next sections.

After the simulation of the multiplication region to determine the maximum voltage capability of the device, the core and termination regions of new timing detectors are designed as a means to guarantee the maximum voltage capability. The behaviour of the electric field and the breakdown voltage are studied in those regions.

3.2.2.1. High Granularity Timing Detectors

The HGTD is designed to be compatible with the AltiRoc0 electronics [104]. The detector is a 2×2 pixel array with a pixel size of 2×2 mm^2. The distance between pixels must be minimized to reduce the area where the electron-hole pairs are not multiplied. Another important requirement is that the time resolution must be less than 30 ps per layer. A resolution of 30 ps was obtained by weightfield2 simulator for 50 µm thick detectors [105], [106]. Therefore, the devices are designed in 50 µm thick high resistivity p-type silicon. Fig. 3. 18. a) presents the HGTD layout. The three cross-sections of the simulated regions are indicated on the HGTD layout as C1, C2 and C3. C1 corresponds to the main multiplication region without edges. Simulating the multiplication region (C1), the maximum breakdown voltage is obtained. Once the maximum breakdown voltage is known, the core region (C2) is simulated to obtain the minimum distance between pixels. Finally, the periphery region (C3) is studied to guarantee that the breakdown happens in the main planar junction.

The cross-section of the whole HGTD device is presented in Fig. 3. 18. b). JTE is not implemented in the edge of the pixels, as it is shown in Fig. 3. 18. b).



a) b)

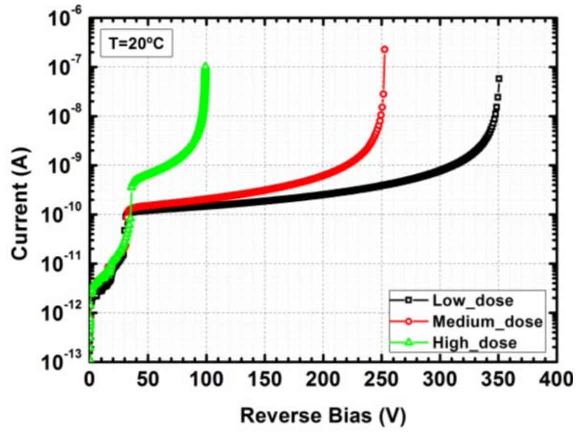
Fig. 3. 18. HGTD device layout a). The cutlines of the simulated cross-section are indicated as C1, C2 and C3 on the layout. Cross-section of a HGTD device on a silicon on insulator (SOI)wafer b).

As aforementioned in the LGAD strips simulation, when the neighbouring pixels are close enough to each other, the use of JTE is not required. The 2×2 pixel array is surrounded by the guard ring. The substrate is silicon on insulator wafer, where the device wafer is bonded to the handle wafer with a buried oxide between both wafers, as shown in Fig. 3. 18. b). The handle wafer is etched in order to contact the pre-implanted p^+ electrode. This wafer is inactive and does not play any role in the electric simulation. Therefore the handle wafer is not taken into account in the simulations.

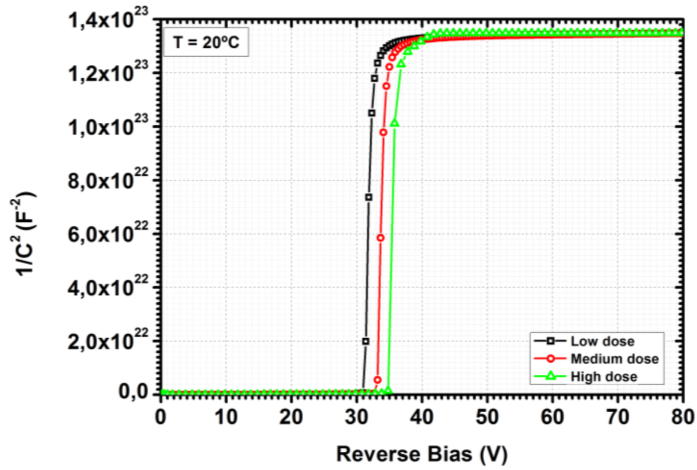
The simulation of the multiplication layer region is performed for three different implantation doses of the multiplication layer, which are labelled as low, medium and high dose. The three doses differ 10% from each other. The current as a function of the reverse bias is presented in Fig. 3. 19. a). The lowest dose shows the highest voltage capability with a breakdown voltage of 350 V. While the medium dose implant breaks at 250 V. Finally, the highest implantation dose presents the lowest voltage capability with a breakdown voltage in the range of 100 V.

The capacitance of the detector is also simulated. Fig. 3. 19. b) shows the inverse square capacitance as a function of the reverse applied voltage. As expected, the depletion voltage of the multiplication layer (V_{MD}) increases with increasing implantation dose. V_{MD} are 30 V, 33 V and 36 V for the low, medium and high dose respectively.

Finally, the gain is calculated from the transient simulation of a MIP crossing the detector. First, the collected charge in a simulated LGAD detector is extracted and divided for the collected charge in a simulated p-i-n detector. The simulated p-i-n structure is an LGAD but with the avalanche mode set off. Thus, the mesh does not change and we can assume that the variation in the collected charge it is only due to the multiplication. The gain obtained for the three implantation doses of the multiplication layer is presented in Fig. 3. 20. The gain for the highest dose is more than twice the gain for the lowest dose. Thus, 20% difference in the implant dose leads to multiply the gain value by more than two times.



a)



b)

Fig. 3. 19. Current as a function of the reverse applied voltage simulation for three implantation doses of the multiplication layer a). Inverse square capacitance vs reverse bias simulation for the three doses b).

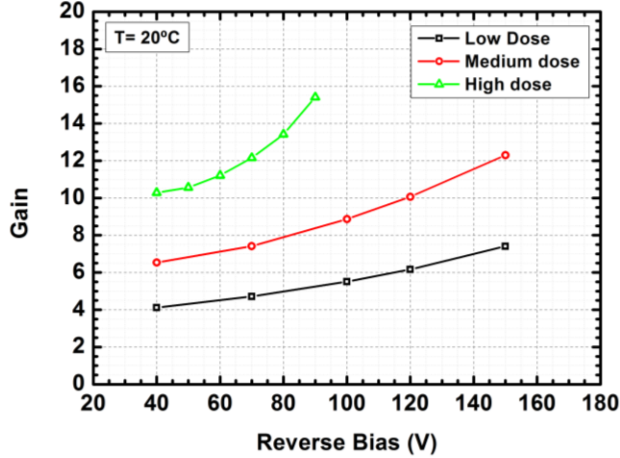


Fig. 3. 20. Gain obtained by simulation of the multiplication region of an LGAD detector for three implantation doses.

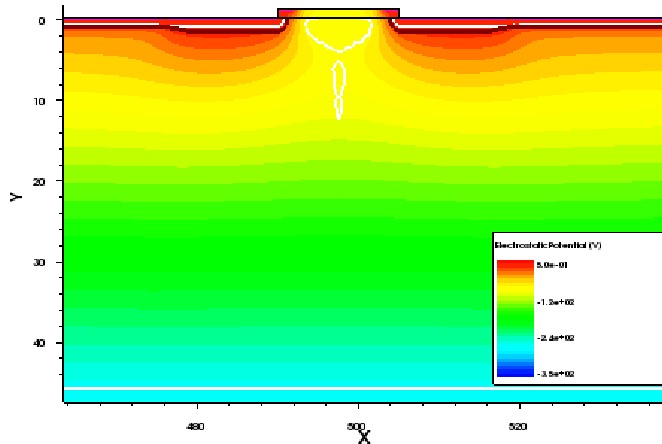
Once the maximum voltage capability of the multiplication region for each implantation dose is determined, the simulation of the core region (C2) is done varying the distance between pixels in order to study the breakdown voltage dependence with the space between pixels.

3.2.2.1.1. Distance between pixels

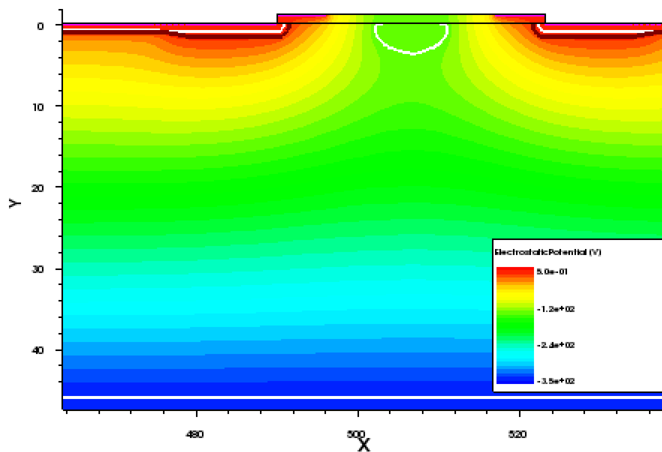
The electrical simulation is carried out grounding the n^+ electrodes and ramping up the voltage of the p^+ electrode from zero to the breakdown voltage, depending on the implantation dose of the multiplication layer. As explained in 3.2.2., a concentration of 10^{11} cm^{-2} positive charges are introduced in the silicon oxide interface.

As mentioned in the LGAD strips simulation, the use of the JTE is not required to protect the edge of the pixels, when the neighbouring pixels are close enough to each other. The voltage drop at the edge of the pixel is reduced by the biased neighbouring pixel, as it is shown in Fig. 3. 21. a) and b), where 15 µm and 33 µm distances between pixels are simulated, respectively. The voltage drop decreases as the space between pixels decreases as well. Thus, the smallest possible distance between pixels is the best option to protect the edge of the pixels.

The plots of the electric field distribution for 15 µm and 33 µm distances between pixels are plotted in Fig. 3. 22. a) and b), respectively. Both plots are taken at the corresponding breakdown voltage, 260V for 15 µm and 350V for 33 µm spaces between pixels. They show how the electric field at the edge of the pixel increases



a)



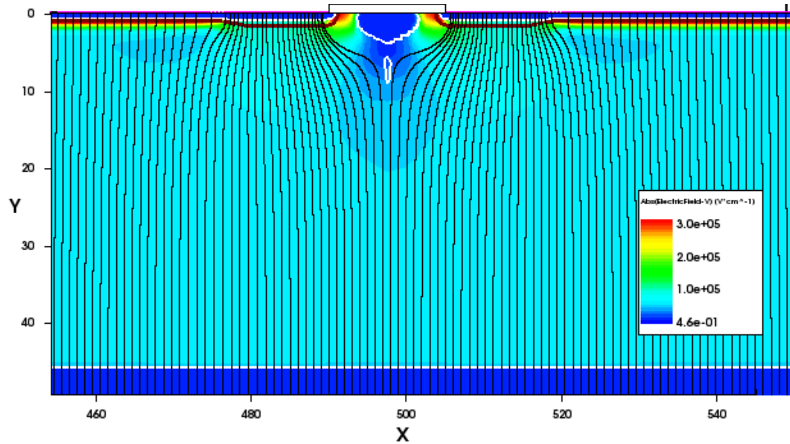
b)

Fig. 3. 21. Electrostatic potential distribution in the simulated core region of the detector for a distance between pixels of 15 µm a) and 33 µm b).

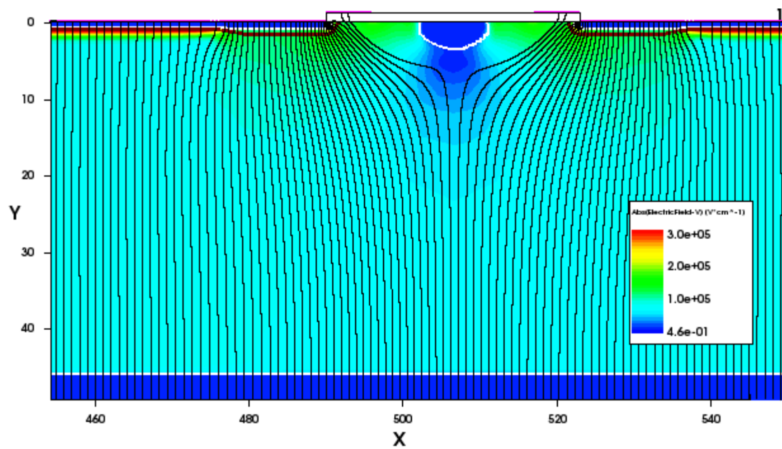
as the distance between pixels decreases. When this distance is too small, a double junction between the n^+/p-stop/n^+ is created altering the performance of the detector. As a consequence, a compromise between the shortest possible distance between pixels and enough separation to avoid breakdown at the edge of the pixels should be reached.

The plot of the current through one pixel as a function of the applied bias is presented in Fig. 3. 23. The used doping profile is the low dose implant because the detector with this dose can withstand higher voltage allowing the detector to reach enough voltage to break at the edge of the detector instead of the planar junction. As it can be seen in this figure, detectors break at 350V for all distances excluding 15 µm space between pixels. For this distance, the detector shows a premature

breakdown at 260V. The total current density distribution for 15 µm and 20 µm distances between pixels is presented in Fig. 3. 24. a) and b), respectively. As it can be seen from the comparison between the current density plots, the distance between pixels should be 20 µm or larger.



a)



b)

Fig. 3. 22. Electric field distribution of the simulated core region for a distance between pixels of 15 µm a) and 33 µm b).

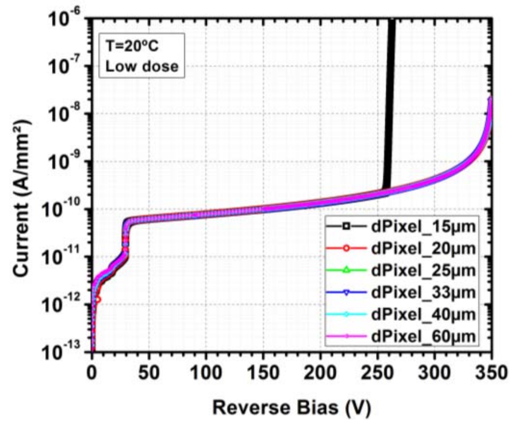
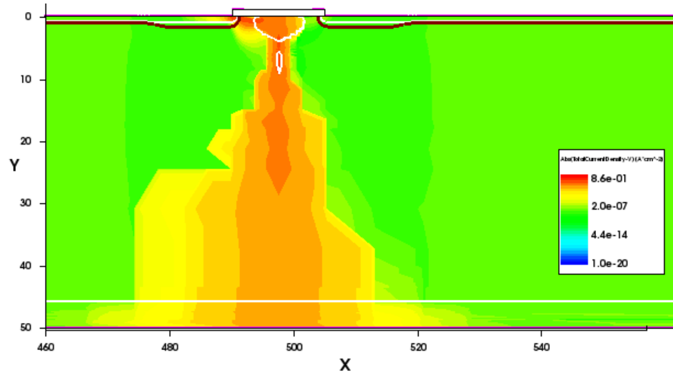
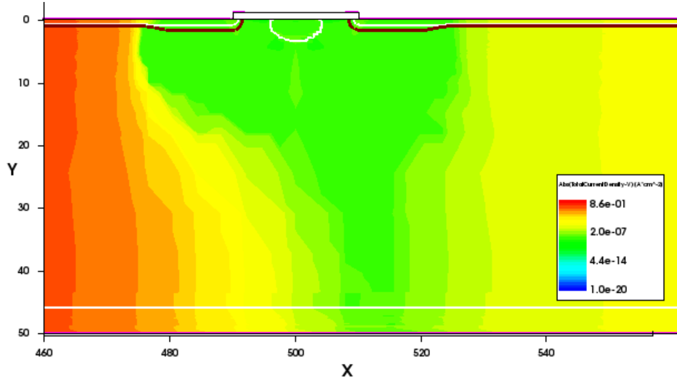


Fig. 3. 23. Plot of one pixel current as a function of the reverse applied bias and the distance between pixels. The space between pixels ranges from 15 µm to 60 µm.



a)



b)

Fig. 3. 24. Current density distribution at the breakdown voltage for a 15 µm a) and 20 µm b) between pixels.

Therefore, 20 µm separation between is the best choice to implement to the HGTD detectors. But first a study of misalignments in the photolithography step must be done to see how they affect to the detector performance.

Since 15 µm distance between pixels is not enough to avoid premature breakdown at the edge of the pixels, this distance is not taken into account in the following simulation with misalignments in the photolithography step.

The maximum misalignment in each of our photolithography step is 1.5 µm in respect of the previous level. Then, a misalignment of 1.5 µm is always introduced in the same direction at each photolithography step. That case would be the worst case scenario during the fabrication. Although the HGTD device does not have JTE implantation at the edge of the pixel, JTE is implemented in other devices on the same wafer. Thus, misalignment in the JTE level must be also taken into account in the HGTD device. After the structure with misalignments is defined, the electrical simulation is performed for distances between pixels ranging from 20 µm to 60 µm. Only the current of the pixel closer to the p-stop is plotted in Fig. 3. 25. because the breakdown is more probable on this pixel. The current of the pixel closer to the p-stop as a function of the applied voltage and the distance between pixels is plotted in Fig. 3. 25.

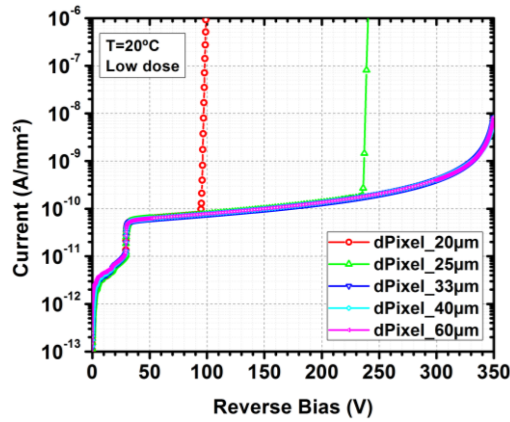
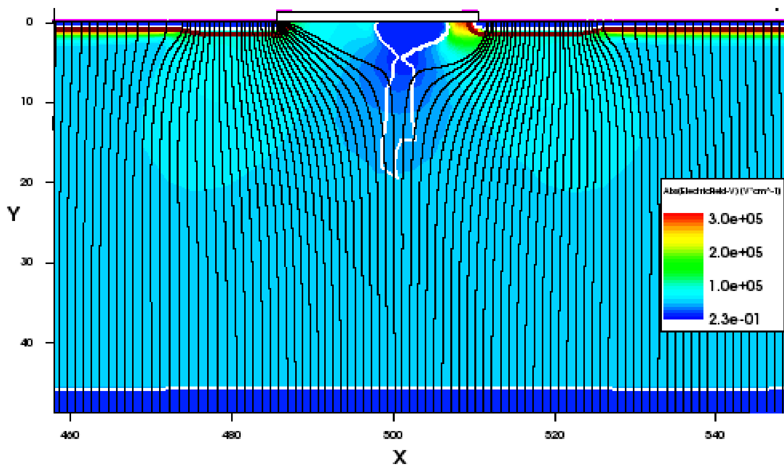


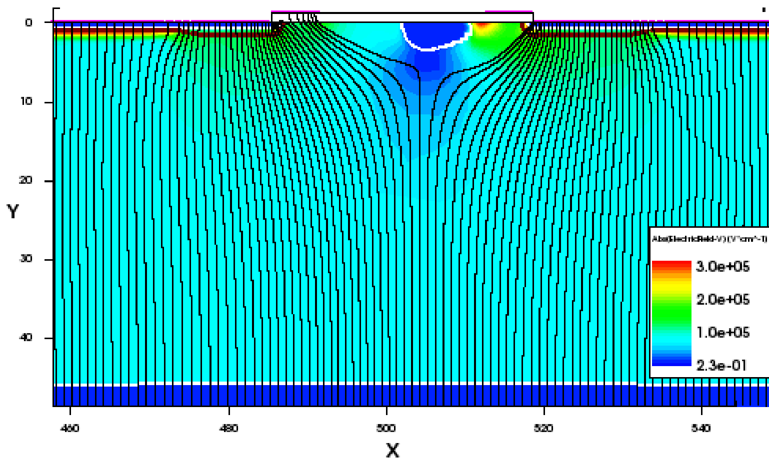
Fig. 3. 25. Plot of the current in the pixel closer to the p-stop as a function of the reverse applied bias and the distance between pixels. The separation between pixels ranges from 20 µm to 60 µm.

The detector reduces its voltage capability for distances lower than 33 µm. The comparison of the electric field distribution at the breakdown voltage for 25 µm and 33 µm case is presented in Fig. 3. 26. a) and b), respectively. Both plots are taken at the corresponding breakdown voltage, 240V and 350V for 25 µm and 33

µm, respectively.



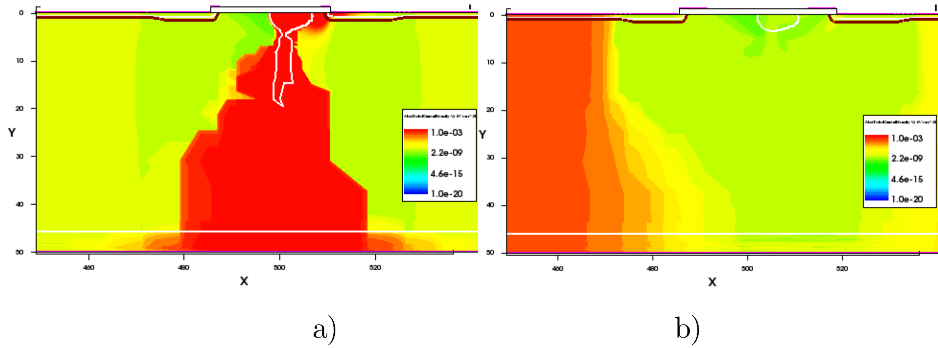
a)



b)

Fig. 3. 26. Electric field distribution of the simulated core region for a distance between pixels of 25 µm a) and 33 µm b).

Fig. 3. 27 shows the total current density at the corresponding breakdown voltage for 25 µm a) and 33 µm b) distances between pixels. It is straightforward from the comparison between plots that the detector breaks at the edge of the pixel closer to the p-stop for 25 µm separation. Thus, the minimum distance between pixels for the HGTD device is fixed to 33 µm in order to avoid premature breakdown due to misalignments during the photolithography.



a) b)

Fig. 3. 27. Current density distribution at the breakdown voltage for 25 µm a) and 33 µm b) space between pixels.

Once the separation between pixels is set to 33 µm, the gain as a function of the position where the MIP crosses the detector is simulated. As usual, the gain is calculated as the ratio of the charge collected for the HGTD sensor and the same structure without gain. The chosen positions are located between the center of the left pixel, which is at 0 µm, and the center of the right pixel, which is at 1013 µm. The representation of the structure, which is presented in

Fig. 3. 28, indicates the edge of the multiplication layer at 475 µm and 538 µm for the left and right pixels respectively, the n^+ edge at 490 µm for the left pixel and 523 µm for the right one, and the p-stop, which extends from 504 µm to 509 µm. The simulation is carried out with the medium dose doping profile and for the fixed distance between pixels of 33 µm. The gain for the left pixel and right pixel is plotted in black and red, respectively. The gain is in the range of 9.8 below the multiplication region. When MIPs get closer to the edge of the multiplication layer, in particular at 35 µm from the edge, the gain starts decreasing until it reaches a value of one at the end of multiplication layer. The gain remains at one until MIPs cross the multiplication layer edge of the right pixel. There the gain starts increasing again until the constant value of 9.8 is achieved at 35 µm from the multiplication layer edge.

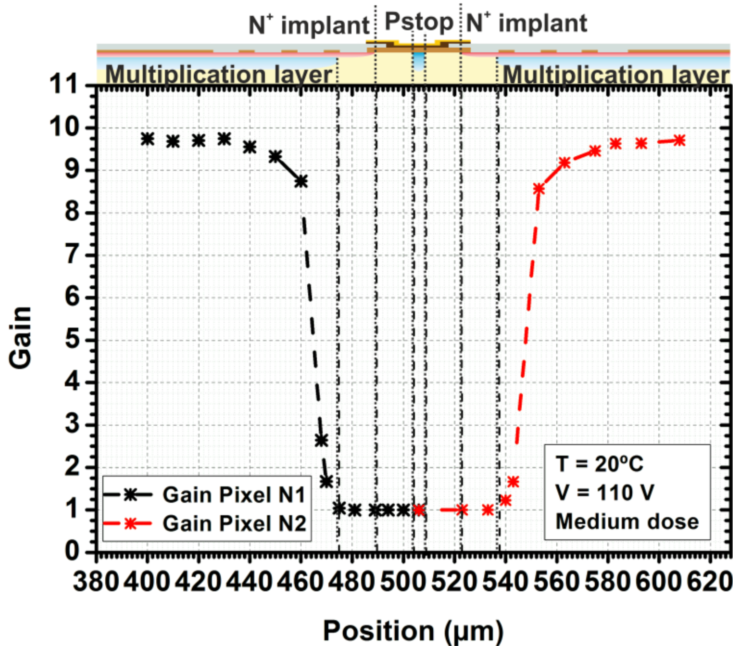


Fig. 3. 28. Gain as a function of the position where a MIP crosses the detector. The locations of the structure as the edge of the multiplication layer and the edge of the n^+ are indicated in the plot. The right and left pixels are indicated as Pixel N1 and Pixel N2 respectively.

3.2.2.1.2. Periphery design

After the study of the core region, the periphery of the device, see C3 cutline in Fig. 3. 18. a), is simulated and optimized.

The simulated distances between the pixel and the guard ring ranges from 20 µm to 60 µm. The guard ring is 120 µm wide to ease the wire bonding on it. The same termination used for 300 µm LGADs is simulated for the HGTD devices [59]. The n^+ electrodes of the pixel and the guard ring are grounded, while the p^+ electrode is ramped up from 0V to the breakdown voltage at -350V. The current as a function of the applied voltage is presented in Fig. 3. 29. The pixel breaks at 350V, although the guard ring stands more than 350V. The same fixed distance of 33 µm between pixels has been used in the periphery. However, a simulation with misalignments in the periphery must be done to guarantee that the detector does not break before the expected voltage.

The worst case scenario for misalignments during the production of detectors is simulated for distances between the pixel and the guard ring ranging from 20 µm to 60 µm. As explained in the previous section, a misalignment of 1.5 µm in each

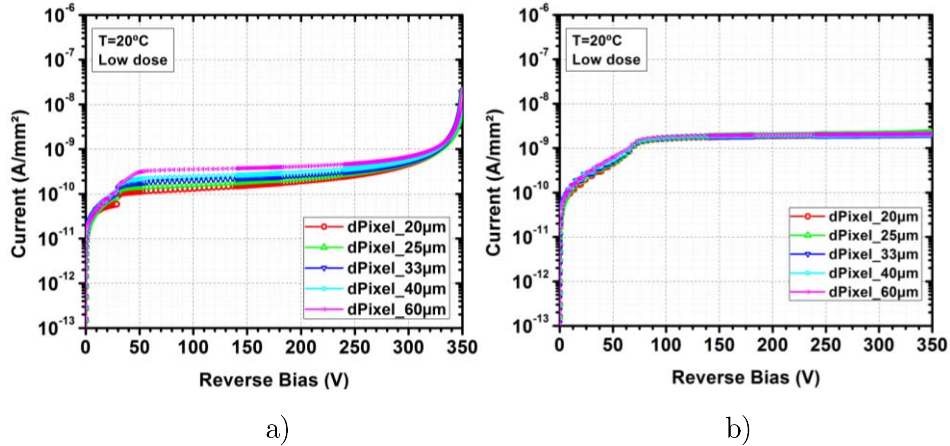


Fig. 3. 29. Current as a function of the reverse bias through the pixel a) and the guard ring b).

photolithography step is introduced in the simulation. The misalignment is always in the same direction and, as a consequence, the guard ring is closer to the p-stop, once the misalignment is applied to the simulated structure. The current through the guard ring as a function of the applied voltage and the distances between the pixel and the guard ring is shown in Fig. 3. 30. The guard ring breaks for distances below 33 µm.

The electric field distribution in the periphery for 25 µm and 33 µm separation between the pixel and the guard ring are presented in Fig. 3. 31. a) and b), respectively. Both plots are taken at the corresponding breakdown voltage. The electric field lines are also plotted on the electric field distribution. The electric field is distributed from the edge of the guard ring along the field plate reducing the electric field peak at the edge and the premature breakdown for 33 µm separation. When the distance decreases, a junction between the p-stop and the guard ring is created causing the rise of the electric field at the junction. The guard ring breaks

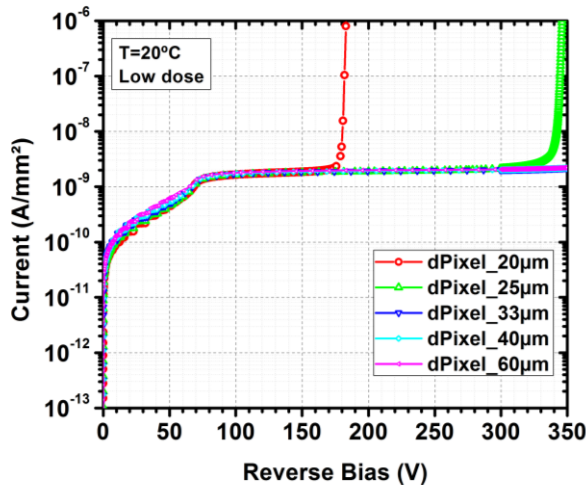


Fig. 3. 30. Current as a function of the reverse bias and the distances between the pixel and the guard ring.

before the pixel, as it can be seen in the total current density plot, which is presented in Fig. 3. 32. As it is shown in Fig. 3. 32. a), the detector breaks at the guard ring for a distance of 25 µm between the pixel and the guard ring, while it breaks at the multiplication layer for a distance of 33 µm, as it can be seen in Fig. 3. 32. b). Thus, 33 µm is also fixed as the optimum distance between the pixel and the guard ring.

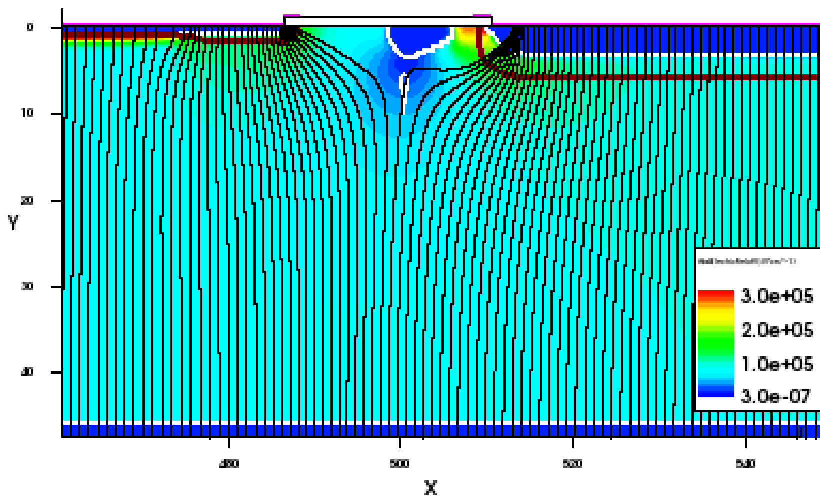


Fig. 3. 31. a) Electric field distribution of the simulated core region for a distance between pixels of 25 µm. The plot is taken at the corresponding breakdown voltage 180V.

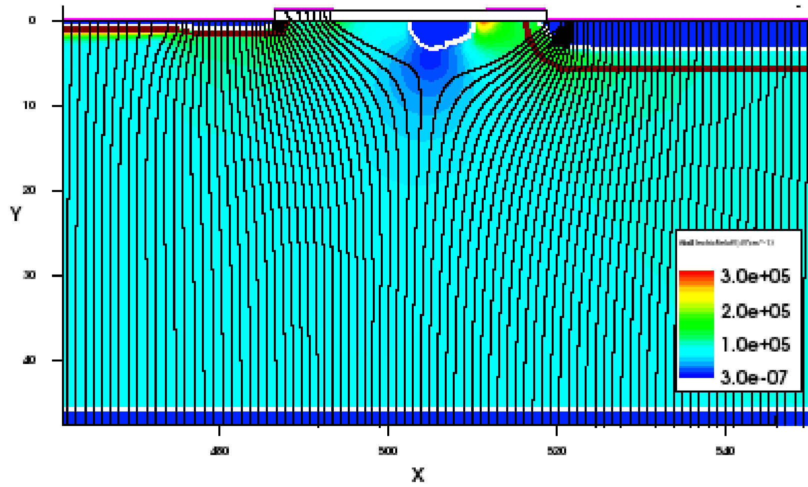
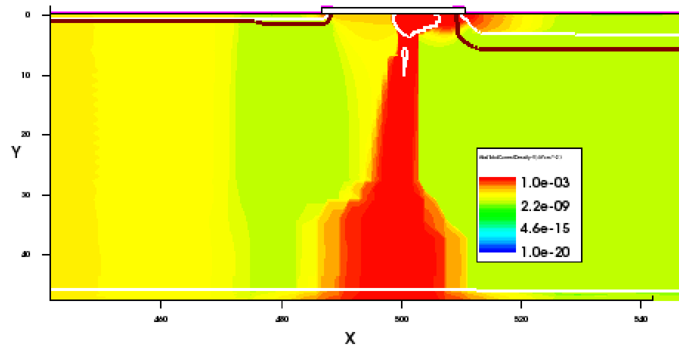
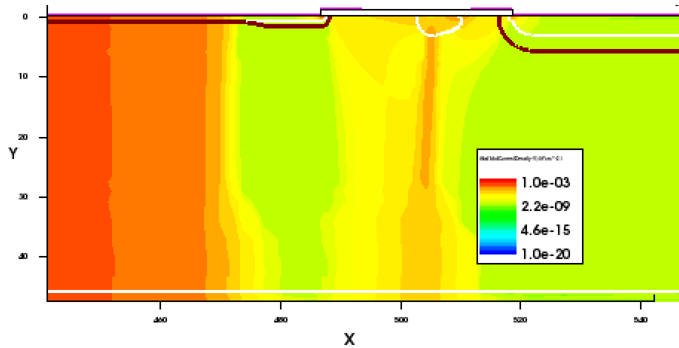


Fig. 3. 31. b) Electric field distribution of the simulated core region for a distance between pixels of 33 µm. The plot is taken at the corresponding breakdown voltage 340V.



a)



b)

Fig. 3. 32. Current density distribution at the breakdown voltage for 25 µm a) and 33 µm b) space between pixels.

3.2.2.2. CMS TOTEM Proton Position Spectrometer

CMS TOTEM Proton Position Spectrometer (CT-PPS) sensors are produced in the same batch as the HGTD. The specifications for the CT-PPS device are the following. The device layout has to be a 2×16 pixel array, which is segmented accordingly to the hit density distribution, as it is shown in Fig. 3. 33. a). Pixels closer to the beam are narrower than further pixels. The pixels should have JTE at their edge and the distance between pixels must be 50 µm or less. The minimum JTE width, which is obtained by simulation, is 10 µm, although a width of 15 µm is fixed as the minimum value to secure its proper technological definition and implementation in the structure. Another important requirement is the reduction of the separation between the nearest pixel to the beam and the detector edge. This distance should be as small as possible but enough to guarantee that the depletion region does not reach the damaged edge of the detector. The final layout of the detector is presented in Fig. 3. 33. b), where the distance between the pixel and the detector edge is reduced to 200 µm. Fig. 3. 34 presents the cross-section of the CT-PPS, where the pixels have a JTE at their edge. The representation is not to scale.

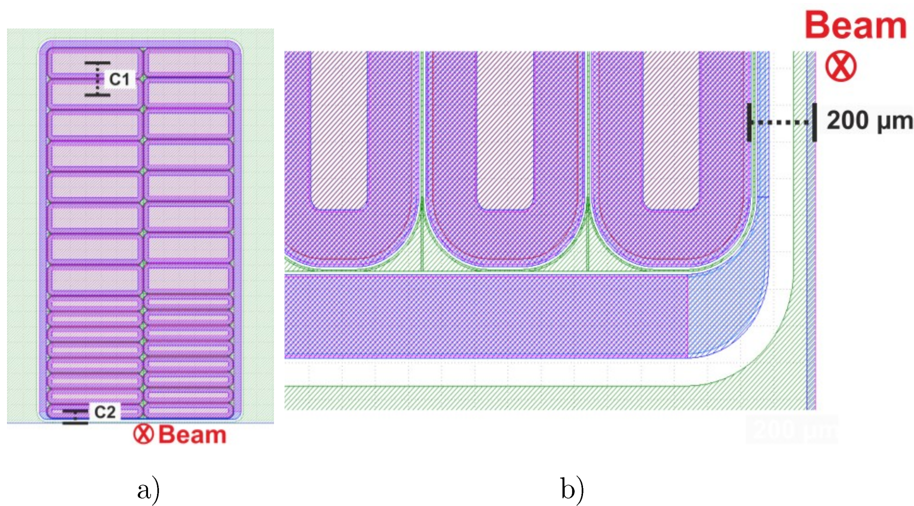


Fig. 3. 33. CT-PPS device layout where the cutlines of the simulated cross-sections are indicated a). Zoom of the mask layout at the edge closer to the beam where the distance between the last pixel and the detector edge is reduced to 200 µm b).

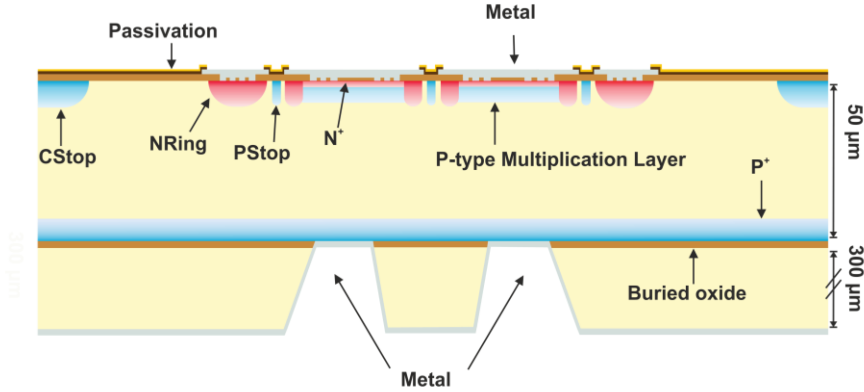


Fig. 3. 34. Cross-section of the CT-PPS sensor produced on a SOI wafer.

As the CT-PPS and HGTD devices will be implemented in the same wafer, the maximum voltage capability and gain for the three doses are those same presented ones in Fig. 3. 19. a) and Fig. 3. 20. respectively. The study of the core and periphery designs is performed with the lowest implantation dose of the multiplication layer because the device reaches higher before its breakdown. Then, the breakdown voltages of low dose devices have a higher probability to depend on the distances between pixels.

3.2.2.2.1. Distance between pixels

The main design parameter for the core region of the CT-PPS devices is the distance between pixels. This distance is required to be shorter than 50 µm. The cutline of the simulated core region is indicated as C1 in Fig. 3. 33. a). The cross-section extends from the center of the first pixel to the center of the neighboring pixel. The JTE width is fixed to 15 µm. The two pixels are grounded, at the same time the anode is ramped down from 0 to the breakdown voltage at -350V. Distances between pixels ranges from 15 µm to 60 µm. A concentration of 10^{11} cm^{-2} positive charges is introduced in the silicon oxide interface. Fig. 3. 35. shows the left pixel current as a function of the reverse bias and the distance between pixels. Only the current of the left pixel is presented because both pixels give the same I-V curve. The voltage capability of the pixel is the same for all distances between pixels. In contrast, HGTD device breaks at 260V for pixel separation shorter than 20 µm. Thus, the JTE protects the p-stop/n^+ junction by increasing its curvature radius.

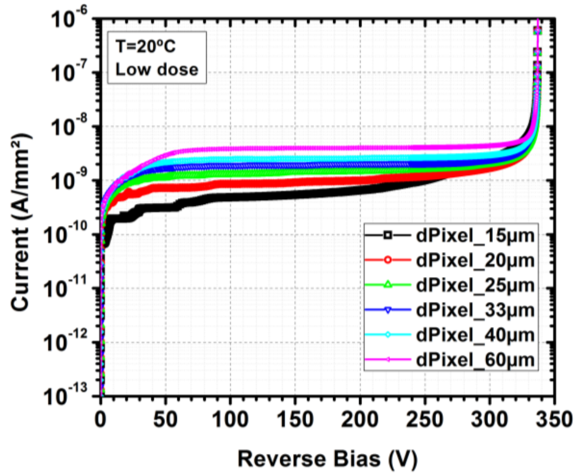


Fig. 3. 35. Current as a function of the reverses applied voltage and the distance between pixels.

The comparison of the current density distribution for a distance of 15 µm and 33 µm is presented in Fig. 3. 36. a) and b), respectively. Although the device breaks in the multiplication layer junction in both cases, the p-stop/JTE junction is near the breakdown for 15 µm pixel separation. Another interesting comparison is the electric field distribution for a distance of 15 and 33 µm, plotted in Fig. 3. 37. a) and b), respectively. As expected, the electric field at the p-stop/JTE junction increases with decreasing pixel separation. The JTE causes a higher bending of the electric field lines compared to the HGTD devices. Then, the space between pixels where the gain is not uniform is expected to be longer than the HGTD.

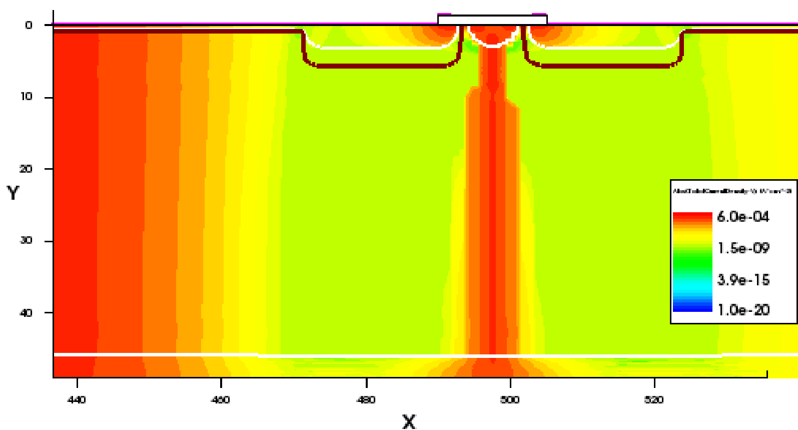


Fig. 3. 36. a) Current density distribution at the breakdown voltage, 337V, for 15 µm between pixels.

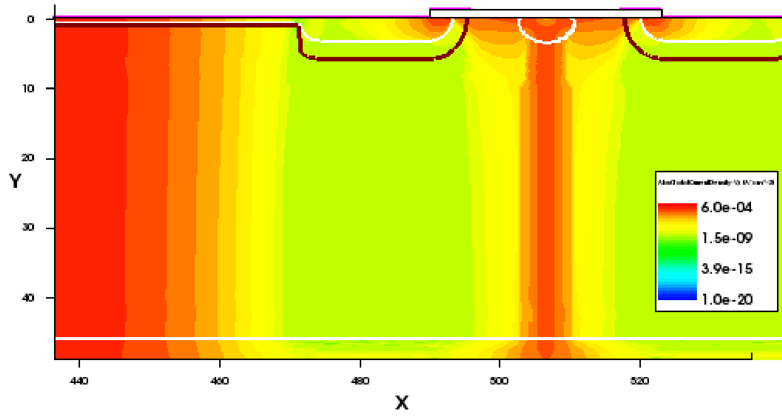


Fig. 3. 36. b) Current density distribution at the breakdown voltage, 337 V, for 33 microns between pixels.

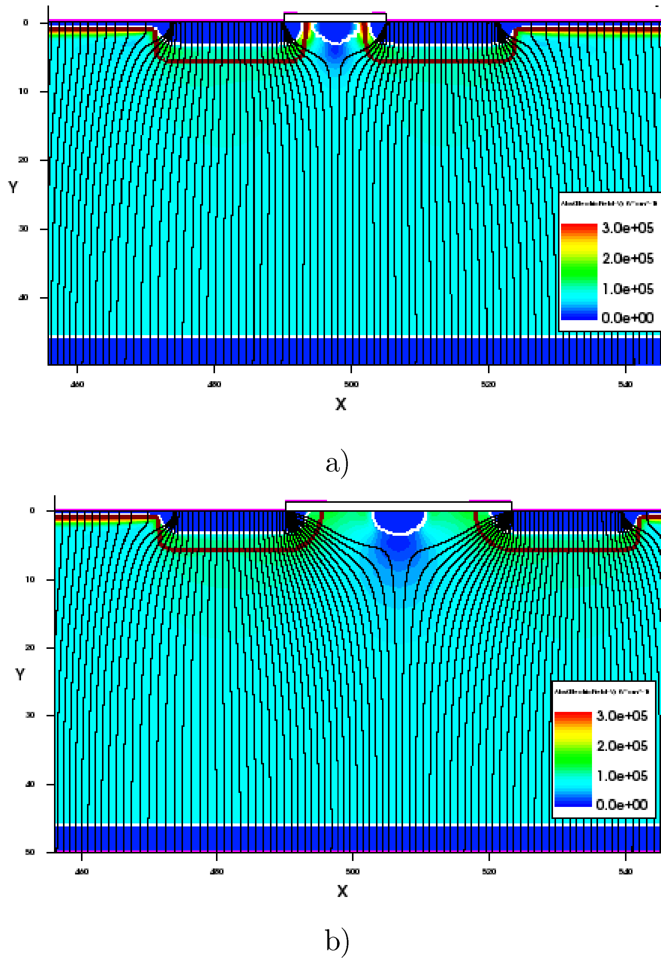


Fig. 3. 37. Electric field distribution of the simulated core region for a distance between pixels of 15 µm a) and 33 µm b).

As already stated, an important issue during the fabrication process is the misalignments in photolithography steps. The misalignments could be of 1.5 µm at each mask level. The simulation of the misalignment is performed in the same direction with the maximum misalignment at each photolithography step. As a consequence, the left pixel gets closer to the p-stop meanwhile the right pixel moves away from the p-stop. The current of the pixel closer to the p-stop as a function of the reverse bias and the separation between pixels is presented in Fig. 3. 38. The space between pixels ranges from 15 µm to 60 µm. As expected, the voltage capability of the detector decreases with the distance between pixels. The right pixel breaks early for distances shorter than 25 µm, as it is shown in the aforementioned plot. Comparing these I-V curves with those obtained for the HGTD sensor, which are plotted in Fig. 3. 25, it is clear that the JTE protects the pixels from misalignments during photolithography steps.

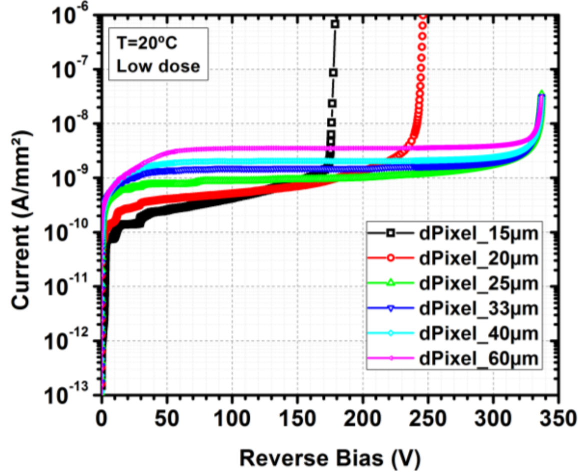
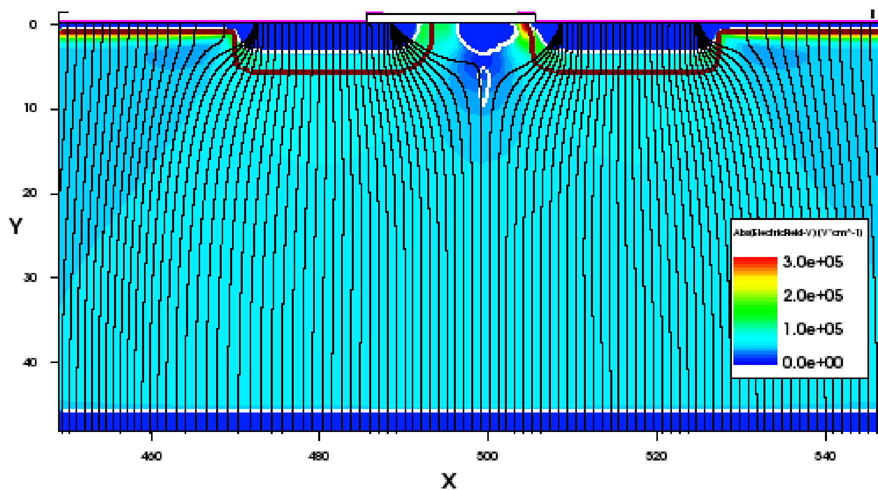
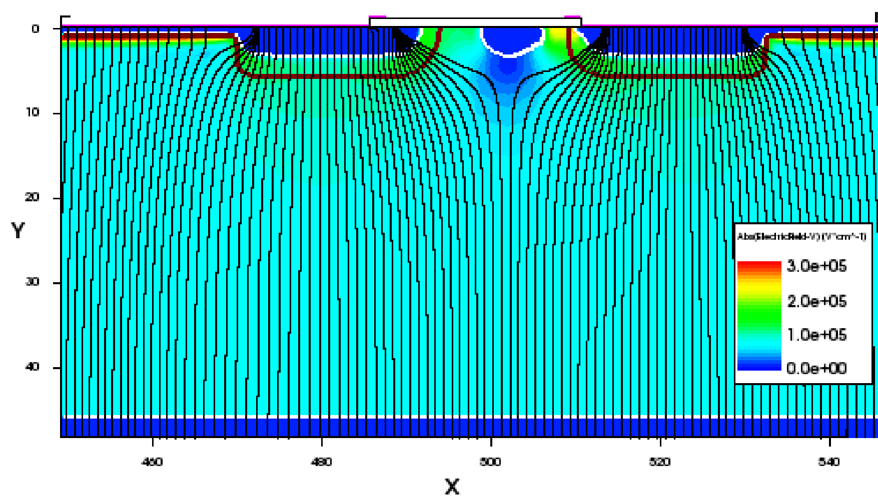


Fig. 3. 38. The plot of the current through the pixel closer to the p-stop as a function of the reverse applied bias and the distance between pixels. The separation between pixels ranges from 15 µm to 60 µm.

The comparison of the electric field distributions for a separation of 20 µm and 25 µm between pixels, which are presented in Fig. 3. 39. a) and b) respectively, clearly shows the increase of the electric field as the space between pixels decreases. Each plot is extracted at their own breakdown voltage: 240 V for 20 µm and 337 V for 25 µm between pixels. The comparison shows how the detector breaks at the edge of the pixel closer to the p-stop, where a junction between the p-stop and the n^+ electrode is formed. The plot of the corresponding current density distributions are presented in Fig. 3. 40. a) and b), respectively. The current density plot verifies that the detector breaks at the edge of the pixel closer to the p-stop for a separation of 20 µm between pixels, while it breaks at the main planar junction for a distance of 25 µm. Thus, the distance between pixels can be reduced to 25 µm instead of 33 µm, when the JTE is used at the edge of the pixels. Although a 25 µm separation between pixels is the optimum distance, 33 µm distance is chosen in order to compare the CT-PPS with the HGTD devices. Therefore, any difference in the produced devices will be related to the JTE.



a)



b)

Fig. 3. 39. Electric field distribution of the simulated core region for a distance between pixels of 20 µm a) and 25 µm b).

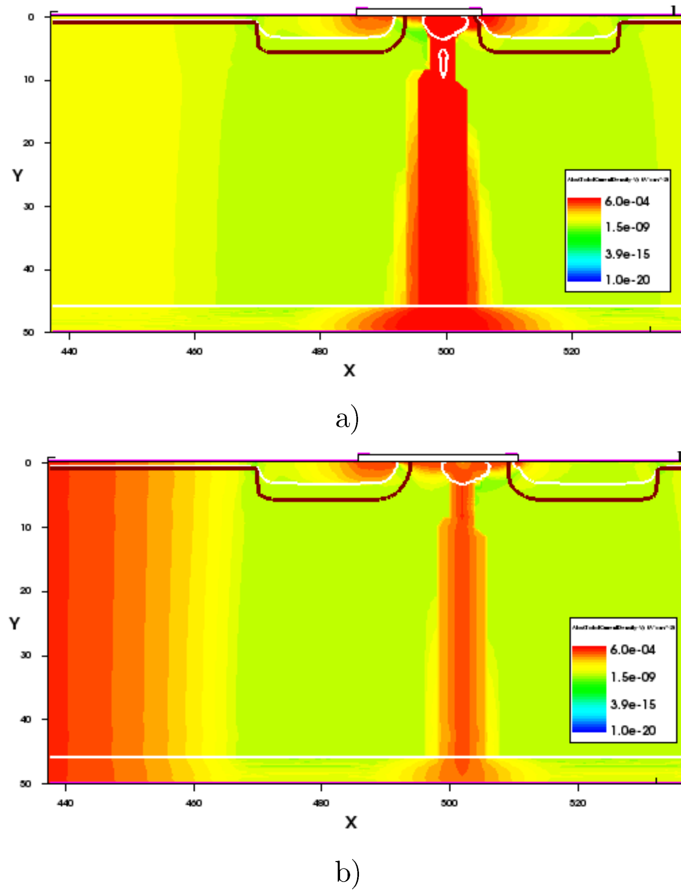


Fig. 3. 40. Current density distribution at the breakdown voltage for 20 µm a) and 25 µm b) space between pixels.

Once the distance between pixels for the CT-PPS device is set to 33 µm, the study of the gain as a function of the position where the MIP crosses the detector is carried out calculating the gain as the ratio of the charge collected for the CT-PPS device to the charge collected for the same structure without gain. The simulation is performed in different positions between the centers of the two pixels. The center of the left pixel is at 0 µm, while the center of the right pixel is at 1013 µm. Fig. 3. 41. shows the structure of the simulated device, where the JTE, the multiplication layer, n^+ and p-stop edges are indicated. The gain for the left pixel and right pixel are plotted in black and red lines, respectively. The gain is in the range of 9.8 almost below the entire multiplication layer. Although the multiplication layer extends beyond 440 µm, the gain starts decreasing until it reaches no gain at 7 µm to the edge of the multiplication layer. The gain remains equal to one until 544 µm, which is 5 µm from the edge of the multiplication layer of the right pixel. Afterwards, the gain starts increasing until it approximately gets its maximum

value at 40 µm beyond the multiplication layer edge.

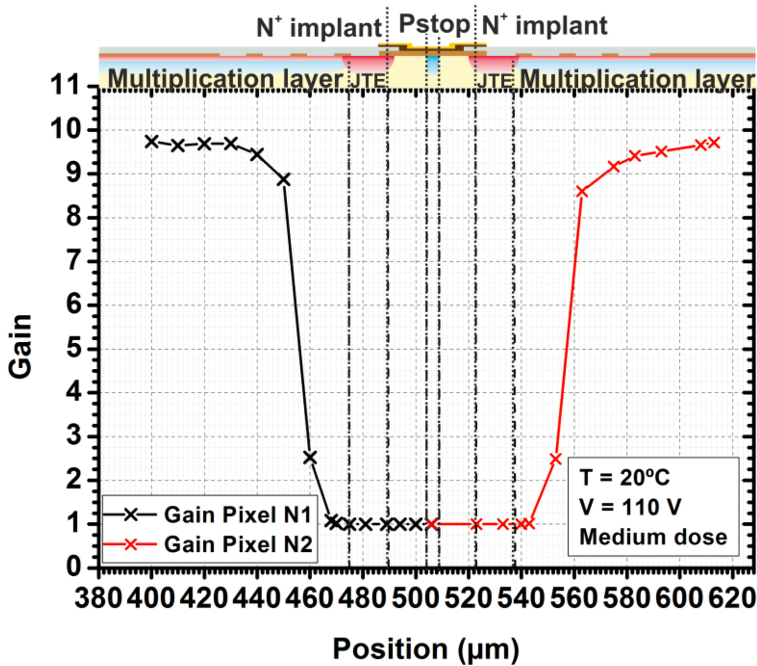


Fig. 3. 41. Gain as a function of the position where a MIP crosses the detector. Locations of the structure such as the edge of the multiplication layer and the edge of the n^+ are indicated in the plot.

It is interesting to compare the gain distribution for both devices in order to visualize the difference in the gain uniformity. The comparison between both designed devices, which are simulated with the same separation between pixels, is plotted in Fig. 3. 42. The HGTD and CT-PPS gain distributions are plotted in dashed and solid lines, respectively. Fixing the acceptable gain to 9, a distance of non-uniform gain of 104 µm is found for the HGTD device, while a distance 124 µm is obtain for the CT-PPS device. Thus, the non-uniform gain region is larger for the CT-PPS than the HGTD device due to the fact that the JTE causes the further bending of the electric field lines.

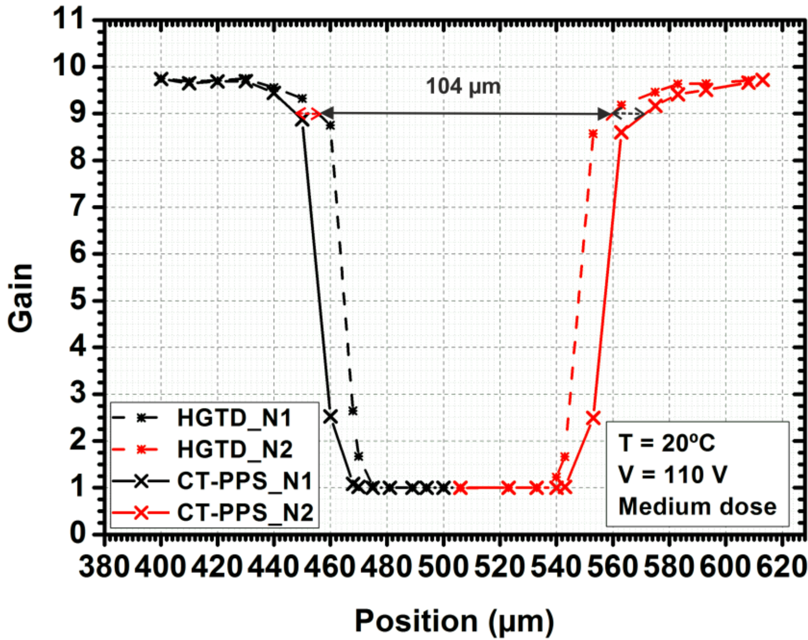


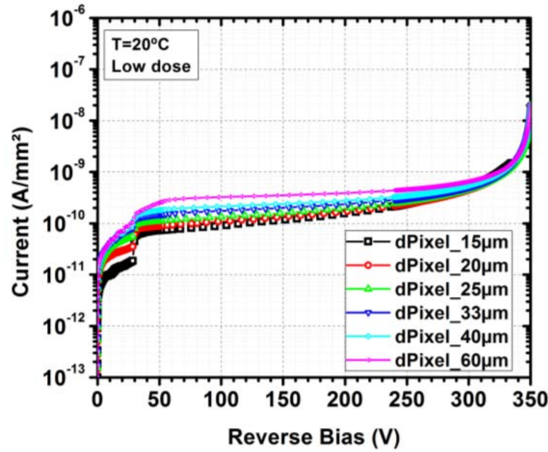
Fig. 3. 42. Gain as a function of the position where a MIP crosses the detector. The gain values in the left pixel are plotted in black, while they are plotted in red for the right pixel. HGTD and CT-PPS are plotted in dashed and solid lines, respectively.

3.2.2.2.2. Periphery design for the CT-PPS device

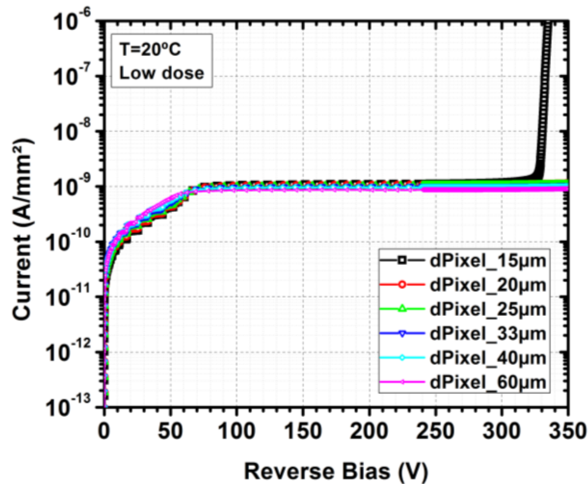
The periphery design must fulfil the minimization of the periphery region near the beam, as shown in Fig. 3. 33. b). The width of the guard ring in this region is reduced to 15 µm to accomplish with the minimization, while its width remains the same (120 µm) in the rest of edges. The parameters, which are optimized by simulation, are the distance between the pixel edge and the guard ring, which is called as dPixel, the distance between the pixel edge and the detector edge and the length of the channel stop at the edge of the detector. First, distances between the pixel and the guard ring are studied simulating the usual termination dimensions. In other words, the distance to the edge and the channel stop length used for the 300 µm thick LGAD detector are used in the simulation to optimize the dPixel value. Thus, the termination is long enough to guarantee that the breakdown only depends on the distance between the guard ring and the pixel edge. Once this separation is obtained, the minimization of the termination is done using the optimum dPixel value.

The simulation of the periphery is carried out grounding the n^+ electrode and the guard ring, ramping down the voltage of the p^+ electrode from zero to the

breakdown voltage at -340 V. A concentration of 10^{11} cm^{-2} positive charges is introduced in the silicon oxide interface. Simulated distances between the pixel and the guard ring range from 15 µm to 60 µm. The current at the pixel and the guard ring as a function of the applied voltage are presented in Fig. 3. 43. a) and b), respectively. The pixel breaks at 350V, while the guard ring stands the 350V for all dPixel values, except for 15 µm, which breaks at 330V, as it can be seen in Fig. 3. 43. b). Therefore a separation of 33 µm between the pixel and the guard ring is a feasible distance. Although the separation can be less than 33 µm, a simulation with misalignments in the periphery must be done to verify that it is enough to avoid premature breakdown.



a)



b)

Fig. 3. 43. Current as a function of the reverse bias through the pixel a) and the guard ring b).

As usual, the worst case scenario for misalignments during the production of devices is taken into account in the simulated periphery. The simulated dPixels range from 15 to 60 µm. A misalignment of 1.5 µm in each photolithography step is introduced in the device simulation and the misalignment is always in the same direction. Therefore, the guard ring gets closer to the p-stop, while the pixel moves away from the p-stop. The current through the guard ring as a function of the applied voltage and dPixel values is shown in Fig. 3. 44. The guard ring breaks for distances below 25 µm, as it can be seen in the aforementioned plot. Electric field

distributions for 20 µm and 25 µm separation are plotted in Fig. 3. 45. a) and b), respectively. Comparing both plots, an electric field increase at the edge of the guard ring is observed, when the dPixel decreases.

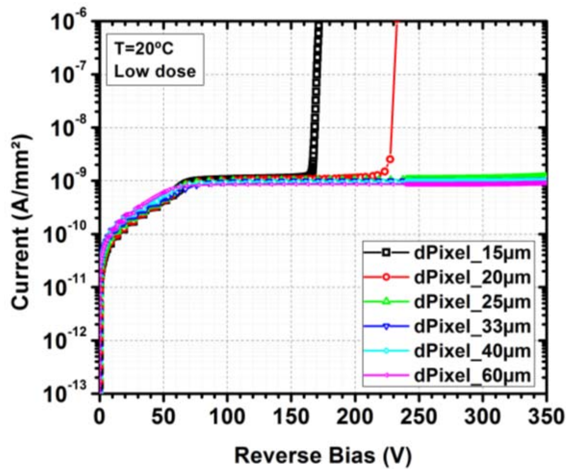


Fig. 3. 44. Current as a function of the reverse bias and the distances between the pixel and the guard ring.

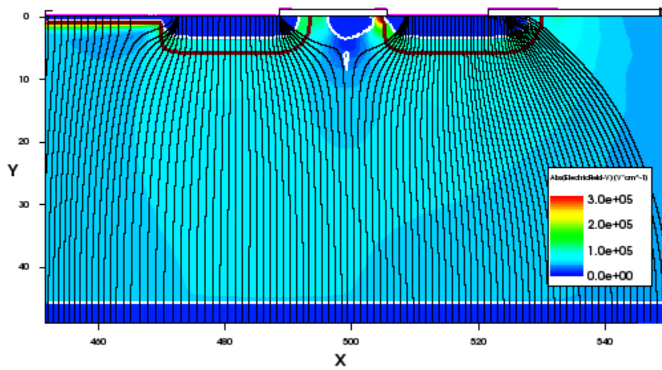


Fig. 3. 45. a) Electric field distribution of the simulated core region for a distance between pixels of 20 µm. The electric field distribution is plotted at the breakdown voltage of the device (230 V).

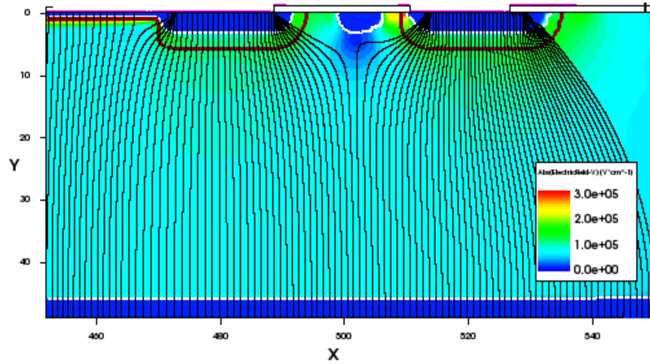


Fig. 3. 45. b) Electric field distribution of the simulated core region for a distance between pixels of 25 µm. The electric field distribution is plotted at the breakdown voltage of the device (350 V).

The representation of the current density for a distance of 20 µm and 25 µm between the pixel and the guard ring is presented in Fig. 3. 46. a) and b), respectively. This comparison clearly points out how the detector breaks at the edge of the guard ring for 20 µm separation, while it breaks at the main planar junction of the pixel for 25 µm. Thus, a distance of 25 µm is the minimum feasible distance.

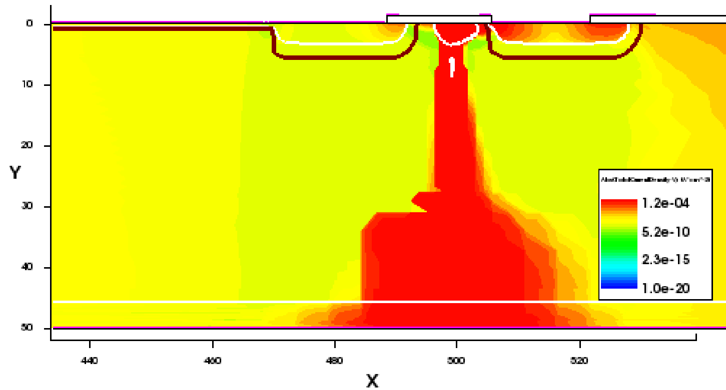


Fig. 3. 46. a) Current density distribution at the breakdown voltage for 25 µm space between pixels.

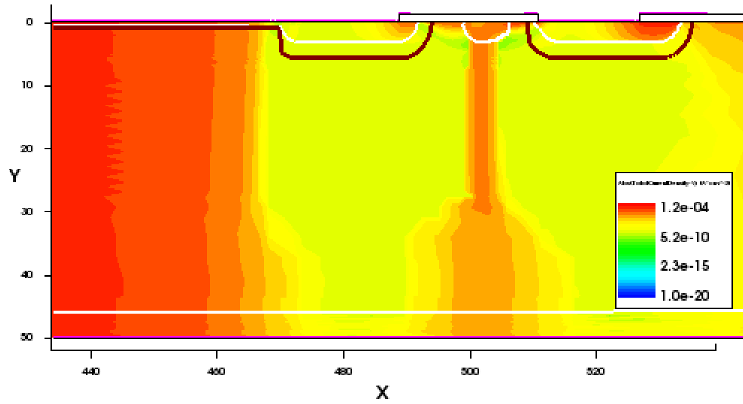
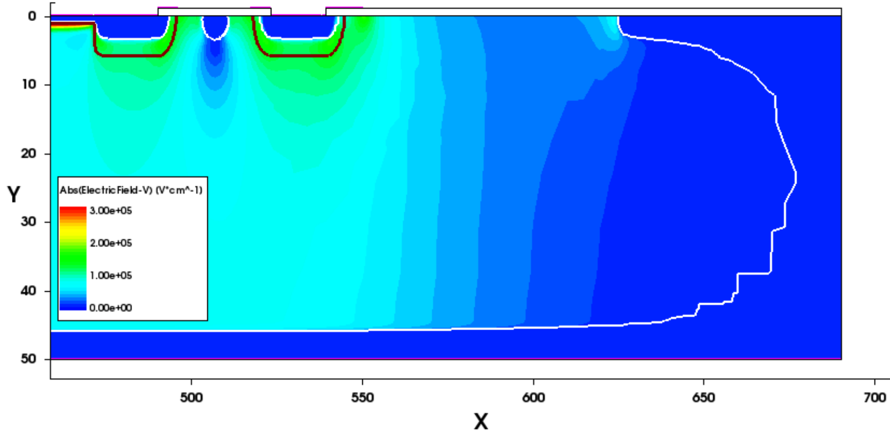


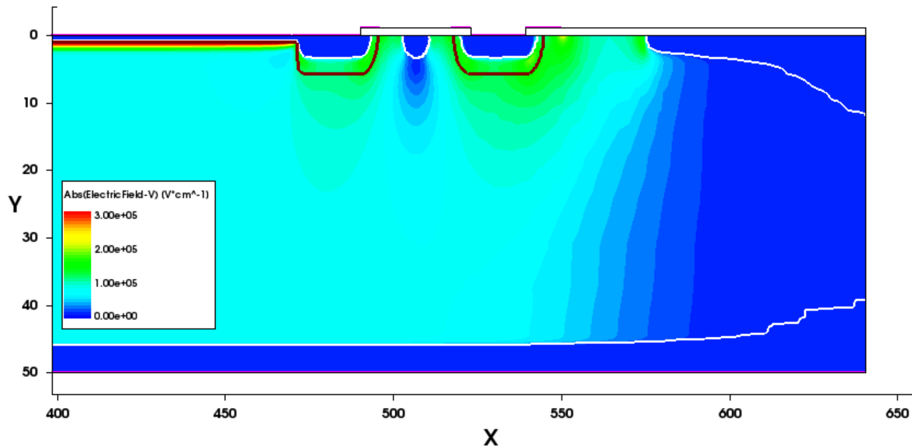
Fig. 3. 46. b) Current density distribution at the breakdown voltage for 33 µm space between pixels.

As previously seen in the core region simulation, the JTE improves the voltage capability of the detector when misalignments are taken into account in the simulation. Although it has been found by simulation that a distance of 25 µm is the best choice for the CT-PPS sensors, a distance of 33 µm has been chosen to make possible the comparison between devices with JTE and devices without JTE.

Once the distance dPixel is fixed to 33 µm, the study of distance from the pixel to the edge is performed to guarantee that the space charge region does not reach the edge of the detector. The simulation is done for 200 µm and 150 µm separation between the pixel and the edge, simulating a 15 µm wide guard ring. The electric field distributions for both distances are presented in Fig. 3. 47. a) and b), respectively. The space charge region is indicated by white lines. The space charge region does not reach the edge of the detector for 200 µm separation, but 150 µm are not enough to prevent that the space charge region reaches the damaged edge of the detector, as it can be seen in Fig. 3. 47. a) and b). Thus, the minimum distance between the pixel and the detector edge is set to 200 µm at the edge closer to the beam.



a)



b)

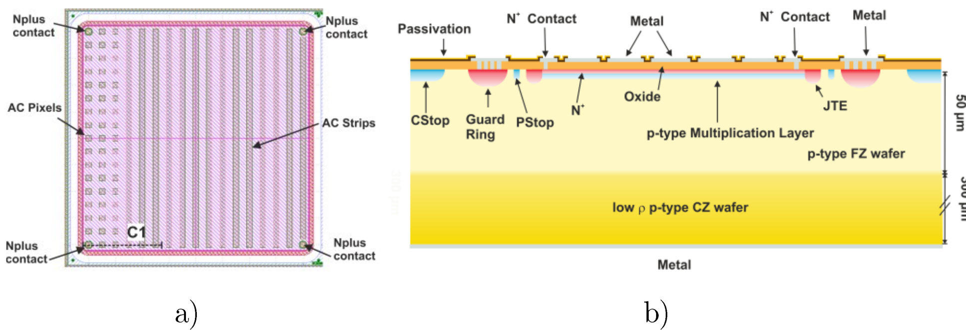
Fig. 3. 47. Distribution of the electric field, where the space charge region is indicated by white lines, for 200 µm a) and 150 µm b) distance between the pixel and the detector edge. Both distributions are plotted at the breakdown voltage, 350 V.

3.2.2.3. AC-LGAD

Capacitive coupled LGAD detectors (AC-LGAD) were also introduced in the same batch as a proof-of-concept device. The idea consists in the use of the thermally grown oxide as a capacitive coupling of the strips or pixels to the n^+ layer [107]. When the generated e-h pairs start moving in the depleted detector, they induce a current in the AC coupled strips or pixels. This kind of coupling is well known and

extensively used in noisy environments to prevent the leakage current from entering the preamplifier [108], [109]. The main difference between AC-LGAD and the standard AC coupled strips/pixels is that the n^+ electrode and the multiplication layer are not segmented. The n^+ electrode is contacted in the edges of the n^+ implant, as it is shown in Fig. 3. 48. a). As it can be seen in the AC-LGAD layout, pixels and strips are implemented in the same pad of the last device. A schematic cross-section of the detector is presented in Fig. 3. 48. b), where it can be seen the capacitive coupling of the strips.

The simulation of the AC-LGAD is studied in this section to find the optimum strip width and oxide thickness of the detector. Fig. 3. 49. shows the diagram of the read out circuit, which is simulated using the mixed mode of SDEVICE. A voltage source is connected to the detector cathode which supplies the high voltage to the detector. The n^+ layer is contacted and connected to the ground through a 90 kΩ resistance. Each strip is read through a preamplifier. Before the circuit is simulated the structure of the detector has to be defined. The simulated implantation dose of the multiplication layer is the medium dose. As used in previous simulations, 10^{11} cm^{-2} positive charges are introduced in the silicon oxide interface. The contact to the n^+ is simulated on the left edge. The contact is followed by five 200 µm wide strips, which are called strip_1, strip_2, strip_3, strip_4 and strip-5, with a pitch of 500 µm. Once the detector system is created, the circuit connections are defined in the mixed mode simulation as indicated in Fig. 3. 49.



a) b)

Fig. 3. 48. AC-LGAD pad layout a), cross-section of AC-LGAD b).

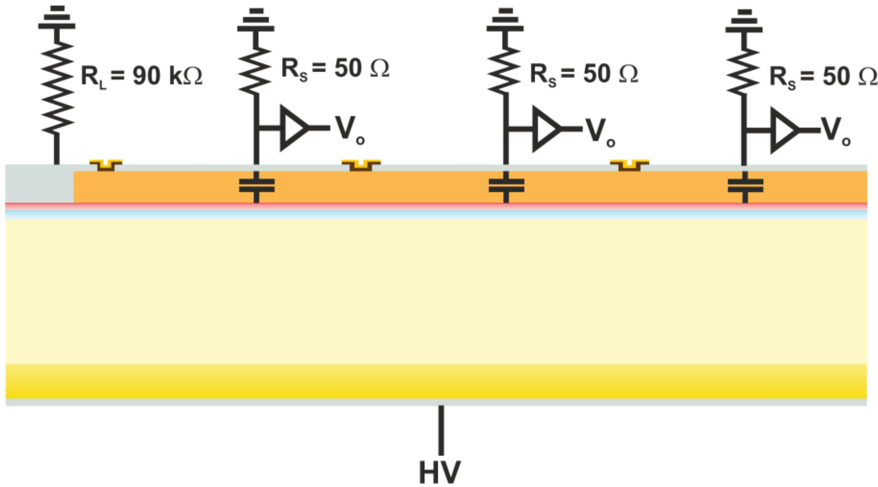


Fig. 3. 49. Schematic representation of the simulated circuit for the AC coupled LGAD strips. The oxide between the n^+ implant and the strips acts as a capacitance.

The voltage source is ramped down from 0 to -110 V while the anode is grounded through the R_L resistance. The strips are also grounded through the R_s resistance which is equal to 50 Ω. Once the anode is set to -110 V a MIP crosses the detector at certain position between strip_2 and strip_3. The induced signals on strip_1, strip_2, strip_3, strip_4 and strip_5 are plotted in Fig. 3. 50 in black, red, green and blue lines, respectively. The simulation is performed for MIPs crossing at the right edge of strip_2 a), at halfway between strip_2 and strip_3 b), at the left edge of strip_3 c) and in the middle of strip_3 d). A bipolar signal is induced in all the strips. The maximum value of the signal decreases as the distance between the position of MIPs and strips increases. For example, when a MIP crosses just at the right edge of strip_2, this strip presents the highest signal, as it is shown in Fig. 3. 50. a). The second highest signal is the one induced in strip_3, which is followed by the induced signal in strip_1, then the signal in strip_4 and finally the lowest signal in strip_5. When a MIP crosses just at halfway between strip_2 and strip_3 the induced signals in those strips are the same, as it can be seen in Fig. 3. 50. b). As MIPs get closer to strip_3, the signal height in strip_4 and strip_5 increases, while it decreases in strip_1 and strip_2, as it can be seen in Fig. 3. 50. c) and d).

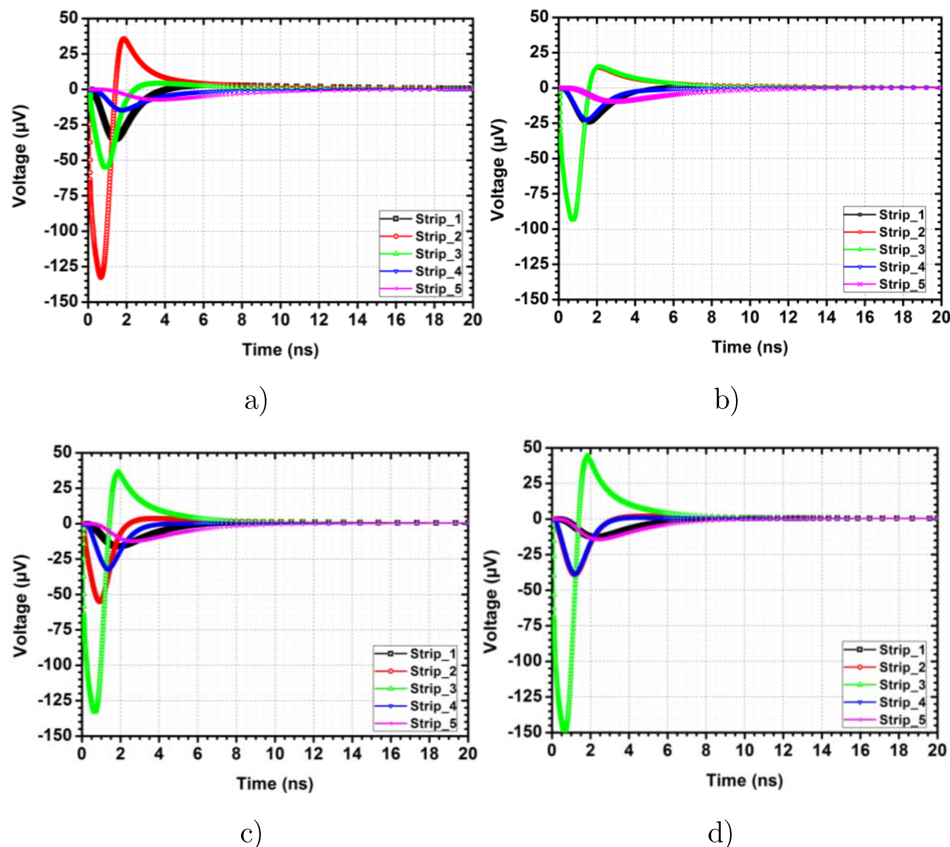


Fig. 3. 50. Induced pulses for a MIP crossing: at the right edge of strip_2 a), halfway distance between strip_2 and strip_3 b), at the left edge of strip_3 c), at the centre of strip_3 d).

An easier way to plot all this information is to represent the maximum value of the pulse as a function of MIP crossing positions for each strip. Fig. 3. 51 presents the maximum value of the induced signal which is indicated as P_{max} as a function of MIP crossing positions. The strips are also plotted for a better understanding. Once MIPs get away from the right edge of strip_2, the signal in strip_2 and strip_1 decrease, while they increase in strip_3, strip_4 and strip_5.

After this first sensor came out, a study of the design is carried out to reduce the induced signal in the neighboring strips. A cross section of the coupling system is presented in Fig. 3. 52. a). As it can be seen in the figure, the strips or pixels are coupled to the n^+ anode through the oxide capacitance C_{ox}. The n^+ implant has a low resistance R_{imp} which depends on the implant sheet resistance, the distance between strips and the length of the strips. The strips are also coupled to their neighboring strips through the interstrip capacitance C_s. Fig. 3. 52. b) shows the schematic circuit of the coupling system, which extends as the number of strips.

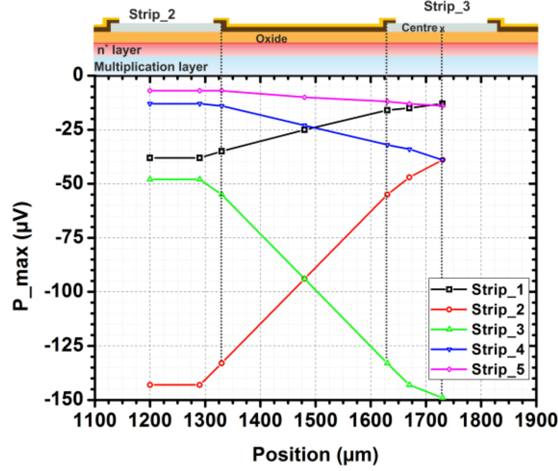


Fig. 3. 51. Maximum pulse value as a function of the MIP position.

The strips are also coupled to their neighboring strips through the interstrip capacitance C_s. Fig. 3. 52. b) shows the schematic circuit of the coupling system, which extends as the number of strips. When a MIP crosses through Strip_3 the signal on this strip depends on the oxide capacitance C_{ox} and the impedance of the strip arrangement $Z_X(R_{imp}, C_{ox}, C_s)$ as it can be seen from the equivalent circuit presented in Fig. 3. 52. c). Thus, the signal in the main strip and the neighboring strips depends on the interstrip capacitance C_s, the oxide capacitance C_{ox} and the resistance between strips R_{imp}. The simulation of the detector is carried out varying these parameters to study how much the signals change due to the parameters variations. The first simulation is done changing the sheet resistance of the n^+ implant without changing the doping profile on the n^+/multiplication layer junction. This can be achieved by a p-type superficial implantation which reduces the concentration of the net doping profile only on the surface while it maintains the doping profile near the junction. Therefore, there is no need to vary the multiplication layer implant and diffusion. The pitch and strip width are kept the same. Just the R_{imp} is modified. The results of the simulation are presented in Fig. 3. 53. b). The n^+ surface concentration is decreased two orders of magnitude, which represents an increase of a factor 10 on the R_{imp} resistance. The standard configuration is presented in Fig. 3. 53. a) for comparison. The comparison of the P_{max} as a function of the MIP position between the standard configuration and the configuration with a resistance ten times the standard resistance ($10 \cdot R_{imp}$) shows a small increase of the signal on the main strip where the MIP crosses through and a slight decrease on the neighboring strips signal when the resistive implant is implemented, as it can be seen in Fig. 3. 53. a) and b) respectively.

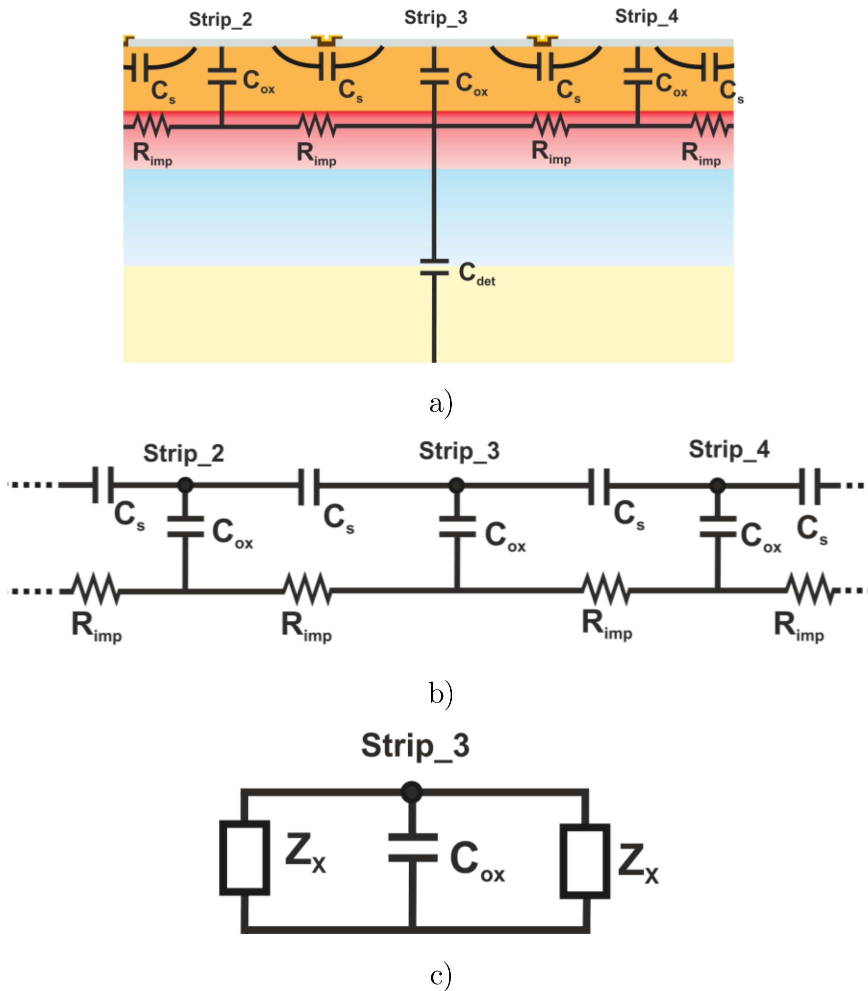


Fig. 3. 52. Cross section of the coupling system a). Schematic circuit of the coupling system b). Equivalent circuit on Strip_3 c).

The second simulation is performed varying the distance between strips using the same strip width, thickness oxide and implant resistance. In other words, the C_{ox} and R_{imp} do not vary, while the interstrip capacitance C_s is modified. In order to vary C_s the distance between strips is set to 30 µm. The results of this configuration are plotted in Fig. 3. 53. c). Although the R_{imp} is not modified, it must be taken into account that the resistance between the edge of strip_2 and the edge of strip_3 is reduced a factor of 10 due to the fact that this distance is also decreased a factor of 10. The decrease of the interstrip distance reduces the signal in the main strip where the MIP crosses through. At the same time the signal in the neighboring strips is increased. Thus, the distance between strips should be kept as large as possible.

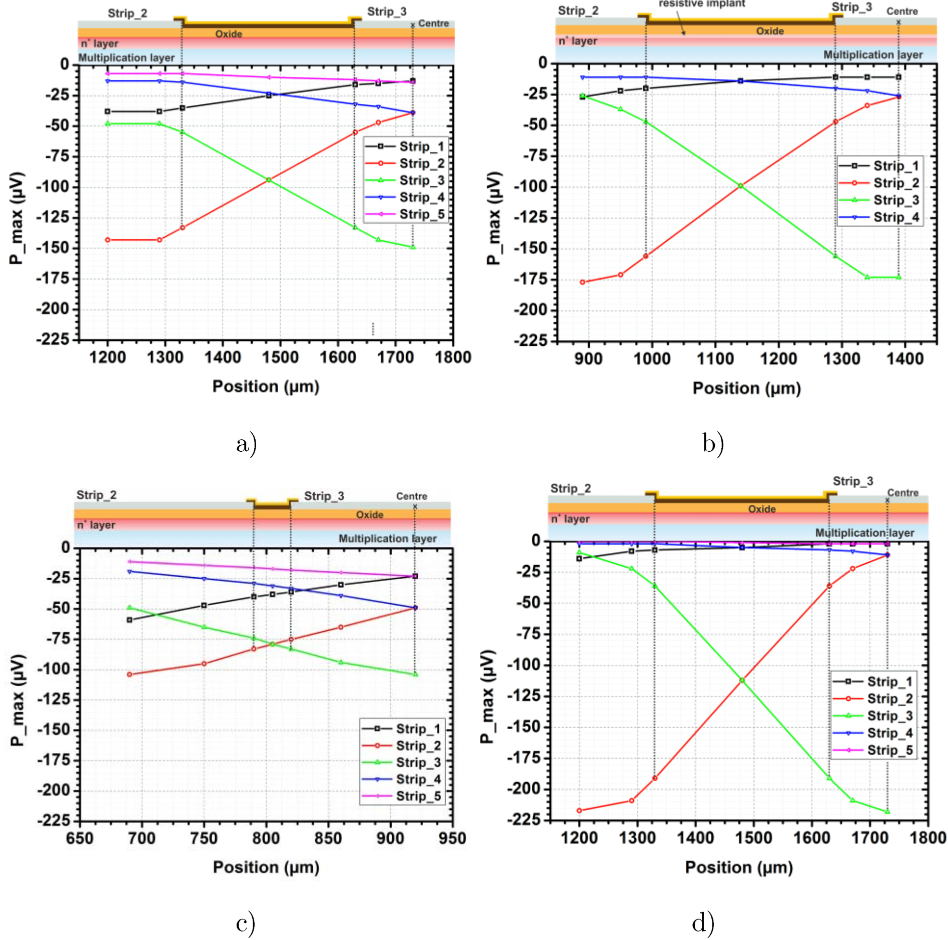


Fig. 3. 53. Pmax as a function of the MIP position for: the standard configuration where the pitch is 500 µm and the strip width 200 µm a), standard configuration with a resistive implant b), 200 µm wide strips with 230 µm pitch c), standard configuration with thinner oxide d).

The last simulation is done modifying the oxide capacitance C_{ox}. The oxide thickness is decreased a factor 8 to increase the oxide capacitance, while the pitch, the width of the strips and the R_{imp} are the same. Therefore, the oxide capacitance is $8 \cdot C_{ox}$ in the simulation. The increase of the capacitance shows a large increase of the signal in the principal strip, where the MIP crosses, decreasing the signal in the neighbor strips, as it can be seen in the representation of the results in Fig. 3. 53. d). After the comparison of all simulation results it is straightforward that the most important parameters which means a significant modifications of the signal in the main strip and the neighboring strips are the C_{ox} and C_s. Different ways to increase the oxide capacitance are the reduction of the oxide thickness, the diminution of the area of the strips and the increase of the pitch length. A batch

with different C_{ox}, C_s and R_{imp} are under production to study these new devices.

4. LGAD PROCESS TECHNOLOGY

Since 2012 LGAD devices have been produced at IMB-CNM's clean room. Through all these years, both the design and process technology of LGADs have been optimized to satisfy the required specifications of the detectors.

This chapter opens with the standard LGAD process for 285 µm thick LGADs before focusing on new detector processes. Then it continues with the device layouts of the different structures and the process technology of 50 µm thin LGADs, and ends with the new LGAD processes with a gallium multiplication layer and the standard boron multiplication layer with carbon spray.

4.1. LGAD process

The standard LGAD process technology is a well-established process on 4-inch Float Zone (FZ) silicon wafers. The silicon is <100>, p-type doped with boron, with a nominal resistivity $> 10\ \mathrm{k\Omega \cdot cm}$ and 285 µm thickness. The whole LGAD fabrication process consists of 67 steps, where the main ones being the implantation and diffusion of the P-Stop, the JTE and Guard Ring, the multiplication layer and the n^+ and p^+ contacts; these are followed by the metallization and the passivation. The main steps in the fabrication process of LGAD detectors are explained in the following sections. More detailed information about silicon manufacturing can be found in references [110], [111].

4.1.1. Field oxide and P-Stop

The process starts with the growth of a 0.8 µm field oxide on both sides of the wafer, as shown in Fig. 4. 1. a), which acts as an implantation mask. Then, the first photolithography level (P-Diff mask level) is carried out to define both the p-stop and a channel stop. As can be seen inFig. 4. 1. b), the photolithographic step consist in the spinning of a UV-sensitive photoresist on the field oxide (SiO_2) of the front side of the wafer. Then, the mask level is placed on top of the photoresist

illuminating the wafer by UV-radiation. Once the photoresist is developed (Fig. 4. 1. c), the wet etching of 0.8 µm of field oxide is performed (Fig. 4. 1. d). Afterwards, the photoresist is stripped on an O_2 plasma and a 380 Å screen oxide is grown to protect the surface before the boron implantation (Fig. 4. 1. e). The screen oxide is also important in order to avoid boron out-diffusion from silicon to gas during the subsequent thermal process. Impurity implantation is always performed with a tilt of 7º in order to avoid channeling of the impurity into the bulk. Finally, the implanted impurity is thermally activated and diffused by an oxidation process (Fig. 4. 1. f).

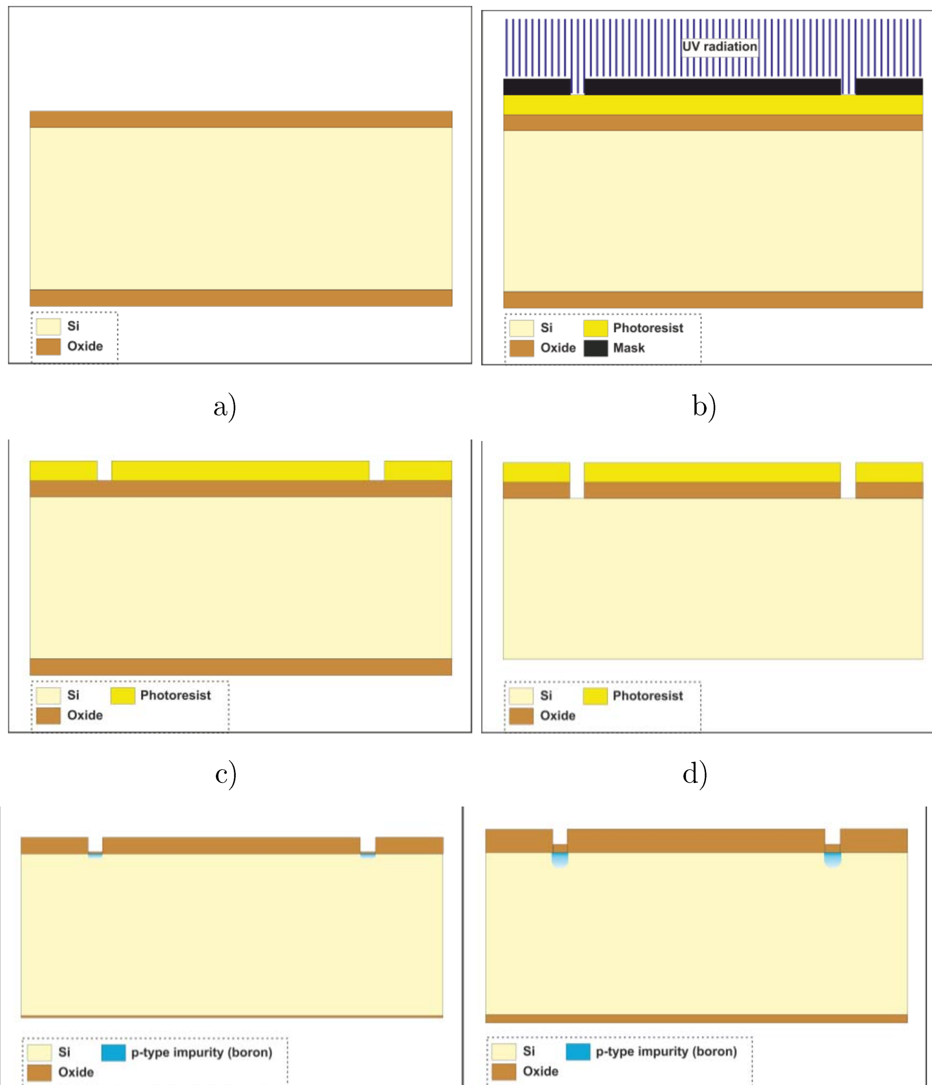


Fig. 4. 1. Field oxide growth a). P-Diff photolithography b). Photoresist development c). Oxide wet etching d). Boron implantation e) and diffusion f)

4.1.2. Junction Termination Extension (JTE) and Guard Ring

The JTE is implemented at the edge of the detection pad. The implantation is conducted with the same mask level as the guard ring. Once the implementation of p-stop is completed, the wafer is prepared for the next photolithography step, the photoresist is spun on the wafer, and the mask (JTE mask level) is aligned to the alignment pattern of the first mask level (P-Diff mask level), as it is shown in Fig. 4. 2. a). Once the photoresist is illuminated with UV-light, the wet oxide etching is performed (Fig. 4. 2. b), phosphorus is immediately implanted after the growth of the screen oxide (Fig. 4. 2. c), and finally the implanted phosphorus is thermally activated and diffused (Fig. 4. 2. d).

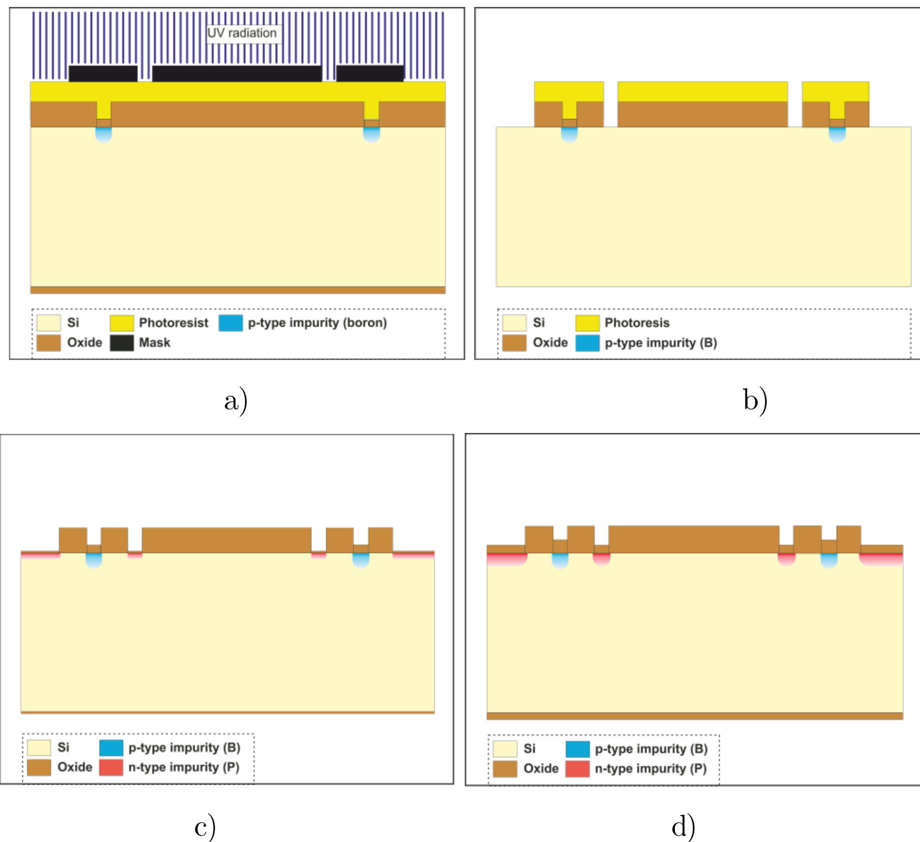


Fig. 4. 2. JTE Photolithography a) and oxide wet etching b). Phosphorus implantation c) and phosphorus diffusion d).

4.1.3. Multiplication layer

The next step is the definition and implantation of the multiplication layer. First, the photolithography of the multiplication mask level (PWell mask level) is implemented aligning the alignment pattern to the previous level (JTE mask level) (Fig. 4. 3. a). Afterwards, the oxide is wet etched (Fig. 4. 3. b) and a screen oxide is grown (Fig. 4. 3. c). Lastly boron impurities are implanted and thermally diffused (Fig. 4. 3. d). As it was discussed in the previous chapter and studied in reference [112], the implantation and diffusion of the multiplication layer are the most critical steps. A 10% increase in the boron implantation dose causes a factor 2 increase in gain. As a consequence, the voltage capability of the detector dramatically decreases.

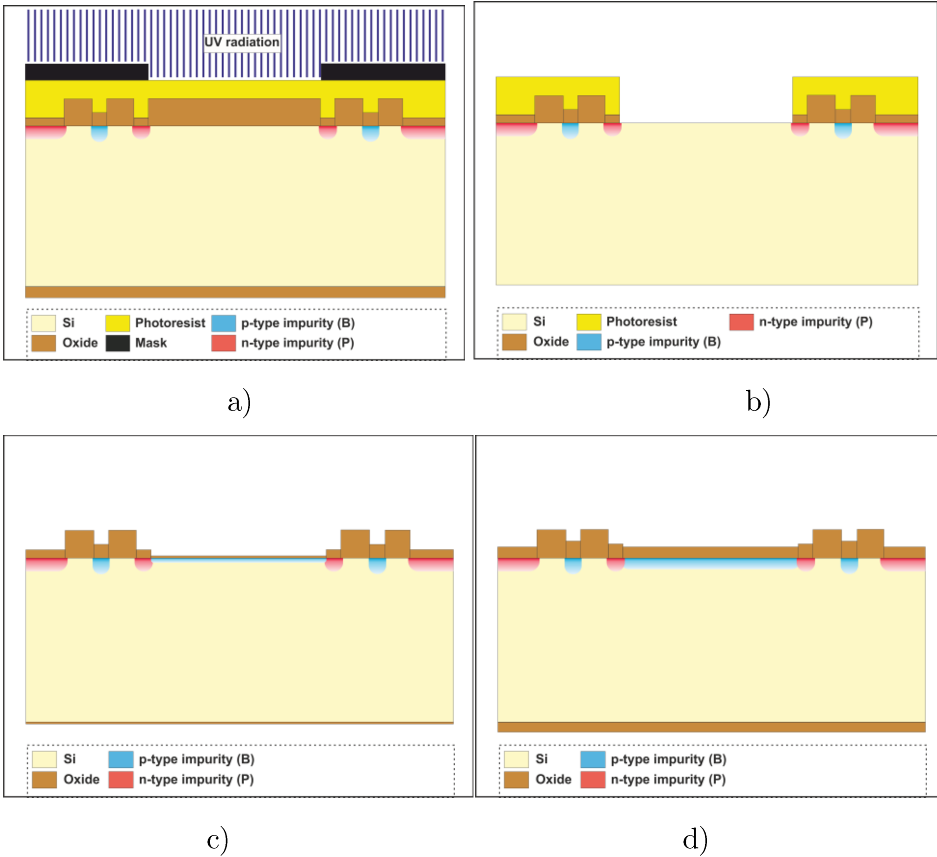


Fig. 4. 3. Multiplication layer photolithography a). Oxide wet etching b). Boron implantation c) and diffusion d).

4.1.4. n^+ and p^+ electrodes

Once the definition of the multiplication layer is completed, the place of the n^+ ohmic contact is defined by photolithography. The new mask level (N-Diff mask level) is aligned with the alignment pattern of the previous mask level, that is the PWell mask level (Fig. 4. 4. a) and the oxide is wet etched (Fig. 4. 4. b). Next the photoresist is stripped and the screen oxide is grown to protect the surface from the ion implantation. Then, the wafer is ready for the phosphorus implantation on its front side, the boron implantation on its backside (Fig. 4. 4. c), and the subsequent impurity activation and diffusion by an oxidation step (Fig. 4. 4. d).

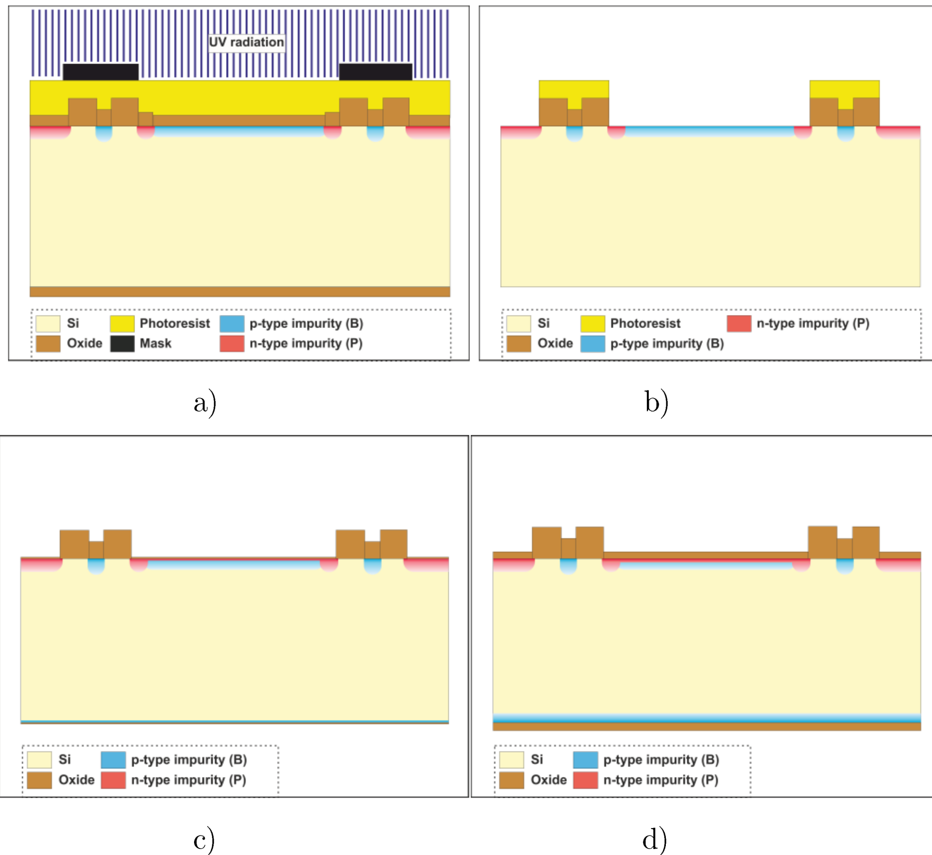


Fig. 4. 4. Photolithography step of the n^+ electrode a) and posterior oxide wet etching b). Phosphorus and boron implantations on the front and back side of the wafer, respectively c). Diffusion of both impurities d).

4.1.5. Contact opening and metallization

Before the metallization process, the contact opening must be performed in order to guarantee a good metal contact to the n$^+$ and the p$^+$ diffusions. Then, a photolithography of the mask level (window mask level) related to the contact openings is aligned with the previous mask level (N-Diff mask level) and illuminated with UV-light (Fig. 4. 5. a). Once the photoresist is developed (Fig. 4. 5. b) and the oxide is wet etched (Fig. 4. 5. c), the photoresist is stripped and the contacts are opened to sputter a 1.5 µm aluminium layer on the front side of the wafer (Fig. 4. 5. d).

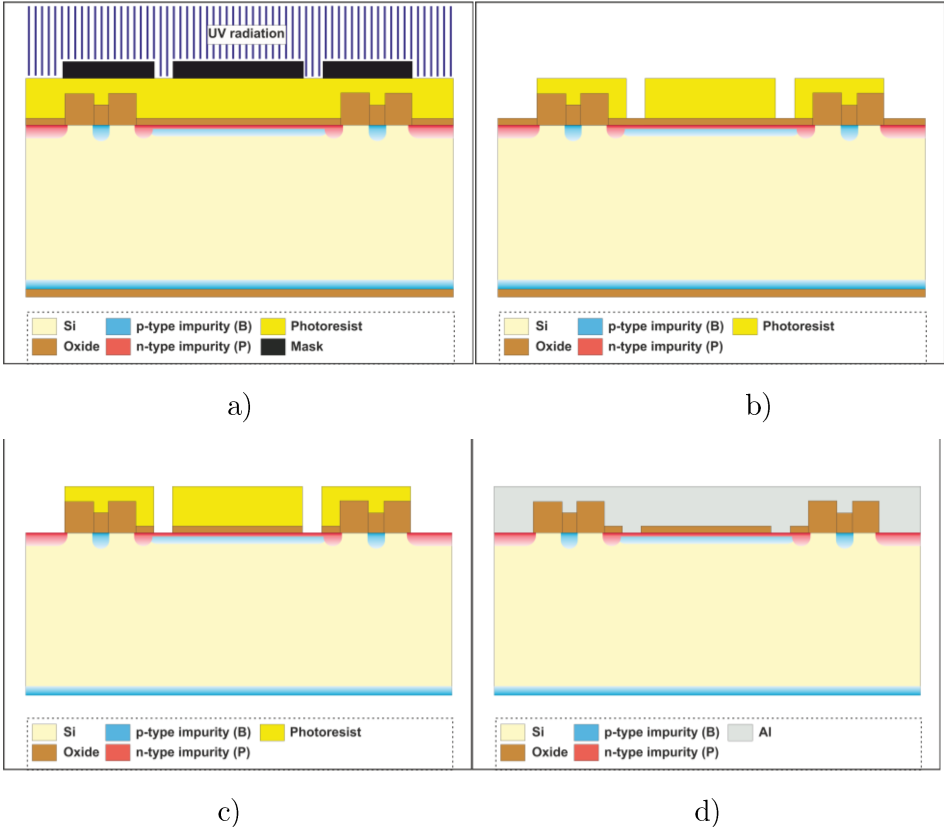


Fig. 4. 5. Photolithography of mask level window a). Photoresist development b). Oxide wet etching c). Metallization d).

As soon as the front side is metallized, the n$^+$ ohmic contact is defined with the photolithography of the metal mask level (Metal mask level). This mask level is aligned with the alignment pattern of the previous mask level (N-Diff mask level) and illuminated (Fig. 4. 6. a). Then the photoresist is developed (Fig. 4. 6. b) and the aluminium is wet etched (Fig. 4. 6. c). Afterwards the photoresist is stripped

and the wafer is cleaned in order to metallize the backside d).

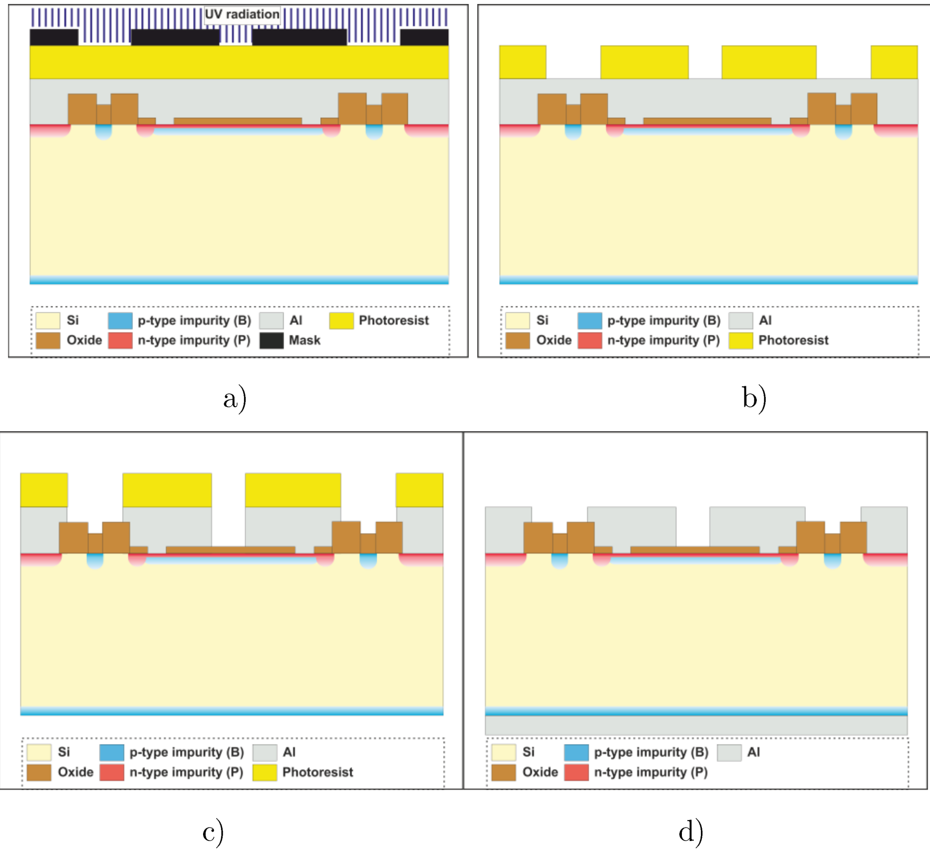


Fig. 4. 6. Photolithography of the Metal mask level a), photoresist development b). Aluminium wet etching c), and back metallization d).

4.1.6. Passivation

Passivation is the last stage of the fabrication process. It consists in the deposit of 4000Å of SiO_2 and 2000Å of Si_3N_4 as a passivation layer on the front side of the wafer. Then the last photolithography is performed using the passivation mask level (Passiv mask level), which is aligned with the Metal mask level (Fig. 4. 7. a). Once the photoresist is illuminated, it is developed (Fig. 4. 7. b) and the passivation layer is dry etched by plasma (Fig. 4. 7. c). Finally the photoresist is stripped. Since the backside is all metallized, it does not required any passivation.

Once passivation is completed, some inspection measurements are carried out before the whole process ends and the detectors are finished.

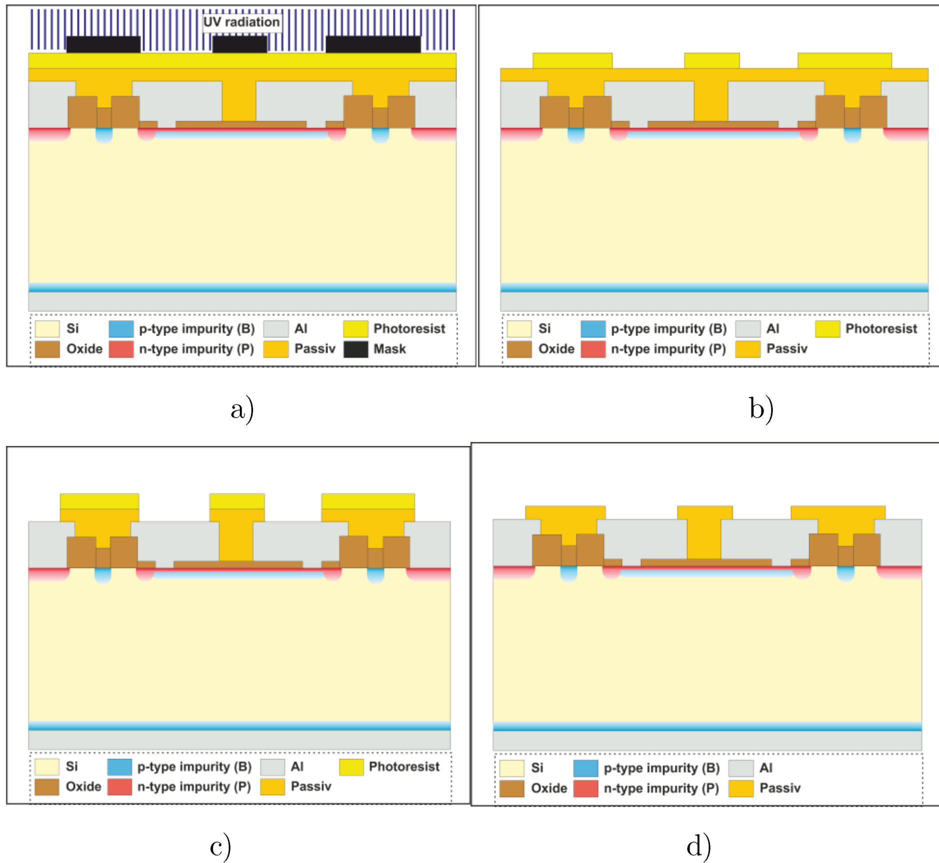


Fig. 4. 7. Photolithography of the passivation layer a). Development of the photoresist b). Plasma ion etching of the passivation layer c). Removal of the photoresist d).

4.2. Thin LGAD Process

The first batch of thin LGAD detectors was fabricated on 4-inch silicon on insulator (SOI) wafers, which is identified as Run9088. The thickness of the active wafer, called device wafer, is 50 µm. The device silicon wafer is <100>, p-type doped with boron and with a nominal resistivity $> 5\ k\Omega \cdot cm$. The thicknesses of both the buried oxide and the handle wafer are 1 µm and 300 µm, respectively. Boron is implanted on the backside of the device wafer before the SOI bonding of the device wafer to the handle wafer and the subsequent thinning of the device wafer. Once the SOI process is completed, the wafers are ready and the production of detectors can start. The batch includes 10 wafers and the whole fabrication process consists of 111 steps. The different boron implantation doses of the

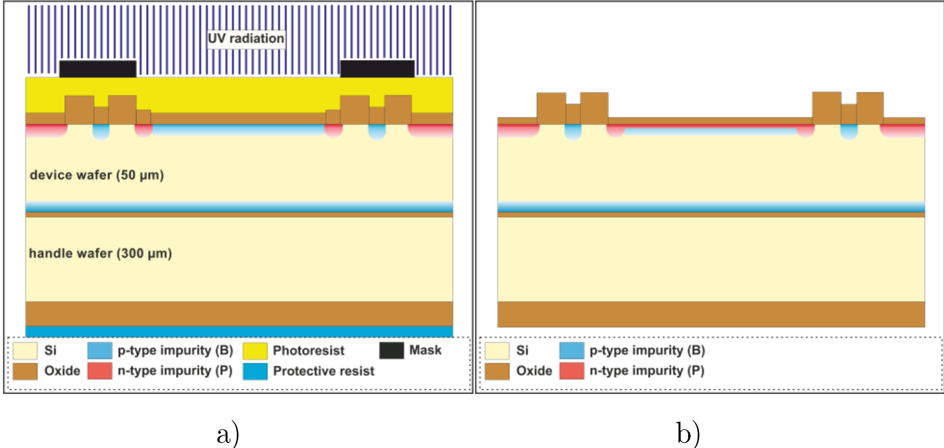
multiplication layer are specified in Table 4. 1.

Table 4. 1: Implantation doses of boron for the multiplication layer

Wafer	Dose (at./cm^2)
W3-W4	$1.8 \cdot 10^{13}$
W5-W10	$1.9 \cdot 10^{13}$
W11-W12	$2 \cdot 10^{13}$

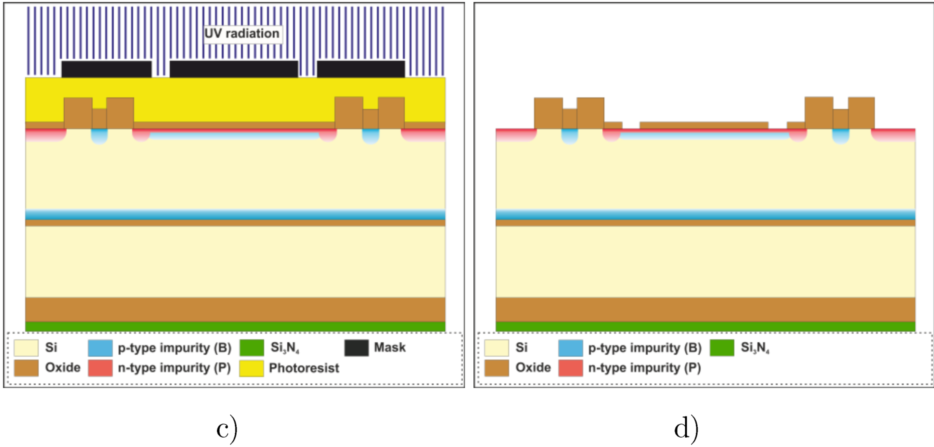
The steps are the same as for the standard LGAD process up to the implantation and diffusion of the n$^+$ contact, but for one difference: all the photolithography processes are performed with a protective resist on the backside surface. Thus, the oxide on the backside is not etched with a thickness increasing in each oxidation step. The main differing steps after the multiplication layer implantation and diffusion are introduced in this section.

First, the photolithography of the n$^+$ contact is defined on the pad and guard ring (Fig. 4. 8. a). Then, the oxide is wet etched and the photoresist is stripped. Phosphorus is implanted and diffused just after the growth of the screen oxide (Fig. 4. 8. b). In order to protect the backside surface during the handle wafer etching, a silicon nitride layer is deposited on the backside surface of the wafer. Next, the photolithography of the front side contact opening is performed (Fig. 4. 8. c). Then, the photoresist is developed, the oxide is wet etched, and the photoresist is stripped (Fig. 4. 8. d).



a) b)

Fig. 4. 8. Photolithography of the n^+ contact a). Phosphorus implantation and drive-in b). Figure continues in the next page.

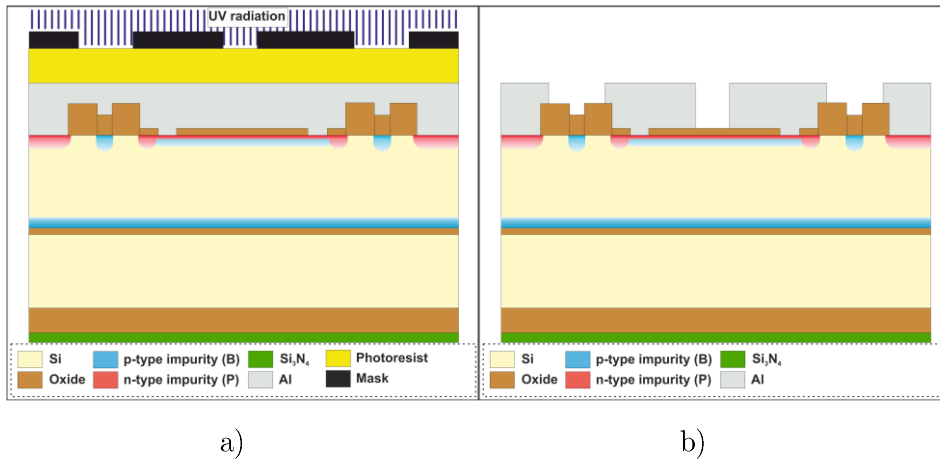


c) d)

Fig. 4. 8. Photolithography of the front side contact opening c). oxide wet etching and photoresist strip d).

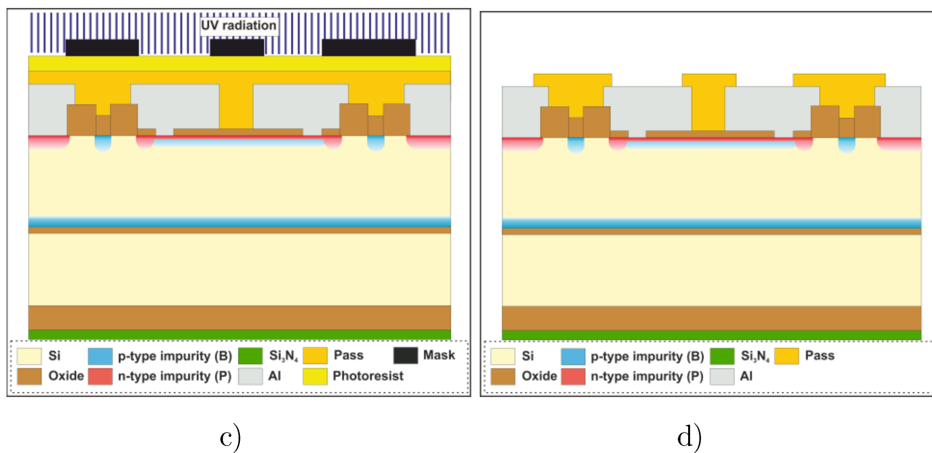
Finally, the surface is cleaned in order to sputter a 1.5 µm aluminium layer on the front side of the wafer.

After the metallization of the front side, the photolithography of the metal is defined (Fig. 4. 9. a). Once the photoresist is developed by illuminating it with UV-light, aluminium is wet etched and the photoresist is stripped (Fig. 4. 9. b). Then, the front side surface is ready, and 4000Å of SiO_2 and 2000Å of Si_3N_4 are deposited on it as a passivation layer. Afterwards, the photolithography of the passivation layer is performed (Fig. 4. 9. c), the passivation is dry etched and the photoresist is stripped (Fig. 4. 9. d). The remaining steps are the contact opening of the backside and the backside metallization.



a) b)

Fig. 4. 9. Photolithography of the front side metal a). Aluminium etching and resist strip b). Figure continues on the next page.



c) d)

Fig. 4. 9. Photolithography of the front side passivation c). Passivation etching and resist strip d).

The opening of the backside contact begins with the definition of the contact by means of the mask level (BCont mask level) photolithography, as shown in Fig. 4. 10. a). The processed front side is protected by resist, as it can be seen in the aforementioned figure. Once the photoresist is illuminated, the 1800Å of silicon nitride is dry etched (Fig. 4. 10. b). Next, the 1.2 µm of field oxide is dry etched and the photoresist is stripped (Fig. 4. 10. c).

Then, 300µm of silicon are wet etched by KOH etching process. The field oxide and the Si_3N_4 act as a mask for the KOH etching. The KOH etching is an anisotropic silicon etching process characterized by the etching of <100> plane

with an angle of 54.74º, as it can be seen in Fig. 4. 10. d). Once the KOH etching reaches the buried oxide, the wafers are cleaned before the next wet etching of the buried oxide (box) begins (Fig. 4. 10. e). Finally, an aluminium layer is sputtered on the detector backside and the detector process finishes (Fig. 4. 10. f).

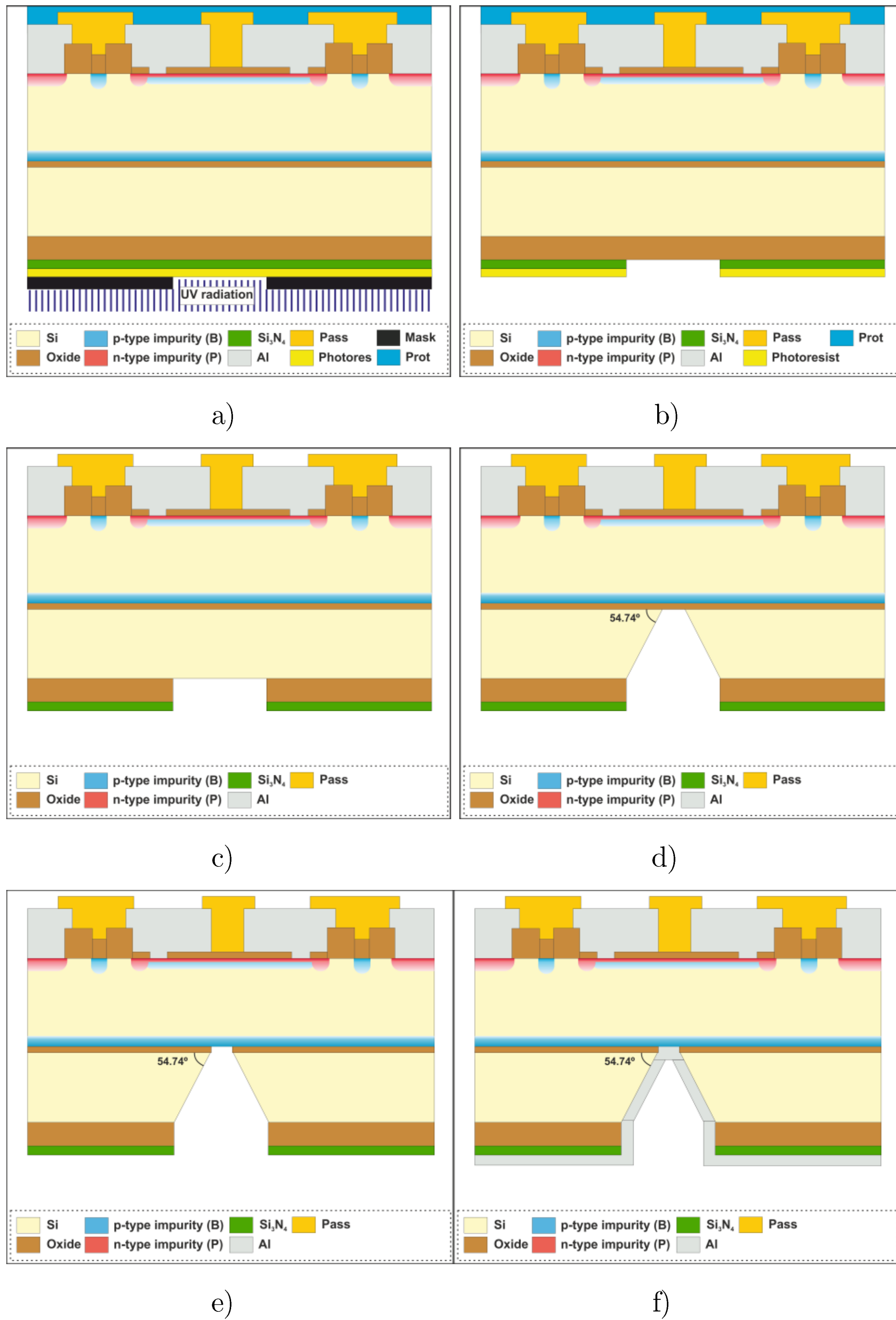


Fig. 4. 10. Photolithography of the backside contact opening a). Si_3N_4 dry etching b). SiO_2 dry etching and removal of the photoresist c). KOH etching d). Wet etching of the buried oxide e). Metallization of the backside f).

In 2017 a new batch, called Run10478, of thin LGADs on silicon-to-silicon wafers was processed at IMB-CNM's clean room. The batch consisted of ten Si-Si wafers and three HR FZ silicon wafers. The silicon device wafer from the Si-Si wafer is <100> oriented, p-type doped with boron and with a nominal resistivity $>$ $10k\Omega \cdot cm$. The thickness of the device wafer and the handle wafer are 50µm and 300µm, respectively. The handle wafer is a low resistivity p-type doped with boron, which acts as a p^+ contact. The use of Si-Si wafers reduces the number of steps in the process because it suppresses the pre-implantation of the p^+ contact before wafer bonding and the posterior etching of both the handle wafer and the buried oxide to contact the p^+ implant.

A new mask set (CNM873) was designed for this batch, which includes new devices for the HGTD with JTE and passivation openings compatible with the AltiRoc0 readout.

The whole process consists of 83 steps. The steps are the same as the standard LGAD process described in section 4.1, but no p^+ implantation on the backside is required because the handle wafer acts as a p^+ contact. After the implantation and diffusion of the n^+ contact, the front side contact opening is performed and the metal is immediately sputtered on the front side surface.

The photolithography of the metal level is carried out, as shown in Fig. 4. 11. a). Afterwards, aluminium is wet etched, the photoresist is stripped, and the backside is metallized (Fig. 4. 11. b). Finally, the passivation layer is deposited on the front side of the wafer. The passivation layer is photolithographed and wet etched, as presented in Fig. 4. 11. c) and d), in order to open the contacts.

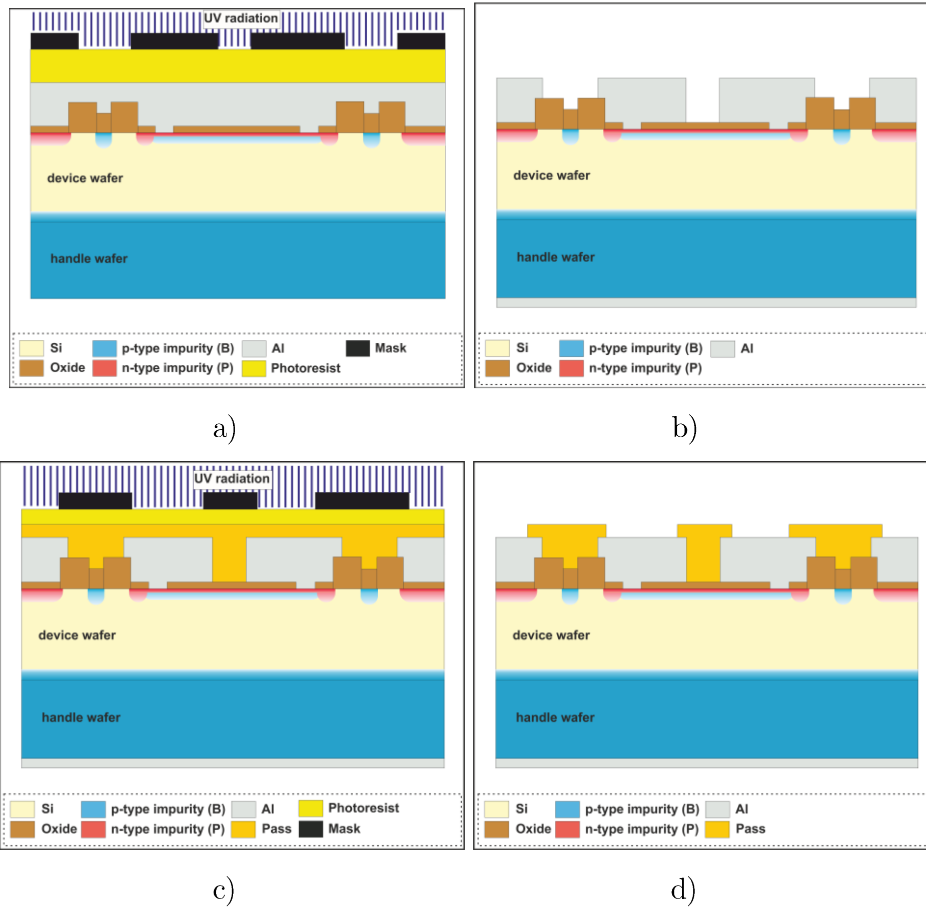


Fig. 4. 11. Representation of the photolithography of the metal layer a), the dry etching of the aluminium, stripping of the photoresist and the sputtering of aluminium on the backside b). Photolithography of the passivation layer c). Dry etching of the passivation layer and stripping of the photoresist d).

4.3. LGAD Process with Gallium multiplication layer

Previous studies on gallium substrates show a lower acceptor removal constant compared to boron substrates, as aforementioned in section 3.1.5. Consequently, a new process with gallium impurities in the multiplication layer has been set-up to develop more radiation resistance LGAD detectors.

Process technology simulations were conducted to determine the implantation energy, dose and the thermal diffusion of gallium, as mentioned in section 3.1.5.1.

The first batch of thin LGADs on Si-Si wafers with gallium, called Run10924, finished in April 2018. A total of nine silicon wafers were processed: seven Si-Si

wafers and two high resistivity FZ wafers. The silicon device wafer of the Si-Si wafer is <100> oriented, p-type doped with boron and with a nominal resistivity > $5k\Omega \cdot cm$. The thicknesses of both the device wafer and the handle wafer are 50µm and 300µm, respectively. On the other hand, the high resistivity FZ wafers are <100> oriented, p-type doped with boron, with a nominal resistivity of 10 $k\Omega \cdot cm$, and a thickness of 285 µm. Table 4. 2 presents the different values of the gallium implantation doses and the type of wafers.

The mask set used is CNM873 and the steps are the same as in the standard LGAD process, but the implantation dose, diffusion time, diffusion temperature and oxidation ambient are adjusted to gallium. Gallium is a well-known fast diffuser in silicon oxide. Even though the segregation coefficient of gallium is larger than unity, it does not follow the expected gallium pile-up during oxidation [113]. The transport coefficient to the silicon oxide is so large that the concentration of gallium in silicon decreases. Studies indicate that SiO_2 is not an effective film to use on gallium doped semiconductors for protection against Ga loss during high temperature anneals [114]–[117]. The oxidation ambient of gallium diffusion has been changed, as a consequence.

Table 4. 2: Implantation doses of gallium for the multiplication layer

Wafer	Dose (at./cm^2)	Wafer type
W1	$5 \cdot 10^{13}$	Si-Si
W2	$5.5 \cdot 10^{13}$	Si-Si
W3-W4; W8	$5.8 \cdot 10^{13}$	Si-Si; HR FZ
W5-W6; W9	$6.0 \cdot 10^{13}$	Si-Si; HR FZ
W7	$6.5 \cdot 10^{13}$	Si-Si

4.4. LGAD Process with Carbon Spray

Carbon is an electrically neutral impurity in silicon. Interstitial carbon (C_i) is highly mobile, which form C_i-O_i complexes after electron irradiation of carbon doped CZ wafers [97]. Therefore, the concentration of O_i after irradiation is expected to be reduced in the presence of C_i. Thus, the boron removal will also be reduced after irradiation. On the other hand, the introduced substitutional carbon is a sink of interstitials, and consequently it decreases the concentration of

interstitials. At high concentrations of substitutional carbon, the diffusion of boron and phosphorus is reduced due to the suppression of interstitials [81], [83], [85], [99], [100]. If the concentration of carbon is too high the doping profile of boron and phosphorus will be modified, and consequently the gain will change.

Carbon was implanted in two different batches. The first batch, called Run9889, is processed on high resistivity silicon wafers which are <100> oriented, p-type boron doped, with a nominal resistivity $> 10\ k\Omega \cdot cm$ and a wafer thickness of 285 µm. Five implantation doses for the boron multiplication layer have been used, as shown in Table 4. 3. Two wafers have been implanted with the same implantation dose, but one with carbon spray and the other without. Thus, the effect of co-implantation of carbon, boron and phosphorus are studied.

The process starts with the growth of 150 Å pedestal oxide and the implantation of carbon through the pedestal oxide on the whole wafer. After the implantation, the pedestal oxide is etched and the process follows the same steps of the standard LGAD fabrication.

The carbon implantation dose and energy have been determined by TCAD simulation, as presented in section 3.1.5.2, in order to obtain a carbon concentration in the range of the oxygen concentration. Simulations of the doping profiles were presented previously in Fig. 3. 7. a).

Table 4. 3: **Implantation doses of boron for the multiplication layer**

Wafer	Dose (at./cm^2)	Carbon Spray
W2; W7	$1.5 \cdot 10^{13}$	Yes; No
W3; W8	$1.7 \cdot 10^{13}$	Yes; No
W4; W9	$1.8 \cdot 10^{13}$	Yes; No
W5; W10	$1.9 \cdot 10^{13}$	Yes; No
W6; W11	$2 \cdot 10^{13}$	Yes; No

On the other hand, wafer number 5 from the LGAD batch on Si-Si wafers, called Run10478 and presented in section 0, has been implanted with carbon spray, as well.

5. Characterization of the produced detectors

Basic procedure to test the performance of the fabricated devices and study if they fulfill the experiment requirements is to perform electrical, charge collection and timing measurement before and after irradiation to the expected fluences of the HL-LHC. In this chapter, the comparison between unirradiated and irradiated produced sensors is presented. First, a study on 285 µm thick LGADs is presented. Afterwards, the results on thin LGADs devices for the ATLAS experiment are introduced. The electrical characterization of the detectors includes the leakage current and capacitance measurements as a function of the reverse bias. Transient Current Technique (TCT) studies and radioactive source charge collection measurements are performed to study the charge collection performance. Timing studies are obtained by radioactive source charge collection and test beam characterization. The whole measurements are done in a humidity controlled ambient with N_2 flow at 20 ºC for unirradiated devices and -20 ºC for irradiated sensors. The devices are irradiated with neutrons at Ljubljana TRIGA nuclear reactor [118], with 24 GeV/c protons at the CERN IRRAD facility [119], and with gamma radiation at Gamma Irradiation Facility at Sandia National Laboratories [120]. Those radiation campaigns were carried out in the framework of the RD50 collaboration.

5.1. Measurements on 285µm thick LGAD

LGADs were designed and fabricated for the first time on 285 µm high resistivity p-type float zone substrates at IMB-CNM in 2012. Since then, the RD-50 community has been enrolled in the study and characterization of these detectors before and after gamma, neutron, and proton irradiation. In this section the measurements on 285 µm LGAD will be presented.

5.1.1. UnIrradiated samples

The measured LGAD and p-i-n detectors are from batch number 7859. As aforementioned, they have 285 µm thickness, a pad area of 3.2x3.2 mm^2 and an active area of 3.3x3.3 mm^2. A high and low boron doses were implanted at the multiplication layer, $1.8 \cdot 10^{13}$ atoms · cm^{-2} and $2.0 \cdot 10^{13}$ atoms · cm^{-2} respectively.

5.1.1.1. LGAD electric characterization

The electric characteristics of the LGAD detectors are studied before their shipment to other institutes within the RD50 collaboration. The measurements are performed on LGAD and p-i-n devices in a controlled temperature (20 ºC) and dry environment (N_2 flow). The explanation of the measurement setup and procedure is extensively described on Appendix B. Cathode current is measured as a function of the reverse applied bias, which is swept up to the device breakdown voltage. The leakage current, power dissipation and breakdown voltage are extracted from this measurement. Current measurements of the first batches are reported in references [20], [58], [121], [122]. Fig. 5. 1. a) and b) present those results. LGAD and p-i-n diodes show a voltage capability higher than 1000 V for both implantation doses and a leakage current in the range of 60 nA for low dose implantations of the multiplication layer (open symbols) and 700 nA for high dose implantations (dashed lines). P-i-n diodes present a leakage current in the range of 10 nA (solid lines). Fig. 5. 1. b) is a magnification of the leakage current between 10 and 200 V making clear the difference between LGAD and p-i-n diodes. Meanwhile, LGAD devices exhibit a sudden increase of the leakage current between 20 and 30 V, p-i-n diodes does not show this increase. The leakage current on LGADs is less than p-i-n diodes until 20 V because the volume of the depletion region of p-i-n diodes is larger than LGADs. Thus the amount of thermally generated carriers in p-i-n diodes is bigger than LGADs. Once the multiplication layer of an LGAD is depleted at 23 V the space charge region spreads out into the substrate bulk.

Thermally generated carriers in the depletion region of an LGAD are multiplied.

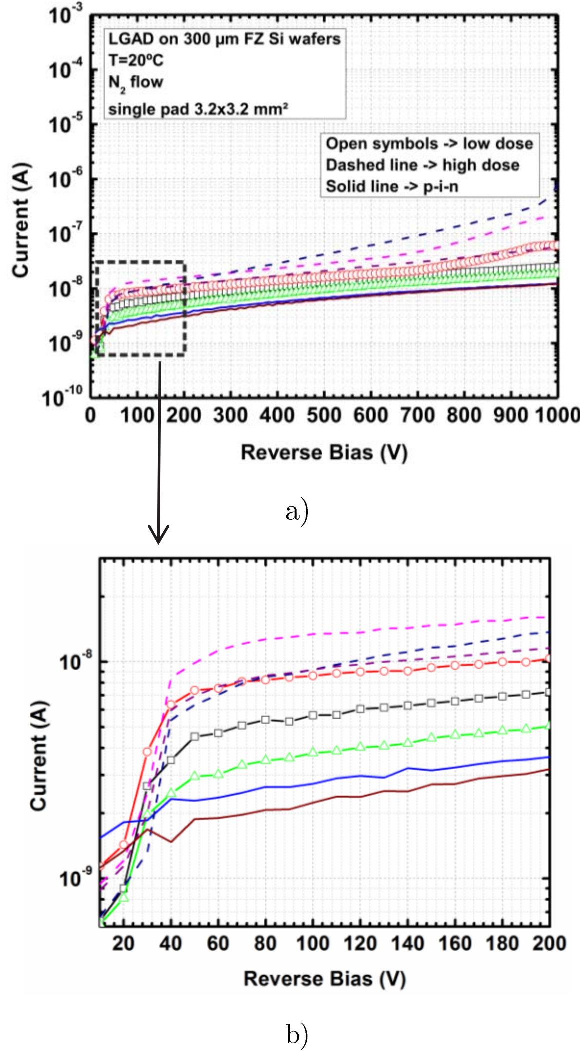


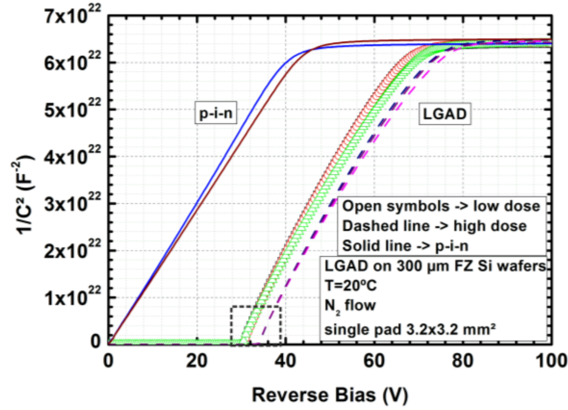
Fig. 5. 1. I(V) curves of LGAD and p-i-n devices on 285 µm thick high resistivity silicon with a low dose implantation of the multiplication layer, open symbols, high dose implantation of the multiplication layer, dashed lines, and p-i-n diodes, solid lines, (a). Zoom of the delimited region (b).

Therefore, the leakage current of an LGAD device is higher than the leakage current of a p-i-n diode after the depletion of the multiplication layer.

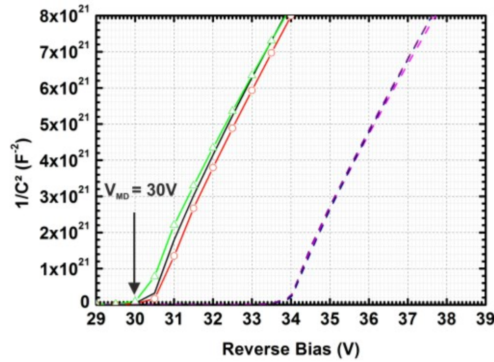
Another important measurement of the detector is the bulk capacitance. The full depletion of the device, the depletion of the multiplication layer and the equivalent noise charge (ENC) are extracted from the capacitance measurement [42], [123]. In order to measure the capacitance, the parallel equivalent mode is used because the parallel resistance at the beginning of the detector depletion, which is the worst

case scenario, is more significant than the series resistance. Therefore, the parallel model is a more appropriate description of the detector depletion. The frequency and amplitude of the AC signal which are used to measure the capacitance of unirradiated detectors are 10 kHz and 500 mV, respectively. Detailed information about the capacitance setup can be found in Appendix B.

As mentioned in the introduction, the representation of the capacitance as a function of the reverse bias voltage provides the full depletion voltage of the detector. Fig. 5. 2. a) shows the $1/C^2$-V curve for single pad LGAD detectors with a low dose implant (open symbols), and high dose implant (dashed lines) of the multiplication layer. The $1/C^2$ vs reverse bias for p-i-n devices is also plotted (solid lines). This $1/C^2$ of representation gives a rough estimation of the gain. The differences between LGADs and p-i-n $1/C^2$-V curves are significant. It is clear from Fig. 5. 2. a) and b) that LGADs curves present three different slopes. While p-i-n curves only exhibit two slopes. The $1/C^2$ as a function of the reverse bias voltage for low implantation dose of the multiplication layer is plotted in solid



a)



b)

Fig. 5. 2. I(V) curves of LGAD and p-i-n devices on 285 µm thick high resistivity silicon with a low dose implantation of the multiplication layer, open symbols, high does implantation of the multiplication layer, dashed lines, and p-i-n diodes, solid lines, (a). Zoom of the delimited region (b).

lines. These LGADs have a first slope between 0 and 30 V, a second slope between 30 and 70 V, and a third slope for voltages higher than 70 V. The first slope, known as foot, is related to the multiplication layer concentration. The range of this slope gives an estimation of gain for different implantation doses of the multiplication layer. The example presented in Fig. 5. 2. b) exhibits a slope which extends up to 30 V. Therefore 30 V is the voltage needed to deplete the multiplication layer and it is indicated as V_{MD}. In the same example higher implantation dose of the multiplication layer is plotted in dashed lines. This implantation dose shows a full depletion of the multiplication layer in the range of 34 V. Then, those devices will have a higher gain. Once the multiplication layer is full depleted at 30 V(34 V) the space charge spreads across the bulk quickly until 65 V(74 V) when the device with low(high) implantation dose is full depleted. Afterwards, the capacitance remains constant.

5.1.1.2. Gain measurements

Although, the $1/C^2$-V plot gives a qualitative measurement of the LGAD gain, a quantitative measurement of the LGAD gain is required. Even though the detector study in test beam facilities before the installation is required, there are few facilities and the given time to study the detectors is limited and expensive. Then a previous study in lab with radioactive sources and laser is important in order to not waste time in the test beam. In this section, gain measurements of LGAD on 285 µm are presented. The gain can be measured by Transient Current Technique (TCT), radioactive source measurements or test beam measurements. It is worth to mention that the study of the gain is done by different institutes with different sources. The obtained gain values are identical.

A gain study with a tri-alpha source is carried out at IMB-CNM. More detailed information about the readout boards and the experiment setup can be consulted in Appendix C and reference [58]. The samples are exposed to the tri-alpha source from the backside. As it is explained in reference [58], measurements performed for a front side illumination gives a lower gain than backside illumination due to the fact that alpha particles have a penetration depth into Silicon of 20 µm [40] and the generated e^- along these 20 µm do not acquire enough energy to start the impact ionization. On the contrary, the generated e^- from backside illumination are drifted all the silicon bulk acquiring sufficient energy to trigger the impact ionization. Fig. 5. 3. a) presents the tri-alpha source spectrum for p-i-n diodes. The corresponding channels for the three peaks of the tri-alpha source are constant versus the increase of the applied bias for the p-i-n structures. In contrast, the tri-alpha spectrum for an LGAD shows two sets of three peaks, as shown in Fig. 5. 3. b). The first set, located at the same channels of the p-i-n diode, is the signal of the generated electron-hole pairs that goes through the JTE instead of the multiplication layer. The second set is the corresponding tri-alpha spectrum for the electron-hole pairs crossing the multiplication layer. As it is shown in Fig. 5. 3. b), this tri-alpha spectrum increases as a function of applied reverse bias.

The gaussian fit of each peak gives the most probable value of the channel for both devices. The gain has been calculated as the ratio of the most probable value for LGAD to p-i-n. The gain calculation for LGADs with low implantation dose (red line) and high implantation dose (green line) are plotted in Fig. 5. 4.

Charge collection measurements are also carried out for a Minimum Ionizing Particle (MIP). MIPs are charged particles, which embody the minimum ionizing losses in matter. In laboratory conditions, beta emitter such as ^{90}Sr is used as a

MIP source. The experiment setup, readout electronics and results are presented in reference [87], [124]. LGAD gain is in the range of 3-5 for devices with low implantation dose of the multiplication layer. High implantation dose devices show a gain between 7 and 17.

After the characterization of LGADs in laboratories, they are also tested in beam facilities. A complete discussion of the measurement in tests beam can be consulted in references [121], [125]. The timing performance of the LGADs devices is studied and a time resolution of 110 ps was achieved in the test beam. In comparison, p-i-n detectors with the same area and thickness show a time resolution of 180 ps.

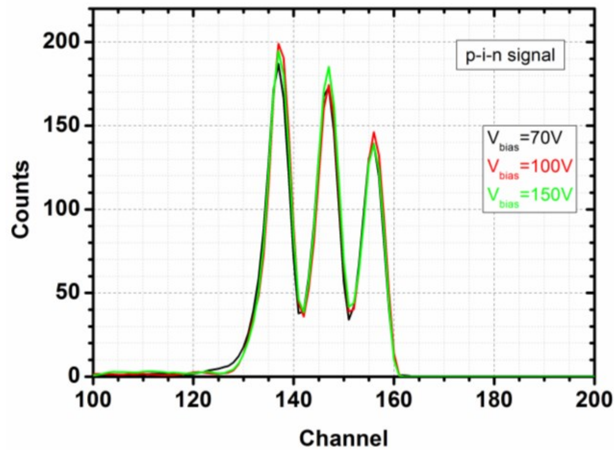


Fig. 5. 3. a) Tri-alpha source spectrum for a p-i-n diode. and an LGAD device with a low implantation dose of the multiplication layer b).

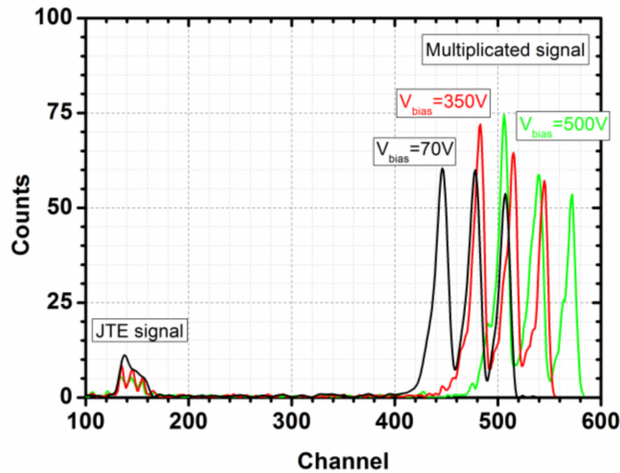


Fig. 5. 3. b) Tri-alpha source spectrum for an LGAD device with a low implantation dose of the multiplication layer.

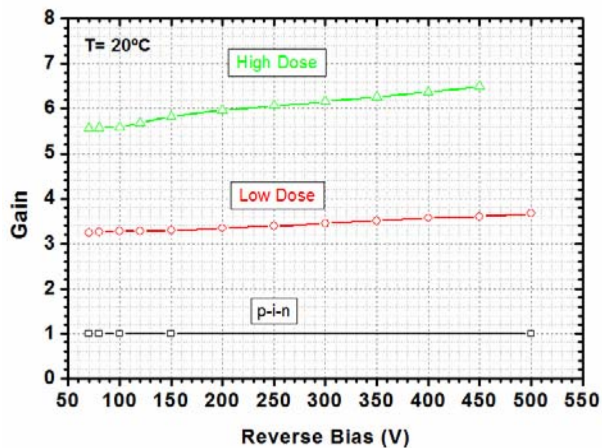


Fig. 5. 4. Gain measurement of LGAD structures for back-side illumination with a tri-alpha source.

5.1.2. Irradiated samples

As introduced in section 2.6, two radiation damage mechanisms affects the irradiated silicon devices: the ionizing and the displacement damage. In this section, a study of the ionizing damage on LGAD samples from run 7859 is performed and the main effects of the displacement damage on LGADs are introduced.

5.1.2.1. Ionizing Damage

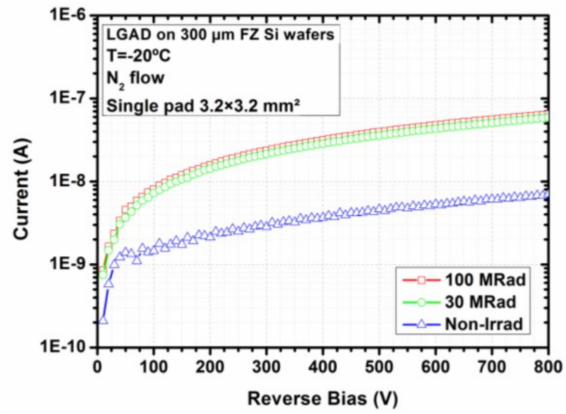
The main effect of ionization damage on LGADs is the increase of the oxide positive charge and the consequent formation of a conductive layer of electrons attracted to the interface by the positive oxide charge. Then, the inverted channel short-circuits the pad with the guard ring and p-stop implantation between the pad and the guard ring is implemented in order to avoid short circuits.

^{60}Cb source is the gamma source used to study ionizing damage in devices. LGAD samples are irradiated to 30 and 100 MRad at Gamma Irradiation Facility at Sandia National Laboratories [120]. b)

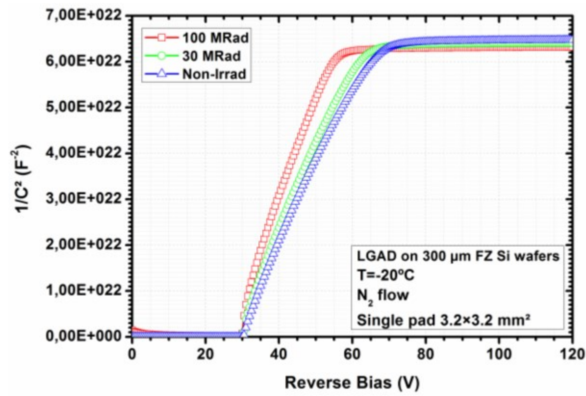
Fig. 5. 5. a) shows the current as a function of the reverse applied bias for gamma irradiated LGADs. The leakage current increases one order of magnitude, saturating after 30 MRad. The leakage current increase is caused by interface traps and oxide charges which increase the surface leakage current. The capacitances before and after gamma irradiation are also compared. $1/C^2$ as a function of the reverse applied voltage and the gamma irradiation shows the same depletion of the multiplication layer as presented in b)

Fig. 5. 5. b). There is only a small difference in the full depletion voltage of the detector, due to the inverted channel below the oxide that introduces an edge effect in the depletion of the detector. Both measurements were done in a humidity controlled environment and at -20 ºC on LGADs with a pad size of 3.2×3.2 mm^2.

After the IV and CV measurements, the gain measurement is performed with the experimental setup detailed in Appendix C. The measurement is performed in a controlled ambient and temperature at 20ºC. The irradiated and non-irradiated detectors are mounted on PCB board with an Amptek charge sensitive preamplifier (A250) and Amptek shaping amplifier (A275). The signal is also amplified and shaped on an Ortec amplifier. After that stage, the signal is processed with a MultiChannel Analyzer (MCA). A tri-alpha source is used to generate electron-hole pairs in the detector bulk. This alpha emitter source presents three peaks, as seen in Appendix C, which correspond to the three most probable alpha decays. The gaussian fit of the peaks gives the most probable value of the channel for both devices. The gain is calculated as the ratio of the most probable value for LGAD to p-i-n. Fig. 5. 6. presents the gain results obtained with the tri-alpha source on gamma irradiated LGADs. The difference in gain is in the range of 10%. This difference could be attributed to the inherent differences between detectors. In summary, ionizing radiation does not alter the performance of LGAD devices.



a)



b)

Fig. 5. 5. Current versus reverse applied bias for gamma irradiated LGADs at 30MRad and 100MRad a). $1/C^2$ versus reverse applied voltage before and after irradiation b).

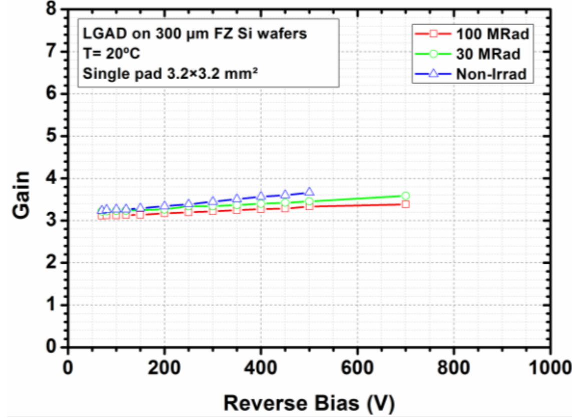


Fig. 5. 6. Gain measurement done with a tri-alpha source on LGAD detectors before and after gamma irradiation.

5.1.2.2. Displacement damage

The electrical and gain measurements are also studied after an irradiation campaign with neutrons at Ljubljana TRIGA nuclear reactor [118] and 24 GeV/c protons at the CERN IRRAD facility [126]. Both studies report the significant decrease in gain as the fluence increases. The irradiated devices collect the same charge as a p-i-n diode after a $2 \cdot 10^{15}$ n_{eq}/cm^2. The gain decrease is attributed to the boron removal [61], [127] of the multiplication layer and the double junction effect [64].

5.2. Measurements on HGTD and CT-PPS detectors

In order to study the detectors without the use of a customized readout board as the AltiRoc0, single pad structures are implemented in each wafer to test the device on single channel boards. The single pads are from Run9088 and Run10478, which differ on the handle wafer bonding, the backside opening and the implantation doses of the multiplication layer, as described in chapter 0. While all three implantation doses of the multiplication layer are measured from Run9088, only one implantation dose of the multiplication layer is measured from Run10478.

5.2.1. Unirradiated samples

Two different single pads are produced in Run9088, the LGA and LGB pads. The size of the LGA and LGB single pads are 1.2x1.2 mm^2 and 3.2x3.2 mm^2,

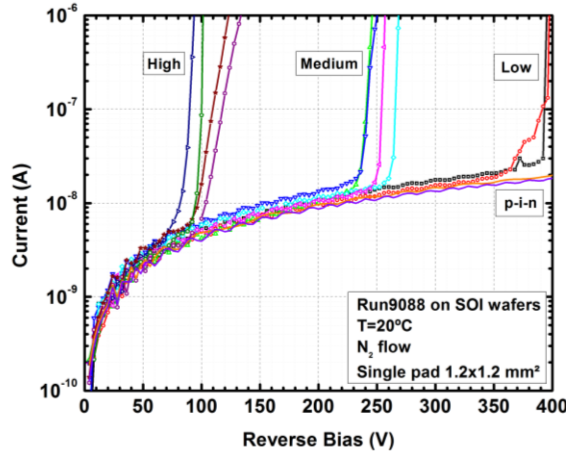
respectively. Once the detectors are full depleted, the active thickness is 45µm and the active areas are 1.3x1.3 mm^2 for LGA and 3.3x3.3 mm^2 for LGB.

Structures from Run10478 are the same size as LGA pads and the active thickness is 45µm also.

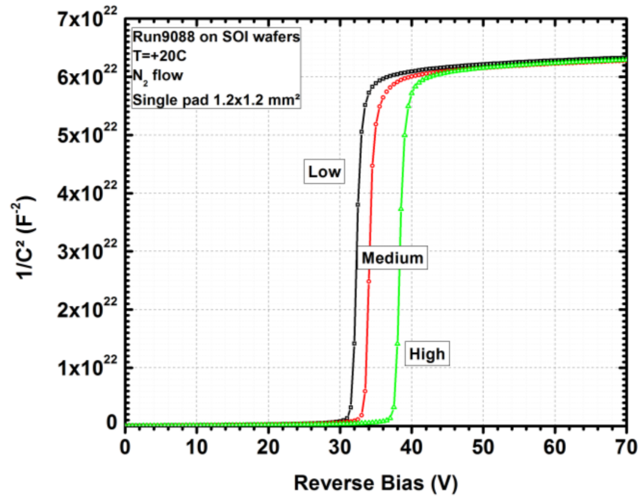
The measurements presented in the next sections are performed on LGA from both batches and LGB pads from batch Run9088.

5.2.1.1. Electrical characterization

Single pad diodes are characterized at the IMB-CNM facilities in order to evaluate their electrical response under typical operating conditions. The used setup is described in Appendix B. The measurements are performed individually on all the samples, after the dicing process, in a controlled temperature (20 ºC) and dry environment (N_2 flow). Cathode current and bulk capacitance values were measured as a function of the reverse applied bias, which is ramped up to the device breakdown. LGA single pads on SOI wafer show different voltage capability depending on the implantation dose, as it can be seen in Fig. 5. 7. a). The voltage capability of devices with medium dose is in the range of 250 V, while the breakdown voltage of detectors with high dose is 100 V. These results agree with the simulation presented in Fig. 3. 19. a) in the previous chapter 1. Standard p-i-n diodes fabricated with the same process technology as the LGAD, but skipping the multiplication layer, are also measured and presented in solid lines in the Fig. 3. 19. a).



a)



b)

Fig. 5. 7. Current as a function of the reverse applied voltage a) and $1/C^2$ versus reverse applied voltage b) for LGA structures from Run9088.

Bulk capacitance is measured as a function of the reverse bias, as well. Fig. 5. 7. b) shows the $1/C^2$–V curve for LGA single pads integrated on SOI wafers, where the characteristic foot of the LGAD, related to the depletion of the multiplication layer, can be observed. As expected, the highest dose corresponds to the highest depletion voltage of the multiplication layer (V_{MD} = 38 V). The detector active volume becomes depleted at 40 V, according to the conventional procedure to estimate the full depletion from the $1/C^2$–V curve. The active thickness of the detectors can be calculated from the capacitance value at full depletion and the area of the device. A 45 µm active thickness is obtained for

the measured detectors.
The same measurements are also performed for LGA single pads integrated on Si-Si wafers. The voltage capability of the LGA pads for the lowest implanted dose is in the range of 135 V, as it is shown in Fig. 5. 8. a). Standard p-i-n diodes from the same wafer are also plotted in the aforementioned figure, as well. Fig. 5. 8. b) presents the $1/C^2$–V curve for LGA pads. The foot related to the multiplication layer is higher than the obtained one in the SOI batch. Thus, the expected gain for this new Si-Si LGADs will be higher than the gain of the SOI LGADs. Indeed, it takes few more volts to reach the full depletion of the detector (44 V in Si-Si LGADs). Finally, the active thickness for the Si-Si LGADs is 44 µm, almost the same value as the value obtained in SOI LGADs.

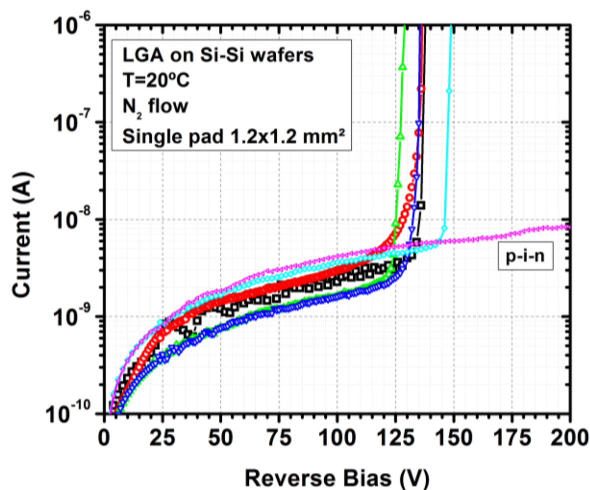


Fig. 5. 8. a) Current as a function of the reverse applied voltage a) and $1/C^2$ versus the reverse applied voltage b) for LGA structures from Run10478.

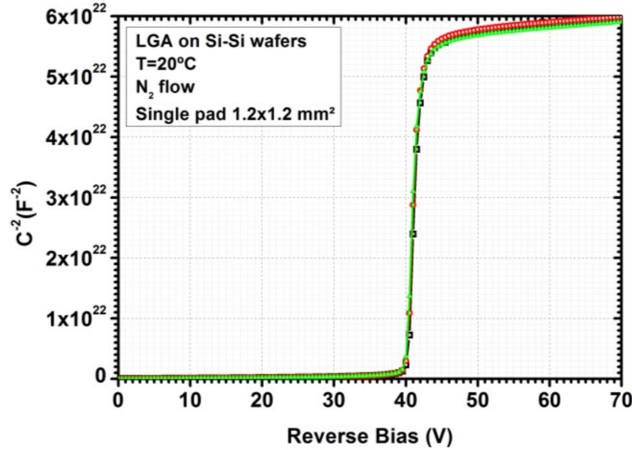


Fig. 5. 8. b) $1/C^2$ versus the reverse applied voltage b) for LGA structures from Run10478.

Another representation of these data is the plot of the current as a function of the depleted depth on the detectors. This representation shows how the current increases during the depletion of the first 5 microns which corresponds to the multiplication layer thickness, as it can be seen in Fig. 5. 9. Once the multiplication layer is depleted, the current barely increases until the detector is full depleted at 45 µm (44 µm) for LGA devices integrated on SOI wafers (Si-Si wafers). The leakage current of p-i-n diodes on SOI and Si-Si wafers is also plotted in the same figure. In this case, the leakage current increase when the depletion region grows.

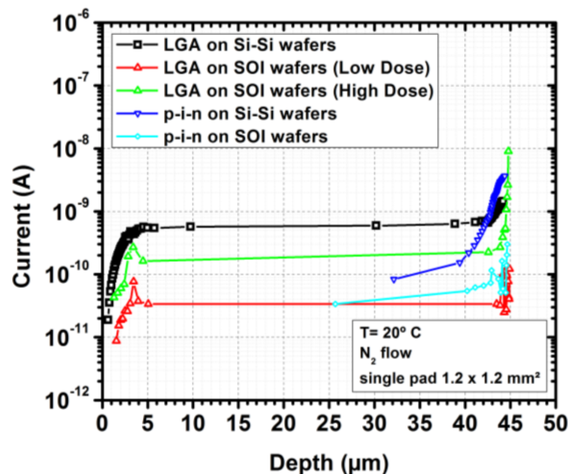


Fig. 5. 9. Current as a function of the depleted depth for LGA structures on Si-Si and SOI wafers.

5.2.1.2. Gain measurements

Charge collection performance of the LGB single pad samples from the SOI batch is evaluated at the Jozef Stefan Institute (JSI) facilities in Ljubljana (Slovenia). Unirradiated detectors were exposed to a ^{90}Sr source with a scintillator placed below the sample. Thus, only the electrons crossing the detector could provide a large enough signal in the photomultiplier to trigger the electronic readout. A detailed description of the setup can be found in [128]. Fig. 5. 10. shows the most probable value of the collected charge on the left axis and the corresponding gain on the right axis as a function of the reverse bias. In the same graph, the simulated gain is also plotted with dashed lines. As it can be seen, gain values between 10 and 50 are achieved for medium and low implantation dose values. LGADs with the highest implantation dose break before reaching a gain of 30. Thus, better timing performance is expected for devices with low and medium doses as a consequence of the higher voltage and gain reached.

MIP measurements on unirradiated LGA single pad detectors integrated on Si-Si wafers are also performed at the Santa Cruz Institute for Particle Physics at UCSC. The experimental setup is the same as the one used for timing measurements. Detailed information about the experimental setup can be found in reference [129]. The measurements are done in a climate chamber with a controlled temperature (20ºC) and dry environment. The gain for LGA detectors from Run10478 is bigger than that for medium dose implantation from Run9088, as it can be seen in the plot of the gain as a function of the reverse voltage in Fig. 5. 11

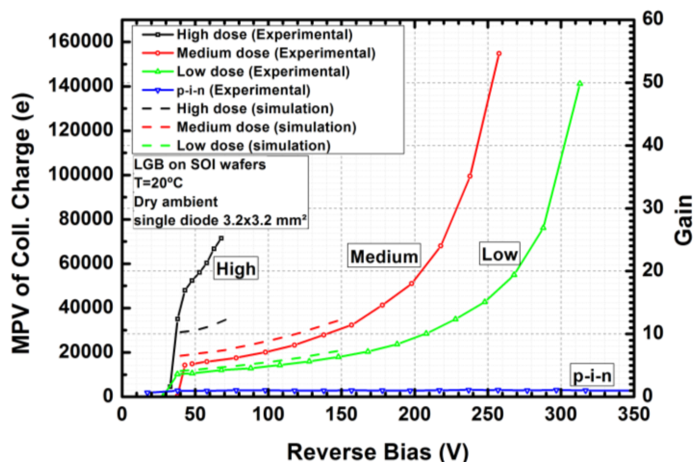


Fig. 5. 10. Plot of the most probable value of the collected charge and gain as a function of the reverse applied voltage to LGB single pads on SOI wafers.

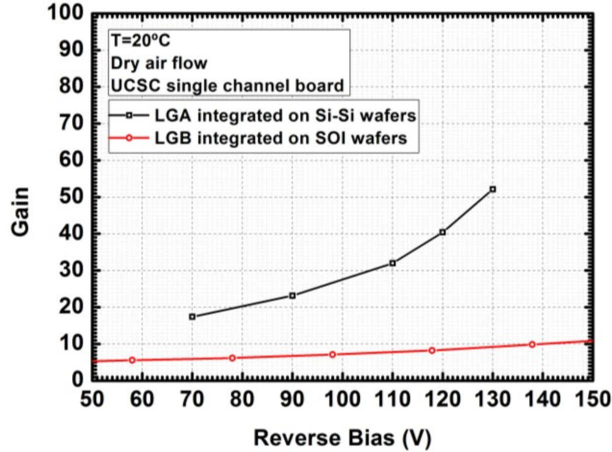


Fig. 5. 11. Gain as a function of the reverse applied bias for LGA single pads on Si-Si wafers.

where the gain of an LGB detector with a medium implantation dose of the multiplication layer from Run9088 is plotted in a red dashed line for comparison.

5.2.1.3. Timing

Timing measurements on LGAD detectors produced on SOI wafers are carried out by different research institutes with different setups, achieving identical time resolution in the range of 30 ps before irradiation [129]–[131].

LGAD detectors integrated on Si-Si bonded wafers have not been tested on beam facilities but first lab timing measurements are done at SCIPP-UCSC laboratory using the ^{90}Sr β-telescope. Si-Si LGA detectors were mounted on UCSC single channel board. More detailed information about the UCSC single channel boards can be found in reference [131]. The ^{90}Sr β-source was placed in the aligning frame inside the climatic chamber just in front of the detector. The trigger is placed just after the detector under test and consists in 50µm thin LGAD on SOI wafer with a time resolution of 35 ps at 20 ºC. The trigger was placed after the detector to make sure that only particles with enough energy crossing through the detector under test and reaching the trigger would be recorded by the scope.

The measurements are performed at 20 ºC with dry air flow. Fig. 5. 12. shows the time resolution of an LGA device from Run10478 as a function of the gain. The time resolution of an LGA detector integrated on SOI wafers is also plotted with a dashed line for comparison purposes. The best time resolution is in the range of 30 ps, which is the same as the one obtained in SOI LGAD counterparts from Run9088.

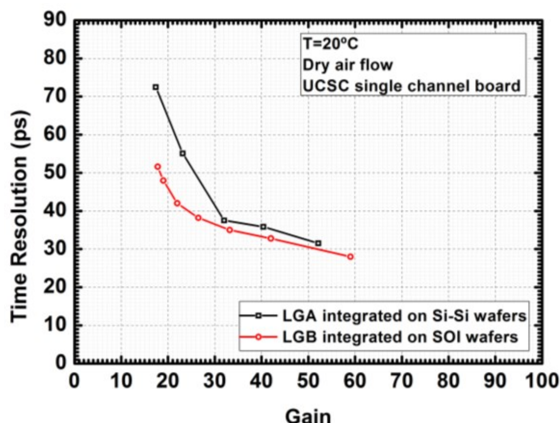


Fig. 5. 12. Time resolution as a function of the gain for LGA single pads on Si-Si and SOI wafers in open symbols and dashed line, respectively.

The time resolution of the detectors integrated on Si-Si wafers for gain values of the gain between 10 and 30 is higher than the obtained time resolution for the detectors on SOI wafers at the same gain range. Therefore the distribution of the most probable value of the pulse maximum value for a detector from Run10478 at gain values lower than 30 is wider than the same one for devices from Run9088. This difference decreases as the gain value increases, becoming minimum at gain values higher than 30.

5.2.2. Irradiated detectors

The production of the new batch, called Run10478, finished on October 2017 and there was no time to prepare the irradiation campaign of the samples and the posterior study of the irradiated samples. Therefore, only the electrical, gain ant timing measurements on LGA and LGB detectors from Run9088 is studied after neutron irradiation of the samples at Ljubljana TRIGA nuclear reactor [118]. The detectors are irradiated with neutrons at fluences ranging from $5 \cdot 10^{13}$ up to $2 \cdot 10^{15}$ n_{eq}/cm^2. Table 5. 1. presents the name, type and neutron fluence of each device under study. In the next sections, the characterization of these samples are presented.

Table 5. 1. Neutron irradiated devices from Run9088

Device name	Dose	Type	Area (mm²)	Fluence(n_{eq}/cm^2)
W8_LGA31	Medium	LGA	1.2×1.2	$5 \cdot 10^{13}$
W8_LGA33	Medium	LGA	1.2×1.2	$1 \cdot 10^{14}$
W7_LGA11P	p-i-n	LGA	1.2×1.2	$1 \cdot 10^{14}$
W3_LGB71	Low	LGB	3.2×3.2	$1 \cdot 10^{14}$
W5_LGB52	Medium	LGB	3.2×3.2	$1 \cdot 10^{14}$
W5_LGB72P	p-i-n	LGB	3.2×3.2	$1 \cdot 10^{14}$
W8_LGA34	Medium	LGA	1.2×1.2	$5 \cdot 10^{14}$
W4_LGA11P	p-i-n	LGA	1.2×1.2	$5 \cdot 10^{14}$
W8_LGA51	Medium	LGA	1.2×1.2	$1 \cdot 10^{15}$
W12_LGA21P	p-i-n	LGA	1.2×1.2	$1 \cdot 10^{15}$
W3_LGB74	Low	LGB	3.2×3.2	$1 \cdot 10^{15}$
W5_LGB61	Medium	LGA	3.2×3.2	$1 \cdot 10^{15}$
W5_LGB72P	p-i-n	LGB	3.2×3.2	$1 \cdot 10^{15}$
W9_LGA34	Medium	LGA	1.2×1.2	$2 \cdot 10^{15}$
W9_LGA21P	p-i-n	LGA	1.2x1.2	$2 \cdot 10^{15}$

5.2.2.1. Electrical characteristics

After the neutron irradiation, the detectors are annealed at 60ºC during 80 minutes because it is the annealing usually used for the HEP community, as aforementioned in section 2.6.3. Then, the detectors are kept in the freezer to stop annealing and avoid their reverse annealing.

The detectors are measured at the IMB-CNM's laboratory. The detailed information about the setup is presented in Appendix B. As mentioned in section 2.6.2.1, the leakage current after irradiaiton increases with the fluence. In order to reduce the leakage current and avoid the high current and noise, the detectors are measured at -20 ºC.

The current measurement as a function of reverse applied voltage is performed on irradiated LGA detectors integrated on SOI wafers in a controlled ambient (N_2 flow) and temperature (-20 ºC). The detectors are irradiated to $5 \cdot 10^{13}$, $1 \cdot 10^{14}$, $5 \cdot 10^{14}$, $1 \cdot 10^{15}$ and $2 \cdot 10^{15}$. Fig. 5. 13. presents the current as a function of the reverse applied voltage and the fluence. The breakdown voltage increases with the fluence. The leakage current barely grows with the fluence for LGAD detectors due to the decrease of gain with the fluence, while p-i-n diodes show more than one order of magnitude increase on the leakage current, as shown in Fig. 5. 14. This increase on the leakage current is proportional to the fluence for p-i-n diodes, as discussed in section 2.6.2.1 and Eq. 2. 7. Fig. 5. 15 presents the leakage current increase as a function of the fluence. The current damage rate is obtained from the slope of the linear fit of data.

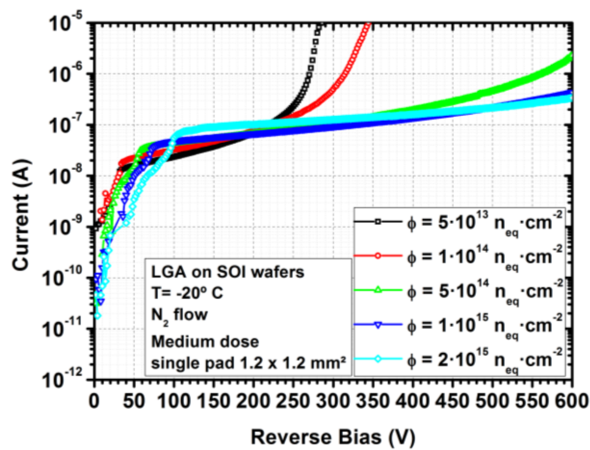


Fig. 5. 13. Current as a function of the reverse applied bias for irradiated LGA detectors.

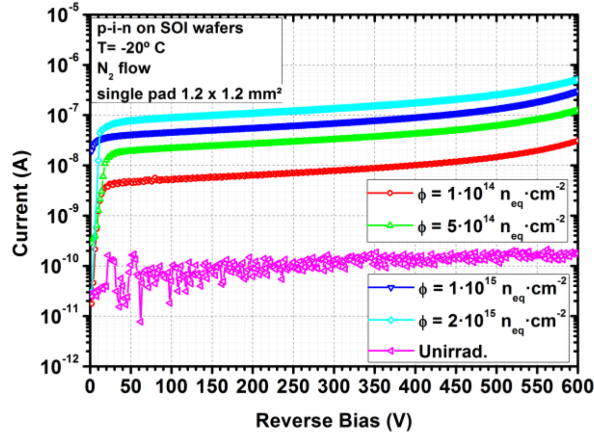


Fig. 5. 14. Current as a function of the reverse applied bias for irradiated p-i-n diodes.

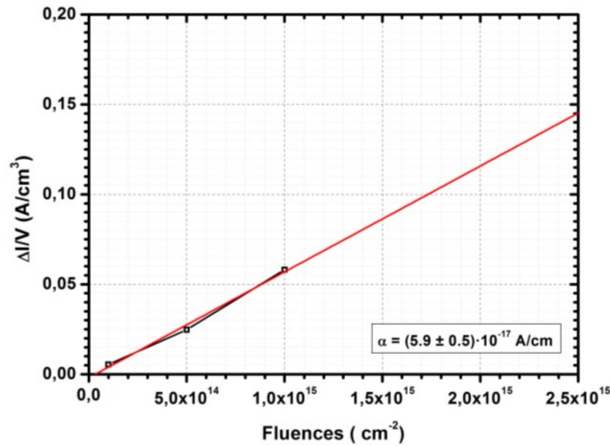


Fig. 5. 15. Lineal fit of the bulk current increase on irradiated detectors as a function of the neutron equivalent fluence.

Once the leakage current is measured, the capacitance measurement is also performed at the IMB-CNM's laboratory. It is well known that the capacitance of irradiated diodes strongly depends on the frequency and the temperature due to the presence of deep traps [132]–[135]. The capacitance dependence on the frequency at a fixed temperature is assumed as a consequence of the less effectively respond of the reaction time of deep traps to high frequency AC signals. Therefore, a study of the effect of the AC frequency on the capacitance measurement is performed to obtain the optimum frequency of the pulse for the measurement [133] [132], [133]. The measurement is performed with AC signal amplitude of 500 mV and different frequencies. These range from 100 up to 1000 Hz. These study is performed on the LGA structures from Run9088 with a medium dose implantation

of the multiplication layer, which is irradiated up to $5 \cdot 10^{14}$ n_{eq}/cm^2. For irradiated silicon detectors, the CV dependence is not described by $1/V^{1/2}$ as for non-irradiated ones. In order to see if there is any power dependence of the capacitance on the applied voltage, the log(C)-log(V) representation of the capacitance data is depicted for these purpose. Fig. 5. 16. presents the log-log graph of the capacitance as a function of the applied voltage for different frequencies. The CV characteristics of irradiated silicon detectors become flatter with increasing frequency, as expected.

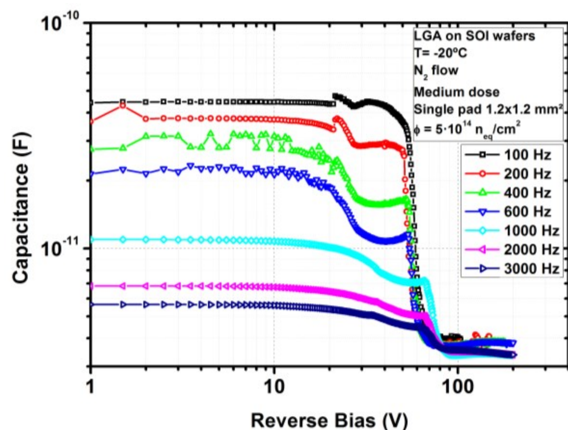
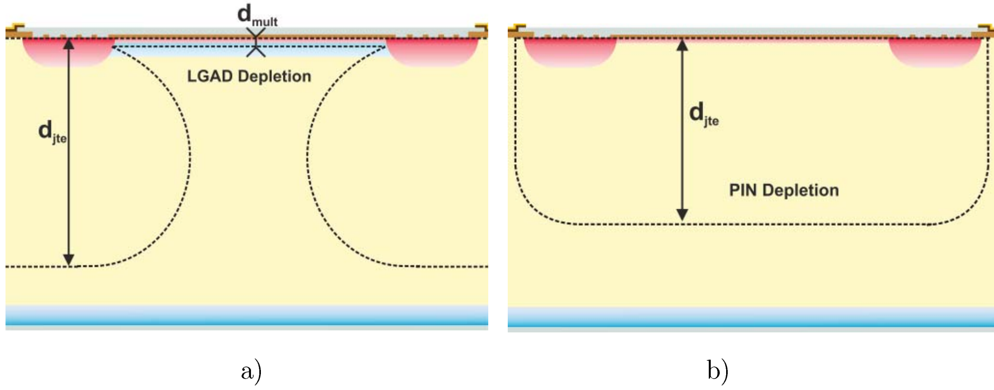


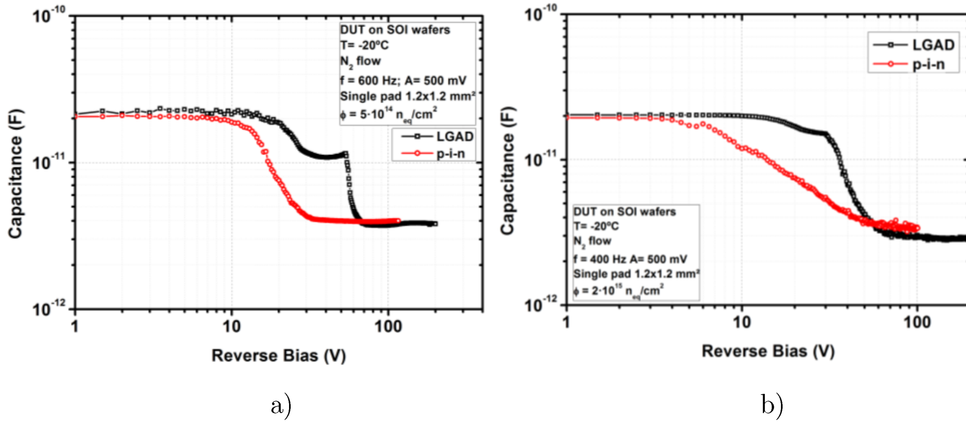
Fig. 5. 16. Log-log plot of the capacitance as a function of the reverse applied voltage and the AC signal frequency for a detector irradiated to ϕ_{neq}=$5 \cdot 10^{14}$ n_{eq}/cm^2.

In the example, the capacitance starts decreasing at 10 V. Afterwards it remains constant from 30 V to 60 V where it decreases until reach the full depletion at 70 V. When the frequency is increased, the constant part of the curve exhibits a peak at 60 V. At a first glance, it was thought that the constant part of the C-V curve is due to the difference between depletion of the JTE and the multiplication layer. The JTE of an LGAD depletes as fast as a p-i-n diode meanwhile the multiplication layer depletes slower than the JTE, as it can be seen in the comparison between LGADs and p-i-ns in Fig. 5. 17. a) and b), respectively. Thus, the slopes in the CV attributed to each region of the LGAD are different. Fig. 5. 18. a) and b) presents the comparison between the capacitance of an LGAD and a p-i-n diode, both are irradiated up to the $5 \cdot 10^{14}$ $n_{eq} \cdot cm^{-2}$ and $2 \cdot 10^{15}$ $n_{eq} \cdot cm^{-2}$, respectively. As inferred in Fig. 5. 18 a), the p-i-n depletes until 30 V, where it becomes full depleted. But for the largest fluence case, the peak in the capacitance of an LGAD moves to 30 V, meanwhile the full depletion of a p-i-n detector increases to 70 V, as shown in Fig. 5. 18. b). Therefore, the depletion of the JTE cannot be responsible of the peak at 30 V.



a) b)

Fig. 5. 17. Representation of an LGAD a) and p-i-n diode b) depletion region.



a) b)

Fig. 5. 18. Log-log plot of the capacitance as a function of the reverse applied voltage for irradiated LGAD and p-i-n diodes to ϕ_{neq}=5 · 10^{14} n_{eq}/cm² a) and ϕ_{neq}=2 · 10^{15} n_{eq}/cm² b).

Thus, the peak must be related to the created traps in the silicon due to radiation. Each trap introduces an energy level in the bandgap diagram, as aforementioned in section 2.6.2. A capacitance simulation of irradiated LGADs is carried out to evaluate the contribution of different traps in the capacitance. The core and periphery region of an LGAD is simulated with Sentaurus TCAD. The new Perugia trap model [136] has been tested with the LGAD structure but neither the frequency dependency, nor the peak are shown in the simulated C-V. The best match between the simulation and the experimental data is the simulation of the three traps level presented in table 5.1. The concentration and cross section of electron and hole traps are taken from reference [135]. The capacitance simulation as a function of the reverse applied voltage and the frequency for an LGAD irradiated up to $5 \cdot 10^{14}$ $n_{eq} \cdot cm^{-2}$ is presented in Fig. 5. 19. a). Although the trap

level due to the B_iO_i complex is introduced in the simulation, the concentration of the B_iO_i must be substrated to the initial active boron concentration of the structure. As it can be seen in Fig. 5. 19 a), a peak in the capacitance appears in the range of 60V. It is found from the simulation that the introduction of the deep donor level produces a peak at 50 V.

Table 5. 2. Simulated Trap levels [135]

Trap	Energy (eV)	σ_n (cm²)	σ_p (cm²)	η
Deep Donor	0.48	$3.3 \cdot 10^{-16}$	$3.99 \cdot 10^{-15}$	0.656
Deep Acceptor	0.525	10^{-14}	10^{-14}	0.28
B_iO_i	0.23	$1.37 \cdot 10^{-16}$	$1.37 \cdot 10^{-15}$	0.012

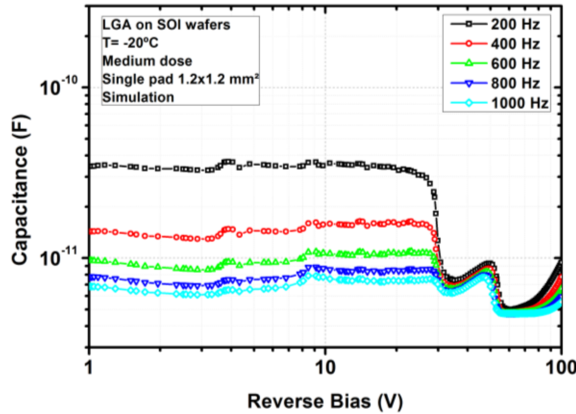


Fig. 5. 19 Log-log plot of the simulated capacitance as a function of the reverse applied voltage and the frequency on an irradiated LGAD up to $\phi_{neq}=5 \cdot 10^{14}$ n_{eq}/cm^2 using the 3 traps model, which is indicated in Table 5. 2.

A frequency study is performed for each irradiated device and the optimum values of the frequency and the amplitude of the AC signal are set to 400 Hz and 500 mV, respectively. All the irradiated devices are measured using the same frequency and amplitude in order to compare the radiation effect on the capacitance performance. Fig. 5. 20 shows the capacitance as a function of the reverse applied voltage for the irradiated devices. As expected, the full depletion voltage of the LGADs increases with increasing fluence and the capacitance for an LGAD irradiated up to $5 \cdot 10^{13}$ $n_{eq} \cdot cm^{-2}$ is equal to the capacitance of unirradiated LGAD. For fluences higher

than $5 \cdot 10^{13}$ $n_{eq} \cdot cm^{-2}$, the bulk starts depleting for voltages lower than 30 V due to the boron removal of the multiplication layer. It also appears a peak in the range of 60 V which decrease at 30 V for the highest fluence. As explained before this peak should be related to the deep donor level introduced by radiation.

The same plot for irradiated p-i-n diodes is presented in Fig. 5. 21. As expected, the full depletion rises as the fluence gets higher due to the increase of the effective concentration of the bulk. As it can be seen, the p-i-n diodes do not present the peak during the depletion. Thus, the deep donor defect is enhanced by the presence of the multiplication layer.

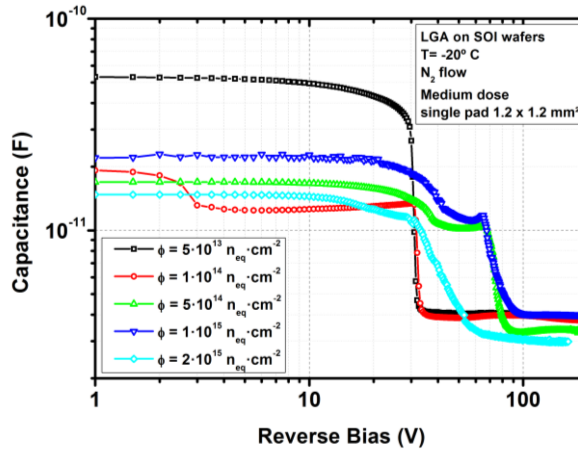


Fig. 5. 20, Log-log plot of the capacitance as a function of the reverse applied voltage and the fluence. The capacitance measurements are taken with a AC signal frequency of 400 Hz and amplitude of 500 mV for all devices.

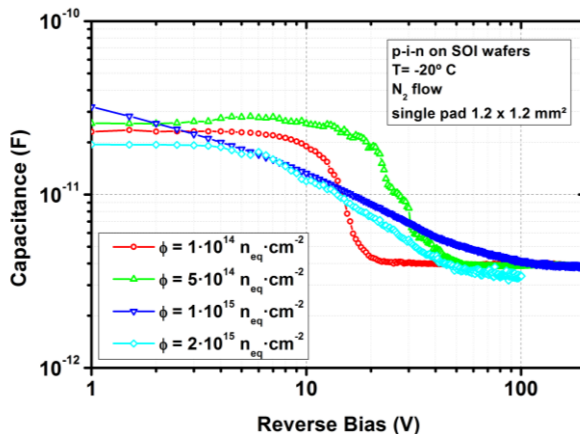


Fig. 5. 21. Log-log plot of the capacitance for irradiated p-i-n diodes as a function of the reverse applied voltage and the fluence. The capacitance measurements are taken with a AC signal frequency of 200 Hz and amplitude of 200 mV for all devices.

5.2.2.2. Gain measurement

The charge collection is performed on irradiated LGB single pad samples from the SOI batch. As stated in section 5.2.1.2, detailed description of the setup can be found in [128]. The measurement is done in a dry ambient and at -10 ºC at the Jozef Stefan Institute with the supervision and help of Dr. G. Kramberger. Fig. 5. 22. shows the most probable value of the collected charge on the left axis and the corresponding gain on the right axis as a function of the reverse bias. The gain decreases significantly with the increasing fluence due to boron removal and the double junction effect [137], [138], as shown in Fig. 5. 22. The effective boron concentration is reduced by neutron irradiation and the gain vanishes for fluences higher than $2 \cdot 10^{15}$ n_{eq}/cm^2. However, the gain vanishes for fluences higher than $2 \cdot 10^{15}$ n_{eq}/cm^2, a restoration of some part of the gain at high bias due to the double junction effect and the increase of the effective space charge concentration has been observed [130].

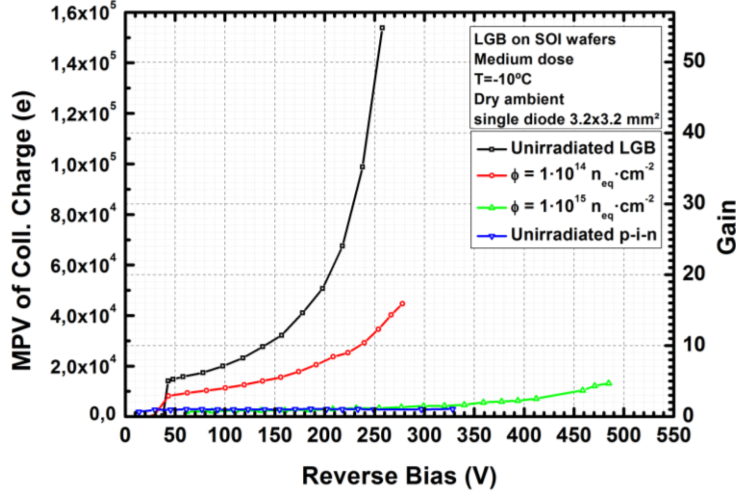


Fig. 5. 22. Plot of the most probable value of the collected charge and gain as a function of the reverse applied voltage for irradiated LGB single pads on SOI wafers.

5.2.2.3. Boron removal rate

A method to study the boron removal in the multiplication layer is the observation of the induced current as a function of the reverse applied voltage, after the front illumination of the detector by red light which has a short penetration depth (~ 7.6 µm) into silicon [37], [40]. The collected charge remains almost zero until the multiplication layer is depleted. Then the charge increases steeply due to the fact that the electrons generated by the red laser are drifted, adquiring enough energy to start the impact ionization. Thus, the steep increase on the collected charge indicates the depletion of the multiplication layer. The measurement is performed TCT setup. The setup is the same as the MIP setup but the ^{90}Sr source is replaced by a red laser which emits pulses with a wave length of 660 nm, a full width at half maximum of 400 ps and a repetition of 500 Hz. Detailed information about the setup can be consulted on references [65], [139].

The measurement is done on irradiated LGB type pads with the medium and low dose implantation. The most probable value of the collected charge as a function of the reverse applied voltage for medium dose implantation is presented in Fig. 5. 23. a). The fit of the charge data to a power function as $Q \propto a \cdot (V_{bias} - V_{md,\phi})^b$ is also plotted in the same figure. The power factor is equal to 0.5, meaning that the space charge grows as $\sqrt{V_{bias}}$. The obtained multiplication layer depletion voltage is plotted as a function of the fluence in Fig. 5. 23. b). The V_{MD} decays as the fluence increases due to the boron removal. The data are fitted to an exponential function with a removal constant equal to $(9.2 \pm 0.4) \cdot 10^{-16}$ cm^2 for medium dose implanted

devices. While the obtained removal constant for low dose implanted devices is equal to $(6.139\pm\ 0.004)\cdot 10^{-16}$ cm^2. Both results are lower than the obtained in reference [139].

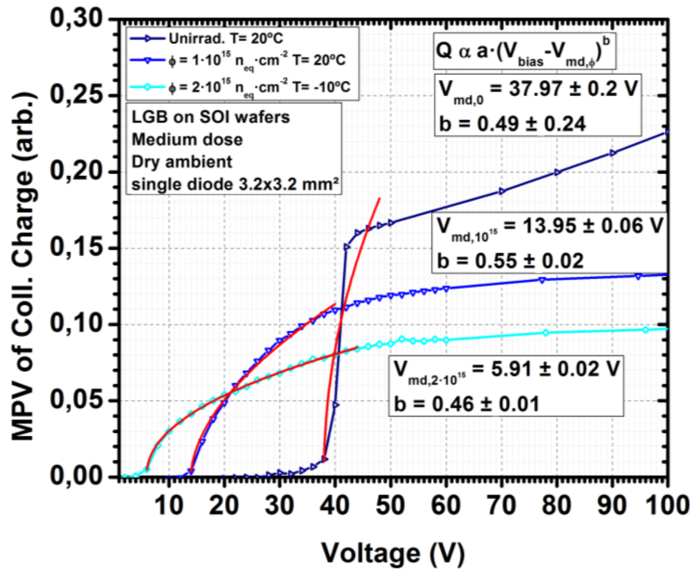


Fig. 5. 23. a) Most probable value of the collected charge as a function of the reverse applied voltage.

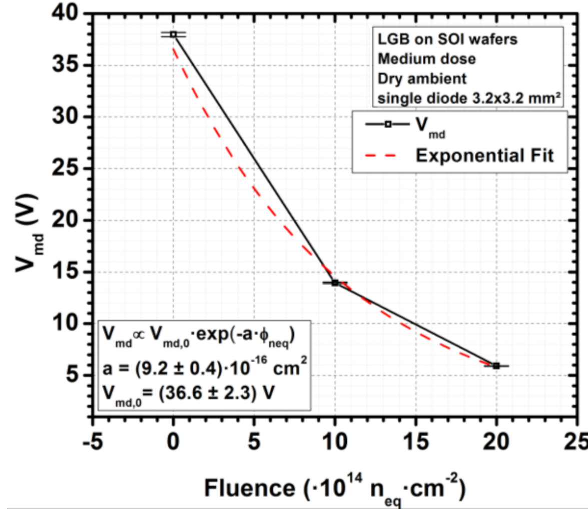


Fig. 5. 23. b) Plot of the multiplication layer depletion voltage as a function of the fluence. The exponential fit of the data is presented in the same graphic in red dashed line.

5.2.2.4. Timing

Timing measurements of irradiated LGAD detectors fabricated on SOI wafers were carried out by the IFAE group in the AFP test beam during summer 2016 at the H6B beam line of the CERN-SPS North Area with 120 GeV pions [130], [140]. The measurements are performed on two unirradiated LGADs which are implanted with the low dose (low, unirr, L1 and L2), two unirradiated LGADs which are implanted with the medium dose (Med, unirr, L1 and L2), two LGADs which are irradiated with neutrons up to $3 \cdot 10^{14}$ $n_{eq} \cdot cm^{-2}$ and implanted with the medium dose (Med, 3e14, L1 and L2) and two LGADs which are irradiated with neutrons up to 10^{15} $n_{eq} \cdot cm^{-2}$ and implanted with the medium dose (Med, 1e15, L1 and L2). All LGADs are LGA type pads, which are mounted on Printed Circuit Boards (PCB), as it can be seen in Fig. 5. 24, where a magnification of the PCB is presented. The voltage is applied on the backside of the detectors while the front side pad is grounded and the guard ring is left floating. The pad is connected to an amplifier and the signal is recorded by an oscilloscope. Two Silicon Photomultipliers (SiPM) are also mounted on the stage just behind the LGADs in order to use them as triggers, as it is shown in Fig. 5. 24. More detailed explanation of the setup can be found in reference [130], [140]. Different runs are taken during the beam test, where an LGAD or a SiPM are used as a trigger.

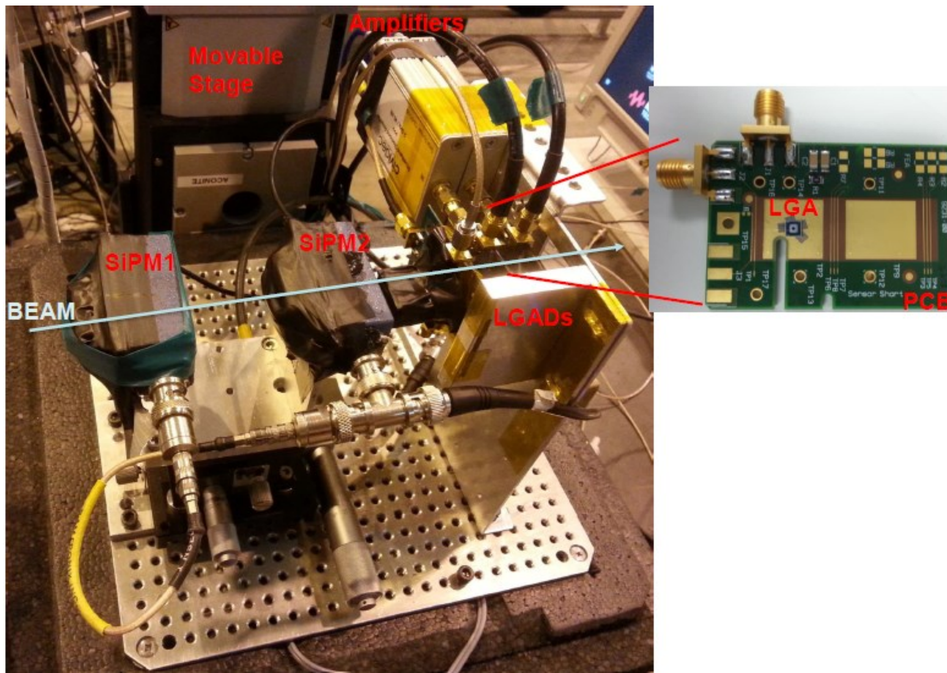


Fig. 5. 24. Beam test setup where the silicon photomultipliers (SiPM1 and SiPM2) and the CIVIDEC C2 TCT amplifiers are indicated. A magnification of the PCB is also presented in the figure. Picture taken from reference [130].

10,000 events are recorded for each run. Since no significant difference on the trigger channel was found, the data are recorded triggering on the LGADs. The MPV of the amplitude, charge, gain, rise time, baseline noise and signal-to-noise ratio (S/N) are extracted from the analysis of the recorded waveforms. The amplitude distribution of the recorded waveforms at a fixed reverse applied voltage is fitted to a Landau-Gauss distribution function to extract the MVP of the amplitude at each applied voltage. The charge is calculated integrating the waveforms from -1ns to 4 ns. Then, the gain was determined dividing the obtained charge of an LGAD by the charge of a p-i-n diode with the same size as the LGAD.

Other parameters which are extracted from the signal analysis is the signal-to-noise ratio and the rise time $t_{r,10\text{-}90\%}$. The S/N is determined as the ratio between the MPV of the amplitude and the noise mean square root. Meanwhile, the rise time is taken as the time between the 10% and 90% of the signal amplitude. Afterwards, the jitter is calculated as indicated in Eq. 2. 6, where the t_r is equal to $t_{r,10\text{-}90\%}/0.8$. The rise time and jitter as a function of the reverse applied voltage for unirradiated and irradiated LGADs are presented in Fig. 5. 25 a) and b), respectively. It is worth to point out that irradiated devices show a rise time lower than the rise time of the

unirradiated devices. Additionally, lowest jitter time resolution is obtained with LGADs implanted with the low dose due to the fact that they have higher voltage capability, reaching a higher gain than LGADs implanted with the medium dose. Irradiated device worsen their time resolution due to the noise increase and the corresponding signal-to-noise ratio decrease.

The total time resolution is determined as the standard deviation of the Gaussian fit of the Δt distribution, where Δt is the Time of Arrival (TOA) difference between two devices. The TOA for each device was determined using an offline Constant Fraction Discriminator (CFD) algorithm. As aforementioned in section 2.4.2, this technique minimizes the walk due to amplitude and rise time variations of the signal. Once the TOA was determined for each device the total time resolution is determined. Since the total time resolution is equal to $\sqrt{\sigma_{DUT_1}^2 + \sigma_{DUT_2}^2}$, the LGAD time resolution is equal to the total time resolution divided by $\sqrt{2}$ in the case that the Δt distribution is between two LGADs and it is equal to $\sqrt{\sigma_{total}^2 - \sigma_{SiPM}^2}$ when the Δt distribution is between an LGAD and a SiPM. Fig. 5. 25 c) and d) shows the time resolution for each LGAD as a function of the reverse applied voltage and gain, respectively. The time resolution decreases as the applied voltage and gain increases. As expected, unirradiated LGADs with low implantation dose of the multiplication layer, which reach the lowest jitter resolution, show the lowest time resolution. They have a time resolution of 28 ps at the maximum applied voltage. The same time resolution is obtained for LGADs irradiated up to $3 \cdot 10^{14}$ $n_{eq} \cdot cm^{-2}$, which are measured in a climate chamber at -20 ºC at its maximum applied voltage. On the other hand, the lowest time resolution obtained on LGADs irradiated up to 10^{15} $n_{eq} \cdot cm^{-2}$ is 57 ps. They are measured in the cooling box at -15ºC.

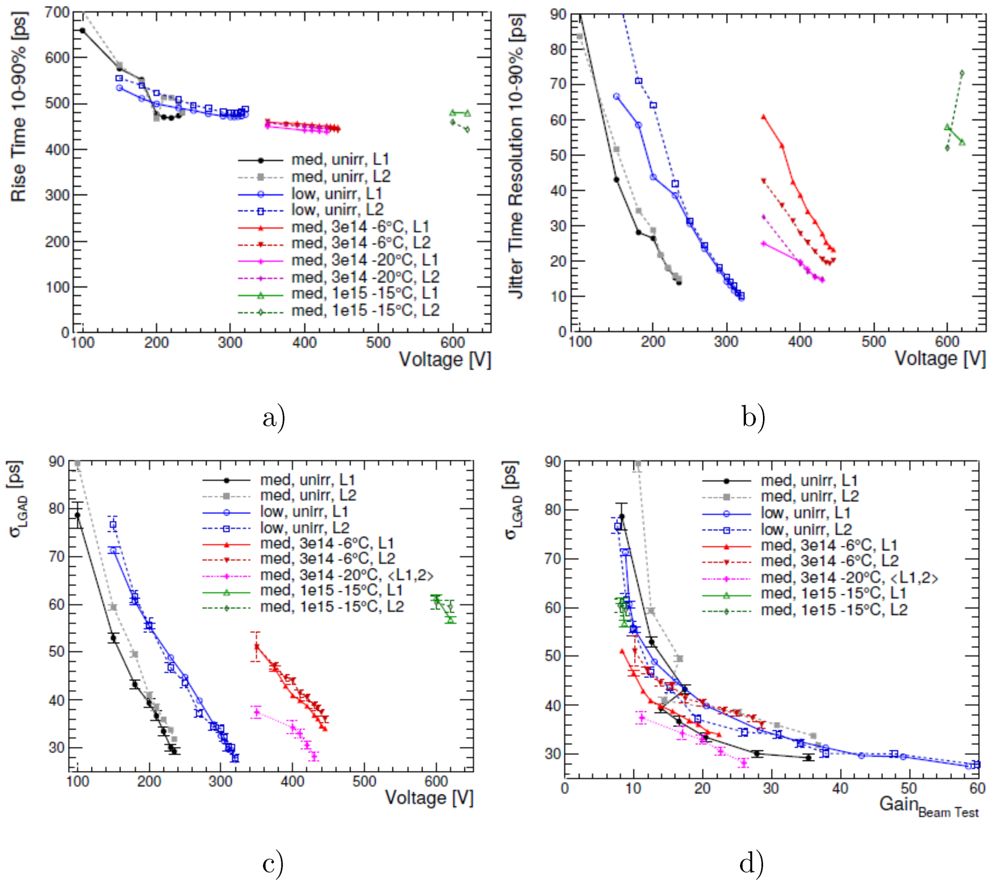
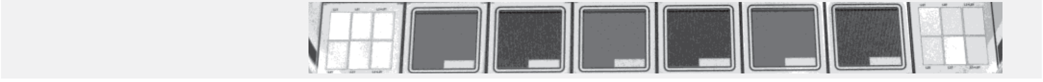


Fig. 5. 25. Rise time and jitter time resolution obtained in the test beam as a function of the reverse applied voltage, a) and b) respectively. Both measurement are performed between the 10% and 90% of the signal amplitude as aforementioned and on irradiated and unirradiated detectors. LGAD time resolution as a function of the reverse applied voltage c) and the gain d). Graphics taken from references [130], [140].

6. i-LGAD

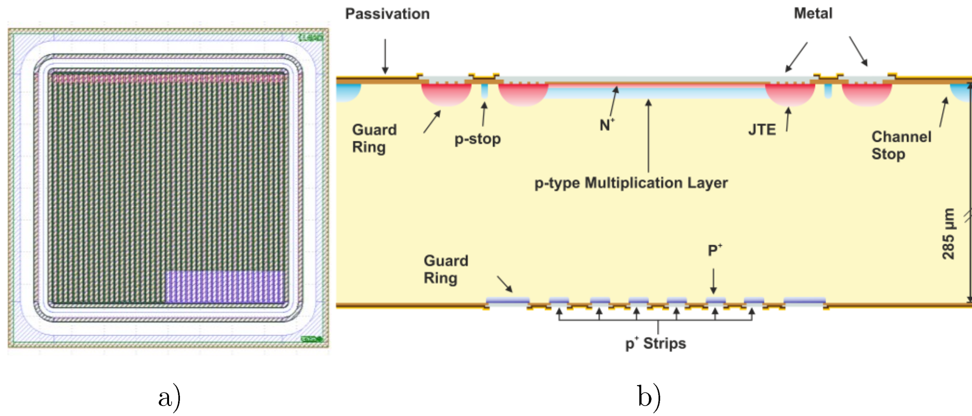


The segmentation of the cathode and the consequent segmentation of the multiplication layer of LGAD microstrips detectors, in order to improve the position sensitivity and decrease the capacitance, presents a non-uniform electric field and gain along the segmented axis, as aforementioned in section 3.2.1.3. An approach to obtain a uniform electric field consists in divide the anode (p^+ electrode) instead of the cathode (n^+ electrode). In this case the multiplication layer is not segmented anymore. This structure is called Inverse Low Gain Avalanche Detectors (i-LGAD)[141], [142]. Thus, an improvement of the fill factor is expected in i-LGAD detectors.

In this chapter, the device structure and the electrical simulations, which were carried out to optimize the device design are presented. Afterwards, the i-LGAD technology process, based on the previous LGAD process, is defined before the presentation of the experimental results.

6.1. i-LGAD design

The i-LGAD structure is based on the conventional LGAD process technology but the segmentation is located at the p^+ ohmic contact, as it was designed and explained in references [141], [143], [144]. Thus, the multiplication diffusion is not segmented and the gain remains constant through the strips or pixels providing a position-sensitive detector with uniform multiplication wherever a particle impinges the detector. Two sizes of microstrips are designed: 32 µm wide strips with a pitch of 80 µm and 112 µm wide strips with a pitch of 160 µm. The layout of the 112 µm wide strips is presented in Fig. 6. 1. a). Fig. 6. 1. b) presents the cross-section of the i-LGAD microstrips detector, where the different dopants and the periphery of the device are clearly detailed. The multiplication junction is protected by a JTE to ensure a high voltage capability. The backside metal is only placed at the edge of the multiplication area to avoid the reflection of the laser while the top side metal is segmented as the implanted p+ microstrips, although a metallization opening is performed at some microstrips in order to be able to carry out TCT measurements illuminating the microstrips with a red laser from the front side.



a) b)

Fig. 6. 1 i-LGAD microstrips device layout a). Cross-section of an i-LGAD device on a HR p-type wafer.

Finally, a p^+ diffusion surrounding the microstrip area is implemented to extract the leakage current generated at the periphery of the device.

6.1.1. Electrical simulation

i-LGAD microstrips detectors are simulated on 300 µm high resistivity p-type silicon substrates to study the gain uniformity and electric field distribution along the segmentation axis.

Only the core region is simulated because the periphery region is equal to the periphery region of a pad detector, which was already simulated. The simulated core region has five microstrips, as shown in Fig. 6. 2. No p-stop between microstrips is implemented in the simulation because the n-type inversion channel under the surface isolates the p-type microstrips. The doping profile used in all simulations is the profile corresponding to the lowest implantation dose of the multiplication layer. The electrical simulation is done grounding the strips and ramping up the voltage of the cathode (electrode n^+) to 1000V. The simulation also takes into account the positive charges in the silicon oxide interface. The concentration of positive charge in the interface is fixed at 10^{11} cm^{-2}.

The plot of the electric field distribution at 1000 V is extracted and presented in Fig. 6. 2. As expected, the maximum electric field is located at the n^+/p junction. Three positions are indicated as Pos1, Pos2 and Pos3 in Fig. 6. 2. They correspond to the three positions where the simulation of a MIP impinging the detector is performed.

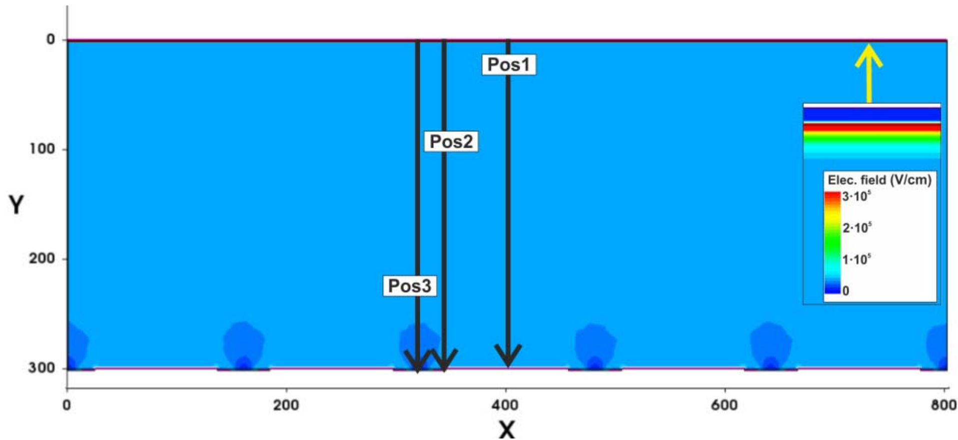
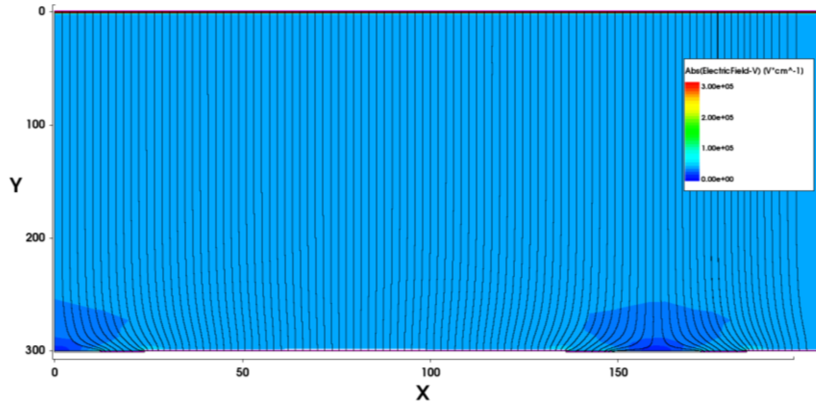


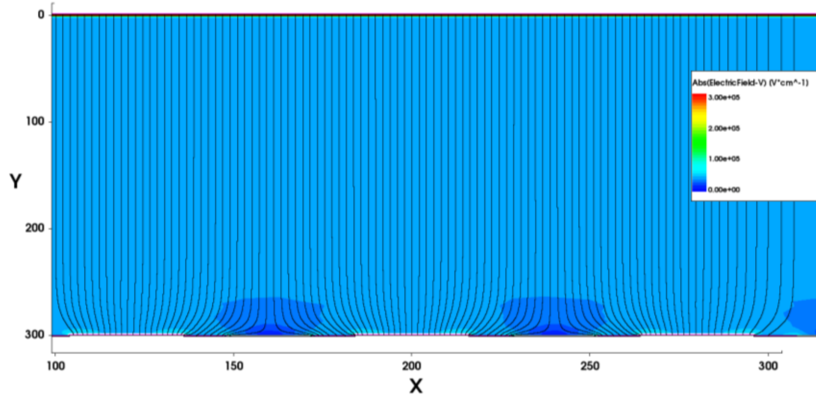
Fig. 6. 2. Electric field distribution of i-LGAD microstrips detectors. The location of the simulated MIP tracks are indicated as MIP1, MIP2 and MIP 3.

The electric field distribution of the detector is studied before the MIP simulation. The electric field distributions at 1000 V for 112 µm and 32 µm wide microstrips are presented in Fig. 6. 3. a) and b), respectively. The electric field lines are plotted on the figures, as well. The comparison of the electric field distributions shows no differences on the electric field distribution for different microstrips widths. Cutlines of the electric field distribution are done at the three Pos positions, which are indicated before. The comparison between electric field cutlines for 112 µm and 32 µm wide strips are presented in Fig. 6. 4. a) and b), respectively. The simulation is extracted at a bias voltage of 1000V. Thus, a uniform gain along the segmentation axis and a fill factor of 1 are expected for i-LGAD microstrips detectors.

The same electrical simulation is performed for 50 µm thin i-LGAD microstrips detectors. The electric field distributions at 200 V for 112 µm and 32 µm wide microstrips are presented in Fig. 6. 5. a) and b), respectively. No appreciable differences between both strips widths are observed. The electric field cutlines of 112 µm and 32 µm wide strips at Pos1, Pos2 and Pos3 positions are presented in Fig. 6. 6. a) and b), respectively. Both simulations are extracted at a reverse applied voltage of 200V. The cutlines of the electric field distribution at the central and edge position (Pos1 and Pos2 positions) for the narrower strips show a slight enhancement of the electric field in the bulk and the back side contact, but these differences are not significant enough to expect differences on the gain.



a)



b)

Fig. 6. 3. Electric field distribution at a reverse applied voltage of 1000V for 112µm a) and 32 µm b) wide strips. The electric field lines are plotted on the figure, as well.

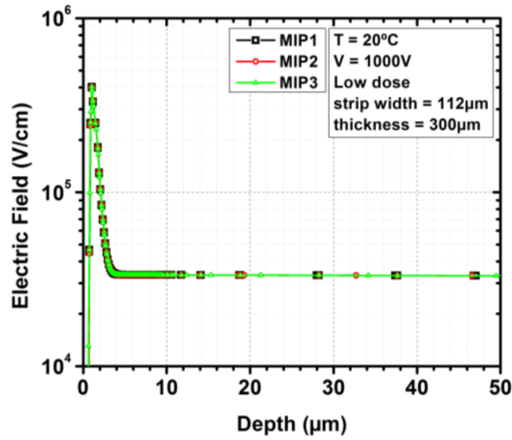


Fig. 6. 4. a) Electric field cutlines for 112µm wide strips. The cutlines are performed at Pos1, Pos2 and Pos3 position.

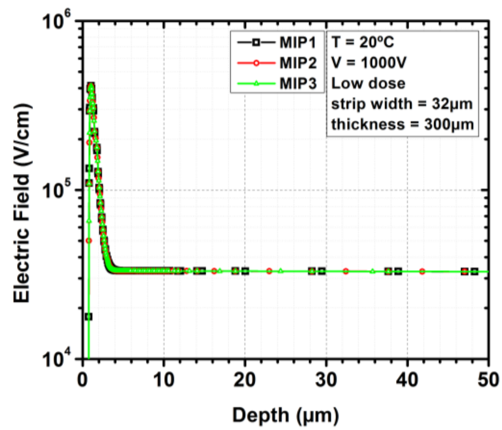
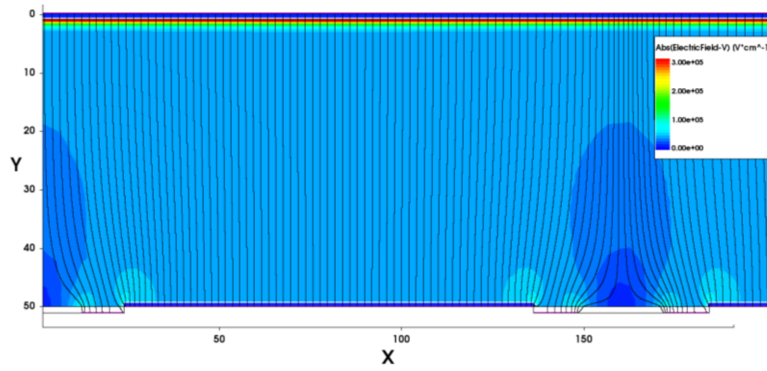
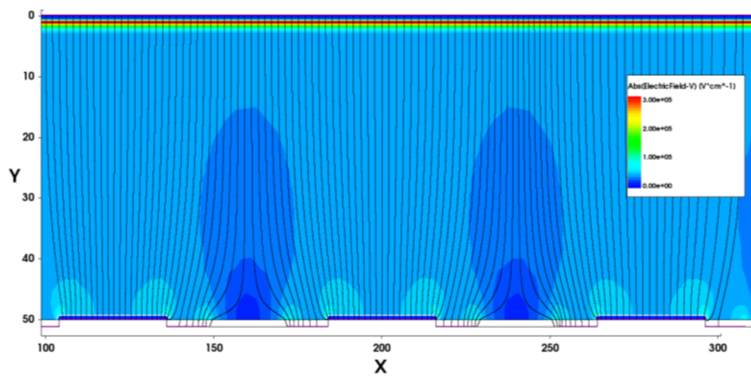


Fig. 6. 4. b) Electric field cutlines for 32µm wide strips. The cutlines are performed at Pos1, Pos2 and Pos3 position.

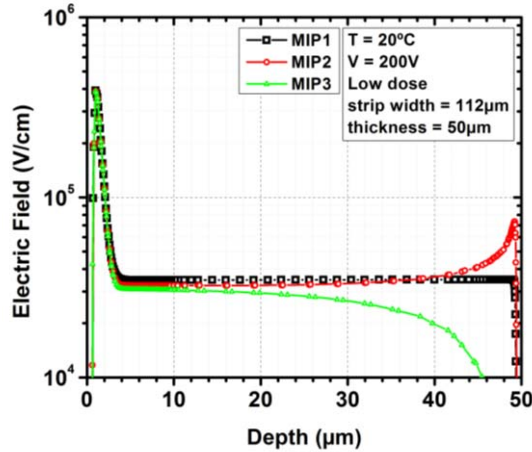


a)

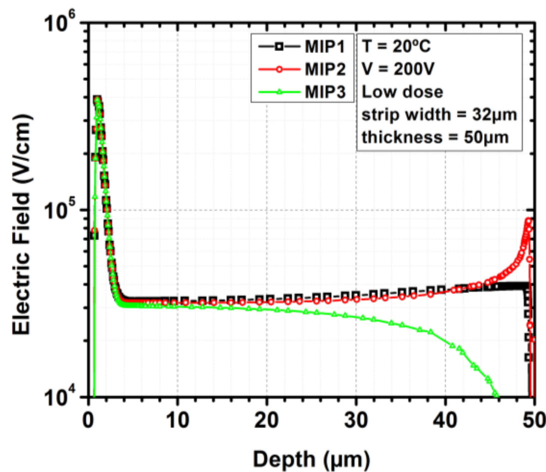


b)

Fig. 6. 5. Electric field distribution at a reverse applied voltage of 200V for 112µm a) and 32 µm b) wide strips. The electric field lines are plotted on the graphic, as well.



a)



b)

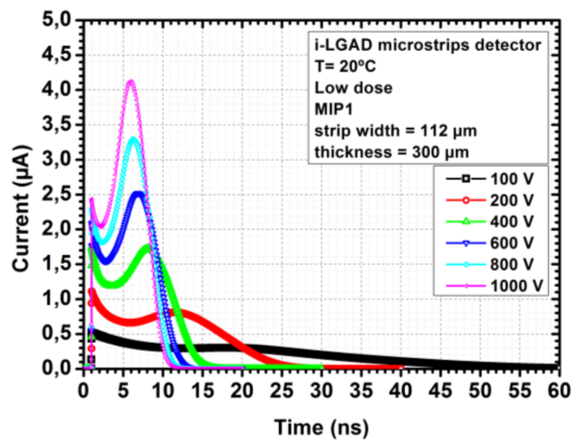
Fig. 6. 6. a) Electric field cutlines of the 50 µm thin i-LGAD simulation at a reverse applied voltage of 200V for 112µm a) and 32 µm b) wide strips.

6.1.2. MIP simulation

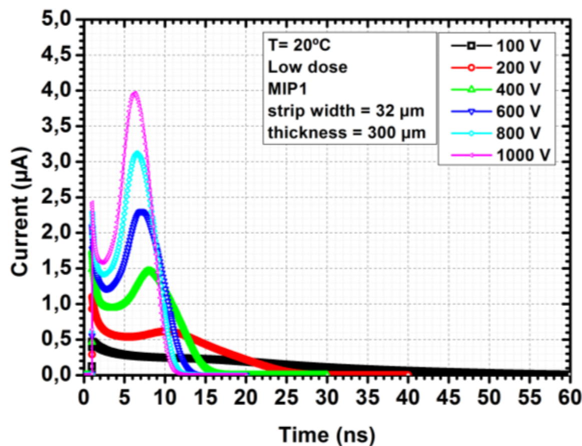
The procedure for gain simulation is the same followed before in section 2.2.1.2. It consists in over-depleting the i-LGAD microstrips detector to a fixed reverse voltage. Afterwards, a MIP is simulated crossing the reverse biased device at a given time (1 ns) and the transient simulation is started. The simulation is repeated at different reverse voltages. The induced current as a function of time for a 300 µm thick i-LGAD microstrips detector with a strip width of 112 µm and 32 µm are plotted in Fig. 6. 7. a) and b), respectively. The pulses for this detector

present two peaks or horns. The first peak is the current induced by the primary electrons and the multiplied electrons, while the second peak is due to the multiplied holes which are drifted to the anode (contact p^+).

The same simulation for 50 µm thin i-LGAD microstrips detectors with the same geometry is performed. When the thickness of the detector is reduced, the two peaks get closer to each other and a single pulse is observed. The transient simulation for 112 and 32 µm wide i-LGAD microstrips are plotted in Fig. 6. 8. a) and b) respectively. The narrow microstrips have a gain larger than wide microstrips, when the induced currents are compared. This charge enhancement is due to the use of different meshing in the simulation, which define a larger multiplication region and it causes a larger gain.

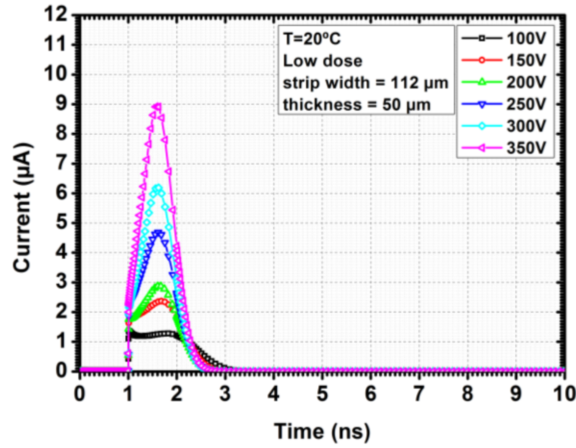


a)

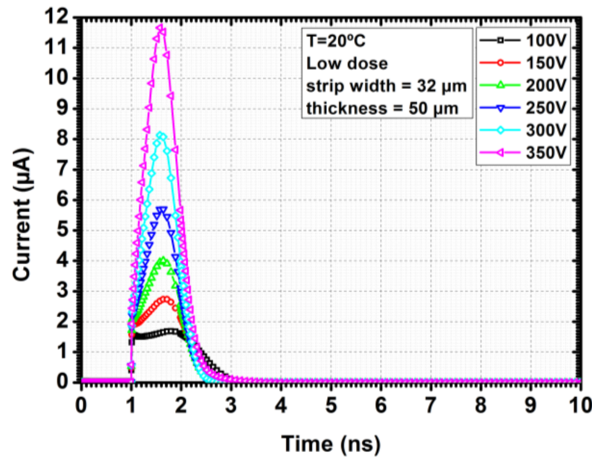


b)

Fig. 6. 7.Transient simulation for a i-LGAD with a thickness of 300 µm and a strip width of 112µm a) and 32 µm b).



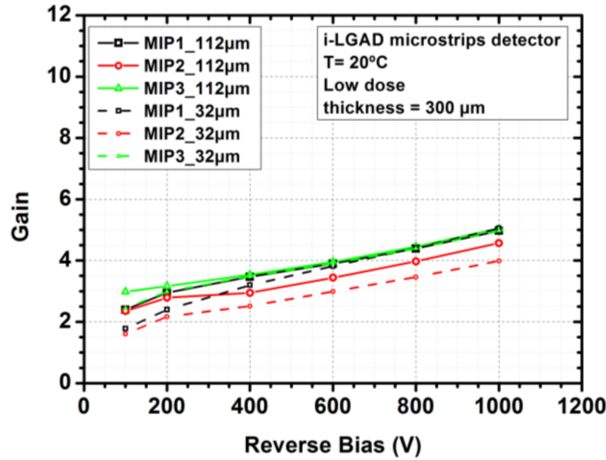
a)



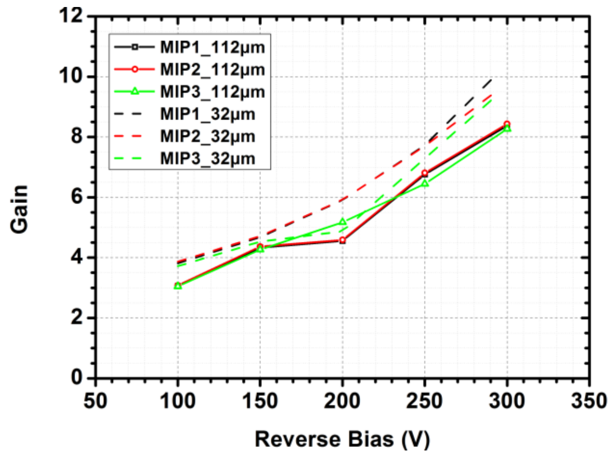
b)

Fig. 6. 8. Transient simulation for a i-LGAD with a thickness of 50 µm and a strip width of 112µm a) and 32 µm b).

The collected charge is calculated integrating the pulses from 0s to 60ns (10ns) for 300 µm (50 µm) thick i-LGAD microstrips detectors. Finally, the gain is calculated as the ration between the collected charge for the i-LGAD and the p-i-n. Fig. 6. 9. a) and b) present the results of the gain simulation as a function of the reverse applied voltage and the strip width for 300 µm and 50 µm thick microstrips, respectively. As it can be seen in both figures, the gain does not depend on the strips width. Thus, the segmentation of the microstrips can be as small as the experiment requires and with a fill factor of 1.



a)



b)

Fig. 6. 9. Simulation of the gain measurement as a function of the applied bias and the strips width for mircrostrips i-LGAD with a thickness of 300 µm a) and 50 µm b).

6.2. i-LGAD technology process

The i-LGAD process is similar to the standard LGAD process, although both sides of the wafer are processed for i-LGADs. Substrates used for i-LGAD are the same substrates used for LGAD process (see chapter 4). The main difference is that the p-stop, JTE, Multiplication, and n^+ contact steps are done on the backside of the wafer, instead of the front side. The batch has 6 wafers with 2 different implantation doses of the multiplication layer, as it is presented in Table 6. 1. P-

stops are also implanted in the backside for two wafers of the batch, namely W1 and W4, in order to study its effects on irradiated detectors. The process starts with the growth of 8000Å field oxide the same way as the LGAD process. Then, the photolithography of the p-stop is defined in the backside of the wafer, while the front side is protected with a resist Fig. 6. 10. a). Once the oxide is dry etched and both resists are stripped b), the backside is protected with a resist and the photolithography of the front side p-stop is defined c). Then, the oxide is dry etched and the resists are stripped. Finally, boron is implanted in both sides of the wafer and impurities are thermally diffused. Afterwards, the front side is protected with the deposit of 2000Å of Si_3N_4 Fig. 6. 10. d). This coating remains on the front side while the JTE and the Multiplication layer are done on the backside, as it is shown in Fig. 6. 11. a) and b) respectively.

Table 6. 1: Implantation doses of boron for the multiplication layer

Wafer	Dose (at./cm^2)	P-Stop on the backside
W1-W3	$1.8 \cdot 10^{13}$	W1
W4-W6	$1.9 \cdot 10^{13}$	W4

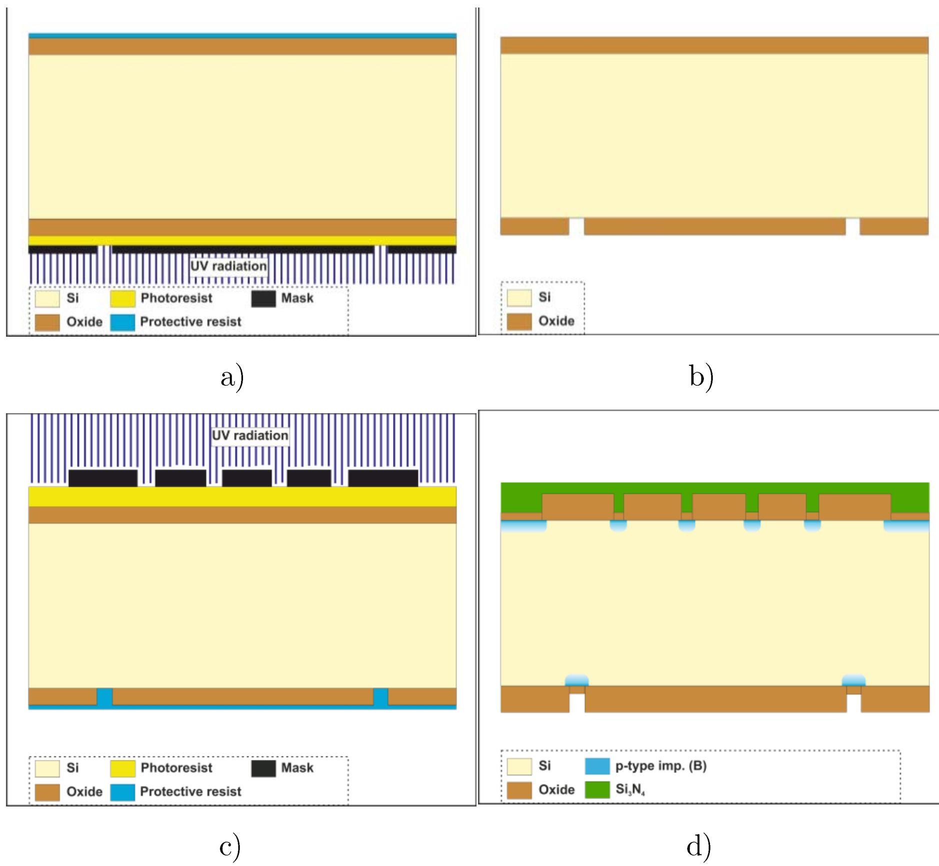


Fig. 6. 10. Photolithography of the backside PStop a), oxide dry etching b), photolithography of the front side mask level PStop c), and boron implantation on both sides and drive-in d).

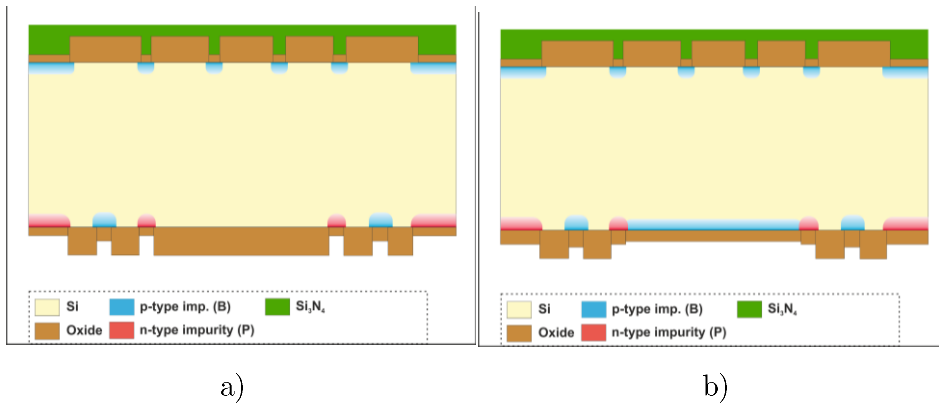


Fig. 6. 11. Photolithography of the backside PStop a), oxide dry etching b), photolithography of the front side mask level PStop c), and boron implantation on both sides and drive-in d).

Once the photolithography of the n$^+$ contact is defined on the backside and the oxide is wet etched, the Si_3N_4 is etched from the front side. Then, the photolithography of the p$^+$ contact is defined in the front side, while the backside is protected with a resist, as represented in Fig. 6. 12. a). Afterwards, the photoresist is developed b), the oxide is wet etched and both resists are stripped c). Finally, the screen oxide is grown, allowing the implantation of boron and phosphorus impurities on the front side and the backside of the wafer, respectively. The implantation is followed by the thermal diffusion of the implanted impurities d).

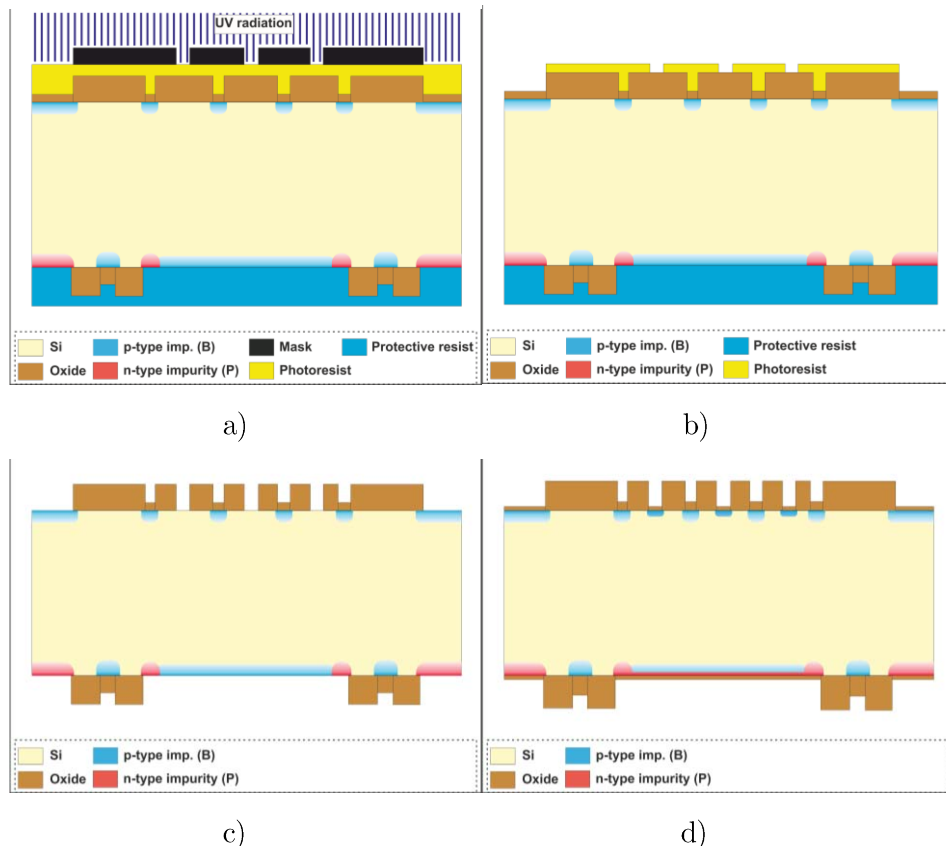


Fig. 6. 12. Photolithography of the front side p$^+$ contact a), photoresist development b), oxide wet etching and resist strip c), boron implantation on the front side, phosphorus implantation on the backside and drive-in d).

Next processes are double side processes. In other words, the same step is performed on the backside of the wafer with the resist protecting the front side and vice versa. Those processes are the metallization and passivation. But, previous to the metallization the contacts are opened. In order to open the contacts, first the photolithography of the backside is performed protecting the front side surface with

a resist Fig. 6. 13. a). Then, the oxide is wet etched and resists are stripped b). The same process is repeated on the front side surface protecting the backside c). Once the contacts are opened, both surfaces are metallized d).

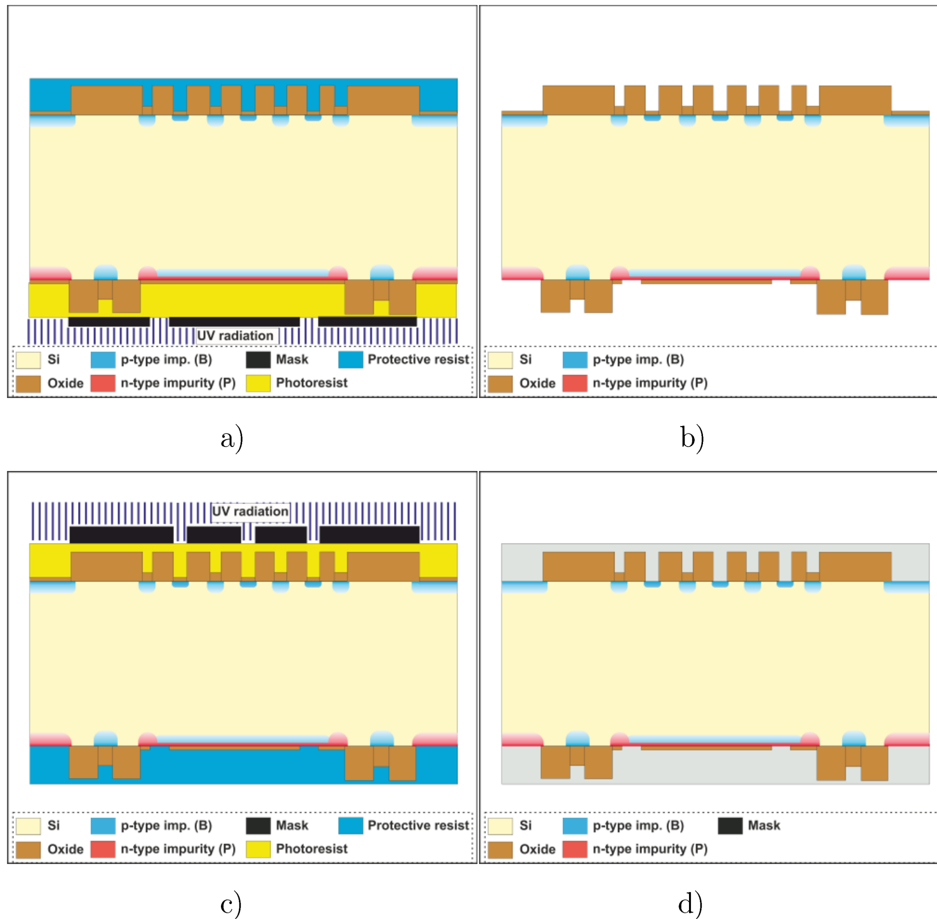


Fig. 6. 13. Photolithography of the backside contact opening a), oxide wet etching of the backside and resists strip b), photolithography of the front side contact opening c), oxide wet etching of the front side and contact metallization d).

After both surfaces are metallized, the photolithography of the backside metal is performed protecting the front side metal with resist Fig. 6. 14. a). Then, the aluminium is wet etched on the backside and resists are stripped from both surfaces b). Afterwards, the photolithography of the front side metal is performed, while the backside is protected c). Finally, the front side aluminium is wet etched and resists are stripped d).

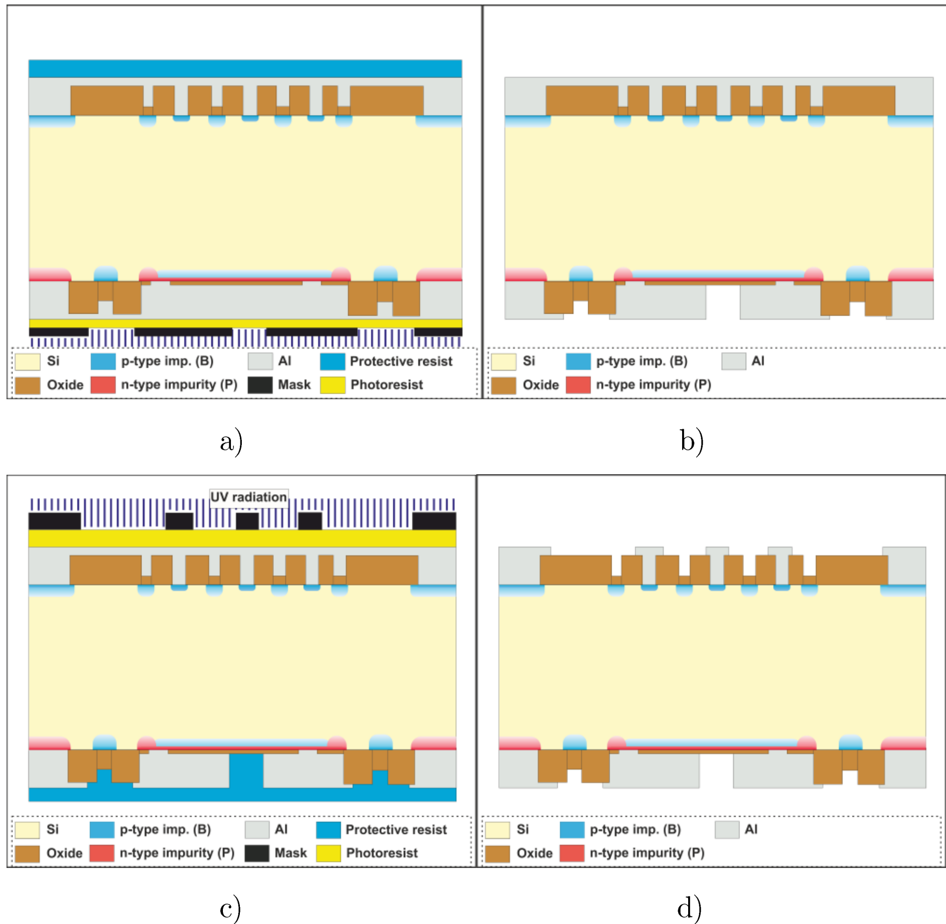


Fig. 6. 14. Photolithography of the backside metal a), Aluminium etching and resist strip b), Photolithography of the front side metal c), Aluminium etching and resist strip d).

Following, both surfaces are passivated with the deposit of 4000Å SiO_2 and 4000Å Si_3N_4 layers, see Fig. 6. 15. a). Afterwards, the photolithography of the backside passivation is defined protecting the front side surface with resist b). Then the passivation is dry etched from the backside electrodes c). The photolithography of the front side passivation is performed, while the backside is protected with resist d). Once the photolithography is performed, the front side passivation is dry etched and the resist is stripped e). Finally, an optical inspection is carried out and the devices are ready to be measured.

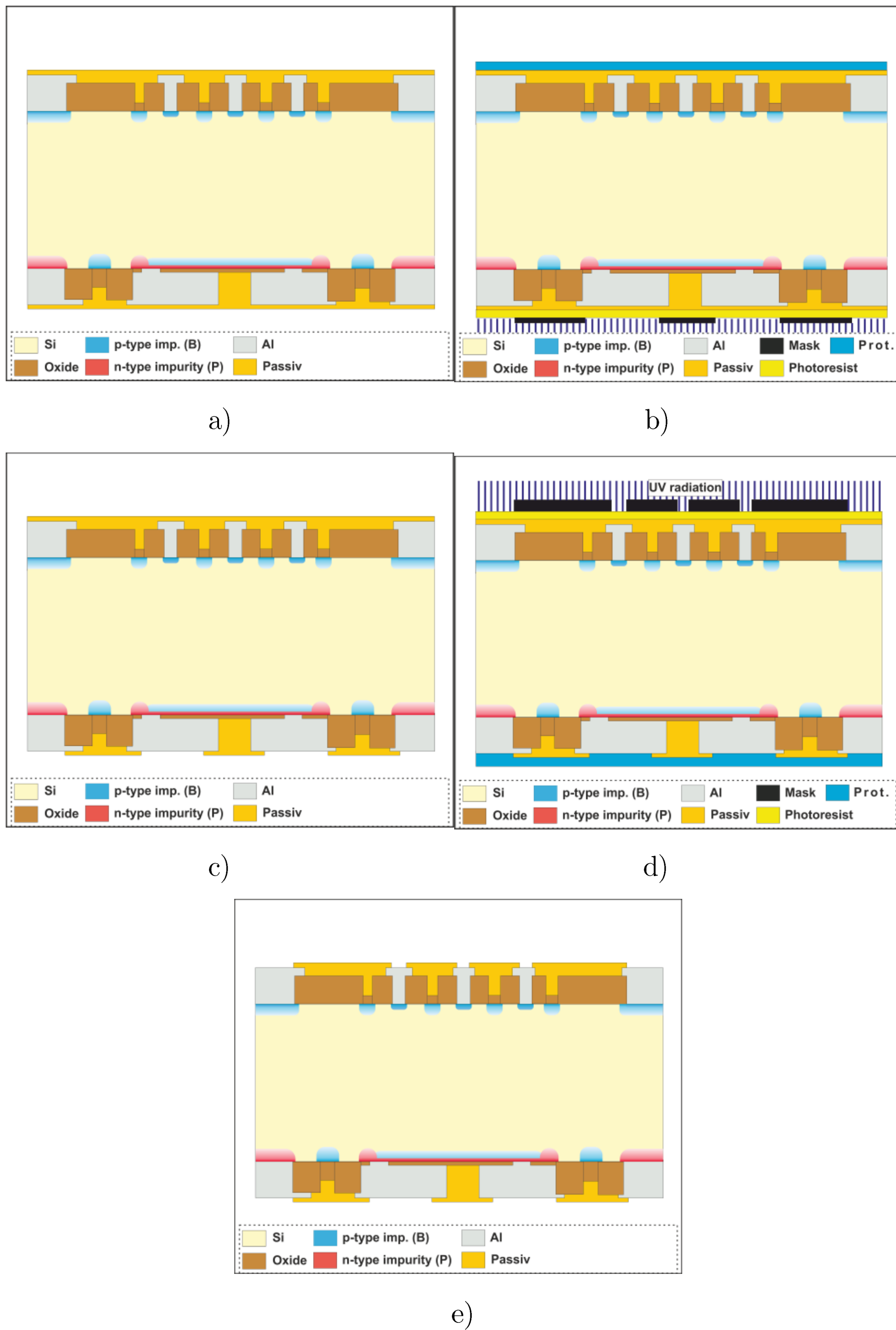


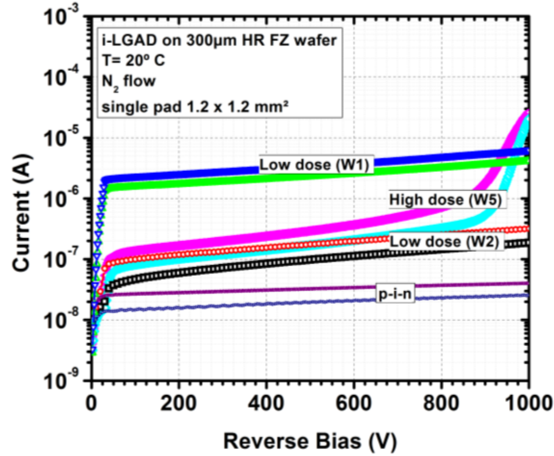
Fig. 6. 15. Deposit of the passivation layer on both surfaces a), photolithography of the backside passivation b), passivation dry etching c), photolithography of the front side passivation d), and passivation dry etching.

6.3. Characterization of unirradiated i-LGAD

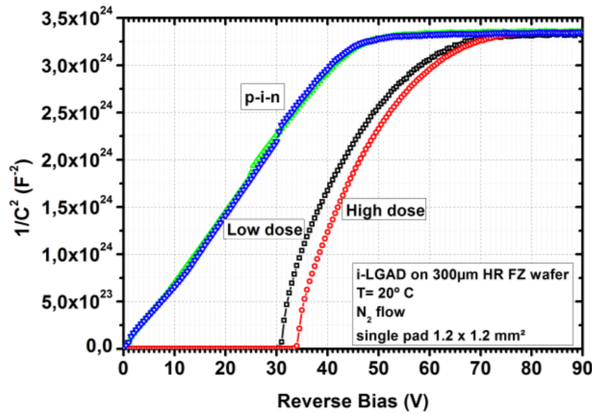
The characterization of i-LGAD microstrips detectors requires the use of customized readout boards as the Alibava system [145]. In the next section a first electrical measurements on i-LGAD pads are presented. Afterwards, the Transient Current Technique (TCT) and timing measurements on i-LGAD microstrips detectors, which are performed in collaboration with the Instituto de Física de Cantabria (IFCA) group, are also presented.

6.3.1. Electrical measurements

The electrical characterization is performed on i-LGAD single pads because the measurement can be done at the IMB-CNM laboratory setup without using a customized readout board to measure them. The i-LGAD single pads are LGADs with a pad area of 1.2×1.2 mm^2 and an active area of 1.3×1.3 mm^2 when the detector is full depleted. A first characterization on i-LGAD single pads have been performed at IMB-CNM laboratory in order to obtain the leakage current, the breakdown voltage and the full depletion voltage of the detectors. The setup used for the measurements is explained in Appendix B. Two different implantation doses were used for the creation of the p-type multiplication layer as aforementioned in section 6.2. They are indicated as Low dose and High dose. The current as a function of the reverse applied voltage of i-LGAD pad detectors from different wafers and different implantation doses of the multiplication layer, are presented in Fig. 6. 16. a). The leakage current for devices with the same implantation dose at the multiplication layer differs from wafer to wafer, as it can be seen in Fig. 6. 16. a), where the leakage current for wafer 1 and wafer 2, which have the same implantation dose of the multiplication layer (Low dose), are plotted. The leakage current of i-LGAD devices from wafer 2 is in the range of 40-200 nA, while detectors from wafer 1 show a leakage current value in the range of 1-5 µA. The voltage capability of devices from both wafers is higher than 1000 V. The difference on the leakage current is due to the fact that wafer 1 has one more process step in the front side than wafer 2, in order to produce the p-stop, as it is explained in section 0. The same behavior is observed between wafer 4 and wafer 5, which are implanted with the same boron dose at the multiplication layer, but they differ in the p-stop implant on the front side. The leakage current for i-LGADs with the highest dose implant in the multiplication layer is in the range of 80-900 nA with a breakdown voltage of 920 V. The same measurement is also performed on p-i-n diodes, which show a leakage current smaller than the obtained one for i-LGADs and a voltage capability higher than 1000 V, as expected.



a)



b)

Fig. 6. 16. Current and $1/C^2$ measurement as a function of the reverse applied voltage, a) and b) respectively. Both measurements are performed on i-LGAD single pad detectors with an area of 1.2x1.2 mm² for two different implantation doses of the multiplication layer.

The plot of $1/C^2$ as a function of the reverse applied bias is presented in Fig. 6. 16. b). As seen in section 5.1.1.1., the depletion of the multiplication layer depends on its own implantation dose. i-LGADs with a low dose implant need 31V in order to deplete the multiplication layer, while i-LGADs with a high dose implant requires a reverse voltage of 34 V to deplete the multiplication layer. After the depletion of the multiplication layer the $1/C^2$ plot should increase linearly with the reverse bias increase, but the curve is not lineal. This is an edge effect which is caused by the JTE. The i-LGADs with low and high dose implants became full depleted at 70 and 75 V, respectively. The capacitance measurements for p-i-n structures from the same batch are also presented in the same plot for comparison.

6.3.2. Charge multiplication

After the first electrical characterization of the detectors, a study of the induced transient current by infrared laser on i-LGAD microstrips detectors are performed at Instituto de Física de Cantabria [146], [147]. The sample under study is an i-LGAD microstrips detector from wafer 1 which is implanted with the lowest dose. P-stop structures between strips are implanted on this wafer. The p-stop acts as a floating strip, which collects the holes. Those collected holes flow from the floating strips to the connected strips. The area of the cathode (n^+ electrode) is 8.2×8.2 mm^2, while the anode consists in 45 microstrips where each one has an area of 0.112×7.152 mm^2. The cathode is connected to the high voltage source, while the strip under study and its first neighbouring strips are grounded. The guard ring is left floating. The strip signal is read out through a channel whose bandwidth is limited by the detector capacitance. The study of the induced current is carried out using a TCT system [71], [148] , where the microstrip under study is illuminated on the front side through the openings on the metallization with an infrared laser (1061 nm), which emulates a MIP crossing the detector. The carriers generated by the laser induce a current in the anode as explained for Ramo's theorem [38], [39]. The transient current waveforms of the DUT at different applied voltages are presented in Fig. 6. 17. The induced current of the i-LGAD microstrips have two peaks. The first peak is dominated by the drift of the primary electrons towards the multiplication layer. The second peak is the induced current by the secondary holes drifted towards the anode contact where the weighting field has its maximum. The secondary holes are generated by impact ionization of the primary electrons crossing the multiplication region. The measurements are done in a controlled ambient and at room temperature. The transient simulations on iLGAD microstrips, which were presented in section 6.1.2, are also plotted in solid lines on the same figure for comparison.

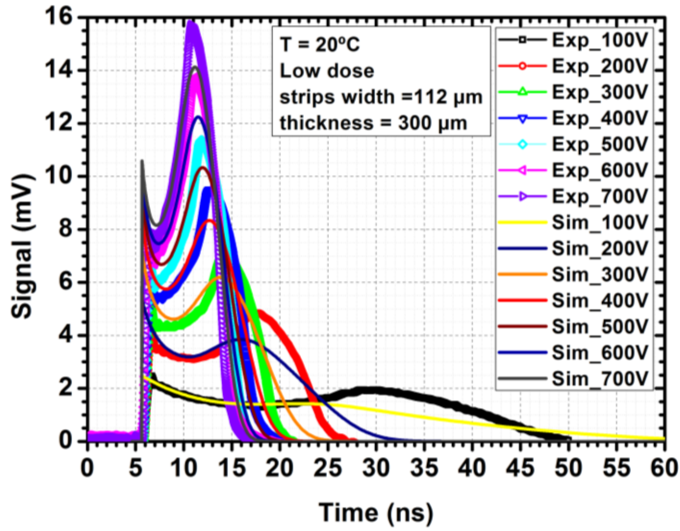


Fig. 6. 17. Transient current waveform corresponding to the carriers injection by IR-laser into an i-LGAD microstrips at different applied voltages. The transient current obtained by simulation are also plotted in the same graph with solid lines.

After this first confirmation of charge multiplication on i-LGAD microstrips a study of the MIP response was carried out by IFCA group in different test beams during 2016 and 2017 at CERN-SPS with 120 GeV pions [149], [150]. A schematic representation of the test beam setup is presented in Fig. 6. 18. The device under test was an i-LGAD microstrips detector with 45 microstrips, where each microstrip has an area of 0.112×7.152 mm^2, an LGAD microstrips detector with the same geometry and thickness as the i-LGAD and a p-i-n microstrips detector

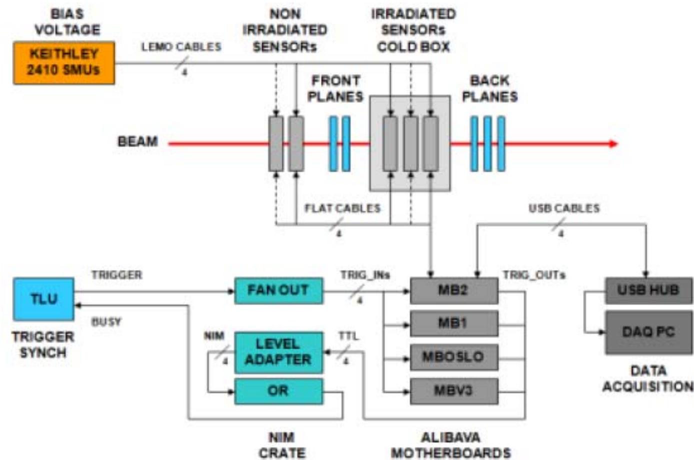
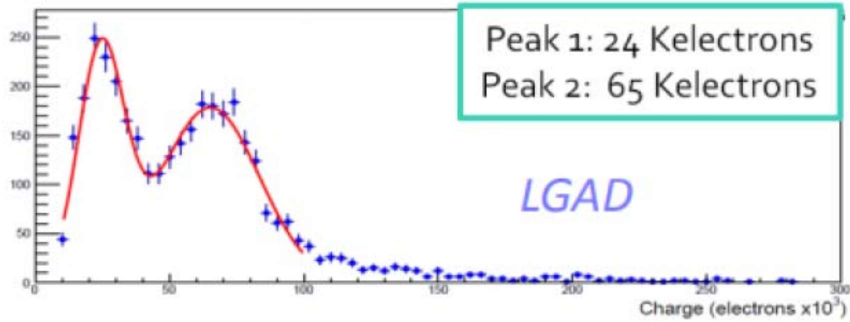
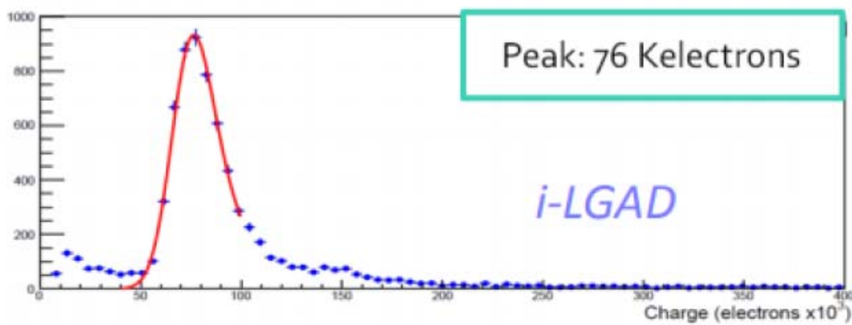


Fig. 6. 18 . Schematic representation of the test beam setup used for the i-LGAD study. Figure taken from reference [150].

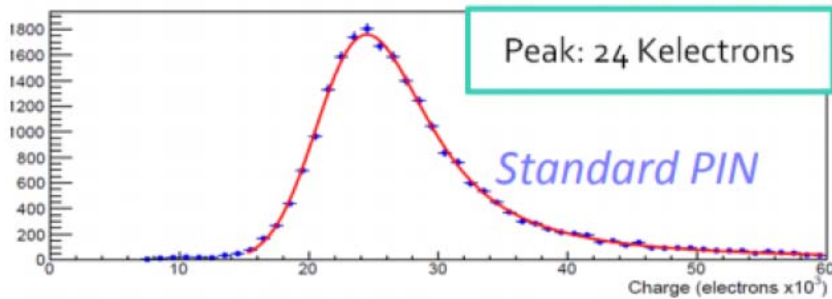
(n on p) with the same strip geometry on the n^{+} electrode. Both detectors have a low dose implantation on the multiplication layer. In order to measure the detectors in a controlled ambient without temperature and humidity variations, as well as, avoiding the noise of ambient light, the detectors were placed inside a cold box. The cathode (n^{+} electrode) was connected to the high bias, while the whole strips were grounded and the guard ring was left floating. The i-LGAD and LGAD microstrips were mounted on Alibava standard daughter board [145]. The two ASIC chips placed on the board can read out up to 256 channels. The readout signals and the external trigger signals are processed by the Alibava motherboard. The coincident readout signals are digitalized by the motherboard. The digitalized signals from an i-LGAD and an LGAD are plotted in Fig. 6. 19. a) and b), respectively. The distributions are fitted with a Landau-Gauss distribution to obtain the MVP of the charge at each bias voltage. The distribution of LGAD microstrips detector shows two peaks. The first peak has a MPV of the charge of 24,000 electrons. This value corresponds to the expected collected charge in a 285µm thick p-i-n detector [36], [151]. The second peak has a MPV of the charge of 65,000 electrons, as it is shown in Fig. 6. 19. a). Therefore, the first peak is due to the drifted electrons, which does not pass through the multiplication layer as explained before in the simulation chapter (section 2.2.1.3). On the other hand, the second peak is caused by the drifted electrons that cross the multiplication layer and start the impact ionization. Fig. 6. 19. c) presents the distribution of a p-i-n microstrips detector for comparison. The MPV of the collected charge is 24,000 electrons, as expected.



a)



b)



c)

Fig. 6. 19 . Distribution of the collected charge for an LGAD a), i-LGAD b) and p-i-n c) microstrips detectors. Figures taken from reference [149], [150].

The gain is calculated as the ratio of the MPV of the charge for an i-LGAD or LGAD microstrips detector to the MPV of the charge for a p-i-n diode. Fig. 6. 20. presents the gain as a function of the reverse bias for i-LGAD and LGAD microstrips detectors. The gain values are similar for both detectors, as well as, the gain values obtained by simulation, which were presented in Fig. 3.16 and Fig. 6. 9.

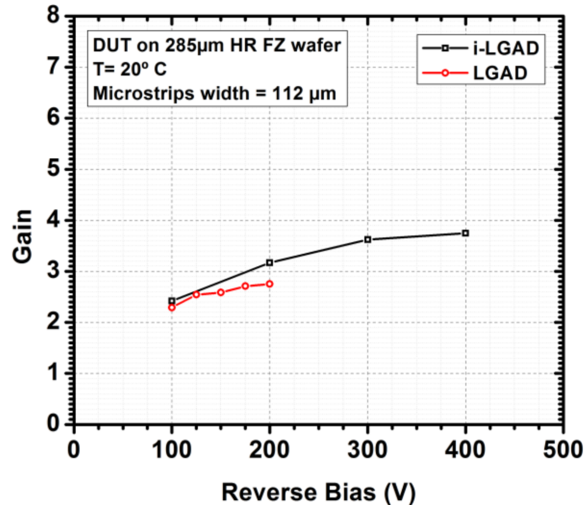


Fig. 6. 20 . Gain as a function of the reverse applied voltage on i-LGAD and LGAD microstrips detectors in black and red open symbols, respectively. Figure taken from references [149], [150]

6.3.3. Timing measurement

The IFCA group has also developed a setup for timing characterization, which was used for measuring the time resolution of i-LGAD microstrips detector [150], [152]. The timing setup consists of a laser diode, a splitter and a combiner, as it can be seen in Fig. 6. 21. a). The laser diode emits a IR laser pulse of 1060nm. Then the IR pulse is split in two branches, one branch send the signal straight to the combiner, the optical fiber on the other branch is set larger than the first branch, in order to introduce a fixed time interval of 52.23 ns between the pulses of the two branches. Afterwards the two branches are combined and the device under test is illuminated with the two pulses. 5000 events are recorded by the oscilloscope. Each recorded waveform from the DUT has two pulses, with a time distance between them of 52.23 ns, as it can be seen in Fig. 6. 21. b). It is worth to mention that the final time resolution is not going to have the Landau fluctuation contribution due to the fact that the device is illuminated with a laser.

In order to calculate the SNR, first of all the average of the 5000 recorded events is computed. Afterwards the noise is estimated as the RMS of the baseline charge between 0 and 20 ns of the waveform. Finally, the signal is calculated as the charge under the transient waveform and the SNR is determined.

Once the SNR is calculated, the time of arrival of the two pulses is computed

emulating a Constant Fraction Discriminator circuit on each recorded pulse. This

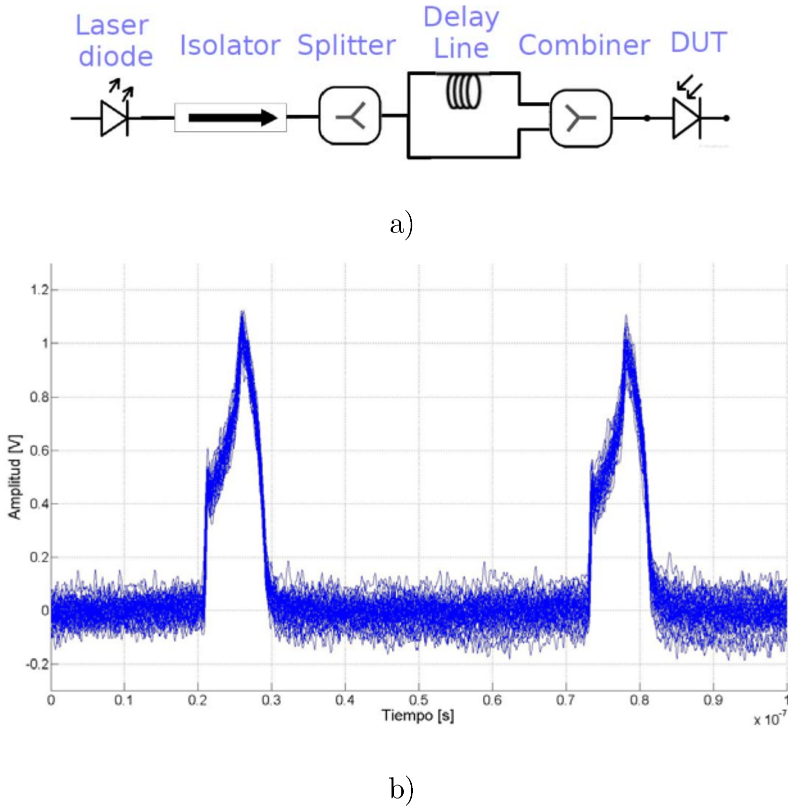


Fig. 6. 21 . Scheme of the timing setup used for the measurement of the time resolution on i-LGAD microstrips detector a). Recorded waveforms from the i-LGAD under test b). Figures taken from references [150], [152].

method is used in order to minimize the contribution in the time resolution of the time walk. Thus, the only contribution that remains from the total time resolution equation (Eq. 1.4) is the jitter.

As aforementioned in section 2.4.2, the CFD sums the delayed signal and the inverted signal, which is attenuated by factor k. Then, the obtained summation is a bipolar signal crossing the zero when the attenuated signal reaches their maximum and the delayed signal is equal to k times their maximum. The zero crossing point is defined as the time of arrival (ToA). Then, the ToA difference (Δt) between the two pulses is computed for each waveform and the Δt distribution is plotted and fitted to a gaussian function, in order to extract the standard deviation or the time resolution of the system ($\sigma_{\Delta t}$). Finally the time resolution of the detector is defined as the division of the time resolution of the system by $\sqrt{2}$, when the measurement is not correlated. The best time resolution is obtained when the constant fraction k

is set to 30%, as it can be seen in Fig. 6. 22, where the time resolution for an i-LGAD microstrips detector as a function of the 1/SNR and the constant fraction

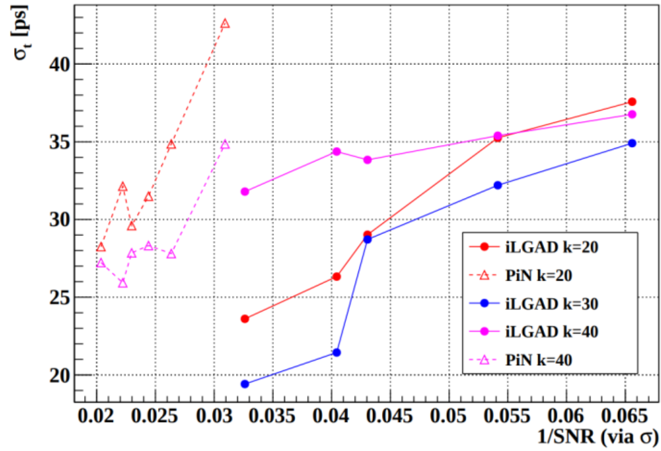


Fig. 6. 22 . Time resolution of an i-LGAD microstrips detector as a function of the SNR and k. The time resolution for p-i-n microstrips detector is plotted in dashed lines for comparison. Figure taken from reference [152].

are plotted in solid lines. The time resolution for p-i-n microstrips detectors are also plotted in dashed lines for comparison. As expected, the time resolution decreases with increasing SNR. A time resolution of 19 ps is achieved for a constant fraction of 30% on i-LGAD microstrips detectors. Meanwhile, the p-i-n microstrips detectors achieve a time resolution of 27 ps for a constant fraction of 40 %. Thus, microstrips detectors show a time resolution better than pad detectors due to the fact that the capacitance is reduced, as a consequence the noise is reduced and the SNR is improved. Additionally, the SNR on i-LGAD microstrips detectors is increased due to the gain.

7. Conclusions and Future Work

The research line of this thesis is the design and characterization of novel pad and microstrips silicon detectors, based on LGAD detectors, in order to fulfil with the time resolution, granularity and expected fluence of the HL-LHC.

Three strategies have been followed in order to improve the radiation hardness and timing performance of LGADs. The first strategy has been the development of thin LGADs. 50 µm thin LGAD pad detectors for the ATLAS Endcap Timing layer (HGTD) and the CT-PPS experiment have been simulated to optimize their design. HGTD is designed without JTE at the junction edge, CT-PPS detectors have JTE instead. The main results obtained from simulations, which were published in [153], are summarized next.

- The LGAD process technology simulation has been calibrated to fit the simulated doping profile with the experimental SIMS. The simulated IV, CV and gain characteristics reproduce the experimental data. The use of the Avalanche model Van Overstraten on the simulation shows the best fit of the IV and CV with the experimental data.
- Once the simulation was calibrated, the HGTD design parameters have been optimized in order to design detectors with the maximum voltage capability. This parameter is the minimum distance between pads. The conservative value, which takes into account the misalignments during the process, has been found to be 33 µm. Using this distance between pads the effective interpad distance, where the gain is not constant, is 104 µm.
- The parameters optimized for the CT-PPS detector are the minimum distance between pads and the minimum distance between the pad and the detector edge. Although 25 µm has been obtained as the minimum distance between pads, which guarantees that the breakdown of the detectors happens in the multiplication layer, 33 µm has been implemented in the

final design, in order to be able to compare the HGTD and CT-PPS devices. The minimum distance between the active area and the sensor edge is 200 µm. This distance is enough to ensure that the space charge does not reach the edge of the sensor. The guard ring in this region has a width of 15 µm. An effective interpad distance of 124 µm has been obtained using these parameters. In other words, the JTE increase the effective distance between pads due to the bending of the electric field lines.

The produced 50 µm thin LGADs have been electrically characterized before and after neutron irradiation. The results are published in [139], [153]. The most important results of 50 µm thin LGADs are presented below.

- The leakage current of unirradiated detectors was measured at 20 ºC in low humidity ambient. The leakage current is in the range of 10 nA. The breakdown voltages for the three different implantation doses of the multiplication layer are summarized in Table 7. 1. The obtained results agree with the expected ones by simulation. The measurement of the capacitance has been also performed. The full depletion voltage and the depletion voltage of the multiplication layer have been obtained from the capacitance. They are presented in Table 7. 1, as well.

Table 7. 1: Electrical characteristics of unirrad. LGADs

Multiplication layer	V_{BD} (V)	V_{FD} (V)	V_{MD} (V)
Low dose	400	35	31
Medium dose	250	37	33
High dose	100	40	38

The detectors, which have a medium dose implant in the multiplication layer, were irradiated with neutrons to 5 different fluences at Ljubljana TRIGA nuclear reactor. Afterwards, the devices were annealed at 60 ªC for 80 minutes. The annealed detectors were measured in dry ambient at -20 ºC. The leakage current ranges from 80 to 300 nA for a fluence up to $2 \cdot 10^{15}$ $n_{eq} \cdot cm^{-2}$. This leakage current barely increases with the fluence due to the gain decrease after irradiation. The breakdown voltages for the different fluences are presented in Table 7. 2. The full depletion voltages for the different fluences are also summarized in the aforementioned table.

Table 7. 2 : Electrical characteristics of irrad. LGADs		
Fluence ($n_{eq} \cdot cm^{-2}$)	**V_{BD} (V)**	**V_{FD} (V)**
$5 \cdot 10^{13}$	270	35
$1 \cdot 10^{14}$	320	35
$5 \cdot 10^{14}$	600	90
$1 \cdot 10^{15}$	> 600	90
$2 \cdot 10^{15}$	> 600	60

50 µm thin LGADs were also characterized with a ^{90}Sr source and a red laser to study the gain and the boron removal of the multiplication layer as a function of the fluence, respectively. The main results are summarized next (published in [139], [153]).

- The gain for unirradiated detectors was measured in dry ambient at 20 ºC. The detectors were exposed to ^{90}Sr source. The gain ranges of the measured detectors for the three implantation doses of the multiplication layer are presented in Table 7. 3.

Table 7. 3: Electrical characteristics of unirrad. LGADs	
Multiplication layer	**Gain**
Low dose	4 - 50
Medium dose	5 - 55
High dose	16 - 27

- The study of the gain was also carried out after the neutron irradiation of detectors from the medium dose implant. The measurement was performed in a controlled ambient at -10 ºC, illuminating the irradiated detectors with a ^{90}Sr source. The obtained gain values are listed in Table 7. 4. The gain decreases after irradiation due to boron

removal but a gain of 6 can be still reached after a fluence up to $1 \cdot 10^{15}$ n_{eq}/cm^2.

Table 7. 4: Electrical characteristics of irrad. LGADs

Fluence ($n_{eq} \cdot cm^{-2}$)	Gain
$1 \cdot 10^{14}$	4 -17
$1 \cdot 10^{15}$	1 - 6

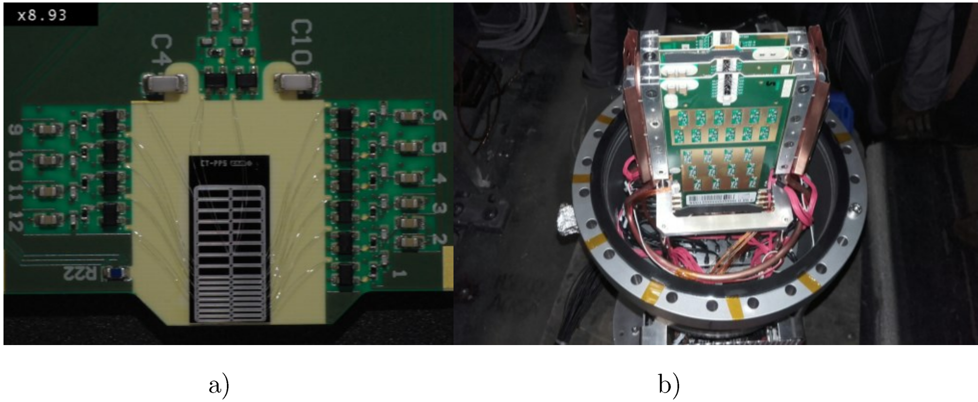
- The boron removal rate was obtained using the TCT technique. The irradiated detectors were illuminated from the front side with a red laser and the collected charge as a function of the reverse bias voltage was studied. Measurements were performed in low humidity ambient at -10 ºC. A constant removal rate of $9.2 \cdot 10^{-16}$ cm^{-2} was obtained from the measured multiplication layer depletion voltage, V_{MD}, at each fluence.

Finally, the time resolution of the produced LGADs was measured using a ^{90}Sr source and in a test beam at CERN (published in [154], [155]). The results are summarized next.

- Unirradiated detectors with medium dose implant in the multiplication layer were measured using the SCIPP ^{90}Sr β-telescope in dry ambient and at 20 ºC. They were also measured in a test beam at CERN-SPS with 120 GeV pions in low humidity ambient at 20 ºC. A time resolution of 28 ps and 27 ps was achieved, respectively.

- The time resolution of irradiated LGADs was measured in a test beam at CERN-SPS with 120 GeV. The measurement was performed at -20 and -15 ºC in a low humidity ambient. A time resolution of 28 ps was found at -20 ºC after an irradiation fluence of $5 \cdot 10^{-14}$ n_{eq}/cm^2. The best time resolution for LGADs irradiated up to $1 \cdot 10^{-15}$ n_{eq}/cm^2 was 56 ps at -15 C.

- CT-PPS devices were installed in the Roman pots of the experiment on April 2017, as it can be seen in Fig. 7. 1 .



a) b)

Fig. 7. 1. Picture of a CT-PPS device mounted on a multichannel board a). 3 layers of the CT-PPS detectors were mounted on their readout boards, inside the Roman Pot b).

The second studied strategy has been the capacitance reduction of the detectors. The design, production and characterization of i-LGAD microstrips detectors have been carried out for that purpose. First of all the detector simulation has been performed. The main simulation results are summarized below (published in [142], [156]).

- The gain for i-LGAD microstrips detectors with the lowest implantation dose ranges from 2 to 5, being uniform along the segmented axis. The simulation does not show any difference between 32 and 112 wide microstrips.

- The transient simulation of i-LGAD microstrips detectors with a thickness of 300 µm shows two peaks. The first peak is the current induced by the primary electrons moving to the n^+ electrode, while the second peak corresponds to the current induced by the secondary holes moving to the p^+ electrode. This double peak pulse merges to one peak waveform for 50 µm thin i-LGAD.

Once i-LGAD microstrips detectors were produced, the electrical measurements were performed on pad detectors with an area of 1.2×1.2 mm^2 and a thickness of 285 µm. The results were published in [142], [156].

- The leakage current was measured as a function of the reverse applied voltage. The measurement was performed at 20 ºC in a low humidity ambient. The leakage current is in the range of 200 nA and 1µA for detectors with the low and medium dose implant, repesctively. Detectors with the same implantation dose in the multiplication region but from different wafers, which were also implanted with the p-stop in the front side, shows an increase on the leakage current from 1 to 7 µA. The breakdown voltages for the two implantation doses are listed in Table 7. 5. The full depletion of the detectors and the depletion of the multiplication layer were obtained from the CV measurement. The results are also summarized in Table 7. 5.

Table 7. 5: Electrical characteristics of unirrad. i-LGADs

Multiplication layer	V_{BD} (V)	V_{FD} (V)	V_{MD} (V)
Low dose	> 1000	70	31
Medium dose	900	75	34

The measurement of the gain on i-LGAD microstrips detectors with the lowest implantation dose was performed by IFCA group in a test beam at the CERN-SPS with 120 GeV pions. They used the Alibava system to measure the collected charge at 20 ºC in a low humidity ambient. The gain ranges from 2 to 4, which agrees with the previous simulation of the gain.

Finally, the timing measurements were performed on i-LGAD microstrips detectors with the lowest implantation dose. The measurements were done using the IFCA setup, which removes the Landau contribution from the time resolution measurement. The measurement was done in a controlled ambient at 20 ºC. A time resolution of 19 ps was achieved for a constant fraction discriminator set to 30 %.

The third studied strategy has been the substitution of boron, as a p-type dopant in the multiplication layer, for gallium. The implantation of a carbon spray on the wafer to reduce the concentration of O_i has been also studied. The simulation of the LGAD process technology for these new impurities has been carried out. The main results are:

- The simulation of the gallium diffusion was calibrated with the SIMS data and the dose and energy of the gallium implantation was obtained by simulation. The temperature and time of the drive-in was also determined by simulation.
- The carbon energy and implantation dose were determined using the SPROCESS tool.
- Both processes were implemented on 285µm thick wafers at the IMB-CNM's clean room facility. The produced LGAD detectors with gallium and carbon are under study.

Thus, two of the three studied strategies to improve the time resolution performance of the detectors before and after irradiation, the reduction of the detectors thickness and the capacitance decrease, demonstrate their effectivity before and after neutron irradiation to fluences of $3 \cdot 10^{14}$ n_{eq}/cm^2. The detectors achieve a time resolution lower than the required one in the HL-LHC (30 ps). It is clear that more studies have to be done in order to improve the radiation hardness of the detectors. The future work to improve the detectors is summarized below.

- Design and production of 30 µm thin HGTD and CT-PPS detectors, in order to study their time resolution before and after irradiation.
- Design and production of 50 µm thin LGAD detectors using gallium as a p-type dopant in the multiplication layer instead of boron. Subsequently, a study of the timing performance of the detectors before and after irradiation should be done.
- Development and production of 50 µm thin i-LGAD microstrips and pixel detectors. Although the capacitance will be increased in thin devices, the gain will increase and the SNR will improve.

- Design and fabrication of 50 µm thin i-LGAD microstrips and pixels detectors using an AC coupling. These devices will eliminate the problem of charge sharing, which was seen in the AC-LGAD detectors. An additional study of the timing performance of the detectors before and after irradiation should be carried out.

- The superior radiation hardness of 3D sensors makes them the best choice for tracking application with harsh radiation environment [16]. The time resolution of unirradiated 3D detectors has been also done by G. Kramberger achieving a jitter of 47ps [157]. Thus, 3D detectors with an optimum cell design for timing applications and their production is under work at IMB-CNM.

Appendix A: Physic Models

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)}$$

The physical models used for the electrical simulation with SDEVICE of the processed devices are presented and explained in the next sections of the present appendix.

1. Band structure model

Bandgap narrowing is an important effect in highly doped devices as LGADs. The band structure models define an effective bandgap which accounts for the bandgap narrowing as:

$$E_{g,eff}(T) = E_g(T) - \Delta E_g^0 - \Delta E_g^{Fermi}$$ Eq. A. 1

where ΔE_g^{Fermi} is an optional correction to account for carrier statistics. The model used to take into account the bandgap narrowing is the Old Slotboom model. The Old Slotboom model is widely used in silicon diodes where the narrowing is modelled by Eq. A. 2.

$$\Delta E_g^0 = E_{bgn}\left[ln\left(\frac{N_{tot}}{N_{ref}}\right) + \sqrt{\left(ln\left(\frac{N_{tot}}{N_{ref}}\right)\right)^2 + \frac{1}{2}}\right]$$ Eq. A. 2

where E_{bgn} = 9 meV, N_{ref} = 10^{17} cm^{-3} and N_{tot} is the total doping concentration.

2. Mobility models

Sentaurus device offers different mobility models which take into account the degradation of the mobility due to carrier scatter with the impurities, carrier scatter with surface phonons and surface roughness, carrier-carrier scattering and high electric field regions.

When more than one mobility model is activated, their contributions are combined

following Mathiessen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} \ldots. \qquad \text{Eq. A. 3}$$

The basic models activated in SDEVICE simulation are doping dependence, degradation at interfaces, carrier-carriers scattering and high field saturation.

Doping dependence mobility

Carriers scatter with impurities introduced in doped silicon leading to a degradation of the carrier mobility. The default model in silicon device simulation is the Masetti model[158]:

$$\mu_{dop} = \mu_{min1} exp\left(-\frac{P_c}{N_{tot}}\right) + \frac{\mu_{const} - \mu_{min2}}{1 + (N_{tot}/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/N_{tot})^{\beta}} \qquad \text{Eq. A. 4}$$

where the reference mobilities μ_{min1}, μ_{min2}, and μ_1, the reference doping concentrations P_c, C_r, and C_s, and the exponents α and β are listed in Table A. 1.

The N_{tot} is the total ionized impurities and μ_{const} is the constant mobility due to phonon scattering.

Table A. 1. Masseti model default coefficients

Symbol	Electrons	Holes	Unit
μ_{min1}	52.2	44.9	cm^2/Vs
μ_{min2}	52.2	0	cm^2/Vs
μ_1	43.4	29.0	cm^2/Vs
P_c	0	$9.23 \cdot 10^{16}$	cm^{-3}
C_r	$9.68 \cdot 10^{16}$	$2.23 \cdot 10^{17}$	cm^{-3}
C_s	$3.34 \cdot 10^{20}$	$6.10 \cdot 10^{20}$	cm^{-3}
α	0.680	0.719	1
β	2.0	2.0	1

Degradation at interfaces

High transverse electric fields present at the interfaces force the carriers to interact with the interface. The mobility degradation due to scattering by acoustic surface phonons and surface roughness is described in the Lombardi model [159]. The surface contribution due to acoustic phono scattering has the form:

$$\mu_{ac} = \frac{B}{E_\perp} + \frac{C(N_{tot}/N_0)^\lambda}{E_\perp^{1/3}(T/T_0)^k} \qquad \text{Eq. A. 5}$$

and the contribution attributed to surface roughness scattering is given by:

$$\mu_{sr} = \left(\frac{\left(E_\perp/E_{ref}\right)^{A*}}{\delta} + \frac{E_\perp^3}{\eta}\right)^{-1} \qquad \text{Eq. A. 6}$$

These surface contributions to the mobility are then combined with the bulk mobility μ_b according to Mathiessen's rule

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}} \qquad \text{Eq. A. 7}$$

where $D = \exp(-x/l_{crit})$ is a damping that switches off the inversion layer terms far away from the interface. Table A. 2 presents the default values of Lombardi model.

Table A. 2. Lombardi model default coefficients

Symbol	Electrons	Holes	Unit
B	$4.75 \cdot 10^7$	$9.925 \cdot 10^6$	cm/s
C	$5.80 \cdot 10^2$	$2.947 \cdot 10^3$	$Cm^{5/3}V^{-2/3}\ s^{-1}$
λ	0.1250	0.0317	1
δ	$5.82 \cdot 10^{14}$	$2.0546 \cdot 10^{14}$	Cm^2/Vs
η	$5.82 \cdot 10^{30}$	$2.0546 \cdot 10^{30}$	$V^2cm^{-1}s^{-1}$
$\mathbf{l_{crit}}$	$1 \cdot 10^{-6}$	$1 \cdot 10^{-6}$	cm

Carrier-carrier scattering

The degradation in the mobility due to the carrier-carrier scattering is described by the Conwell-Weisskopf screening theory [160]:

$$\mu_{eh} = \frac{D\left(\frac{T}{T_0}\right)^{3/2}}{\sqrt{np}}\left[ln\left(1 + F\left(\frac{T}{T_0}\right)^2 (pn)^{-1/3}\right)\right]^{-1} \quad \text{Eq. A. 8}$$

where n and p are the electron and hole densities respectively, and the values of parameters D and F are $1.02 \cdot 10^{21}$ $cm^{-1}V^{-1}s^{-1}$ and $7.452 \cdot 10^{13}$ cm^{-2} respectively.

High field saturation

In high electric fields, the carrier drift velocity is no longer proportional to the electric field, instead, the velocity saturates to v_{sat}. The velocity saturation is implemented in the simulator by using the Canali model [161]:

$$\mu(E) = \frac{(\alpha+1)\mu_{low}}{\alpha+\left[1+\left(\frac{(\alpha+1)\mu_{low}E}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \quad \text{Eq. A. 9}$$

where α equals zero for silicon, μ_{low} denotes the low-field mobility and v_{sat} and β are temperature dependent according to:

$$v_{sat} = v_{sat,0}\left(\frac{T_0}{T}\right)^{v_{sat,exp}} \quad \text{Eq. A. 10}$$

$$\beta = \beta_0\left(\frac{T}{T_0}\right)^{\beta_{exp}} \quad \text{Eq. A. 11}$$

Table A. 3 lists the default values of the Canali model.

Table A. 3: Default coefficients of Canali model

Symbol	Electrons	Holes	Unit
$v_{sat,0}$	$1.07 \cdot 10^7$	$8.37 \cdot 10^6$	cm/s
$v_{sat,exp}$	0.87	0.52	1
β_0	1.109	1.213	1
β_{exp}	0.66	0.17	1

Generation-recombination models

Generation-recombination processes exchange carriers between the conduction band and the valence band.

Shockley-Read-Hall (SRH) recombination

SRH recombination is assisted via deep defect levels in the gap. The net recombination of SRH process is

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n+n_1)+\tau_n(p+p_1)} \quad \text{Eq. A. 12}$$

where the carriers concentrations n_1 and p_1 related to the traps are

$$n_1 = n_i exp\left(\frac{E_{trap}-E_i}{k_B T}\right) \quad \text{Eq. A. 13}$$

$$p_1 = p_i exp\left(\frac{E_i-E_{trap}}{k_B T}\right) \quad \text{Eq. A. 14}$$

and the doping dependence of the minority carriers lifetimes are modeled with the Scharfetter relation

$$\tau_{dop}(N_i) = \tau_{min} + \frac{\tau_{max}-\tau_{min}}{1+\frac{N_i}{N_{ref}}} \quad \text{Eq. A. 15}$$

where the parameters τ_{min}, τ_{max}, N_{ref} for electron and holes are listed in Table A. 4.

Table A. 4: Parameters of the Scharfetter relation for the doping dependence of the minority carriers lifetimes

Symbol	Electrons	Holes	Unit
τ_{min}	0	0	s
τ_{max}	$2 \cdot 10^{-3}$	$7 \cdot 10^{-4}$	s
N_{ref}	10^{16}	10^{16}	cm^{-3}

Auger recombination

Auger recombination process is important at high carrier densities and involves the presence of a third particle (electron or hole) that receives the difference of energy of this band-to-band transition. The net recombination for Auger process is given by:

$$R_{net}^{Auger} = (C_n n + C_p p)(np - n_{i,eff}^2) \qquad \text{Eq. A. 16}$$

where the Auger coefficients C_n and C_p, corresponding to the two possible transitions are

$$C_n(T) = \left(A_{A,n} + B_{A,n}\left(\frac{T}{T_0}\right) + C_{A,n}\left(\frac{T}{T_0}\right)^2\right)\left(1 + H_n exp\left(-\frac{n}{N_{0,n}}\right)\right) \qquad \text{Eq. A. 17}$$

$$C_p(T) = \left(A_{A,p} + B_{A,p}\left(\frac{T}{T_0}\right) + C_{A,p}\left(\frac{T}{T_0}\right)^2\right)\left(1 + H_p exp\left(-\frac{p}{N_{0,p}}\right)\right) \qquad \text{Eq. A. 18}$$

Table A. 5 presents the values of the parameters A_A, B_A, C_A, H and N_0.

By default, SDEVICE only uses positive values of eq. 2.16 R_{net}^{Auger}. Negative values of R_{net}^{Auger} are replaced by zero. The WithGeneration option must be activated to allow the Auger generation of electron-hole pairs.

Table A. 5: Parameters of the Auger recombination coefficients

Symbol	Electrons	Holes	Unit
$\mathbf{A_A}$	$0.67 \cdot 10^{-31}$	$0.72 \cdot 10^{-31}$	cm^6/s
$\mathbf{B_A}$	$2.45 \cdot 10^{-31}$	$4.5 \cdot 10^{-33}$	cm^6/s
$\mathbf{C_A}$	$-2.2 \cdot 10^{-32}$	$2.63 \cdot 10^{-32}$	cm^6/s
H	3.46667	8.25688	1
$\mathbf{N_0}$	10^{18}	10^{18}	cm^{-3}

Avalanche generation

Electron-hole pair generation due to impact ionization requires a certain threshold field strength and wide space charge regions. Sentaurus device implements five models of the threshold behavior of the ionization coefficients. The model used in the simulation is the van Overstraeten-de Man, based on the Chynoweth law [162]:

$$\alpha(E_{ava}) = \gamma \cdot a \cdot exp\left(-\frac{\gamma b}{E_{ava}}\right) \quad \text{Eq. A. 19}$$

with:

$$\gamma = \frac{tanh\left(\frac{\hbar\omega_{op}}{2kT_0}\right)}{tanh\left(\frac{\hbar\omega_{op}}{2kT}\right)} \quad \text{Eq. A. 20}$$

The coefficients a, b, and $\hbar\omega_{op}$, as measured by van Overstraeten and de Man [163], are applicable over the range of fields $1.75 \cdot 10^5$ Vcm^{-1} to $6 \cdot 10^5$ Vcm^{-1} and are listed in Table A. 6.

Table A. 6: Coefficients for van Overstraeten-de Man model

Symbol	Electrons	Holes	Range of electric field	Unit
a	$7.03 \cdot 10^5$	$1.582 \cdot 10^6$	$1.75 \cdot 10^5$ Vcm^{-1} to E_0	cm^{-1}
	$7.03 \cdot 10^5$	$6.71 \cdot 10^5$	E_0 to $6 \cdot 10^5$ Vcm^{-1}	
b	$1.231 \cdot 10^6$	$2.036 \cdot 10^6$	$1.75 \cdot 10^5$ Vcm^{-1} to E_0	V/cm
	$1.231 \cdot 10^6$	$1.693 \cdot 10^6$	E_0 to $6 \cdot 10^5$ Vcm^{-1}	
E_0	$4 \cdot 10^5$	$4 \cdot 10^5$		V/cm
$\hbar\omega_{op}$	0.063	0.063		eV

Appendix B: Electrical characterization setup

The current and the capacitance of the detectors as a function of the reverse applied voltage must be measured because they determine critical parameters of the detector performance as the breakdown voltage, power dissipation, the shot noise, the equivalent noise charge, and the full depletion of the detector. In this appendix the electrical setup available at IMB-CNM radiation laboratory, in order to measure the current and the capacitance of the produced detectors, is presented. The setup consists of a Cascade Microtech probe station [164], a Espec thermal chuck system [165], two power suppliers [166], a LCR meter [167], a capacitive decoupling box and a PC with the acquisition programme, as it can be seen in Fig. B. 1.

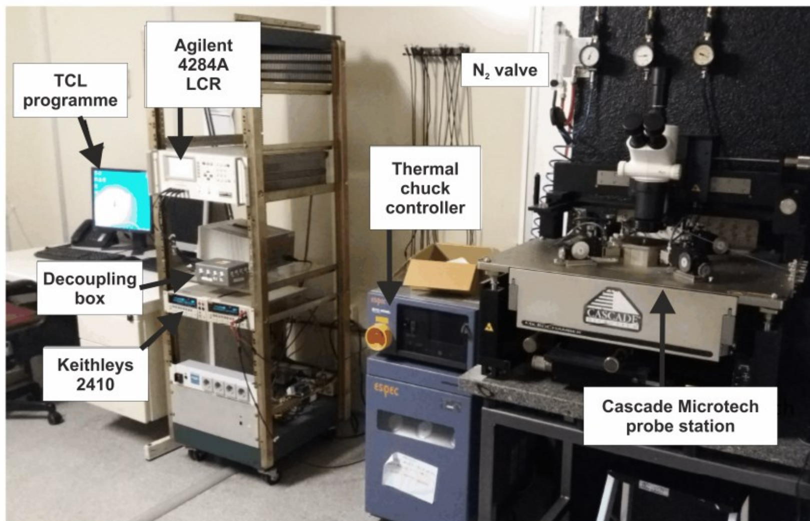


Fig. B. 1. Picture of the IMB-CNM Radiation lab electrical setup which consist of: a probe station (Cascade Microtech model), a Thermal chuck system (Espec), two power supplies (Keithley 2410), a capacitive decoupling box, a LCR meter (Agilent 4284A) and a PC with the acquisition tcl programme.

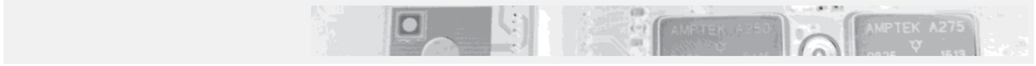
The Cascade Microtech probe station has 4 probes positioners, which are closed inside a Faraday box to seal the samples from electromagnetic interferences and light exposure. A N_2 valve is connected to the Faraday box to purge air from the box. The air is replaced by N_2 gas and the humidity inside the Faraday box decreases. The chuck is thermally controlled by the Espec thermal system. The temperatures can range from -60 to 200 ºC. The probes and chuck are connected to the power suppliers or the decoupling box via a triaxial and coaxial cable connector, respectively. The power suppliers are two Keithley 2410 sourcemeters, which can supply a maximum voltage of 1100 V and they can measure current values from 10 pA to 1.055 A. One Keithley is used to bias the pad/strips/pixels, while the other one is connected to the guard ring. Both Keithleys are connected to the same ground. The decoupling box decouples the sinusoidal signal of the LCR meter from the sourcemeter DC signal. Finally the PC with a tcl programme controls the LCR meter and both power suppliers. The programme was designed to perform simultaneous voltage sweeps on both Keithleys.

The chuck is always grounded and the high voltage is applied at the probes which contact the cathode (n^+ electrode) of the pad and the guard ring. The measurements are done in a controlled humidity ambient at 20 C.

The tcl programme which controls all the instruments allows to set the starting and final voltage of the voltage sweep, the sweep step, the number of measurements per point and the compliance. The number of measurements per point is set to 5 and a compliance value of 10 µA is used in all the measurements. The programme aborts the measurement whenever the current reaches the compliance.

In order to measure the capacitance with the LCR meter, an initial open correction should be performed. The short correction is not done because the offset error due to the residual impedance is negligible for capacitance values < 10 pF. Different capacitance modes can be used to measure the capacitance. The model Cp-G of the LCR meter is selected to do the capacitance measurement since the measured capacitance is small. This small capacitance yields a large reactance which means the effect of the parallel resistance is more significant than the series resistance and this last one can be neglected. Finally, the amplitude and frequency of the small AC signal are set in the tcl programme to 500 mV and 10 kHz, respectively.

APPENDIX C: GAIN MEASUREMENT SETUP



The measurement of the gain is performed at the IMB-CNM-CSIC radiation laboratory. In this appendix the available setup used to measure the gain is presented. The setup consists of a readout board which is placed inside a light tight box, a TTI EX354Tv triple power supply, a Keithley 2410 sourcemeter, a Ortec 671 amplifier, a Tektronix TDS 2024B oscilloscope, a MCA8000A multichannel analyzer and a PC with the ADMCA software, as it can be seen in Fig. C. 1.

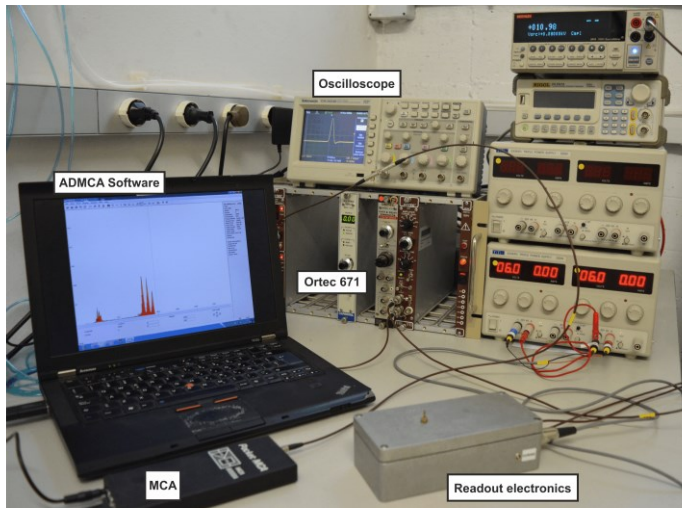
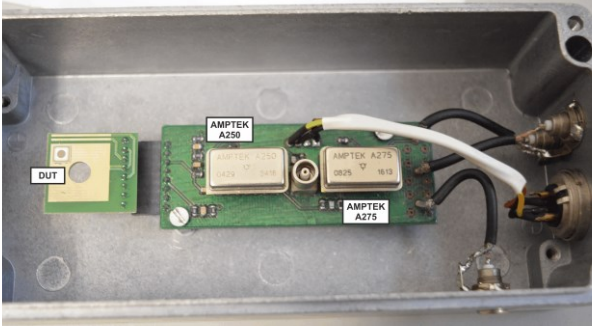


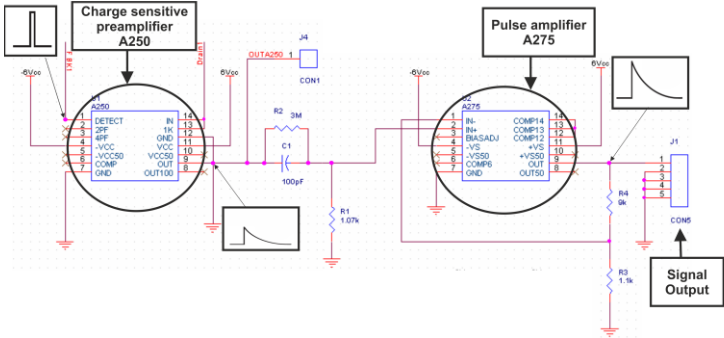
Fig. C. 1. The tri-alpha setup consist of: the Amptek readout board where the detector under study is wire bonded, the Ortec amplifier which shapes the pulse to a gaussian pulse, a oscilloscope, a MCA multichannel analyzer and a PC with the ADMCA Display and Acquisition Software.

The device under test is glued to a PCB board using silver conductive adhesive, as it is shown in Fig. C. 2. a). The board is placed inside a light tight box which also has a valve allowing the flow of N_2 inside the box. A small hole on the board, where the detector is going to be glued, is done to let the pass of alpha particles. The pad of the DUT is wire bonded to the ground, while the guard ring is left

floating. The high voltage is applied to the backside plane with a Keithley 2410 sourcemeter. The tri-alpha source is placed under the DUT. The signal generated in the backside illuminated detector is amplified and shaped by a charge sensitive preamplifier Amptek A250. The long decay of the step impulse is shortened forming a pointy cusp, as it can be seen in Fig. C. 2. b). The output of the Amptek A250 is the input of the Amptek A275, which amplifies by a factor of 10 the input signal. Before the digitalization, the pulse needs a smooth cusp. The Ortec 761 amplifier shapes the output signal of the Amptek A275 into a symmetric gaussian pulse smoothing the pulse cusp. It also amplifies the signal by a factor of 2.5 which is the minimum available gain of the Ortec. The integration time of the electronics is 500 ns, which is larger than the collection time of irradiated detectors. The pulse is visualized by the Tektronix TDS 2024B oscilloscope before it is digitalized by the MCA8000A multichannel analyser. The ADMCA software records and graphs the counts vs. the channels provided by the MCA during a determined interval of time.



a)



b)

Fig. C. 2. Picture of the Amptek board where the DUT and Amptek amplifiers are indicated a) . Electronic scheme of the readout electronics b). The evolution of the pulse is also plotted after each amplifier.

List of Publications

G.Pellegrini et al. "Recent technological developments on LGAD and iLGAD detectors for tracking and timing applications", *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 831, pp. 24–28, Sep. 2016; http://dx.doi.org/10.1016/j.nima.2016.05.066

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D. Vázquez Furelos et al. "3D sensors for the HL-LHC", *J. Instrum.*, vol. 12, January 2017; http://dx.doi.org/10.1088/1748-0221/12/01/C01026

O. Alonso et al. "Readout electronics for LGAD sensors", *J. Instrum.*, vol. 12, February 2017; http://dx.doi.org/10.1088/1748-0221/12/02/C02069

Cartiglia et al. "Beam test results of a 16ps timing system based on UFSD detectors", *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 850, pp. 83–88, Apr. 2017; http://dx.doi.org/10.1016/j.nima.2017.01.021

J.Lange et al. "Gain and time resolution of 45µm thin Low Gain Avalanche Detectors before and after irradiation up to a fluence of 10^{15} n_{eq}/cm^2", *J. Instrum.*, vol. 12, May 2017; http://dx.doi.org/10.1088/1748-0221/12/05/P05003

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A. Apresyan et al. "Studies of uniformity of 50µm low gain avalanche detectors at the Fermilab test beam", *Nucl. Instruments Methods Phys. Res.*

Sect. A Accel. Spectrometers, Detect. Assoc. Equip., vol. 895, pp. 152–172, Jul. 2018; https://doi.org/10.1016/j.nima.2018.03.074

G.Kramberger et al. "Radiation hardness of gallium doped low gain avalanche detectors"; *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 898, pp. 53–59, Jul. 2018; https://doi.org/10.1016/j.nima.2018.04.060

C. Allaire et al. "Beam test measurements of low gain avalanche detector single pads and arrays for the ATLAS High Granularity Timing Detector"; *J. Instrum.*, vol. 13, June 2018; https://doi.org/10.1088/1748-0221/13/06/P06017

M. Carulla et al. "50 µm thin LGAD for timing applications"; *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 924, pp. 373–379, Apr. 2019; https://doi.org/10.1016/j.nima.2018.08.041

S. Otero et al. "Radiation tolerance of proton-irradiated LGADs"; *IEEE Trans. Nucl. Sci.*, vol. 35, no. 8 pp. 1667–1675, 2018; http://doi.org/10.1109/TNS.2018.2826725

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