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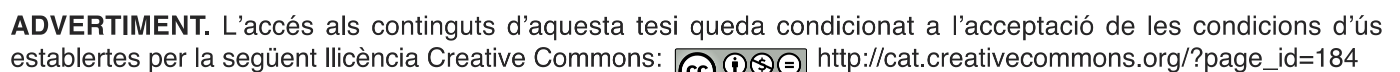
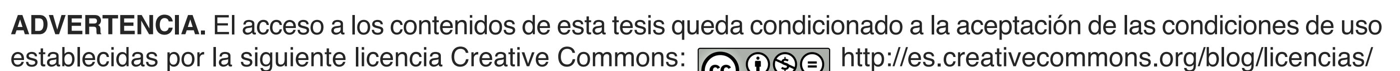
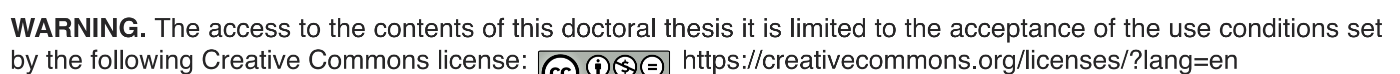
ADVERTIMENT. L'accés als continguts d'aquesta tesi queda condicionat a l'acceptació de les condicions d'ús establertes per la següent llicència Creative Commons:  http://cat.creativecommons.org/?page_id=184

ADVERTENCIA. El acceso a los contenidos de esta tesis queda condicionado a la aceptación de las condiciones de uso establecidas por la siguiente licencia Creative Commons:  http://es.creativecommons.org/blog/licencias/

WARNING. The access to the contents of this doctoral thesis it is limited to the acceptance of the use conditions set by the following Creative Commons license:  https://creativecommons.org/licenses/?lang=en

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Directed self-assembly of block copolymers for the fabrication of nanomechanical structures

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Dissertation for the degree of Doctor in Electronic and Telecommunication Engineering

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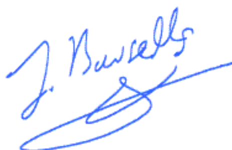
Academic tutor: 

Joan Bausells Roigé

Abstract

The main goal of this dissertation, entitled “Directed self-assembly of block copolymers for the fabrication of nanomechanical structures”, is to demonstrate the possibility of fabricating nanomechanical functional structures by employing the directed self-assembly (DSA) of block copolymers (BCPs) as a nanopatterning tool.

DSA is a bottom-up nanolithography technique based on the ability of BCPs to segregate into domains at the micro/nanoscale, and it has attracted high interest due to its inherent simplicity, high throughput, low cost and potential for sub-10 nm resolution. Thanks to these characteristics, the technique has been heavily studied by the semiconductor industry for nanoelectronics, and also applied to alternate fields that might require from the definition of high-density nanoscale features.

In this thesis we present a novel fabrication route based on DSA that proves to be suitable for the fabrication of nanomechanical systems. Here, we demonstrate the fabrication of suspended silicon membranes clamped by high-density arrays of silicon nanowires by using a DSA approach based on the graphoepitaxy of polystyrene-b-poly(methyl methacrylate) (PS-b-PMMA), a well-known diblock copolymer. Obtained devices can be further developed for building up high-sensitive mass sensors based on nanomechanical resonators.

Resumen

El principal objetivo de esta tesis, titulada “Autoensamblaje dirigido de copolímeros de bloque para la fabricación de estructuras nanomecánicas”, es demostrar la posibilidad de fabricar estructuras nanomecánicas funcionales mediante el autoensamblaje dirigido (DSA) de copolímeros de bloque (BCPs) como técnica de nanoestructuración.

El DSA es una técnica de nanolitografía *bottom-up* basada en la capacidad que tienen los BCPs de segregarse en dominios de escala micro/nanométrica. Gracias a su alta resolución, alto rendimiento y bajo coste, esta técnica ha sido muy estudiada por la industria de semiconductores para nanoelectrónica, pero también ha sido aplicada en otros campos que requieren de una alta densidad de elementos a escala nanométrica.

En esta tesis presentamos un proceso novedoso basado en DSA que demuestra ser apto para la fabricación de sistemas nanomecánicos. Demostramos la fabricación de membranas de silicio suspendidas ancladas por matrices de gran número de nanohilos de silicio empleando la grafoepitaxia de poliestireno-b-polimetilmetacrilato (PS-b-PMMA), uno de los BCP más extendidos. Los dispositivos obtenidos pueden desarrollarse para construir sensores de masa de alta sensibilidad basados en resonadores nanomecánicos.

To my parents and my wife.

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List of abbreviations and symbols

α – phase

β_n – wavenumber

$\Delta\omega_{3dB}$ – bandwidth at full-width at half-maximum

ε – strain

ε_0 – vacuum permittivity

ε_r – relative permittivity

ζ – damping ratio

ϑ – Poisson’s ratio

κ – dielectric constant

λ – wavelength

ρ – density

χ – Flory-Huggins interaction parameter

ω –frequency

ω_n – eigenfrequency

ω_r – resonant frequency

A – area

AFM – atomic force microscopy

Al – aluminum

Al_2O_3 – aluminum oxide, alumina

ALD – atomic layer deposition

AlN – aluminum nitride

Ar – argon

ArF – argon fluoride

Au – gold

b – base width

$\vec{B}$ – magnetic flux density

BCP – block copolymer

BJT – bipolar junction transistor

BOX – buried oxide

c – coefficient of damping

C – capacitance

C=O – carbonyl group

CF_2 – difluorocarbene

CF_4 – carbon tetrafluoride

C_4F_8 – octafluorocyclobutane

CHF_3 – trifluoromethane

CMOS – complementary metal-oxide-semiconductor

CNT – carbon nanotube

CO – carbon monoxide

CO_2 – carbon dioxide

Cr – chrome

d – distance

DRAM – dynamic random access memory

DSA – directed self-assembly

DUV – deep ultraviolet

E – Young's modulus

E_p – potential energy

EBL – electron-beam lithography

EUV – extreme ultraviolet

f – relative volume fraction

F – force

f_{CAR} – carrier wave frequency

f_{MES} – message wave frequency

F_e – electrostatic force

$\vec{F}_L$ – Lorentz force

FEM – finite element modeling

FinFET – fin field-effect transistor

GAA – gate-all-around

GaAs – gallium arsenide

GaN – gallium nitride

GF – gauge factor

GP – guiding pattern

h – height

HF – hydrofluoric acid

HfO_2 – hafnium oxide, hafnia

Hg – mercury

HSQ – hydrogen silsesquioxane

I – electric current

I_Y – moment of inertia with respect to Y

IBM – International Business Machines Corporation

ICP – inductively coupled plasma

IPA - isopropanol

k_{eff} – effective spring constant

KrF – krypton fluoride

L – length

LDV – laser-Doppler vibrometry

L_0 – block copolymer natural pitch at thermodynamic equilibrium

m – mass

m_{eff} – effective mass

MEMS – microelectromechanical systems

MIBK – methyl isobutyl ketone

MOSFET – metal-oxide-semiconductor field-effect transistor

$MoSi_2$ – molybdenum disilicide

n – density multiplication

N – degree of chain polymerization

N_2 – nitrogen

N_2O – nitrous oxide

NEMS – nanoelectromechanical systems

NGL – next-generation lithography

NIL – nanoimprint lithography

NW – nanowire

O_2 – oxygen

PECVD – plasma-enhanced chemical vapor deposition

PGMEA – propylene glycol methyl ether acetate

PMMA – poly(methyl methacrylate)

PS – polystyrene

PS-b-PMMA – polystyrene-block-poly(methyl methacrylate)

PS-r-PMMA – polystyrene-r-poly(methyl methacrylate)

PZT – lead zirconate titanate

q – charge

Q – quality factor; electric charge

R – resistance

RF – radio frequency

RIE – reactive ion etching

SADP – self-aligned double patterning

SEM – scanning electron microscopy

SF_6 – sulfur hexafluoride

Si – silicon

SiARC/SOC – silicon antireflective coating/spin-on-carbon

SiC – silicon carbide

SiF_4 – silicon tetrafluoride

SiH_4 – silane

SiO_2 – silicon dioxide

SiNW – silicon nanowire

SIS – sequential infiltration synthesis

Sn – tin

SOI – silicon-on-insulator

TEM – transmission electron microscopy

TiN – titanium nitride

TMA – trimethyl-aluminum

TMAH – tetramethylammonium hydroxide

UV – ultraviolet

$\vec{v}$ – velocity

V – electric potential, voltage

V_0 – amplitude of carrier wave

V_{EMF} – electromotive force

W – width

W – tungsten

Xn – xenon

x_0 – amplitude of motion

z_0 – amplitude of vibration

ZnO – zinc oxide

ZrO – zirconium oxide

Chapter 1

Introduction to nanolithography and block copolymers

Since the middle of the 20th century, the semiconductor industry has been a worldwide leader in terms of technological development. Competitiveness has pushed the limits of innovation in such a way that in less than 80 years, 27-ton military computers have turned into the smartphone in your pocket. The main enabler of such scaling has been the evolution of lithography, as advances in optical lithography have provided enough resolution to reach the 7-nm node. Nevertheless, for further scaling, exponentially increased costs and light diffraction li

mitations have led to the search of new lithographic alternatives.

This chapter discusses the evolution of lithography towards extreme scaling, gives an introduction to the main properties of block copolymers and discusses the interest they draw in the enhancement of resolution of current lithography tools.

1.1 THE EVOLUTION OF SCALING

Introduction

Undoubtedly, the semiconductor industry arose with the invention of the bipolar junction transistor (BJT) in 1947 at Bell Telephone Laboratories, by J. Bardeen and W. Brattain. A decade later, during 1958 and 1959, Jack Kilby, at Texas Instruments, and Bob Noyce, at Fairchild Semiconductor, started working on the possibility of fabricating all devices (transistors, capacitors and resistors) integrated in a sole piece of semiconductor, giving birth to the integrated circuit [1].

With the evolution to digital technologies and increasing density of transistors, the n-type metal–oxide–semiconductor field-effect transistor (MOSFET) replaced the BJT, to transition in the 1980s toward complementary metal–oxide–semiconductor (CMOS), more complex and costly but with low-power characteristics [2].

Moore's Law and steady scaling

Moore's Law, named after Intel's co-founder Gordon Moore, postulates that the number of transistors in integrated circuits doubles, at constant price, approximately every two years [3]. This empirical observation has proven correct and steady since its last reformulation in 1975 and has served as a guideline for investors, manufacturers and scientists to predict their business model and plan their research [4]. In light of expectations, a race towards shrinkage was started: the smaller the transistors, the more that could be packed in the same area, generating more powerful devices.

In table 1.1, an outlook of the evolution of semiconductor process nodes since 1971 is presented. When referring to a process node, all industrial methods and technologies involved in the fabrication process of those devices are considered. The concept was typically associated with the physical gate length of the transistor or the minimum half-pitch of metal interconnect obtained in such process [5], but nowadays the nomenclature no longer matches any actual physical dimension.

TABLE 1.1
SEMICONDUCTOR PROCESS NODES, WITH CORRESPONDING YEAR AND MAJOR TECHNOLOGY ENABLER

Node	Year	Technology associated
10 μm	1971	Constant-voltage scaling
6 μm	1974	
3 μm	1977	
1.5 μm	1981	Chemically amplified resist
1 μm	1984	
800 nm	1987	
600 nm	1990	Constant-field scaling
350 nm	1993	Hg lamp (λ = 365 nm)
250 nm	1996	
180 nm	1999	KrF laser (λ = 248 nm)
130 nm	2001	
90 nm	2003	ArF laser (λ = 193 nm)
65 nm	2005	Stressed channel
45 nm	2007	High-κ metal gate
32 nm	2009	Double patterning
22 nm	2012	FinFET
14 nm	2014	
10 nm	2016	Multiple patterning
7 nm	2018	EUV
5 nm	2019	
3 nm	~2021	
2 nm	~2024	

As exposed in the table, at the dawn of the second millennium devices reached nanoscale dimensions thanks to advances in short-wavelength sources, lenses, resists and masks. In the 90-nm node (2003), lithography relying on deep ultraviolet (DUV) was introduced with ArF lasers as light source, combined with immersion lithography [6]. In immersion lithography the air gap between lens and wafer is replaced with purified water, which has a higher refractive index, enhancing resolution.

As dimensions kept decreasing, complex doping, stress engineering [7] and new high-κ insulators [8] made the scene to avoid short-channel and quantum effects, but it was not until the 32-nm node when the feature pitch was below the resolution limit of the optical projection system and further scaling required the use of double patterning for the first time [9].

In 2010 Intel commercially launched the first working 32-nm processor, defined by self-aligned double patterning (SADP, figure 1.1) [10]. With the arrival of the 22-nm node, the semiconductor industry was once more revolutionized with the introduction of the fin field-effect transistor (FinFET) [11], which represented a radical shift in terms of architecture (figure 1.2). By using a transistor in 3D instead of planar, the contact surface of the gate is maximized, gaining substantial control over the channel [12].

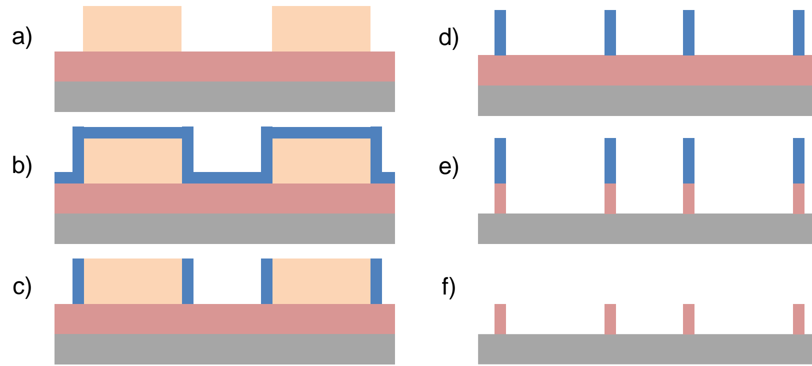

Fig. 1.1. Self-aligned double patterning. First, a conformal thin film of oxide is formed on top of a pre-patterned feature on the substrate (a, b). Afterwards, the horizontal surfaces and the pre-patterned features are etched in plasma (c, d), leaving the lateral spacers as mask for further pattern transfer (e, f).

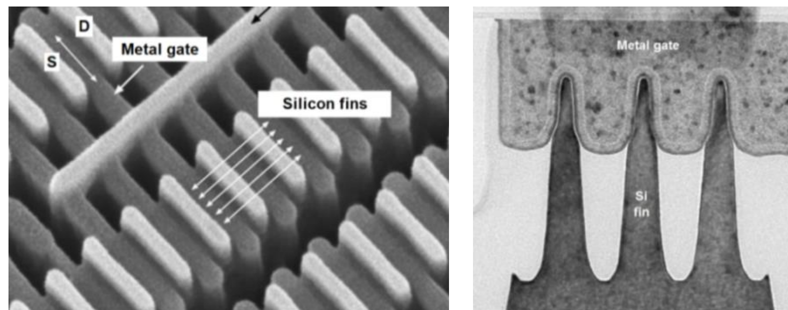

Fig. 1.2. On the left, scanning electron microscopy (SEM) tilted-view micrograph of 14-nm node FinFETs from Samsung's Exynos 7420 (D is drain and S is source). On the right, their transmission electron microscopy (TEM) cross-section [13].

Latest nodes

Samsung was the first chipset giant to develop a fabrication process of 7-nm devices completely fabricated by extreme ultraviolet lithography, entering wafer testing in late 2019 [14]. Other companies like TSMC extended the use of conventional ArF immersion lithography combined with several cycles of SADP for the node, to finally jump to EUV by the end of 2019 as well [15].

Plans for the 5-nm node have already been unveiled, and both Samsung and TSMC have targeted high volume production for late 2020 [16], [17]. It is still undisclosed, however, whether FinFETs will remain the main architecture for logic devices in the following nodes, as gate-all-around field-effect transistors (GAA FETs) based on

nanowires or nanosheets are considered an alternative at both 5 nm and 3 nm [18], [19]. In these devices, the gain in contact surface is even higher, as the gate oxide completely surrounds the body of the transistor, enhancing electrostatic control over the channel [20].

1.2 NEXT-GENERATION LITHOGRAPHY TECHNIQUES

Several new integration schemes and materials have been proposed to keep the relentless increase in device density going. The four candidates best adapted to mass production, and known as next-generation lithography (NGL) techniques, are: extreme ultraviolet lithography, nanoimprint lithography, multi-beam electron-beam lithography and directed self-assembly of block copolymers [21].

As of today, EUV has taken over the main spot for advanced lithography at the industry level and has been successfully introduced in production lines of nanoelectronic devices, but as its combination with multiple patterning presents exponentially increased costs due to its complexity, research in the rest of NGL techniques still remains of great interest.

Extreme ultraviolet lithography (EUV)

EUV is based on soft X-ray technology, with a laser-driven Sn plasma source that emits light at the extremely short wavelength of 13.5 nm, then reflects in at least 10 multilayer reflective $MoSi_2$ mirror systems in a hydrogen atmosphere, to finally reach the wafer in high vacuum [22]. Tools (figure 1.3) are very complex, weigh around 180 tons, cost approximately $120 million and exclusively produced by the Dutch company ASML.

Initially, the major problem of EUV was the high and stable power needed at the source. As all matter absorbs EUV radiation, even by using all-reflective optics and photomasks, a very significant fraction of the input power gets lost in the path to the wafer, hence the high powers needed [23].

Figure 1.3. EUV tool. Image from ASML.

Resist advances to meet roughness standards and photospeed [24] have also been an issue, as well as the development of protective covers (known as pellicles) to reduce mask defects [25].

EUV has been the most conservative patterning strategy taken into consideration for advanced nodes, therefore the preferred option for chipmakers. It had already been considered for the 16-nm node, but technological issues delayed its transition into high-volume manufacturing [26]. Finally, as of 2020, all major foundries have already committed to EUV for their cutting-edge production lines.

Nanoimprint lithography (NIL)

NIL is a stamp-based process where a mold (fabricated by conventional technology) is pressed against resist on a wafer. Features in the mold are then negatively transferred into the resist and remain once the mold is detached.

Two different approaches can be used to cure that resist in order to replicate the mold: heat and ultraviolet (UV) radiation (figure 1.4). In the first case, the polymer used is a thermoplastic that is heated above glass transition temperature, adapting its shape to that of the mold. In the second, resist is an UV-curable polymer, able to polymerize when the sample is irradiated by UV light through a transparent mold [27].

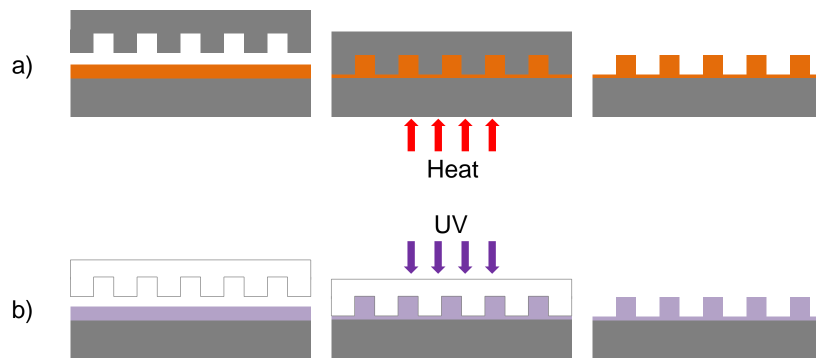

Fig. 1.4. Scheme of the principles of NIL by heat (a) and UV radiation (b).

NIL is a simple technology, completely unrelated to light diffraction limitations, and has made significant progress in defectivity, throughput and resolution in the last few years. In fact, it is able to compete with DUV light sources in low-demanding lithography applications [28].

Nevertheless, for advanced logic and dynamic random access memory (DRAM), ultra-high resolution is needed for the fabrication of stamps, making them expensive and with limited lifetime [29]. Fabrication techniques need to be optimized to achieve higher resolution stamps free of damage [30], to improve multilayer alignment and to avoid resist adhesion [31].

Multi-beam electron-beam lithography (Multi-beam EBL)

EBL is a well-known technique that offers extremely high resolution (sub-6 nm) thanks to the very short wavelength of its source, which is in fact, a beam of electrons accelerated at 5 to 100 kV. These electrons are focused on a resist-coated wafer, chemically modifying the exposed area and enabling its selective removal after development [32].

Resolution, although limited by many of the processing variables (temperature, optics, beam energy, dose, development, scattering and backscattering of electrons in the resist), is high enough for manufacturing at the latest nodes. Unfortunately it is not easily scalable as it writes feature after feature in a direct writing method. The only industry niches where EBL has established itself so far are the fabrication of optics gratings, masks and prototyping.

Plausible alternatives to adapt EBL to high-volume manufacturing have been studied by KLA-Tencor, Tokyo Electron or MAPPER. In MAPPER's approach, a beam from a single electron source is split up into 13,000 parallel electron beams able to write simultaneously and be blanked controllably [33]. Even though their systems achieve very high resolution, they are still too slow for industry requirements (300 wafers per hour) and no tool is expected to be developed for high-volume manufacturing [34], [35].

Directed self-assembly (DSA) of block copolymers (BCPs)

In DSA, BCPs –a variety of polymers that are able to segregate into long-range ordered periodic nanostructures– are used to increase the density multiplication of pre-existing patterns fabricated by conventional lithography [36].

Researchers have been able to integrate DSA into conventional 300-mm pilot lines to generate parallel line density multiplication or contact-hole shrinking arrays [38], [39], [40], [41], [42] without relevant infrastructure upgrades, as the key processing steps can be implemented in existing tracks.

Being an affordable high-resolution method with the possibility of scaling up [37], it has drawn a lot of attention in industrial semiconductor processing since the late 1990s [43], [44], [45], long before the commercial availability of EUV [46], [47], [48]. However, the present main limitation for its further incorporation into high-volume manufacturing is its capability to meet industry defect density standards [49], [50].

1.3 PHYSICAL PROPERTIES OF BLOCK COPOLYMERS

Definition

BCPs are macromolecules consisting of covalently bonded homogeneous blocks (or chains) of chemically different monomers. Due to the repulsion forces between the blocks, and in order to present minimal free energy, BCPs spontaneously segregate into microdomains after a thermally driven phase separation process, generating self-assembled structures that form spatially high-resolution periodic patterns in the nano/microscale [51], [52]. Typically, after self-assembly, one of the blocks is removed and the remaining polymer is used as mask to pattern the substrate underneath [53].

The simplest BCPs are linear A-b-B diblock copolymers, where A and B are two different polymeric blocks, joined together by a covalent bond. It is the case of the BCP used in the experimental section of this thesis: polystyrene-block-poly(methyl methacrylate), or PS-b-PMMA (figure 1.5), formed by a chain of polystyrene (PS) and a chain of poly(methyl methacrylate) (PMMA) covalently bonded.

PS-b-PMMA is amongst the most extended BCPs for lithography applications, as both PS and PMMA are polymers with studied etch properties, easy to manipulate, show a reasonable temperature range for annealing and present similar affinity to air [54], [55], [56]. Extensive characterization of self-assembled PS-b-PMMA thin films has been carried out regarding annealing conditions, kinetics, defectivity, line-edge roughness and nanomechanical properties of the blocks [57], [58], [59], [60], [61], [62], [63], [64], [65]. However, for extreme scaling, PS-b-PMMA is limited due to its low χ value (χ = 0.03 at 150 ºC), which restricts attainable minimum feature size [66], [67].

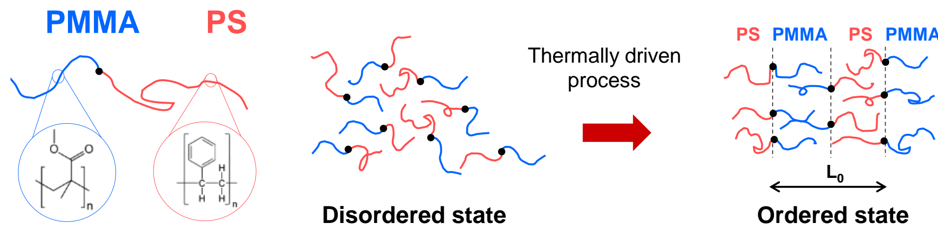

Fig. 1.5. Illustration of PS-b-PMMA, in disordered and assembled, or ordered, state. L_0 represents the block copolymer natural pitch at thermodynamic equilibrium and for PS-b-PMMA can be as small as ~22 nanometers.

Morphologies and phase segregation in diblock copolymers

Three parameters determine the size, morphology and phase behavior of a diblock copolymer with species A and B: the total number of monomer units that compose the BCP (degree of chain polymerization, N), the relative volume fraction of each component A and B in the mixture (f) and the Flory-Huggins interaction parameter (χ) [52], [68].

Both N and f depend on stoichiometry and entropy, while the Flory-Huggins parameter [69] is of enthalpic nature, inversely proportional to temperature [70], and depends on the material selection (block copolymer chemistry). It gives an idea of how strong the repulsive force between blocks A and B is.

The microphase segregation strength of BCPs is typically expressed by the product χN. In order to observe an ordered phase, it needs to be above the critical limit of 10.5 [52], [71]. For values below that, phase segregation does not exist and the BCP is in a disordered state. For χN values much higher than 10.5, strong microphase segregation is complete: the segregation force is strong enough for the phases to be composed of only one type of monomer (A or B). For values closer to 10.5, however, thermodynamic segregation is weak to ensure the formation of a sharp phase boundary between the two phases, generating regions of disorder and defects [72]. Therefore, to obtain structures with small period from BCPs with low N, high immiscibility between blocks is desired [66]. Also, for a certain χN, self-assembly occurs in different shapes depending on f, as shown in the phase diagram of a diblock copolymer (figure 1.6).

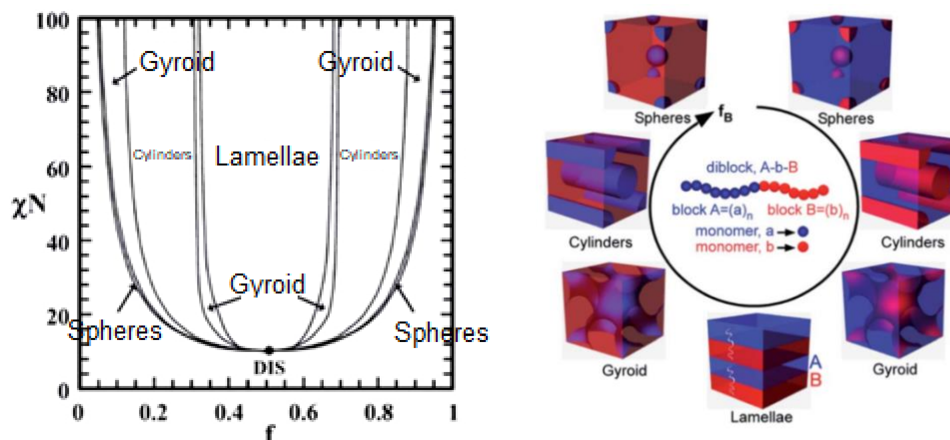

Fig. 1.6. Theoretical phase diagram and morphologies for an A-b-B diblock copolymer, adapted from [73]. Tuning the volume fraction of one of the blocks (f), polymer segregation takes place in different phases: closed-packed spheres, hexagonally packed cylinders, body-centered spheres, gyroid and lamellae.

1.4 BLOCK COPOLYMERS IN NANOLITHOGRAPHY

Block copolymer self-assembly on thin films

When a diluted solution of BCP is spin-coated on a substrate in the form of a thin film and self-assembly is induced, microphase segregation takes place in short-range order, generating condensed arrays of random periodic structures. In this situation, the contribution of bottom and top interfaces to the total free energy becomes very significant and phase behavior is strongly influenced by surface energetics [74].

If domain orientation is not controlled, the orientation of the arising pattern will be determined by the relative strength of surface affinity to each block of the BCP. An untreated substrate will show higher affinity to one of the blocks, attracting the domains with lower interaction energy stronger than the others. This effort to keep minimal free energy at the polymer-substrate interface can cause the BCP to assemble in an undesired wetting morphology, which might be useless for nanolithography applications (figure 1.7).

The most straightforward way to control pattern orientation is to balance the surface free energy between domains by spin-coating a random copolymer composed of the same monomer units as the block copolymer (PS-r-PMMA for PS-b-PMMA) in between substrate and BCP [55], [75], [76]. This thin film is known as neutral layer or brush, and by tuning its composition interface energy can be modified to favor the affinity of the substrate to one block or the other. Then, by applying a certain temperature higher than the glass transition temperature of both blocks, homogeneous phase separation can be achieved, as the mobility of polymer chains is increased [72].

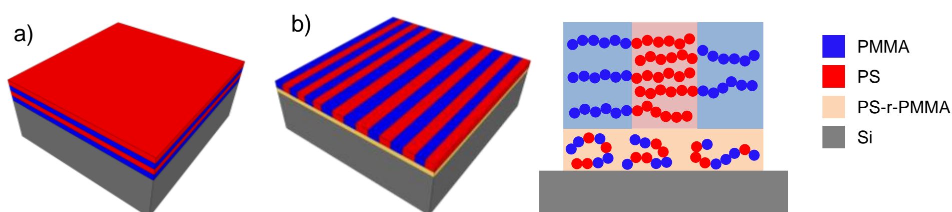

Fig. 1.7. Self-assembly of lamellar PS-b-PMMA. In a), the substrate shows preferential interaction with PMMA and self-assembly in horizontal lamellae guarantees minimal free energy. In b), however, a random copolymer brush (PS-r-PMMA) was used to impel neutral affinity to the substrate, coercing the generation of vertical PS and PMMA lamellae.

Enabling lithography with block copolymers

If the way BCPs self-assemble when rising temperature is not somehow guided, the immiscible polymer chains will generate random short-range patterns, in an arrangement similar to a fingerprint. In order to be useful for lithographic purposes, some guiding patterns (GPs) are necessary to place the self-assembly process into the desired morphology and long-range order, whilst BCP properties (molecular weight and composition) and thermodynamics control the feature size, shape and uniformity of the resulting domains. GPs are normally fabricated by top-down techniques, following two different approaches: chemoepitaxy and graphoepitaxy (figure 1.8) [36], [75], [77].

Chemoepitaxy involves the creation of dense chemical patterns on a neutral surface to generate preferential wetting sites for one of the blocks, enabling to direct the position and orientation of the molecules [78]. Such guiding patterns must have a pitch close to an integer of the natural pitch of the BCP ($n{\cdot}L_0$, n= 1, 2, 3), in order to assure commensurability of the film. This factor n is known as density multiplication of the guiding pattern. In addition, the lateral size must correspond to the half-pitch of the block copolymer or 1.5 times the block copolymer pitch [79]. Perpendicular DSA patterns have been demonstrated in symmetric PS-b-PMMA with density multiplication up to 10 in BCPs with higher χ values [80].

Multiple processes and techniques have been successfully used to selectively tune the surface free energy of a neutral surface, including photolithography [81], electron-beam lithography (EBL) and oxygen plasma functionalization [82], [83], [84], [85], [86], direct EBL exposure [79] and scanning-probe lithography [87], [88], [89].

Graphoepitaxy, on the other hand, is based on the definition of 3D features on the substrate, within DSA takes place [90], [91], [92], [93]. These topographical templates can be physically tailored, and bottom and walls along the trenches chemically modified to impose different affinity to each of the polymer blocks, enforcing their orientation along the topography [94], [95]. Regarding commensurability, if GP dimensions do not match an integer of the pitch of the BCP ($n{\cdot}L_0$, n= 1, 2, 3), the pattern might compress or stretch, releasing stress by generating dislocations along the GP length [94], [96].

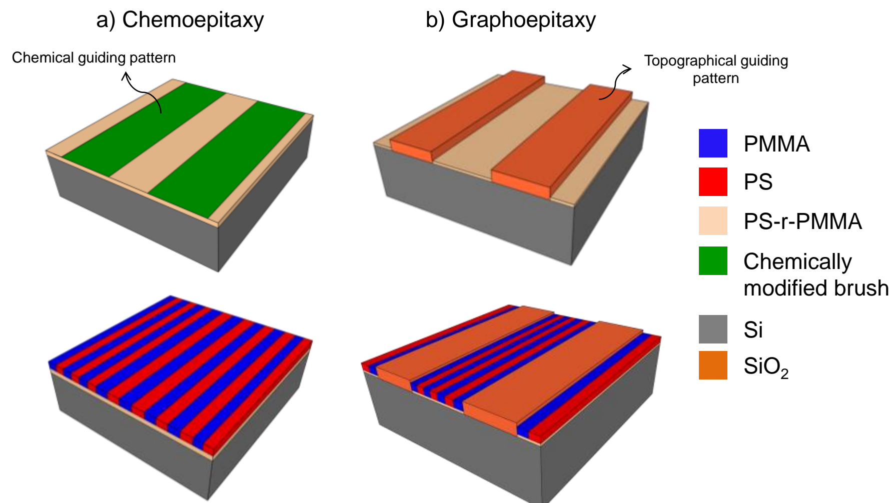

Fig. 1.8. Scheme of DSA by chemo- and graphoepitaxy. (a) In chemoepitaxy, areas of the substrate are chemically activated to show stronger affinity to one of the blocks, directing the self-assembly; (b) in graphoepitaxy, the substrate is topographically structured to direct the self-assembly.

Of special interest in graphoepitaxy are contact-hole and line-space pitch multiplication applications. In the first one, a lamellar or cylindrical block copolymer is used to reduce the dimensions of device contacts [97], [98]. The second one uses lamellar BCPs to generate arrays of lines for transistor fabrication [99], [100].

Present directions

The most attractive possibility of DSA to be incorporated into high-volume manufacturing seems to go through combining with mainstream patterning, primarily sponsored by its ease of integration into conventional process flows and wafer tracks, low cost and high throughput. DUV or EUV could pre-pattern GPs, without the need of double or quadruple patterning, where DSA could take the helm and define FinFETs [101] or contacts [102].

Still, the low value of χ in PS-b-PMMA limits minimum attainable resolution (to about 22 nm) [67]. Solutions to overcome this limitation come from chain modification of existing BCPs [103], [104], the use of additives [105] or the pursuit of novel molecular architectures of high-χ BCPs, giving access to sharp phase-separation at smaller natural periods [106], [107].

A wide variety of high-χ BCPs have been synthetized in the last few years, including organic and inorganic species [108], [109], [110], [111] which combine polymers that are strongly immiscible. Examples include organic polystyrene-b-poly(2-vinyl pyridine) (PS-b-P2VP) [112], [113], polystyrene-b-poly(4-vinyl pyridine) (PS-b-P4VP) [114] or polystyrene-b-poly(propylene carbonate) (PS-b-PPC) [115], and inorganic polystyrene-b-poly(trimethylsilylstyrene) (PS-b-PTMSS) [116] or polystyrene-b-polydimethylsiloxane (PS-b-PDMS) [90], for instance.

The development and implementation of such BCPs is not trivial, nonetheless. High-χ BCPs tend to organize differently on the substrate surface than at the air surface, usually needing solvent annealing [117], [118], [119], [120] or an overcoat of polymer to assure lamellae are standing up in the final BCP film [121], [122].

In addition, the selection of blocks must be optimum for etching, showing good selectivity between them and presenting compatible glass and order-disorder transition temperatures. The inclusion of inorganic blocks is particularly interesting as they provide higher etch contrast during selective block removal and pattern transfer [123], [124], although their lower surface energy can make it necessary to increase the number of etching steps due to the presence of preferential wetting layers [125].

Recent research on DSA has also been greatly focused on the study, understanding and mitigation of defects [126], [127], [128], [129], [130], [131], [132], [133], [134], [135]. As mentioned, minimization of defects is crucial for the incorporation of DSA into high-volume manufacturing, either as a primary patterning option or in combination with already established techniques like DUV or EUV.

BCPs for the fabrication of functional devices

Line-space pitch multiplication and contact via level patterning are the two most important applications of DSA in high-volume manufacturing. In line-space applications lamellar BCPs are used as mask to define arrays of silicon fins that form the main body of FinFETs. Multiple processes have demonstrated the capability of DSA to generate silicon fins [100], [136], [137], [138], [139], with probably the two most renowned being the LiNe and IBM lift-off chemoepitaxial processes. In the LiNe process a cross-linked polymer mat is deposited on the substrate and then patterned by photolithography to define the GPs. Then, the interspatial regions where the base polymer was removed after patterning are refilled with a neutral brush layer, continued by self-assembly [140], [141]. On the other hand, in the IBM lift-off process sacrificial features are defined by photolithography, followed by the deposition of a neutral layer and lift-off, leaving exposed areas with neutral brush and areas preferential to one of the BCP blocks [81], [142].

Centering on graphoepitaxial strategies for line-space pitch multiplication applications, the most usual approach is to use topographical GPs in the shape of trenches, balancing the surface free energy between BCP domains and bottom of the trench, while GP walls show stronger affinity to one of the blocks [54], [143], [144]. As result, after performing DSA, domains result perpendicularly aligned to the bottom surface and parallel to the walls. Nonetheless, this methodology presents some disadvantages. First, defects might occur due to local variation of affinity in areas of the sidewall. Second, high-resolution lithography is required for the fabrication of the GPs, as only few lamellae are normally possible to align parallel to the GP walls with low defectivity. Finally, great control in the deposition of the brush layer is needed to only graft it on the bottom of the trench and not on the sidewalls.

In contact-hole patterning cylindrical or lamellar BCPs can be integrated directly into conventional CMOS lithography to generate contact shrinking, contact multiplication or contact uniformity enhancement [40], [98]. Firstly, GPs are pre-patterned using optical

lithography (or EBL), followed by dry etching for their structuring. Afterwards, the surface of the cavity that serves as GP is tuned to be attractive to one of the blocks. Then, the BCP is spin-coated filling the GP and self-assembly is carried out by thermal annealing. Finally, the outermost block is selectively etched away, and the remaining block in the center is used as mask for pattern transfer of shrunk uniform holes [145], [146].

Another interesting application of DSA in nanoelectronics is the fabrication of nanoscale silicon vertical pillars. This has been demonstrated by combining DSA with tone-inversion [147], [148], by sequential infiltration synthesis in BCPs [149], [150], and directly by pattern transfer of the BCP template [151]. As we approach the most extreme semiconductor nodes in terms of scaling, alternative architectures and devices such as vertical GAA FETs or single-electron transistors are entering into discussion [152], which could be potentially fabricated by DSA.

Furthermore, besides DSA for logic, research efforts in BCP technology have lately centered their attention on other emerging areas that were looking for large area nanostructuring techniques. Many of these fields are low-demanding regarding defectivity levels and, in many cases, self-assembly does not require to be directed, but rather takes place on a free surface without guidance. Applications include, but are not limited to, hard-disk drive and magnetic storage devices [147], [153], [154], [155], [156], nanophotonics and plasmonics materials [157], [158], [159], or chemical sensors [160]. Most often, BCPs are still used as templates for patterning, as in the case of graphene structuring [80], [161], [162], [163], the fabrication of nanoporous membranes [164], [165], [166], [167], [168] or energy storage, photovoltaics and batteries [169], [170], [171], [172]. In other applications, however, BCPs can present a more active role and can be used as stabilizing agent, for surface functionalization [173], [174], [175], [176] or to aid in nanoparticle self-assembly [177].

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Chapter 2

Basics of nanomechanical resonators

Similarly to the evolution of microelectronics onto nanoelectronics driven by Moore's Law, the scaling of microelectromechanical systems (MEMS) has also progressed in search of lower costs and improved performance, giving birth to nanoelectromechanical systems (NEMS). In particular, nanomechanical resonators generate significant interest within the NEMS discipline due to their remarkable sensitivity to detect small physical magnitudes.

The aim of this chapter is to give a general presentation of nanomechanical resonators. The most basic theoretical fundamentals of doubly clamped beams are firstly introduced, as they are structures of importance for the devices discussed later on in this thesis. Then, some of the most usual actuation and detection techniques are revised. Finally, a review of nanomechanical resonators for mass sensing is presented.

2.1 INTRODUCTION

NEMS are miniaturized systems that integrate mechanical structures of critical dimensions below 100 nm with transducers and electronics [1], [2]. Although they can be seen as a mere reduced version of MEMS, they also profit from additional characteristics inherent to their small size in terms of weight, power dissipation, speed and precision [3]. Thanks to this, they have become a technology with presence in multiple sectors in applications where structures of very small mass and large surface area-to-volume ratios deliver critical functionality, like mass sensing [4], biological sensing [5], chemical sensing [6], force sensing [7], temperature sensing [8] or high-frequency devices [9].In the future, the NEMS market is expected to expand thanks to the fast development of technological revolutions like 5G, the Internet of Things, wearable electronics, artificial intelligence and virtual reality, where small, low power-consuming sensors will be in need [10].

Nanomechanical resonators are a special type of NEMS that have received significant attention from the scientific community, especially for mass sensing applications [11]. They are resonant devices (cantilevers, beams, strings, plates, membranes) that can transform mechanical disturbances to an electric signal and vice versa via transducers. They are usually driven into resonance and kept under constant vibration by an actuator, while their resonant frequency is monitored by a detection mechanism. An attached or adsorbed mass on the resonator causes a shift in resonant frequency, therefore enabling its detection. Thanks to their reduced size and dynamic characteristics, nanomechanical resonators are able to reach ultra-high and very-high resonant frequencies [12], [13] enabling their use in ultra-sensitive detection.

2.2 THEORETICAL FUNDAMENTALS

If nanomechanical resonators were ideal continuum mechanical structures and energy was added to the system to initiate their oscillation, they would perennially vibrate at a certain frequency known as eigenfrequency or natural frequency (ω_n). At this frequency, kinetic and potential energy would be unceasingly transformed to each other without losses [14].

In real mechanical systems, however, energy conversion is not ideal and energy is dissipated during vibration. Nevertheless, at a certain vibration frequency (resonant frequency, ω_r) the commute between kinetic and potential energy is optimum and losses are minimum. This resonant frequency is typically close to the eigenfrequency and corresponds to a particular vibrational mode, or mode shape [15].

Because nanomechanical resonators are usually operated in resonance, the study of their frequency response in dynamic mode is of great interest. As later on in this thesis silicon doubly clamped beams are a structure of concern, the study here is focused on them.

Dynamic response of the free behavior of a doubly clamped beam by the Euler-Bernoulli beam theory (linear theory of elasticity for small deflections)

For the study of this ideal case, a homogeneous rectangular silicon beam of cross-section area A is assumed, with axis along X, small deflections and negligible rotational inertia and shear deformation (figure 2.1). Therefore, the device can be modeled as a one-dimensional elastic beam with only flexural motion, in other words, only bending along its length.

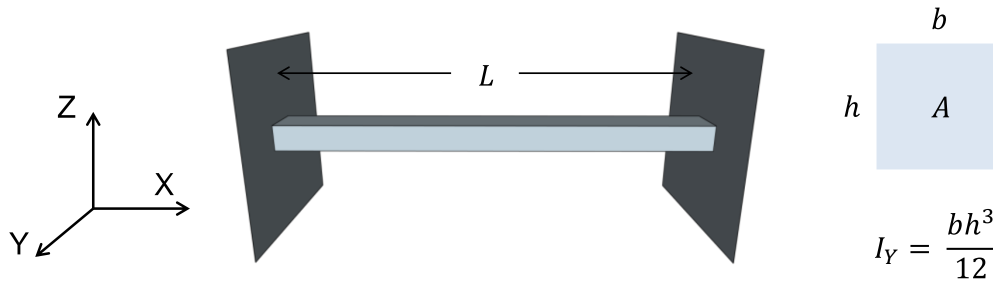

Figure 2.1. Geometry, orientation and dimensions of the doubly clamped beam model used in this study. The value for the moment of inertia I_Y corresponds to a beam of rectangular cross-section.

When the beam is deformed during resonance, the free behavior of the structure can be described by the Euler-Bernoulli beam theory [16], following the differential equation

$$EI_Y \frac{\partial^4 w(x,t)}{\partial x^4} + \rho A \frac{\partial^2 w(x,t)}{\partial t^2} = 0 \quad (1)$$

where $w(x,t)$ is the displacement of the beam at position x and time t, E is Young's modulus, ρ is beam density, A is the cross-section area of the beam and I_Y is the moment of the inertia with respect to Y.

The solution to this equation, which is demonstrated elsewhere [17], yields that the beam has a stable oscillating solution comprised of multiple superposed vibrational modes at determinate eigenfrequencies with different associated spatial mode shapes. The displacement of the resonator can be described as

$$w(x) = A_n cos(\beta_n x) + B_n sin(\beta_n x) + C_n cosh(\beta_n x) + D_n sinh(\beta_n x) \quad (2)$$

where β_n is a dimensionless coefficient known as wavenumber, dependent on the shape of the vibration mode. The terms with the cosine and sine represent the standing waves in the beam center, while the hyperbolic terms represent the influence of the clamping [15].

By combining equations (1) and (2), it is possible to obtain a relationship between the eigenfrequency and the wavenumber in

$$\omega_n = {\beta_n}^2 \sqrt{\frac{EI_Y}{\rho A}} \quad (3)$$

Then, by applying the boundary conditions of a doubly clamped beam (zero displacement and curvature at both clampings) in equation (2), coefficients A_n, B_n, C_n and D_n can be extracted, and equation (2) resumed in

$$\cosh(\beta_n L)\cos(\beta_n L) = 1 \quad (4)$$

rendering the solutions in table 2.1. By introducing these solutions in equation (3), it is possible to obtain the eigenfrequency of each of the vibrational modes of the doubly clamped beam.

TABLE 2.1
ROOTS OF THE FREQUENCY EQUATION OF
A DOUBLY CLAMPED BEAM

n, Mode number	$\lambda_n = \beta_n L$
1	4.7300
2	7.8532
3	10.9956
4	14.1372
5	17.2788
6	20.4204
n	(2n+1) π /2

In figure 2.2, the first three mode shapes of a doubly clamped beam of unitary length are represented from the side.

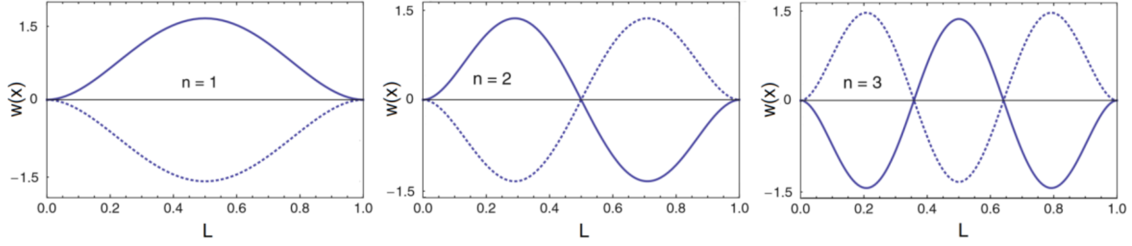

Figure 2.2. Shape of the first three resonance modes of a doubly clamped beam resonator with unitary length L [15].

Dynamic response of the free behavior of a doubly clamped beam by the mass-damper-spring model

Another way to study the vibration of a doubly clamped beam is by reducing the motion of each of its particular points to a basic mass-damper-spring model (figure 2.3). This simplification is useful to study the response near the resonant frequency of a particular mode, but it does not provide any information about resonance parameters, which need to be calculated by the Euler-Bernoulli beam theory, nor takes into account possible coupling between different vibrational modes [18].

In this model, according to Newton's laws, a 2nd order differential equation can describe the system harmonic oscillation as

$$m_{eff}\frac{\partial^2 x}{\partial t^2} + c\frac{\partial x}{\partial t} + k_{eff}x = F \Rightarrow$$
$$\Rightarrow \frac{\partial^2 x}{\partial t^2} + \frac{c}{m_{eff}}\frac{\partial x}{\partial t} + \frac{k_{eff}}{m_{eff}}x = \frac{F}{m_{eff}} \quad (5)$$

where $\mathrm{m_{eff}}$ is the effective mass of the nanomechanical resonator, c is the coefficient of damping, $\mathrm{k_{eff}}$ is the effective spring constant and $\mathrm{F = F_0 \sin(\omega t)}$ is a sinusoidal excitation force externally applied to overcome the damping.

In the ideal case of the free behavior of a system that does not suffer from any damping from the medium ($\mathrm{c} = 0,\ \mathrm{F} = 0$), equation (5) can be simplified to

$$\frac{\partial^2 x}{\partial t^2} + \frac{k_{eff}}{m_{eff}}x = 0 \quad (6)$$

If for this 2nd order system, the eigenfrequency is defined as

$$\omega_n = \sqrt{\frac{k_{eff}}{m_{eff}}} \quad (7)$$

equation (6) can be rewritten as

$$\frac{\partial^2 x}{\partial t^2} + {\omega_n}^2 x = 0 \quad (8)$$

with solution

$$x(t) = x_0 sin(\omega_n t + \alpha) \quad (9)$$

where x_0 is the amplitude of motion and α is the phase, being both determined by the initial conditions.

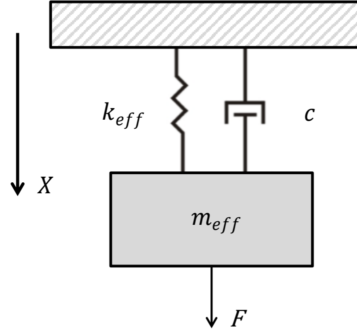

Figure 2.3. Mass-damper-spring model.

The effective parameters can be calculated by the Euler-Bernoulli theory or by comparing the kinetic energies of the Euler-Bernoulli model and the mass-damper-spring model [15]. For a doubly clamped beam displaced by a punctual perpendicular force applied at its center ($w(L/2)$), they adopt the form

$$k_{eff} = \frac{192EI_Y}{L^3} \quad (10)$$

where E is Young's modulus, I_Y is the moment of inertia and L is the length of the beam, and

$$m_{eff} = \frac{192m}{{\beta_n}^4} \quad (11)$$

where β_n is the wavenumber of the particular normal mode and m is the real mass of the beam. The effective mass is used for the calculations in lieu of the real mass of the nanomechanical resonator because not all the mass is under the same vibration [19].

On the other side, if a real system with damping effects and an applied periodic force to overcome them is considered, equation (5) results in

$$\begin{aligned} m_{eff}\frac{\partial^2 x}{\partial t^2} + c\frac{\partial x}{\partial t} + k_{eff}x = F_0 \sin(\omega t) \Rightarrow \\ \Rightarrow \frac{\partial^2 x}{\partial t^2} + \frac{c}{m_{eff}}\frac{\partial x}{\partial t} + \frac{k_{eff}}{m_{eff}}x = \frac{F_0 \sin(\omega t)}{m_{eff}} \end{aligned} \quad (12)$$

If the coefficient of damping is defined as

$$c = 2n_c m_{eff}$$

equation (12) results in

$$\frac{\partial^2 x}{\partial t^2} + 2n_c \frac{\partial x}{\partial t} + \frac{k_{eff}}{m_{eff}} x = \frac{F_0 \sin(\omega t)}{m_{eff}} \tag{13}$$

In this context, a damping ratio can be defined as

$$\zeta = \frac{n_c}{\omega_r} \tag{14}$$

where ω_r is the resonant frequency of the system.

The solution to equation (13) yields an approximate expression for the amplitude of vibration of [14]

$$|z_0| = \frac{\frac{F_0}{m_{eff}}}{\sqrt{(\omega_r - \omega^2)^2 + 4\zeta^2 \omega_r{}^2 \omega^2}} \tag{15}$$

which proves that amplitude is maximum when the frequency of the excitation signal is equal to the resonant frequency of the structure ($\omega = \omega_r$). The relationship between the resonant frequency ω_r of the system and its eigenfrequency ω_n in an ideal undamped state, can be expressed as [19]

$$\omega_r = \omega_n \sqrt{1 - 2\zeta^2} = \omega_n \sqrt{1 - \frac{1}{2Q^2}} \tag{16}$$

where Q is a factor known as quality factor. For very slight damping ($\omega_r \approx \omega_n \approx \omega$) the maximum amplitude can be approximated to

$$|z_0| = \frac{F_0}{2\zeta \omega_n{}^2 m_{eff}} = \frac{F_0}{k_{eff}} Q$$

Quality factor

The quality factor is a key performance indicator for NEMS and represents the amount of losses during operation at resonant frequency [20]. It can be physically defined as

$$Q = 2\pi \frac{Average\ energy\ stored}{Energy\ lost\ per\ cycle} = \frac{m_{eff}\omega_r}{c} = \frac{\sqrt{1 - 2\zeta^2}}{2\zeta} \tag{17}$$

The loss of energy in nanomechanical resonators during resonance occurs through different mechanisms, most importantly due to interactions with the environment (clamping to the substrate [21] and surrounding medium [22]), but also through intrinsic defects in the structure [23].

Experimentally, the quality factor can be calculated by analyzing the frequency response, as the ratio between the resonant frequency and the bandwidth at full-width at half-maximum of the resonance peak (figure 2.4):

$$Q = \frac{\omega_r}{\Delta\omega_{3dB}} \tag{18}$$

For high-sensitivity nanomechanical resonator applications, the goal is to obtain high Q values with minimized losses and low damping. This increases the amplitude at resonance (height of the resonance peak), reduces the bandwidth (width of the resonance peak) and simplifies the setup needed to measure the response [24].

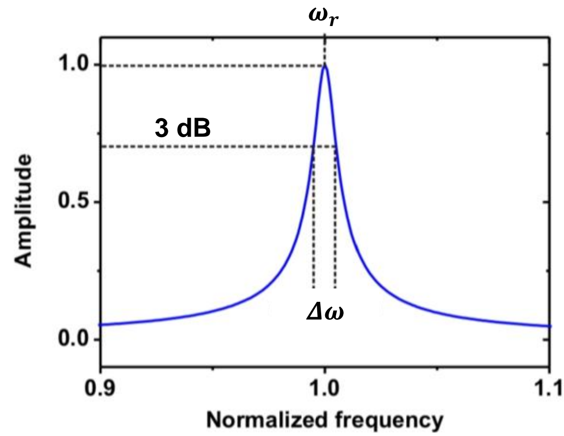

Figure 2.4. Calculation of the quality factor from the frequency response of the resonator [25].

2.3 TRANSDUCTION MECHANISMS

Several transduction strategies can be used to convert electric signals into mechanical energy to actuate a device or by contrary, detect and receive a mechanical stimulus from the movement of a resonator and transform it into a measurable electric signal. In this section some of the most common transduction techniques are described [26].

The scalability of such mechanisms is particularly challenging when devices are reduced in size, as response time and output signals decrease because of the small amplitudes and high frequencies of the mechanical vibrations, along with non-linearities. Due to these factors, fast and very sensitive read-outs are eventually necessary [27], [28].

Electrostatic actuation and detection

Electrostatic actuation systems are one the most extended in the field of nanomechanical resonators thanks to their ease of integration, low power, wide range of conductive materials [29] and wide range of frequencies [30].

The main enabler of this actuation mechanism is the Coulomb force experienced by the electrodes of a capacitor when an electric potential is applied between them. Usually, the nanomechanical resonator is used as one of the electrodes, in parallel to the driving electrode. The potential energy (E_P) stored in the capacitance is

$$E_P = \frac{CV^2}{2} \tag{19}$$

where V is the electric potential between resonator and driving electrode and C the capacitance. The electrostatic force on the resonator yields

$$F_e = \frac{\partial E_P}{\partial x} = \frac{V^2}{2}\frac{\partial C}{\partial x} \tag{20}$$

where $\partial C/\partial x$ is the gradient of the change in capacitance when the nanomechanical resonator vibrates. The capacitance of the system depends on geometry, being the most basic model the case of two parallel plate electrodes (figure 2.5). In this

configuration, the initial capacitance between the two electrodes of area $\mathrm{A} = \mathrm{WL}$ and situated in a medium with relative permittivity ε_r is

$$C_0 = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{21}$$

where ε_0 is vacuum permittivity (8.854188·10^{-12} F/m) and d is the distance between electrodes. Considering that the movement of the nanomechanical resonator varies electrode separation in a distance x, capacitance adopts the form

$$C(x) = \varepsilon_0 \varepsilon_r \frac{A}{d-x} \tag{22}$$

Introducing this expression into equation (20), the electrostatic force on the resonator can be written then as

$$F_e = \frac{V^2}{2}\frac{\partial}{\partial x}(\varepsilon_0 \varepsilon_r \frac{A}{d-x}) = \frac{V^2}{2}\varepsilon_0 \varepsilon_r \frac{A}{(d-x)^2} \tag{23}$$

As generally the amplitude of the motion of the resonator is minuscule in comparison to the gap between electrodes, the force can usually be simplified to

$$F_e = \frac{V^2}{2}\varepsilon_0 \varepsilon_r \frac{A}{d^2} \tag{24}$$

Apart from being an actuation method, electrostatic transduction can additionally be used to detect the vibrational motion of a device. The electric charge stored in the capacitive system adopts the form

$$Q(x) = VC(x) \tag{25}$$

where V is the electric potential between the electrodes and $\mathrm{C(x)}$ the system capacitance, modulated with the vibration of the resonator along the x direction. Changes in capacitance generate a charge variation on the fixed electrode, allowing detection of the vibration of the resonator as a small current I

$$I = \frac{\partial Q}{\partial t} = V\frac{\partial C(x)}{\partial t} \tag{266}$$

Nonetheless, parasitic capacitances can absorb part of the signal and sometimes elaborated readout schemes are necessary to detect this small relative variation of the system capacitance [31].

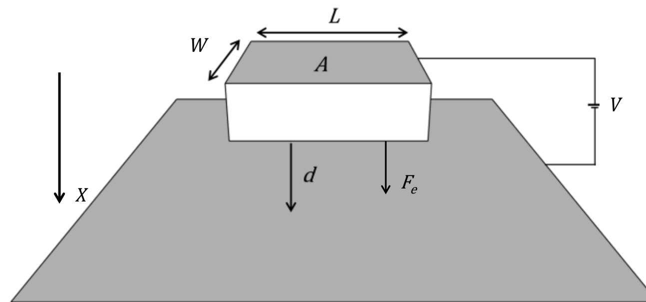

Figure 2.5. Parallel electrode plates with electric potential difference.

Electrodynamic actuation and detection

Electrodynamic transduction is based on the Lorentz force that acts on moving charges under the effect of a uniform magnetic field. It can be used to actuate and detect the motion of nanomechanical resonators such as doubly clamped beams with frequencies up to GHz [15]. Each of the charges comprising the current is subject to the following force

$$\vec{F}_L = q\vec{v} \times \vec{B} \tag{27}$$

where q is charge, $\vec{v}$ is the velocity vector of the charged particles and $\vec{B}$ the magnetic flux density. By merging this formula with the definition of electric current, the total force exerted on a doubly clamped beam through which an electric current is flowing can be obtained:

$$\vec{F} = \frac{nq\vec{v}}{L} \times \vec{B} = L\vec{I} \times \vec{B} \tag{287}$$

where L is the length of the wire, $\vec{I}$ the electric current and $\vec{B}$ the magnetic flux density. The resultant force is perpendicular to the magnetic field and the velocity vector (figure 2.6).

In addition, the Lorentz force acting on each individual charged particle results in their separation within the beam, generating an electric potential along it that can be detected with a network analyzer, known as motional electromotive force (V_{EMF}) [32].

Depending on the dimensions of the nanostructures and the intensity of the magnetic field, relatively high currents are needed to produce forces large enough to be detectable. Consequently, resistivity should be made small, through doping or proper choice of materials, to avoid large voltage drops along the beam that would limit the current [18].

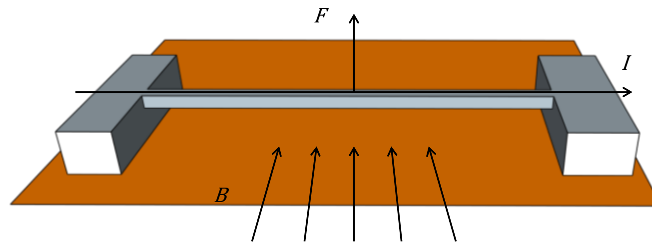

Figure 2.6. Scheme of a configuration to electrodynamically actuate doubly clamped beams.

Piezoelectric actuation and detection

In piezoelectric actuation, dielectric materials that experience mechanical deformation when subject to an external electric field [33] are used to generate mechanical displacement and actuate nanomechanical resonators. Piezoelectric materials include thin films of lead zirconate titanate (PZT) [34], zinc oxide (ZnO) [35], gallium arsenide (GaAs) [36], gallium nitride (GaN) [37] and aluminum nitride (AlN) [38]. The usual setup is a dielectric thin film sandwiched between two metal electrodes that generate an electric field when applying an electric potential difference. This electric field modifies the generalized Hooke's Law and forces the structure out of equilibrium, allowing displacements controlled with great precision [39].

Reversely, the application of mechanical deformation on piezoelectric materials also results in the generation of electric charges that accumulate along the deformed structure, enabling the detection of resonator vibrations [18]. It is common, in fact, to implement simultaneous piezoelectric actuation and detection systems in resonant devices in timing, filtering, or sensing applications [40], [41].

Piezoresistive detection

Piezoresistivity is the variation of electric resistivity in a material when this is subject to mechanical strain. Piezoresistive detection is therefore based on the measurement of changes in resistance of a conductive element, typically known as strain gauge [15], when mechanical strain is applied.

For small elastic strain, piezoresistivity can be considered linear, and the gauge factor of a strain gauge defined as the normalized change in resistance per strain [42]

$$GF = \frac{\Delta R}{R}\frac{1}{\varepsilon} = \frac{\Delta R/R}{\Delta L/L} \tag{29}$$

where $\varepsilon = \Delta L/L$ is strain, ΔL the absolute change in length, L the original length of the strain gauge, ΔR the change in resistance due to axial and lateral strain and R the initial resistance of the strain gauge.

For materials electrically and statically isotropic (resistivity, Young's modulus, and Poisson's ratio constant along all directions), the gauge factor can also be expressed as

$$GF = \frac{\Delta\rho}{\rho}\frac{1}{\varepsilon} + (1 + 2\vartheta) \tag{30}$$

where ϑ is the Poisson's ratio of the material and ρ the resistivity. The first term in this formula is known as strain coefficient of resistivity, and is related to the variation of inter-atomic distance after deformation. The second term is an effect of geometric nature originated from the elongation and thinning of the material under physical strain [43]. In most materials, such as metals, the change in resistivity due to stress is negligible compared to geometrical effects. However, in piezoresistive materials such as semiconductors, variations in resistivity prevail.

In the case of nanoelectromechanical resonators, piezoresistors can be located in areas of large strain (anchors to fixed elements), to maximize the sensitivity of the detection system, or even the resonator structure itself can act as a piezoresistive gauge [44], [45].

Optical detection

Optical detection is an alternative to track the displacement of nanomechanical resonators, particularly in out-of-plane translational vibrations. The use of optical strategies for detection presents certain advantages over other methods such as the inexistence of electric interference, parasitics or physical contact with the device [18].

Optical detection is well extended in AFM, for instance, where a collimated laser beam is focused on top of a cantilever tip and the reflected beam directed to a split photodiode. Deflections result in the displacement of the laser spot from the center of the photodiode, tweaking an output electric current. This method is mostly used with reflective cantilevers, but no so much with doubly clamped beams [15].

Most usual options for the optical sensing of these are optical interferometry methods, like Fabry-Pérot and Michelson interferometry, based on wave interference (figure 2.7) [26]. In them, a laser beam is directed at the resonant surface and reflected creating interference patterns due to phase differences. By analyzing these fringes and their evolution, nanoresonator movement can be determined.

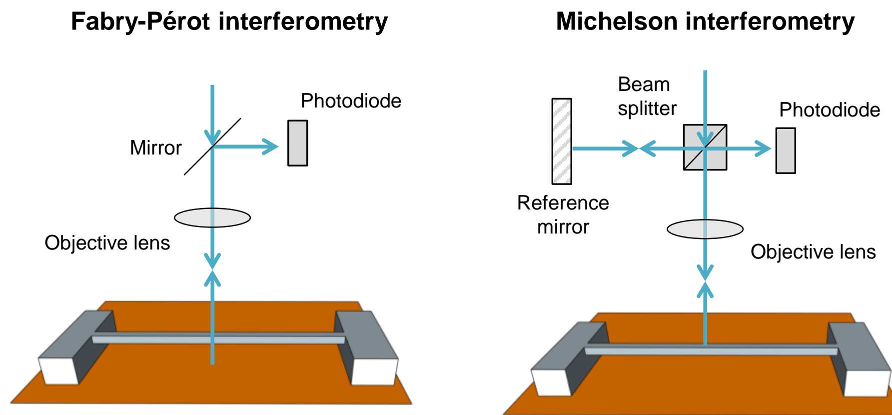

Figure 2.7. In Fabry-Pérot interferometry, a laser beam is focused on the resonator and the reflected light is collimated through the same lens and directed onto a photodiode. In Michelson interferometry, the reflected light interferes with a reference beam created by a beam splitter and a reference mirror [26].

2.4 NANOMECHANICAL RESONATORS FOR MASS SENSING

In this section a brief review about nanomechanical resonators in the particular field of mass sensing is presented, including some relevant milestones and representative references.

Nanomechanical resonators present very high resonant frequencies, high quality factors and reduced masses, all desirable attributes for the fabrication of mass sensors and spectrometers of ultrasensitive responsivity [23]. Once a particle is adsorbed, the effective mass of the resonator increases, generating a shift in the resonant frequency of the system, which enables mass detection.

The manufacturing of these devices relies on the same techniques developed for nanoelectronics, therefore they have also significantly benefited from advances in nanofabrication, with special focus on miniaturization. Top-down and bottom-up approaches have been used by researchers to fabricate the smallest resonators possible in order to measure the smallest detectable masses.

Micromachined resonant mass sensors with high mass sensitivities were firstly demonstrated in the 1990s [46] and early 2000s [47]. In 2003, Lavrik et al. proved femtogram-level (10^{-15} g) mass detection with gold-coated silicon cantilevers of resonant frequencies around 1 to 6 MHz in air [48]. In 2004, Ilic et al. reported the fabrication of poly-Si and silicon nitride nanocantilevers with eigenfrequencies from 1 to 15 MHz, that showed attogram (10^{-18} g) mass sensitivity [49].

The work of Professor Roukes' group at Caltech deserves distinctive attention, as they served as pioneers for the first generations of NEMS [2], [23], [32], [50], [51]. In 2004 they demonstrated attogram-scale mass sensitivity with doubly clamped beams fabricated out of Al-coated SiC that adsorbed gold atoms in ultra-high vacuum [4]. Later, in 2006, they reported a doubly clamped SiC beam with resonant frequency of 133 MHz that was able to attain zeptogram (10^{-21} g) resolution when adsorbing Xe atoms [52].

During the last fifteen years, the number of mass-sensing devices in literature fabricated by top-down techniques has become enormous, including cantilevers [53], [54], [55], doubly clamped beams [56], [57], [58] and other alternate shapes and forms [59], [60], [61] to measure the masses of nanoparticles or atoms [62], [63], proteins [64], viruses [65] and biomolecules [66], [67], [68]. All of these devices have been fabricated by standard micro/nanofabrication processes such as deposition and growth of thin films; pattern definition by optical lithography, EBL or focused ion beam implantation [69], and dry or wet etching [18]. Developments in each of these three main steps have generated technological advances that have enabled the miniaturization and transformation of MEMS into NEMS.

On the other side, bottom-up nanofabrication approaches using atoms or molecules as aggregated blocks have also been developed, and nanotubes and nanowires grown by bottom-up techniques have drawn a lot of attention in the field. In these devices, dimensions are not limited by lithography, etch roughness or the synthesis of epitaxially grown substrates, and they show remarkable mechanical and electrical properties, which make them attractive to work at ultra-high resonant frequencies (up to the GHz range) [12], [26]. However, these new materials and devices present certain drawbacks related to their synthesis and integration with conventional top-down microfabrication [70].

Some of the first nanowire nanomechanical resonators fabricated by bottom-up techniques were reported by Roukes' group in 2003, with devices based on doubly clamped platinum nanowires. Nanowires were 43 nm in diameter and 1.3 µm in length, with a resonant frequency of 105.3 MHz [13].

An example of a fruitful bottom-up technique for the fabrication of nanomechanical resonators based on nanowires is the growth of silicon nanowires from catalytic gold nanoparticles by the vapor-liquid-solid growth mechanism. Several works, including some authored by members of our research group, have demonstrated the possibility of using gold nanoparticles as seeds to grow doubly clamped silicon beams or cantilevers at predetermined positions, that can be used as mass sensors [71], [72], [73], [74].

On the other hand, carbon nanotubes (CNTs) are popular bottom-up structures for mass and force sensing, as firstly proposed by Poncharal et al. in 1999 [75]. CNTs hold all the mass and force sensitivity records thanks to their extreme properties: low density, ultra-small cross-section, high Young modulus (1 TPa), low defectivity and surface without dangling bonds [76], [77].

Some of the first CNT resonators were reported by Sazonova et al., presenting nanotubes of 1-4 nm in diameter grown by chemical vapor deposition, with resonant

frequencies between 3 and 200 MHz [78]. In 2005, Nishio et al. demonstrated a nanotube cantilever for zeptogram-level (10^{-21} g) mass detection using the focused electron beam of a SEM [79]. Later, in 2006, a CNT resonator with a diameter of 3.5 nm and 300 nm of length was reported by Peng et al., reaching mass sensitivity resolution of attograms (10^{-18} g) at room temperature, with a resonant frequency over 1.3 GHz [80]. Lassagne et al. reached 1.4 zeptograms ($1.4 \cdot 10^{-21}$ g) of mass resolution by measuring chromium atoms deposited on a CNT of 1 nm of diameter at cryogenic temperatures, in a paper published in 2008 [81]. Almost simultaneously, researchers at Berkeley and Caltech reported atomic-resolution nanomechanical mass sensors based on CNTs showing mass sensitivities of $1.3 \cdot 10^{-21}$ g [82] and $0.085 \cdot 10^{-21}$ g [83], respectively. In 2012, mass sensitivity resolution of 1.7 yoctograms ($1.7 \cdot 10^{-24}$ g) was reported, using a 150-nm long CNT nanoresonator with a diameter of 1.7 nm that vibrated at almost 2 GHz [84].

Nevertheless, read-out setups to successfully transduce the mechanical motion of CNTs into a measurable electric signal are usually complicated [85], [86] and even require experiments to take place at low temperatures [87].

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Chapter 3

Self-assembly of PS-b-PMMA and pattern transfer

The work exposed in this chapter summarizes the optimization of a fabrication process that consists in the self-assembly of PS-b-PMMA and its pattern transfer onto silicon and silicon oxide substrates by dry etching. Sequential infiltration synthesis of PS-b-PMMA was performed and the possibility of using infiltrated samples as mask for silicon etching was demonstrated. Furthermore, self-assembly of PS-b-PMMA was successfully directed within topographical guiding patterns fabricated by optical lithography and silicon fins perpendicularly oriented to their walls were obtained.

3.1 INTRODUCTION

Basics of dry etching

Dry etching is one of the most essential processes in semiconductor manufacturing, as it is an extended technique to anisotropically remove material (in a preferred direction). Reactive ion etching (RIE) is a type of dry etching that consists in the generation of chemically reactive plasma inside a vacuum chamber and the acceleration of those active radicals and ions towards the substrate.

Classical RIE systems generate the plasma capacitively, in tools that are typically referred to as RIE, as well. Gases enter the chamber under vacuum and a radio frequency (RF) voltage is applied between anode and cathode plates at 13.56 MHz, generating collisions between ionized electrons and the gas ions. A capacitor connected between anode and RF source creates a difference of electrical potential, generating an electric field that propels the ions towards the negatively charged chuck containing the sample [1].

Other systems generate the plasma in an inductively coupled plasma (ICP) setup. These tools are usually referred to as ICP-RIE. Inside them, the plasma is generated by a time-varying RF delivered by a changing magnetic field. A large coil encloses the chamber generating a magnetic field that induces an electric field. This electric field tends to circulate the plasma in the plane parallel to the plates and ions are then accelerated like in a regular RIE tool. Figure 3.1 represents two schemes of RIE and ICP-RIE tools. This combination of RIE with an ICP power source gives the possibility to independently control ion density in the plasma (by ICP, RF1) and the acceleration voltage in the direction of the substrate (by RIE, RF2) [2]. In this chapter both RIE and ICP-RIE instruments have been used.

Although the most important parameters in ICP-RIE processing are the chemistry used and the ratio between gases, it is necessary to tune plasma and acceleration powers to favor either a more chemically or physically active etching process [3]. Increases in

plasma power increase the amount of interactions and ions generated, by result giving more importance to the chemical aspect of the etching, whereas an increase in acceleration power favors the milling side of the attack. Both powers need to be adjusted to avoid excessive stress of the mask and keep selectivity high.

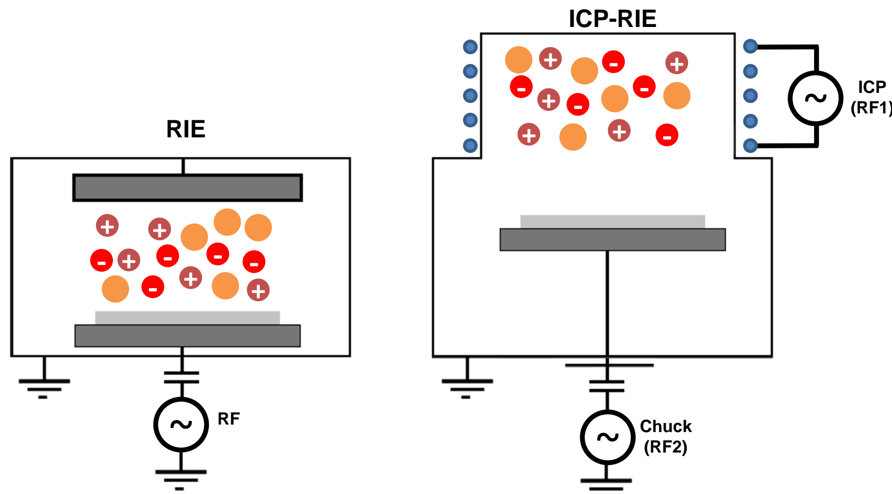

Figure 3.1. Schemes of RIE based on capacitively coupled plasma (left) and inductively coupled plasma (right).

Bosch process for silicon etching

Two different methodologies can be distinguished in the dry etching of silicon: unpassivated or passivated. Unpassivated etch chemistries are simpler, as only etch agents are introduced in the chamber. Eventually, multiple gases can be combined and introduced simultaneously, varying the etching mechanisms of the process and changing the etch rates (e.g. SF_6, CF_4, O_2 [4]), but still remaining an unpassivated event. The main weakness of unpassivated silicon etches is their poor anisotropy, as a significant amount of ions laterally etch the sidewalls [5].

On the contrary, passivated etch chemistries employ some other gases that interact with the exposed silicon sidewalls and create a passivation layer, leading to higher anisotropy. Furthermore, this passivation agent can be introduced in alternated pulses with the etch gas (pulsed-mode etch) or simultaneously with it (mixed-mode etch).

One of the most common passivated etch chemistries for silicon etching is the Bosch process [6], which happens to be a pulsed-mode etch. In the process, silicon is alternatively etched by SF_6 and then passivated by C_4F_8. SF_6 is injected into the chamber, ionized and propelled towards the silicon substrate, generating SiF_4 as etch product. In the following pulse, C_4F_8 is also introduced, ionized and accelerated, producing an inhibition polymer layer of different CF_x species (mostly CF_2 [7]) all over the substrate. This CF_x layer avoids the chemical reaction of SF_6 with silicon. Thanks to the mechanical component of the etching process, when SF_6 ions hit horizontal surfaces of the sample, CF_x is removed and silicon etched away, without affecting the still protected lateral walls.

Block copolymer templates for dry etching

Three different approaches can be used to transfer block copolymer templates to an underlying substrate by dry etching techniques: a direct pattern transfer, the pattern transfer onto a hard mask for further etching, and the use of sequential infiltration synthesis (SIS).

The first approach, and the simplest, consists in the selective removal of one of the blocks of the BCP and the use of the remaining blocks directly as mask. When these are organic blocks, they usually do not offer good etch resistance, which results in a rapid consumption of the mask that limits depth and width of the obtained structures. As mentioned in chapter 1, the incorporation of inorganic segments into block copolymers addresses this issue, but brings difficulties in the control of wetting morphologies in the air/film and film/substrate interfaces [8], [9].

Another extended approach to avoid etch resistance limitations is the transfer of the BCP pattern onto a hard mask, like silicon antireflective coating/spin-on-carbon (SiARC/SOC), to enable deeper substrate etching [10], [11].

Finally, in a third method, it is possible to transform one of the polymer blocks into a different material by SIS, obtaining higher etch contrast between the BCP components. In this technique, an atomic layer deposition (ALD) precursor of a metal oxide is nucleated and selectively grown within the blocks of the thin film that present certain functional groups, converting them into a polymer-inorganic hybrid material with larger etch resistance [12], [13]. One example is the selective infiltration of PS-b-PMMA using trimethyl-aluminum (TMA) to transform PMMA into an alumina-like material [14].

3.2 SELF-ASSEMBLY OF PS-b-PMMA AND PATTERN TRANSFER ON A FREE SURFACE

Deposition and self-assembly process

Experiments in the absence of guiding patterns (self-assembly on a free surface) were carried out using lamellar and cylindrical PS-b-PMMA diblock copolymers of different natural pitches: L_0 = 37 nm (lamellar), L_0 = 30 nm (lamellar) and L_0 = 36 nm (cylindrical) nm. Block copolymer materials were supplied by the chemical company Arkema S.A. (France), under tradename Nanostrength® EO. Their properties are shown in table 3.1.

Two different starting substrates were used. On one hand {100} silicon (p-type, 4-40 Ω·cm) chips, bearing a native silicon oxide layer; on the other hand, the same silicon chips with 12 nm of silicon oxide deposited by plasma-enhanced chemical vapor deposition (PECVD) on top. All chips were approximately 2 × 2 cm^2.

Prior to brush grafting, sample surface was cleaned in acetone and isopropanol (IPA) and activated by oxygen plasma for 5 minutes at 500 W and 600 sccm O_2 flow. Then, a 1.5 wt. % propylene glycol methyl ether acetate (PGMEA) solution of a random copolymer brush (PS-r-PMMA) was spin-coated at 1500 rpm on the top of the surface and annealed for 5 min at 230 ºC inside a tube furnace with nitrogen atmosphere.

Two different random copolymer PS-r-PMMA solutions were employed, with different PS content, depending on whether the PS-b-PMMA was lamellar or cylindrical. In the case of lamellar block copolymers, a brush layer containing 60% of PS ($PS_{60\%}$-r-PMMA, NL2 R60) was used to ensure self-assembly took place in vertical lamellae. On the other hand, when working with the cylindrical block copolymer, a brush layer containing 70% of PS ($PS_{70\%}$-r-PMMA, NL1 R70) was used to ensure PMMA cylinders self-assembled vertically with respect to the PS matrix.

TABLE 3.1

PROPERTIES OF PS-b-PMMA DIBLOCK COPOLYMERS USED IN THIS SECTION

Morphology	Pitch, L_0 (nm)	Molecular weight (kg/mol)	PS weight (%)	PMMA weight (%)
Lamellar	37	79	50	50
Lamellar	30	61.2	47	53
Cylindrical	36	67.1	71	29

After annealing, the non-grafted PS-r-PMMA was removed by repeatedly spin-coating PGMEA on the chips for 90 seconds. The thickness of the remaining brush film still anchored to the surface after this PGMEA rinse was ~8 nm.

Finally, a 2 wt. % PGMEA solution of the corresponding PS-b-PMMA was spin-coated at 2000 rpm for 30 seconds and annealed for 10 minutes inside a tube furnace with nitrogen atmosphere. Lamellar block copolymers were annealed at 265 ºC, while the cylindrical BCP was annealed at 230 ºC. For higher temperatures partial degradation was observed. Final combined BCP and brush thickness was measured by an optical-measurement system (Nanospec AFT/4150, Nanometrics, USA) as function of speed of BCP spin-coating, as exposed in table 3.2. Top-view images of the obtained self-assembled thin films are shown in figure 3.2, with identical results on silicon and SiO_2 substrates.

TABLE 3.2

PS-b-PMMA 2% FILM THICKNESS (INCLUDING BRUSH) AND CORRESPONDING SPIN-SPEED

Speed (rpm)	Thickness (nm)
1500	67
2000	57
2500	54

Self-assembly was also optimized at wafer level, with annealings performed on a hot plate instead of a tube furnace, attaining microphase separation even in the absence of a nitrogen flow. Spin-coating 700 µl of 2 wt. % PGMEA solution of PS-b-PMMA at 2000 rpm for 1 min resulted in reproducible thickness values between 48 and 55 nm in the edge and center of the wafer, respectively (6.3% of uniformity, 1.67 nm of standard deviation and 51 nm of mean value).

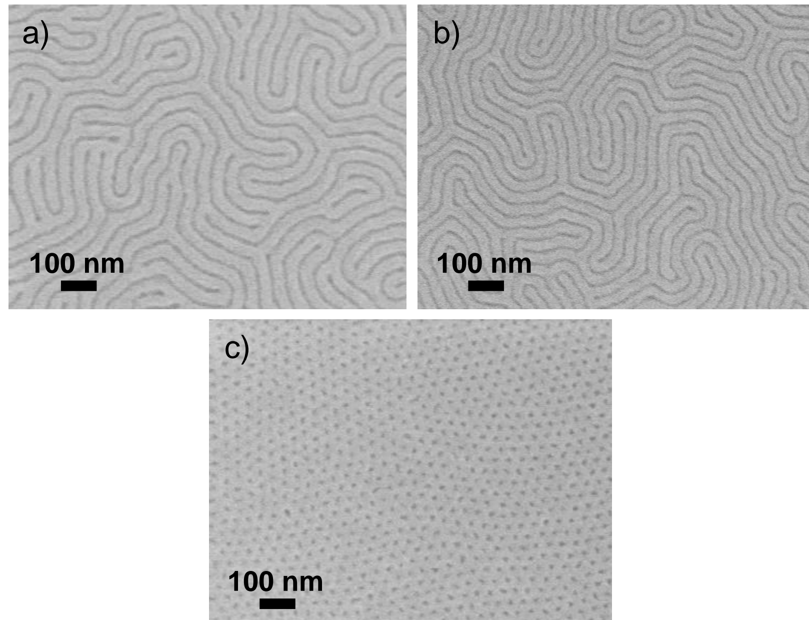

Figure 3.2. SEM top-view micrographs of self-assembled lamellar and cylindrical PS-b-PMMA. a) L_0 = 37 nm, b) L_0 = 30 nm, c) L_0 = 36 nm.

Selective removal of PMMA

When using PS-b-PMMA as mask for dry etching, the most usual approach is to first selectively remove PMMA by RIE, although its wet development in acetic acid after ultraviolet or electron-beam exposure is also possible [15]. Different gases have been tested in literature to selectively remove PMMA, such as oxygen [16], Ar/O_2 [17], CO/Ar [18] and O_2/CHF_3 [19] mixtures. The recipes in this thesis were carried out in Ar/O_2 plasma due to gas availability reasons.

Ar plasmas show much more mild etching rates of PS than pure O_2 [20]. However, to suppress possible variations in PMMA etch rates with time due to oxygen depletion, this can be added to Ar plasma in small percentages to avoid losing selectivity with respect to PS [21], [22]. Both PS and PMMA are organic materials and selectivity in their dry etching is based on carbon content: the higher the carbon content, the more resistant to ion bombardment [23]. As PS has higher carbon content, it is more durable as compared to PMMA monomer units. Also, benzene rings in PS render more etch resistance as compared to PMMA [24].

Figure 3.3 illustrates the evolution of PMMA removal with etching time in the developed RIE process. The initial combined thickness of PS-b-PMMA (L_0 = 30 nm) and brush was 57 nm for the four samples. Each one was then processed in a 5000Mark II RIE (Applied Materials, USA), with the parameters exposed in table 3.3. It is important to point out that the recipes in this thesis can serve as a guide but may not be completely reproducible in other tools and setups, where other parameters can lead to similar plasma conditions.

For an effective pattern transfer, PMMA domains and brush under them need to be entirely removed. This is a necessary condition for two reasons: first, to ensure that all areas of the Si substrate start etching at the same time so that features are uniform;

and second, to avoid unnecessary stress and consumption of the PS mask when trying to etch remnants of residual brush.

Experimental attack times were observed to be larger than the estimated opening times for PMMA. This was due to the higher etch resistance of the brush with respect to the block copolymer. PMMA is etched more easily than the brush layer which, in the case of the samples in figure 3.3, ($PS_{60\%}$-r-PMMA, NL2 R60) contained a 60/40 ratio of PS/PMMA. As a result, and despite having cleared all the PMMA, some extra etching time was necessary to open the brush layer, therefore also etching and stressing the PS mask. Conducting the self-assembly with thinner brush layers would have resulted in an easier complete removal. At 1.5 wt. % concentration, the neutral layer thickness was ~8 nm, whereas the same neutral layer at 0.25 wt. % is expected to be around 3 nm [25].

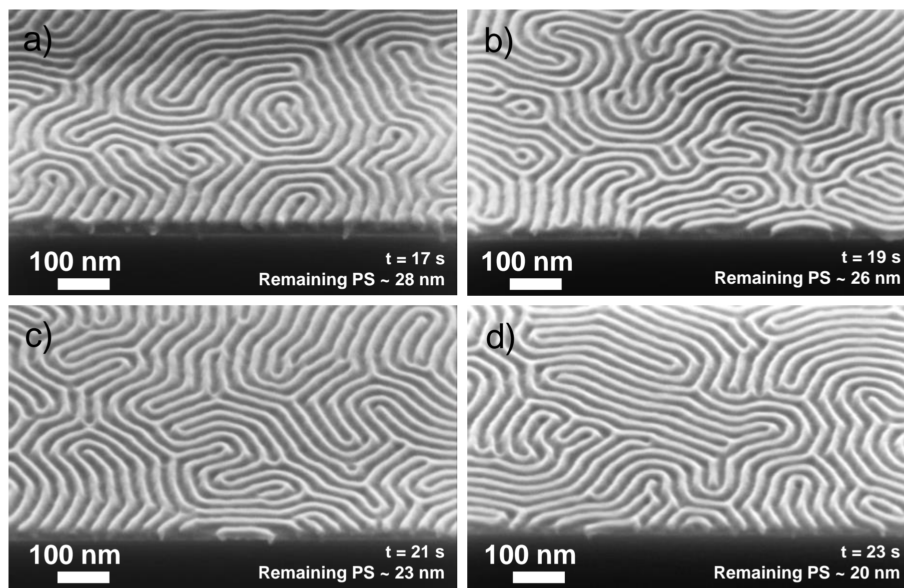

Figure 3.3. SEM tilted (30º) micrographs of four samples after PMMA removal in Ar/O_2 plasma. Initial BCP thickness was 57 nm. Processing parameters were the same (table 3.3) except for etching time (shown as insets). Samples a), b) and c) are not open to the silicon surface. In sample d) however, PMMA and brush have been completely removed, enabling the pattern transfer onto the substrate.

Table 3.4 shows details of an equivalent selective PMMA removal process, but performed in an ICP-RIE tool (AMS 110DE, Alcatel, France) instead. In this case two different powers can be distinguished: the ICP power that generates the plasma (RF1) and the chuck power that accelerates the ions towards the substrate (RF2).

TABLE 3.3

PROCESS PARAMETERS FOR SELECTIVE PMMA REMOVAL IN PS-b-PMMA BY RIE

T (ºC)	P (mTorr)	O_2 (sccm)	Ar (sccm)	RF (W)	PMMA etch rate (nm/s)	PS etch rate (nm/s)	PMMA:PS selectivity
20	30	4	80	25	~2.6	~1.6	1.6:1

TABLE 3.4
PROCESS PARAMETERS FOR SELECTIVE PMMA REMOVAL IN PS-b-PMMA BY ICP-RIE

T (ºC)	P (Pa)	O_2 (sccm)	Ar (sccm)	RF1 (W)	RF2 (W)	PMMA etch rate (nm/s)	PS etch rate (nm/s)	PMMA:PS selectivity
20	1.33	10	200	200	5	~1.5	~0.6	2.6:1

Pattern transfer onto silicon by a mixed-mode Bosch process

The use of PS-b-PMMA for nanostructuring presents two particular challenges. One is the removal of PMMA with high enough selectivity to PS, as explained in the preceding section. The other one is that the remaining PS must be strong enough to survive the etching of the underlying material. It is common with organic BCPs to transfer the pattern to a hard mask of high etchant selectivity, although in the work exposed here the silicon substrate was directly attacked with the PS mask after PMMA removal, as it was simpler. To do so, a mixed-mode process based on the Bosch process [26] was used.

The Bosch process is a very well-established method for deep silicon etching, but not optimum for nanoscale structures due to scalloping and undercutting effects [27], [28]. In order to avoid the impact on the walls caused by the alternating cycles and a precipitated etch rate of the mask, its mixed-mode variation is an interesting alternative. By employing the same chemistry as in pulsed mode, SF_6 and C_4F_8 can be concurrently introduced into the chamber. Despite simultaneous passivation, etching of the horizontal surfaces in the sample prevails thanks to the milling component, and the passivating polymer chains of CF_2 are removed faster than deposited. In the meantime, walls are kept under a passivation layer, producing smooth profiles, slow etch rates and low undercutting and chopping effects [29], [30].

Process parameters are exposed in table 3.5. The main goal behind the use of high source power to generate the plasma is to favor the chemical aspect of the process. By increasing RF1, more fluorine ions are created by SF_6 ionization. Nevertheless, there is a maximum value (1200 W), from where increases in power generate so many passivation ions, that chemical etching cannot be preferential anymore [29]. At the same time, chuck power (RF2) is kept at the lowest value (10 W) that enables removal of CF_2 from horizontal surfaces. Higher values can improve anisotropy but might destroy the weak mask and lead to local heating and reflow of the block copolymers, increasing line roughness [22]. This combination of conditions potentiates selectivity and reduced milling and mask wear.

TABLE 3.5
PROCESS PARAMETERS FOR PATTERN TRANSFER ONTO Si BY ICP-RIE

T (ºC)	P (Pa)	SF_6 (sccm)	C_4F_8 (sccm)	RF1 (W)	RF2 (W)	Si etch rate (nm/s)	Si:PS selectivity
20	2	30	30	1200	10	~2.3	2.5:1

Other alternatives to increase fluorine ions for the set plasma power are to increase the ratio of etchant to passivation gas (SF_6:C_4F_8) or pressure in the chamber. Elevated pressures, however, can lead to instabilities in the plasma, and too-high gas flows can cause scattering between the ions, hindering the etching. In the available ICP-RIE tool, 30 sccm of SF_6 and 30 sccm of C_4F_8 was a reasonable starting point. Very small fluctuations of gas flow rates considerably influence the profile of the structures and even the possibility of performing the etching, as shown in figure 3.4, so the process window is small. These important alterations may be related to variation in etch product removal rate, which is critical in nanoscale topography [31].

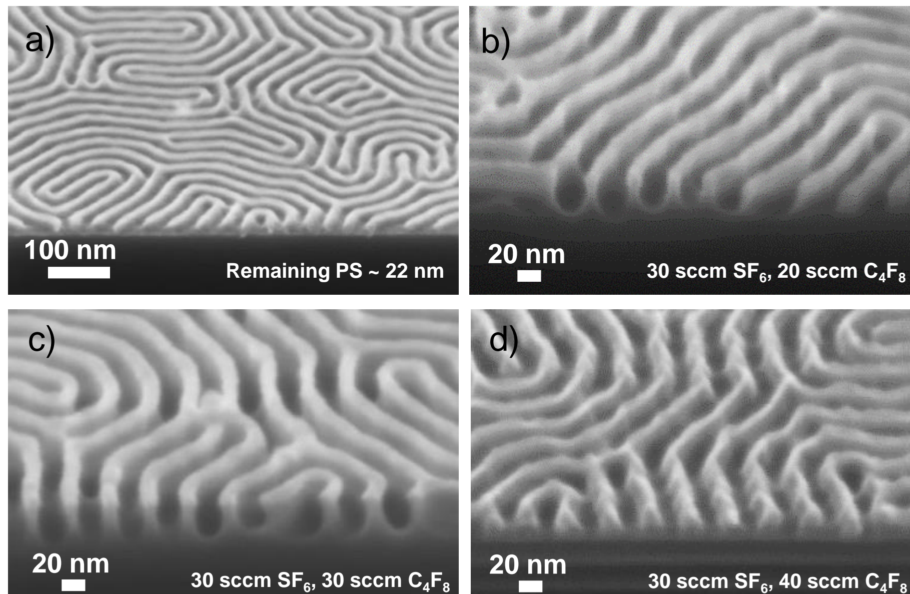

Figure 3.4. Influence of the flux of passivation gas C_4F_8 during mixed-mode Bosch etching of nanostructures. In a), PS-b-PMMA of L_0 = 30 nm was self-assembled on a silicon sample and PMMA selectively removed by ICP-RIE. The chip was then divided into three pieces, where Si was etched with the same power but different SF_6:C_4F_8 ratios for 14 seconds (b, c, d). The higher the SF_6:C_4F_8 ratio, the more isotropic the etching (b). If the flow of C_4F_8 is too high, milling is not large enough to overcome passivation, disabling the possibility of transferring the pattern (d).

This recipe is also very sensitive to complete brush removal and PS mask thickness, as exemplified in figure 3.5. Here, three different examples of pattern transfer are illustrated using the same mixed-mode process. The images on the column on the left (a, b, c) display the initial sample after PMMA removal, with the remaining PS mask thickness as an inset. The images on the right (d, e, f) show their respective pattern transfer in an ICP-RIE process with the parameters detailed in table 3.5. The three samples were etched under identical conditions for 13 seconds.

Successful pattern transfer was only achieved in sample e), thanks to the brush layer being totally removed in b). The brush layer in sample a), however, was not completely etched away, blocking the transfer to silicon. PS in sample c) was over-etched during PMMA removal and the mask was too weak to withstand the mixed mode Bosch process.

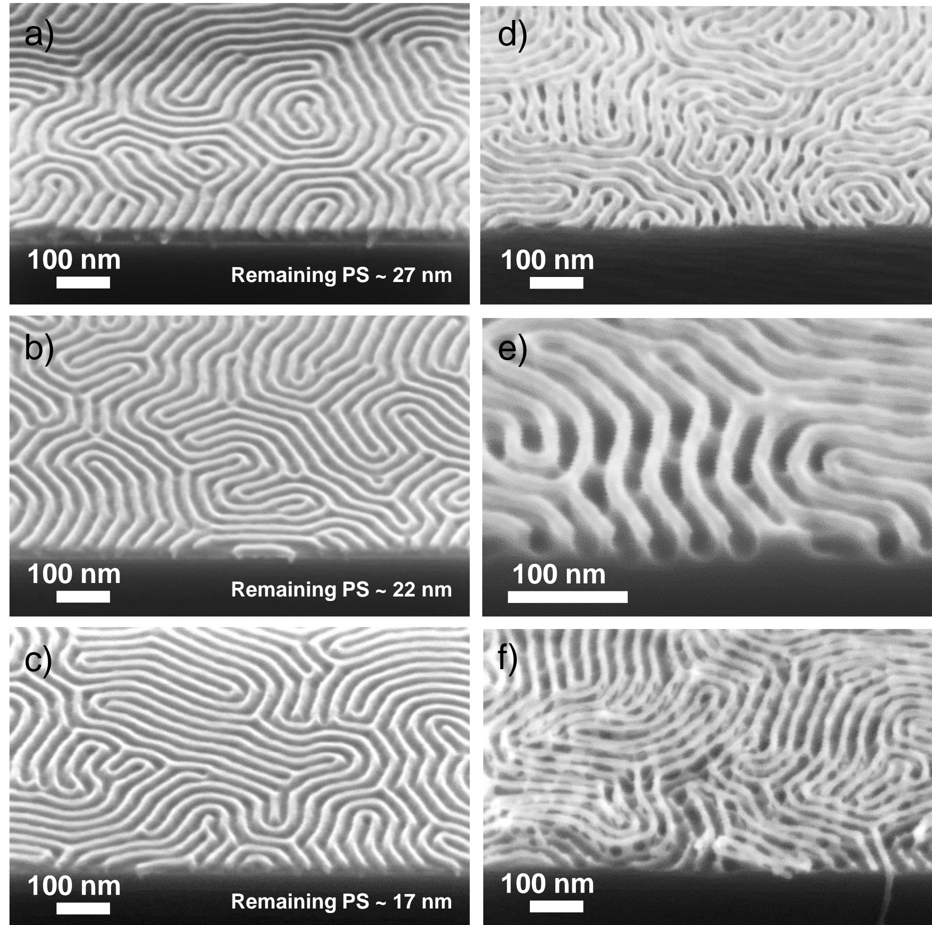

Figure 3.5. SEM tilted (30º) micrographs of three samples after pattern transfer. Samples on the left column show the PS mask thickness after PMMA removal (a, b, c). Images on the right column (d, e, f) show those samples after a mixed-mode Bosch process in an ICP- RIE tool for 13 seconds. Successful pattern transfer was only achieved in sample e).

An example of fruitful pattern transfer onto silicon is demonstrated in figure 3.6, where silicon fins of ~33 nm in height and ~11 nm in width were achieved. After silicon etching, the chip was processed in O_2 plasma to descum remains of PS. Width of the obtained structures is smaller than BCP chain length and half of the natural pitch (L_0 = 30 nm) due to a sidewall-bowing effect that can be explained by several factors [32]. Firstly, the interphase between PS and PMMA domains after self-assembly is not a radical frontier, but presents a gradient of composition in the range of 0 to 5 nm [33], therefore some varying etch resistance may be expected. Secondly, when etching nanostructures so densely packed, electric field gradients can cause ions to be deflected towards the sidewalls, varying species density and causing lateral etching [31]. Thirdly, re-deposition of neutral polymeric components might occur on the sidewalls of such narrow trenches, generating diffusion limitations and impeding their correct passivation [34].

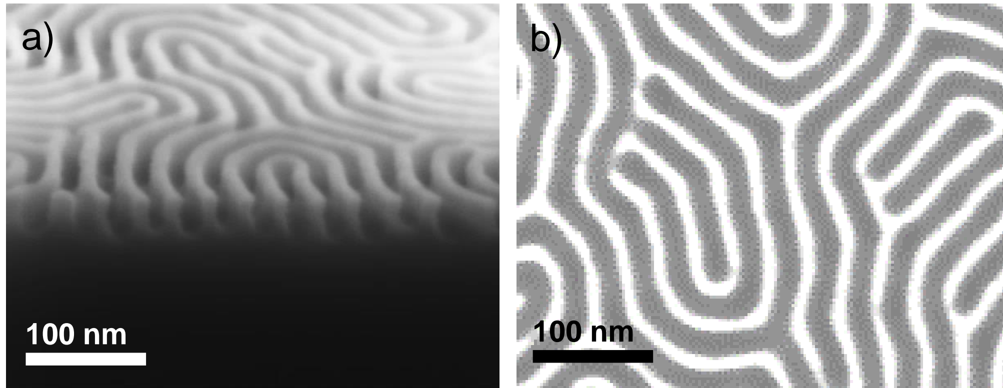

Figure 3.6. SEM tilted (30º) (a) and top-view (b) micrographs of silicon nanostructures obtained after pattern transfer of PS-b-PMMA (L_0 = 30 nm). Obtained fins are ~33 nm in height, and ~11 nm in width.

Pattern transfer onto silicon oxide

A recipe to anisotropically transfer PS-b-PMMA templates onto silicon oxide has also been demonstrated, based only on C_4F_8. The gas serves as simultaneous etchant and passivation gas, in a process similar to the mixed-mode Bosch process for silicon etching described before.

Once PMMA blocks are selectively removed from the self-assembled PS-b-PMMA and only the PS mask is left, C_4F_8 is injected into the chamber of the ICP-RIE and ionized into fluorine and carbon ions, which are accelerated towards the sample surface. There they combine with the SiO_2 atoms of the substrate, generating the volatile byproducts SiF_4 and CO_2, while passivating the sidewalls of the nanostructures with CF_2 [29].

Starting oxide substrates were {100} silicon chips of 2 × 2 cm^2 where 12 nm of SiO_2 had been deposited by PECVD. After self-assembly of a 37-nm-pitch PS-b-PMMA and selective PMMA removal in Ar/O_2 plasma following the recipes explained so far, a mask of 22 nm of PS still remained on the SiO_2 surface. The pattern was subsequently transferred through the silicon oxide layer down to the underlying silicon using only C_4F_8 for 10 seconds. Processing parameters and etch rate were determined experimentally and are shared in table 3.6. Figure 3.7 showcases the resulting transfer.

TABLE 3.6
PROCESS PARAMETERS FOR PATTERN TRANSFER ONTO SiO_2 BY ICP-RIE

T (ºC)	P (Pa)	C_4F_8 (sccm)	RF1 (W)	RF2 (W)	SiO_2 etch rate (nm/s)	SiO_2:PS selectivity
20	2	45	450	60	~1.4	1.2:1

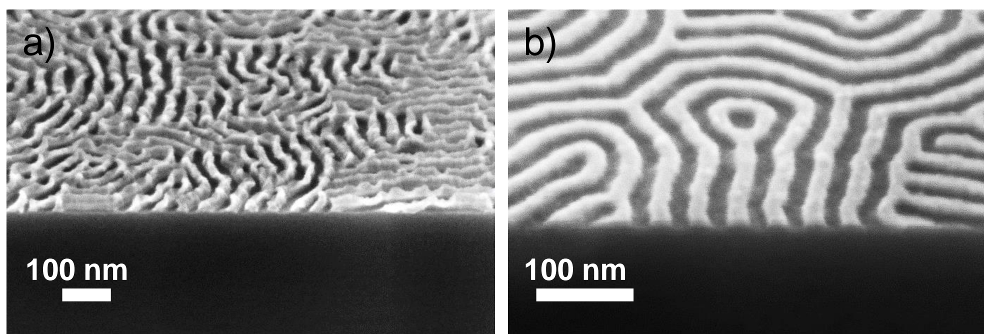

Figure 3.7. SEM tilted (30º) micrographs of the pattern transfer of L_0 = 37 nm PS-b-PMMA onto SiO_2. Image a) was captured right after C_4F_8 etching and shows that not all the PS mask was consumed. Micrograph b) is the same sample after having applied oxygen plasma to remove mask residues. The 12 nm of SiO_2 were pierced and silicon underneath was reached.

Pattern transfer onto silicon after SIS

As already discussed, SIS is a method based on ALD, used to increase the etch resistivity of thin films to a variety of plasma etching chemistries [35]. In this set of experiments, after grafting a random PS-r-PMMA brush onto silicon chips, followed by self-assembly of PS-b-PMMA (cylindrical L_0 = 36 nm and lamellar L_0 = 30 nm), several ALD cycles of gas-phase TMA and water were repeated to infiltrate the PMMA domains with Al_2O_3.

During this process, TMA and water vapor are introduced in sequence in the reactor, intercalating purging steps of inert gas to remove unreacted molecules and by-products [36]. TMA diffuses through the BCP free volume and alumina grows selectively in the whole PMMA domains thanks to chemical interactions between TMA and the oxygen atom in carbonyl groups (C=O) along the PMMA chains [35], [37], [38]. In PS, however, the reactive sites are not C=O groups (inexistent), but defects of hydroxyl groups, with alumina growth occurring at a much slower pace and only within the subsurface [39], [40], [41]. The excess TMA vapor is pumped away in a purging step and H_2O vapor is introduced to finish the reaction forming aluminum oxide only where PMMA is present [42].

Infiltration parameters are resumed in table 3.7 and processes were performed in a Savannah-100 tool (Cambridge Nanotech, USA) in Lund Nano Lab (Lund University, Sweden). By tuning process parameters, especially the number of cycles [43] and time of purge, it is possible to control the alumina content in PMMA, and hence the swelling of the domains and the resistance of the mask in consequent dry etching applications [37], [44]. Processing temperature was set at 115 ºC, as it is near the glass transition temperature of PMMA, what should accelerate TMA diffusion [45]. For such times and temperature, the optimum number of cycles in order to obtain an alumina mask able to withstand silicon dry etching was observed to be 8.

During SIS, the underlying random copolymer PS-r-PMMA which serves as neutral brush for vertical alignment of lamellas and cylinders is infiltrated as well, as it contains both PS and PMMA units. This creates a continuous alumina layer (with thickness proportional to the concentration of PMMA [41]) that needs to be drilled in order to

reach the substrate. To do so, chuck power (RF2) needed to be increased up to 35 W, without fear of putting in danger the mask thanks to its new enhanced resistance.

TABLE 3.7
SIS PROCESS PARAMETERS FOR INFILTRATION OF PS-b-PMMA SAMPLES

Temperature (ºC)	Cycles	Pre-pulse	t TMA (s)	t water (s)	t purge (s)
115	8	Yes	80	80	10

Results after infiltration of the two thin films can be seen in figure 3.8. As expected from literature, Al_2O_3 SIS did not vary the pitch of the lamellae or cylinders, although the size of PMMA domains was increased with respect to PS [12]. Selective growth of alumina in PMMA also includes the interface between PS and PMMA, where chains of both polymers are entangled in a gradient of composition of few nanometers [37]. The increase in chuck power generated a Si etching more dependent on the physical facet of the attack, therefore more anisotropic. Thanks to this additional milling, it was possible to raise the ratio of C_4F_8 with respect to SF_6 to improve wall passivation, without facing any trouble in removing it from horizontal surfaces.

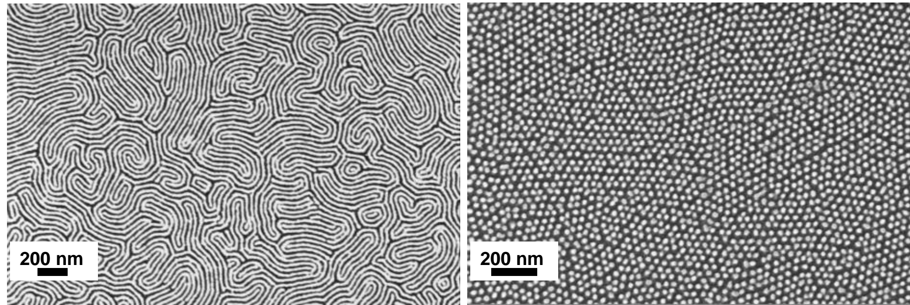

Figure 3.8. SEM top-view micrographs of two samples after SIS: lamellar (left) and cylindrical (right). Infiltration of PMMA by TMA causes a contrast reversal: now the light domains are infiltrated PMMA, and the dark are PS.

After a 5-minute 500 W oxygen plasma to strip the remaining polymer, nanoscale features were transferred onto the silicon substrate (figures 3.9 and 3.10) with alumina as mask. Aspect ratios obtained were higher than the ones obtained by direct pattern transfer using PS as mask. Dry etching conditions were re-optimized and standard established processing parameters are shared in table 3.8.

TABLE 3.8
PROCESS PARAMETERS FOR PATTERN TRANSFER ONTO Si WITH INFILTRATED PMMA AS MASK

T (ºC)	P (Pa)	SF_6 (sccm)	C_4F_8 (sccm)	RF1 (W)	RF2 (W)	Si etch rate (nm/s)
20	2	20	45	1200	35	~1.2

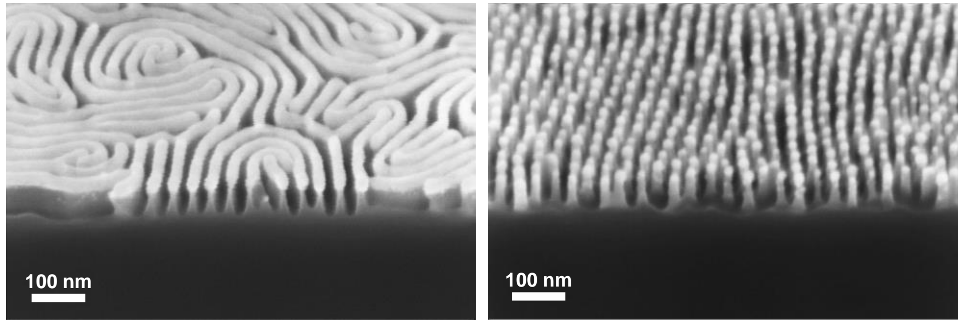

Figure 3.9. SEM tilted (30º) micrographs of two samples after pattern transfer with infiltrated PMMA. Structures of up to 50 nm in height were obtained.

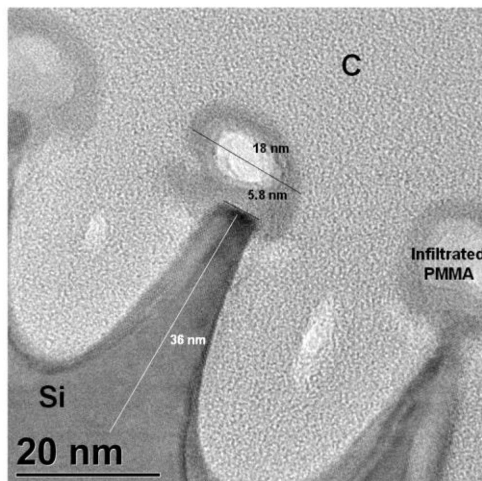

Figure 3.10. TEM micrograph of silicon fins obtained after pattern transfer with a mask of PMMA infiltrated by SIS. The alumina mask can still be observed on top of the etched nanostructures.

3.3 SELF-ASSEMBLY WITHIN GUIDING PATTERNS FABRICATED BY OPTICAL LITHOGRAPHY

Influence of brush deposition in the control of surface affinity

As introduced in chapter 1, microphase segregation of BCPs alone is not useful for lithographic applications. It is necessary to control domain orientation and guide the BCPs into de desired long-range order and morphology [46]. One of the approaches to attain this is the use of topographical guiding patterns (GPs), in a method known as graphoepitaxy. Yet, if during graphoepitaxy surface affinity of the substrate and guiding patterns is not controlled, undesired morphologies might still occur. Figure 3.11 shows four different examples of the graphoepitaxy of lamellar PS-b-PMMA on a silicon substrate with silicon oxide GPs. In them, the bottom and sidewall surfaces of the trenches have their affinity chemically modified, impacting BCP morphology after self-assembly.

In figure 3.11 a), a PS-r-PMMA brush layer is grafted only on the bottom of the trench, balancing free energy between surface and BCP domains [47], [48]. In this template, self-assembly takes place in vertical lamellae parallel to the GP walls, in an interesting morphology for the transfer of lines and spaces. This orientation is explained by the absence of brush macromolecules on the sidewalls of the trench, making SiO_2 preferentially interact with PMMA [49], [50], [51]. However, this approach presents several drawbacks. First of all, due to the absence of a sidewall pre-treatment, local variation of affinity might occur, and self-assembly can be prone to defects. In addition, GPs must be defined by high-resolution lithography, as only a limited amount of lamellae are possible to align parallel to the GP walls with low defectivity. Lastly, the deposition of the brush layer inside the pattern needs to be very well-controlled to avoid partial grafting on the sidewalls [52].

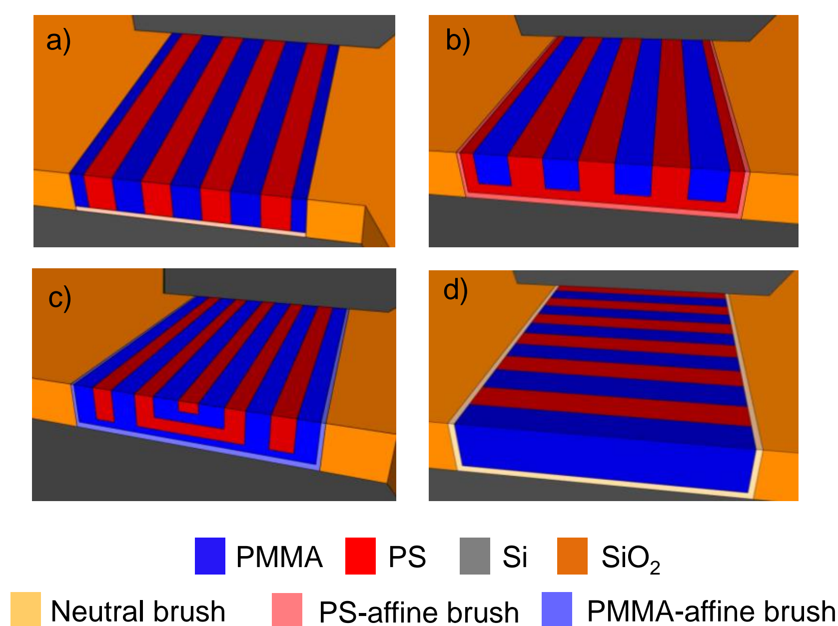

Figure 3.11. Graphoepitaxy of lamellar PS-b-PMMA in silicon oxide trenches. If the bottom of the trench is neutral, but walls are affine to one block, vertical lamellae self-assemble parallel to the walls (a). If bottom and walls are affine to one block, undesired wetting morphologies can hinder the pattern transfer (b, c). If walls and bottom are neutral, vertical lamellae self-assemble perpendicular to bottom and trench walls.

Therefore, departing from the premise that it is advisable to control the affinity of the whole trench for long-rage order without defects, three options are available: to force sidewalls and bottom of the cavity to be affine to PS, affine to PMMA or neutral.

Figures 3.11 b) and c) exemplify the morphologies adopted by PS-b-PMMA after self-assembly if bottom and walls present preferential affinity to one of the two blocks. If a PS brush is deposited thick enough than it can graft bottom and sidewalls of the trench, a PS layer will be formed over the brush and will wet the sidewalls, forming a fork shape. On the contrary, if a PMMA brush is grafted on all the surfaces, PMMA will wet them, generating morphologies that alternate PS and PMMA layers, hindering the pattern transfer [25], [52].

Finally, if a neutral layer of PS-r-PMMA is deposited thick enough to completely cover walls and bottom of the trench, both PS and PMMA will wet all surfaces and the BCP will self-assemble in vertical lamellae perpendicularly aligned to the GP walls (figure 3.11 d) [53]. This approach with a neutral brush as opposed to the one in figure 3.11 a), does not need high-resolution lithography for the fabrication of GPs and a thick brush layer is grafted all over the trench, not only extremely controlled on the bottom.

To demonstrate this last more relaxed approach of graphoepitaxy, directed self-assembly of lamellar PS-b-PMMA within silicon oxide GPs fabricated by conventional optical lithography was conducted.

Fabrication of SiO_2 guiding patterns

For the fabrication of 3D GPs, a {100} silicon (p-type, 4-40 Ω·cm) wafer was thermally oxidized to grow 54 nm of SiO_2 on top, the final height of the trenches sidewalls. Standard i-line (λ = 365 nm) photolithography, which renders a critical dimension of 350 nm, was used to define the grooves, followed by RIE down to the Si substrate. Guiding patterns like the one shown in figure 3.12 were obtained with gaps ranging between 350 nm and 750 nm.

Deposition and directed self-assembly

As a first step, the wafer was diced and samples were cleaned in acetone and IPA and activated by oxygen plasma for 5 minutes at 500 W and 600 sccm O_2 flow. Then, a 1.5 wt. % PGMEA solution of $PS_{60\%}$-r-PMMA was spin-coated at 1500 rpm and annealed for 5 min at 230 ºC in a tube furnace with continuous nitrogen flow. After annealing, the non-grafted random copolymer was removed by spin-coating PGMEA on the chips for 90 seconds. By this time, the neutral brush layer was attached to bottom and walls of the trench, forcing neutral affinity to PS and PMMA. Lastly, a 0.5 wt. % PGMEA solution of PS-b-PMMA (L_0 = 28 nm) was spin-coated at 1500 rpm for 30 seconds and annealed for 10 minutes at 265 ºC inside a tube furnace with a nitrogen stream.

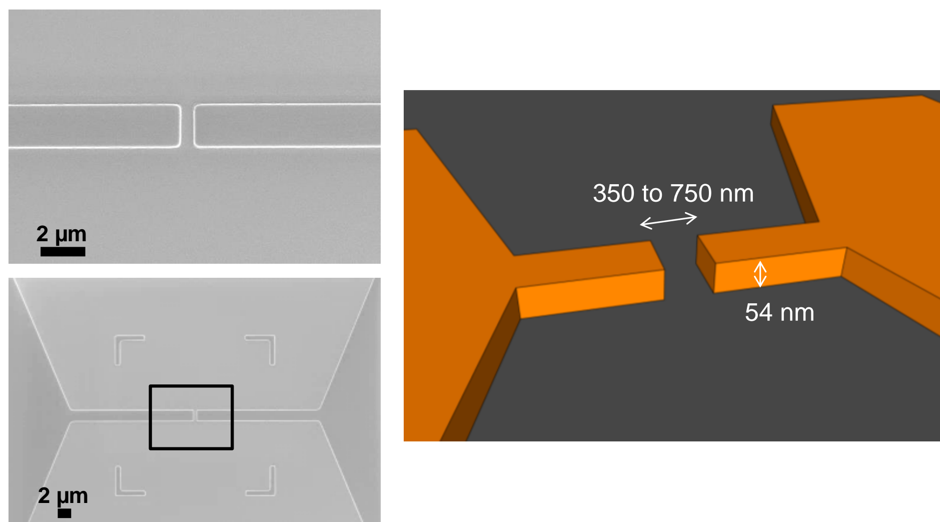

Figure 3.12. SEM top-view micrographs and scheme of the 3D guiding patterns fabricated by optical lithography (i-line).

Results after DSA in trenches of multiple widths are shown in figure 3.13. SEM micrographs show defect-free perpendicular alignment on trenches up to 600 nm. Atomic force microscopy measurements (figure 3.14 a)) disclosed that for these processing conditions, gaps accumulated between 25 and 30 nm of BCP in the trench (plus the additional brush layer thickness, which on a free surface is ~8 nm for 1.5 wt. % $PS_{60\%}$-r-PMMA).

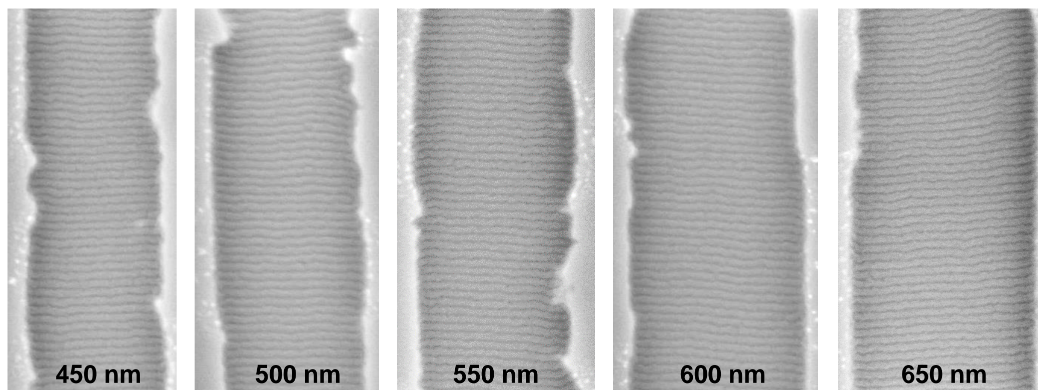

Figure 3.13. SEM top-view micrographs of the graphoepitaxy of lamellar PS-b-PMMA (L_0 = 28 nm) in SiO_2 trenches fabricated by standard optical lithography.

Selective PMMA removal and pattern transfer onto silicon

In order to transfer the BCP nanopatterns onto the Si substrate, PMMA was selectively removed by ICP-RIE in Ar/O_2 plasma, followed by a mixed-mode Bosch process. Process parameters have already been detailed in tables 3.4 to 3.6 for pattern transfer on a free surface. However, as it is common in plasma etching, etch rates depend on feature size, aspect ratios and topography distribution [54], [55]. As trench width decreases, etch rates inside become slower [56]. A 37-40% decrease in etch rates with respect to free surface conditions was observed, and new parameters are resumed in tables 3.9 to 3.11.

To entirely eliminate the PMMA domains and brush layer under them, chips were etched following the recipe detailed in table 3.10. Depending on trench width and BCP thickness, dry etching was carried out for 20 to 25 seconds. The remaining PS mask (between 13 and 18 nm) was then used to successfully obtain 25 nm silicon fins perpendicularly aligned with respect to the wall, as the ones shown in figure 3.14 b).

TABLE 3.9
PROCESS PARAMETERS FOR SELECTIVE PMMA REMOVAL IN PS-b-PMMA BY RIE
(OPTICAL LITHOGRAPHY GUIDING PATTERNS)

T (ºC)	P (mTorr)	O_2 (sccm)	Ar (sccm)	RF (W)	PMMA ER (nm/s)	PS etch rate (nm/s)	PMMA:PS selectivity
20	30	4	80	25	~1.6	~1	1.6:1

TABLE 3.10
PROCESS PARAMETERS FOR SELECTIVE PMMA REMOVAL IN PS-b-PMMA BY ICP-RIE
(OPTICAL LITHOGRAPHY GUIDING PATTERNS)

T (ºC)	P (Pa)	O_2 (sccm)	Ar (sccm)	RF1 (W)	RF2 (W)	PMMA etch rate (nm/s)	PS etch rate (nm/s)	PMMA:PS selectivity
20	1.33	10	200	200	5	~0.55	~0.2	2.6:1

TABLE 3.11
PROCESS PARAMETERS FOR PATTERN TRANSFER ONTO Si BY ICP-RIE
(OPTICAL LITHOGRAPHY GUIDING PATTERNS)

T (ºC)	P (Pa)	SF_6 (sccm)	C_4F_8 (sccm)	RF1 (W)	RF2 (W)	Si etch rate (nm/s)	Si:PS selectivity
20	2	30	30	1200	10	~1.4	2.5:1

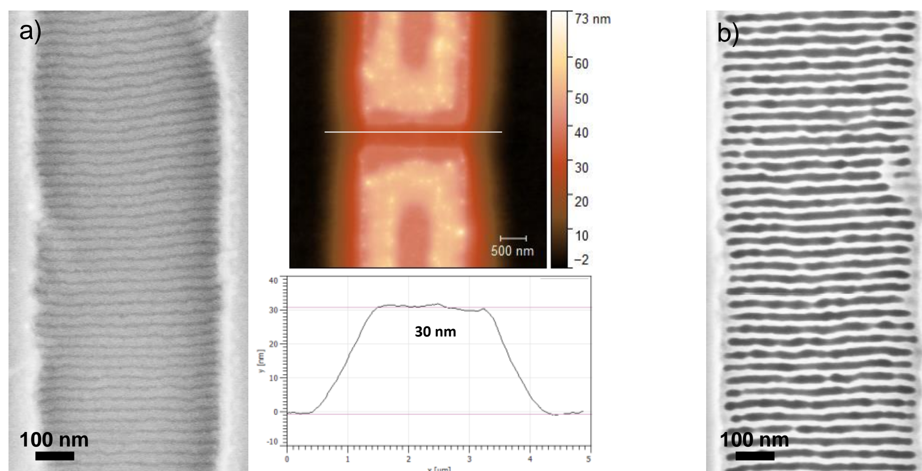

Figure 3.14. a) SEM top-view micrograph of a 450-nm gap and the corresponding BCP profile after self-assembly, as measured by AFM. b) SEM top-view micrograph of parallel silicon fins of approximately 25 nm of height and 12 nm of width perpendicularly aligned with respect to SiO_2 guiding patterns.

3.4 CONCLUSIONS

In this chapter optimum conditions for the self-assembly of several PS-b-PMMA BCPs (lamellar L_0 = 37 nm, lamellar L_0 = 30 nm and cylindrical L_0 = 36 nm) on silicon and silicon oxide substrates were demonstrated.

Then, dry etching recipes for the pattern transfer of PS-b-PMMA onto silicon and silicon oxide were developed, by selectively removing PMMA in Ar/O_2 plasma and then using the remaining PS blocks as mask. With these processes silicon fins between 30 and 40 nm of height were repeatedly obtained, as well as nanopatterns transferred through thin films of silicon oxide of 12 nm. Final structures presented widths smaller than theoretically expected, according to the BCP natural pitch used. The main reason

behind this was a certain degree of isotropy during dry etching processing, despite it being a passivated etch.

Sequential infiltration synthesis of PS-b-PMMA was also performed by running several ALD cycles with TMA and water, to infiltrate PMMA domains with Al_2O_3. These experiments resulted in infiltrated samples with higher etch resistivity, and as result, previously developed dry etching recipes were readjusted to obtain silicon fins and pillars with heights in the 50-nm range.

Finally, self-assembly of PS-b-PMMA was directed following a graphoepitaxial approach, by using topographical SiO_2 guiding patterns defined by standard optical lithography. By forcing the walls and bottom of such trenches to present neutral affinity to PS and PMMA, and performing self-assembly and dry etching, silicon fins perpendicularly oriented to the GP walls were obtained.

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Chapter 4

DSA of PS-b-PMMA for the fabrication of functional devices

In this chapter we present a novel fabrication route based on the introduction of DSA of BCPs as a patterning option for the fabrication of suspended silicon membranes clamped by dense arrays of single-crystal silicon nanowires. The overall fabrication process combines DSA with EBL, but can be adapted to high-volume manufacturing by employing conventional optical lithography. After release, the resulting devices can be further developed for building up high-sensitive mass sensors based on nanomechanical resonators.

4.1 INTRODUCTION

As discussed in chapter 2, NEMS are interesting building blocks for the realization of sensors as the properties conferred by their extremely reduced dimensions, large surface area-to-volume ratios and minimal masses allow obtaining ultrahigh sensitivity [1]. Nanowires and membranes are structures of special importance as, being very small, they are easy to control electrostatically, have minimal mass, and show large resonant frequencies which make them ideal for the fabrication of high-resolution mass sensors [2], [3]. A wide spectrum of materials has been studied for their fabrication [4], although compatibility with standard semiconductor processing confers silicon nanowires (SiNWs) great interest.

As explained in chapter 1, DSA not only has been considered a cost-effective alternative for patterning in the most advanced nanoelectronics nodes, but also applied to multiple fields where dense nanoscale structures need to be created. However, little to no results can be found on DSA for the definition of NEMS. We believe DSA can emerge as an appealing option for this thanks to its low cost, ease of scalability and capability of achieving very high resolution. As proof, in this chapter we present a DSA process based on the graphoepitaxy of lamellar PS-b-PMMA, which enables the fabrication of ultra-thin silicon membranes suspended by high-density arrays of silicon nanowires with sub-10-nm features.

The key steps of the whole fabrication process are depicted in figure 4.1, and combine top-down and bottom-up lithography. Each stage of the fabrication process is compatible with standard CMOS technology and can be scalable to high-volume manufacturing.

First, silicon oxide structures are created on top of a silicon-on-insulator (SOI) substrate by EBL (figure 4.1 (a)), generating walls and trenches that will aid as GPs for graphoepitaxy. In addition, these structures not only serve as GPs for DSA, but also as mask for membrane definition during RIE. Then, graphoepitaxy of lamellar PS-b-PMMA is performed by previously grafting a neutral brush layer all over the GP

surfaces, in an approach already demonstrated in chapter 3 with GPs fabricated by optical lithography. After selectively removing PMMA (figure 4.1 (c)), PS and SiO_2 are directly transferred onto the device layer of the SOI substrate by dry etching (figure 4.1 (d)), creating the nanowires and membranes. Finally, devices constituted by dense arrays of SiNWs and membranes are released and suspended by attacking the buried oxide (BOX) in hydrofluoric acid.

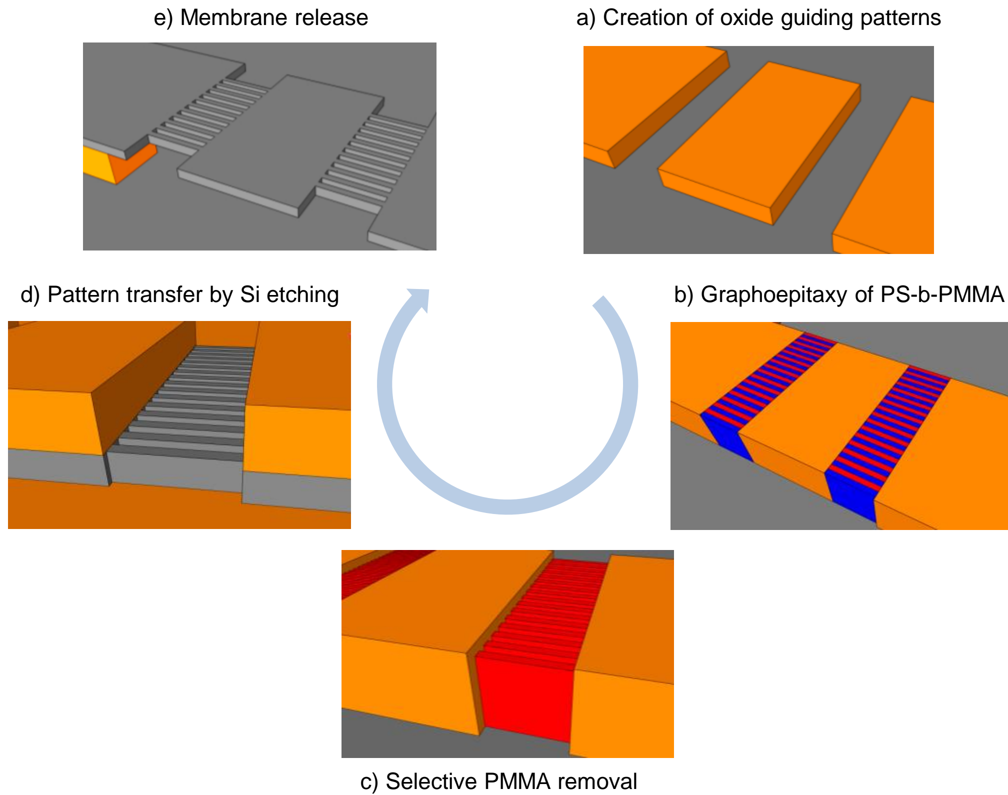

Figure 4.1. Main steps of the process flow developed for the fabrication of suspended Si membranes.

4.2 KEY PARAMETERS OF EBL EXPOSURE

As introduced in chapter 1, EBL is a maskless nanolithography technique based on the scanning of a focused beam of electrons to chemically modify a sensitive film (resist) through the generation of secondary electrons. Once this resist is developed, the exposed or non-exposed regions (depending on the type of resist) are removed, enabling the definition of very small structures. EBL allows the fabrication of high-resolution features but presents an important drawback in terms of throughput, which limits its use to photomask fabrication and research [5].

In the Raith 150^{TWO} tool (Raith GmbH, Germany) available at the IMB-CNM, the electron beam is generated by applying an electric field to a Schottky field emitter of W/ZrO in high vacuum. Electrons are pulled out from the W tip in the form of a very stable current, while ZrO reduces work function and replenishes the material ripped from the needle [6]. Then, the electron beam is deflected by electromagnetic lenses through the column and focused on the sample. The sample is fixed on a holder on a stage by spring-loaded mechanisms. The stage, which allows XYZ and rotation

movements, is also placed on a vibration isolation system to attenuate possible mechanical vibrations, which might affect patterning. In addition, a CCD camera allows visualizing the inside of the chamber.

Before sample exposure, the user needs to set a series of parameters, depending on the resolution and smoothness needed, resist and substrate used and time available. In this section, a brief introduction to these parameters is given so that later, experimental details are more clearly understood.

Write-field

It is the largest area than the electron beam can scan without moving the stage, only by deflecting the beam around the wafer surface. Its choice is a balance between obtaining the maximum resolution needed while minimizing stage movements, which take longer time [7]. Large write-fields may suffer from a loss of focus at the edges and limit the minimum step size that can be defined by the digital-to-analog converter when fracturing the pattern into pixels [8]. In the experiments of this thesis, all patterns were designed to fit into 200 × 200 μm^2 write-fields.

Tool write mode

In most EBL systems there are two modes of scanning the beam inside each write-field: raster and vector scan (figure 4.2). In a raster scan, the beam is scanned over the complete area of the write-field, being only unblanked when there is a feature to be exposed. In a vector scan, in contrast, the beam directly scans only over the areas to be patterned, typically saving more time. In our experiments, a vector scan was used in all exposures.

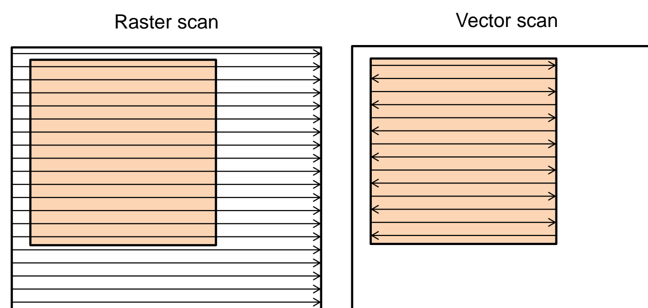

Figure 4.2. EBL writing strategies. Vector scan is generally faster than raster scan mode, as the beam is only scanned over the areas that must be exposed. In raster scan, the beam is driven all over the working area, unblanking when necessary.

Acceleration voltage

Most dedicated EBL systems in research provide a circular-cross-section beam of Gaussian-intensity profile, with spots between 2 and 10 nm (full width half maximum) [9]. However, a certain theoretical beam size does not automatically imply that the same beam spot is achieved on resist. Electrons emitted by the column undergo multiple interactions when they go through the resist and hit the substrate, suffering from forward-scattering and generating backscattered electrons, secondary electrons and X-Rays, amongst others. These effects limit the resolution achieved, influence resist sensitivity and cause proximity effects [10].

Penetration depth of electrons will depend on the atomic weight of the substrate, resist thickness and acceleration voltage [11]. Electrons accelerated at high energy penetrate deeper into the sample with very little forward-scattering, and as a result, the beam spot barely suffers from broadening when going through the resist, achieving very high resolution. However, electrons can spread laterally due to backscattering when reaching the substrate, giving rise to the possibility of the proximity effect. Also, sensitivity is low, as inelastic collisions in the resist (necessary for resist cross-linking or chain scission) decrease [12]. At low acceleration voltages, important forward-scattering of electrons of the incident beam takes place, transferring more energy to the resist, which generates a broader beam spot (lower resolution). However, as energy transfer if so efficient, lower dose is also required to clear the resist and lower times are needed for exposure [5], [8], [13].

Aperture

Beam spot not only depends on acceleration voltage, but also on beam current, regulated by aperture. Changes in aperture modify the numerical aperture of the incident beam, varying the amount of electrons emitted from the filament that reach the sample. Smaller beam spots (higher resolution) are obtained by decreasing aperture, which decreases current, increases depth of field and increases the time needed for exposure. Higher apertures are needed to expose faster, with the drawback of experimenting a loss in resolution [14].

Dose and step size

Dose is the charge per unit area the resist receives during exposure. Each resist has a clearing dose that fully exposes its whole thickness and allows precise shape definition for certain development conditions [14], so exposure dose needs to be selected in accordance.

Step size is the distance between the steps of the beam as it writes the pattern. The analog design to be exposed is digitalized by software and converted into a grid of pixels or steps, usually rectangles or parallelograms, of a size determined by the user. Then, when exposure is launched, the beam starts following a vector scan, individually moving from one pixel to the next, exposing each of them with the set exposure dose and beam size.

Both dose and step size influence the writing time of each pixel (dwell time), as shown in equation 1. The higher the exposure dose set per unit area and the step size, the longer the beam needs to stay over each pixel. However, when step size is increased, a lower number of pixels needs to be addressed, which reduces the number of beam movements, beam settling time, etc. Figure 4.3 exemplifies why it is necessary to choose a right combination of beam size, step size and dose, in order to ensure good fidelity of the design and smoothness of the edges of the pattern.

$$Dwell\ time = \frac{Dose \cdot \ Step\ size^2}{Beam\ current} \tag{1}$$

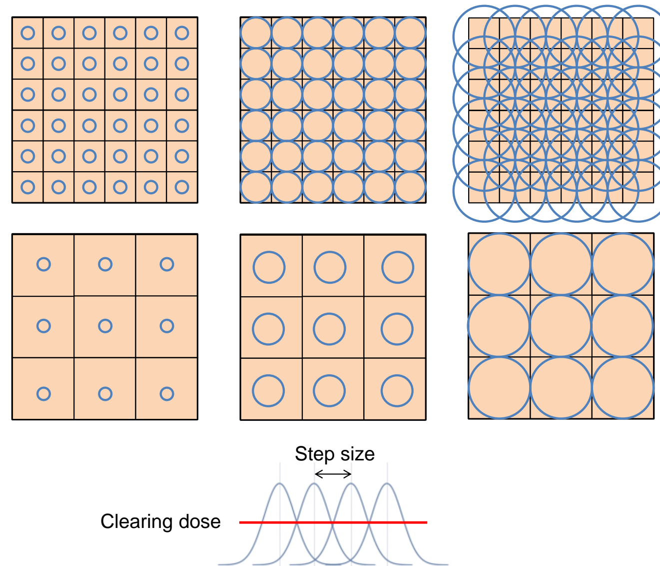

Figure 4.3. Several combinations of beam size and step size to expose the pattern (brown squared area) are shown. Beam size is usually set similar to step size, or even slightly bigger, to avoid exposing separated holes in the resist. However, if beam size is much larger than step size, feature dimensions will not match the design. Also, the bigger step size is, the fewer steps to expose, but the coarser the pattern becomes even by choosing an appropriate beam size.

4.3 FABRICATION OF ALIGNMENT MARKS AND GUIDING PATTERNS BY EBL

Creation of Au alignment marks by lift-off

Starting substrates in this fabrication process were SOI 2 × 2 cm^2 chips with an ultra-thin top silicon layer between 15 and 25 nm (p-type, 9-15 Ω·cm), which determined the final SiNW and membrane thickness. The buried oxide (BOX) was 155 nm.

The initial step was the definition of metal alignment marks on the chips by EBL and lift-off. These marks were essential for correct alignment of the multiple lithography steps comprised in the fabrication process flow. Gold was the selected material for mark definition as, thanks to its high atomic number, provides high contrast in backscattered-electron imaging [15].

Substrates were cleaned in acetone and IPA, followed by a 5-minute oxygen plasma at 600 W and a baking step for dehydration. Next, a bilayer stack of EL6 and PMMA was deposited to facilitate lift-off. By introducing a bilayer of fast (bottom) and slow (top) resists, a single exposure and development can create an undercut that facilitates lift-off with clean edges [6]. Spin-coating of copolymer resist EL6 (6% in Ethyl Lactate, MicroChem Corp., USA) was performed first, at 1500 rpm for 1 minute, followed by a baking step of 1 minute at 180 ºC on a hot-plate. PMMA 950K (2% in Anisole, MicroChem Corp., USA) was then spun at 2000 rpm for 1 minute, with another baking step of 1 minute at 180 ºC on a hot-plate. Total resist thickness after baking was ~270 nm (200 nm of EL6 and 70 nm of PMMA).

L-shaped marks were patterned by EBL at 10 kV of acceleration energy, with a 30 µm aperture. The dose used was 110 µC/cm^2 and the area step size was 5 nm. After exposure, each sample was developed for 30 seconds in a methyl isobutyl ketone (MIBK) and IPA 1:3 solution, continued by a dip of 30 seconds in IPA and N_2 drying. A thin film consisting of 2 nm of Cr (for adhesion) and 30 nm of Au was deposited by evaporation. Lift-off was performed in acetone for 5 minutes at 40 ºC in an ultrasound bath. Examples of the final alignment marks are shown in figure 4.4.

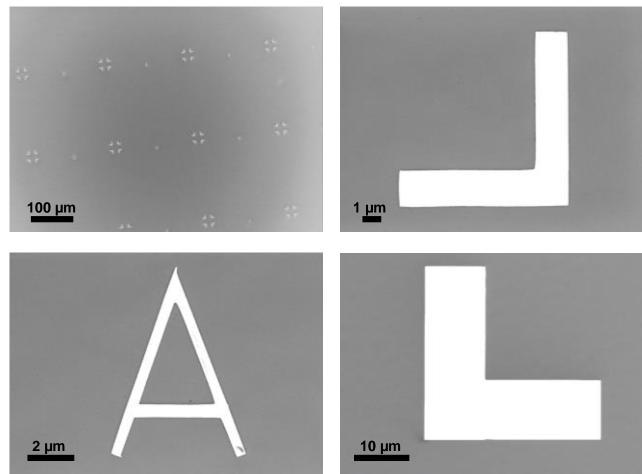

Figure 4.4. SEM top-view micrographs of several Cr/Au alignment marks obtained by EBL and lift-off.

Creation of silicon oxide GPs

As DSA was going to be carried out by graphoepitaxy, topographical GPs were created on top of the substrates to control and lead the BCP to self-assemble in the desired direction and orientation [16]. Silicon oxide GPs were defined by EBL, mainly thanks to its flexibility for prototyping. Nonetheless, other higher throughput top-down lithography techniques like UV, DUV or EUV lithography are alternatives to adapt the process flow for high-volume manufacturing, as demonstrated in chapter 3 with the fabrication of SiO_2 GPs for graphoepitaxy by i-line optical lithography.

First, the substrate surface was cleaned by oxygen plasma at 600 W for 5 minutes, and remaining attached water molecules removed in a short baking step. Later, a single layer of hydrogen silsesquioxane (HSQ) was spun on the SOI chips device layer using a 2% XR-1541 solution in MIBK (Dow Corning, USA). Spin-coating was performed at 1500 rpm for 1 minute, followed by a baking step of 4 minutes at 80 ºC on a hot-plate.

HSQ is an inorganic compound that serves as negative resist for EBL when very fine resolution is needed [17], [18]. When areas with HSQ are exposed with enough dose, it cross-links and transforms into a SiO_x material, similar to silicon oxide. After development, the exposed areas remain and can be used as mask for etching, for instance. HSQ handling is not trivial: it needs to be stored in a refrigerator at 4 ºC and reacts easily with humidity in its container or on the substrate surface.

After alignment with existing Cr/Au marks, squared and rectangular GP designs were patterned at 30 kV of acceleration energy, with a 10 µm aperture. The dose used was 940 µC/cm^2 and step size was 5 nm. After exposure, samples were immediately developed for 75 seconds in tetramethylammonium hydroxide (TMAH) 25% at 50 ºC, followed by a rinse in deionized water, a dip in IPA and dried in flowing N_2 (figure 4.5).

Development at high temperature was beneficial to eliminate undesired partly cross-linked molecules lying on the border and in between GPs, and these conditions proved to be vital for good reproducibility. For dense patterns, a multistep including a dip in very diluted HF can be introduced [19], [20]. The minimum dose experimentally found able to cross-link HSQ while surviving this development was 700 µC/cm^2. However, when using negative resists as mask for dry etching, it is necessary to expose at a higher dose than the minimum necessary to cross-link the polymer, while avoiding high doses that may produce unwanted features [19].

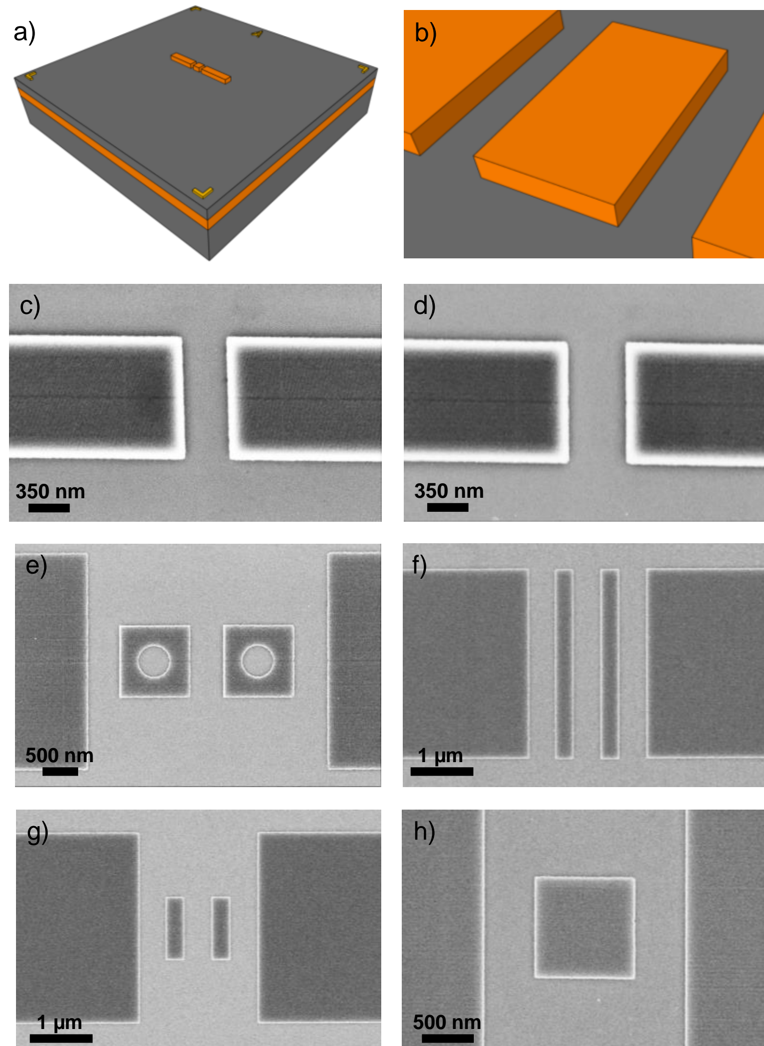

Figure 4.5. Schemes (a, b) and SEM top-view micrographs of several HSQ GPs. Single trenches of 350 nm and 450 nm of width are shown in c) and d), respectively. Different GPs with HSQ structures to define membranes are shown in (e-h). The width of the trenches is always designed to be between 350 nm and 550 nm to decrease the probability of defects in the self-assembly of PS-b-PMMA.

Trenches for graphoepitaxy were designed with widths between 350 nm and 550 nm to ensure defect-free perpendicular alignment of PS-b-PMMA. Final GP height after exposure and development is also function of exposure dose (figure 4.6). It was in our best interest to keep HSQ final height at ~30 nm (figure 4.7) as this provided: 1) a suitable SiO_x mask for the dry etch of at least 25 nm of Si, and 2) a GP sidewall height that ensured trenches were completely filled with 30 nm of BCP, an optimum thickness for the pattern transfer of SiNWs.

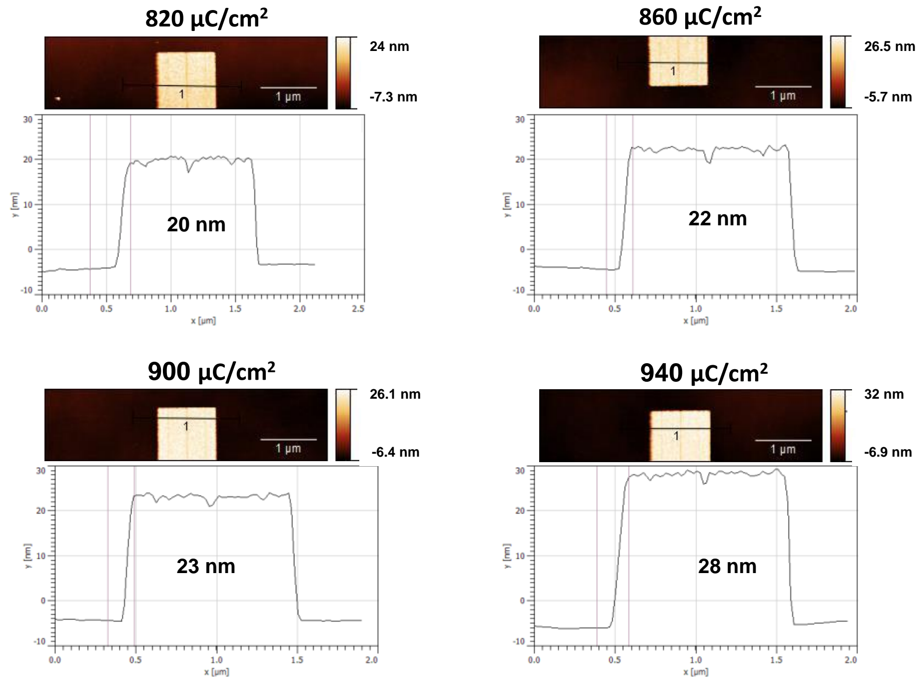

Figure 4.6. AFM images and profiles of HSQ guiding patterns exposed in EBL with different doses.

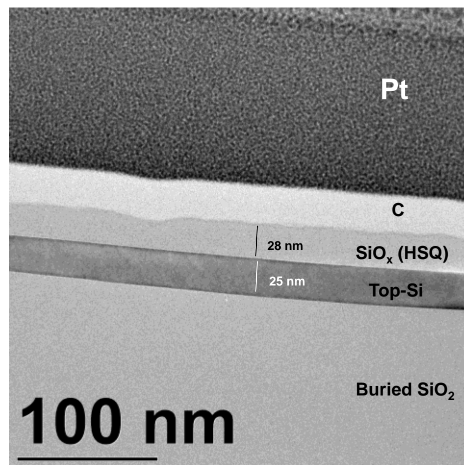

Figure 4.7. TEM micrograph of a lamella across one of the guiding patterns fabricated. The device layer of the SOI substrate is 25 nm. HSQ thickness of the GP is 28 nm. C and Pt films were deposited as protection and to enhance imaging contrast.

4.4 GRAPHOEPITAXY OF PS-b-PMMA

Usually in graphoepitaxy, the surface free energy between BCP domains and bottom of the trench is balanced by grafting a random copolymer brush layer on it, while non-grafted GP walls show stronger affinity to one of the blocks [21]. As consequence, when DSA is performed, domains are aligned perpendicularly to the bottom surface and parallel to the walls. Nevertheless, as discussed in chapter 3, high-resolution lithography to fabricate the trenches and extreme control in the deposition of the neutral layer to graft it only at the bottom are needed.

In this process a less-demanding methodology in terms of GP resolution and brush deposition control needed is presented. Here, the brush layer is grafted on bottom and walls, by spin-coating a thick layer of PS-r-PMMA that covers the full GP. As the three surfaces present neutral affinity, after BCP annealing PS and PMMA lamellae become perpendicularly aligned to bottom and sidewalls. This approach is much less strict as extremely fine lithography is not needed anymore for the definition of the GPs, and the grafting of the brush layer is not constrained to the bottom of the trench.

Before BCP spin-coating, chips were processed for 5 minutes in oxygen plasma at 600 W to activate the surface. Afterwards, a thick layer of a 1.5 wt. % solution in PGMEA of $PS_{60\%}$-r-PMMA was spin-coated on top of the chips at 1500 rpm for 30 seconds. The random BCP completely filled the gaps between the GPs, coating all surfaces. After a 5-minute annealing step at 230 ºC in a tube furnace with nitrogen atmosphere, the chips were rinsed in PGMEA in a second spin-coating step at 1500 rpm for 1 minute. This ensured that all the non-grafted brush was diluted and washed away, leaving behind a thin film of $PS_{60\%}$-r-PMMA attached to walls and bottom of the trenches. The thickness of this neutral layer was ~8 nm on a free surface for these same processing conditions.

Subsequently, a 0.5 wt.% PGMEA solution of PS-b-PMMA (L_0 = 28 nm) was spin-coated at 1500 rpm for 30 seconds and annealed at 265 °C for 10 min in a tube furnace with a continuous flow of N_2 to induce self-assembly. AFM characterization showed that polymer thickness inside the trenches, including BCP and brush layer, filled the gap completely (figure 4.8). In the areas outside the trenches, the BCP thin film was discontinuous, adopting the form of islands, due to the reduced thickness obtained at 0.5 wt. %. Effective perpendicular alignment with respect to the GPs (figure 4.9), demonstrates that the brush layer successfully covered bottom and trench walls.

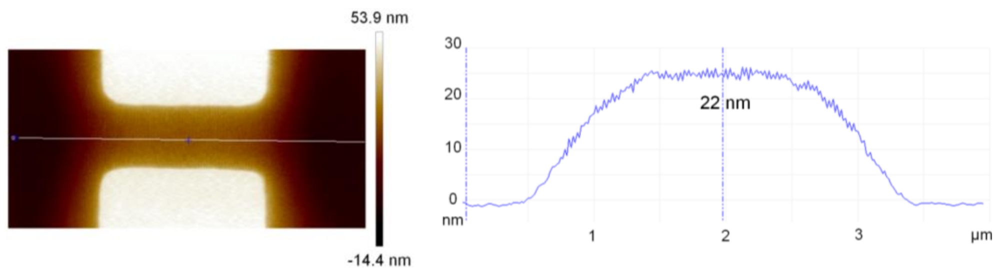

Figure 4.8. AFM image and profile of PS-b-PMMA self-assembled into vertical lamellae within a GP of 30 nm of height. The profile shows a PS-b-PMMA thickness of 22 nm. Taking into consideration the thickness of the $PS_{60\%}$-r-PMMA brush layer (~8 nm), it is confirmed that the gap of the GP is completely filled with BCP.

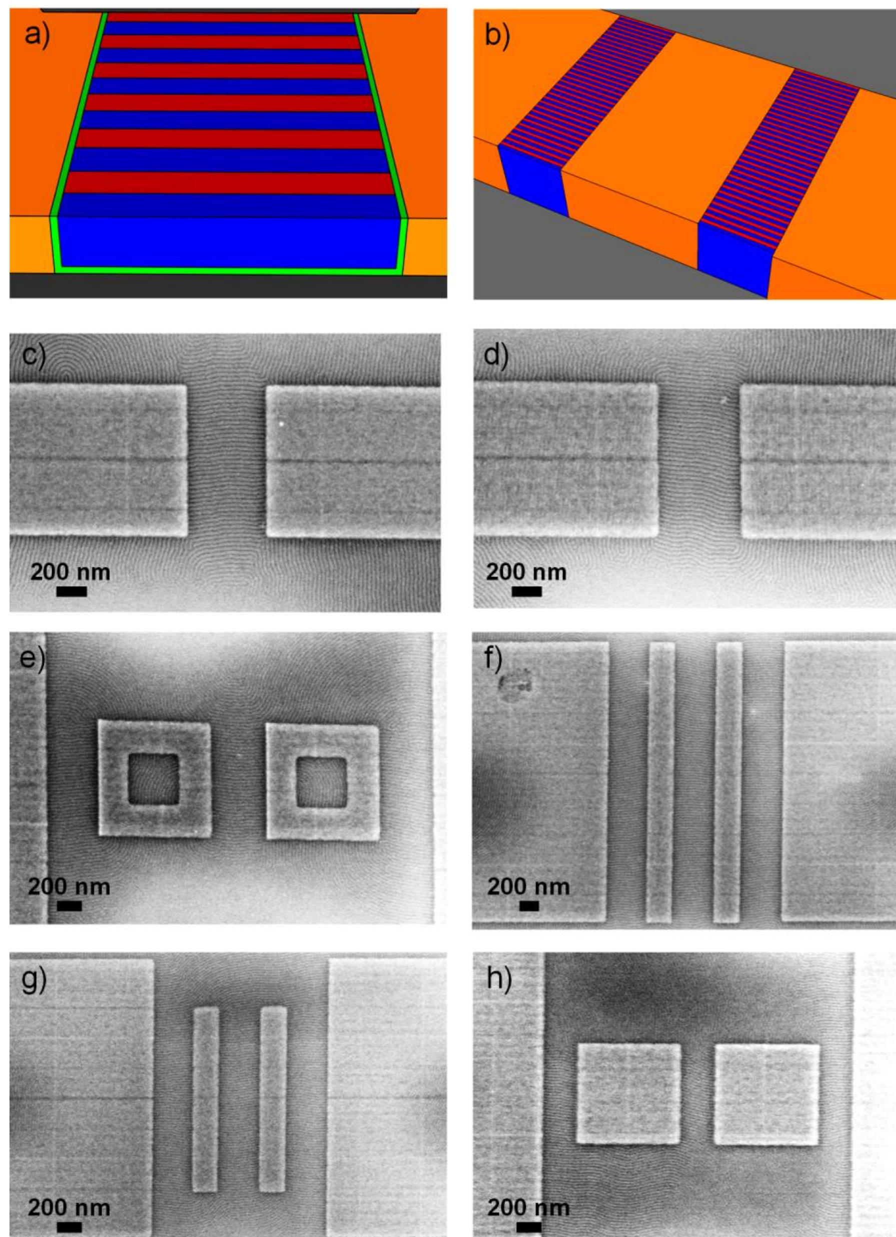

Figure 4.9. Schemes (a, b) and SEM top-view micrographs of the graphoepitaxy of PS-b-PMMA (28-nm pitch) within HSQ GPs. To obtain vertical lamellae perpendicularly oriented to the GP walls, a brush layer was grafted on bottom and walls of the trench (in green in a). Single trenches of 500 nm and 550 nm of width are shown in c) and d), respectively. Different GPs after successful DSA are shown in (e-h).

4.5 SELECTIVE PMMA REMOVAL AND PATTERN TRANSFER BY SILICON DRY ETCHING

After DSA, BCP inside the trenches barely presented any variance in terms of thickness (~30 nm) regardless of the width of the gap of the GPs (350 nm to 550 nm). PMMA was selectively removed by ICP-RIE (figure 4.10) in Ar/O_2 plasma, following the recipe introduced in chapter 3 for the pattern transfer within optical lithography GPs. Parameters are shown in table 4.1. An attack of 55 seconds was enough to eliminate PMMA from all gaps with enough selectivity to still leave ~20 nm of PS unconsumed.

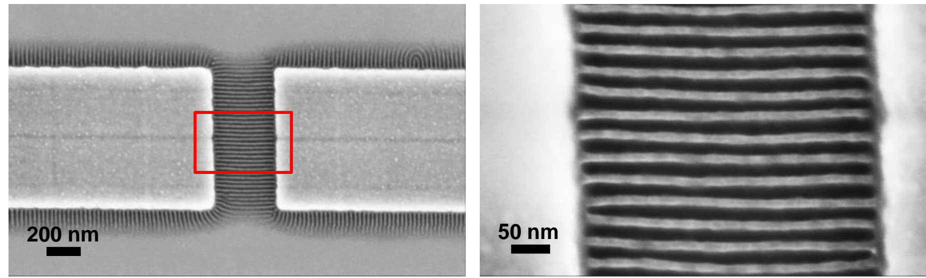

Figure 4.10. SEM top-view micrograph of a 375-nm GP after PMMA removal in ICP-RIE. Anisotropy is very good; the width of PS features is 14 nm.

TABLE 4.1
PROCESS PARAMETERS FOR SELECTIVE PMMA REMOVAL IN PS-b-PMMA BY ICP-RIE (EBL GUIDING PATTERNS)

T (ºC)	P (Pa)	O_2 (sccm)	Ar (sccm)	RF1 (W)	RF2 (W)	Time (s)
20	1.33	10	200	200	5	55

Pattern transfer onto the device layer of the SOI substrate (figure 4.11) using the remaining PS as mask was carried out in a mixed-mode Bosch process based on SF_6 and C_4F_8, also detailed in chapter 3. Process parameters are shared in table 4.2. Etching time depended on the thickness of the top-Si layer, and for 15-25 nm was between 13 and 18 seconds.

TABLE 4.2
PROCESS PARAMETERS FOR SILICON ETCHING BY ICP-RIE (EBL GUIDING PATTERNS)

T (ºC)	P (Pa)	SF_6 (sccm)	C_4F_8 (sccm)	RF1 (W)	RF2 (W)	Time (s)
20	2	30	30	1200	10	13 - 18

In this process flow the height of SiNWs comes determined by the thickness of the top-Si layer, as it is etched down to the BOX. A certain degree of isotropy reduced nanowire dimensions from the expected. The main explanation behind this lateral etching is resumed in a combination of inefficient passivation, difficulties in diffusion due to the small dimensions and the deflection of ions from their direct trajectories. Electric field gradients can be generated in dense arrays of nanostructures, which deviate ions from the normal, thus hitting the sidewalls of the trench. Also, re-deposition of material might occur at the top of the trench, which generates the peak or in the upper part of the NW [22], [23], [24], [25], [26].

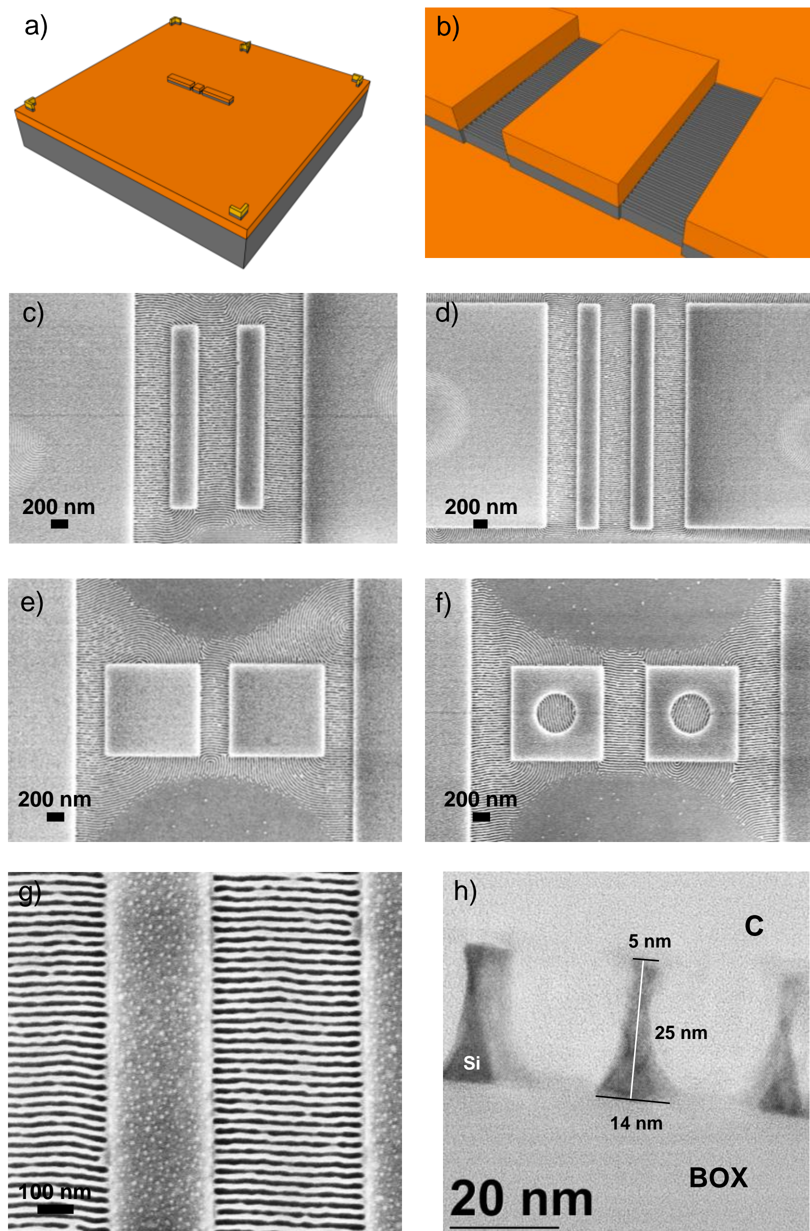

Figure 4.11. Schemes (a, b) and SEM top-view micrographs of SiNWs obtained after pattern transfer of PS-b-PMMA (c-g). Image h) is a TEM micrograph of a lamella across several SiNWs.

4.6 DISCARD OF UNDESIRED SILICON NANOWIRES

Once parallel nanowires and membranes were defined, it was necessary to remove any unwanted structure that had been transferred onto silicon as well. BCP accumulation, domain separation after annealing and pattern transfer not only took place in between GP sidewalls, but also along the border of each GP, in areas with residual BCP thickness. To eliminate these features, a third EBL step was performed to protect the sought-after nanowires, while leaving exposed the areas with undesired structures. Then, in a dry etching step, these were removed.

Before resist deposition, chips were subject to a 5-minute oxygen plasma at 600 W, followed by a baking step. Next, PMMA 950K (2% in Anisole) was deposited at 2000 rpm for 1 minute, and baked for 1 minute at 180 ºC on a hot-plate. Rectangular areas where nanowires wanted to be removed were exposed by EBL at 20 kV of acceleration energy, with an aperture of 20 µm. The dose used was 180 µC/cm^2 and the area step size was 5 nm. For development, each sample was immersed for 30 seconds in a MIBK:IPA 1:3 solution, followed by a dip of 30 seconds in IPA and N_2 drying.

After development, samples were dry etched for 20 seconds following the same parameters from table 4.2. Lastly, the PMMA mask was stripped in O_2 plasma for 10 minutes. Some examples of the results are shown in figure 4.12.

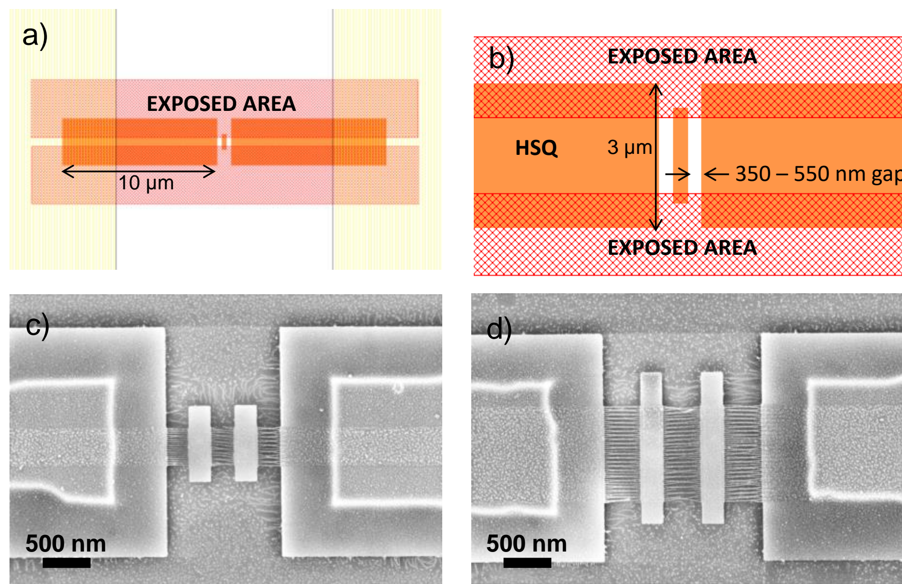

Figure 4.12. Schemes (a, b) of the EBL layout and SEM top-view micrographs (c, d) of samples after elimination of undesired nanowires. Samples were coated with PMMA and then the areas were SiNWs wanted to be removed were exposed by EBL, opening rectangular windows. In a dry etching step, SiNWs in those exposed areas were removed.

4.7 FABRICATION OF METAL CONTACT PADS

In order to give the possibility of electrically exciting the structures for characterization, metal contact pads were fabricated. Contact pads, defined in a fourth EBL step, were designed to end in 60 × 60 µm^2 areas, in order to be large enough for wire-bonding or eventual contact with a probe.

Sample surface was once more prepared in oxygen plasma at 600 W, and dehydrated. Following, a bilayer of EL6 and PMMA was deposited for lift-off, following the same approach to what was used to fabricate the alignment marks.

Pad areas were patterned at 10 kV of acceleration energy, with 30 µm of aperture. The dose used was 110 µC/cm^2 and the area step size was 10 nm. Chips were developed for 30 seconds in a MIBK:IPA 1:3 solution and a dip of 30 seconds in IPA, and dried

with N_2. Then, in an evaporation step, 5 nm of Cr and 80 nm of Au were deposited and the process was completed with lift-off of the metal in acetone for 5 minutes at 40 ºC in an ultrasound bath (figure 4.13).

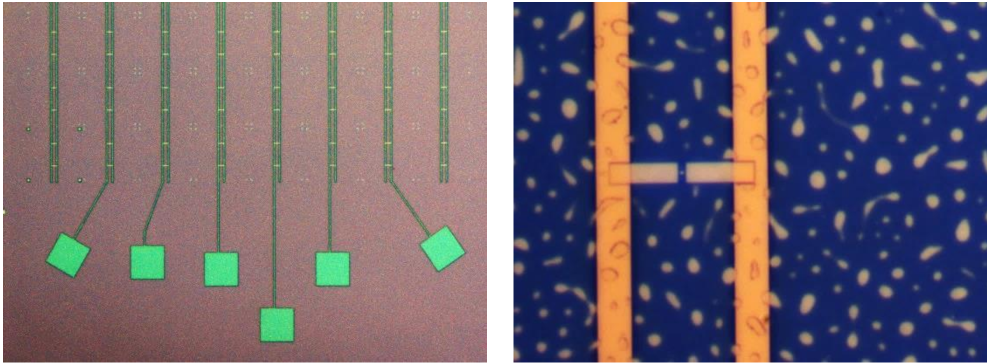

Figure 4.13. Optical microscope top-view images of Cr/Au contact pads obtained by EBL and lift-off.

4.8 RELEASE IN VAPOR PHASE HYDROFLUORIC ACID

In the final stage of the process flow, structures were released from the substrate using a SPTS µEtch tool (SPTS Technologies, UK) at the Center of Microtechnology in EPFL (Switzerland). This gas etching process takes place in vacuum, and uses low-pressure gas-phase hydrofluoric acid (HF) and alcohol to etch SiO_2 without liquids or critical point drying, avoiding potential collapse of the structures.

Prior to etching, samples were baked at 250 ºC for 2 minutes to remove humidity. Then, chips were introduced and the system automatically performed a conditioning step based on N_2 and EtOH to remove water molecules adhered to the walls inside the chamber. The main step of the process was performed by introducing 1250 sccm of N_2, 300 sccm of EtOH and 310 sccm of HF at a pressure of 126 Torr. To end the process, the chamber was purged and vented with N_2.

Processing time was approximately 3 minutes, but independently adjusted for each chip, to guarantee full release of the structures in the design without completely releasing the GPs that serve as clamping. Different tests were performed to tune this time (table 4.3) and some successful final devices are shown in figure 4.14.

TABLE 4.3
PROCESSING TIME TESTS FOR SILICON OXIDE ETCHING BY VAPOR-PHASE HF

Test	Time (min)	Max SiO_2 etched (nm)	Min SiO_2 etched (nm)	Average etched (nm)
1	5	450	390	422
2	3	227	197	216
3	2	229	149	186

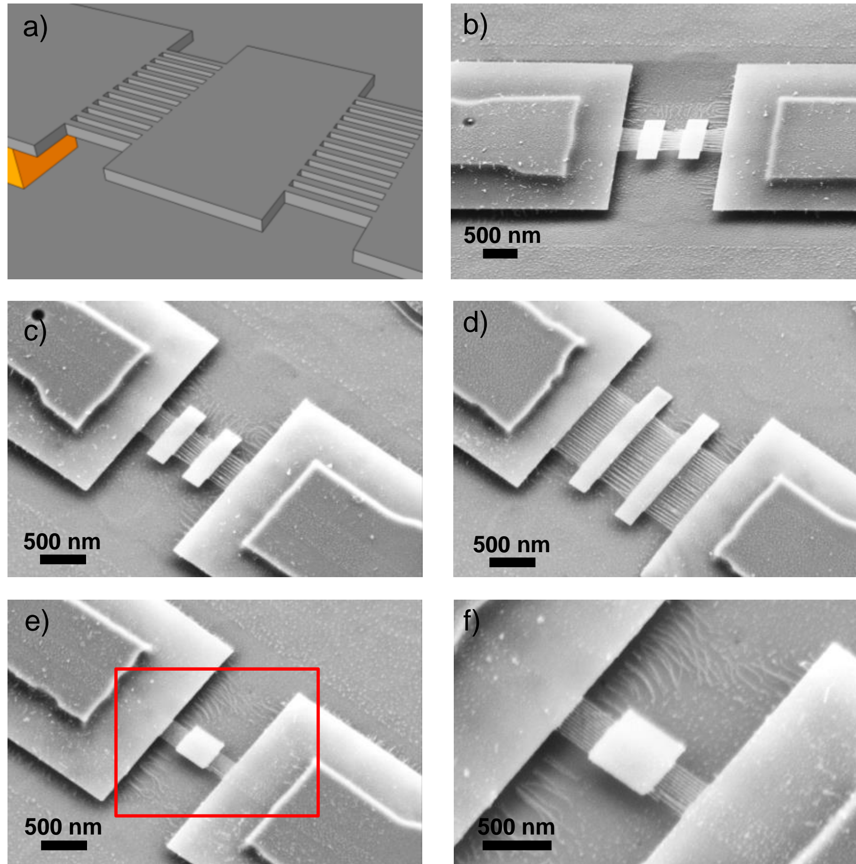

Figure 4.14. Scheme (a) and SEM top-view micrographs of several suspended silicon membranes (b-f). During release of these structures in vapor phase HF, the BOX under the membranes was completely removed. Likewise, the mask of HSQ from the GPs was also totally removed.

4.9 CONCLUSIONS

In this chapter a process flow for the fabrication of functional devices based on DSA of BCPs that could potentially be employed for the development of nanomechanical resonators was presented. Suspended silicon membranes clamped by high-density arrays of silicon nanowires of sub-10-nm diameter were fabricated, following a graphoepitaxial approach firstly introduced in chapter 3. While in chapter 3 GPs were structured by optical lithography, in this case they were created by EBL, and other top-down lithography methods could have been an alternative, as well.

Obtained devices evidence DSA enables the structuring of extremely high-resolution features in a cost-effective manner. Moreover, it gives the possibility of defining dense arrays of structures such as nanowires, which could be difficult by other high-resolution techniques like EBL due to the proximity effect.

Final fabricated structures were composed of arrays of SiNWs with lengths between 350 nm and 500 nm, combined with either a single or a pair of silicon membranes. These were designed rectangular or squared-shaped, with lateral dimensions ranging from 0.5 μm to 3 μm. Concatenated membranes were restricted to two, as three or more resulted in structure collapse after release.

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Chapter 5

Characterization of fabricated devices

In this chapter, a preliminary evaluation on the performance of devices obtained in chapter 4 is presented. Firstly, 3D eigenvalue simulations in finite element modeling software were conducted, taking into account real dimensions of fabricated structures. Then, experiments to characterize their resonant frequency by optical readout and AFM were carried out. Lastly, their ability to conduct electric current was tested.

5.1 INTRODUCTION

Nanomechanical structures fabricated in chapter 4 were composed of arrays of SiNWs of lengths between 350 nm to 500 nm, combined with a single or a pair of Si membranes. Similar structures including a silicon membrane, or paddle, supported by smaller arms or rods in the shape of beams had been developed in the past. Examples include torsional mechanical electrometers electromagnetically [1] or electrostatically driven [2], light modulators driven by the thermal effect of unmodulated incident laser light [3], or quad beams developed for distributed mass sensing applications [4], [5].

Although arrays of SiNWs obtained through the processes described in this thesis could have been directly used for the development of nanomechanical resonators by themselves, their extremely small dimensions and mass shoot their resonant frequencies up to levels above the limit of many characterization setups. In these sense, the incorporation of membranes into the design also helped decrease resonant frequencies thanks to the additional mass [6].

5.2 FINITE ELEMENT MODELING (FEM) SIMULATIONS

As a first step, simulations in COMSOL Multiphysics were carried out to calculate the theoretical eigenfrequencies of fabricated devices and evaluate whether their response laid in a measurable range for the available readout configurations. In order to create the models, real geometric parameters previously obtained by SEM and TEM characterization were taken into consideration. This included number of nanowires, nanowire shape and length, device layer thickness, membrane dimensions and top-Si layer undercut.

Once geometry, materials (in-library silicon and silicon oxide) and boundary conditions (fixed BOX) were defined, a Physics-controlled mesh was applied to the solid, and the eigenfrequency analysis launched. The analysis provided the first few eigenfrequencies of each device and their mode shape, including torsional and translational modes (figure 5.1), although it did not provide any information of the amplitude of vibration.

Results were calculated by applying the theory of linear elasticity, supposing small deformations and linear elastic material, and omitting any energy loss through clamping or due to dissipation mechanisms in the surrounding medium. Table 5.1 shares parameters of some of the modeled devices, together with the first four eigenfrequencies calculated. The totality of simulated devices showed natural frequencies in the 30 to 150 MHz range, confirming device design was successful for readout through the available optical and AFM-based characterization setups.

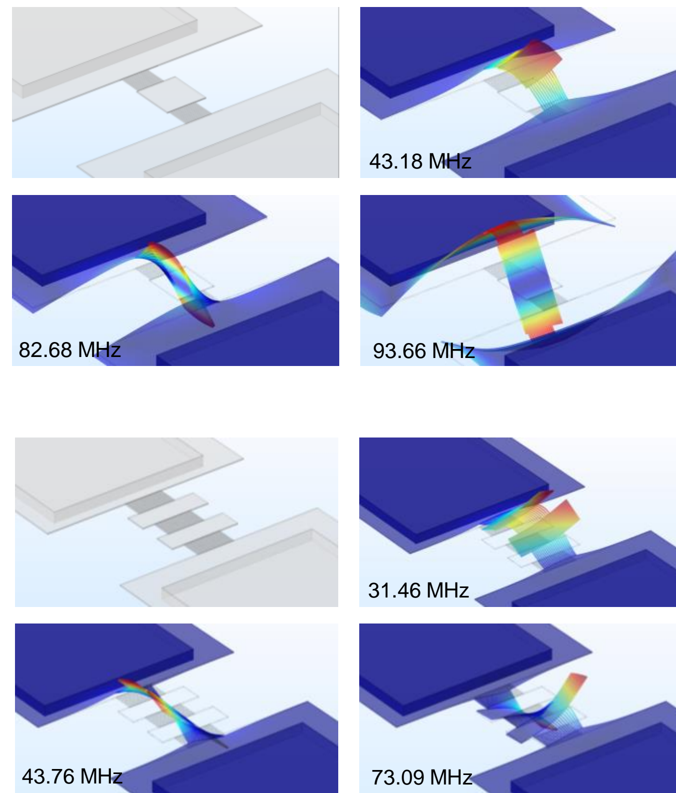

Figure 5.1. First three eigenfrequencies and mode shapes of two of the fabricated silicon membranes and nanowires. Devices are shown in figures 4.14 c) and e).

TABLE 5.1
GEOMETRICAL PROPERTIES AND CORRESPONDING EIGENFREQUENCIES CALCULATED BY COMSOL MULTIPHYSICS SIMULATIONS

Top-Si (nm)	NW length (nm)	Membrane #	M. length (nm)	M. width (nm)	Eigenfrequencies (MHz)			
15	292	1	496	528	43.2	81.7	93.7	101.2
15	285	2	320	1050	42.9	59.1	70.4	124.6
16	278	2	294	955	31.5	43.8	73.1	92.8
16	389	1	302	1833	83.2	87.1	103.1	146.4
22	282	2	280	1882	71.8	80.3	109.2	136.9
22	418	2	328	2045	34.8	41.5	49.2	65.3
25	430	2	330	3092	38.4	40.9	51.7	76.3

5.3 FREQUENCY CHARACTERIZATION BY LASER-DOPPLER VIBROMETRY

Laser-Doppler vibrometry (LDV) is an optical technique based on the Doppler-effect, which enables to determine motion at a fixed point thanks to scattered light [7], [8]. This is done by superposing on a photodetector a reference laser beam and the same beam scattered from the targeted moving element. When the vibrating object moves, a signal shifted in frequency and phase is generated with information about displacement and vibrational velocity of the oscillation [9], [10]. Specialized software then performs the fast Fourier transform of the modulated data received, plotting the intensity of the signal at each frequency of the selected frequency spectrum.

Experiments to optically characterize the dynamic behavior of suspended membranes and SiNWs by LDV were performed in two different setups at the Advanced NEMS Group lab from EPFL.

The first setup used (figure 5.2) consisted of an ultra-high frequency vibrometer (UHF-120 SV, Polytec GmbH, Germany), which incorporated a sensor head (UHF-I-120, Polytec GmbH) and a Mach-Zehnder interferometer; an LDV controller (UHF-E-120, Polytec GmbH), a signal generator, an oscilloscope, a precision XY-stage and a vacuum chamber. The LDV was able to reach frequencies up to 2.4 GHz, and its laser displayed an invariable power of 5 mW. The system showcased an optical objective of 100X, which resulted in a laser beam spot of approximately 700 nm of diameter.

Chips were glued to a piezo shaker and a PCB using silver paint, and introduced in the vacuum chamber. Both the piezo shaker and the thermal effect induced by the impacting laser on the membranes and NWs were used to drive mechanical motion of the device [11]. Ideally the piezo shaker would have been excited at an eigenfrequency of the device to enhance the oscillation amplitude, but its maximum frequency could not go above 10 MHz.

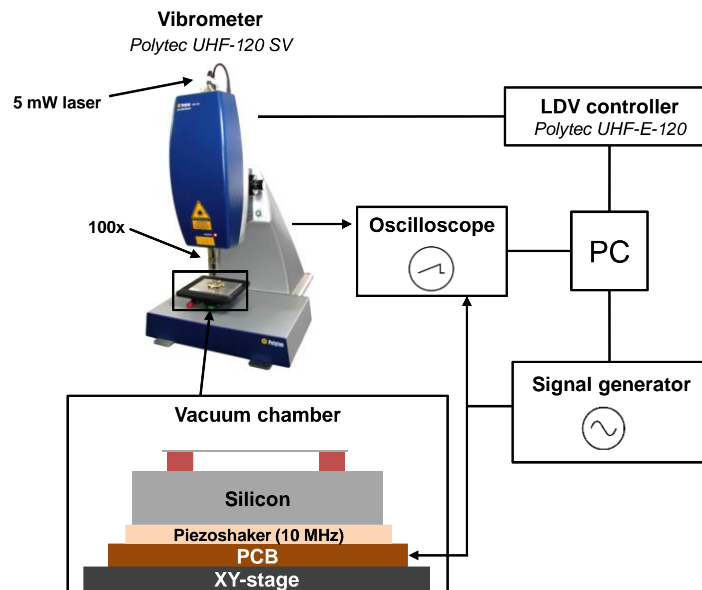

Figure 5.2. Scheme of the ultra-high frequency LDV setup used for the optical characterization of the resonance behavior of suspended devices.

Before frequency scans were launched, a scan grid with between 6 to 20 measurement points was defined in the tool software, completely covering the nanowire and membrane areas, in order to ensure measurements took place on top of the device and not on the substrate. During the scan, amplitude and phase were recorded at every scan point over acquisition time spans of 5, 10 and 20 µs. Measurements were performed at atmospheric pressure and in mild vacuum (~10^{-4} mbar), to avoid any possible viscous dissipation induced by air surrounding the device. Obtained amplitudes were minimal in both cases and resonance peaks could not be identified. A representative example of the plots obtained is shown in figure 5.3.

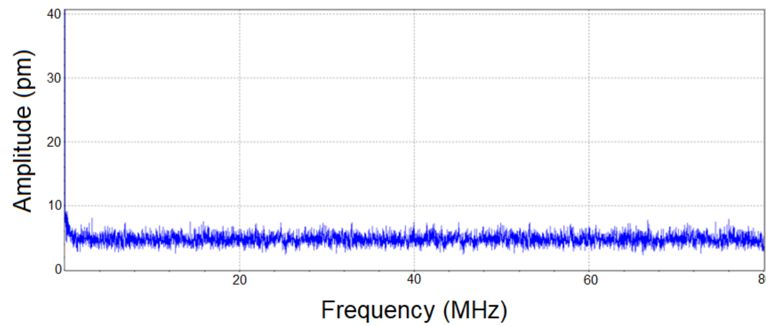

Figure 5.3. Frequency vs. amplitude plot obtained after LDV characterization.

The second setup used (figure 5.4) was composed of an optical microscope (100X objective), a fiber optic sensor head (OFV-551, Polytec GmbH), an LDV controller (OFV-5000, Polytec GmbH), a lock-in amplifier (UHFLI, Zurich Instruments), an oscilloscope, a precision XY-stage and a vacuum chamber. The laser power was fixed at 1 mW.

Despite displaying a highest measurable frequency of 24 MHz (all resonance peaks obtained by FEM were above 30 MHz), measurements were performed with this system nonetheless, to confirm the absence of unexpected peaks. None could be identified in neither atmospheric nor vacuum conditions.

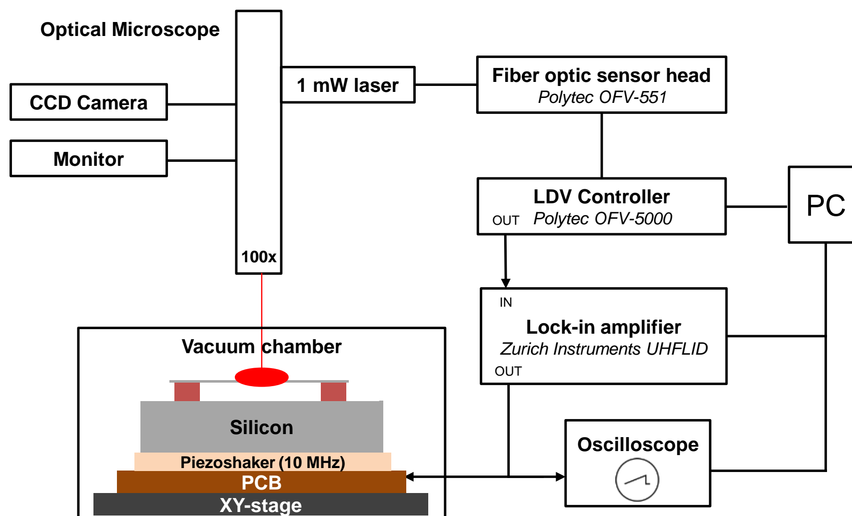

Figure 5.4. Scheme of the second LDV setup used for the optical characterization of the resonance behavior of suspended devices.

The main hypothesis behind this absence of peaks was the mismatch between laser power, LDV bandwidth and low device resistance to heat. When performing measurements in the LDV setup that included the 5 mW laser, high sampling times resulted in burnt devices (figure 5.5). Silicon membranes absorbed large amounts of light, and SiNWs did not provide a pathway for diffusing enough heat. On the other hand, lower acquisition times did not show enough resolution to make resonance peaks stand out from background noise. Thanks to the laser power being only 1 mW in the second LDV setup, acquisition time spans could be set higher without resulting in damaged devices because of heat, but no resonance peaks could be detected due to the limited measurable frequency bandwidth of 0-24 MHz.

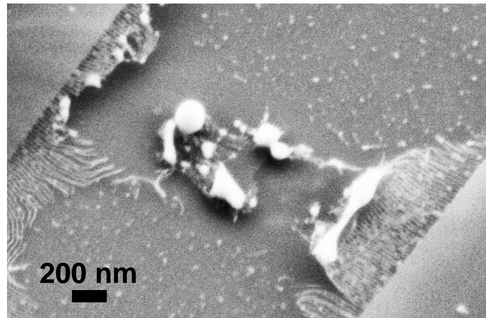

Figure 5.5. Example of a burnt device due to laser damage after LDV characterization.

5.4 FREQUENCY CHARACTERIZATION BY AFM

Resonance behavior of fabricated devices was studied using an approach based on AFM and amplitude modulation, previously reported for the detection of mechanical vibrations and eigenmodes in CNT resonators and graphene sheets [12], [13]. This characterization strategy is based on the scan of an AFM probe over the surface of a suspended device, while this is concurrently vibrating at a frequency close to that of resonance. The setup is shown in figure 5.6.

Due to the fact that AFM cantilevers cannot follow oscillations as high in frequency as those of devices in resonance, this method requires turning to an amplitude modulation technique. By doing so, the electric signal used as excitation is defined by a carrier wave at the eigenfrequency of the device (f_{CAR}) and a message wave at the frequency of the first eigenmode of the AFM cantilever (f_{MES}).

Chips were glued with silver paint to a PCB and an amplitude-modulated wave was created for electrostatic actuation through a back-gate (the substrate). As in electrostatic actuation force the voltage is squared,

$$V = V_0 \cos(f_{CAR}t) \Rightarrow V^2 = V_0^2\, cos^2(f_{CAR}t) = \frac{V_0^2}{2} + \frac{V_0^2}{2}\cos(2f_{CAR}t) \qquad (1)$$

f_{CAR} was initially set at half of the eigenfrequency ($\omega_n/2$) of the device. On the other side, f_{MES} was set at 300 kHz, which corresponds to the frequency of the first eigenmode of the used cantilever (OTESPA, Bruker, USA). The initial amplitude of the carrier wave (V_0) was set at 1 V, and amplitude modulation depth was set at 100%.

The measurement strategy consisted in performing frequency sweeps in the vicinity of expected eigenfrequencies, as calculated by FEM simulations. Firstly, broad sweeps were carried out around the initial frequency value (f_{CAR} ± 15 MHz, steps of 500 kHz) to have an overview of possible resonance peaks, then followed by finer sweeps (f_{CAR} ± 1 MHz, steps of 100 kHz). Further measurements were also made by increasing the carrier wave amplitude to 2 V and 3 V. Membrane vibrations were sensed by the AFM cantilever scanning in tapping mode, and measured with a lock-in amplifier tuned at f_{MES} as reference. Topography was obtained simultaneously at the second eigenmode of the cantilever.

Figure 5.6. Setup used for the characterization of the resonance behavior of suspended devices by AFM.

No insights on resonance could be drawn from these measurements. Figure 5.7 is a representative example of the obtained data. In the particular case of this device, a resonance peak was expected at 44 MHz (f_{CAR} = 22 MHz) as per simulations, but could not be experimentally identified. Equal measurements were also performed on an open area of the chip (without any devices), revealing that obtained peaks were acquired from the substrate.

Increases in the amplitude of the carrier wave (from 1 V to 2 or 3 V) generated larger detected amplitudes during excitation. Nevertheless, no resonance peaks could be isolated, as the signal coming from the substrate was also amplified (figure 5.8). In the

case of this characterization approach, the limiting factor seemed to be the quality factor of the devices in air versus noise. Finally, to discard that obtained curves were the result of electrical artifacts from the AFM probe, tests with the tip withdrawn from the sample were performed (figure 5.9).

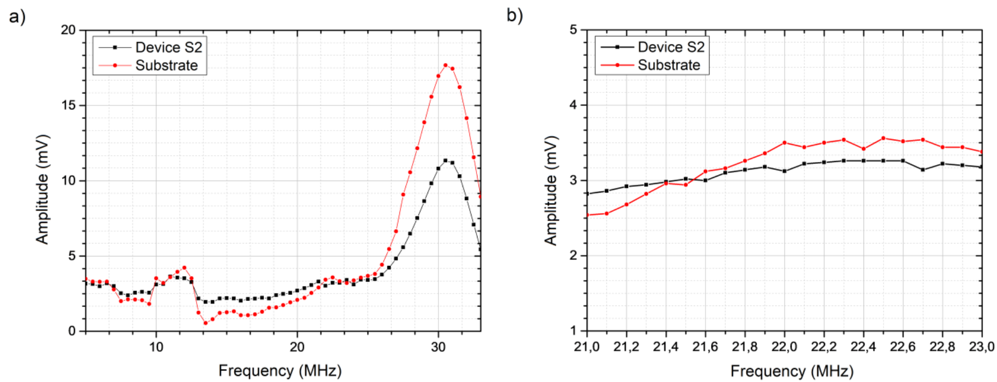

Figure 5.7. Frequency vs. amplitude plots for a particular device (in black) and for the substrate (in red). Carrier wave amplitude was set at 2 V. In a), f_{CAR} was swept from 5 to 35 MHz, in steps of 500 kHz. In b), f_{CAR} was swept between 21 and 23 MHz, in steps of 100 kHz.

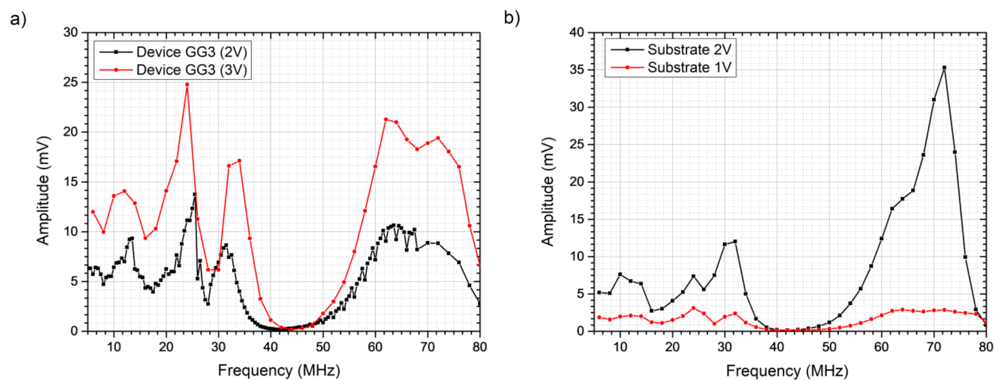

Figure 5.8. Frequency vs. amplitude plots at different carrier wave amplitudes in a) for a particular device, and in b) for the substrate.

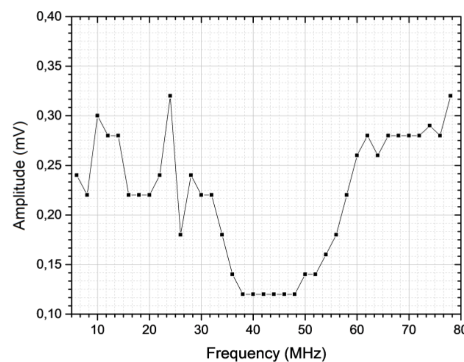

Figure 5.9. Frequency vs. amplitude plot with the AFM tip withdrawn from the sample. Carrier wave amplitude was set at 2 V.

5.5 ELECTRICAL CHARACTERIZATION

Difficulties in conducting electrical current were predictable given the reduced dimensions of the obtained nanowires and the initial resistivity of the top-Si layer of the SOI substrate.

Substrate resistivity, 9-15 Ω·cm, corresponds to a boron dopant concentration between 1 and $1.5 \cdot 10^{15}$ atoms/cm^3, or an equivalent 1 to $1.5 \cdot 10^{-6}$ atoms/nm^3. Taking into consideration nanowire dimensions,

$$NW_{length} \cdot NW_{width} \cdot NW_{thickness} = \\ = 500\,nm \cdot 10\,nm \cdot 25\,nm = 1.25 \cdot 10^5\,nm^3 \quad (2)$$

the approximate maximum number of dopants per nanowire can be calculated as

$$Dopants\ per\ NW = 1.25 \cdot 10^5\,nm^3 \cdot 1.5 \cdot 10^{-6}\frac{atoms}{nm^3} = 0.185\,atoms \quad (3)$$

which results in nanowire resistivity being that of intrinsic silicon.

In a last set of experiments, I-V measurements were performed by contacting present metal contact pads with two probes and sweeping a DC voltage (0 to 10 V) across multiple devices in parallel.

As pictured in figure 5.10, one probe was contacted to a common pad that connected all devices on the chip, and served as ground, while the second one was contacted to a single pad individually fabricated to connect multiple devices (up to 18) from the same column in parallel.

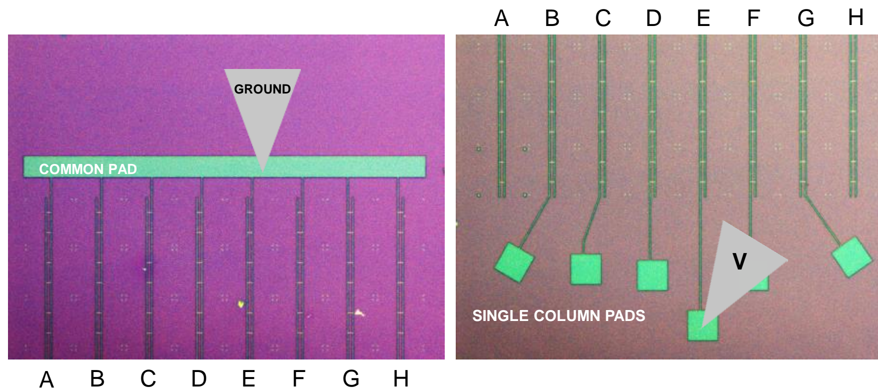

Figure 5.10. Scheme of the electrical characterization of fabricated devices. The top pad served as ground for the 8 columns of devices on the chip (A to H). Devices in each column were connected in parallel and a sweeping V_{DC} was applied with a second probe.

As expected, most devices showed lack of conductivity, and only one of the measured arrays started conducting current at an applied voltage of ~7 V (figure 5.11). This behaviour could be addressed by including a doping step in the process flow, bearing in mind already existing materials. For instance, in these chips, as Au was used for the definition of alignment marks and contact pads, nanowire doping was not possible due to the temperature limitations of gold.

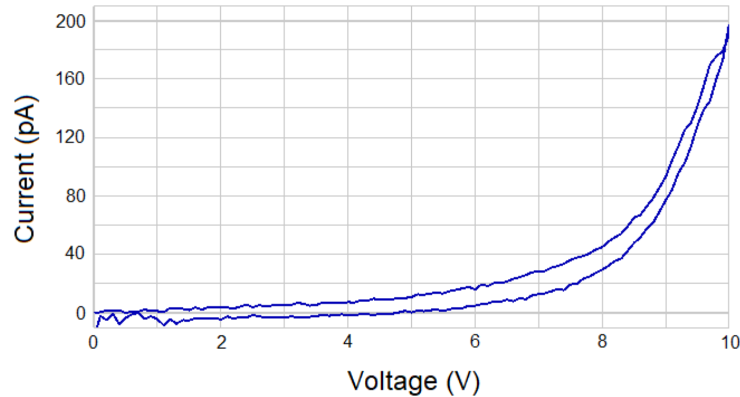

Figure 5.11. Obtained voltage vs. current curve after electrical characterization.

5.6 CONCLUSIONS

Although the main objective of this thesis is to demonstrate the suitability of a nanolithography technique for the fabrication of functional devices, early results on the characterization of obtained devices were shared in this chapter.

FEM simulations confirmed that fabricated devices presented eigenfrequencies in an adequate frequency range for characterization as nanomechanical resonators with the setups available.

Preliminary frequency measurements by optical readout were performed using laser-Doppler vibrometry, but devices resulted damaged due to small heat transfer rates when incident laser light was absorbed by silicon. A solution to this issue in future measurements would be the incorporation of a laser beam attenuator to filter the power of the laser.

Additional measurements were also carried out by AFM and an amplitude-modulation technique, although resonance performance was limited due to the small quality factor of devices in air.

For the fabrication of future batches, it would be interesting to include a doping step in the process flow, in order to be able to conduct electric current through the SiNWs and membranes, for excitation purposes.

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General conclusions

The main objective of this dissertation is to demonstrate that DSA of BCPs is a high-resolution nanolithography technique with potential for the fabrication of nanomechanical structures which could be employed for the development of sensors or NEMS.

To prove so, a process flow for the fabrication of suspended silicon membranes and nanowires was conceived and implemented. All the fabrication steps included in the designed flow were optimized:

- Parameters for self-assembly on silicon (on a free surface) of multiple PS-b-PMMA BCPs of different pitches (lamellar L_0 = 37 nm, lamellar L_0 = 30 nm and cylindrical L_0 = 36 nm) were optimized.

- Dry etching recipes for the pattern transfer of PS-b-PMMA onto silicon substrates were successfully developed. These include the selective removal of PMMA in Ar/O_2 plasma and a mixed-mode Bosch process to transfer PS onto silicon. Recipes were adjusted first for pattern transfer on a free surface, where silicon fins presenting heights between 30 and 40 nm were obtained. Then, recipes were tuned for pattern transfer of fins within GPs.

- Graphoepitaxy of PS-b-PMMA was successfully carried out following an approach in which high-resolution lithography and brush deposition control are not severe limitations. This was done by grafting a neutral brush layer on the three surfaces of the trench, forcing walls and bottom of the GPs to present neutral affinity to PS and PMMA. Lamellae perpendicular to walls and bottom of the trench were obtained after annealing and defect-free perpendicular alignment was achieved on trenches up to 600 nm.

- Topographical SiO_2 GPs were successfully defined by standard optical lithography at the resolution limit of the tool (350 nm). The use of these in graphoepitaxy proved that the designed process flow can be adapted to high-volume manufacturing.

- Parameters of EBL exposure and development were optimized in order to repeatedly obtain sharp HSQ GPs for graphoepitaxy.

- A vapor phase HF recipe was effectively regulated to release the defined silicon nanowires and membranes, suspending them without collapse.

Final attained devices were composed of high-density arrays of SiNWs with lengths between 350 nm and 500 nm and sub-10-nm diameters, combined with ultra-thin rectangular or squared silicon membranes. These structures show that DSA is a suitable technique for the development of sensing devices.

Moreover, several additional processes resulted as fruitful byproducts of the main process flow:

- Self-assembly on a free surface of PS-b-PMMA was also successfully carried out on SiO_2 substrates.

- A dry etching recipe based on C_4F_8 was developed for the pattern transfer of PS nanopatterns onto SiO_2. Obtained silicon oxide structures presented at least 12 nm of height.

- SIS was successfully performed by infiltrating PS-b-PMMA with Al_2O_3 by ALD. Then, dry etching recipes were re-adjusted for pattern transfer of the infiltrated mask onto Si, obtaining silicon fins and pillars with heights in the 50-nm range.

Although the objective of this work was focused on the fabrication process, initial characterization results on obtained devices are included:

- FEM simulations were executed, confirming device eigenfrequencies belonged in an adequate frequency range for their characterization as nanomechanical resonators.

- LDV measurements were performed to optically characterize the resonance frequency of obtained devices. These resulted in damaged membranes due to the elevated power of the laser available.

- Additional measurements were carried out by AFM and amplitude modulation, although the small quality factor of devices in air did not allow for resonance detection.

Future work to follow up the results obtained in this thesis would include additional optimization of the dry etching recipes to obtain attacks even more anisotropic, and the incorporation of a doping step in the process flow, in order to obtain conductive nanowires and membranes that enable electric excitation.

As a final conclusion, this work has shown that DSA of BCPs can be used for the definition of functional nanomechanical structures, which can be exploited for the development of sensor and NEMS devices.

Appendix I

Multilayer lift-off after PS-b-PMMA self-assembly for sub-15-nm patterning

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In this appendix a method that allows the patterning of gold nanostructures of less than 15 nm of lateral resolution is reported. In the process, an inorganic-organic multilayer allows lift-off of the metal after previous PS-b-PMMA self-assembly and pattern transfer of the nanopatterns onto a hard mask.

AI.1 INTRODUCTION

Gold nanostructuring is important in the fabrication of sensing, nano-optics and plasmonics devices [1], [2], [3] and both bottom-up and top-down high-resolution nanopatterning techniques have been demonstrated [4], [5], [6]. As we have discussed throughout this thesis, BCP self-assembly is an affordable bottom-up nanolithography technique that allows very high-resolution, so in principle it would be appealing for the nanopatterning of Au. However, direct pattern transfer of block copolymers onto a non-volatile metal like Au (also Cu or Pt) is not easy. Its low volatility during dry etching complicates the transition from the surface to gas phase, and generates a tendency to redeposit on the substrate or mask [7]. In the case of pattern transfer using PS-b-PMMA, an increase in the influence of milling during RIE can assist by removing metal in a more physical way, but at expense of severely debilitating the BCP mask, which might eventually give in.

On the other side, lift-off of Au using BCPs as has already been demonstrated for the fabrication of vertical SiNWs [8], for instance. Still, the use of BCPs for lift-off processes in general is difficult to control due to the absence of undercuts in the profile of the mask [9]. In addition, the thickness of the BCP thin film restrains metal deposition to very few nanometers and problems in the lift-off might occur due to partial coating of the template layer walls [10], [11].

In this appendix a simple multilayer stack configuration is present, which allows the fabrication of metal nanostructures of less than 15 nm of lateral resolution by PS-b-PMMA self-assembly and lift-off. The use of this multilayer stack can help overcome the limitations mentioned above, as it is possible to produce higher aspect ratios than with the BCP alone, thanks to the increased thickness, and undercuts, thanks to the different selectivity of the layers in dry etching [9].

The multilayer stack consists of a thin film of PMMA, a sacrificial layer of SiO_2 and a layer of self-assembled PS-b-PMMA on top. The SiO_2 middle layer allows a self-assembly performance similar to that of the BCP on silicon, a successful pattern transfer of the fine structures from the BCP template, and provides a hard mask for the

etching of PMMA to obtain small undercuts to facilitate the lift-off process [12]. The full process is shown in figure I.1.

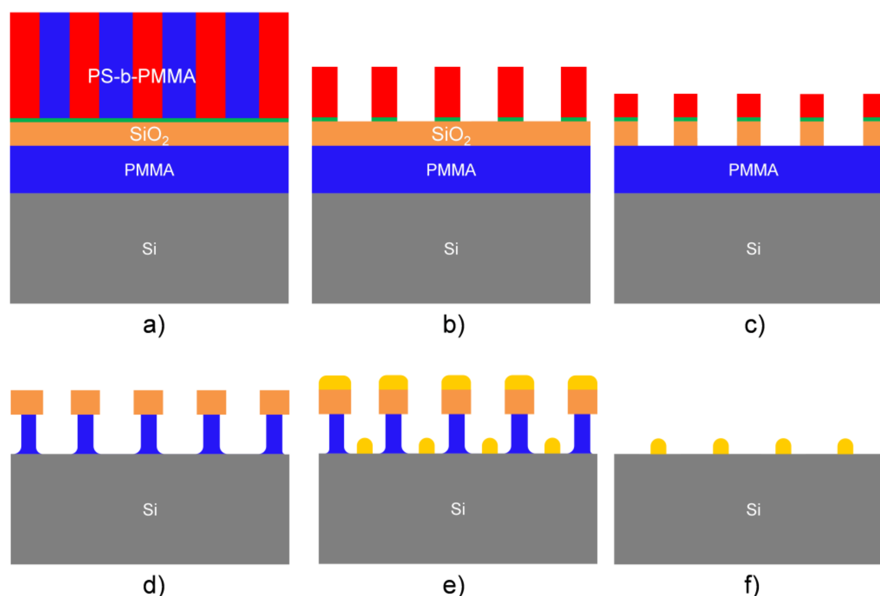

Figure I.1. a) Multilayer stack for lift-off. In b), PMMA in PS-b-PMMA is selectively removed in Ar/O_2 plasma. Then, SiO_2 is patterned with the remaining PS mask (c). PMMA is etched to obtain undercuts (d) and metal is deposited by evaporation (e). Sonication mechanically removes the Au on the template, while leaving the metallic pattern on silicon (f).

AI.2 BUILD UP OF THE MULTILAYER

Starting substrates were {100} silicon (p-type, 4-40 Ω·cm) chips of 5 × 5 cm^2 that were cleaned in acetone and IPA, and activated by oxygen plasma for 5 minutes at 600 W. First, a PMMA 950K (1% in Anisole, MicroChem Corp., USA) thin film was spun for 1 minute at 5000 rpm, followed by annealing for 1 minute at 180 ºC on a hot-plate. The thickness of the film was measured at 25 nm by reflectometry (Nanospec AFT/4150, Nanometrics, USA), taking into account 2.5 nm of native SiO_2.

On top, a 10-nm SiO_2 layer was deposited by PECVD in an Oxford Plasmalab tool (Oxford Instruments, UK) following the parameters shown in table I.1. Tests to calibrate oxide thickness were carried out and results are shown in table I.2.

As previously detailed in this thesis, a $PS_{60\%}$-r-PMMA neutral brush layer was used to ensure self-assembly took place in vertical lamellae, evening the surface free energy to PS and PMMA. After annealing for 48 hours inside a vacuum oven at 150 ºC, the non-grafted brush was removed by repeatedly spin-coating PGMEA. The final thickness of the brush film was approximately 8 nm. Finally, a 2 wt. % PGMEA solution of lamellar PS-b-PMMA (L_0 = 37 nm) was spin-coated at 2000 rpm for 1 minute and annealed for

24 hours inside a vacuum oven at 150 ºC, as well. Final combined BCP and brush thickness was 59 nm, and the final result can be observed in figure I.2.

TABLE I.1
PROCESS PARAMETERS FOR PECVD OF SILICON OXIDE THIN FILMS

T (ºC)	P (Torr)	SiH_4 (sccm)	N_2 (sccm)	N_2O (sccm)	RF (W)
150	1	25	955	1000	100

TABLE I.2
PECVD PROCESSING TIME AND CORRESPONDING OXIDE THICKNESS

Time (s)	Thickness (nm)
4	3.3
6	6.6
8	8.4
10	10.2

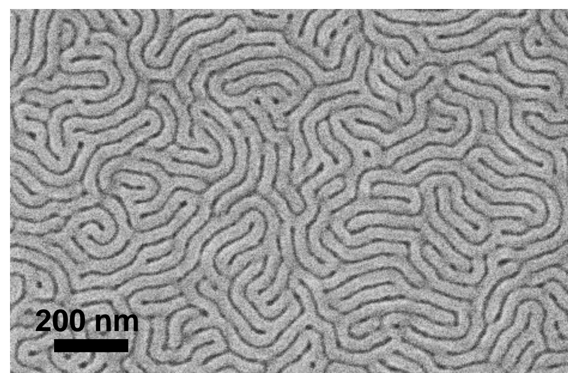

Figure I.2. SEM top-view micrograph after PS-b-PMMA self-assembly (L_0 = 37 nm) on top of the stack.

Differently to the experiments exposed in chapters 3 and 4, both neutral layer and BCP annealings were performed at 150 ºC instead of 230 and 265 ºC, respectively. PECVD of the SiO_2 thin film was also carried out at 150 ºC. The main reason behind this was to avoid damage of the bottom PMMA lift-off layer, as PMMA loses thermostability and starts to degrade in the 200-240 ºC temperature range [13], [14], [15]. In addition, when PMMA is exposed to high processing temperatures it can be prone to toughening, what could hinder the lift-off process [16]. Annealing times were increased to try to compensate for the lower temperatures, but shorter range order in microphase segregation could not be avoided.

AI.3 ETCHING OF THE STACK AND LIFT-OFF

After self-assembly, PMMA blocks from PS-b-PMMA, as well as the brush layer, were selectively removed by ICP-RIE in Ar/O_2 plasma, using the parameters shown in table I.3. The remaining PS blocks, with an approximate thickness of 32 to 35 nm, were transferred onto the silicon oxide sacrificial layer by dry etching with C_4F_8, with the parameters shown in table I.4. In a third ICP-RIE step, the bottom PMMA layer was etched with SiO_2 as a hard mask using the parameters in table I.5. A SEM micrograph of the cross-section after this step, prior to metal evaporation, is shown in figure I.3.

TABLE I.3
PROCESS PARAMETERS FOR SELECTIVE PMMA REMOVAL IN PS-b-PMMA BY ICP-RIE

T (ºC)	P (Pa)	O_2 (sccm)	Ar (sccm)	RF1 (W)	RF2 (W)	Time (s)
20	1.33	10	200	200	5	41

TABLE I.4
PROCESS PARAMETERS FOR SILICON OXIDE ETCHING BY ICP-RIE

T (ºC)	P (Pa)	C_4F_8 (sccm)	RF1 (W)	RF2 (W)	Time (s)
20	2	45	450	60	12

TABLE I.5
PROCESS PARAMETERS FOR PMMA ETCHING BY ICP-RIE

T (ºC)	P (Pa)	O_2 (sccm)	Ar (sccm)	RF1 (W)	RF2 (W)	Time (s)
20	1.33	10	200	200	5	19

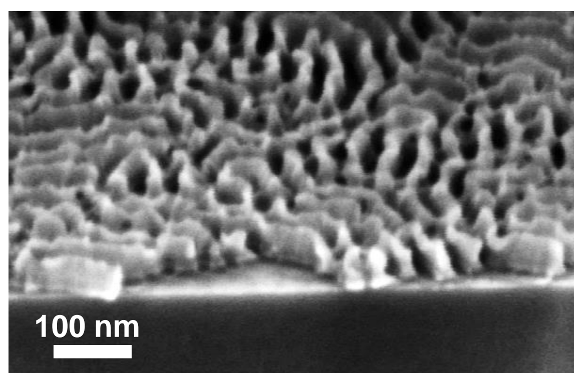

Figure I.3. SEM tilted (30º) image after consecutive etching steps to open the multilayer. Final total mask thickness for lift-off is between 40 and 45 nm.

A metal bilayer consisting of 3 nm of Cr and 9 nm of Au was deposited by e-beam evaporation, followed by ultrasonic lift-off for 5 minutes in acetone, to remove PMMA. The effectiveness of the multilayer stack as a lift-off mask was demonstrated by the successful fabrication of gold nanopatterns (figure I.4).

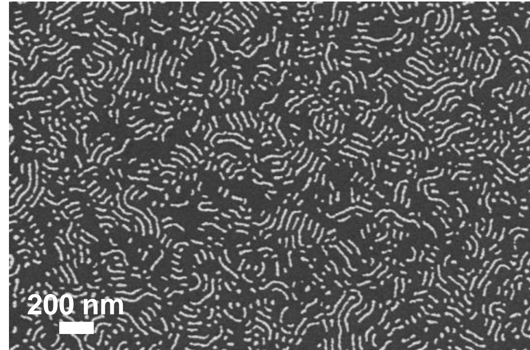

Figure I.4. SEM top-view image after evaporation of the Cr/Au thin film and sonication in acetone for lift-off.

Nevertheless, certain areas of the sample were missing nanostructures due to an incomplete opening of the multilayer lift-off mask. The main hypothesis to this event is linked to a lack of uniformity in the PECVD of SiO_2 for such short processing times. In addition, eventual lift-off-related defects were also observed, as shown in figure I.5. These were associated to partial coating of the template walls.

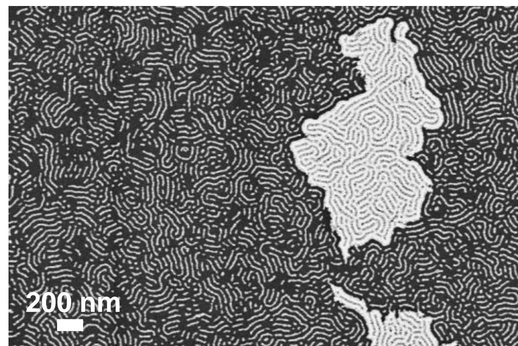

Figure I.5. In certain isolated areas lift-off was not successful despite sonication, due to partial coating of the template walls.

AI.4 CONCLUSIONS

In this appendix a strategy to create gold nanopatterns by a lift-off approach was demonstrated. A multilayer thin-film stack consisting of PMMA, silicon oxide and PS-b-PMMA was used, which allowed obtaining the essential undercuts needed for a successful and clean lift-off.

Obtained metal patterns presented sub-15 nm lateral resolution limited by the BCP used in the top layer, in this case 37-nm pitch PS-b-PMMA. Metal pattern thickness

was restricted to 12 nm (3 nm of Cr for adhesion and 9 nm of Au), to maintain a safe 1:3 ratio between deposited film and sacrificial layer thickness.

Higher aspect ratio structures are potentially possible by employing a BCP with a smaller natural period and thicker layers in the multilayer stack, although as consequence, the ICP-RIE processes would need to be tuned and/or new recipes considered. The development of a PECVD process that results in the deposition of more uniform silicon oxide thin films would help to avoid uneven etching times along the substrate.

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Appendix II

Metallization over fins obtained after pattern transfer of PS-b-PMMA

In this appendix the deposition of thin films over silicon structures obtained after pattern transfer of PS-b-PMMA is reported. Both chemical and physical deposition methods were employed to deposit materials typically associated with transistor gate stacks over silicon fins obtained by the processes developed in chapter 3.

AII.1 INTRODUCTION

As introduced in chapter 1, transistor scaling requirements to fulfill Moore's Law have motivated the semiconductor industry to move from planar CMOS towards 3D FinFETs. This architecture offers the possibility of higher packing density and better drive current, since it is possible to create a channel over three surfaces. To do so, it is necessary to build a gate stack that fully covers the structure, by uniformly depositing thin films on each of the three sides of the fin. The inability to do so, affects device performance, threshold voltage and work function [1].

Continuous scaling has also influenced materials used in gate stacks, and high-κ dielectrics and metals are used to avoid leakage, gate depletion and connect the device with upper levels [2], [3], [4], [5]. Among metals, TiN is the most popular thanks to its mechanical and thermal stability, low electrical resistivity, compatibility with high-k dielectrics and the possibility of tuning its work function with film thickness [6], [7].

The goal of the experiments shared in this appendix was to prove the possibility of metalizing silicon structures (figure II.1) that could potentially be used for the development of FinFETs. To do so, thin film processing tests with materials such as Al, W, TiN and HfO_2 were performed over silicon fins obtained in chapter 3.

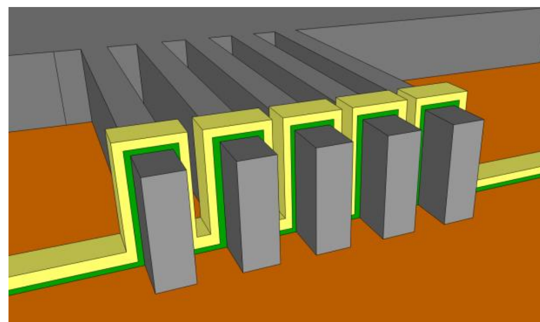

Figure II.1. The most basic FinFET structure would be comprised by a silicon fin, a gate oxide (green) and a metal gate (yellow).

Three different techniques were used to deposit the thin films of interest: magnetron sputtering (TiN), e-beam evaporation (Al and W) and ALD (HfO_2 and TiN). The two first are physical vapor deposition techniques (PVD) while ALD is a derivative of chemical vapor deposition.

In PVD techniques a thin film is grown on a substrate by atomizing or vaporizing material from a solid target in vacuum [8]. Thin films obtained can present thicknesses between some nanometers to several microns, and their properties can also be affected by the type of substrate. Deposition of a high diversity of materials is possible with good adhesion and controlled morphology [9].

Magnetron sputtering is a commonly-used PVD method in the semiconductor and hard-coating industries. In the process, a target is bombarded with argon ions accelerated by high voltage generating plasma. With this bombarding, atoms from the target are physically ejected by momentum transfer and deposited on the substrate. The biggest disadvantages are a low deposition rate, lack of directionality and a characteristic line-of-sight deposition, which makes the coating of deep holes and trenches difficult [10].

In e-beam evaporation the target acts as source and is heated at high vapor pressure by the bombardment of electrons. Argon is introduced in the vacuum chamber to generate plasma and accelerate the particles towards the substrate, successively depositing layers of compressed material in a very directional way [11], [12].

Lastly, in ALD reactants are introduced in a vacuum chamber sequentially in independent pulse steps, separated by a purge step. The technique gives the possibility of depositing monoatomic conformal layers of great uniformity [13].

AII.2 ALD OF HAFNIA AND SPUTTERING OF TiN

The coupling of HfO_2 with TiN has been successfully used in high-κ/metal gate technology, thanks to the thermal stability of the pair, low resistivity and compatibility to conventional CMOS processing [6], [7].

Firstly, silicon chips of 2×2 cm^2 containing transferred fins of 35 to 45 nm of height were cleaned in oxygen plasma to remove any possible remains of BCP. They were then dipped in HF to remove native oxide, followed by the deposition of 2 nm of hafnia via ALD (Savannah 200, Cambridge Nanotech, USA). Finally, 8 nm of TiN were deposited by sputtering at a chamber pressure of 1 Pa (KS800H, Kenosistec, Italy). The TiN thin film was simultaneously deposited on a blank control substrate, and laid an electrical resistivity of $1.28 \cdot 10^{-5}$ Ω·cm by the four-point probes method.

As it can be observed in figure II.2, HfO_2 successfully covered the structures while TiN did not penetrate in between fins. We attribute this to the nature of the sputtering process that, although known for being an isotropic deposition method, presents problems when trying to cover high aspect ratio structures or deep trenches [14]. In this case, the accumulation of TiN on top of the fins simply did not allow any material to enter the inter-fin space.

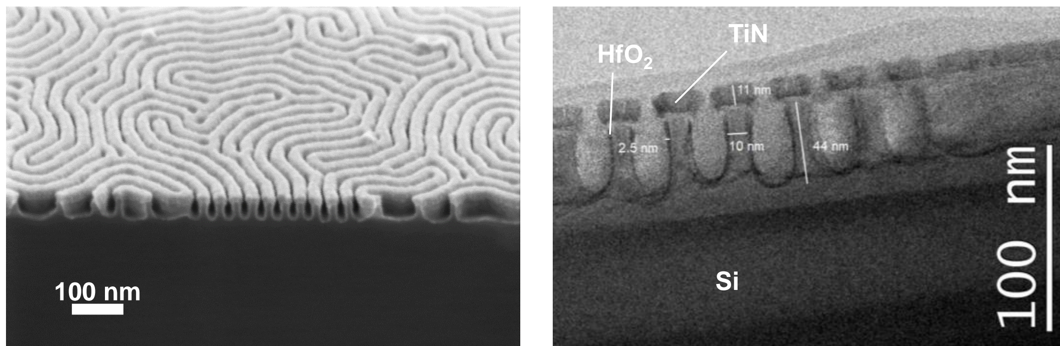

Figure II.2. SEM tilted (30º), left, and TEM, right, micrographs of the deposition of 2 nm of hafnia and 8 nm of sputtered TiN over silicon fins.

AII.3 EVAPORATION OF Al AND W

To study the possibility of defining Al and W contacts over the fins, 20 nm of both metals were deposited by evaporation (Univex 450B, Oerlikon, Switzerland) directly on silicon. As observed in figure II.3, evaporation was more directional than sputtering (as expected), and some metal was successfully deposited in the bottom of the trenches. Nevertheless, material directly deposited on top of the fins resulted in the closing of the apertures in a clogging effect than precluded complete filling of the space between fins.

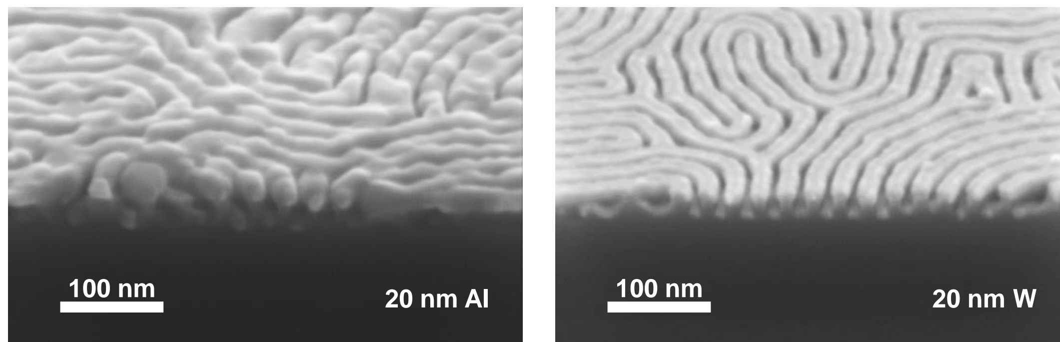

Figure II.3. SEM tilted (30º) micrographs of the evaporation of 20 nm of Al and W over fins.

AII.4 ALD OF TiN

In a final run of experiments, silicon chips with patterned fins and bearing native oxide were sent to the CoCooN research group from Ghent University, where a thin film of 8 nm of TiN by was deposited by ALD.

TiN was deposited at 100 ºC, with NH_3 as precursor and at a power of 250 W. The TiN thin film was also deposited on a control chip, which laid an electrical resistivity of 1.25 $\cdot 10^{-5}$ Ω·cm by the four-point probes method. As shown in figure II.4, the deposition of

TiN by ALD rendered a perfect covering of the three sides of each of the fins, thanks to the conformal nature of ALD.

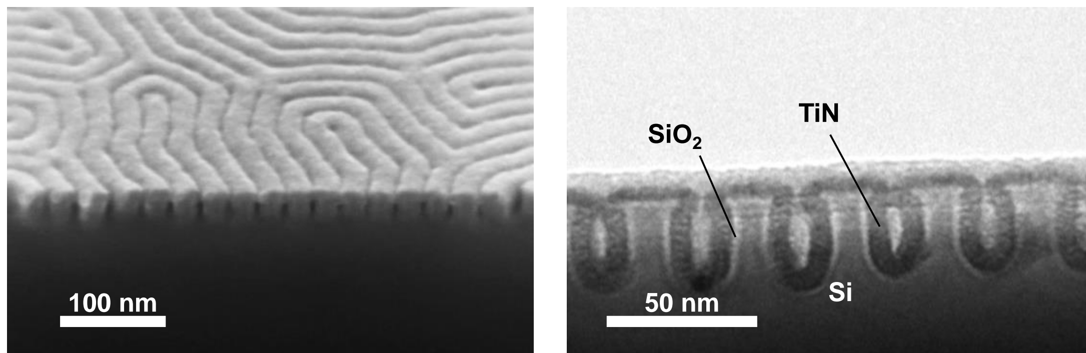

Figure II.4. SEM tilted (30º), left, and TEM, right, micrographs of the deposition of 8 nm of TiN by ALD over silicon fins bearing native oxide.

AII.5 CONCLUSIONS

Experimental results show that fins obtained after pattern transfer of PS-b-PMMA templates onto silicon could be used as the building block of FinFETs by carefully choosing the deposition techniques to create the gate stack.

Due to the reduced dimensions and the small periods, ALD needs to be the primary thin film deposition technique used for the fabrication of a high-κ/metal gate stack. Thanks to its conformability, both hafnia and TiN deposited by ALD perfectly covered the three sides of the fins, which could not be attained by sputtering and evaporation.

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Appendix III

Scientific contributions

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1. **PAPER: Directed self-assembly of block copolymers for the fabrication of functional devices**
   C. Pinto-Gómez, F. Pérez-Murano, J. Bausells, Luis Guillermo Villanueva and M. Fernández-Regúlez
   2020, Polymers, 12 (10), 2432

2. **PAPER: Self-assembly of block copolymers under non-isothermal annealing conditions as revealed by grazing incidence small-angle X-ray scattering**
   M. Fernández-Regúlez, E. Solano, L. Evangelio, S. Gottlieb, C. Pinto-Gómez, G. Rius, J. Fraxedas, E. Gutiérrez, A. Nogales, M.C. García-Gutiérrez, T. Ezquerra, and F. Pérez-Murano
   2020, Journal of Synchrotron Radiation, 27 (5), 1278-1288

3. **POSTER: In situ characterization of block copolymer self-assembly kinetics**
   M. Fernández-Regúlez, E. Solano, C. Pinto-Gómez, S. Gottlieb, E. Gutiérrez, A. Nogales, M.C. García-Gutiérrez, T. Ezquerra, J. Fraxedas, and F. Pérez-Murano
   2019, 5th International Symposium on DSA, Milan, Italy

4. **ORAL: Block copolymer self-assembly kinetics by GISAXS**
   M. Fernández-Regúlez, E. Solano, C. Pinto-Gómez, S. Gottlieb, E. Gutiérrez, A. Nogales, M.C. García-Gutiérrez, T. Ezquerra, J. Fraxedas, and F. Pérez-Murano
   2019, IX AUSE Conference, Bellaterra, Spain

5. **POSTER: Arrays of doubly-clamped silicon nanowires defined by directed self-assembly of block copolymers**
   C. Pinto-Gómez, F. Pérez-Murano, J. Bausells, and M. Fernández-Regúlez
   2019, 16th International Workshop on Nanomechanical Sensors (NMC), Lausanne, Switzerland

6. **ORAL: Self-assembly methods for nanoelectronics**
   F. Pérez-Murano, L. Evangelio, S. Gottlieb, M. Fernández-Regúlez, C. Pinto-Gómez, E. Amat, A. Del Moral, and J. Bausells
   2019, NanoSpain Conference 2019, Barcelona, Spain

7. **PAPER: Synchrotron radiation for the understanding of block copolymer self-assembly**
   M. Fernández-Regúlez, C. Pinto-Gómez, and F. Pérez-Murano,
   2019, Journal of Photopolymer Science and Technology, 32 (3), 423-427

8. **ORAL: Extracting block copolymer dynamics from GISAXS**
   M. Fernández-Regúlez, E. Solano, S. Gottlieb, C. Pinto-Gómez, L. Evangelio, G. Rius, J. Fraxedas, F. Pérez-Murano, H. Amenitsch, E. Gutiérrez, A. Nogales, M.-C. García-Gutiérrez and T. Ezquerra
   2018, 4th International Symposium on DSA, Sapporo, Japan

9. **ORAL: Directed self-assembly of block copolymers for the fabrication of nanowire-based electromechanical devices**
   C. Pinto-Gómez, R. Mas, F. Pérez-Murano, J. Bausells, and M. Fernández-Regúlez
   2018, 4th International Symposium on DSA, Sapporo, Japan

10. **ORAL: Directed self-assembly of block copolymers for the fabrication of FinFETs and nanomechanical devices**
    C. Pinto-Gómez, R. Mas, F. Pérez-Murano, J. Bausells, and M. Fernández-Regúlez
    2018, 44th International Conference on Micro and Nanoengineering (MNE), Copenhagen, Denmark

11. **POSTER: Nanowire device fabrication by optical lithography and directed self-assembly of block copolymers**
    M. Fernández-Regúlez, L. Evangelio, C. Pinto-Gómez, S. Gottlieb, J. Bausells, and F. Pérez-Murano
    2018, E-MRS 2018 Spring Meeting, Strasbourg, France

12. **POSTER: Fabrication of FinFETs based on the directed self-assembly of block copolymers**
    C. Pinto-Gómez, L. Evangelio, F. Pérez-Murano, J. Bausells, and M. Fernández-Regúlez
    2017, 3rd Scientific Meeting of BNC-b students, ICMAB, Bellaterra, Barcelona, Spain

13. **ORAL: FinFET fabrication by the combination of electron beam lithography and directed self-assembly of block copolymers**
    C. Pinto-Gómez, L. Evangelio, F. Pérez-Murano, J. Bausells, and M. Fernández-Regúlez
    2017, 7th Spanish Workshop in Nanolithography, IMDEA, Madrid, Spain