Universitat Autònoma de Barcelona

Modelling and Physical Design Automation for Organic and Printed Devices and Circuits

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Ph.D. Thesis Dissertation

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I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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Si tant busques busques,

al final trobes trobes.

Josep López, “Lopes”

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Abstract

In recent years, the interest in the manufacture of low-cost electronic systems has been on the rise due to increasing efforts of using sensors in Smart Cities and Industry 4.0. Multiple low-cost applications are beginning to appear, such as RFID stickers for product identification, flexible displays, or smart tags among others. Due to this need, Organic and Printed Electronics has positioned itself as an alternative technology to silicon with competitive advantages thanks to innovative materials and manufacturing methods in the world of electronics, allowing the production of low-cost, flexible, lightweight, large area and biodegradable devices. Despite this interest, there is still a lot of work to be done related to device modeling, design and simulation of complex circuits.

This thesis focus on the development of a Process Design Kit (PDK) with the necessary methodologies for the elaboration of an industrial model, which incorporates the DC and AC behavior of organic transistors, combined with the variations introduced by environmental factors and the intrinsic variability of the device. The PDK has been developed with a large automatic component, so it can evolve at the same time as the organic devices to be used.

Within the framework of the thesis, an automatic electrical characterization environment has been developed with an output that provides the reports of devices and models allowing the analysis of a large number of transistors and their parameters. At the same time, a study of how it is affected by different external factors such as light, humidity or temperature, and the incidence of the application over and over again of potentials in the terminals has been done. The physical design part of the PDK is based on a set of Parameterized Cells (PCells), made in such a way that they are correct by design and combined with automatic methods allow the generation of arrays of devices and circuits in a reduced time. Multiple different devices and circuits have been made following this methodology in order to be able for characterization and modeling using the tools developed in the PDK.

The results of this thesis have allowed applying the knowledge in two different manufacturers of organic devices with the aim of design flexible systems. One of the great achievements of this thesis is the simulation and design of a 16-bit RFID tag developed by using organic technology and based on the methods developed and implemented in the developed PDK. On the other hand, the implemented tool allows following the evolution of the devices without a greater intervention on it, allowing advancing with new devices, creating and parameterizing models without great efforts.

Resum

Durant aquests darrers anys, l'interès per la fabricació de sistemes electrònics de baix cost ha anat augmentant degut a l'esforç en la sensorització de les ciutats intel·ligents i la indústria 4.0. Han anat apareixent múltiples aplicacions de baix cost, com per exemple, adhesius RFID per la identificació de productes, pantalles flexibles o etiquetes intel·ligents entre d'altres. Per aquesta necessitat, l'Electrònica Orgànica i Impresa s'ha posicionat com a tecnologia alternativa al silici amb uns avantatges competitius importats gràcies als materials i mètodes de fabricació innovadors en el món de l'electrònica, permetent l'elaboració de dispositius de baix cost, flexibles, lleugers, de gran àrea i biodegradables. Tot i aquest interès, hi ha molta feina encara per fer en relació amb el modelatge de dispositius, el disseny i la simulació de circuits complexos.

Aquesta tesi està enfocada al desenvolupament d'un Process Design Kit (PDK) amb les metodologies necessàries per a l'elaboració d'un model industrial que incorpora el comportament DC i AC dels transistors orgànics, combinat amb les variacions introduïdes pels factors ambientals i la variabilitat intrínseca del dispositiu. El PDK s'ha desenvolupat amb una gran component automàtica, de tal forma que pugui evolucionar en paral·lel als dispositius orgànics a ser usats.

En el marc de la tesi s'ha desenvolupat un entorn de caracterització elèctrica automàtica que genera informes dels dispositius i dels models permetent l'anàlisi de gran quantitat de dispositius i els seus paràmetres. Al mateix temps, s'ha dut a terme un estudi de com l'afecten els diferents factors externs com la llum, humitat o temperatura, i la incidència de l'aplicació de potencials en els terminals de forma repetitiva. La part de disseny físic del PDK està basat en un conjunt de cel·les parametritzades (PCells) elaborades de tal forma que siguin correctes per disseny i que combinades amb mètodes automàtics permeten la generació de matrius de dispositius i circuits en un temps reduït. S'han realitzat múltiples dispositius i circuits diferents seguint aquesta metodologia per tal de poder ser caracteritzats i modelats usant les eines desenvolupades en el PDK.

Els resultats d'aquesta tesi han permès aplicar els coneixements en dos fabricants de dispositius orgànics amb l'objectiu de dissenyar circuits orgànics. Un dels grans assoliments d'aquesta tesi és la simulació i disseny d'una etiqueta RFID de 16 bits elaborada mitjançant tecnologia orgànica i basada en els mètodes desenvolupats i implementats en el PDK desenvolupat. Per altra banda, l'eina implementada permet seguir l'evolució dels dispositius sense una intervenció major en la mateixa, permetent avançar amb els nous dispositius, creant i parametritzant models sense grans esforços.

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Glossary

AC	Alternating Current
ALU	Arithmetic Logic Unit
AMS	Analog and Mixed Signal
BB	Black Box
BGBC	Bottom Gate Bottom Contact
BGTC	Bottom Gate Top Contact
CANCER	Computer Analysis of Nonlinear Circuits, Excluding Radiation
CD	Channel Dimension
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CNM	Centro Nacional de Microelectrónica
CRC	Cyclic Redundancy Check
CS	Common Source
CSIC	Consejo Superior de Investigaciones Científicas
CTFT	Corbino Organic Thin Film Transistor
CuO	Copper Oxide
C-V	Capacitance Voltage
DC	Direct Current
DFSA	Dynamic Frame Slotted Aloha
DIKW	Data, Information, Knowledge and Wisdom
DOD	Drop On Demand
DOS	Density Of States
DRC	Design Rules Check

EDA	Electronic Design Automation
EGOTFT	Electrolyte Gated OTFT
ERC	Electrical Rule Check
FDMA	Frequency Division Multiple Access
FET	Field-Effect Transistor
FSA	Frame Slotted Aloha
GB	Gray Box
GPIB	General-Purpose Instrumentation Bus
HF	High Frequency
IC	Integrated Circuit
ICAS	Circuitos Integrados y Sistemas
ID	Identification
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IMB	Institut de Microelectrònica de Barcelona
IoT	Internet of Things
ISE	Integral Square Error
ISO	International Organization for Standardization
ITO	Indium Tin Oxide
I-V	Current Voltage
KIT	Karlsruher Institut für Technologie
KIT	Karlsruher Institut für Technologie
LED	Light Emitting Diode
LF	Low Frequency
LSB	Less Significant Bit

LVS	Layout Versus Schematic
MAPE	Mean Absolute Percentage Error
MASE	Mean Absolute Scaled Error
MIS	Metal-Insulator-Semiconductor
MNR	Meyer Neldel Rule
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MS	Metal-Semiconductor
MSE	Mean Squared Error
MTR	Multiple Trapping and Release
NFC	Near Field Communication
NiO	Nickel Oxide
NTU	Nanyang Technological Univesrity
OE	Organic Electronics
OGI	Organic Gate Insulator
OLED	Organic Light-Emitting Diode
OPDK	Organic Process Design Kit
OPV	Organic Photovoltaics
OSC	Organic Semiconductor
OTFT	Organic Thin Film Transistor
P&R	Place and Route
PA	Pure Aloha
PCell	Parametric Cell
PDK	Process Design Kit
PE	Printed Electronics

PEX	Parasitic parameter Extraction
PISO	Parallel Input and Serial Output
POC	Point-Of-Care
PROM	Programmable Read Only Memory
RFID	Radio Frequency Identification
RH	Relative Humidity
RLC	Resistance, Inductance and Capacitance
RMSE	Root Mean Square Error
ROM	Read Only Memory
RSD	Relative Standard Deviation
RTL	Register-Transfer Level
SA	Slotted Aloha
SAM	Self-Assembled Monolayer
SDMA	Space Division Multiple Access
SGT	Source Gated Transistors
SMAPE	Symmetric Mean Absolute Percentage Error
SMU	Source Measure Unit
SPI	Standard Commands for Programmable Instruments
SPICE	Simulation Program with Integrated Circuits Emphasis
SRL	Sputter Resistant Layer
TDMA	Time Division Multiple Access
TFT	Thin Film Transistor
TGBC	Top Gate Bottom Contact
TGTC	Top Gate Top Contact
UHF	Ultra High Frequency

UOTFT	Universal Organic Thin Film Transistor
UV	Ultraviolet
VRH	Variable Range Hopping
VTC	Voltage Transfer Characteristics
WB	White Box

List of symbols

A	Area
b_0	Bit at LSB position
C	Capacitance
C_{GD}	Gate drain capacitance
C_{GS}	Gate source capacitance
C_{ins}	Insulator capacitance
C_{OX}	Gate capacitance
E_C	Conduction band
E_D	Electron donor
E_F	Fermi level
E_V	Valence band
g_{DS}	Output Conductance
g_m	Transconductance
GND	Ground
I_0	Input at LSB position
I_D	Drain current
I_{ON}/I_{OFF}	On/off current ration
I_{SD}	Source drain current
J_D	Current density
J_S	Saturation current density
L	Channel length
n	Free electron concentration
NF	Number of fingers

n_i	Intrinsic carrier concentration
O_0	Output at LSB position
p	Free hole concentration
r_0	Output resistance
R_1	Interior Corbino radius
R_2	Exterior Corbino radius
R_D	Drain resistance
R_{OFF}	Off resistance
R_{OSC}	Semiconductor resistance
R_{OUT}	Output resistance
R_S	Source resistance
SS	Subthreshold slope
t_{ins}	Insulator thickness
V_{BG}	Back gate voltage
V_D	Drain voltage
V_G	Gate voltage
V_{IN}	Input voltage
V_{OUT}	Output voltage
V_{SD}	Source drain voltage
V_{SG}	Source gate voltage
V_{SS}	Supply voltage
V_T	Threshold voltage
V_{TH}	Thermal voltage
W	Channel width
ΔL	Channel length reduction

ε_0	Vacuum permittivity
ε_R	Relative permittivity or dielectric constant
η	Diode emission coefficient
λ	Channel length modulation
μ	Device mobility
μ_{eff}	Device effective mobility
μ_{lin}	Device linear mobility
μ_{sat}	Device saturation mobility
Φ	Surface inversion potential

1 Dissertation Summary

The competition in the electronics field had led the industry to achieve high level of optimization in device manufacturing and performance, with extreme device density for offering products with a reduced cost. Regards the optimization work in all the different areas, the silicon electronics devices still require of expensive fabrication techniques and materials. This situation has limited the development of very cheap electronic solutions and large area electronics devices.

1.1 Objectives of the thesis

Currently, Organic Electronics (OE) manufacturing technologies still lack standardized procedures, despite the fact that the Institute of Electrical and Electronics Engineers (IEEE) and International Electrotechnical Commission (IEC) are promoting the development of methodologies for this technology. This absence of standardization is also present in the design flow step, where different Electronic Design Automation (EDA) tools and models have worked successfully following the same methodology as in silicon-based technology.

EDA tools have been the base for the current microelectronic industry since they have allowed the design of more and more complex systems that include a massive number of devices, in a reduced design time. The methodology of EDA tools can be implemented independently of the manufacturing technology used, and thus, for this reason, EDA tools have been widely standardized. Process Design Kits (PDK) are developed for connecting the EDA tools with the fabrication techniques using a set of data files, libraries, scripts, and rule sets containing the

specific information of the fabrication and technology used. Based on this, the PDKs provides inputs for supporting the different layers of the EDA software.

The main objectives of this thesis are the modelling and layout design of organic devices for an automatic PDK generation. Focusing to develop a reliable automatized system and a robust model for circuit design that allows a continuous evolution of the models with a minimum effort, different sub-objectives had been identified and defined:

- Elaboration of automatic methodologies and tools for the characterization of electronic devices with the extraction of key parameters for the generation of compact models for circuit simulation. Moreover, automatic methods for layout design should be included.
- Study of the parameter variability and degradation of the Organic Thin Film Transistors (OTFT) and other electronic devices for compact model support. These devices parameters have not been well studied in this type of devices and variability, degradation over time and variation respect to environmental conditions (light, temperature or humidity) need to be investigated.
- Development of an industrial compact model for the OTFT device with Alternating Current (AC) and Direct Current (DC) behaviour including parameter variability and the and non-idealities presented by the devices.
- Implementation of alternative design strategies for the realization of reliable circuits with devices of high variability.
- Design of systems based on organic electronics for the realization of analog and digital circuits with the models and design strategies developed.

1.2 List of publications

During the elaboration of this thesis different publications in journals, conferences and collaborations had been done:

- **A. Arnal**, L. Terés, and E. Ramon, “Organic and printed process design kits: review, analysis and comparison,” *Flex. Print. Electron.*, vol. 6, no. 3, p. 33001, 2021, doi: 10.1088/2058-8585/ac1d39.
- **A. Arnal**, A. Crespo-Yepes, E. Ramon, L. Terés, R. Rodríguez, and M. Nafría, “DC characterization and fast small-signal parameter extraction of organic thin film transistors with different geometries,” *IEEE Electron Device Lett.*, vol. 41, no. 10, pp. 1–1, 2020, doi: 10.1109/led.2020.3021236.

- **A. Arnal**, C. Martínez-Domingo, S. Ogier, L. Terés, and E. Ramon, “Monotype Organic Dual Threshold Voltage Using Different OTFT Geometries,” *Crystals*, vol. 9, no. 7, p. 333, 2019, doi: 10.3390/cryst9070333.
- **A. Arnal**, L. Terés, and E. Ramon, “An organic process design kit, from characterization to modelling and simulation,” *Proc. - 2020 IEEE 8th Electron. Syst. Technol. Conf. ESTC 2020*, 2020, doi: 10.1109/ESTC48849.2020.9229883.
- G. C. Marques, A. M. Sukuramsyah, **A. Arnal**, S. Bolat, A. Aribia, X. Feng,S. A. Singaraju, E. Ramon, Y. Romanyuk, M. Tahoori and J. Aghassi-Hagmann “Fabrication and Modeling of pn-Diodes Based on Inkjet Printed Oxide Semiconductors,” *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 187–190, 2020, doi: 10.1109/LED.2019.2956346.
- G. C. Marques, A. Birla, **A. Arnal**, S. Dehm, E. Ramon, M. B. Tahoori and J. Aghassi-Hagmann, “Printed Logic Gates Based on Enhancement- And Depletion-Mode Electrolyte-Gated Transistors,” *IEEE Trans. Electron Devices*, vol. 67, no. 8, pp. 3146–3151, 2020, doi: 10.1109/TED.2020.3002208.

1.3 Thesis outline

Following the objectives that steered the course of this thesis, the dissertation is organized in seven different chapters summarized below.

1. **Dissertation Summary**: provides a brief introduction of the organization, scientific contributions, work done and the different activities and rewards connected with this thesis.
2. **State of the Art**: is devoted to introduce the basics of the organic electronics field involving the materials, fabrication techniques and main applications. Moreover, this chapter also provides a background to the automation system basics combined with processes design kit needs.
3. **Layout Design**: focused on the automation of the layout step based on Parametric Cells (PCells) and the different EDA tools for layout verification and the development of a layout means different technology validators and test structures implemented in two different layout editors and manufacturers.
4. **Device Modelling**: the chapter involves the basis of characterization and modelling techniques used and how this is implemented in the developed automatic characterization system and the automatic modelling procedure with the organic devices. The methodology involves the DC and AC parameter extraction and is resumed in automatic generated reports.

5. **Device Simulation**: Ambient and variability parameters are extracted and based on the industrial model generated devices and circuits are simulated under different circumstances. The model is used together with robust design techniques for circuit optimization.
6. **Radio Frequency Identification (RFID) System Design**: using an improved technology in the organic electronic field, an RFID system for very cheap applications is simulated and designed under the guidelines of the work done.
7. **Conclusions**: summarizes the work done in this thesis, provides some insights how the field is evolving and indicates future work to be done.

1.4 Thesis Framework

The main part of this thesis has been carried out in the facilities of the Institut de Microelectrònica de Barcelona (IMB-CNM) from Consejo Superior de Investigaciones Científicas (CSIC) in the group of Integrated Circuits and Systems (ICAS) leaded by Dr. Lluís Terés.

The researcher has been working in the following industrial and research projects at Spanish and International level during his PhD period:

- **"SensiFlexTag: Plataforma avanzada para aplicaciones IoT con printed electronics para soluciones de trazabilidad, monitorización y localización de personas o productos en entorno de riesgo"**, Ministerio de Ciencia, Innovación y Universidades (RTC-2017-6679-7). 01/01/2019-31/12/2020.
- **"Manufacturable Extended Gate Array Sensors (MEGA Sensors)"**, Innovate UK (87711-543770), Technology transfer contract with Neudrive Ltd (UK). 01/05/2017-30/04/2018.
- **"SmartBallot"**, Ministerio de Industria, Energía y Turismo (TSI-100103-2015-041), Technology transfer contract with Scytl Secure Electronic Voting S.A. 01/07/2015-31/12/2017.
- **"SMART PRINTED PAPER: Printed Electronics para nuevas funcionalidades en papel"**, Ministerio de Economía y Competitividad (RTC-2014-2619-7), 01/02/2014-31/12/2016.
- **"Desarrollo de una etiqueta Near Field Communication (NFC/RFID) flexible con electrónica orgánica (Flex-NFC)"**, CDTI (IDI-20210365), 01/07/2020-30/06/2022.
- **"Disposable Paper Electronic Devices for Sustainable Eco-friendly Platforms (EcoTronic)"**, Ministerio de Ciencia, Innovación y

Universidades, RETOS de Investigación (RTI2018-102070-B-C21), 01/01/2019-31/12/2021.

- **"Consultancy Contract with Smartkem Ltd for the development of a roadmap for a Full-Custom Digital Design Strategy"**, Technical viability study, 01/05/2021-10/09/2021.

During the development of this doctorate, the student has taught two practical courses directly related to the topics of this thesis:

- *Training for Glade Layout*, in August 2020 for 10 hours.
- *Python aplicado para instrumentación de Laboratorio*, in May 2021 for 7 hours.

During the research, he participated as organizer in two different congresses:

- *1st Workshop Red-RISCV*, at Escola Enginyeria of UAB on the 5th and 6th of February 2020.
- *5th Scientific Meeting of PhD Students (JPhD2020)*, at UAB Campus on the 17th and 18th of September 2020.

And have attended and participated in three different conferences for the research spread:

- XXXIII DCIS Lyon, France, 14th-16th November 2018. With the work "*A short review of Organic Process Design Kits, from modelling to circuits and systems*" had been present in poster session.
- LOPEC 2019 Munich, Germany, 20th and 21st of March 2019. With the work "*Review of Organic Process Design Kits, from modelling to circuits and systems*" had been present in poster session.
- ESTC 2020 virtual conference, 15th to 18th September 2020. With the work "*An Organic Process Design Kit, from characterization to modelling and simulation*" had been present in an oral session.

An award had been received from part of the thesis results:

- *DC Characterization and Fast Small-Signal Parameter Extraction of Organic Thin Film Transistors With Different Geometries* for the best publication in impact journal of 2019-2020 by Microelectronics and Electronic Systems Department of the UAB.

Additionally, four different final degree thesis had been supervised and a website had been made showing part of the results obtained in this work related to a tool development where is offered as a service: http://pueg.imb-cnm.csic.es/opdk.html.

During the duration of this thesis, a stage of 3 months (May-July 2019) at the Institute of Nanotechnology of the Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, was done. During the stage he was working in the group

“Low Power Electronics with advanced Materials” leaded by Jasmin Aghassi-Hagmann under the direct supervision of Mr. Gabriel Cadilha Marques. Where he collaborated with the elaboration of two publications related to modelling, and circuit design in the printed electronic field.

2
State of the art

Organic and Printed Electronics is one of the most promising technologies for the fabrication of new, smart, flexible and low-cost electronic systems. It provides the opportunity of using flexible substrates and novel solution-based materials due to the diverse fabrication techniques they involve [1]–[4], allowing a reduction in the cost and waste generated in the process [5], [6]. OE opens a world of new, smart systems in different fields such as RFID tags, passive components, disposable sensors, flexible displays and functional circuity [7]–[10]. These systems have the advantages of being instantly made, fully additive, low-temperature processing, lightweight, bendable, large-area, easy scalable and environmentally friendly, all of this combined with low-cost processing. Furthermore, these new features enable wearable and disposable devices in the electronics field.

The forecast for OE market applications are important with some reports predicting a market grow of $45.6b, increasing from $31.7b in 2018 to $77.3b in 2029 [11] The OE field is very interesting for both industry and researchers as shown in **Figure 1** where the number of publications is increasing yearly. Most of the devices fabricated use inherited graphic arts processes, a continuous evolution of these techniques has led to improvement [12], [13], achieving lower resolutions and better performance in the fabricated devices. In this regard, printed electronics have had limited success in industry so far, mostly in displays, requiring further improvements in the stability and reliability of the printing process due to new functional ink materials [14]. Nowadays, while printing technologies cannot compete with the features of conventional silicon technologies, OE can offer new characteristics that cannot be produced with other technologies.

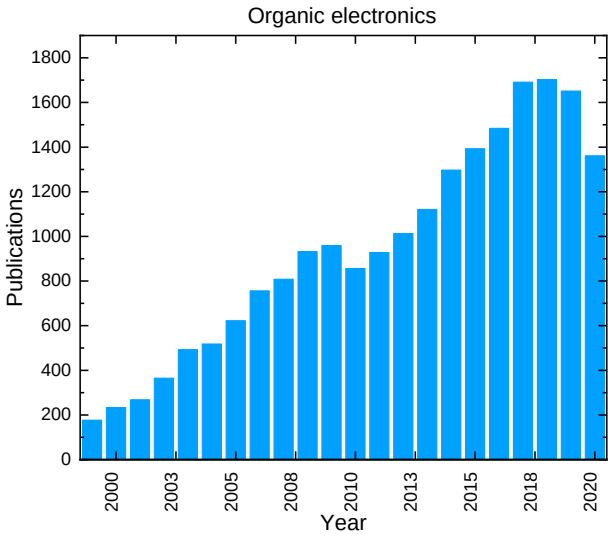

Figure 1. Publications by year in the organic electronics field (source: Web of Science at March 2021).

The use of EDA tools for circuit design had become a must nowadays, since the fabrication of a prototype can be expensive, ranging from 3.000 € to 12.000 €, depending on the foundry or technology used. Lately, this expensive first step is diluted between the high number of devices that are fabricated thus allowing the Integrated Circuit (IC) prices at which we are used. Moreover, EDA tools had reduced the time to market of the product while allowing the increase of design and process complexity.

For OE technologies, different models and PDKs have been presented over time [15]–[18]. These solutions cover some of the current requirements for system design. However, a lot of work still remains to be done on design standardization for the OE field. Moreover, printing technologies and organic materials imply new effects in the fabricated devices, and PDKs must include new approaches to overcome these new challenges.

One of the biggest challenges to deal with is the large disparity in the fabrication processes available for OE. The diverse nature of manufacturing technologies creates different constraints providing dispersed results, thus making the standardization methodology a key issue to implement generic models and circuits designs in order to have accurate, robust and reliable results to complete the design flow.

2.1 Printed and organic electronics fabrication

2.1.1 *Types of materials*

The electronic devices manufactured in the printed and organic field are based on three different functionals components that can be or not organic:

- **Conductor**, which offers free space for electrons
- **Semiconductor**, which allows space for electrons under some conditions.
- **Dielectric**, which does not offer free space for electrons

As can be seen in terms of electron mobility there is two opposite materials, conductor and dielectric, complemented with a component that varies their properties depending on the electric field under it is exposed. The three basic functional materials can be complemented with passivation and encapsulation techniques for avoiding external influences and degradation into the device.

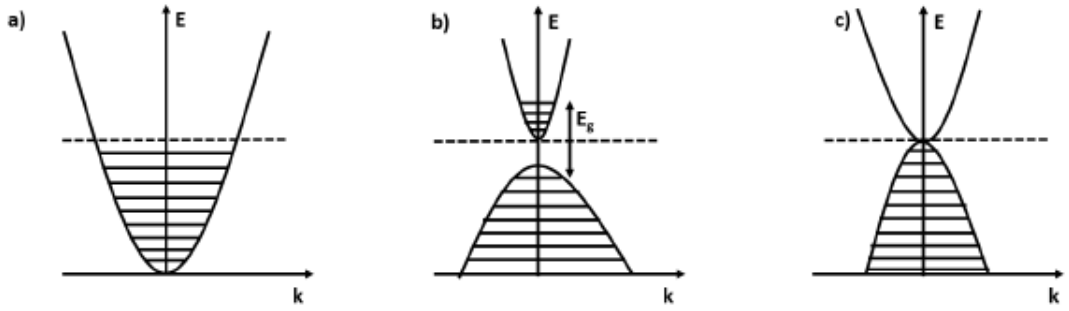

Figure 2. Band Structures (energy vs momentum) of **A)** metal, **B)** ITO and **C)** Graphene. The dotted line represents the Fermi energy. The valence and the conduction band overlap for metals and in ITO, the Fermi level lies beyond the bandgap, Eg, in the conduction band due to doping. In Graphene, there exists six double cones at which the conduction and valence bands touch [23].

Metals are the most common conducting materials, but not the only ones since different organic, oxides and carbon-based materials are also used as conducting materials. In silicon technology the electrodes are made with doped silicon with a layer of metal evaporated over the contact area [19]. The charge transport is based on the overlapping of valence and conduction bands complemented and an excess of electrons ready for free flow **Figure 2A**. Metals can be evaporated but also printed on the surface mean metal solutions inks, that solutions are prepared in two ways, using a precursor-based solution or a nanoparticle dispersion. The precursor-based solution uses chemical method to obtain the metallic film, being the most popular the silver ones [20], regards that oxides like Indium Tin Oxide (ITO) [21] are also popular since the degeneration of the conduction bands due the high level of doping that shift the fermi level upwards to the conduction band **Figure 2B**. Nanoparticle dispersion solutions are prepared by using nano powders of metal with a fixed weight combined with a solvent with a binder to keep the ink stable over time. Moreover, carbon-based materials as graphite or graphene are being popular as a conductor [22]. Graphene has carbon atoms arranged in a honeycomb lattice in which the carbon atoms have three neighbours each and forms alternating single and double bonds, like in benzene. Undoped graphene **Figure 2C** is a zero-bandgap semiconductor, which is characterised by six double cones with the Fermi level situated at these connection points, giving to the material a very high electron mobility.

Semiconductors are key element in the electronic world, since it allows the development of active components, they had been categorized in two groups, p-type and n-type, depending on the majority carrier, holes or electrons. Most of the organic electronics semiconductors are based on p-type materials [24], regards this situation n-type devices are starting to appear with the use of printable oxide materials [25]. As depicted in **Figure 3** the semiconductor have the same number of electrons in the conduction band (E_C) and holes in the valence band (E_V), with a fermi level (E_F) almost in the middle of the two bands following the expression $E_F = E_C - E_V$ as in **Figure 3A**, having a symmetric energy distribution based on the law of mass action in **Equation 1**.

$$np = n_i^2 \quad \textbf{(1)}$$

When the n-type semiconductor is doped with an electron donor, the energy level of the donor (E_D) usually lies within E_F, closer to E_C as in **Figure 3B**. The fermi level changes, and the majority charge carrier becomes electron, witch concentration is then calculated from E_F. The law of mass-action is still applicable and therefore, the minority charge carrier (hole) concentration is reduced. P-type doping of an intrinsic semiconductor is carried out in a similar way and the fermi level shifts towards the valence band.

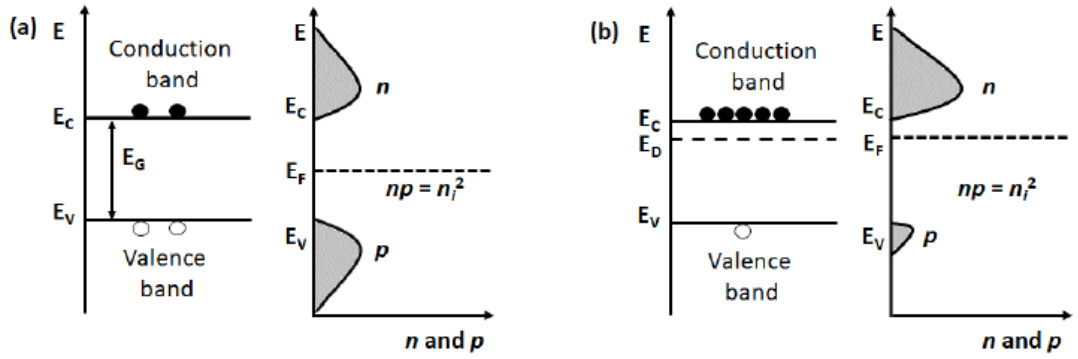

Figure 3. N-type doping of a semiconductor. **A)** Intrinsic semiconductor has equal number of electrons and holes. The fermi level lies in the middle of the bandgap. **B)** Addition of electron donor increases the electron concentration, and the fermi level shifts towards the conduction band [23].

Dielectrics or insulators are in charge to reduce the leakage currents while are polarized by an external potential. Oxide dielectrics are the more popular in the silicon technology and some works had been done using these materials since can be solution deposited with a very thin film [26]. In OE other materials are also used as polymers, organic, self-assembled mono and multilayers, inorganic, hybrid materials or electrolytes [27], [28].

Dielectrics have an intrinsic permittivity or dielectric constant ε_R respect the vacuum permittivity. It is defined as the factor by which the electric field between the charges is decreased relative to the vacuum. The calculation of capacitance can be found in **Equation 2**, where the capacitance (C) of a dielectric in between

two parallel plates is proportional to the product of ε_R and permittivity of vacuum (ε_0), the surface area (A) and to the inverse of the thickness, d.

$$C = \frac{\varepsilon_R \varepsilon_0 A}{d} \quad (2)$$

These three materials are deposited with different techniques over a substrate that in traditional electronics is the silicon bulk, but for OE the options are much wider, and more substrates can be used since lower temperatures are required for the manufacturing step, allowing the use of paper or plastic but also keeping the option to use crystalline bases.

2.1.2 *Fabrication techniques*

From the fabrication point of view, it is possible to organize the devices in two main groups; the fully additive ones, and the ones that contain some subtractive steps, usually based on clean-room conventional manufacturing technologies. **Figure 4** shows a comparison between the two main fabrication steps. On the one hand, fully additive processing includes printing technologies such as inkjet, offset, screen printing, gravure, and flexography, allowing scalable patterning, low-cost fabrication by using solution-based materials while facing a low process resolution, typically in the range of 40-50 µm, and a reduced performance. Recent publications had shown results below 1 µm [29], promising devices with better performance and reduced area in the near future. On the other hand, the use of subtractive processes, largely implemented in silicon-based technologies, can provide better performance and resolutions down to 5 µm, but are mainly based on the use of expensive equipment, and the handicap of not being easily scalable because of the impossibility of being integrated in a Roll-to-Roll process.

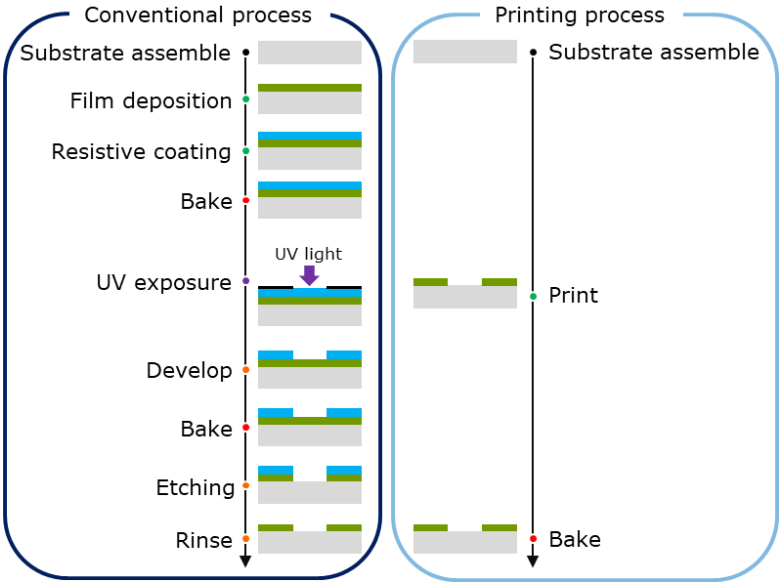

Figure 4. Conventional subtractive fabrication compared with the additive process.

For the fully additive ones, grouped in the printing techniques are basically divided in two major classes: contact printing, which deposits inks by direct contact between the printing plate and the bulk substrate, and non-contact printing, by which the ink is deposited on the substrate without any contact with the printing plate, **Figure 5**.

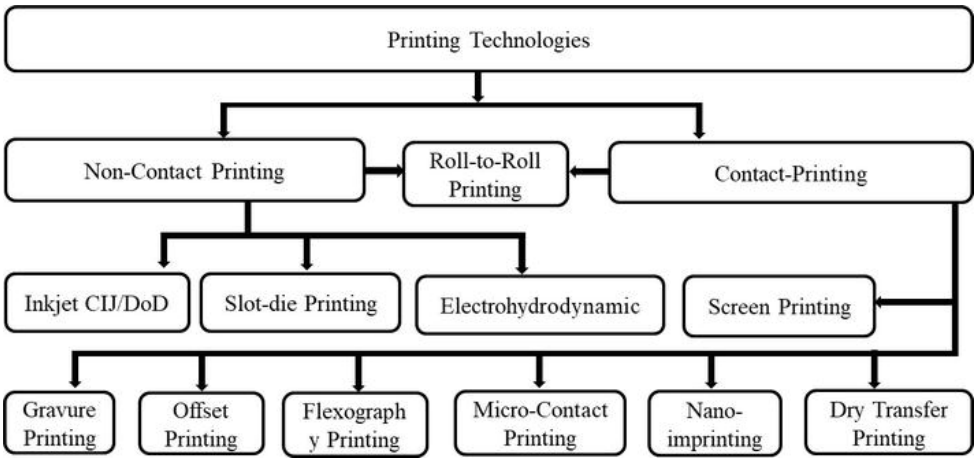

Figure 5. Scheme of the classification of Printing techniques [30].

The contact-based printing technologies involves gravure, offset printing, flexography, micro-contact printing, dry transfer printing and screen-printing. While the non-contact printing techniques include laser direct writing, slot-die coating and inkjet printing. The non-contact printing techniques had received greater attention due to their capabilities such as affordability, simplicity, adaptability to the fabrication process, reduced material waste and high resolution of patterns. Moreover, it allows printing onto very fragile substrates. The major handicap of non-contact printing techniques is the low scalability to industrialization process for product manufacturing, this is solved in contact-printing methods such as gravure and flexography that are commonly employed as roll-to-roll methods, providing large impression areas with a low cost.

Inkjet fabrication technique, **Figure 6**, is the most used technology of the non-contact group it uses a thermal or piezoelectric actuator to jet ink from a reservoir in order to deposit the droplet on the substrate. A pattern is then generated by either moving the substrate or inkjet nozzle to enable Drop-On-Demand (DOD) printing [31]. The flexibility of the inkjet-printing system allows a change on the fly of the pattern, additionally there is no need of any mask or auxiliary pattern for the geometry manufacture.

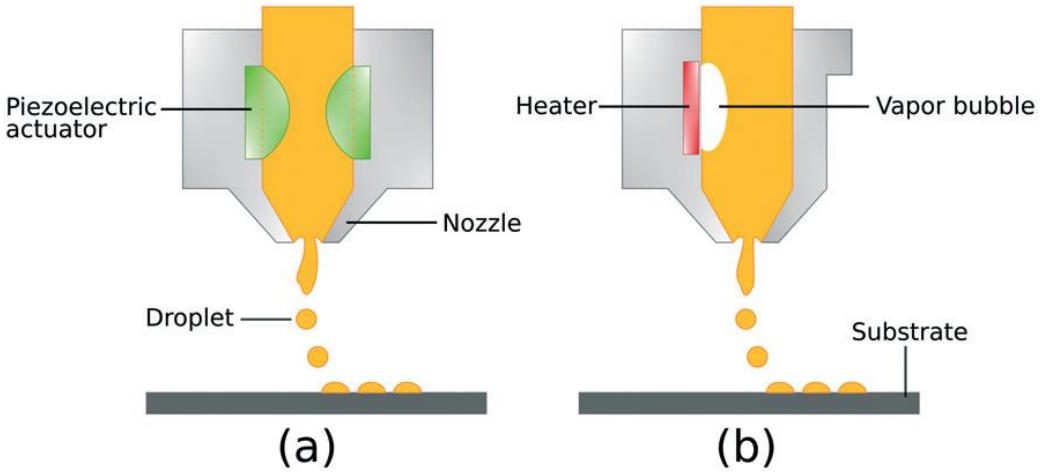

Figure 6. Schematic illustration of drop-on-demand inkjet printing process: **A)** piezoelectric DOD mode and **B)** thermal DOD mode [32].

In the contact fabrication group, the three most common and used are the ones coming from the graphic arts field, screen-printing, flexography and gravure.

Screen-printing, **Figure 7**, is the most popular and matured technology for printed electronics as it has been practiced in electronics industry for printing metallic interconnects on printed circuit boards. It is faster and more versatile than other printing tools, since it distinguishes by the simplicity, affordability, speed and adaptability of the fabrication process. It is composed of a screen mesh with the pattern to be stretched over a screen frame. In a pre-printing process, an emulsion, whose properties depend on the chemical and physical properties of the ink to be printed, is poured onto the backside of the mesh and then is pushed with the squeegee for print the pattern.

A) **B)**

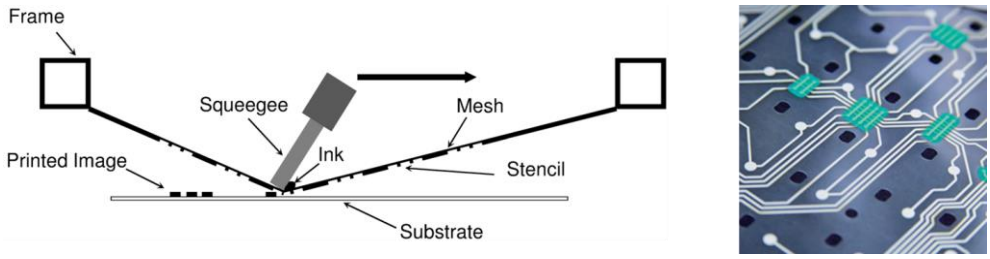

Figure 7. **A)** Scheme of the screen printing technology. **B)** Picture of a circuit fabricated using screen printing technology [33].

Flexography, **Figure 8A**, is used for high-speed runs of printed electronics employing a set of cylinders. The transfer of ink is done through direct contact of a soft printing plate cylinder, typically made of rubber or a photopolymer, which reproduces the positive image of the final pattern. The inking of the printing plate cylinder is provided via a ceramic anilox roller characterized by engraving small cavities separated by small walls, where the supplier deposits the ink. The anilox cylinder is continuously supplied with ink by contact with a fountain roller that is

partly immersed in an ink bath. The excess of ink on the anilox is removed by a doctor blade ensuring good control of the wet layer thickness, which is defined by the volume of the cavities in the anilox cylinder and the transfer rates from the printing plate cylinder to the substrate.

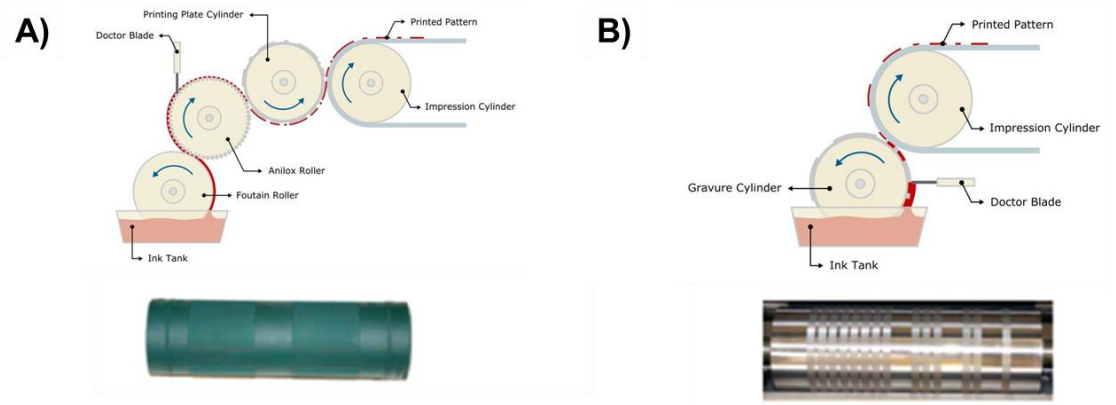

Figure 8. Schematic diagram of **A)** Flexography and **B)** Gravure [34].

Gravure printing, **Figure 8B**, is an intaglio printing technique in which ink is carried from an ink fountain to a printing surface using an engraved cylinder, which is electroplated with chrome to protect it from wear and tear during the ink transfer when is in contact with the substrate. The cylinder comprises periodic cells filled with ink, and the excess is scraped off the surface using a doctor blade.

A wide literature has been published which compares in detail the different printing techniques: for more specific information, a careful reading of these articles are recommended [35]–[37].

2.2 Overview of printed and organic electronics technology

Organic electronics technology had already conquered the display market with the Organic Light-Emitting Diode (OLED) technology. With this establishment new devices and applications have been developed into the fields of Organic Photovoltaics (OPVs), Lighting, RFID, Electronics and Components (as memories, diodes, batteries and others) and Integrated Smart Systems (like smart tags, sensors and smart textiles).

OPV had present significant breakthroughs in efficiency and in transparency modules and cost reduction. Since the technology is getting more mature, multiple companies are starting to produce them increasing production capacity, flexible OPV modules can be bought online for a low price, and more building integration installations have been done, by these reasons their market expansion is expected to be in the near-term.

Organic lighting, it is shifting from an expensive design option of luxurious complements into more mainstream architectural lighting since prices are starting to decrease. Non-planar and bendable lighting has appeared in consumer products, such as automotive taillights and display panels. Flexible and transparent lights are intended to be commercial products in the near-term.

The increasing demand of wireless communication is accelerating the development of RFID tags, **Figure 9**. The RFID systems are expected to replace the barcode system in order to improve automation of inventory and sales control. RFID tags at item level can potentially be integrated with a sensor and a display to provide product information such as expiration date. Most economic analysis suggests that the cost of each tag needs to be less than one cent USD to be used massively and become economically viable. Regards this goal is extremely challenging [38], Decathlon had started to implement it successfully with more expensive silicon-based tags [39]. The implementation to most of the consumer products is expected in the near-medium term.

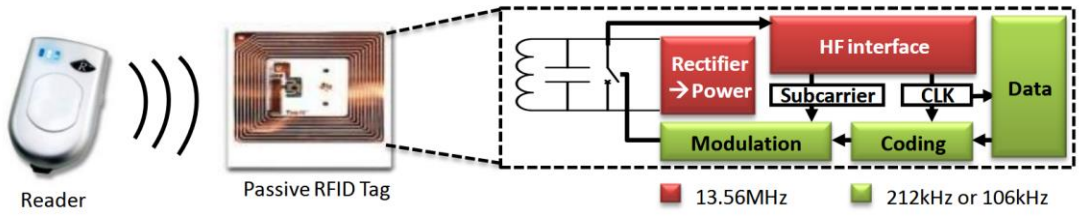

Figure 9. A basic RFID system comprises a reader and a passive tag [40].

2.2.1 *Device Types*

Electronic devices and components can be classified into two main families: passive or active elements. In the one hand, passive elements use the energy of the circuit for working. For instance, passive components are conducting pads, resistors, capacitors or inductors [41]. On the other hand, active devices are typically more complex structures than the passive elements and deliver power or energy to the circuit while are capable to introduce power gain or control the current flow. Transistors, thyristor, diodes, batteries or solar cells are examples of active elements [42].

Smart systems refer to products with functions of sensing, actuation, and control that integrate multiple technologies to create added value. Using the best properties of organic electronics field and silicon technology, hybrid systems can be done for ambient monitoring, energy harvesting/storage, wellbeing applications or even health wearable systems. In the sensing area, with the emergence of the need for Point-Of-Care (POC) devices, the use of Printed Electronics (PE), in particular, screen-printing and inkjet printing techniques have become widely used [43].

2.2.2 *Organic circuits*

In the last years, different circuits and systems have been reported in the organic electronics field, but not all of them has been simulated with EDA tools before their manufacturing. The choice of the simulation model is justified since each system have been processed with a specific fabrication technique, which generates different behaviours of the organic transistors. In this section, we will focus on those circuits which have been designed, simulated and fabricated closing the loop between manufacturing and design.

Analog circuits are strongly dependent on the intrinsic variability of the devices and the manufacturing processes because a change in a transistor can modify the behaviour of the complete system as stated above. This is the case regarding the current mirror circuit, since it clones the electric current flowing from one branch to the other branch proportionally to the transistor's dimension. A mismatch in an OTFT involved in the circuit will cause the reflected current to be different from that expected. Tylor et al. reported one current mirror [44] showing differences between the simulations and the experimental data of approximately 20%, as can be seen in **Figure 10**. This is a good result since the OTFTs used show a relatively high variability and the presented current mirror is made with four of them. They justified the mismatch between the experimental and the simulation results due to the different threshold voltage in the devices and the variations in the Organic Semiconductor (OSC) mobility introducing modifications in the current of the transistors.

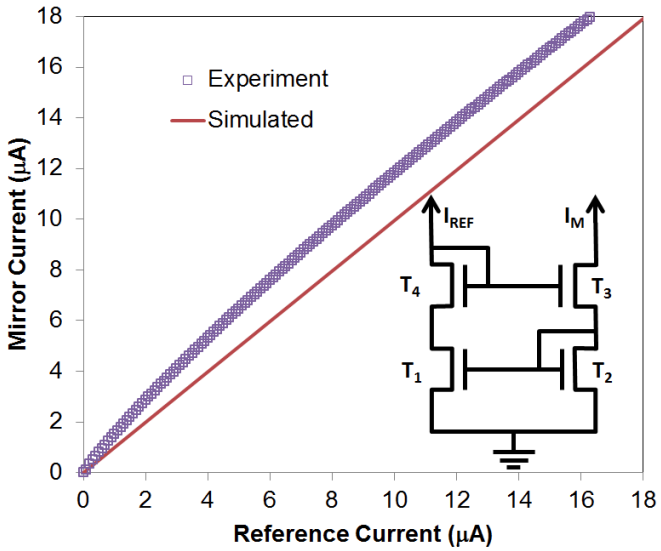

Figure 10. Comparison of experimental and simulated performance of the current mirror circuit shown in the inset. The transistors were nominally identical with W = 2500μm and L = 50μm [44].

Several digital systems with organic components can be found in the literature. The inverter circuit is one of the most basic circuits and it has been implemented in different fabrication methods. The inverter usually presents low

variability when using a single transistor combined with a resistance. In this way, the OTFT variability is lower since the number of transistor used is minimum [45]. When more devices are used, as in the case of a flip-flop, where inverters and NAND gates are used, the variability has a higher impact. Xia et al. reported a D Flip-Flop [46], where the simulations did not exactly fit the experimental results despite of the fact that the digital behaviour was well defined in both cases, as shown in **Figure 11**.

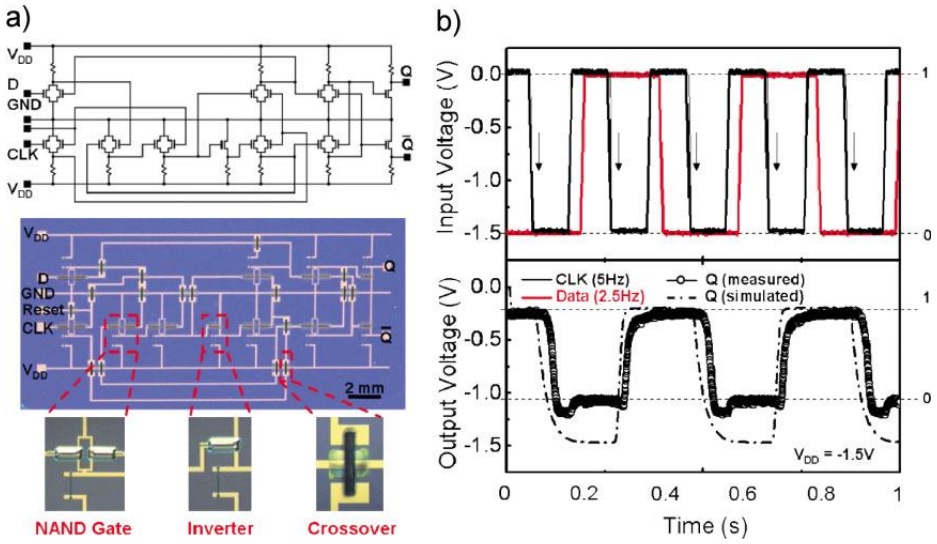

Figure 11. Printed D flip-flop circuit. **A)** Circuit diagram (top) and optical image of the circuit (bottom). The magnified images show the three most important features of the printed circuit. **B)** Dynamic response of the device. The red and black lines in the top panel represent the data and clock signals, respectively. The open circles in the bottom panel show the output response and the dashed line the simulated output [46].

Table 1 summarizes the different circuits and systems simulated and characterized in the literature. Information about the fabrication process is also included.

Table 1. Organic Circuits and Systems simulated and fabricated

Simulation model	Implemented Circuits	Fabrication method	References	Compensation	Max temp (Cº)	Year
DC behaviour	DC-DC converter and full wave rectifier	Subtractive	[47]	Threshold voltage	-	2013
Torricelli	Envelope detector and transconductance amplifier	Subtractive	[48]	Monte Carlo	100	2013
Zhang	Single stage amplifier and differential amplifier	Additive-screen printing & slot die coating	[49]	Monte Carlo	120	2015
Low pass filter	Low pass filter	Additive – inkjet	[50]	-	160	2016
UOTFT	Current mirror	Additive – roll to roll	[44]	-	100	2014
Torricelli	Inverter, NAND, ring oscillator, flip flop and comparator	Subtractive	[48]	Monte Carlo	100	2013
Estrada	Inverter	Subtractive	[51]	-	-	2011
Marques	Ring oscillator and latch	Additive – inkjet	[52], [53]	-	400	2017,2018
Marinov	Inverter	Subtractive	[54]	-	140	2018
MOSFET lvl 1	Inverter	Subtractive	[55]	Monte Carlo	-	2014
Arnal	Inverter, NAND	Subtractive	[45], [56]	Dual threshold	100	2019

Simulation model	Implemented Circuits	Fabrication method	References	Compensation	Max temp (Cº)	Year
Newman	Inverter, NOR, NAND, latch and flip flop, DRAM, ring oscillator	Subtractive	[57], [46]	-	-	2011,2010
UOTFT	Inverter, NAND, NOR and Latch	Additive – roll to roll	[44]	-	100	2014
Fadlallah	Inverter and, ring oscillator	Additive – inkjet	[58]	-	-	2007
UOTFT	Ring oscillator	Additive – roll to roll	[59]	Parameter variability	100	2014
DC behaviour	Negative voltage reference	Subtractive	[47]	Threshold voltage	-	2013
Valletta	ADC and DAC	Subtractive	[60]	-	100	2013
Newman	6-Bit ADC	Subtractive	[61]	-	-	2016
Ganesan	Smart Temperature Sensor	Subtractive	[62]	Parameter variability	-	2013
Fadlallah	RFID sequencer	Additive – inkjet	[58]	-	-	2007

Analog	Digital	Mixed Signal

Ring oscillators are simple circuits based on an odd number of concatenated inverters. The circuit generates an oscillating signal at the output. Two key parameters, supply voltage and oscillation frequency are used as a benchmark for the validation of the materials and the fabrication techniques used. The objective of the circuit is to provide higher oscillation with the lowest supply voltage possible. With this in mind different results had been obtained, as shown in **Figure 12**, from very low voltage circuits with reduced oscillation to high oscillation output with high voltage supply.

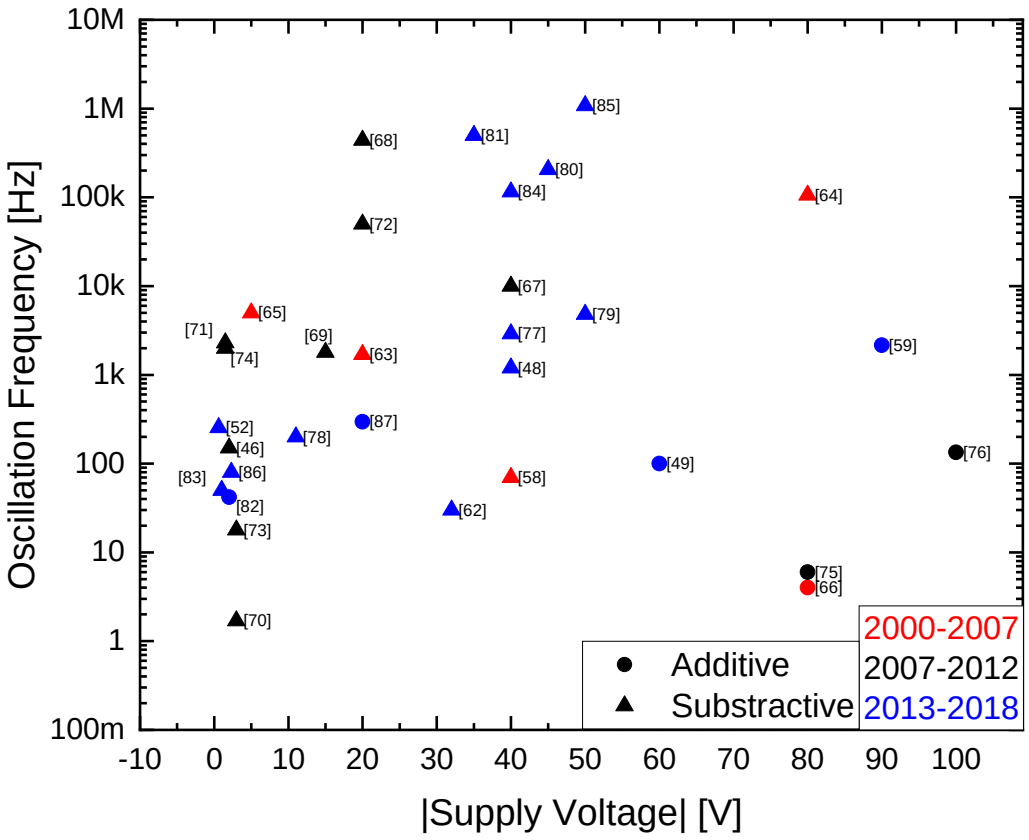

Figure 12. Ring oscillators with different processing based on OE.

In circuit implementation, special mention has to be made to Myny et al., for the achievement of a functional 8-bit Organic Microprocessor [10], as shown in **Figure 13**. Using only ModelSim [63] as a simulator. In this work, the OTFTs were not simulated considering their analog behaviour. The simulation was implemented using the Register-Transfer Level (RTL) behaviour of the transistors. RTL is a design abstraction level, which models a synchronous digital circuit in terms of flow of the digital signals, considering transistors as ideal switches.

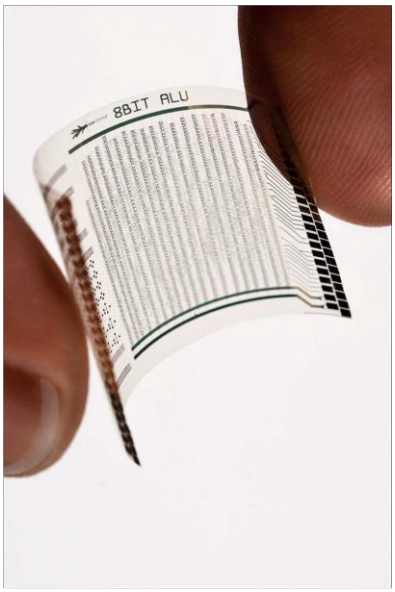

Figure 13. Photograph of the 8-bit Arithmetic Logic Unit (ALU)-foil [10].

2.3 Overview of automation systems

Nowadays, the use of automatic systems is present in the majority of processes around us. The advances in technology had allow more and more complex automatic systems, supporting the reduction of human intervention and displacing the worker to system supervision. The automation had as a goal the maximization of productivity, optimization, stability, reliability, safety and continuity in the production or research.

Automation is term that started to be used widely when Ford established an automation department in 1947, it is applied to any mechanism that moves by itself or is self-dictated. The word 'automation' is derived from ancient Greek words of Auto (means '*self*') Matos (means '*moving*'). In terms of precision, power, and speed of operation, automatic systems had demonstrated a higher performance than their manual counterparts had.

In automation control, multiple process variables must be collected and monitored to avoid any problem. All these variables are acquired, processed and controlled by the control system. This control system using the data processed and together with the different actuators involved in the automatic system allow a flexible, efficient and reliable production system. An automated system needs special dedicated hardware and software products for working where multiple protocols are described and implemented.

Any automatic system is composed by sensors, actuators and the control unit. The sensors convert the different physical process into electrical form and using the communication bus sends the data to the control unit that process and

activate the required actuator that translates this electrical form to physical variables for the proper production performance.

The automation on the testing setups can significantly reduce the effort required for perform a test, or significantly escalate the test duration allowing increasing the number of tests that can be done in limited time. Automated tests are repetitive, using exactly the same inputs in the same time sequence. A mature test automation setup should allow to perform a test at the “touch of a button”, supporting to run tests overnight when machines would be on stand-by. For a proper automation test system, a good test case must be used, this must follow four points. First of all, it must be exemplary, an exemplary test case should test more than one thing, thereby reducing the total number of test cases required, secondly it must be optimized to perform, analyze, and debug, thirdly is has to be cost-efficient and finally has to be evolvable for futures upgrades and new test. These four attributes must often be balanced one against another, a representation of this can be seen in **Figure 14**.

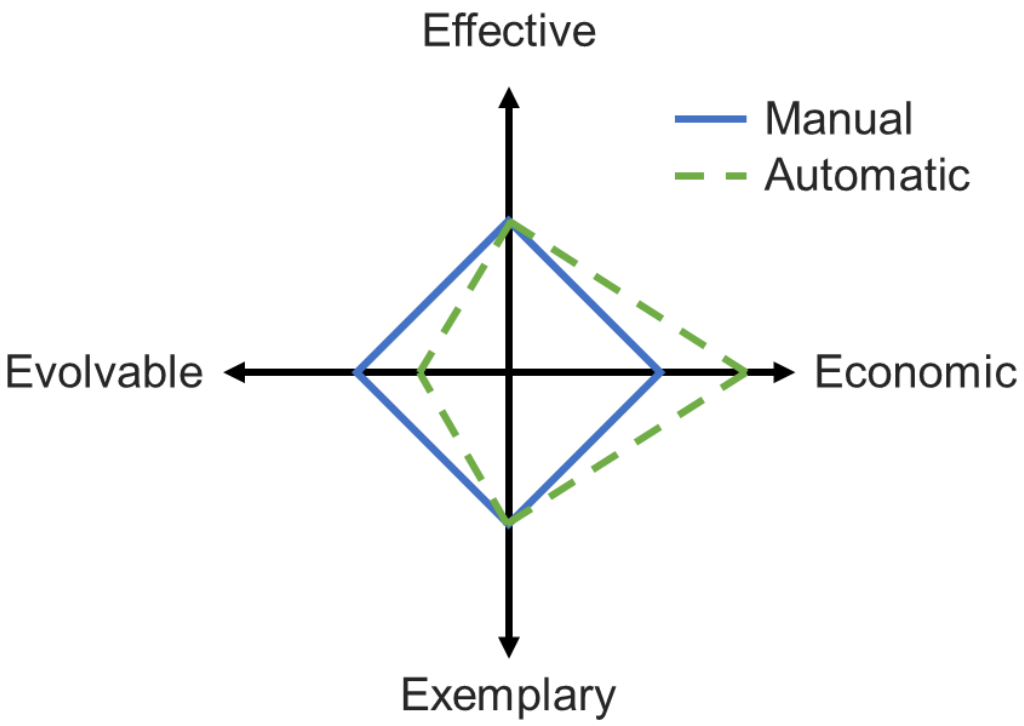

Figure 14. Test case performance for manual or automatic test.

In order to gain benefits from test automation, the tests need to be carefully selected and implemented. Automated quality is independent of the test quality since it is not important how well you automate a test if the base test achieves nothing, and then the result is an automatic test that achieves nothing faster. Once implemented, an automated test is generally much more economic and faster than the effort to perform it manually. However, automated tests generally

cost more to create and maintain. Automation test generation steps can be seen in **Figure 15**.

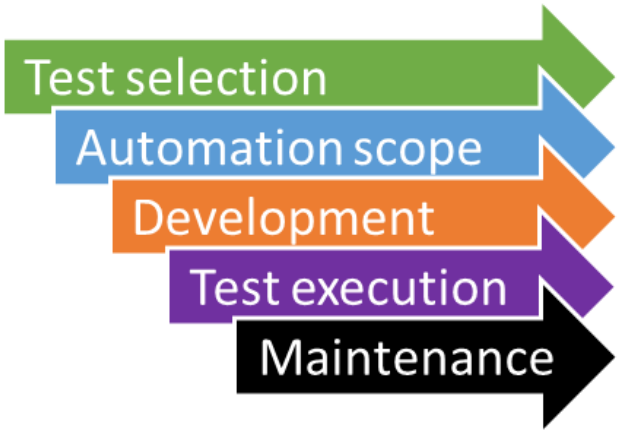

Figure 15. Test automation development process.

As pointed in [64], test automation can enable some testing tasks to be performed more efficiently than could ever be done by testing manually and there are also other benefits listed below.

1. Run existing tests on a new version of a program.
2. Run more tests more often.
3. Perform tests that would be difficult or impossible to do manually.
4. Better use of resources.
5. Consistency and repeatability of tests.
6. Reuse of tests.
7. Earlier time to market.
8. Increased confidence.

2.3.1 *Electrical automation solution*

EDA tools automation is a hot topic the companies in the analog designs, **Figure 16**, regards that the number of transistors is more reduced than in digital ones. The successful automation of digital designs have not arrive yet to their analog counterparts, since analog circuits are characterized by a much richer and more complex set of design constraints that need to be considered simultaneously and which may span several domains (e.g., electrical, electro-thermal, electro-mechanical, technological, geometrical domain), see **Figure 17**. The constrains are classified in four different groups:

- **Technological constraints** that enable the fabrication and are derived from fabrication restrictions, known as geometrical design rules. These constraints

can be very complex, but most of them belong to one of the following groups: minimum width, minimum distance, minimum overlap or minimum enclosure.

- **Functional constraints** that ensure the desired electrical behaviour of the design. They can be separated into circuit-specific requirements or process-specific requirement.
- **Design-methodical constraints** are deliberately introduced to reduce the complexity of the design process facilitating the use of computer-aided automation approaches.
- **Commercial constraints** that arise from chip area or packaging requirements.

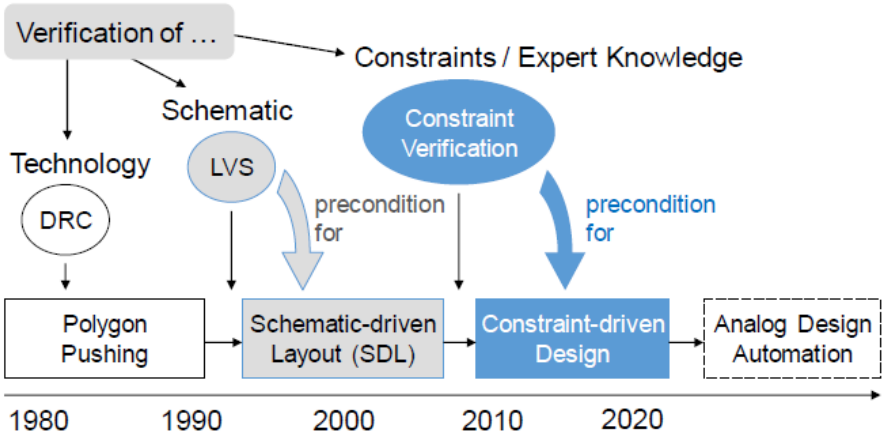

Figure 16. Evolution of analog physical design methodologies towards the goal of a fully automated analog design flow [65].

Only technological and functional constraints are mandatory in the different designs, while the Design-methodical ones depend on the design tool used and the commercial sector of the application or project funding.

The constraints can be implicit or explicit. An implicit constraint is not clearly expressed: it can be a plain textual note, or it could arise from assumptions intrinsically built into circuit descriptions or layout generators. Explicitly defined constraints are visible and accessible to design algorithms.

Applying the automation steps in the PDK development allows obtaining the exact same characterization for each test, very important to avoid any characterization variability, faster development and improvement of models, reduced layout errors, increasing the reliability of the final system with minimum supervision time and immediate feedback of the characterization results by means of automation display. Regards the benefits it has some counterparts as the time and cost required for the system automation development, use the same distribution of the pads in the layout step and a system to detect and avoid defects or anomalies.

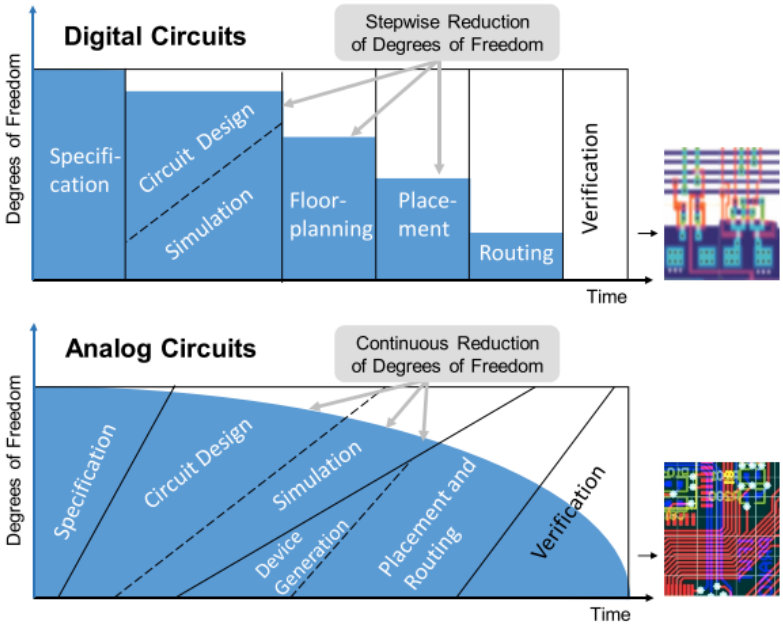

Figure 17. Simplified design flow for digital circuits and for the analog counterparts where steps typically overlap and are tightly linked [65].

2.4 Overview of organic PDK

A process/physical design kit is a set of data files and scripts used within EDA tools to define a complete design flow, going from the device modelling to the layout step through the schematic and the different optimization phases. PDKs includes different models and symbols for the different devices, active and passive, with a set of tools focused on the optimization of the simulation processes in order to be as close as possible to the experimental data. Different tools are involved in the design flow such as Electrical Rule Check (ERC), circuit simulation, Design Rules Check (DRC) and Layout Versus Schematic (LVS). Parasitic parameter Extraction (PEX) is usually incorporated for more precise simulations. Furthermore, to make the design stage quicker and reliable, Parametrized Cells (PCells) are also used. The basic flow of the simulation and design is presented in **Figure 18**.

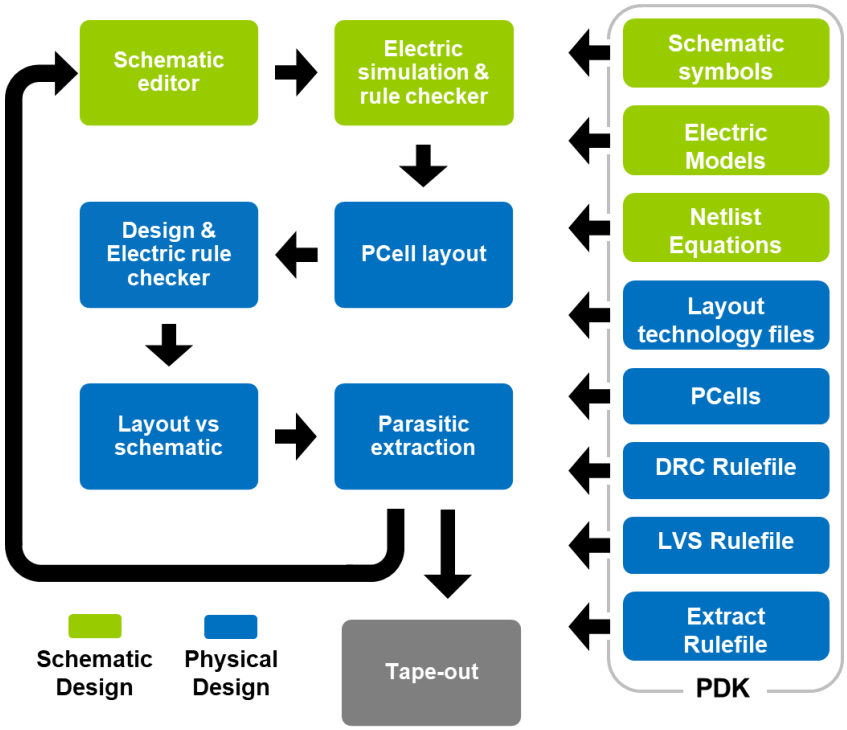

Figure 18. Generic methodology for full-custom circuit design supported EDA tools.

As a novelty to the conventional silicon PDK, OE-PDKs need to incorporate additional factors for the design, fabrication and simulation of the systems: flexibility and degradability. The introduction of flexible substrate provides different characteristics to the device depending on the bending radius, an important parameter to consider since it can introduce important variations in the performance of the system [66]. As an example, the impact of the bendability of OTFT parameters is shown in **Figure 19**. Advanced materials such as the ones presented in [67] reduce the bending effect in the device parameters. Likewise, degradability is a key parameter for commercialization since it offers an estimation of the longevity of the system and if it can be used as disposable system or if it should follow specific recycling steps. Some of the presented PDKs show the characteristics of flexibility incorporated as a parameter affecting the threshold voltage and the mobility for the device simulation [68].

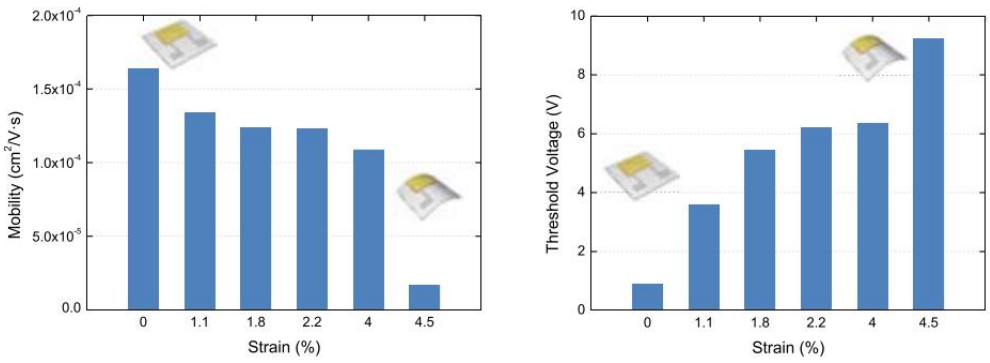

Figure 19. Mobility and threshold voltage bending dependence [66].

2.4.1 *PDK Components*

Simulation models are used to pattern the device behaviour in a mathematical language, allowing the simulation of the circuits and systems. Direct and Alternating currents (DC and AC) behaviour are usually included in the model for static and transient simulations of the devices and systems. Each device model is associated with a device symbol for fast identification and easier understanding of the schematic configuration for the designer.

The Electrical Rule Check (ERC) tool is used to verify the consistency of the electrical connections and the input-outputs of the system, both at schematic and layout levels, generating warnings when detecting missed functions in the circuit network. These rules are technology specific and not using the tool can result in reduced yield or non-detected defects, compromising the design robustness. Usually, ERC includes checking floating devices, nets or pins, shorted outputs, connections of high voltage to thin gates, etc. The electrical rules are specified as topological structures allowing proper verification of the design ensuring proper function, performance and yield.

Design Rules Check (DRC) is a set of rules used to verify if the physical layout implementation can be fabricated, with a specific technology, assuring a high yield and reliability. When design rules are infringed, the design may not be functional or the performance downgraded. The most common types of DRC rules are minimum width, spacing and area, wide metal jog, misaligned via wire or notch spacing. The rules may differ with the different manufacturing processes and they usually scale with the manufacturing technology complexity. Complex silicon PDKs can integrate up to 1000 design rules on their technology files for proper fabrication.

The Layout Versus Schematic (LVS) tool is used to compare the electrical behaviour described in the schematic with the extracted characteristics of the design in the layout step. It provides the mismatch between the expected results from the schematic and the layout design, allowing re-designing the system to correct the reported defects and mismatches. It works in three steps, starting with the layout extraction based on shape recognition, then the reduction step combines the different shapes into known devices and generates a netlist that is finally compared with the provided schematic netlist at the final step. This tool allows the detection of wire short- or open circuits, component mismatches, missing components, missing device terminal or extra device terminals.

Parasitic parameter Extraction (PEX) describes the circuit taking into consideration the behaviour of the connections between devices and the device stack, emulating the final physical response of the circuit. The main parasitic extractions are made in the capacitance, resistance and inductance between interconnections, crossovers and the different layers of the device. The extracted parameters are incorporated into a more accurate analog description of the

circuit, thus allowing precise simulations including timing, power and signal integrity analysis.

Parametrized Cells (PCells) are a key element for the circuit design, since they increase the productivity and the flexibility for the layout generation. They allow the implementation of devices using a basic cell that can have their geometric parameters modified in order to achieve the desired device layout, thus allowing its adaptation to technology changes at the electrical and geometrical level. Design time is reduced with the use of P-cells scripts since multiple device sizes can be implemented in an automatic way. Furthermore, the use of PCells reduces the number or errors in the design, thus making the verification step shorter. PCell workflow is depicted at **Figure 20**.

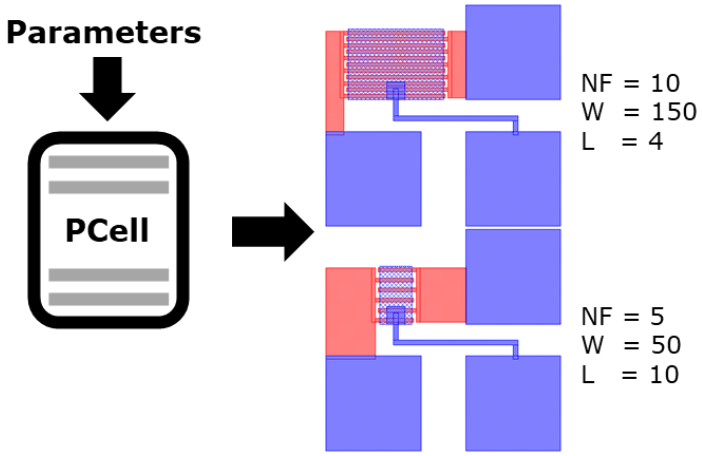

Figure 20. PCell workflow, parameters variation in Number of Fingers (NF), finger Width (W) and channel Length (L).

2.4.2 *Well-known software in the organic field*

While Synopsys [69], Cadence [70] Silvaco [71] and Mentor [72] dominate the EDA software tools used with silicon technology, in the OE field, a large diversity of software are used. Currently, two classifications between simulation and design software can be made:

For circuit simulation, the most popular free software tools are Ngspice, Xyce, Alliance CAD, Micro-Cap, QUCS, Spice Opus or LTspice. For the licensed software, the main players are HSpice (Synopsys), Virtuoso (Cadence), ModelSim (Mentor), Smart Spice (Silvaco), Tina, Circuitlogix, Advanced Design system (ADS) or Simulink. Most of them works properly with Verilog-A or Simulation Program with Integrated Circuits Emphasis (SPICE) models.

In relation to the design software, the most used free tools for layout design are Magic, Glade, KiCad or Klayout. Looking at the licenced software, the most popular graphic editors are Altium and CleWin. The classification is shown in **Figure 21**.

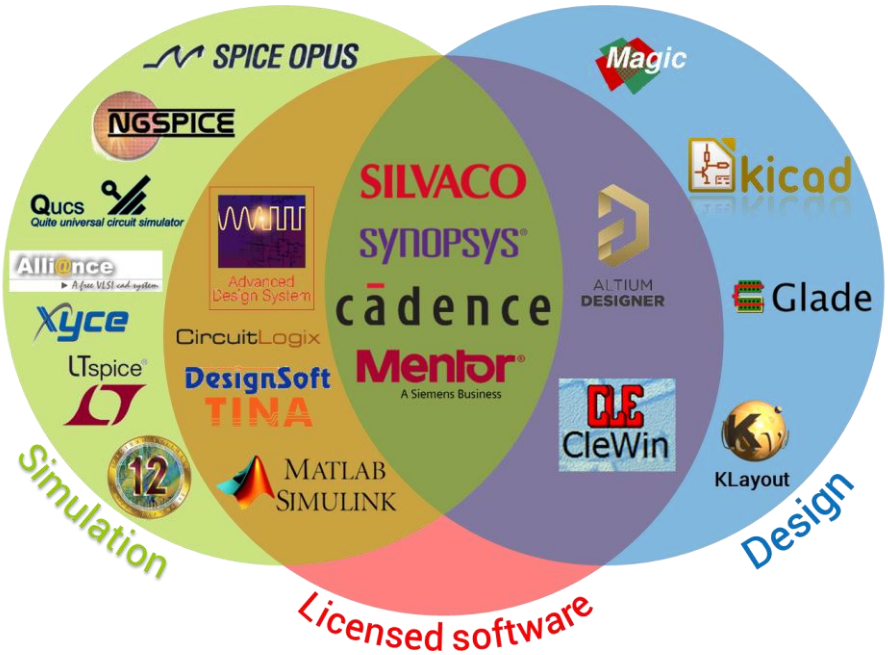

Figure 21. EDA tools used in the organic electronics field.

The existence of a very heterogeneous group of tools used in the OE field is noticeable due to the mix of graphic arts processes with electronic technology. In specific fabrication techniques, several designers run software tools that are also used in graphic art design. When designing simple devices, sensors and small circuits, programs out of the electronic scope such as Inkscape, Gimp, CorelDraw or Illustrator are used.

When using these types of design tools, the simulation step is not considered making it impossible to take into account a prediction of the final circuit performance and limiting the development of more complex systems.

2.4.3 *Organic PDKs*

Since there are diverse fabrication methodologies available and different transistor topologies and stacks can be implemented, specifics steps of the design flow must be adapted for each manufacturing process. The most critical steps regarding the different fabrication technology in a PDK are the DRC and the parasitic parameters extraction, since they are fully technologically dependent and need to be adapted in each case with a deep knowledge of the materials, fabrication techniques and devices.

In OE, some compact models have been developed and introduced in different commercial EDA tools. Silvaco [73] is currently offering the Universal Organic Thin Film Transistor (UOTFT) [74] model on its PDK and some circuits have already been published using the UOTFT model and the Smart Spice simulator. Additionally, for Cadence EDA tools, the Organic PDK (OPDK) [15] has been developed and implemented by the University of Minnesota with circuit design and simulation features [61]. At the Karlsruhe Institute of Technology

(KIT), Cadence have been used as base software for the development of their PDK [75]. Nanyang Technological University (NTU), have their own PDK where the effects of compression or extension of the devices are taken into account for the electric performance simulation by means of commercial EDA tools [68]. In addition to these commercial-based tools, a complete open software PDK has been described in the TDK4PE project [76], including the schematic editor, netlist generator, model simulator, layout designer and a backend tool to convert the layout output in a set of bitmap files ready to be printed by an inkjet printer. A list of the available organic PDKs is presented in **Table 2**.

Table 2. PDKs developed for organic and printed electronics

PDK	Model	Schematic editor	PCell	DRC	Parasitic extraction	References	Website	Year
KIT	Marques	Virtuoso	✓	✓	✓	[75]	-	2018
TDK4PE	Fitting & Estrada	Ngspice	✓	✓	✓	[76]	[76]	2015
Silvaco	UOTFT	Smart Spice	✓	✓	✓	[77]	[78]	2009
IMB-CNM	Arnal	Virtuoso	✓	✓	✓	[56]	[79]	2020
NTU	Zhang	Virtuoso/ Hspice	✓	✓	-	[68]	[80]	2016
TU/e	Torricelli	Virtuoso	✓	✓	✓	[81]	-	2019
FHE	Marinov	-	-	✓	✓	[82]	-	2018

2.4.4 *OTFT models*

Compact models provide a bridge between fabrication technology, circuit simulation and system design [83]. They should be simple enough to be incorporated into EDA software and sufficiently accurate to make the simulator results useful for the circuit designers [84]. Compact modelling is based on parametric equations that use different variables inspired in the behaviour of the device and some physical characteristics of the materials used or the device geometry implemented.

Marinov et al. [85] exposed the following features that might accomplish any compact OTFT model:

- It must represent consistently the behaviour of the OTFT.
- It must reflect the symmetry of the OTFT structure.
- It needs to be analytical, without differentials or integrals.
- It must be simple and easily derivable.
- It should have parameters easily obtained.
- It has to be up/down-gradable, in order to have different levels of computation complexity.
- It should have relations that can be physically justified.
- It should be close to other FETs compact models.
- It should be adaptable to the experimental data that can be inaccurate.

Additionally, as a good compact model it should have a low computation time and provide acceptable accuracy. The model desired is the one that finds a good compromise between accuracy, complexity and computational requirements. It must also be robust and reliable to allow a predictable behaviour of the device.

2.4.4.1 *Modelling languages*

Circuit simulations have been crucial for the silicon electronics industry, since they allow predicting the behaviour of complex systems before their fabrication. The circuit simulations are a continuation of the electrical simulation tools that started in 60s with the Computer Analysis of Nonlinear Circuits, Excluding Radiation (CANCER) project [86]. Later, EDA tools were improved adding additional tools such as DRC, LVS, parasitic extraction algorithm and circuit optimization, incorporating new simulations methods and generating more accurate simulations. Nowadays, for silicon-based electronics, professional EDA programs are mandatory for any Integrated Circuits (IC) design, where very complex systems are achieved. For the incorporation of analog simulation

models in EDA software, two main description languages are used: SPICE and Verilog-A.

SPICE [87] is a general purpose analog circuit simulator, developed by Laurence Nagel in the University of Berkeley [88] deriving in big measure from the former CANCER project. The aim of this general-purpose and open-source descriptive language is to simulate, in the first instance, analog electronic circuits, using build-in models that are the base of this language. The latest version of SPICE uses C language code for the description of the compact models, but previously it was developed using Fortran. SPICE is one of the most popular description languages for modelling since its first release in 1973, and nowadays, a large diversity of simulators and models are available.

Verilog-A [89] is a subset of Verilog-Analog and Mixed Signal (Verilog-AMS) that was developed at Gateway Design Automation (USA) in 1985, by Phil Moorby, as a proprietary language for hardware modelling [90]. Later, in 1995, it was transferred to public domain and submitted to IEEE as standard 1364-1995. It was initially intended for use in analog and continuous time simulations. Verilog-A is one of the most popular languages for compact model description, this is due to the simplicity of implementation of the derivative and integration operations in the mathematical behaviours of the devices, allowing the designer a quicker and optimized way to describe compact models. Verilog is based on a hierarchy of modules that communicate between them with a set of input, output and bidirectional ports. Using this structure, the scalability of the models is simple to modify, allowing the creation of complex devices where different parts can be added or removed depending on the requirements. In addition, this modular configuration allows the description from a physical level, based on charges behaviour, up to high levels of abstraction, as far as pure mathematical models are supported. Verilog-AMS offers the combination of analog and digital systems in the same code based on the use of different modules for the system description. Due to this versatility, most of the new models generated are coded with Verilog-A.

Circuit simulation tools are based on electrically common points, also known as nodes. These points are used to represent the terminals of the devices and the interconnection between them, allowing the configuration of the circuit as the designer wants and obtaining a netlist of the connections between the devices. The netlist is translated into a group of nonlinear differential algebraic equations that are solved using integration methods such as Newton-Raphson and sparse matrix. These mathematical operations allow running simulations of the circuits using the implemented models.

Each EDA tool implements a simulator with SPICE or Verilog-A language, or both, depending on its use or market scenario. These languages have different benefits and weaknesses, and the designer can choose the most appropriated one for the circuit simulation in accordance with their knowledge of the modelling

languages. The model language selection can introduce small differences which influence the simulation time required for each device [91]. However, this is not something that necessarily has an effect on the final simulation results.

2.4.4.2 *Charge transport on organic devices*

Since there are various organic transistor types, topologies and stacks, different models have been proposed to cover them. In this way, extended reviews have been carried out [92], [93], with an in-depth study of the physical approach of each model.

Studies comparing models and different OTFT topologies have been performed in the literature. Necliudov et al. [94] tested how swapping top and bottom contact of the source and drain has a direct effect on device behaviour and performance. BGBT OTFT stack exhibits nonlinearities in the output characteristics at low voltage between the drain and the source contacts, while the same effect was not observed in BGTC topology. Kramer et al. [95] studied two step model generation for different types of devices and topologies, looking for the optimization of the channel length dependence of their devices.

For the modelling of organic semiconductor performance, different theories of charge transport have been formulated. One of the most popular is the Variable Range Hopping (VRH) theory [96], as shown in **Figure 22A**. This is based on the disordered structures of the OSC allowing the electrons the chance to move to the lowest activation energy with the shortest hopping distance, creating a variable conductivity that relies on the temperature and the molecular structure of the semiconductor [97]. In contrast, Multiple Trapping and Release (MTR) theory, **Figure 22B**, [98] proposes that the predominant carriers are trapped in localized states in the channel of the transistor that is associated with defects of the OSC and the dielectric. These trapped charges cannot move in a direct way from one state to another. In this case, the carriers are promoted to an extended-state band in which the charge transport occurs. The density of free carriers for transport relies on the difference in energy between the trap level and the extended-state band and these bands are linked to the gate voltage and the temperature [99]. The Polaron model, **Figure 22C**, [100], is based on the combined mobility of the electron tunnelling and hopping motion. For the low temperatures range, the tunnelling effect is predominant, while the hopping motion is the dominant effect for high temperatures. Each contribution depends on the actual values of the carriers [101]. Finally, the Disorder model, **Figure 22D**, has been proposed with the focus on the amorphous properties of some OSC solutions that provides a shapeless molecular morphology. This creates disorder in the electrical structure of the device, where the charges are distributed on the different states of the band. The conduction of carriers occurs with the charges jumping between neighbouring molecules [100].

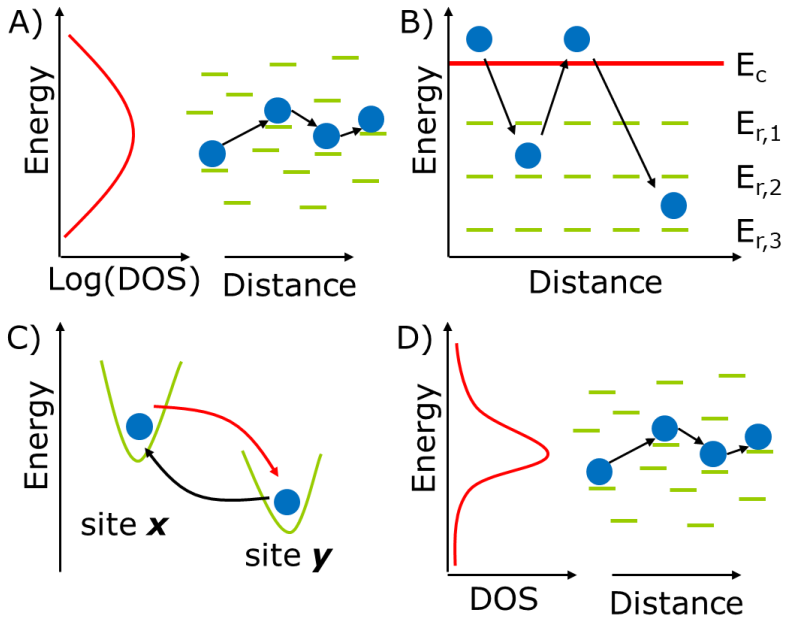

Figure 22. **A)** Variable Range Hopping, **B)** Multiple Trapping and Release, **C)** Polaron model and **D)** Disorder model. Density Of States as (DOS).

Table 3 summarizes the currently available models based on new developments or improvements in silicon or amorphous-silicon models adapted to OTFT device characteristics. The base transport model for the different transports models is listed in combination with the parameter extraction methodology and a specific modelling language for simulation purposes. The models have been generated/adapted with the focus on a unique device of type, while few of them have been reused in other OTFT stacks with different fabrication processes, most of the presented models had been reviewed in deep on [92].

Table 3. Compact models for organic devices.

Model	Transport method	DC	AC	Parameters extraction	Language	Year
Fadlallah	VRH [96]	[102]	[102]	[102]	SPICE	2006
Valletta	Gradual Channel Approximation [103]	[104]	[105]	[104]	SPICE	2014
Marinov	TFT compact level 1	[85]	[106]	[107], [108]	SPICE	2009
UOTFT	VRH [96]	[74]	[109]	[110]	SPICE	2009
Newman	Shichman-Hodges [111]	[112]	[112]	[112]	SPICE	2004
Marques	Curtice [113]	[114]	[75]	[114]	Verilog-A	2017
Arnal	Shichman-Hodges [111]	[56]	[115]	[115]	Verilog-A	2020
Zhang	AIM-SPICE Level 15 [116]	[49]	[49]	[49]	Verilog-A	2015
Yaghmazadeh	AIM-SPICE Level 15 [116]	[116]	-	[116]	Verilog-A	2009
Estrada	UMEM [117]	[118]	[119]	[120], [121]	Verilog-A	2003
Ganesan	VRH [96]	[122]	[123]	[123]	Verilog-A	2013
Torricelli	Single-Transistor Method [124]	[125]	[126]	[124]	Verilog-A	2015
Tejada	UMEM [117]	[127]	-	[127], [128]	-	2009

2.4.5 *Model Classification*

A conceptual classification for the compact models used is the box model concept, where the categorization is distributed depending on the relation between the model and the physical characteristics of the devices. On the one hand, Black-Box (BB), also called behavioural model, describes the device in terms of its inputs and outputs, without any correlation with the physical characteristics, becoming a pure mathematical model. On the other hand, White-Box (WB) is the opposite case, since it requires a lot of knowledge or assumptions, about how the physics of the system works for the model development. Between these two classifications, are located the Grey-Box (GB) ones, that can use some of the physical characteristics and additionally use pure mathematical solutions inside the model. Most of the models presented in **Table 3** can be included in this category.

Black-Box models can follow two different approaches. Table models are pure empirical models where the characterized output and transfer curves are stored in a table that is accessed by the EDA tool based on the voltage applied to the device. Since the values are stored in the table, high precision is achieved in this specific device. Curve-fitting is the other methodology used, where the data for the mathematical representation of the device is obtained from an equation that can be evaluated in the simulation tool. Both methodologies, allow the generation of quick and easy implementation of experimental and non-established devices in EDA tools with a very simple procedure. The big issue of this type of models is that they are not able to predict the system performance when it is scaled or outside of the model characterization region. Grey-box models are the bridge between the compact physical models and the black box ones, implementing restrictions to the pure mathematical methodology while using some well-known physical parameters. Despite the simplicity of these mathematical models and sometimes the better accuracy they provide, few studies have been done in the OE field [129]–[131]. An illustration of the three different categories is shown in **Figure 23**.

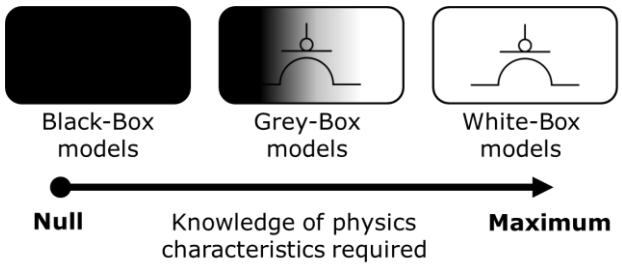

Figure 23. Box model representation.

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3
Layout Design

IC design relies on the schematic as a starting point, where the information about the connectivity of the devices in the circuit is represented together with the design intent. The circuit is validated by using the DRC, ERC and LVS checking tools in multiple iterations with corrections in order to get the final version that achieves the expected behaviour with the correct design rules and the proper connections.

EDA tools such as Cadence, Mentor, Synopsys, KLayout or Glade, allows the design of systems and devices with a defined stack of materials and provides tools to assure that the design can be fabricated with the DRC defined. Some of these programs, additionally to circuit design, allow the system simulation. As introduced before, in OE most of the circuits designed are digital [1]–[5]. The low presence of analog circuits is due the low performance and parameter variability of the OTFT and the few models available. These handicaps make that the digital circuits examples are more numerous than their analog counterparts. Despite of the fact that OTFTs circuits are not so complex as in silicon technology, demonstrators such as a 8-bit microprocessor based in OE had been reported [6] showing the potential of the technology that intrinsically is more cheap and environmental friendly, could be an option in the near future.

Layout automation have shown major progress in the silicon technology for the last 30 years allowing the development of complex integrated circuits in a quick and reliable way. The use of PCells combined with the Place and Route (P&R) scripts suppressed the need for complex DRC checks, keeping the layout under the fabrication requirements. Some of the benefits of using this EDA tools are the rapid placement of devices and other structures, visual interaction of constraints in both the schematic and layout domains, automatic recognition of constraints, and ease of use or editing capability at high abstraction level. The

actual methodology pursues the correct-by-construction layout as a goal, giving LVS and ERC correct designs without expensive rework.

Regards that Cadence and Synopsys leads the layout field, interesting free alternatives had appeared the last years. In this thesis two layout EDA tools were used, KLayout and Glade, both of them freeware. The use of these tools answers to the need of simple and cheap way to design the layouts in the OE field. Both tools can be seen in **Figure 24**.

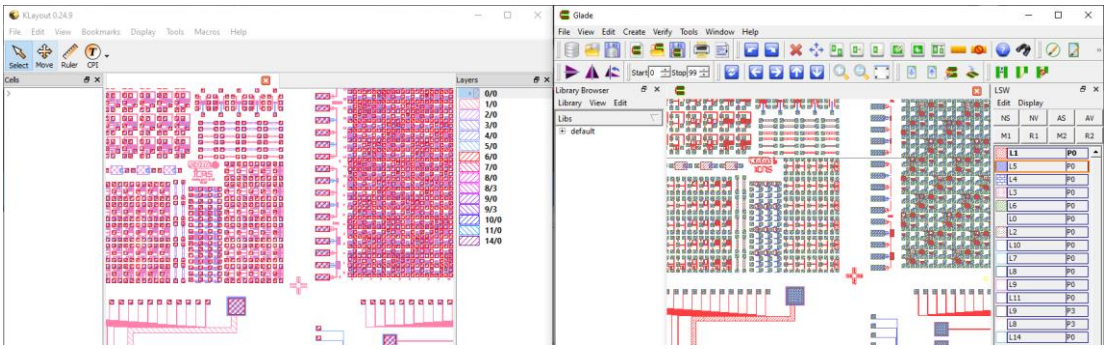

Figure 24. KLayout (left) and Glade (right) layout tools.

Glade (Gds, Lef And Def Editor), is freeware program developed by Keith Sabine, that can be used in Windows, Linux and Mac operating systems. The developer defines the tool as:

> *Glade is an IC layout and schematic editor capable of reading and writing common EDA formats. With built in DRC, extraction and LVS you can generate and verify schematics and layout in a single customizable tool* [7].

The tool can be managed using Python scripts that allows the implementation of Pcells, providing simplicity in the design of circuits and systems. Moreover, Glade can be controlled through a visual interface or using the command line section.

KLayout started as a GDS file viewer developed by Matthias Köfferlein that have evolved to a layout editor with drawing functions. It supports external libraries and PCells, combined with DRC and LVS that includes XOR tool, a layout differential, search & replace, a technology package manager and add-on package manager ("Salt"). It runs under Windows, different Linux distributions and Mac operating systems.

KLayout provides an intuitive interface or can be used with Ruby-based scripting environment. Moreover, it is extensible and configurable in a large degree, with an integrated development environment for Ruby and Python scripts, allowing PCell description in both languages.

This chapter of the thesis presents the work done for two manufacturers in the OE field, NeuDrive and SmartKem, both of them with the objective to develop

a PDK with maximum automation possible due their constant evolution in the materials and fabrication techniques.

3.1 Automatic layout generation of single gate devices

The first run designed was done for NeuDrive Ltd., with the objective of a PDK development and the aim to develop most of the work under automatic methodologies that can be implemented to other technologies without huge effort. The layout design was planned, sent to manufacture and characterized.

The fabrication was carried out at the Centre for Process Innovation (CPI, Sedgefield, UK) using the Gen2 photolithography facilities. The OTFTs employ Top Gate Bottom Contact (TGBC) architecture in which the fabrication process begins with the spin-coating of the planarizing layer of a proprietary acrylate polymer (PCAF, from CPI) on carrier glass followed by a soft-bake. Then a cross-linking process using UV light in a nitrogen environment, followed by hard-baking. Au (50 nm) were sputter coated and patterned using photolithography and wet etching to form drain and source electrodes. In order to increase the surface energy, the substrates were oxygen plasma-treated and then a Self-Assembled Monolayer (SAM) of 3-fluoro-4-methoxythiophenol (Fluorochem, Glossop, United Kingdom) was deposited from a 10 mM solution in isopropanol and baked at 100 °C for 60 s. Afterwards, the OSC FlexOS^{TM} solution was spin-coated at 500 rpm for 10 s followed by 1000 rpm for 60 s and then a further bake at 100 °C for 60 s in order to obtain a 20 nm thick film. The OSC solution comprises a small molecule semiconductor and a high-k polymer semiconductor binder. The dielectric used in this work was Cytop CTL-809M (Asahi Glass, Tokyo, Japan) and it was diluted to 4.5% solids and spin-coated in order to obtain a 300 nm thick film and a gate capacitance of $6 \cdot 10^{-9}$ F/cm^2. Au (50 nm) was thermally evaporated, patterned using photolithography and wet etching. The gate-source/electrode overlapping area is $2.6 \cdot 10^{-4}$ cm^2 and $1.4 \cdot 10^{-5}$ cm^2 for Corbino and interdigitated devices, respectively. The unwanted areas of OSC and dielectric were patterned by oxygen reactive-ion etching plasma etching using the gate metal as a hard-mask. Subsequently, Polyvinyl alcohol (Sigma-Aldrich, Saint Quentin Fallavier, France) and SU-8 (MicroChem, Westborough, United States of America) were deposited and patterned as a passivation layers. The metal interconnect layer (Au 50 nm) was sputtered and patterned to create electrical connections. Finally, the third protective passivation layer (SU-8, 450 nm thick) was deposited in a similar way to the first two passivation layers. All the layer thicknesses were measured through SEM images. A device representation and stack of materials can be seen in **Figure 25**.

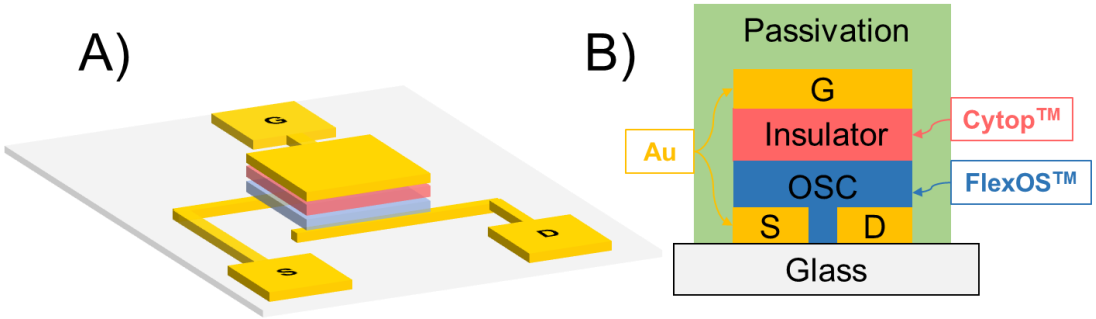

Figure 25. A) OTFT architecture and **B)** stack of materials.

The layout is based on two main areas, the transistor array and the analog design. All the devices included in the layout had been generated by using PCells allowing a correct-by-construction design with a huge time saving in the verification step. Additionally, using these PCells, place and route scripts were developed for the device array generation with the proper configuration for the automatic characterization step. The distribution around the wafer of the 9 pieces of the transistor array and the 2 parts of the analog design can be seen in **Figure 26**.

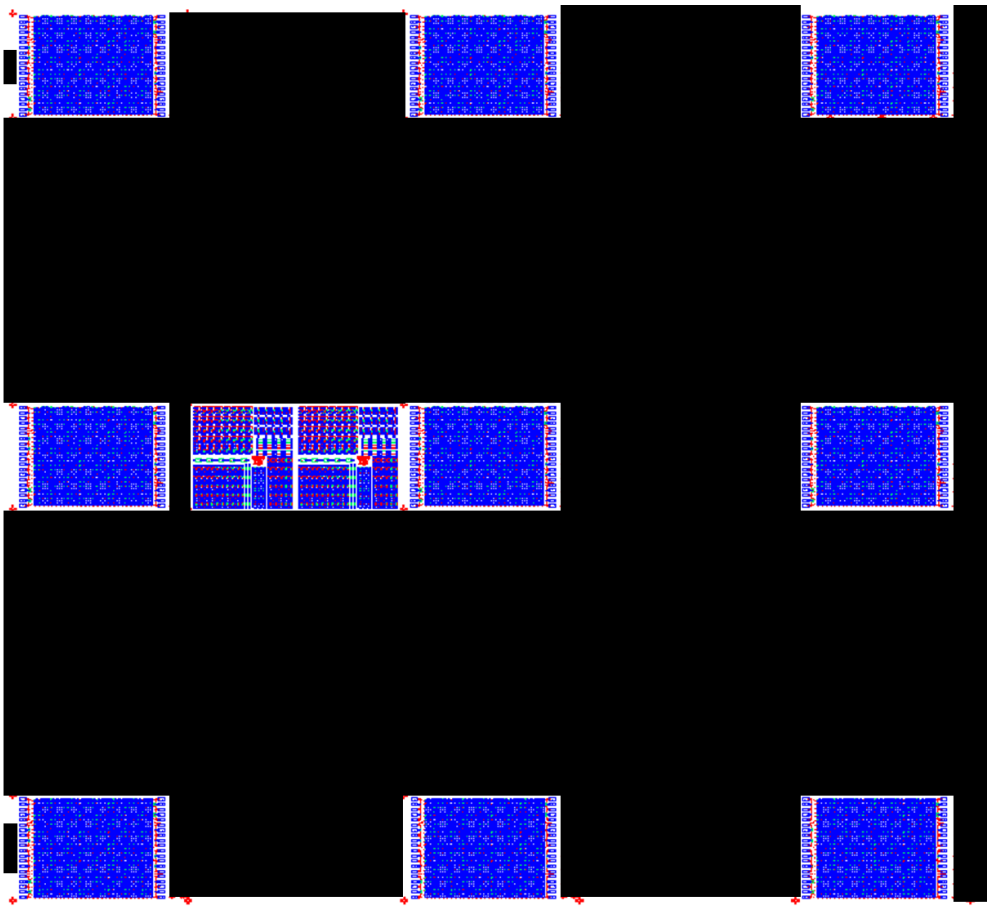

Figure 26. Run layout with the 9 transistor array and two analog parts. Black areas are other systems from external designers.

The parts of interest of the wafer were isolated by using saw cuts for a proper circuit characterization. A picture of the parts once prototyped can be seen in **Figure 27**.

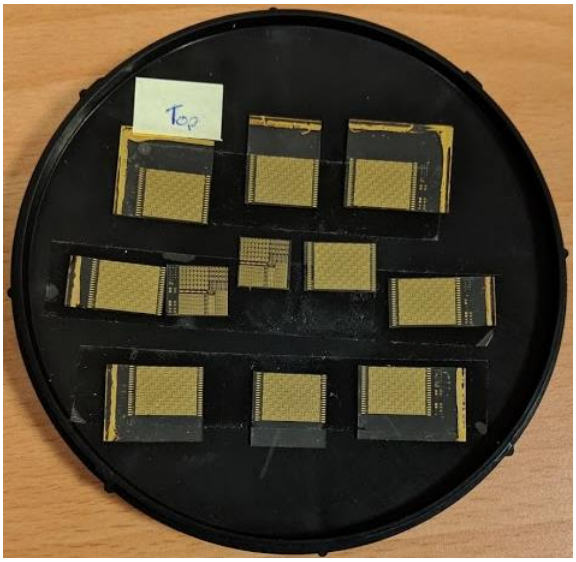

Figure 27. Photo of the different parts of the prototyped layout.

In the layout an array of 29 columns by 24 rows has been designed, **Figure 28**, providing a total of 696 transistors for each set. The array has in their two sides 40 pads, distributed in two groups of 20, the pads are used to contact 16 transistors in pairs of the same sizes, allocating 4 pairs in each side. The pads had been distributed having in consideration the contacts of TSOP-I standard for a 40-pin chip, with the objective to use a TSOP-I socket for an easy external connection for circuit configuration, see **Figure 29**. The total size of each array is 14.000 µm by 9.740 µm.

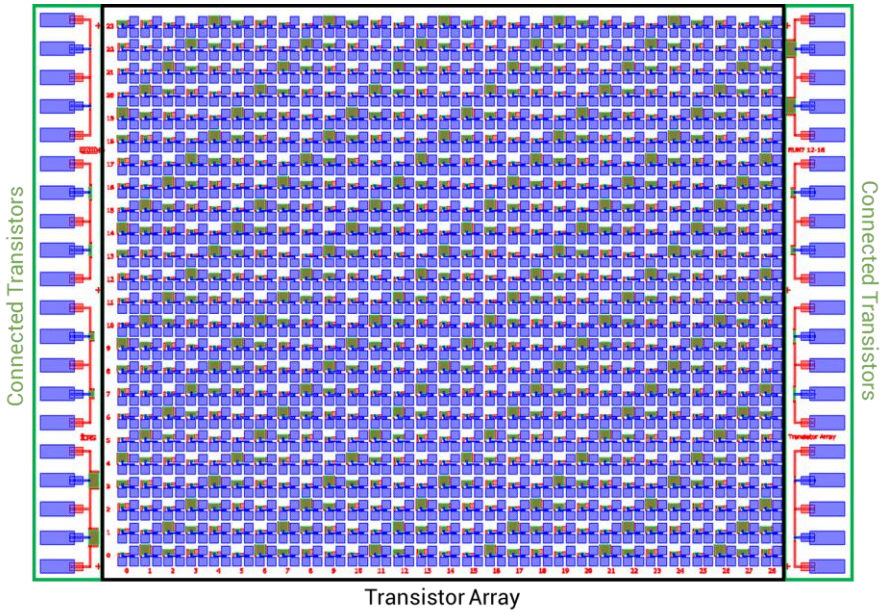

Figure 28. Transistor array design.

Regarding the connected transistors, the sequence of the transistor of one side and the other are the same. Each pair of transistors have their sources connected and can be used to implement differential pairs, current mirrors, inverters or more complex circuits using the external connections and the other transistors through the socket. In **Figure 30** the transistors pair series are shown and in the **Table 4** geometric parameters are listed.

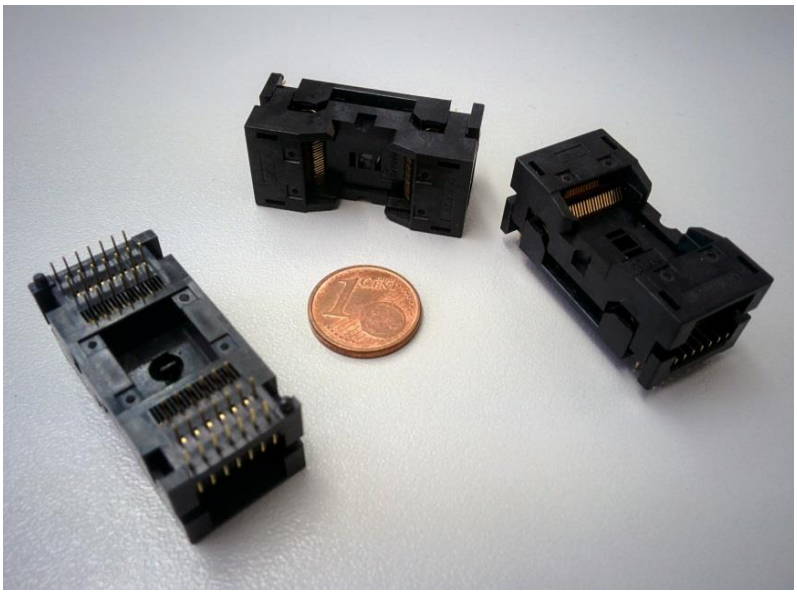

Figure 29. TSOP-4P Socket compared with 1 cent of €.

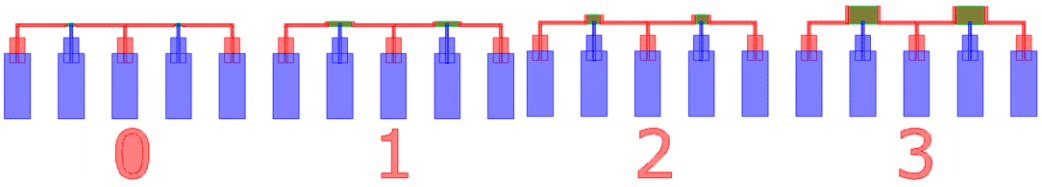

Figure 30. Transistors with pads design for external interconnection.

Table 4. Transistors with pads dimensions.

Type	Transistor dimensions
0	W=48 µm L=4 µm NF=2
1	W=200 µm L=4 µm NF=4
2	W=100 µm L=4 µm NF=8
3	W=250 µm L=4 µm NF=16

The transistor array is configured with five different dimensions, **Figure 31**. A transistor pattern of different sizes is repeated 139 times in the same order, providing a perfect distribution of the different device area around all the array. The series starts, **Figure 32**, at (0,0) position and increasing the area at following higher rows combining with an area decrease in the consecutive columns. The last transistor generated in the position (23,28) is randomly chosen and in the final design it has the dimension of type 3 transistor as defined in **Table 5**.

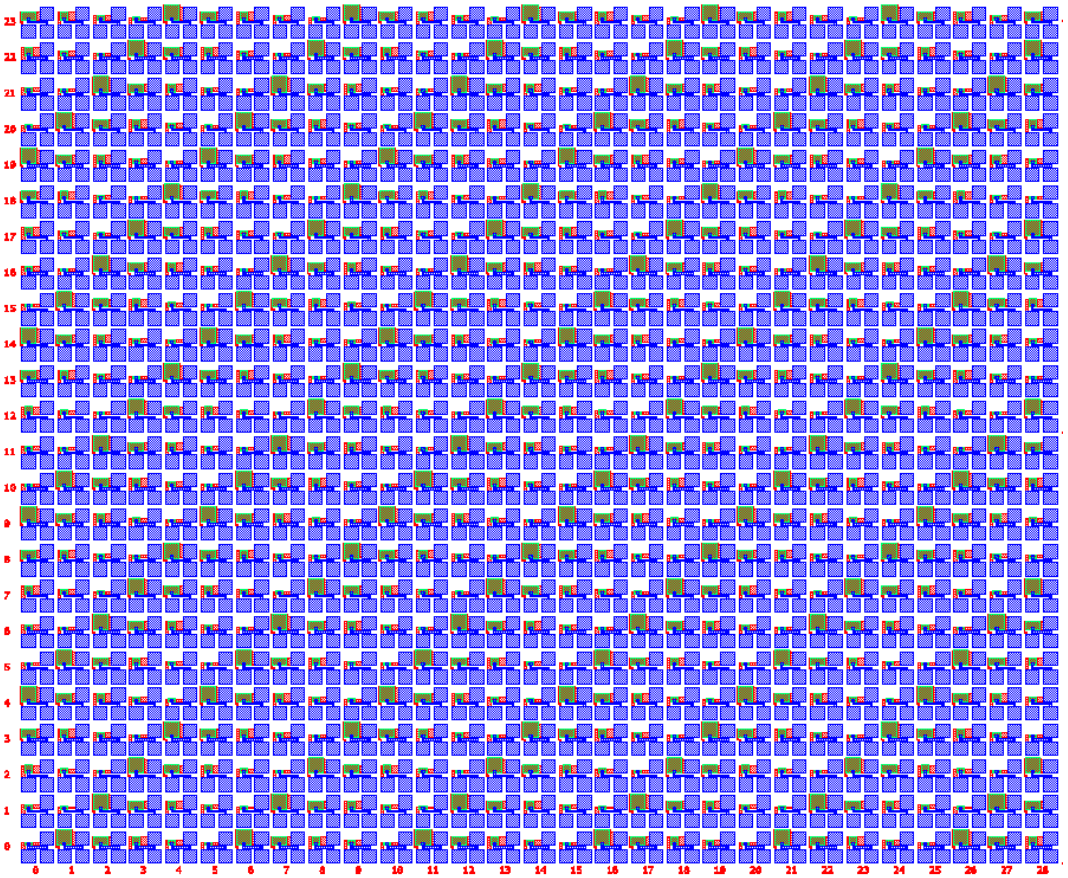

Figure 31. Transistor array.

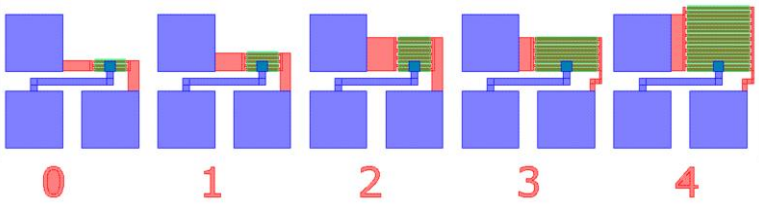

Figure 32. Array pattern sequence.

This design is distributed in the foil on 9 different positions, taking the corners and the middle of the wafer, with this scheme a homogeneous distribution of the arrays is achieved allowing a proper study of the in-wafer variability, crucial for any fabrication study to allow the commercialization of the produced systems.

Table 5. Array transistor dimensions.

Type	Transistor dimensions
0	W=80 µm L=4 µm NF=2
1	W=80 µm L=4 µm NF=4
2	W=80 µm L=4 µm NF=8
3	W=160 µm L=4 µm NF=8
4	W=160 µm L=4 µm NF=16

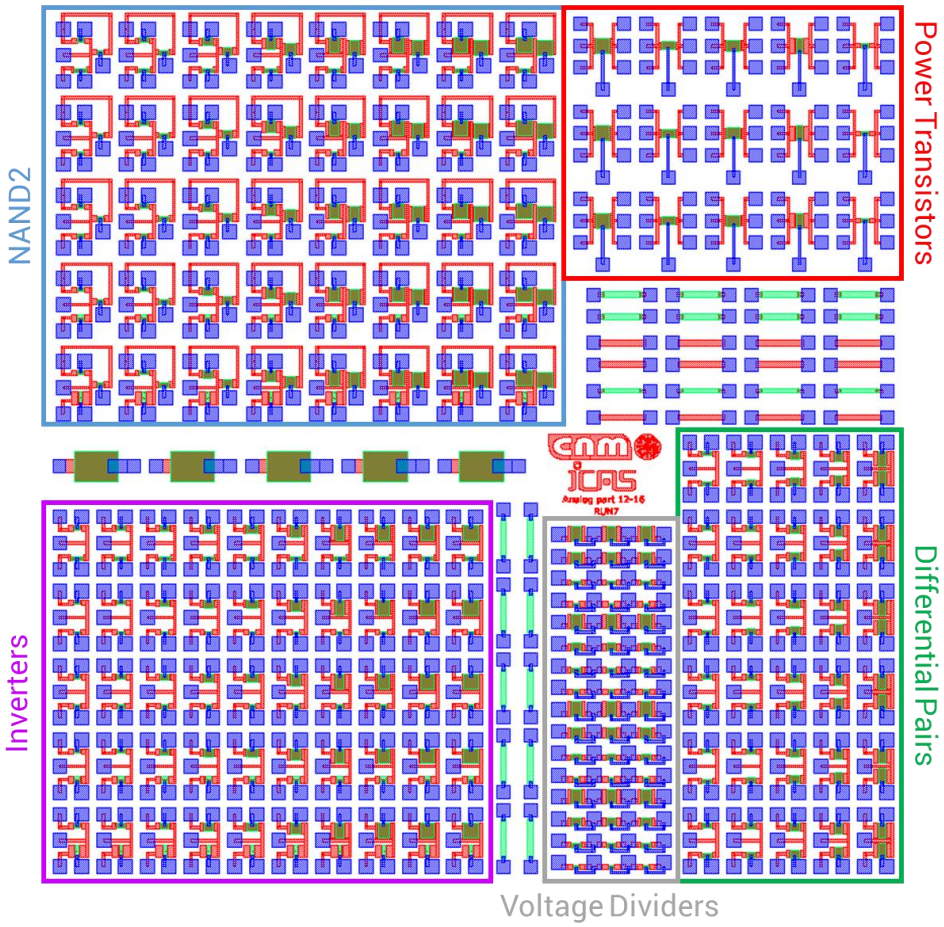

Figure 33. Analog layout design.

An analog part had been included in the run where 5 different types of analog designs were included: NAND gates, power transistors, inverters, voltage dividers and differential pairs/current mirrors. **Figure 33** shows the layout and distribution of the different circuits designed. Moreover, some technology validators are introduced in this design. The design technology validators such

as capacitors and resistances by using the different materials available in the device stack. With these devices, physical parameters of the materials can be extracted, in **Figure 34** these validators are pinpointed. Capacitances, metal resistances and semiconductor resistances are included in order to characterize them for assure a successful run fabrication. The area occupied for this layout is 9.700 µm by 9.900 µm.

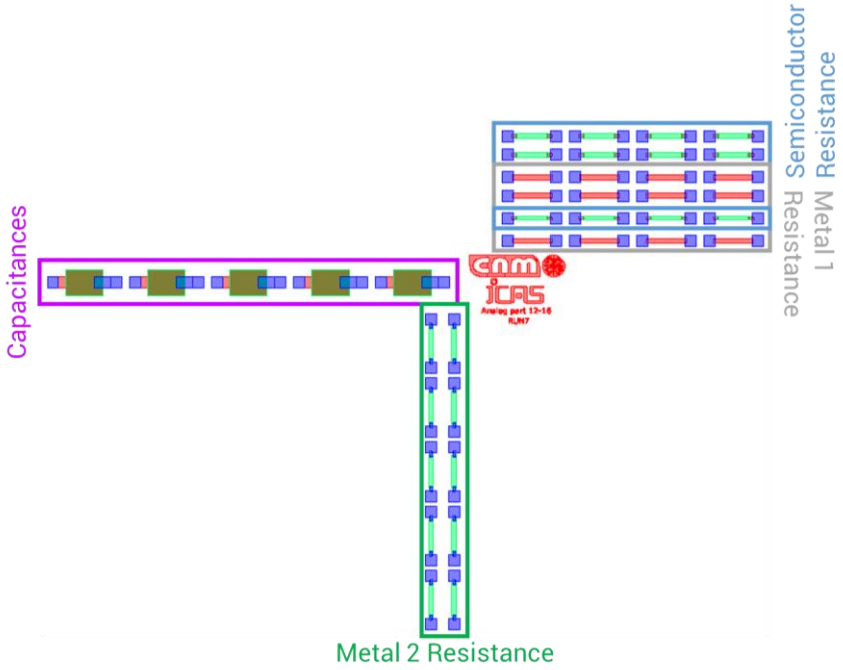

Figure 34. Technology validators distribution.

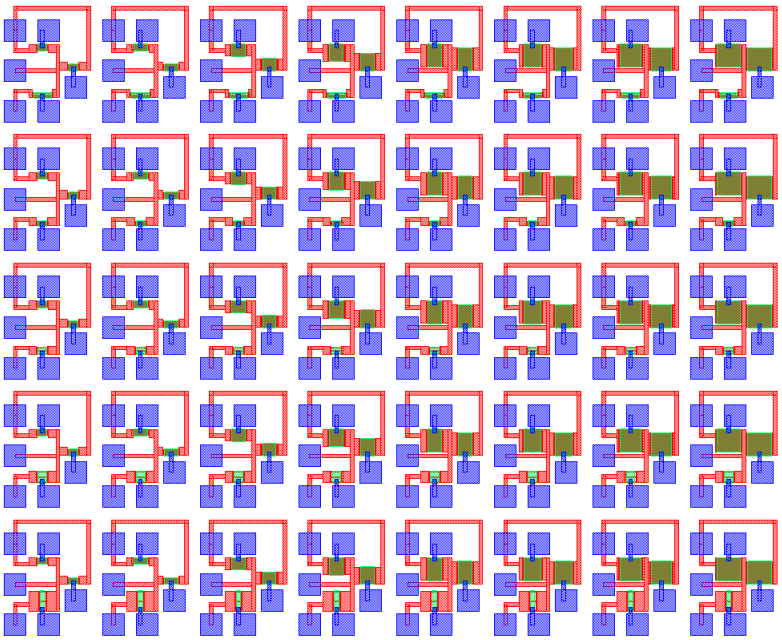

Figure 35. NAND-2 array.

NAND gate with two inputs is distributed in a matrix of 5 rows by 8, providing a total of 40 gates with different sizes, layout is shown in **Figure 35**. Dimension of the load transistors rely on the row where the device is, **Table 6** , and column has different dimensions of the input pair of transistors, **Table 7**.

Table 6. NAND-2 load transistor dimensions.

Row	Load transistor dimensions
0	W=32 µm L=64 µm NF=2
1	W=64 µm L=32 µm NF=2
2	W=64 µm L=16 µm NF=2
3	W=64 µm L=8 µm NF=2
4	W=128 µm L=8 µm NF=2

Table 7. NAND-2 input transistors dimensions.

Column	Input transistor dimension
0	W=64 µm L=4 µm NF=4
1	W=100 µm L=4 µm NF=4
2	W=100 µm L=4 µm NF=8
3	W=100 µm L=4 µm NF=12
4	W=100 µm L=4 µm NF=16
5	W=125 µm L=4 µm NF=16
6	W=150 µm L=4 µm NF=16
7	W=175 µm L=4 µm NF=16

Inverter circuits are distributed in a matrix of 5 rows by 10 columns, providing 50 inverters of different sizes, **Figure 36** shows the inverter layout. Following the same methodology than NAND gates, each row had a different input transistor dimension, **Table 8**, while the load transistor dimension change in each column, **Table 9**.

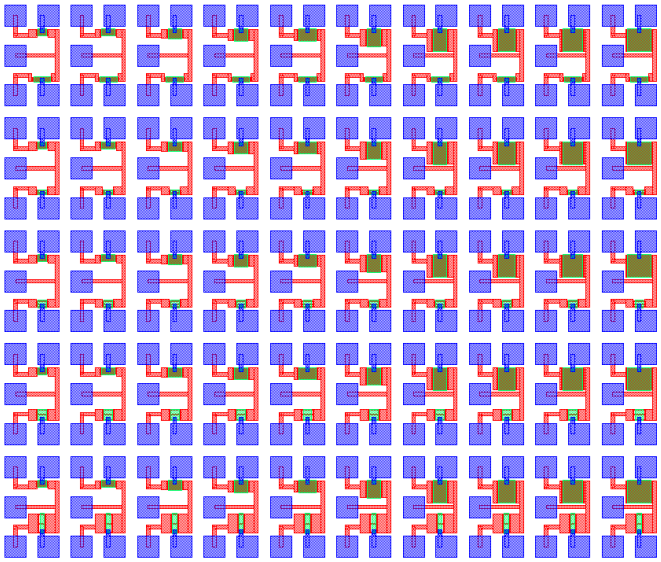

Figure 36. Inverter array.

Table 8. Inverter input transistors dimensions.

Column	Input transistor dimensions
0	W=64 µm L=4 µm NF=4
1	W=100 µm L=4 µm NF=4
2	W=100 µm L=4 µm NF=6
3	W=100 µm L=4 µm NF=8
4	W=125 µm L=4 µm NF=8
5	W=100 µm L=4 µm NF=12
6	W=100 µm L=4 µm NF=16
7	W=125 µm L=4 µm NF=16
8	W=150 µm L=4 µm NF=16
9	W=175 µm L=4 µm NF=16

Table 9. Inverter load transistors dimensions.

Row	Load transistor dimensions
0	W=32 µm L=64 µm NF=2
1	W=64 µm L=32 µm NF=2
2	W=64 µm L=16 µm NF=2
3	W=64 µm L=8 µm NF=2
4	W=128 µm L=8 µm NF=2

A voltage divider is designed using three equal transistors in serial connection, **Figure 37**, in total 16 voltage dividers have been designed with 8 different dimensions, **Table 10**. All the transistors in the same voltage divider have identical dimensions.

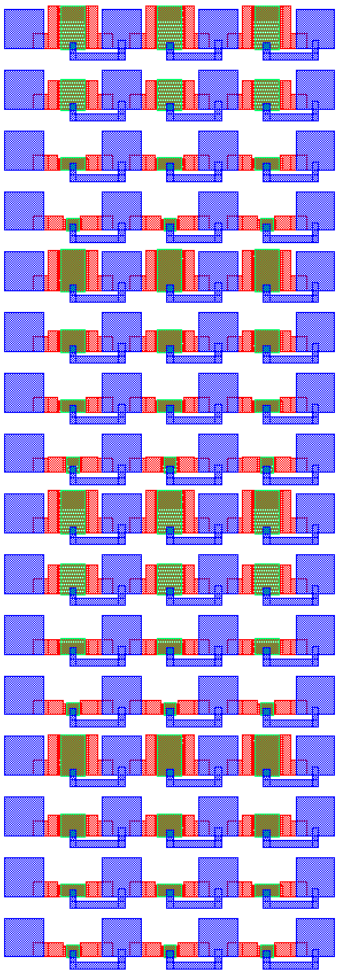

Figure 37. Voltage reference array.

Table 10. Voltage reference transistors dimensions.

Row	Transistor dimensions
0	W=50 µm L=4 µm NF=4
1	W=100 µm L=4 µm NF=4
2	W=100 µm L=4 µm NF=8
3	W=100 µm L=4 µm NF=16
4	W=50 µm L=8 µm NF=4
5	W=100 µm L=8 µm NF=4
6	W=100 µm L=8 µm NF=8
7	W=100 µm L=8 µm NF=12

A differential pair is designed and distributed in a matrix of 5 rows by 6 columns, where each pair of transistors is repeated in each row, **Figure 38**. In all the differential pairs, both the transistors had the same dimensions, **Table 11**. Since both transistors share only one pad, the device can be used as current mirror with proper connections implemented outside the die.

Table 11. Differential pair transistor dimensions.

Column	Load transistor dimensions
0	W=100 µm L=4 µm NF=4
1	W=100 µm L=8 µm NF=4
2	W=100 µm L=4 µm NF=8
3	W=80 µm L=8 µm NF=8
4	W=80 µm L=4 µm NF=16

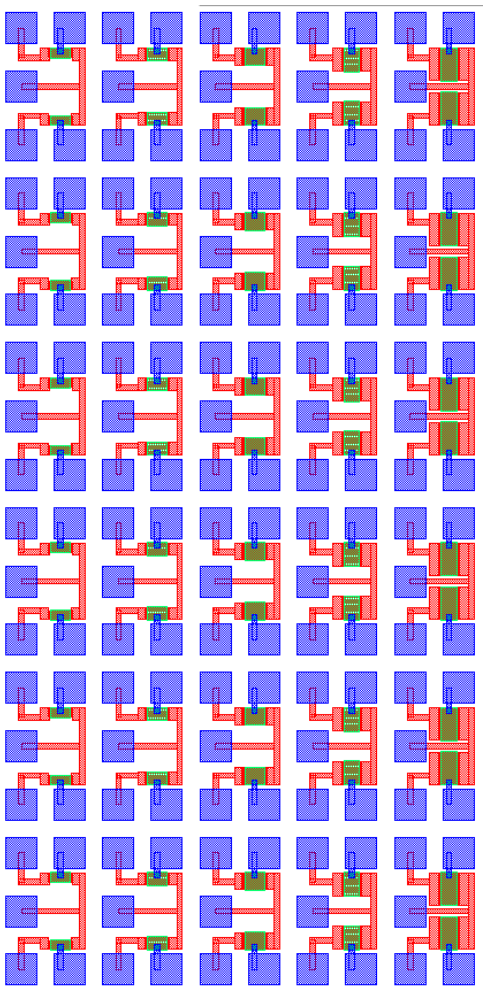

Figure 38. Differential pair array.

Additionally, to the presented circuits, 15 power transistors, **Figure 39**, with 5 different sizes had been introduced, **Table 12**. This special design of the transistors will allow the thermal observation of the current flow in the device depending in which pad are used to introduce the bias current.

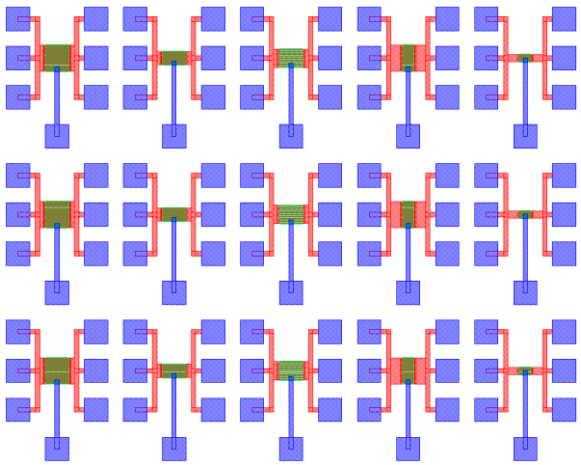

Figure 39. Power transistors array.

Table 12. Power transistor dimensions.

Colum	Transistor dimension
0	W=150 µm L=4 µm NF=16
1	W=150 µm L=4 µm NF=8
2	W=150 µm L=8 µm NF=8
3	W=75 µm L=4 µm NF=16
4	W=75 µm L=4 µm NF=4

In this wafer the layout presented have an area of around 1.500 mm^2 and more than 6.600 devices had been designed and integrated. The structure had allowed the automatic characterization setup and the modeling automation developed in this thesis.

3.2 Automatic layout generation of dual gate devices

Taking the advantage of the work done and the experience acquired with the first run, at the final stage of the thesis another PDK was started to be developed for SmartKem Ltd. company, which works on organic devices manufactured with photolithographic processes with a dual gate stack improving the performance of the devices compared with the other organic transistors.

The fully solution dual gate devices with bottom source drain contact and top and bottom gate contact, see **Figure 40A**, was fabricated at the Centre for Process Innovation (CPI, Sedgefield, UK) using their Gen2 photolithography facilities under the instructions of SmartKem. The process starts with 50-nm were sputter coated and patterned using photolithography and wet etching to work as bottom gate followed by spin coated truFLEX® base layer, stacked on top, another 50-nm thick of Au layer is sputtered for the drain and source contacts. The truFLEX carrier injection modification based on a as a Self-Assembled Monolayer (SAM) that modifies the work function and surface chemistry of electrodes, it controls charge injection into OSC and the uniformity of it. SAM layer is deposited over the source and drain contacts for matching the working functions of the organic semiconductor and the metal layers. Combining high mobility small molecules with a semiconducting polymer and solvents the truFLEX® Organic Semiconductor is crafted. This OSC provides a high mobility of 3 cm^2/s in channel lengths of 3 µm with a good uniformity between the different

transistors. A 12 nm thick truFLEX® OSC is spin-coated at the wafer and after a hotplate baking at low temperature a 110 nm layer of a TruFlex® Organic Gate Insulator (OGI) and a 300 nm thick TruFlex® Sputter Resistant Layer (SRL) are spin coated and baked. A 50 nm thick Au film is then sputtered as the top gate. Finally, cross-linked TruFlex® Passivation Layer is deposited to impart chemical resistance and physical integrity to the OTFT stack, see **Figure 40B**.

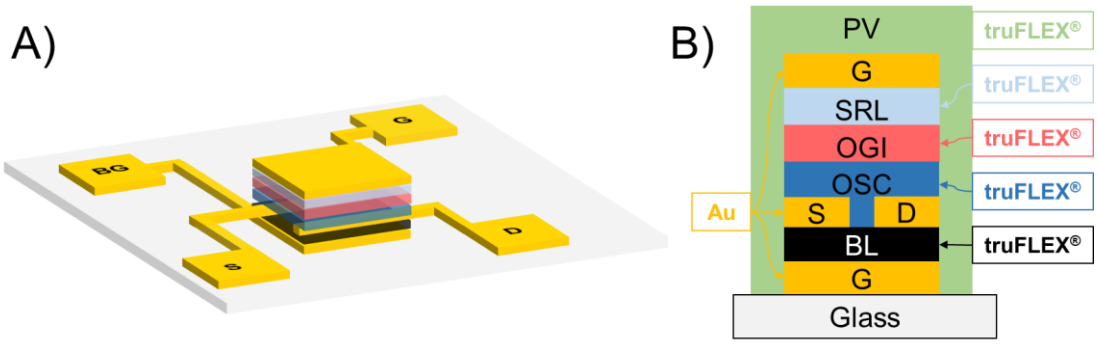

Figure 40. A) OTFT architecture and **B)** stack of materials.

The resulting devices can be fabricated in a wide range of plastics and glass, giving flexibility or robustness depending on the final application with an excellent impact resistance and a low production cost. The layout is based on four main areas, the large dual gate transistor array, combined array of OTFT and NAND gates, digital circuits area and DRC structures with technology validators. Taking advantage of this run dummy structures for IC hybridization had been designed and included in the layout. All the devices included in the layout had been generated by using PCells allowing a correct-by-construction design with a huge time saving. Additionally, using these PCells, place and route scripts had been developed for the device array automating the layout design and with the proper configuration for the automatic characterization step. The design and distribution around the wafer of the different parts in the layout can be seen in **Figure 41**.

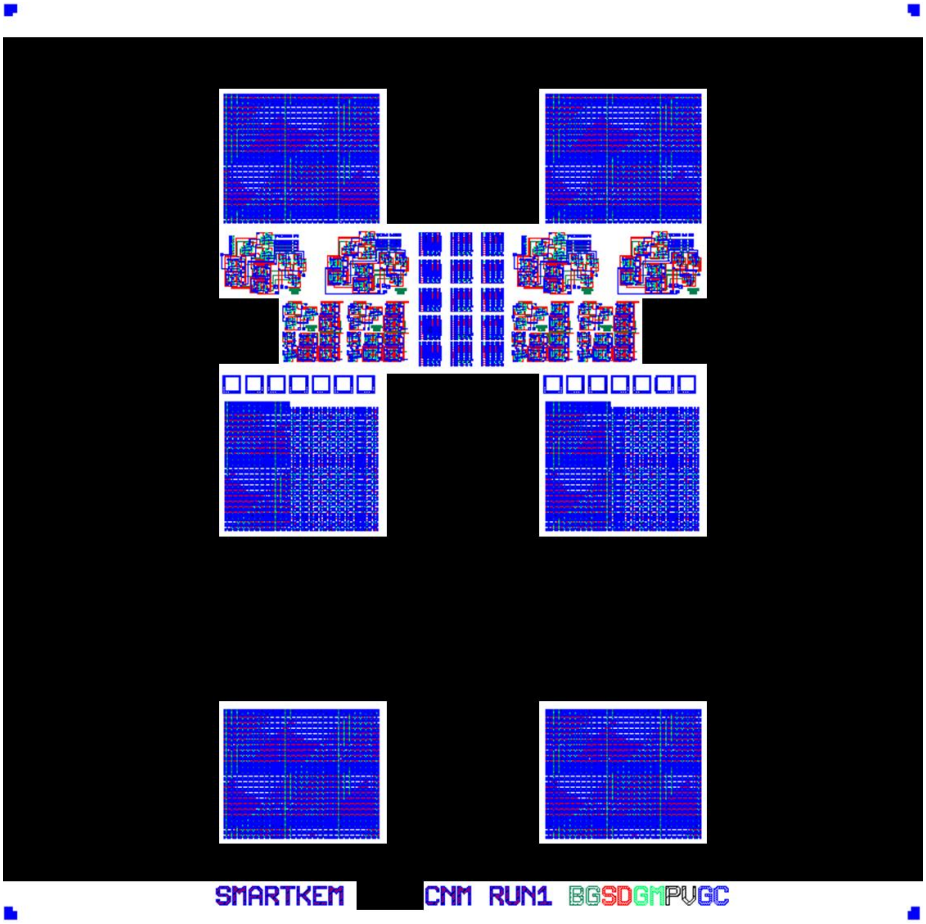

Figure 41. Run layout with 4 large dual gate OTFT in the sides complemented with the two central arrays with individual transistors and NAND gates. DRC structures and technology validators are incorporated together with dummy hybridization pads and circuits for testing.

The large dual gate array of transistor is composed by a matrix of 24 rows by 29 columns with a total transistor number of 696 distributed in 25 dimensions that are repeated 27 times around the matrix and the last 21 devices are choose randomly, see **Figure 42**.

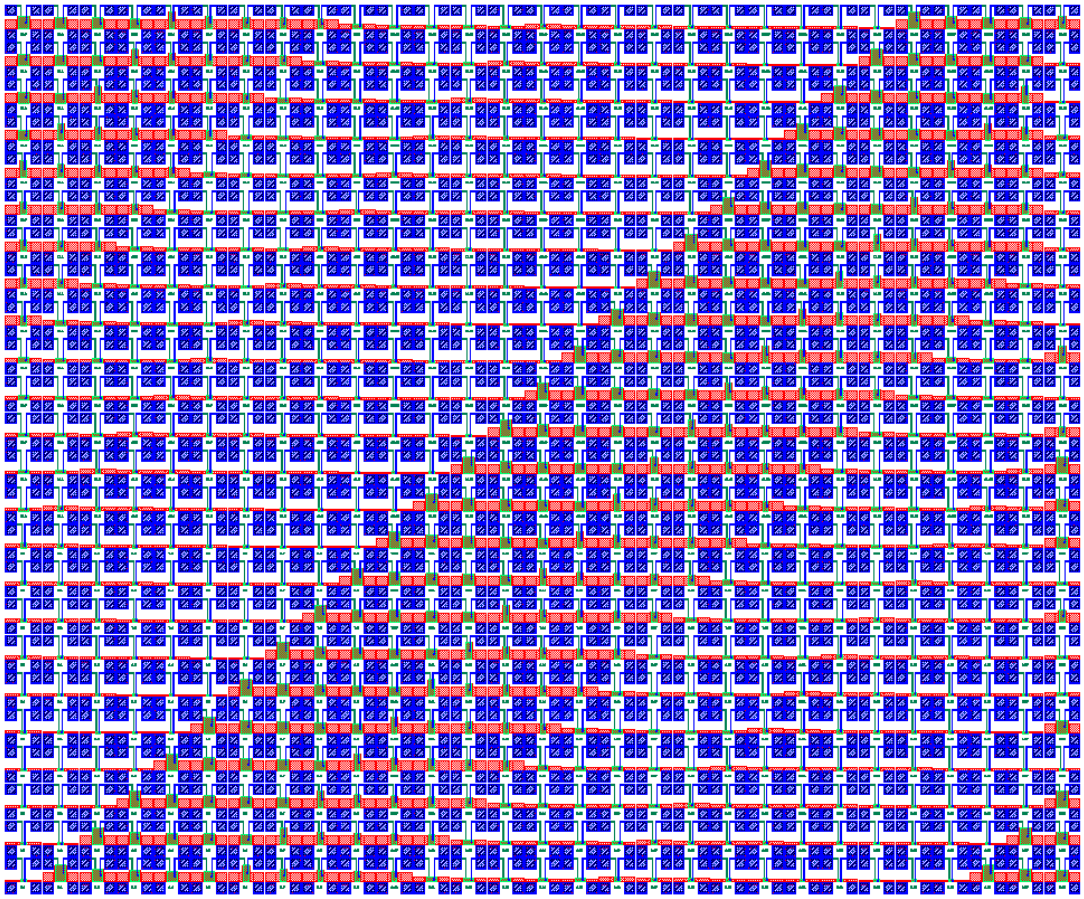

Figure 42. Large dual gate transistor array.

Table 13. Large array of dual gate transistors dimensions.

Type	Transistor dimensions
0	W=80 µm L=3 µm NF=2
1	W=80 µm L=4 µm NF=2
2	W=80 µm L=5 µm NF=2
3	W=80 µm L=6 µm NF=2
4	W=80 µm L=10 µm NF=2
5	W=80 µm L=3 µm NF=4
6	W=80 µm L=4 µm NF=4
7	W=80 µm L=5 µm NF=4
8	W=80 µm L=6 µm NF=4

Type	Transistor dimensions
9	W=80 µm L=10 µm NF=4
10	W=160 µm L=3 µm NF=4
11	W=160 µm L=4 µm NF=4
12	W=160 µm L=5 µm NF=4
13	W=160 µm L=6 µm NF=4
14	W=160 µm L=10 µm NF=4
15	W=80 µm L=3 µm NF=16
16	W=80 µm L=4 µm NF=16
17	W=80 µm L=5 µm NF=16
18	W=80 µm L=6 µm NF=16
19	W=80 µm L=10 µm NF=16
20	W=160 µm L=3 µm NF=16
21	W=160 µm L=4 µm NF=16
22	W=160 µm L=5 µm NF=16
23	W=160 µm L=6 µm NF=16
24	W=160 µm L=10 µm NF=16

Focusing on the central matrix that are composed by an array of dual gate transistors followed by and array of a NAND gates with two inputs and dual gate control, see **Figure 43**. The OTFT is distributed in 24 rows and 12 columns, giving a total number of 288 devices with 25 different combinations of widths and lengths, **Table 13**, that is repeated 11 times and the 13 left devices had been chosen randomly. The NAND array is formed by 23 rows and 10 columns, presenting 229 logic gates with 7 different width length ratios between the input transistors and the driver one, **Table 14** and **Table 15**, repeated 32 times and the left 5 sizes chosen randomly.

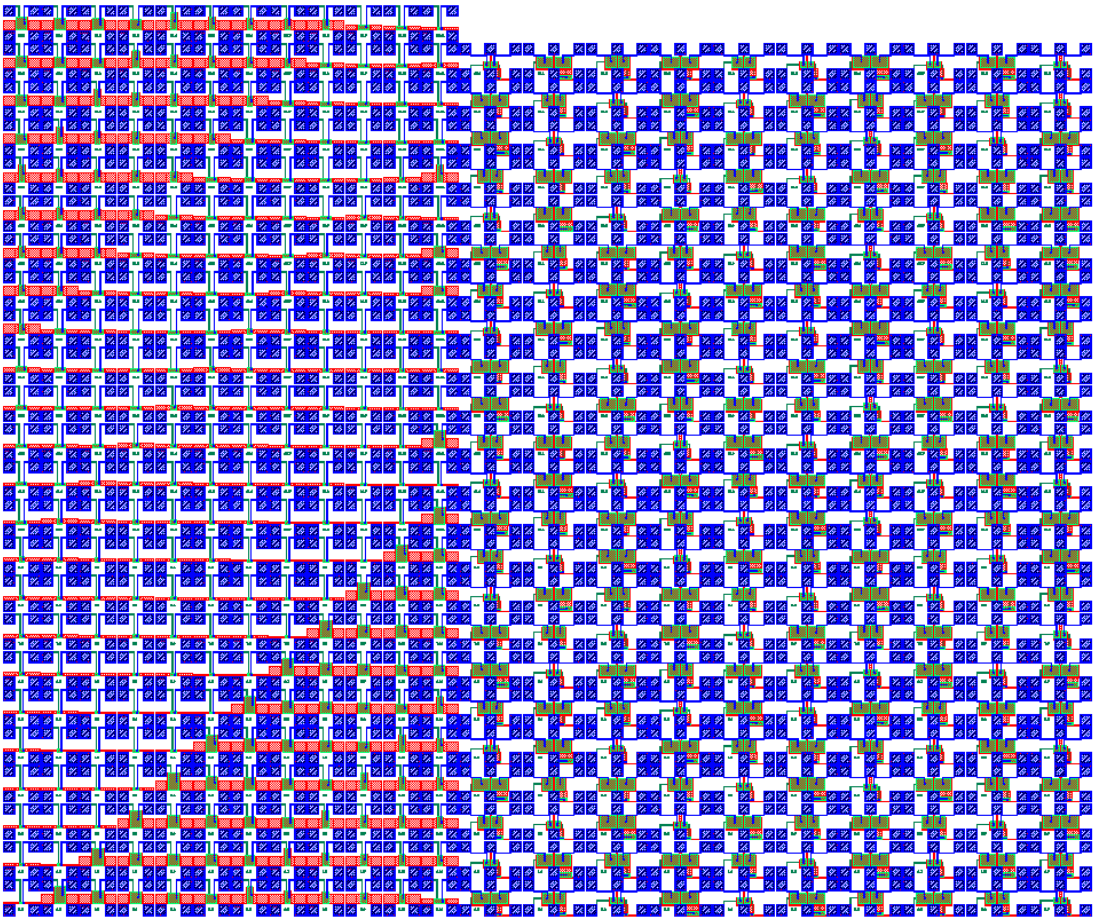

Figure 43. Central array with the dual gate transistors on the right and the NAND gates on the left.

Table 14. NAND-2 input dual gate transistors dimensions.

Type	Input transistor dimensions
0	W=250 µm L=4 µm NF=16
1	W=80 µm L=4 µm NF=8
2	W=160 µm L=4 µm NF=16
3	W=250 µm L=5 µm NF=16
4	W=80 µm L=5 µm NF=8
5	W=160 µm L=5 µm NF=16
6	W=250 µm L=5 µm NF=16

Table 15. NAND-2 load dual gate transistors dimensions.

Type	Load transistor dimensions
0	W=20 µm L=10 µm NF=4
1	W=20 µm L=4 µm NF=4
2	W=40 µm L=4 µm NF=8
3	W=60 µm L=4 µm NF=16
4	W=20 µm L=5 µm NF=4
5	W=40 µm L=5 µm NF=8
6	W=60 µm L=5 µm NF=16

The PCells of the OTFT and NAND gates used can be seen in **Figure 44**. The channel length, width and number of channels can be configured under the limitations imposed by the pads position and the DRC rules imposed, allowing a quick and reliable system to design the arrays and circuits.

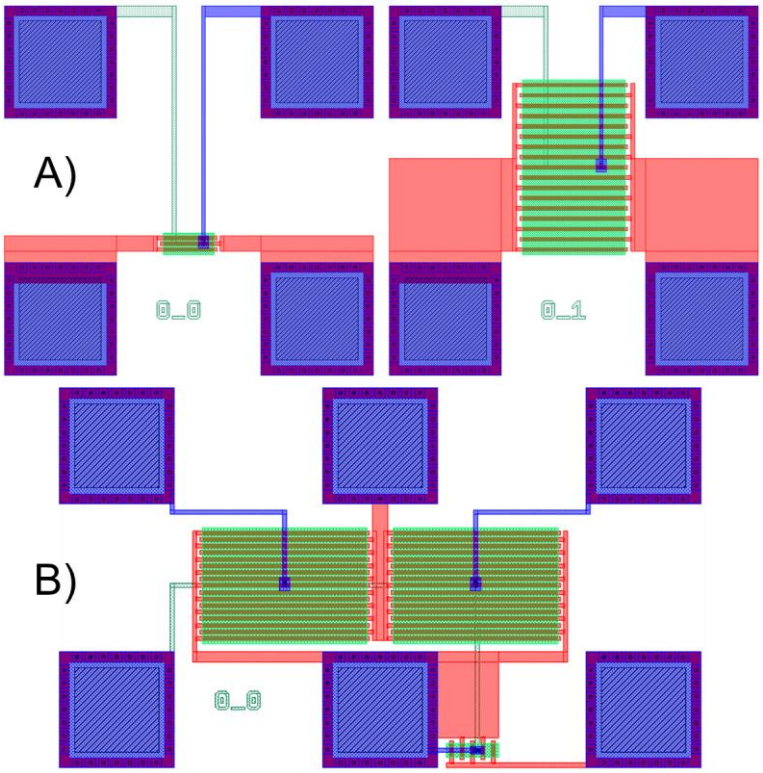

Figure 44. PCell **A)** of the dual gate transistor **B)** and NAND gate.

The main digital circuit part is composed by two RFID tags with programmable memory, one without internal clock and the other with a seven stages ring oscillator, see **Figure 45**. The RFID tags are composed of a 4-bit counter and two multiplexer with 4-inputs connected to a PROM memory that allows being programmed through inkjet printing, more detailed information at the RFID system design section of this thesis can be found.

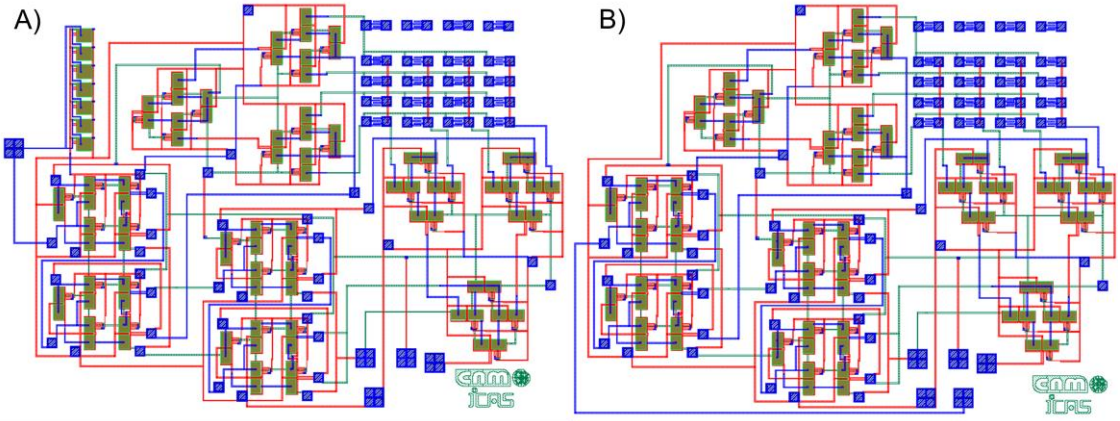

Figure 45. **A)** RFID tag with ring oscillator, **B)** RFID tag without internal clock.

The digital subcircuits part is composed with type D Flip Flops, multiplexers of 2- and 4-inputs and a counters of 2 and 4 bits, see **Figure 46**, the section is repeated two times at the circuit area. All these different circuits were combined for the RFID system. The NAND gates ratio had been optimized at the RFID system design section of this thesis.

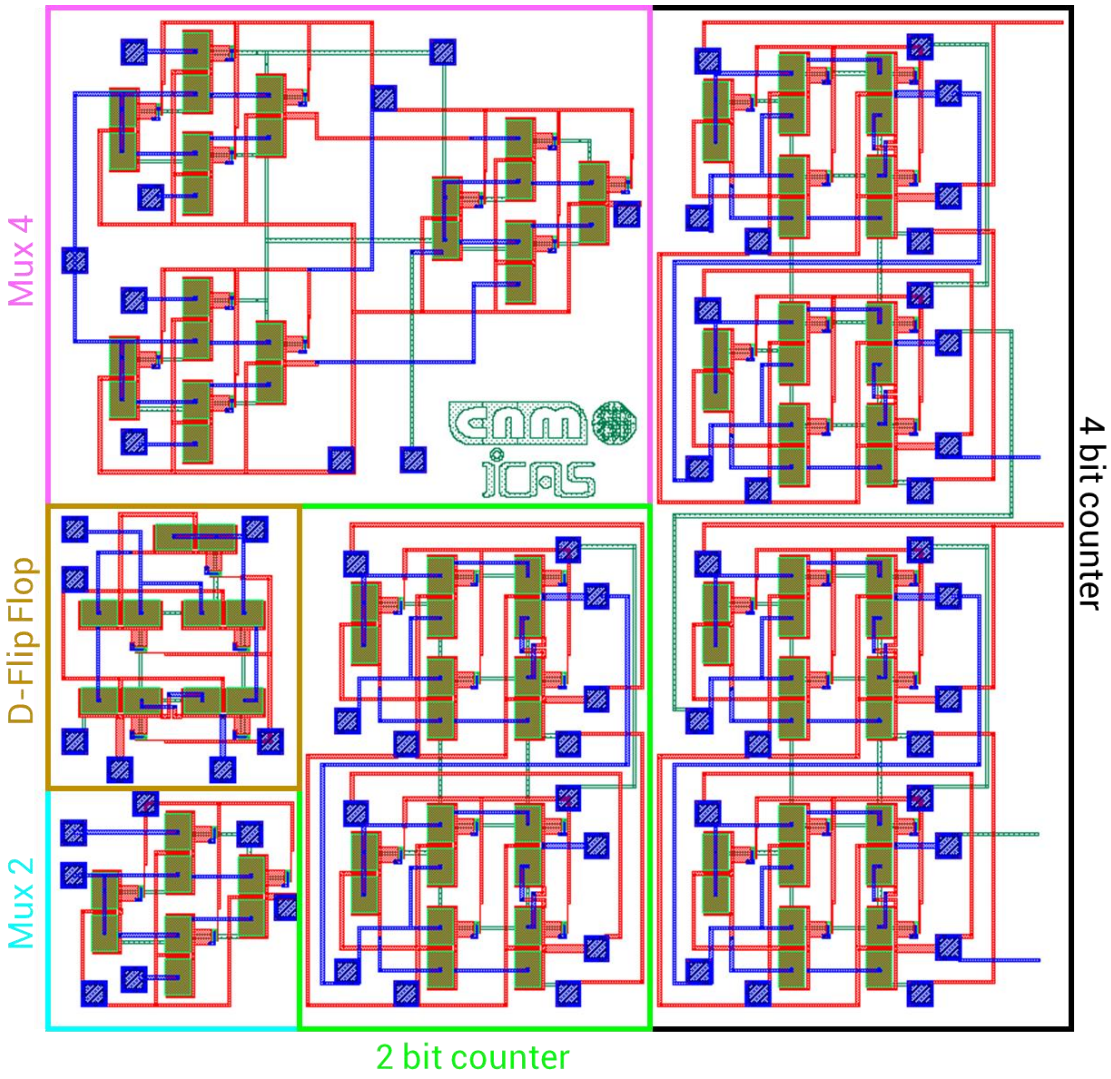

Figure 46. Subcircuits designed for testing.

Technology validators and DRC structures are grouped in a small area that repeats 15 times, for proper validation in the central area of the wafer. Examples of validators includes the extraction of the resistance of the different layers together with capacitances. The DRC structures pursue the extraction of basic rules to avoid fabrication problems. The complete set of devices are depicted at **Figure 47**.

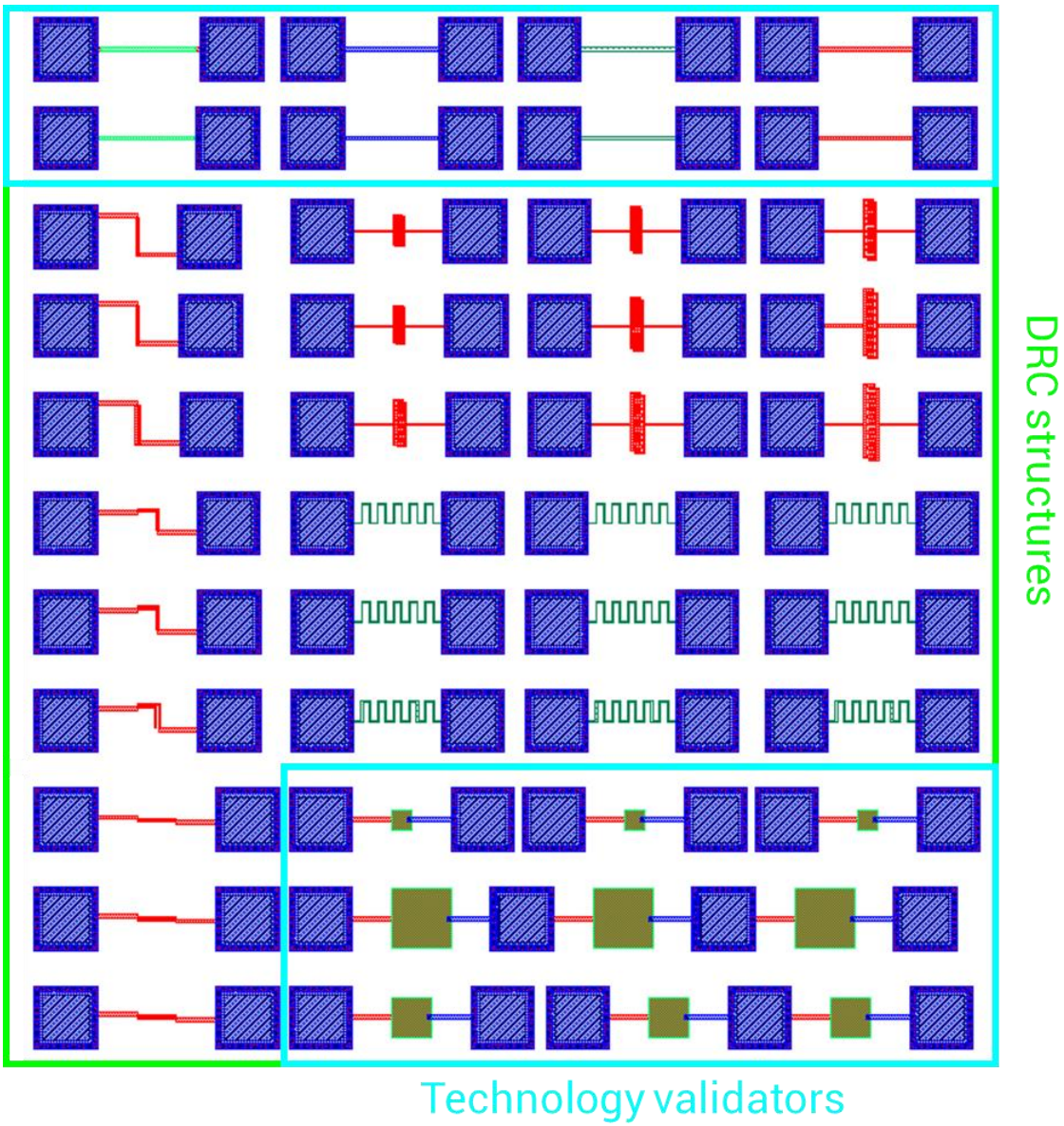

Figure 47. DRC structures and technology validators.

In this wafer, the layout presented have an area of around 2.255 mm^2 and more than 5.500 devices had been designed, it is expected to be characterized with the automatic characterization setup developed in this thesis.

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4 Device Modelling

Models are developed with the objective to achieve an analytical way to express the device behaviour. The use of mathematical expressions helps to know, understand and simulate the modelled system.

OTFT and Metal Oxide Semiconductor Field Effect Transistor (MOSFET) transistors have different physical stacks of materials and fabrication techniques [1], regards that fact, lot of the work carried on in OE is based in the well-studied model of MOSFET devices [2], since the OTFT presents a similar behaviour. Additionally some specific models of the OTFT had been developed, looking after a physical meaning, WB, [3], or like almost of the models used, with an analytical bases, GB, [4]–[7], developing the model from the acquired data and some physics fundamentals. Moreover, some pure mathematical models had been also tested, BB, [8], [9]. Additionally, few groups had developed methods to extract the coefficients using neural networks [10].

Compact models provides a bridge between fabrication technology, circuit simulation and design [11]. The compact models must be simple enough to be incorporated in circuit simulators and sufficiently accurate to make the simulator results useful for circuit designers [12]. Compact modelling is based in parametric equations that use different parameters inspired in the behaviour of the device.

All the data used in the modelling had been extracted from the characterization of the devices presented in the layout generation by using the automatic characterization system developed.

4.1 Overview of characterization and modelling techniques

The initial step for a correct automatic characterization system is to know the type of measurement to be done and their requirements, that are defined by the following parameters:

- **Accuracy**: as the degree of the closeness with which instrument reading approaches the true value of the quantity being measured.
- **Sensitivity**: as the ratio in the magnitude response of the output signal to the magnitude response of the input signal.
- **Reproducibility**: as the degree of the closeness with which a given quantity may be repeatedly measured.

Electrical characterization of organic devices is not different than in the silicon electronics and multiple works had already been published [13], [14]. Regards resistance, Hall Effect, capacitance-voltage (C-V), charge pumping or low-frequency noise measurements are usual, from a modelling point of view the main characterization procedure is based on current-voltage (I-V) curves. IV curves are widely used for parameter extraction, moreover, they can provide valuable information about the quality of materials used and the general device behaviour, in **Figure 48** an example of transistor curves can be seen.

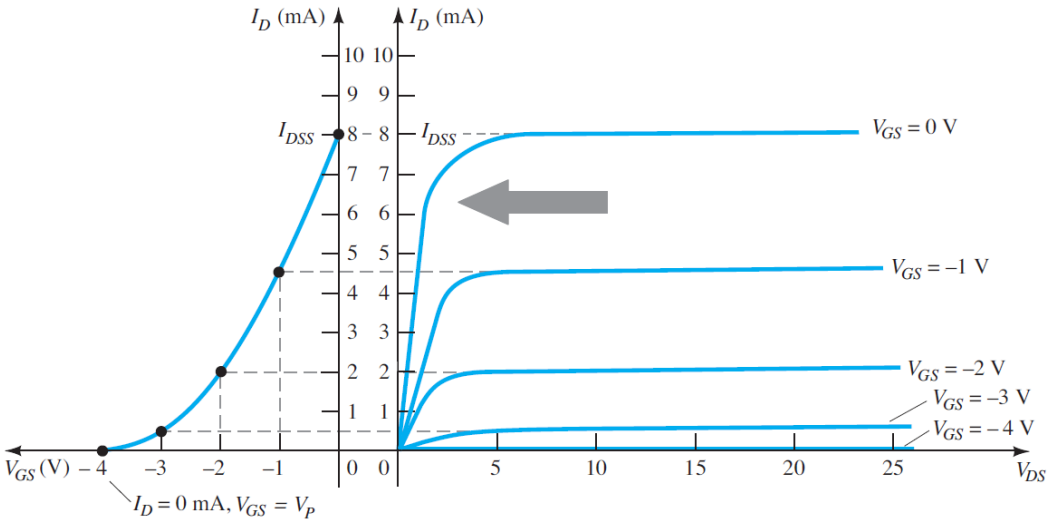


Figure 48. Transfer and output curves of a Field Effect Transistor (FET) [15].

I-V measurements can be used to obtain information about the quality of the semiconductor, contacts, oxide and semiconductor–oxide interface, but the most important part form a modelling point of view is the opportunity to extract model parameters form these curves. In the case of an OTFT, the parameters that can be extracted are the threshold voltage (V_T), the transconductance (g_m), the

mobility (μ), the parasitic source (R_S) and the drain resistances (R_D) in series with the intrinsic channel resistance, the channel length reduction ΔL, the output conductance (g_{DS}) and the subthreshold slope (SS) among others.

Following the classification introduced in the state of the art, models can be organized in BB, GB and WB, depending on the device physics knowledge. Since OE is an emerging technology there are few WB models available since they require a deep study into the physics of the device. GB and BB models needs of an optimization or fitting step to obtain the best statistical parameters. This optimization step can be done with multiple mathematical ways like neural networks, genetic algorithms, polynomial algorithms, machine learning or random parameter generators.

Error metric is fundamental in the parameter optimization step, each metric will be more appropriated than other depending on the data and optimization type. Since the error metrics are almost limitless, the most popular are listed: Mean Squared Error (MSE), Root Mean Square Error (RMSE), Mean Absolute Scaled Error (MASE), Mean Absolute Percentage Error (MAPE), Symmetric Mean Absolute Percentage Error (SMAPE) and Integral Square Error (ISE).

The objective of curve fitting is to select functional coefficients which minimize the total error over the set of data points being considered. With a functional form and an error metric selected, curve fitting becomes an optimization problem over a set of given data points.

4.2 Automatic characterization system

The developed and maintained characterization system is based on the automatization of two main instruments, semiconductor analyser and semiautomatic probe station, connected through a General-Purpose Instrumentation Bus (GPIB) to the system controller. The full system is coordinated by means of Python scripts with a simple and effective graphic interface, which allow high adaptability to new technologies, devices and basic building blocks in the setup. The system controller coordinates the instruments involved, which comprise the semiconductor analyser and the semi-automatic probe station, also is in charge for the report generation. A scheme of the system is shown **Figure 49**.

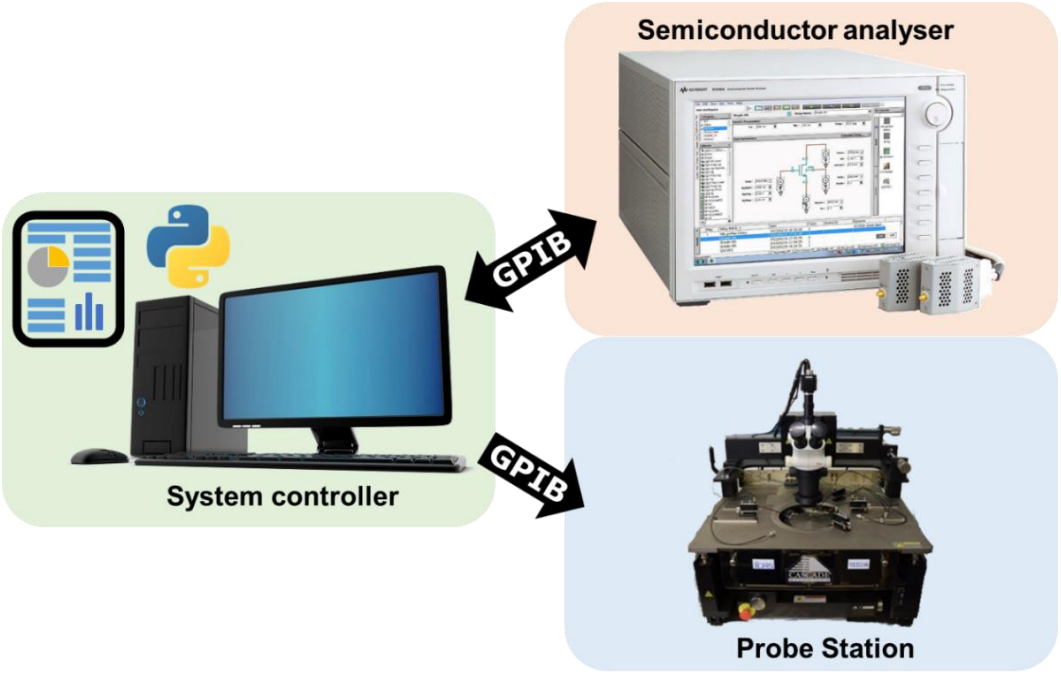


Figure 49. Automatic characterization system schema.

Characterization automation is based on Standard Commands for Programmable Instruments (SPI) commands properly configured for obtaining the desired data with the accuracy, sensitivity and reproducibility required. The report script generator starts to work with the characterization step to avoid any problem if the setup finds problems in the middle of the test and stops, storing the received device data after is acquired and thus providing robustness to the system. At the end of the measurements a report with transfer and output curves for specified voltages are extracted for each device. Furthermore, key parameters are calculated such as device mobility, threshold voltage, turn on voltage, maximum current, minimum current, maximum/minimum current ratio, maximum gate current, maximum transconductance, maximum connection resistance and maximum sub-threshold swing. Position maps are also generated allowing identification of the different devices. Global statistical data is extracted allowing a quick overview of how the characterization of the run parameters and how the devices performed. Part of the single transistor report can be seen **Figure 50**.

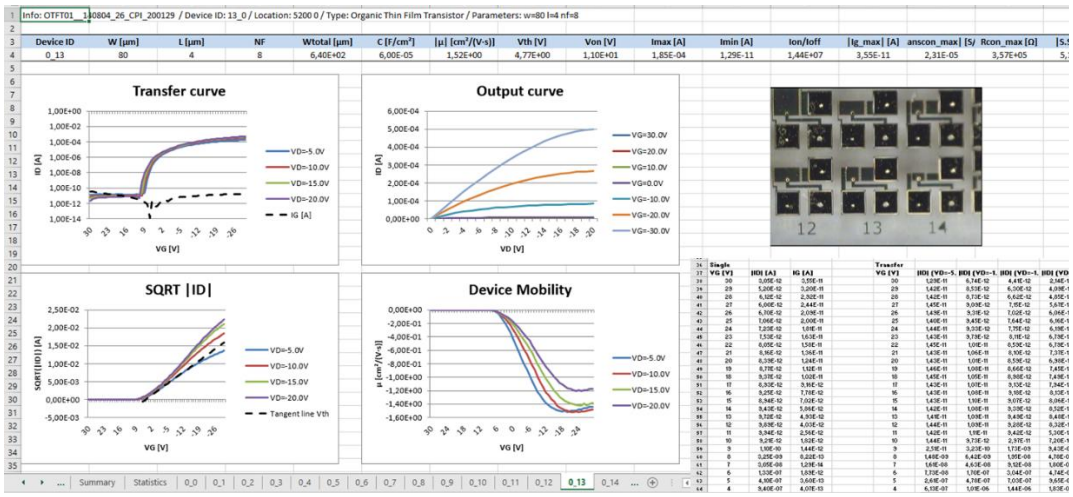


Figure 50. Report example of individual transistor with graphics, images and data obtained.

Ongoing with the automatic report generator, tendencies in sizes and run positions are identified via calculation of statistical distributions of key parameters such as device mobility, threshold voltage, turn-on voltage, maximum current, minimum current, maximum/minimum current ratio, maximum gate current, maximum transconductance, maximum connection resistance and maximum sub-threshold swing in different graph like gaussian distribution, heat map position and box chart with size classification. Furthermore, the statistical report can include raw data of non-normalized devices or data of normalized devices allowing the analysis of the best geometry ratio, some tendencies can be seen **Figure 51**. For summarizing all the information of the characterization, a dynamic table with the device parameters is included where defective OTFT and parameter are highlighted to allow fast identification and the root cause.

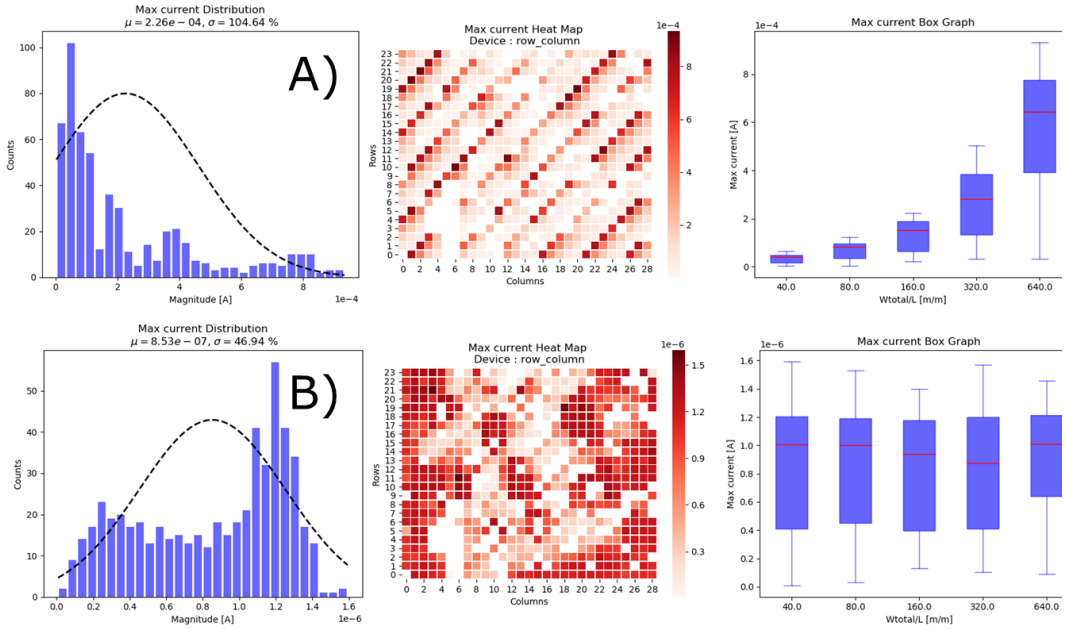


Figure 51. **A)** Raw maximum current distribution row and **B)** Normalized by size of each device maximum current row.

The methodology for the device characterization can also be used for basic building blocks. In this case, the characterization is performed on inverters, but the setup can be adapted to any circuit of up to 6 Source Measurement Units (SMU). Position matrix is generated for basic building block identification. Global statistics are also extracted, and the data of each circuit is represented in graphs. Key parameters are also obtained i.e., maximum gain in the case of an inverter, see **Figure 52**. Statistical distributions of key parameters such as gain are calculated to allow identification of tendencies in size and run positions, following the methodology developed for the OTFT.

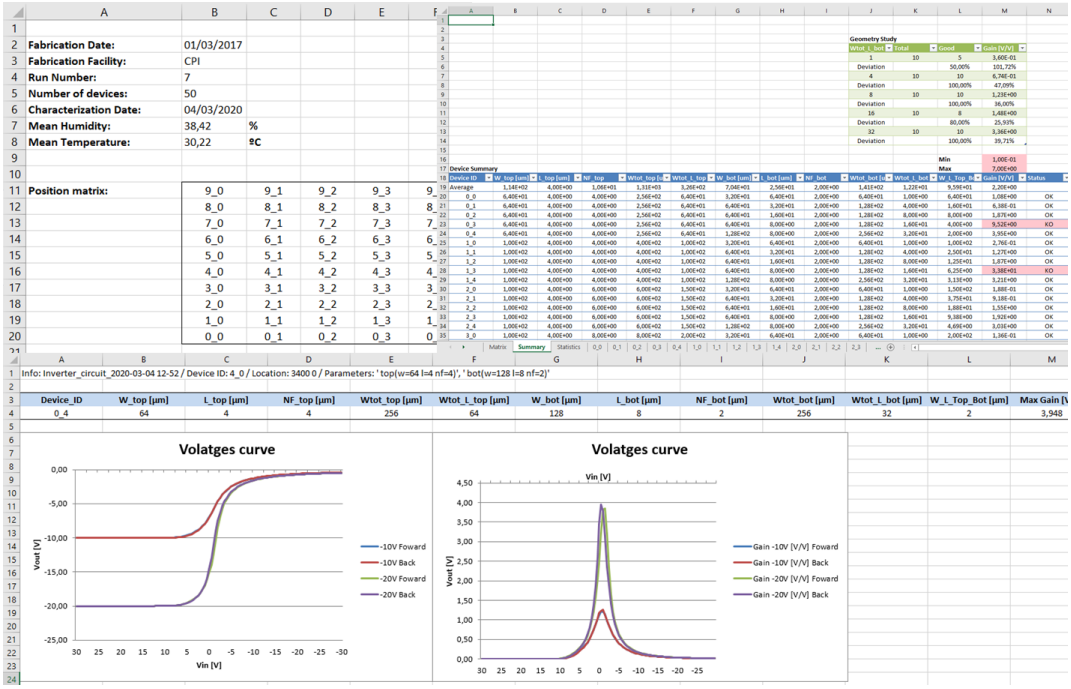


Figure 52. Basic building block report example for an inverter array.

4.3 Automatic modelling procedure

For the modelling procedure automation, a set of Python scripts had been developed and optimized in order to allow the massive parametrization of devices with the model adapted. Once the characterization step had succeeded, the modelling of the device can start using the acquired data.

The parameters optimization is based in a feedback loop method based on neural networks methodology. Recursive and lower election of ISE optimization code is implemented to obtain and use the optimum parameters. Fixing the iteration number to an amount that provides a reliable value and precision this allows us to obtain repetitive and accurate statistical results for the mean values of the model parameters.

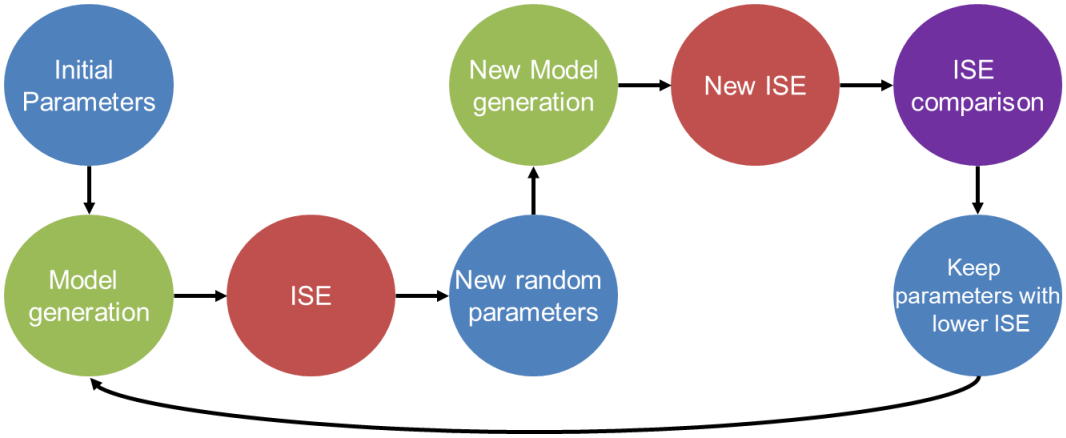


Figure 53. Flow chart parameters optimization.

As a figure of merit, the ISE will be used to represent the comparison between the model and the experimental data. With this, a quality factor of the system performance based on the square of the measure minus the theoretical value error in mean value is used. This method is very popular in the linear optimal control and estimation theory. **Figure 53** depicts the optimization method thought the basic steps. The program starts with initial parameters to generate the model, using this model and the experimental data, the first ISE value is calculated. The calculation of the new parameters is done with a ponderation of the initial values with random coefficients and a new model is generated. Again, ISE is computed and a comparison between first and second ISE values is made to keep the parameters that provides a lower ISE value, returning to the start of the iterative method.

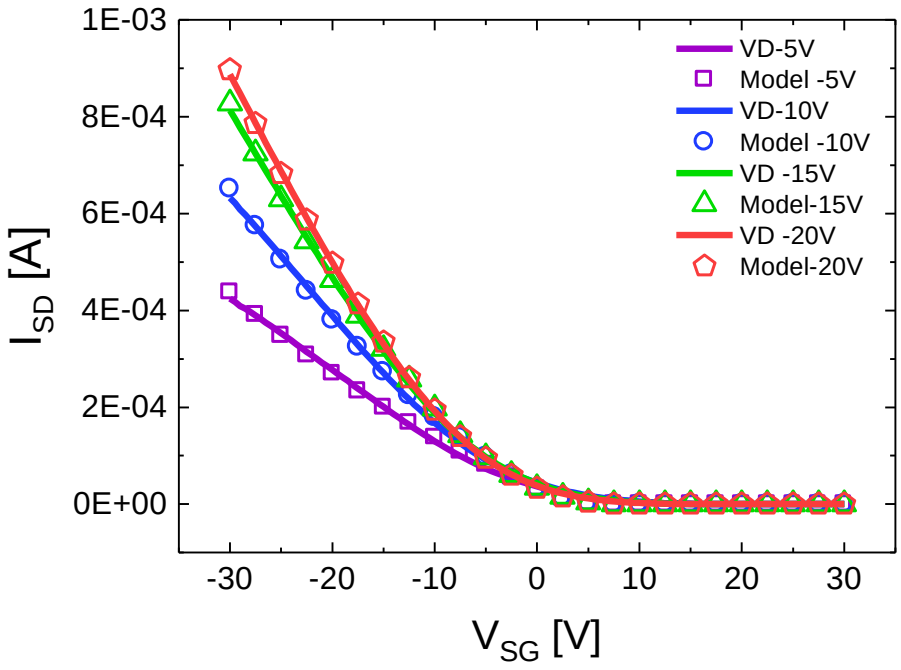
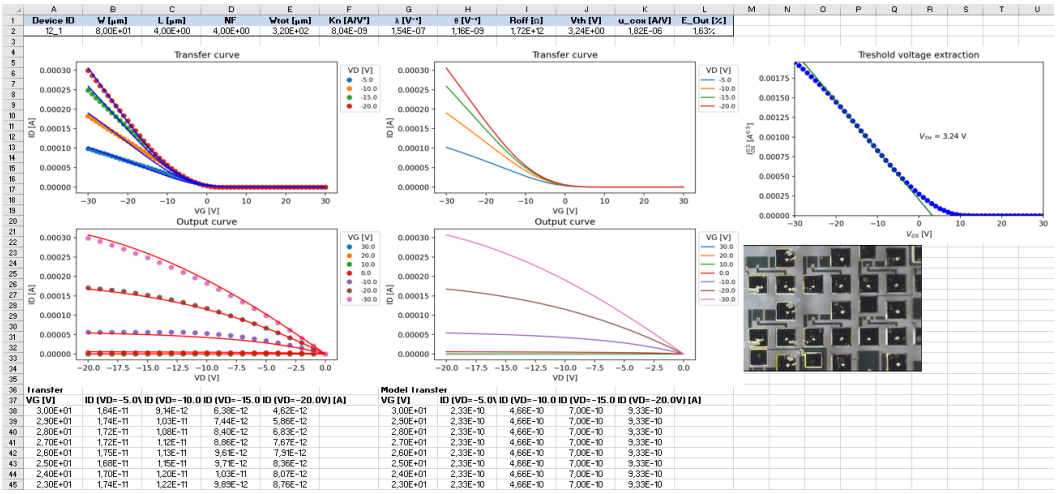


Figure 54. Transfer curves of an OTFT for different drain potentials from experimental data (lines) and model (symbols).

The resulting model and a comparison with the extracted data can be seen in **Figure 54**, for a multiple transfer curves in an OTFT. The final ISE calculated is down to 2% of the experimental data showing very good fitting.

With all the devices modelled, a report containing the model parameters of all the devices is generated, including the picture of the device, the curves of the characterization and a comparison between the device performance and the model calculations. The data of the characterization and the model calculation for those specific curves are included in each device. Additionally, the extraction of physical device parameters is depicted and the model parameters are listed, see **Figure 55**.

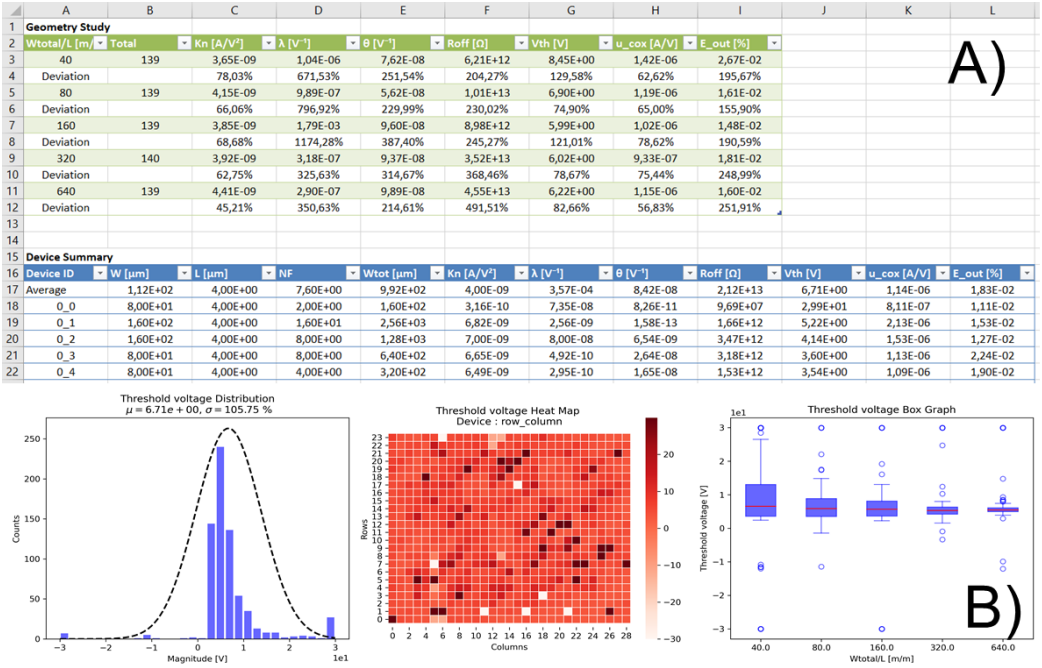


Device ID	W [µm]	L [µm]	NF	Wtot [µm]	Kn [A/V²]	λ [V⁻¹]	θ [V⁻¹]	Roff [Ω]	Vth [V]	u_cox [A/V]	E_Out [%]
12_1	8,00E+01	4,00E+00	4,00E+00	3,20E+02	8,04E-09	1,54E-07	1,16E-09	1,72E+12	3,24E+00	1,82E-06	1,63%

VG [V]	ID (VD=-5.0V)	ID (VD=-10.0	ID (VD=-15.0	ID (VD=-20.0V) [A]	VG [V]	ID (VD=-5.0V)	ID (VD=-10.0	ID (VD=-15.0	ID (VD=-20.0V) [A]
3,00E+01	1,64E-11	9,14E-12	6,38E-12	4,62E-12	3,00E+01	2,33E-10	4,66E-10	7,00E-10	9,33E-10
2,90E+01	1,74E-11	1,03E-11	7,44E-12	5,86E-12	2,90E+01	2,33E-10	4,66E-10	7,00E-10	9,33E-10
2,80E+01	1,72E-11	1,08E-11	8,40E-12	6,83E-12	2,80E+01	2,33E-10	4,66E-10	7,00E-10	9,33E-10
2,70E+01	1,72E-11	1,12E-11	8,86E-12	7,67E-12	2,70E+01	2,33E-10	4,66E-10	7,00E-10	9,33E-10
2,60E+01	1,75E-11	1,13E-11	9,61E-12	7,91E-12	2,60E+01	2,33E-10	4,66E-10	7,00E-10	9,33E-10
2,50E+01	1,68E-11	1,15E-11	9,71E-12	8,36E-12	2,50E+01	2,33E-10	4,66E-10	7,00E-10	9,33E-10
2,40E+01	1,70E-11	1,20E-11	1,03E-11	8,07E-12	2,40E+01	2,33E-10	4,66E-10	7,00E-10	9,33E-10
2,30E+01	1,74E-11	1,22E-11	9,89E-12	8,76E-12	2,30E+01	2,33E-10	4,66E-10	7,00E-10	9,33E-10

Figure 55. Example of device sheet for the model report with the model parameters, the curves used for the calculation and the theoretical result.

As a summary, the information of the huge device sets are used to generate the model an represented key parameters in a single report with intuitive graphics and all the data related. Additionally, a sheet with a geometry study is done with the different sized and model parameters distributions. Moreover, summary of all the devices parameters is shown in a dynamic table, **Figure 56A**. For quick detection of anomalies and to know better the parameters dispersion a gaussian distribution, a heat map position and size classification with box chart is done for each parameter, **Figure 56B**.



A)

Geometry Study									
Wtotal/L [m/]	Total	Kn [A/V²]	λ [V⁻¹]	θ [V⁻¹]	Roff [Ω]	Vth [V]	u_cox [A/V]	E_out [%]	
40	139	3,65E-09	1,04E-06	7,62E-08	6,21E+12	8,45E+00	1,42E-06	2,67E-02	
Deviation		78,03%	671,53%	251,54%	204,27%	129,58%	62,62%	195,67%	
80	139	4,15E-09	9,89E-07	5,62E-08	1,01E+13	6,90E+00	1,19E-06	1,61E-02	
Deviation		66,06%	796,92%	229,99%	230,02%	74,90%	65,00%	155,90%	
160	139	3,85E-09	1,79E-03	9,60E-08	8,98E+12	5,99E+00	1,02E-06	1,48E-02	
Deviation		68,68%	1174,28%	387,40%	245,27%	121,01%	78,62%	190,59%	
320	140	3,92E-09	3,18E-07	9,37E-08	3,52E+13	6,02E+00	9,33E-07	1,81E-02	
Deviation		62,75%	325,63%	314,67%	368,46%	78,67%	75,44%	248,99%	
640	139	4,41E-09	2,90E-07	9,89E-08	4,55E+13	6,22E+00	1,15E-06	1,60E-02	
Deviation		45,21%	350,63%	214,61%	491,51%	82,66%	56,83%	251,91%	

Device Summary											
Device ID	W [µm]	L [µm]	NF	Wtot [µm]	Kn [A/V²]	λ [V⁻¹]	θ [V⁻¹]	Roff [Ω]	Vth [V]	u_cox [A/V]	E_out [%]
Average	1,12E+02	4,00E+00	7,60E+00	9,92E+02	4,00E-09	3,57E-04	8,42E-08	2,12E+13	6,71E+00	1,14E-06	1,83E-02
0_0	8,00E+01	4,00E+00	2,00E+00	1,60E+02	3,16E-10	7,35E-08	8,26E-11	9,69E+07	2,99E+01	8,11E-07	1,11E-02
0_1	1,60E+02	4,00E+00	1,60E+01	2,56E+03	6,82E-09	2,56E-09	1,58E-13	1,66E+12	5,22E+00	2,13E-06	1,53E-02
0_2	1,60E+02	4,00E+00	8,00E+00	1,28E+03	7,00E-09	8,00E-08	6,54E-09	3,47E+12	4,14E+00	1,53E-06	1,27E-02
0_3	8,00E+01	4,00E+00	8,00E+00	6,40E+02	6,65E-09	4,92E-10	2,64E-08	3,18E+12	3,60E+00	1,13E-06	2,24E-02
0_4	8,00E+01	4,00E+00	4,00E+00	3,20E+02	6,49E-09	2,95E-10	1,65E-08	1,53E+12	3,54E+00	1,09E-06	1,90E-02

Figure 56. **A)** Geometry study with device relevant parameters table and **B)** example of parameter dispersion in gaussian distribution, heat map position and size classification with box chart.

With this final report, the automation from the characterization step to the model generation is completed allowing the fast development of proper models to obtain correct PDKs. Applying to the Data, Information, Knowledge and Wisdom (DIKW) hierarchy the first three steps had been automated successfully resting the final part, wisdom, where the circuit designer must use properly an EDA simulator together with the report generated in order to achieve the desired system behaviour.

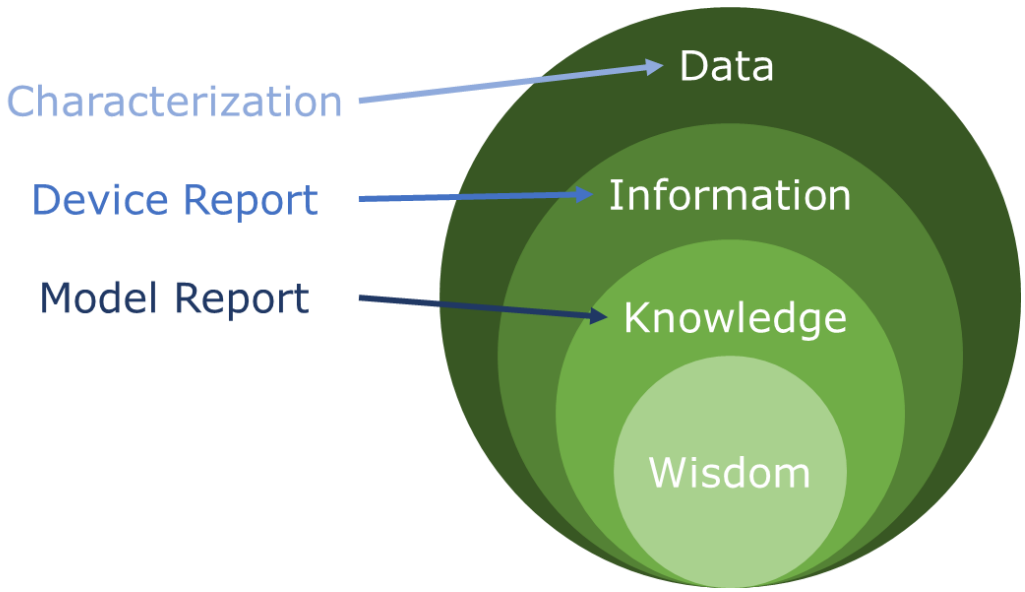


Figure 57. Data, information, knowledge, wisdom hierarchy and their correspondence with the automated work.

4.4 Diodes

Diodes are two terminal devices characterized by an asymmetric I-V behaviour. The terminals are called anode and cathode. Typically, the resistance in forward bias is negligible and in reverse bias condition is high. Diode can be realized using three types of interfaces based on p-n junction, the Schottky-Mott barrier formed at the Metal-Semiconductor (MS) interface, or Metal-Insulator-Semiconductor (MIS) devices.

During the stage at the KIT in Karlsruhe, Germany, a pn-diode manufactured with inkjet printing technique had been manufactured and modelled. Their fabrication with the modelling results had been published at [16].

The work is based on an inkjet printed pn-diode based only on oxide semiconductors. The n- and p-type films are based on Indium oxide (In_2O_3) and either Copper Oxide (CuO) or Nickel Oxide (NiO), respectively. It is the first of their class with an inkjet printed oxide pn-diodes. With the objective to enable circuit design, it was important to develop proper model and integrate them into a PDK.

Figure 58. **A)** Top and **B)** cross section view of a pn-diode based on oxide semiconductors [16].

Various diode models have been proposed, following a physics based modelling approach, while others are more focused on the terminal behavior of the device [17]–[20]. In this work, a mix of empirical and physical model is implemented for describing the pn-diode, allowing a straightforward implementation, suitable for printed electronics process design kits (PDK) and circuit simulation [21].

The physical parameters used for the model in terms of current density (J_D), are the saturation current density (J_S), the emission coefficient (η), the off-resistance in the reverse region (R_{OFF}), and the thermal voltage (V_{TH}), which is 25.4 mV at room temperature:

$$J_D = \begin{cases} J_S \left(\frac{V_D}{V_{TH}} \right)^{\eta} & V_D \leq 0 \\ \frac{V_D}{R_{OFF}} & V_D > 0 \end{cases} \quad (3)$$

As for the conventional pn-diode equation, the emission coefficient, extracted in this case, describes by how much the current curve deviates from an ideal pn-diode curve. The extraction of the off-resistance value is obtained by the division of the lowest voltage value by the current in that point. Saturation current and the emission coefficient are extracted by fitting the model of **Equation 3** to the measurements. Thereby a robust model with a quick and automatic extraction methodology implemented in a Matlab script is obtained.

Table 16. Extracted PN-Diode parameters

Parameter	CuO	NiO
R_{OFF} (kΩ)	1.4	1
J_S (μAcm^{-2})	38.4	1.6
V_{TH} (mV)	25.4	25.4
η	1.5	2.2

Table 16 summarizes the extracted parameters. By comparing the measured and simulated curves **Figure 59**, one can see that the simulated curve fits very well with the measured curve. Independent of the material stack, this model is able to model the behaviour of these novel pn-diodes.

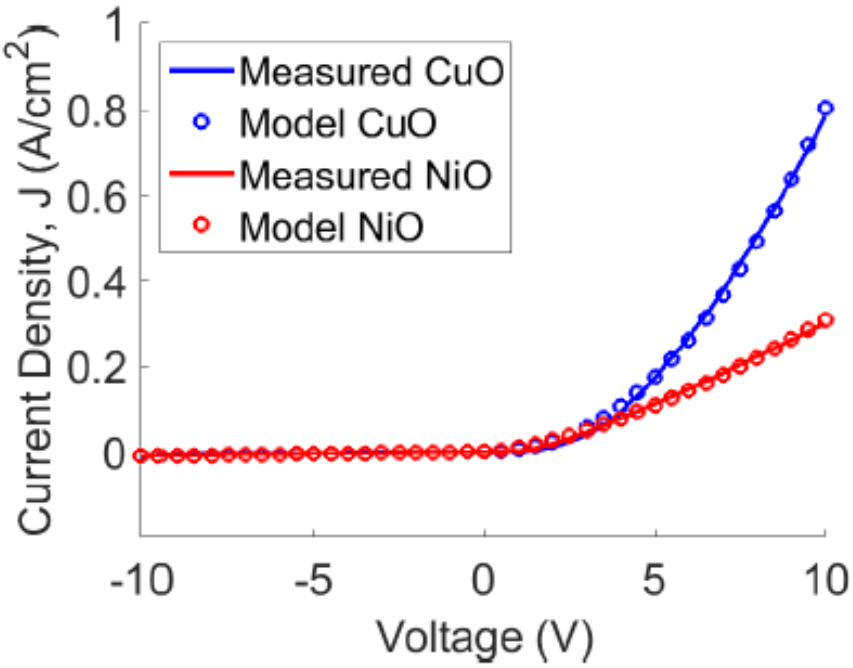


Figure 59. Comparison between the measured and simulated diode curve.

4.5 OTFT

OTFTs are three-terminal electronic devices based on an OSC layer, an insulating (dielectric) layer, and three electrodes: the source, drain and gate. The active OSC layer can be made of oligomers, polymers, or organic nanostructured materials that are deposited as thin films (few tens of nanometers thick) by, generally, solution casting, spin coating, sublimation, or printing techniques. Special characteristic of this device is that an electric field is established across a dielectric layer separating the gate electrode from the semiconductor layer. This electric field can manipulate the size and shape of a region of high conductivity in the semiconductor, and hence, modulate the current flowing through the device, creating a relation between gate voltage (V_G) and drain current (I_D). Basically, the thin film transistor operates like a capacitor. When a voltage is applied between source and gate, a charge is induced at the insulator-semiconductor interface. This charge forms a conducting channel which conductance is directly related to V_G.

OTFTs can be categorized into different topologies depending on the source, drain and gate contact positions. The first category is the bottom gate configuration where the gate of the transistor is below and the source and drain are located between the gate and the OSC (named Bottom Gate Bottom Contact - BGBC) or on top of the entire stack (named Bottom Gate Top Contact - BGTC). The second category is when the gate is placed on top of all the other layers and the position of the source and drain contacts are placed on the bottom of the structure (named Top Gate Bottom Contact - TGBC), or between the gate and the OSC (named Top Gate Top Contact - TGTC). All of the different topologies are depicted in **Figure 60**. Due to the large diversity of materials and techniques, each stack will be more suitable depending on the manufacturing technologies used and some constraints related to the materials.

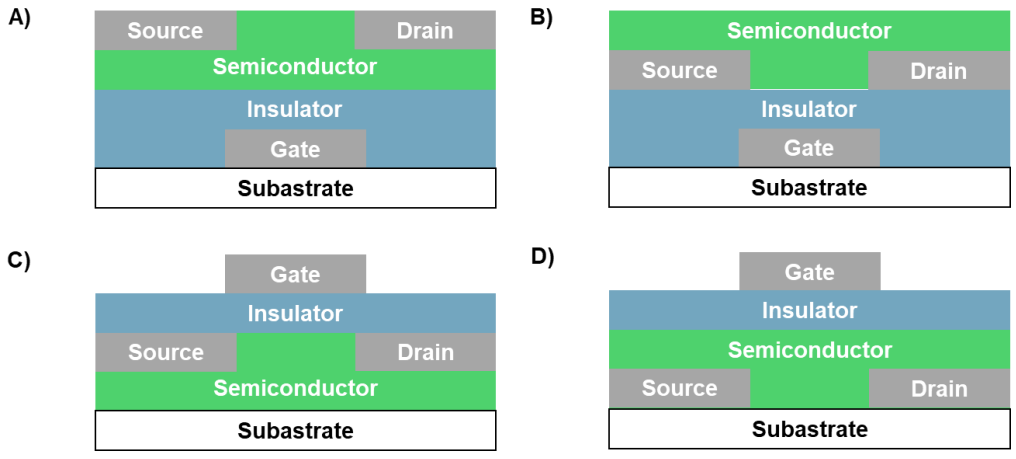


Figure 60. A) Bottom Gate Top Contact, **B)** Bottom Gate Bottom Contact, **C)** Top Gate Top Contact and **D)** Top Gate-Bottom Contact.

Additionally, different shapes of gate had been tested for various purposes. In **Figure 61** an optical image of single gate and circular OTFT is shown.

Interdigitated OTFT, the most common for circuit design, are designed with the drain and source contacts intercalated with the same distance, channel length, and a fixed width, finger width. The number of source or drain contacts determine the number of fingers that multiplied by the finger width provides the transistor width. Both terminals are covered with the gate to control the channel formation in the semiconductor between the drain and source. This type of transistor presents a high scalability since the increase of the geometric parameters give a good area efficiency.

Transistors with circular geometry, also known as Corbino, are not the common transistor type used in circuit designs, this gate shape is more usually used in the display field for opening or close a Light Emitting Diode (LED). Pads position in this transistor type are different than in the interdigitated ones. In the middle of the transistor is placed the source/drain of the transistor and the outside ring, is placed the complementary element of this symmetric structure, drain/source. In the space between them the gate is deposited to cover all the channel area. In this transistor topology the channel has ring shape. The width of the channel is determined by the perimeter of the circle and the length of the channel is the constant distance between source and drain terminals. The handicap of this type of transistor is the area efficiency, to achieve big widths a large area is required since the use of fingers is not an option [22].

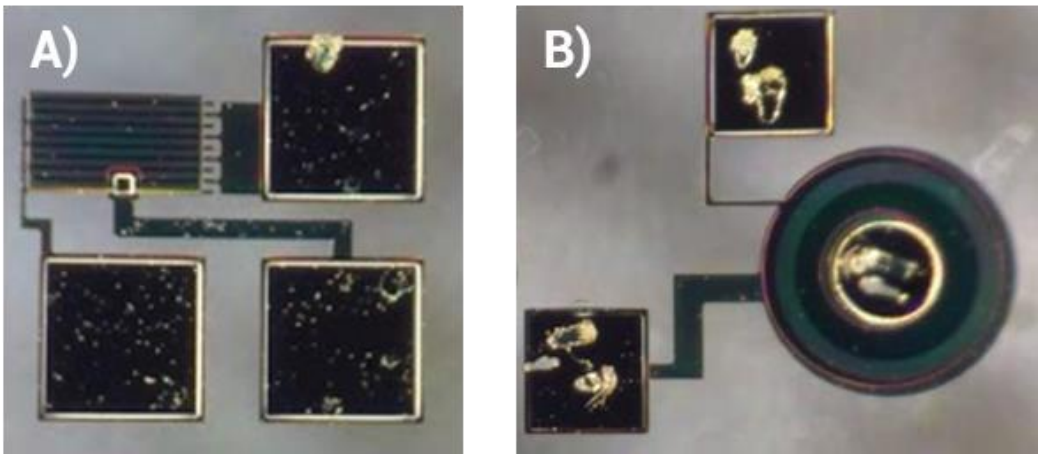


Figure 61. A) Single gate and B) Corbino OTFT.

Regarding number of gates, single gate transistors are the most conventional transistors, witch as explained previously the gate position can be on top or on the bottom of the stack. The advantages of this structure are simplest stack with less steps of the fabrication process and the well-known models present in the literature. As a handicap, in some organic semiconductors present an reverse threshold voltage, so the transistor with no potential at the gate, allows the current flow, between the drain a source electrodes [23]–[25].

Double gate transistors**, Figure 62A,** present the same options with the source and drain position than the single gate devices, but related to the gate, there is always a top and bottom gate. On the one hand, this topology increment the number of deposited layers, but it solves the problem of the open channel with 0 V at the gate, with the appropriate use of the back gate, [26]–[28].

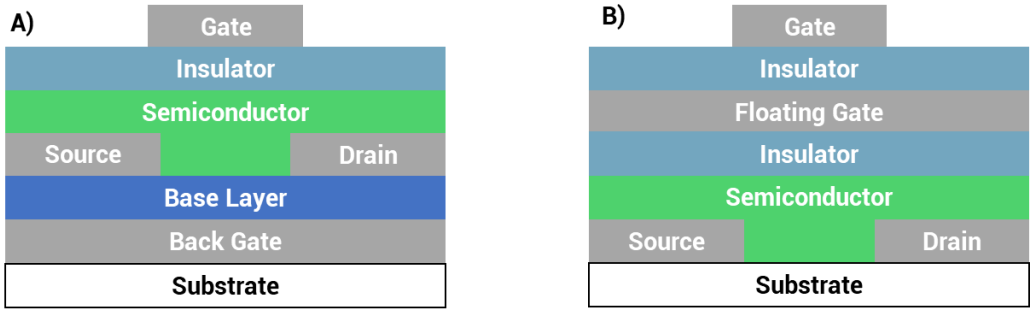


Figure 62. **A)** Dual gate and **B)** floating gate OTFT stack.

Floating gate, **Figure 62B**, allows same configurations as single gate transistor for the source and the drain terminals. It presents two gates, one on top of the other, and regarding position of both it can be in top or bottom location of the device stack, but both gates have to be placed together. The use of floating gate is useful for variation compensation [29].

Multiple electrical simulation models have been presented for organic p-type OTFTs in the literature [2], [3], [6], [30]. Despite of that, none of them is able to reproduce the behaviour of the devices fabricated by NeuDrive since the threshold voltage is located in positive potentials of the gate [31], reversing the usual behaviour shown by this type of devices. Moreover, the subthreshold region presents a non-ideal off-current not included in the conventional organic models. For this reason, the Shichman-Hodges Model [32], also known MOSFET Level 1, have been adapted to our device.

4.5.1 *Performance and key parameters*

Multiple parameters can be extracted for the different models to be implemented. As regards that fact, there is a group of parameters that are being used as benchmark to compare the different transistors [33]. The parameters are listed below:

- Operation voltage range
- Mobility
- On-Off ratio
- Threshold voltage

Operating voltage range is defined as the potentials needed/supported between the device terminals, this parameter is used to compare the different

devices, but each application will require one operating range or another, making some device more suitable to the final application than the others.

Mobility is one of the most used parameters for device comparison, since it implies that higher device mobility allows better device performance. Field effect mobility is the average charge carrier drift velocity per unit of electric field, and it measure of how easily the charge carriers can move inside the device. Mobility increases with larger channel lengths and active semiconductor layer thickness. To calculate the mobility from the transistor characteristic curves the transconductance, $\frac{\partial I_D}{\partial V_G}$, can be used in the linear region or the square root of the current respect the gate potential can be used in the saturation regime, $\frac{\partial \sqrt{I_D}}{\partial V_G}$. The mobility in terms of the device parameters can be described for the linear region as **Equation 4** or in the saturation region as **Equation 5**.

$$\mu_{lin} = \frac{L}{WCV_D}\left(\frac{\partial I_D}{\partial V_G}\right) \quad \textbf{(4)}$$

$$\mu_{sat} = \frac{L}{WC}\left(\frac{\partial \sqrt{I_D}}{\partial V_G}\right)^2 \quad \textbf{(5)}$$

On-Off ratio is defined as the division of the maximum current between the minimum current, showing the on and off states of the transistor. This parameter is crucial for digital circuits where higher on-off ratios allows to have more differentiated 0 or 1 states, increasing the robustness of the logic gates and consequently the final system. It depends on the threshold voltage and the subthreshold swing, in that the value of the threshold voltage determines where the off-current occurs, and the value of the subthreshold swing determines the rate at which the on-current is reached.

The threshold voltage of a transistor depends on the semiconductor used and the carrier traps that it has. Threshold voltages determines whether the channel in the semiconductor is formed or not depending on the terminals potentials, in this stage the gate capacitance is also involved. Multiple ways to extract the threshold voltage had been presented [34] and the most popular one is in the saturation region of the transfer curve.

4.5.2 *DC*

The devices used had been fabricated by NeuDrive at the Centre for Process Innovation (CPI, Sedgefield, UK) using the Gen2 photolithography facilities and following the process described at the layout generation section. The DC model generation methodology, was published in the proceedings of a conference [35].

Shichman-Hodges Level 1 model is a simple implementation with a mix of physical and empirical basis, providing good accuracy with low simulation time combined with greater tendency to converge than other models avoiding any discontinuity between or inside the device operating regions. The generated model allows an easy implementation in the modern EDA tools through Verilog-A language compilers. It is based in physical parameters (μ_{eff}, t_{ins}, C_{ins}, V_T, R_{off}) combined with mathematical extracted ones (λ, Φ).

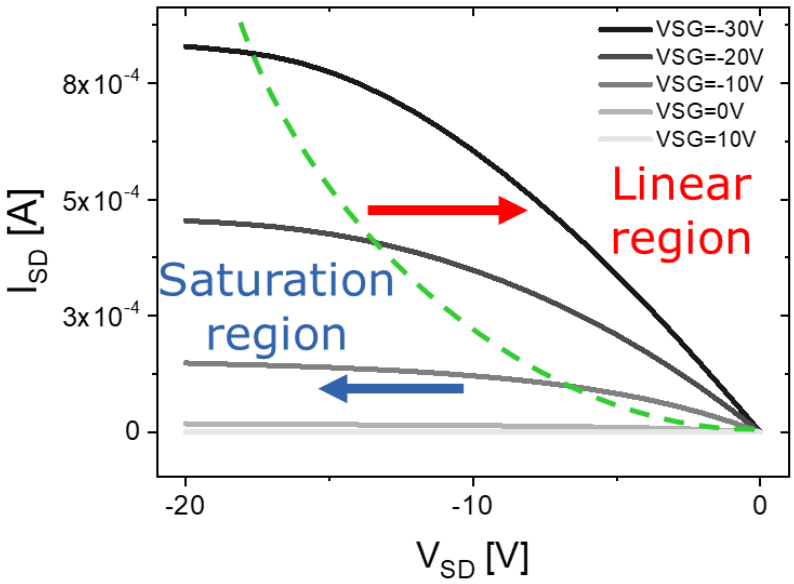


Figure 63. Regions of the Shichman-Hodges Model applied to output curve of an OTFT.

The model presents three regions, cutoff region represented by **Equation 6**, the linear region represented by **Equation 7** and the saturation region represented by **Equation 8**, the regions are also depicted in the **Figure 63**. The cutoff region is modelled by an off-resistance dependent of the source drain potential, being always valid if the threshold voltage is higher than the source gate potential. In the linear region, the current is flowing in a linear way with respect to the drain voltage through the device until the saturation region is reached, when the source drain potential is higher than the source gate plus the threshold voltage. At this point, the conducting path is saturated, and the current dependence of the drain path disappears remaining only the dependency of the gate potential.

$$I_{SD} = \frac{V_{SD}}{R_{OFF}} \tag{6}$$

$$I_{SD} = \frac{\mu_{eff} \cdot \frac{C_{ins}}{t_{ins}} \cdot \frac{W}{L} \cdot \left(V_{SG} + V_T - \frac{V_{SD}}{2}\right) \cdot V_{SD} \cdot \left(1 + \lambda \cdot V_{SD}\right)}{1 + \theta \cdot \left(V_{SG} + V_T\right)} + \frac{V_{SD}}{R_{OFF}} \tag{7}$$

$$I_{SD} = \frac{\frac{1}{2}\cdot\mu_{eff}\cdot\frac{C_{ins}}{t_{ins}}\cdot\frac{W}{L}\cdot\left(V_{SG}+V_T\right)^2\cdot\left(1+\lambda\cdot V_{SD}\right)}{1+\theta\cdot\left(V_{SG}+V_T\right)}+\frac{V_{SD}}{R_{OFF}} \quad (8)$$

The fabrication parameters C_{ins} and t_{ins} are related to the capacitance per unit area and the thickness of the insulator. Transistor mobility, μ_{eff}, is extracted from the maximum value of the derivate in the saturation region of the transfer curve while the threshold voltage, V_T, uses the square root derivative of the transfer curve to trace a tangent line from the maximum to find the interception with the gate voltage axis which value is the threshold voltage, this process can be seen in **Figure 64A**. The off resistance, R_{off}, is directly dependant in the source drain potential [36], see **Figure 64B**, the parameter extraction is done modelling the resistance in all the points of thee output curve and calculating the mean value. Channel length modulation, λ, and the surface inversion potential, Φ, are used as statistical values that are extracted using a neural network that learns from the OTFT data inputs for optimizing the model generated providing high accurate results with an automated methodology. The experimental data compared with the extracted model is depicted in **Figure 64C**.

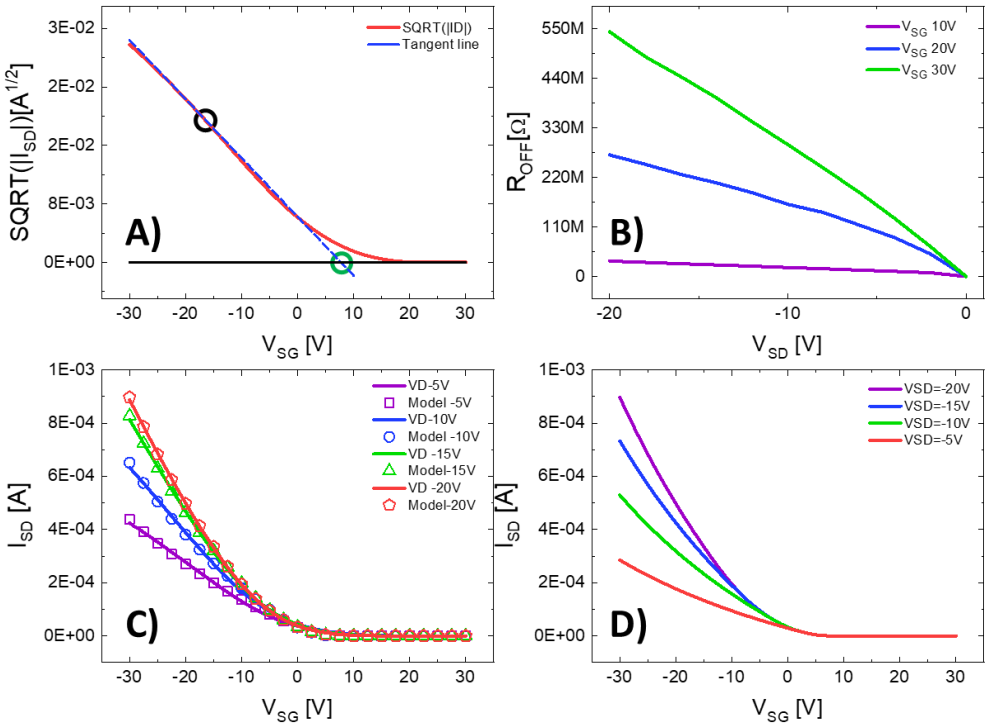


Figure 64. **A)** Mobility and threshold voltage extraction **B)** off resistance depending on drain and gate potentials **C)** transfer curves with the parameter extraction model **D)** simulation in Cadence of the Verilog-A model.

For the model parameters extraction, a Python script was inspired on neural networks theory, had been developed using the ISE method [37] to minimize the computational effort with the mathematical parameter fitting. Moreover, it is a useful guideline to compare the compact model generated, that provides a mean

accumulated error of 0.01% with respect to the measured data. Once the parameters are determined, another Python script automatically generates the Verilog-A model with the transistor variables extracted. The implementation and simulation of an OTFT can be seen in **Figure 64D**.

4.5.3 AC

This study of the AC behaviour of the OTFT and Corbino OTFT (CTFT) had been published in a journal [38].

AC models are unusual in the organic electronics technology since they require an extensive study of the device and their model implementation is more complex. Two different architectures of Organic Thin Film Transistors have been studied for the AC model development: 1) Interdigitated fingers for the source and drain terminals OTFT, and 2) CTFT [39] with a cylindrical shape (see **Figure 65A** and **Figure 65B**, respectively).

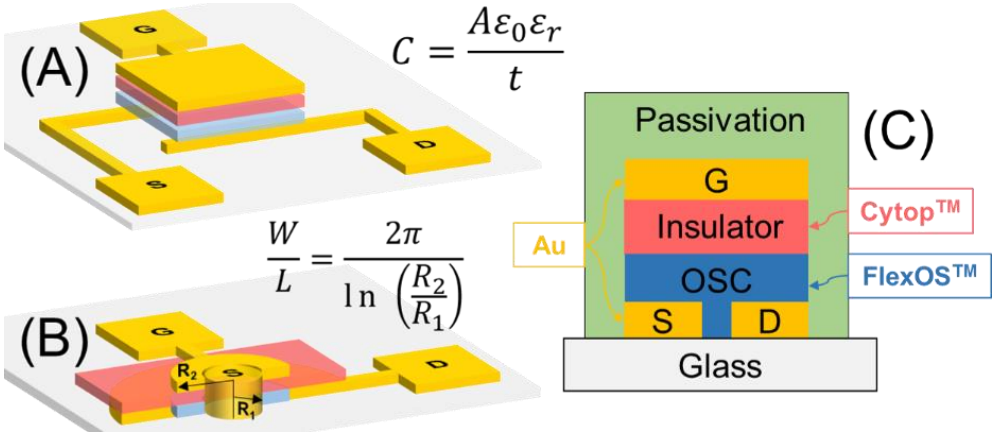


Figure 65. Architecture of the **A)** Interdigitated OTFT, and **B)** Corbino OTFT. **C)** OTFT Stack materials, common to both architectures.

The Interdigitated OTFTs processed by NeuDrive present the classical interdigitated geometry, where source and drain are interleaved behind the gate. This geometry allows easy scalability since different widths can be achieved by using multiple fingers. Two different interdigitated channel lengths were used, 10 µm and 4 µm. For the 10 µm length devices, two widths were studied: 980 µm and 9800 µm. For the 4 µm channel length devices, five widths were studied: 160, 320, 640, 1280 and 2560 µm using two different finger widths. For the Corbino OTFT, four different channel lengths (5, 10, 20 and 40 µm), combining three different external radiuses R_2 (105, 100 and 120 µm) with two internal radiuses R_1 (100 and 80 µm) [40].

I-V and C-V curves of the devices were measured with the Semiconductor Parameter Analyzer Keithley 4200, which allows large current and capacitance resolution measurements with high voltage biasing (±30 V). The frequency response of the Common-Source amplifiers built with the studied OTFTs was

determined by measuring the amplitude of the output voltage, when the frequency of the input signal was swept from 100 Hz to 1 MHz. General-purpose digital scope was used for the output signal measurement.

To evaluate the device performance, I-V characteristics and C-V curves were measured on the devices with different architectures and dimensions. **Figure 66** shows typical Drain Current – Gate Voltage (I_D-V_G) characteristics of all of them. As can be seen, subthreshold region is located at voltages above 0 V, implying that these devices (p-type transistors) are operating in depletion mode [41]. Off currents are of the order of pA in most of the cases, resulting in a low consumption when the device is off, **Figure 66**. Note that when the device is on, currents in the ~100 µA-1 mA range are achieved with mobilities between 1 to 1.75 $cm^2/V{\cdot}s$, under operating voltages around ±30 V [42]. These voltages are much larger than in CMOS technology (~0.8 V) [43], but usual in organic devices [31].

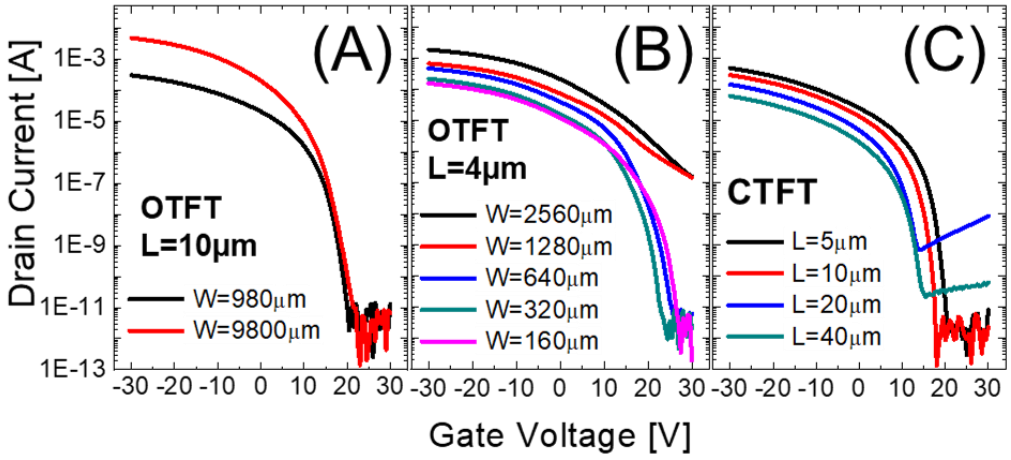


Figure 66. Drain Current–Gate Voltage characteristics measured on Interdigitated OTFT with **A)** L = 10 µm, **B)** L = 4 µm and **C)** Corbino OTFT

For the interdigitated OTFTs, I_D increased as expected, linearly with device width (**Figure 67A**). In contrast, for the Corbino architecture, an I_D reduction can be observed **Figure 67A**, because device width and length change with the radiuses as well (L = R_1-R_2). However, when representing I_D as a function of device aspect ratio, in both cases, Interdigitated and Corbino, was proportional to W/L, **Figure 67B**. To evaluate the dependence of V_T on the device area, as a criterium, V_T was defined as the gate voltage at which I_D = 10 µA. **Figure 67C** shows that V_T of Interdigitated devices grows linearly with the device width, while in the Corbino it decreases with channel length. Note that I_D and V_T follow the same geometry scaling dependence as MOS technologies [44].

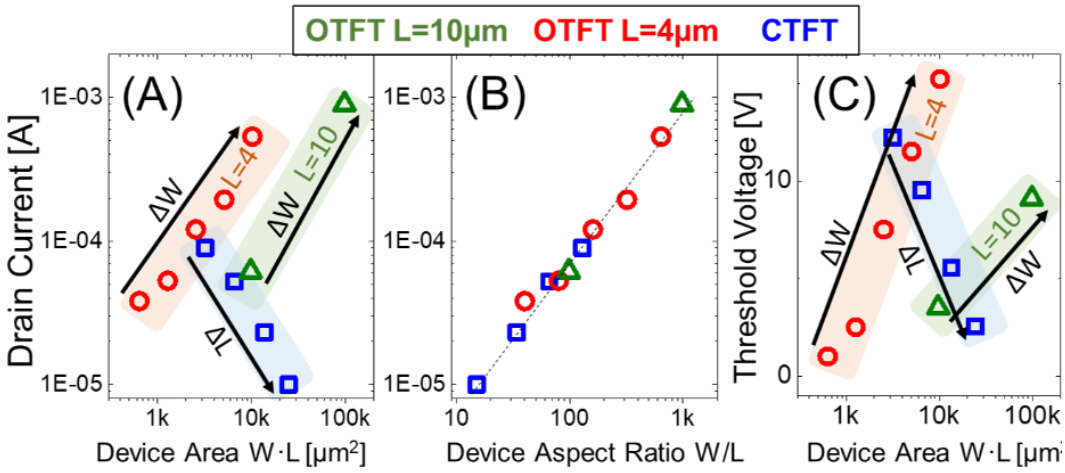


Figure 67. I_D as a function of **A)** the device area for OTFT and CTFT and **B)** as a function of the aspect ratio W/L. **C)** V_T as a function of device area.

The parasitic capacitances associated with the stack were also measured (C-V curves) in the same devices. The gate capacitance (C_{OX}) was measured when source and drain were grounded (similar values to those measured on MIM structures were obtained for the capacitances per unit area, $5{,}94 \cdot 10^{-5}$ F/m). C_{GD} and C_{GS} were also measured with the drain or source terminals grounded, respectively, while the other terminal was kept floating.

A strong dependence of the measured capacitance with the device area can be observed, **Figure 68**, for the two OTFTs architectures. The inset in **Figure 68A** shows that for negative polarities, the three capacitances (C_{OX}, C_{GS} and C_{GD}) are almost equal, indicating that the channel region acts as a bottom terminal of the stack when the device is ON (accumulation of p-type carriers). In the case of CTFT devices, capacitance increases with device area (i.e. channel length decreases) when applying positive bias (subthreshold region). This dependence is observed because, in that regime, the area of the capacitance depends only on the overlapping between the gate and drain-source electrodes. However, at negative bias, CTFT capacitance exhibits similar values for different areas, because the effective area under the gate terminal is the same due to the effect of the channel (i.e. gate metal electrode does not scale with device area). Therefore, their cylindrical architecture implies an L-independent gate area when the CTFT device is ON.

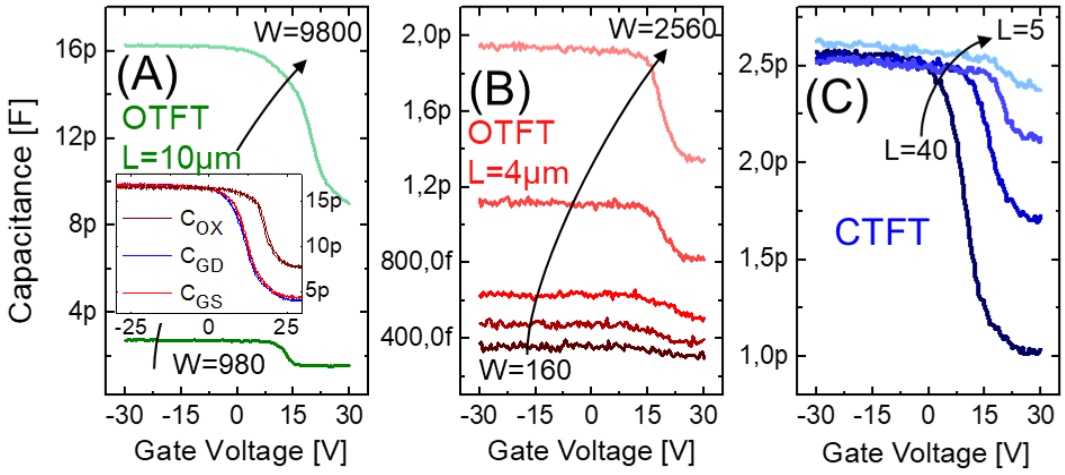


Figure 68. C-V characteristic of the Gate stack for the interdigitated OTFT with **A)** L=10µm, **B)** with L=4µm, and for **C)** Corbino OTFT. The inset in **A)** shows the area dependence of the three measured capacitances.

In order to evaluate the performance of the studied OTFT and CTFT, a Common Source (CS) amplifier was used [45], which allows easy correlation of device and circuit performances, because the amplifier's gain and cut-off frequency strongly depend on the transistor parameters [46]. This configuration is represented in **Figure 69A** and the corresponding small signal equivalent circuit in **Figure 69B**, where a MOSFET-like small-signal model is considered for the OTFT. Circuit analysis leads to a transfer function given by **Equation 9**, which shows that the CS circuit gain depends on the transconductance (g_m) and output resistance of the transistor (the last one included in R_{OUT}, which is defined as $R_{OUT}= r_0//R_D//R_{OSC}$). In addition, the cut-off frequency is determined by the parasitic Gate-Drain capacitance (C_{GD}), being independent of C_{GS}. These parameters can be extracted from |H(s)| measurements.

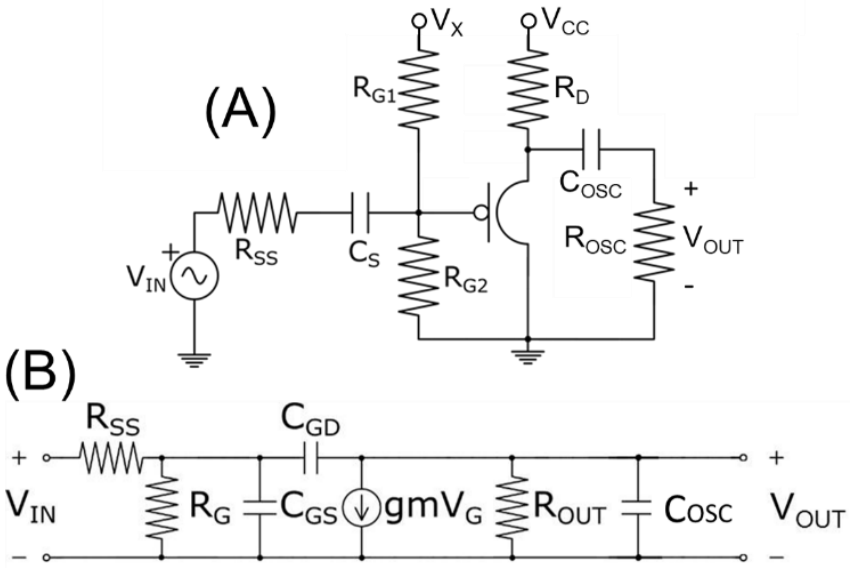


Figure 69. A) Common Source (CS) amplifier implemented to evaluate the OTFT performance in the frequency domain, and **B)** small signal model for mid and high frequency regims. $R_G=R_{G1}//R_{G2}$ and $R_{OUT}= r_0//R_D//R_{OSC}$.

$$H(S)=\frac{V_{OUT}(S)}{V_{IN}(S)}=\frac{R_{OUT}C_{GD}S-gmR_{OUT}}{S\left(C_{OSC}+C_{GD}\right)R_{OUT}+1} \quad \textbf{(9)}$$

In our experiments, the value of R_{SS} (the output resistance of our input source), R_{G1}, R_{G2}, C_S, R_{OSC} and C_{OSC} (being the last one the input impedance of our scope) and the DC voltage supply, V_{CC}, were fixed. It must be emphasized that, in these experiments several parameters change from experiment to experiment (i.e. when a different device area or geometry are used, different voltages at device terminals are registered), thus direct comparisons are meaningless. Moreover, circuit values such as R_D or V_x were selected in order to maximize the gain. Consequently, to account for the differences in the OTFTs, R_D values could vary between 340 kΩ and 1 MΩ. V_{GS} and V_{DS} DC values were registered before extracting the frequency response, to assure the transistor operating point. A frequency sweep of the input signal was performed from 100 Hz to 1 MHz. Only the mid and high frequency regimes were analysed, since low frequency response is mainly given by the circuit parameters.

Figure 70 shows the magnitude of the frequency responses of the CS amplifiers built with the different Organic transistors, measured (lines) and their fitting to **Equation 9** (circles). As observed, the gain increases with the device width and in the best case it is ~6 dB. The cut-off frequency also increases with the device width. In addition, the effect of the transmission zero (given by C_{GD}) in **Equation 9** is clearly observed in the 100 kHz-1 MHz interval.

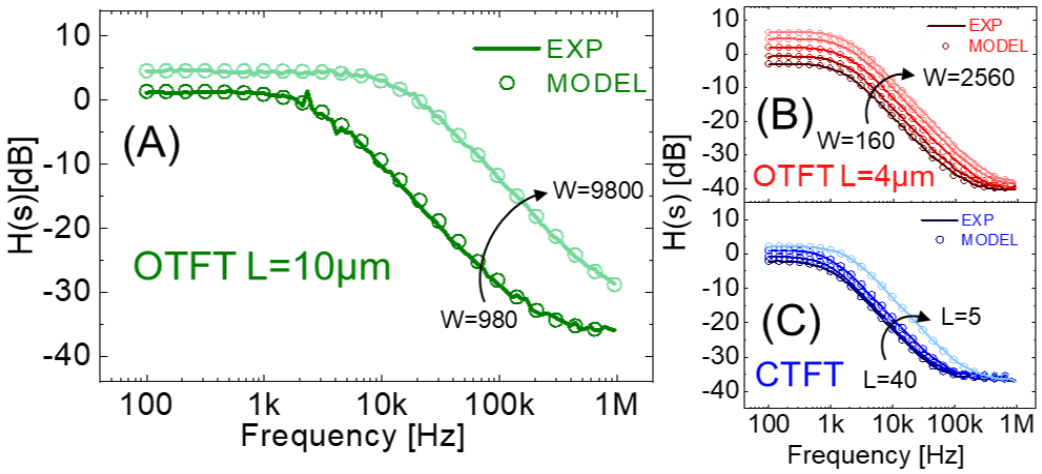


Figure 70. A) Experimental (lines) and fitted (circles) frequency response for the Interdigitated OTFT with L = 10 µm, **B)** Interdigitated OTFT with L = 4 µm and **C)** Corbino OTFT.

The device parameters obtained from the fitting of the experimental data in **Figure 70** to **Equation 9** are depicted in **Figure 71**. **Figure 71A** shows the parasitic capacitance between gate and drain terminals (C_{GD}) as a function of the device aspect ratio obtained analytically (considering that for negative voltages

C_{GD}=C_{OX}, as shown in the inset in **Figure 68A** (squares), from the experimental C-V curve (circles) and from the fitting of the amplifier frequency response to the **Equation 9** (triangles). Similar values of C_{GD} are obtained for the different topologies and areas for the three extraction methods. The r_0 and g_m parameters are depicted in **Figure 71B**. A large dependence of these parameters with the channel dimensions can be observed in both OTFT architectures, being less significant in the case of CTFT due to their complex device width and length radius-dependence. As observed, for the Interdigitated OTFT, g_m increases and r_0 decreases linearly with device area. Inversely, for the CTFT, g_m decreases and r_0 increases non-linearly with device area, which means larger separation between radiuses (i.e. L increase).

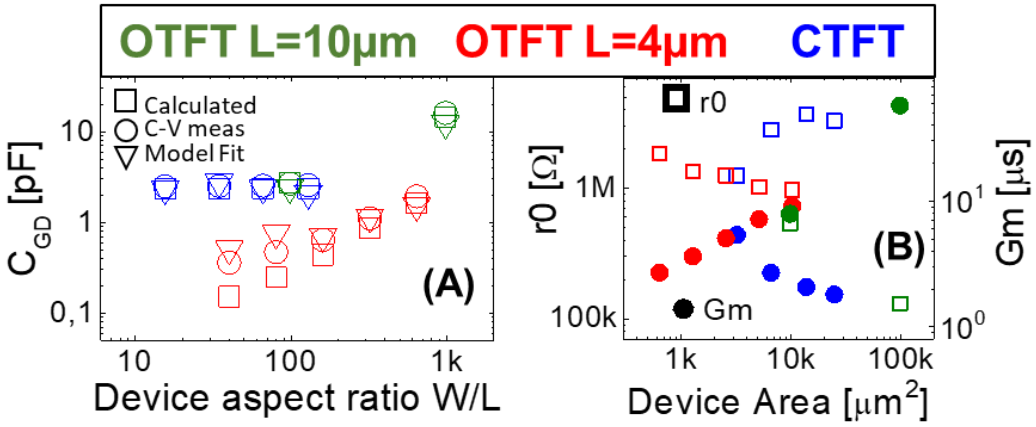


Figure 71. A) Analytically calculated Gate-Drain capacitance (squares), measured from the C-V curves (circles) and obtained from the data fitting (triangles). **B)** r_0 (empty squares) and g_m (circles) obtained from the fitting.

The results show that the extracted small signal model parameters (g_m, r_0, and C_{GD}) depend on the device dimensions and materials properties. A linear dependence of r_0, g_m and C_{GD} with device width was observed in the Interdigitated OTFT. In the case of the Corbino devices, C_{GD} did not depend on the device widths or lengths (i.e. radiuses), since there was the same effective area under the gate electrode for negative biasing. Furthermore, g_m and r_0 presented a non-linear area dependence, due to the relation between width and length in the CTFT. Therefore, circuit performance was strongly driven by device dimensions, as for MOS devices, despite the large voltages applied.

Using the extracted AC parameters, the Verilog-A model have been adapted to allow the simulation in the transient domain. The inclusion of parameters is performed by means of the capacitance C_{GD} multiplied with the derivative of the potentials in the different device terminals. The use of intrinsic nodes in the Verilog-A module provides robustness to the model, making convergence in the simulations easier to achieve. **Figure 72A** shows a fabricated two-input NAND gate working at 10 kHz, where 10 V is considered “0” and -10 V “1”. The output signal presents tree different levels but two of them can be considered “1” while

when output reach 0V is treated as a “0”. **Figure 72B** shows the circuit simulation of the same circuit by using the AC signal model previously described.

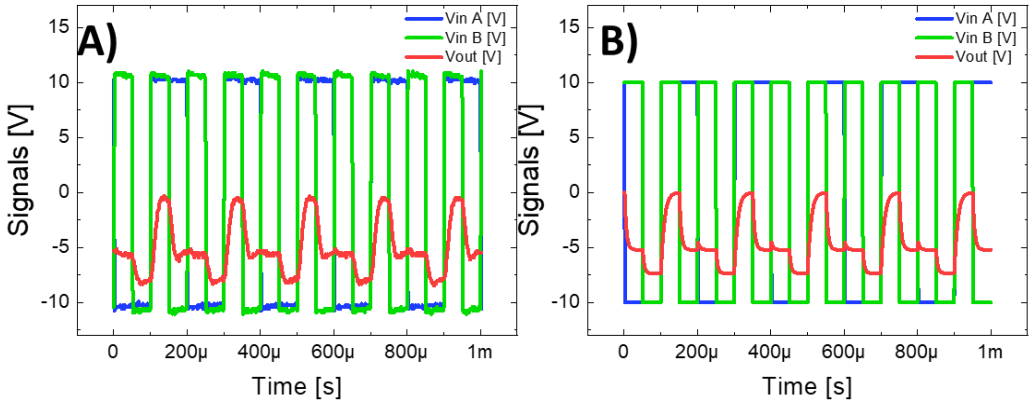


Figure 72. Input and output signals of a NAND2 gate at 10kHz **A)** experimental data **B)** circuit simulation by using our AC signal model.

4.5.4 *Parameter variability*

With respect to the theoretical model working principle, most of the organic and printed devices present high variability in their behaviour from the nominal characteristics. This variability is caused by two main factors: process-induced or time-zero variability and degradation due to ambient effects.

4.5.4.1 *Compensation methods of process variation*

Variability in process fabrication is a well-known problem in silicon technology, where multiple compensation techniques have been developed [47]. Process-induced variability is also present in the OE field, where different fabrication techniques require custom compensation techniques. For inkjet printing, Sowade et al. [48], Vila et al. [49] and Ramon et al [100] have conducted extensive studies on failure automatic detection and compensation techniques in the geometric design and pattern design to improve the yield and to reduce the parameter variability; an example is shown in **Figure 73**. All this work was developed during the TDK4PE project, developing a DRC based on statistical data extracted from large arrays of devices [50] and delimiting multiple geometry parameters in the numerous materials used with patterns to optimize their performance. Conductivity in metal lines over a set of more than 10.000 devices using different dimensions and drop spacing was reported allowing the definition of design rules. Furthermore. multiple patterns were analysed in order to apply compensation techniques to improve device printing. Finally, using a semi-automated characterization system, electrical characterization was performed on a large set of transistors, in order to identify the different failure origins such as

short-circuits, open-circuits, high leakage currents, no field effect modulation or atypical transfer curve [51].

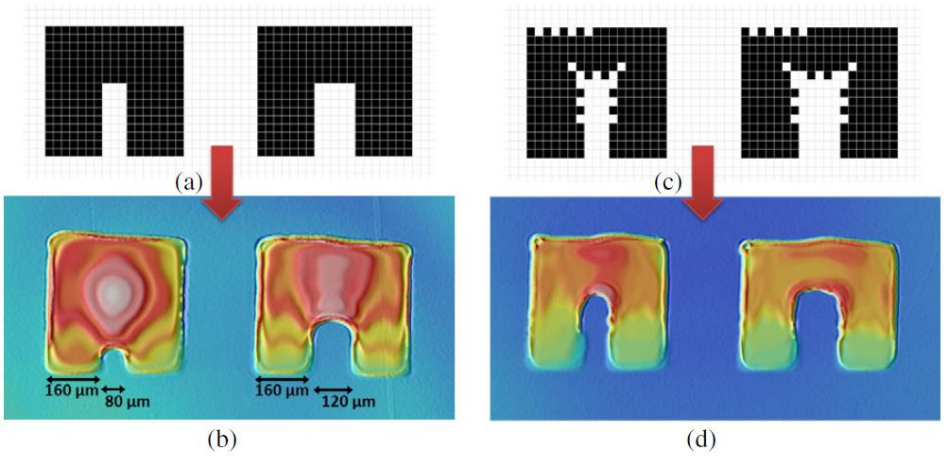


Figure 73. A) Non-compensated notch pattern; **B)** 3D image of the deposited non-compensated pattern; **C)** PSC compensated notch pattern; and **D)** 3D image for PSC compensated notch rule [52].

KIT [53] proposed a reliability-ware routing solution for additive manufacturing circuits using a genetic algorithm, allowing the printing of more reliable circuits. The script is based on defining different costs to the path, crossover and pad of the circuit and with these attributes, multiple versions are created following the genetic algorithm and the optimum one is used.

From the Technical University of Munich [54], an algorithm was developed where the device is divided in confined areas and the code determines the order of printing the geometries to reduce fabrication problems and obtain the best printing results. With this methodology, the obtained yield increased from 10% to 81% using the same number of layers.

Heinrichsdobler et al. [55] also studied inkjet printing compensation techniques in order to reduce pinhole probability by three orders of magnitude and also suggest a droplet patterning mechanism that could reduce the pinholes by an additional 50%.

For the roll to roll technique, Kang et al. [56] proposed a compensation method to cancel out the disturbance of the machine directional register in the downstream span providing an over-shot by more than 58% compared with the conventional fabrication technique, as shown in **Figure 74**.

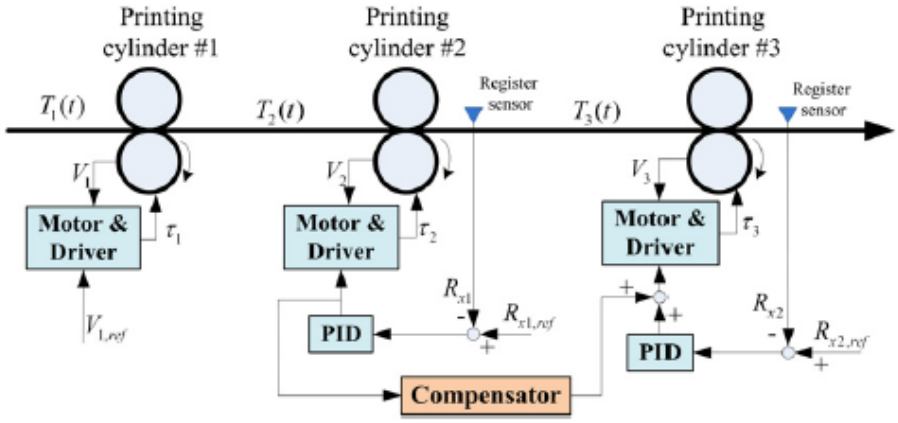


Figure 74. Schematic of the three-layer direct gravure printing system [56].

In the photolithographic process, Ji et al. [57] used a double exposure method in the fabrication of flexible OTFTs and circuits to obtain better performance than the conventional fabrication method.

4.5.4.2 *Thermal issues*

When talking about organic devices, it is important to bear in mind the degradability of these materials, for the benefits and handicaps it implies. The first issue, and one of the most challenging, is the temperature effect. In practice, all charge transport theories are based on temperature as a key factor in charge transport, and different studies can be found in the literature showing the device dependence on this parameter.

Jung et al. made an extensive study of OTFTs [58] for a wide range of temperatures from 273 K to 453 K. They reported that in the range between 273 K and 333 K, the current increases with the temperature linearly, but above these values the relation with the temperature is reversed, thus achieving a saturation point showing a maximum of the semiconductor mobility at 333 K.

Liang et al. [59] studied the application of different temperatures on an OTFT used as a non-volatile memory for a range between 223 K and 423 K. The devices presented a lower on/off ratio when the lowest temperatures were applied and for high temperature a higher current ratio, see **Figure 75**. Regarding the threshold voltage of the OTFT, it presents a non-lineal behaviour with the temperature increasing from the lower temperatures until 323 K where it reaches its maximum value and then decreases with lower slope than in the previous range.

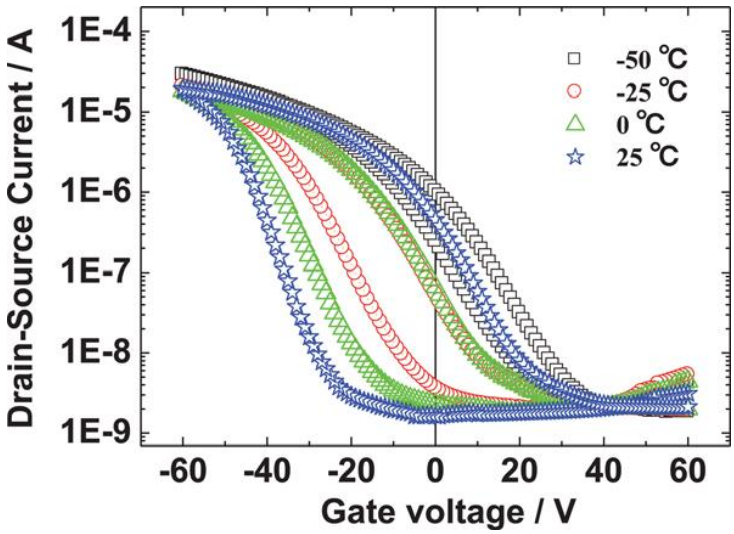


Figure 75. Transfer characteristics of the OTFT device with PMLG as the ferroelectric layer at different temperatures [59].

Li et al. [60] studied their devices between 200 K and 300 K and developed a model for the semiconductor mobility that incorporates the relation between the temperature, the gate voltage and the conduction on the device.

Other studies such as the one from Chesterfield et al. [61] also studied the temperature dependence on OTFTs. They focused in the relation between the temperature and the current in the semiconductor for n-channel OTFT on the range of 100 K to 300 K. Their results show that higher temperatures allow higher currents. This relation was linear in all the range of temperatures. Additionally, a mobility model was developed in order to explain the dependency of the device with temperature.

Lee et al. at [62], did a study in which the findings were based on the temperature applied to the substrate where the semiconductor was deposited. The resulting OTFTs revealed different performance depending on substrate temperature. For the lower temperatures, the devices had higher on/off current ratio with lower mobility, while for higher temperatures, the transistors had a higher threshold voltage and more elevated saturation current. The origin of this effect is related to the grain size of the deposited layer that increases with the temperature. Bigger grain sizes generate higher density of traps and thus lower on/off ratios.

Soltman et al. [63] also published a work related to the fabrication temperature. They focused on inkjet printing technology and the specific non-idealities of that technique, and how to mitigate them, applying different temperatures with a combination of the parameters of the printer as the drop spacing and the delay of drop ejection, see **Figure 76**. These two last examples reveal the effect of printing strategies on device performance.

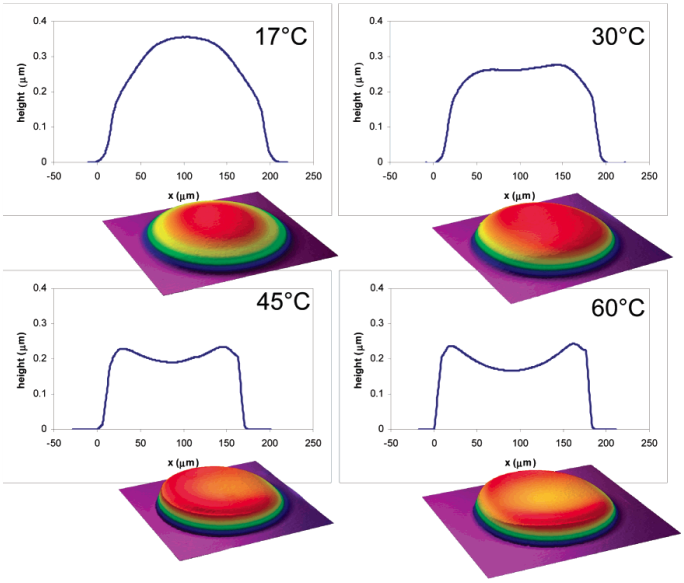


Figure 76. Cross section and 3D projection from an optical profilometer of single drops printed at the noted temperatures [63].

4.5.4.3 *Humidity issues*

Another ambient parameter affecting device performance and stability is humidity. Cadilha et al. [64] studied the humidity dependence of their devices and circuits, showing an optimum operation at 60% of humidity and non-functioning in extreme humidity conditions, moreover they analysed the evolution of their model parameters through all the measured range.

With different materials, Zafar et al. [65] tested their OTFT as a humidity sensor obtaining a current variation of 29,4 times with humidity increasing from 40% to 80% with a high increase from 70% to 80%, showing high dependence of the PEDOT:PSS used as active layer.

Li et al. [66] studied the degradation caused by humidity when using different organic semiconductors such as pentacene, C6TFT and C12FTTF in devices fabricated with different topologies and dimensions. They found the best performance with the lower ambient humidity, having losses in performance of 90% in the worst case.

4.5.4.4 *Light issues*

The effect of light in organic semiconductor devices is well-known. Groups such as Noh et al. [67], showed the increase of the off current of organic devices under illumination due the photons absorbed by the semiconductors.

Wrachien et al. [68], also studied the effects of light, bias and temperature on organic devices. Their results show an increase of hole trapping or electron neutralization when devices are illuminated while biasing the device. This induces

a high charge trapping while temperature releases the traps, as shown in **Figure 77**.

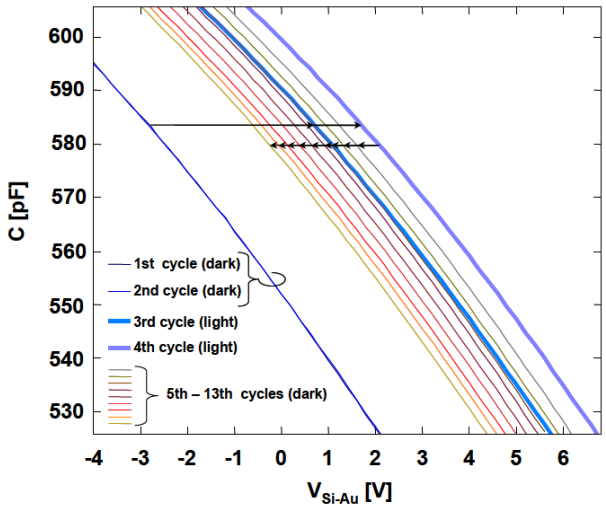


Figure 77. C-Vs with negligible changes under dark 1st and 2nd cycle. Strong variation occurs, if the C-Vs are performed under illumination 3rd and 4th cycles, and progressively move to negative voltages when in dark again 5-13 cycles. [68]

4.5.4.5 *Aging*

Device degradation over time is also a key effect in organic devices. Pannemann et al. [69] monitored the evolution of their devices over 9 months in ambient air conditions where the mobility was reduced over 3 orders of magnitude, while the on-current decreased more than 1 order of magnitude in the same period of time.

Using a shorter period, Saito et al. [70] characterized over 9 days, p- and n-type devices demonstrating a loss of mobility higher in the n-type devices than in the p-type ones. This change of mobility affected mainly the device on-current, that in p-type devices was reduced by 60% and the n-type ones achieved a loss of more than 75%.

Meijer et al. [71] and Ullah et al. [72] performed a study about the Meyer-Neldel Rule (MNR), where it is stated that the mobility prefactor increases exponentially with the activation energy. With their studies, they report that the MNR is directly linked to the charge transport mechanism affecting the current flowing across the device; the more temperature the higher current.

Ruiz et al. [73], had studied organic devices under bias stress by using Kelvin Probe Force Microscopy measures, providing useful information at the device level showing at nano-scale the damage of the different materials/regions in the device.

Za'aba and Taylor [74], shown a detailed study of bias stress in OTFT in different situations of humidity and temperature. The devices present shift in the

threshold voltage when the devices is under stress and a relaxation of first order when the stress is opposite. Their devices had shown a direct threshold voltage dependence with the humidity and inverted with temperature.

These studies underline the importance of taking into account the variability of the devices in the simulation step, either by intrinsic effects of the materials, manufacturing techniques or external ambient effects. The percentages of variation on important electrical parameters of the devices reveal that variability effects need to be taken into account applying techniques such as Monte Carlo simulations in order to predict the robustness of the circuits designed. Moreover, most of the presented works stress the need for device encapsulation in order to reduce the material dependence of ambient factors, achieving more stable devices and circuits.

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5 Device Simulation

The circuit simulation provides the device behaviour through the implemented model in the schematic designed, allowing to predict how will work a circuit that have not been fabricated. Use of simulations allows developing a higher level of understanding about the operation of the system. Circuit simulation is based on compact models that allows to use of computational power to resolve mathematical equations and obtain the simulations results, corroborating that the systems accomplish the behaviour expected and optimizing multiple device parameters for better system performance [1]–[6].

For circuit simulation purpose, Verilog-A description language is used to build the compact analog model in an understandable way for the simulator software. Cadence is the simulator tool chosen, since the open software alternatives are not good enough at this time as they are not easy to use and does not have all the capabilities of the licensed software used. Based on their Verilog compiler and the Virtuoso analog design environment combined with the ADE explorer, the generation of circuit schematic, simulation and results analysis of the electronic systems designed can be done with accurate results.

Pure mathematical models, also known as BB models, have been implemented and evaluated with not acceptable behaviour, regards they are very accurate, simulation convergence is a big issue. Moreover, because they are based in mathematical equations, they only model the performance of the fitted curve for a specific voltage range, not providing good results outside the characterization data used in the model generation step.

Verilog is a standard of the IEEE used to describe electronics devices and systems. It allows the description of digital circuits at register level. From this standard appeared later the extension AMS that allows the definition of mixed

and analog circuits. Verilog-A supports the description of digital and analog devices giving a more versatile tool to the designer, moreover the use of only mathematical models is possible.

The components used in the language are constructed using nodes and branches. A node is a point where the endpoints of branches may connect, and a branch is a single path between two nodes. With this two parameters Kirchhoff laws are applied, and the electrical parameters calculated.

Using nodes, branches and mathematical expressions, models can be defined compiled and simulated. **Figure 78** presents the Resistance, Inductance and Capacitance (RLC) series behaviour and an example code.


```
module series_rlc (t1, t2);

electrical t1, t2;

parameter real r=1;

parameter real l=1;

parameter real c=1 exclude 0;

analog begin

  V(t1,t2) <+ r*I(t1,t2);

  V(t1,t2) <+ l*ddt(I(t1,t2));

  V(t1,t2) <+ idt(I(t1,t2))/c;

end

endmodule
```

Figure 78. RLC series description in Verilog-A.

Cadence is one of the most important EDA tools, used for the most complex designs [7]. The suite box provides different programs that allows the design of full-custom integrated circuits, schematics, behavioural modelling (Verilog-A), circuit simulation and layout design. Using this tool, the model can be computed in the defined schematic and the circuit output can be represented. Moreover, the defined models in Verilog-A can have the parameters modified as the designer wants in the schematic or the simulation panel.

With a defined model in Verilog, a symbol can be generated and used in the schematic view. Ports and their distribution are configured with the symbol generator of Virtuoso software.

As introduced in the State of the Art section, multiple devices and different circuits had been simulated in the OE field, in this section the focus will be done around the industrial model developed in this thesis with the different ambient parameters affecting to the device and the circuit and the fabrication variability of the devices. Moreover, robust design techniques are studied and exposed.

5.1 Device variability study

The p-type OTFTs fabricated using the Gen2 photolithography line by NeuDrive Ltd (UK) [8] at the Centre for Process Innovation (CPI, Sedgefield, United Kingdom UK) [9] were employed for developing the compact industrial simulation model. The device fabrication uses different manufacturing processes such as spin-coating, UV light curing, hard-baking, metal sputtering, photolithography patterning, plasma treating, and thermally-evaporated metals and wet etching was utilized [10]. It is worth mentioning that the OTFT devices were manufactured in various W/L aspect ratios and present a common architecture based on a top gate bottom contact structure, as shown in **Figure 79** along with its optical image.

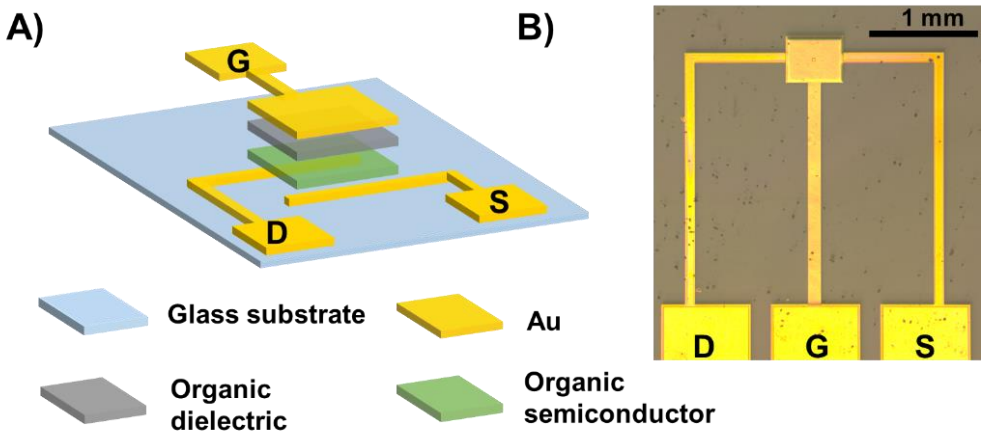


Figure 79. **A)** 3D scheme of the Interdigitated geometry and **B)** its optical image. D, G and S refer to Drain, Gate and Source electrodes, respectively.

The devices were electrically characterized by applying a wide range of potentials in the three electrodes as is required by the model extraction methodology, performing a wide range of values for the gate or drain voltages applying gate potential from -30 V to 30 V and drain voltages between 0 V and -20 V. Owing to the large data generated from the automatic characterization setup, a multitude of statistics in terms of OTFT key parameters were collected and analysed. In particular, on voltage (referred as V_{ON}) was obtained from the

intercept of the maximum slope in the transfer curve represented in logarithmic scale with the V_G axis. Threshold voltage (V_{th}) was extracted from the maximum slope of the square root of the transfer current and V_G-axis intercept. Based on the maximum slope value of the transfer current, the hole mobility (μ) was obtained from isolating the transconductance (g_M) from device capacitance. On/off current ratio (Ion/Ioff) was acquired from maximum and minimum drain current at a drain voltage of -15 V. Finally, maximum gate current was obtained from the transfer characteristics at -15 V of drain potential. The effect of the W/L parameter on the electrical parameters is represented in **Figure 80** using box charts for the different sizes. All the different parameters present a linear tendency to increment with the device size with more or less proportionately, although some sizes were out of the tendency for a few parameters, such as the device with W/L dimensions of 2560/4 for the V_{ON} or the Ion/Ioff ratio, and the device with W/L dimensions of 160/4 in the maximum current gate. These exceptions can occur when some transistors that are not fully functional are not correctly dismissed by the system of thresholds implemented to avoid the defective devices. The OTFTs show a normally on behaviour since they present a conducting channel when the gate voltage is 0 V since the threshold voltage is reversed from the usual transistor p-type behaviour.

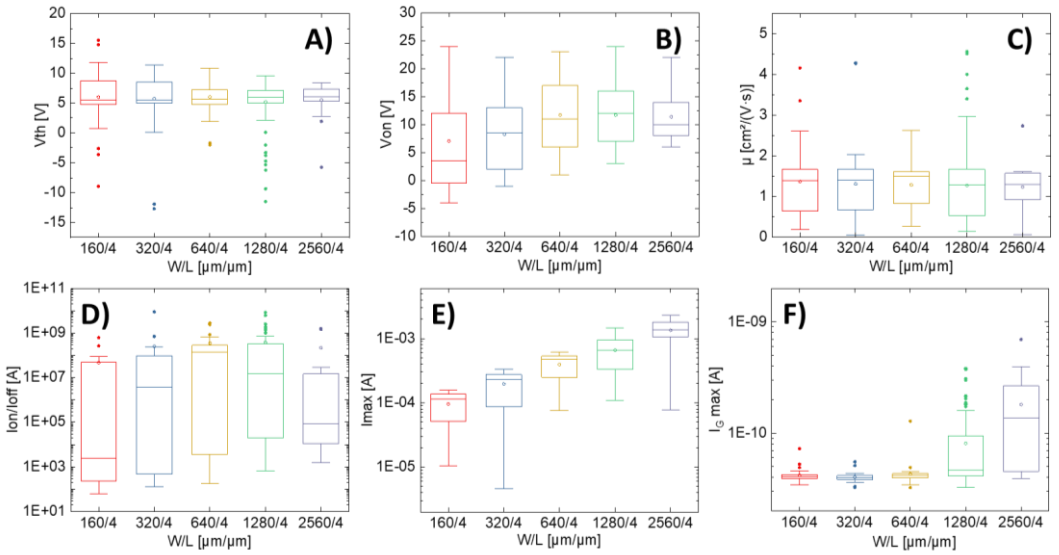


Figure 80. Parameters distribution of different dimensions devices **A)** Threshold voltage, **B)** On voltage, **C)** mobility **D)** Ion/Ioff, **E)** Maximum drain current and **F)** Maximum gate current. The central mark represents the median, box limits indicate the 25th and 75th percentiles, and whiskers extend to the 5th and 9th percentiles.

The parameters obtained from the normalization of the device current by their area are shown in **Figure 81**. Threshold voltage (**Figure 81A**), on voltage (**Figure 81B**) and, maximum current (**Figure 81E**) show a population more centred, i.e. less dispersion of the values, than the mobility, Ion/Ioff and, maximum gate current, whose dispersion is in the range of their mean.

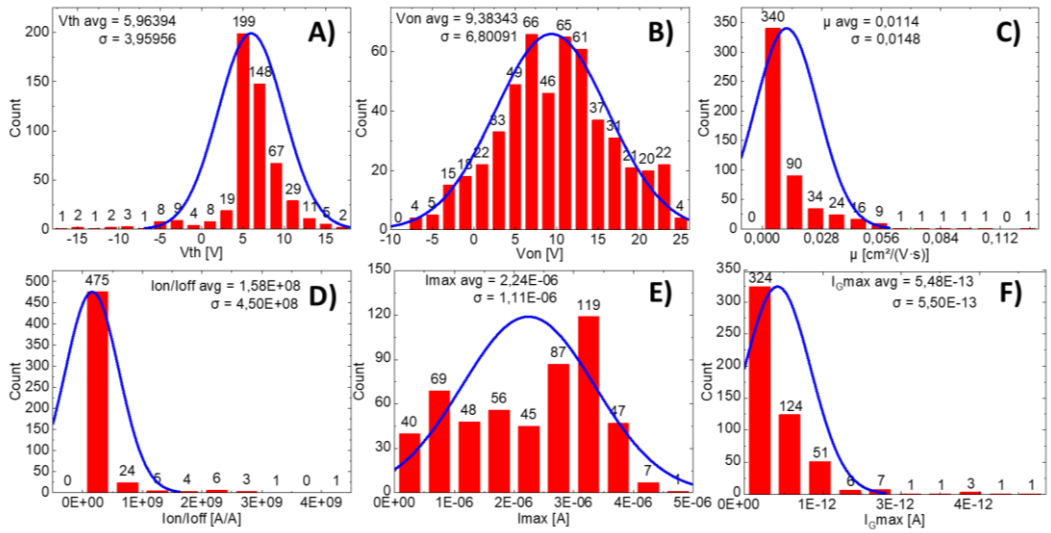


Figure 81. Parameters distribution of normalized device **A)** Threshold voltage, **B)** On voltage, **C)** mobility **D)** Ion/Ioff, **E)** Maximum drain current and **F)** Maximum gate current.

Furthermore, external factors such as humidity, temperature and light were assessed, as shown in **Figure 82A**, **Figure 82B** and, **Figure 82C**-**D**, respectively. The exposure of the OTFTs to various Relative Humidity (RH) from 20% to 80% resulted in a negligible effect for the I_{DS} while in the increment in gate current did not produce an irreversible breakdown. Humidity is an external parameter that needs to be taken into account as demonstrated by the influence of this parameter on device performance reported in other works [11]. The influence of temperature was assessed in the range of 0ºC to 60ºC, resulting in a small threshold voltage shift to more negative values combined with bigger on current and higher mobility when devices were exposed to lower temperatures. The opposite occurred for high temperatures where the gate current increased slightly. Since the protective top layer is transparent, significant differences are expected when the organic semiconductor is illuminated. The light induced produced an increase in the I_{DS} and the gate current and, a shift of the Vth to positive voltage upon irradiation.

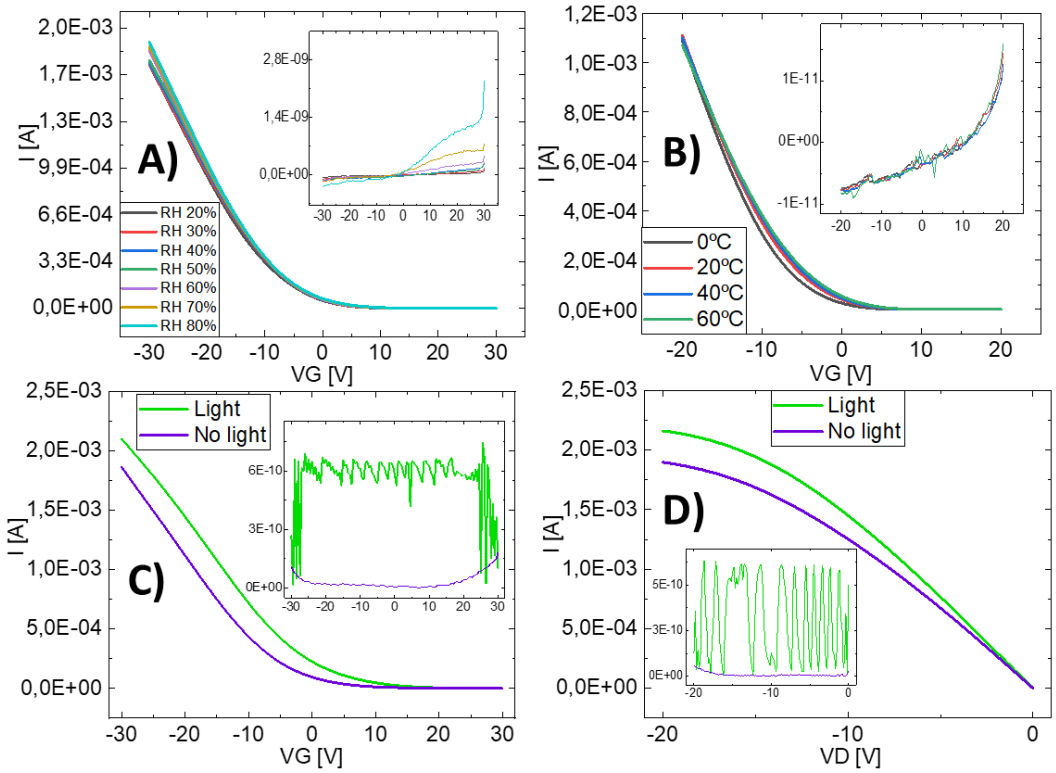


Figure 82. **A)** Relative humidity comparison V_D = -20 V, **B)** Temperature measurement comparison VD = -15 V, **C)** Transfer curve comparison under light or no light V_D = -20 V and **D)** Output curve comparison under light or no light V_G = -30 V, all measures of the same device dimensions with L = 4 µm and total W = 2560 µm.

The significant reliability of the OTFTs against bias-stress is demonstrated in **Figure 83A** and **Figure 83B**, where the transfer characteristics showed a near-perfect overlapping. Taking into account this good reliability in consecutive measurements, the aging-effect was studied by depositing the devices for one month in a transparent case without controlled atmosphere, i.e. 70-50% RH and temperatures from 15ºC to 25ºC. During this period, the devices did not show a clear tendency of degradation in terms of electrical parameters. Thus, the disparity behaviour in terms of I_{DS} could be attributed to the intrinsic features of the organic semiconductor, such as charge traps rather than external factors. This inconsistent behaviour in time can be seen in **Figure 83C** and output **Figure 83D**.

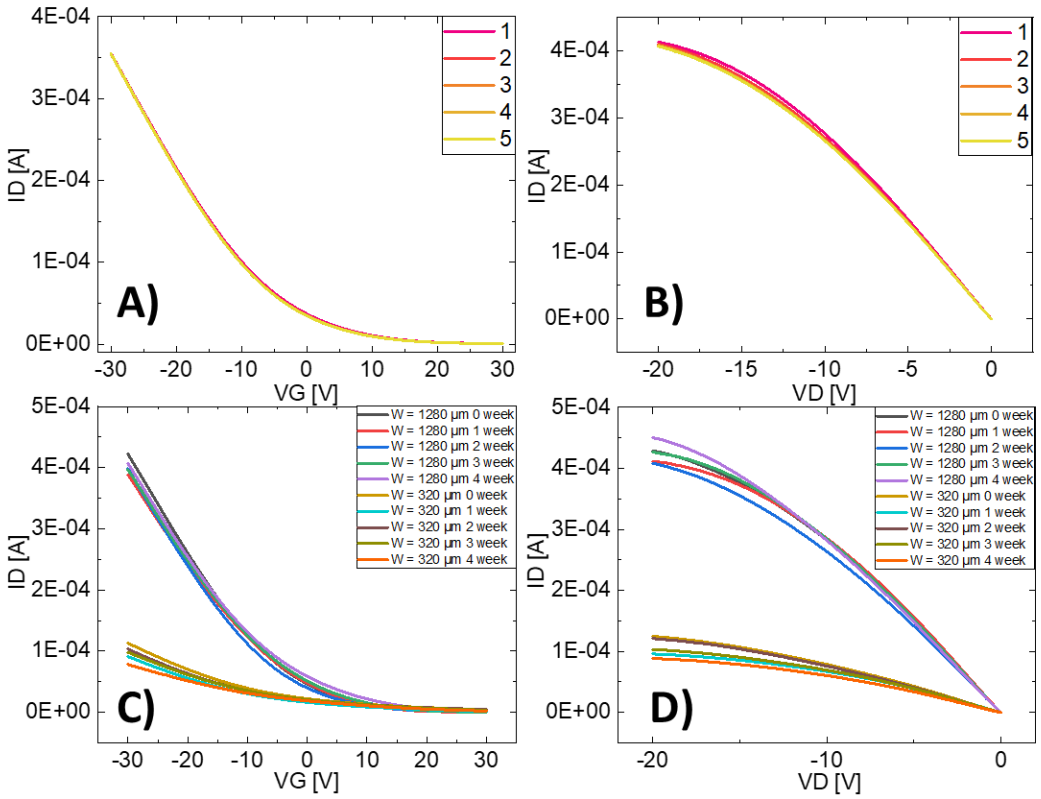


Figure 83. **A)** Repetitive Transfer curve W = 1280 µm and V_D = -15 V, **B)** Repetitive Output curve W = 1280 µm and V_G = -30 V, **C)** Historic Transfer curve V_D = -20 V and **D)** Historical output curve V_G = -30 V.

Parameter variations were also observed when the OTFTs were integrated in a circuit. The inverter circuit was configured through two p-type OTFTs where the top device acts a switch with the input voltage at the gate potential, and the bottom transistor was biased as resistor by connecting its gate terminal to the output of the circuit. **Figure 84A** shows the robustness of the inverter to multiple bias-stress for two different devices with a size ratio between the top and the bottom OTFTs of 2.7 and 0.5, respectively. Here again, the light exposure was also carried out. The results clearly show an influence in the threshold voltage reducing the gain from 6 to 4 and, shifting the transition point to more positive voltages as shown in **Figure 84B**.

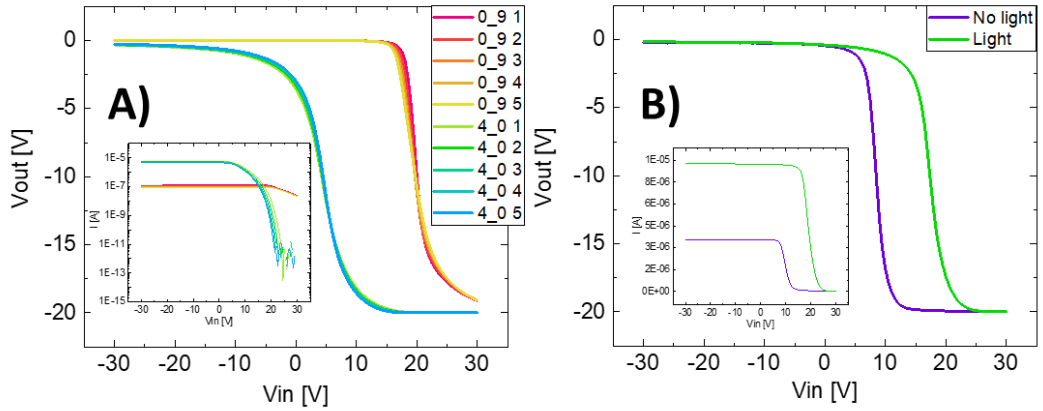


Figure 84. **A)** Inverter repetitive measure comparison with an inset of the current behaviour and **B)** Light influence on an inverter circuit with an inset of the current behaviour with a size ratio of 5,4.

5.1.1 *Model Parameter Variability*

A key point for a proper implementation of the compact model to industrial levels is the Monte Carlo simulation, since it facilitates the analysis of the best and worst cases allowing reliable designs without any failure in the system behaviour. Monte Carlo simulations use the model parameters statistical distribution to calculate all the feasible resulting systems. With this objective, a Python script collects the data of the characterized devices and calculates the model following the same procedure in the aforementioned sections. A report with the distribution of the model parameters is generated, allowing the implementation of the simulation into different scenarios.

Almost 700 devices were characterized and modelled with the automatic procedure developed. The distribution of the model parameters can be seen in **Figure 85**. Threshold voltage is shown in **Figure 85A** and *Kn* in **Figure 85E**, presenting a coefficient variation lower than one. **Figure 85B** shows theta values, **Figure 85C** depicts off resistance and **Figure 85D** shows lambda with a standard deviation higher than the mean value. Regarding the distribution of the parameters, **Figure 85F** shows a small standard deviation in relative error.

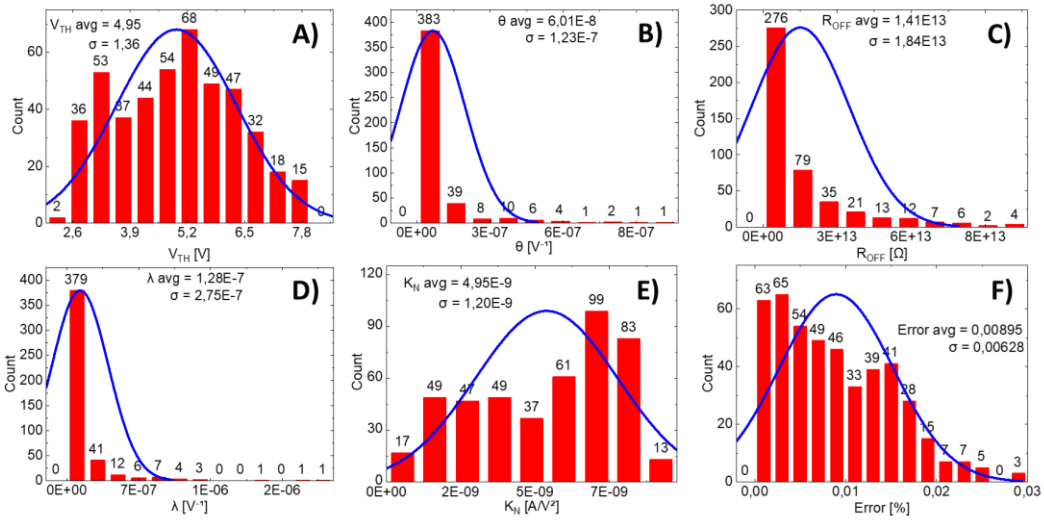


Figure 85. Parameters distribution of modelled device **A)** Threshold voltage, **B)** theta, **C)** off resistance **D)** lambda, **E)** Kn as the product of the device capacitance with the mobility and **F)** Relative error in respect of the experimental data.

Device performance can be also affected by its location on the foil due to inherent manufacturing variability. The spatial distributions are shown in **Figure 86A** and the same data normalized to the device ratio in **Figure 86B**. From the heat map, a clear tendency arises showing higher performances along edge sides compared with those placed in the middle of the wafer. This result shows a dependence of the electrical parameters as function of their location.

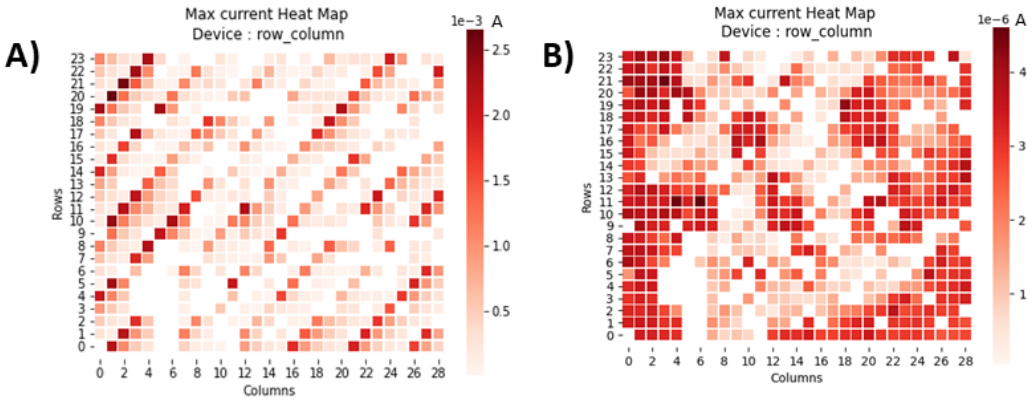


Figure 86. **A)** Spatial distribution of max current and **B)** normalized spatial distribution of max current.

Pelgrom's law has been widely used for the in-wafer variability analysis in silicon technology [12], [13], while only a few studies have been carried out in the organic electronics field [14]. This law states that the variance of the threshold voltage, the current factor and the substrate factor are inversely proportional to the transistor area [15].

$$\sigma(V_{th}) = \frac{A_{Vth}}{\sqrt{WL}}$$
$$\frac{\sigma(\beta)}{\bar{\beta}} = \frac{A_{\beta}}{\sqrt{WL}} \quad \textbf{(10)}$$

Equation 10 describes the dependence of closely spaced devices making the assumption that the long-correlation distance variations are negligible for the threshold voltage and the current factor. The equation uses both standard deviations (σ) and, the average current factor ($\bar{\beta}$) obtaining a mean proportionality constant of 203,16 Vμm for A_{Vth} and 26,58 %μm for A_{β}, extracted from **Figure 87**. Regarding the high value of the proportionality constants, the data reveals that the mismatch between two identically adjacent OTFTs reduces inversely with the gate area, exactly as Pelgrom's law predicts for local variations.

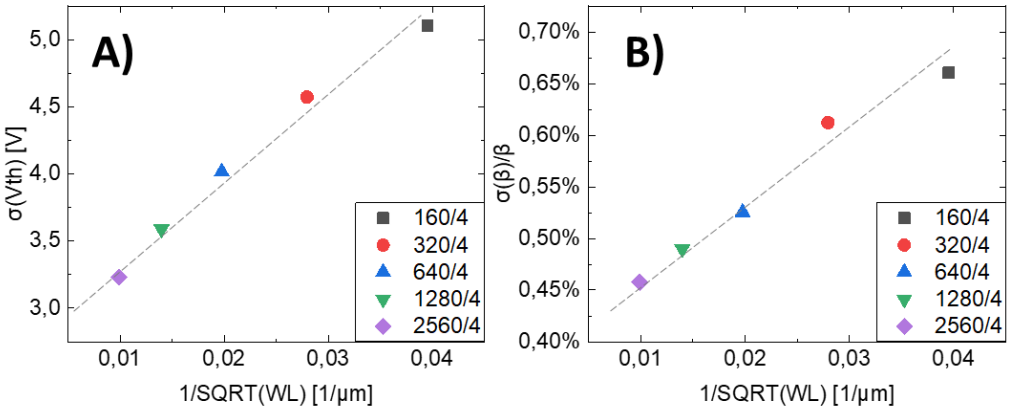


Figure 87. **A)** Threshold voltage deviation and **B)** current factor deviation versus the square root of the inverse transistor area.

5.2 Circuit simulation

Using Cadence Virtuoso, adapting the model and generating the required auxiliar file for variability, up to 500 Monte Carlo simulations were performed for the transistor, inverter circuit and NAND2 gate in order to obtain the best and the worst cases in each circuit. For parameter variation, an auxiliary variable was created and added to the model parameter. The auxiliary variable was used in the variability file that generated a Gaussian distribution with null mean and standard deviation from the graphs, as depicted in **Figure 85**. For the sake of simplicity, the best device ratio was not taken into account and as a result, all the transistors considered presented the same dimensions with a channel width of 2560 μm and a length of 4 μm.

Using the extracted AC parameters, the Verilog-A model was adapted to allow the simulation in the transient domain. The inclusion of parameters was

performed by means of the capacitance C_{GD} multiplied with the derivative of the potentials in the different device terminals. The use of intrinsic nodes in the Verilog-A module provides robustness to the model, making convergence easier to achieve in the simulations. A further step was carried out in order to validate the model in logical gates. **Figure 88A** shows a two-input NAND gate working at 10 kHz, where 10 V is considered "0" and -10 V "1". The output signal presents three different levels but two of them can be considered "1" while the 0 V is treated as a "0". **Figure 88B** shows the circuit simulation of the same circuit by using the AC signal model previously described. As can be observed, the model perfectly fits the electrical response of the logical gates.

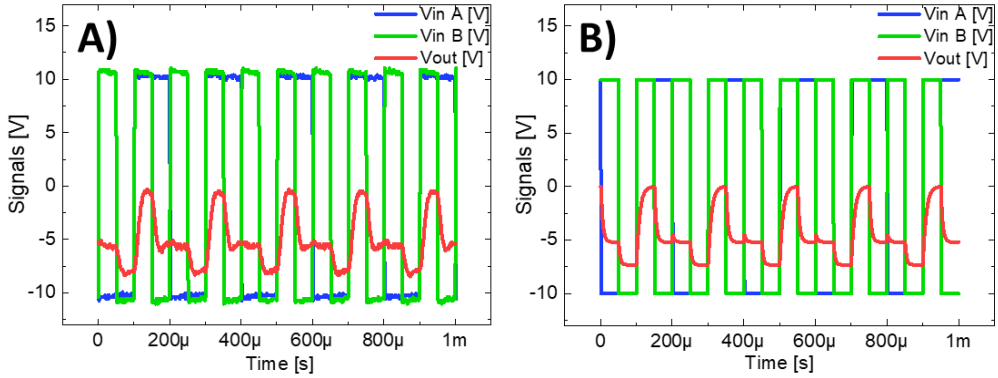


Figure 88. Input and output signals of a NAND2 gate at 10kHz **A)** experimental data **B)** circuit simulation by using our AC signal model.

Three different schematics were simulated in Cadence in order to validate the industrial model generated with the parameter variability file. 500 Monte Carlo simulations were performed for a single transistor (**Figure 89A**) with a V_D voltage of -20 V, an inverter circuit (**Figure 89B**) with two different supply voltages, and a NAND gate (**Figure 89C**) with two different supply voltages. The single transistor simulation allowed to confirm the proper implementation of the model. The inverter circuit simulation allowed to validate the DC behaviour, and finally the transient simulation of the NAND gate allowed the understanding of the device AC behaviour. For the different Monte Carlo simulations the mean of the simulations has been extracted and highlighted for clarification. Moreover, all the simulations provided a yield of 100% while providing two differentiated voltage levels in the digital behaviours.

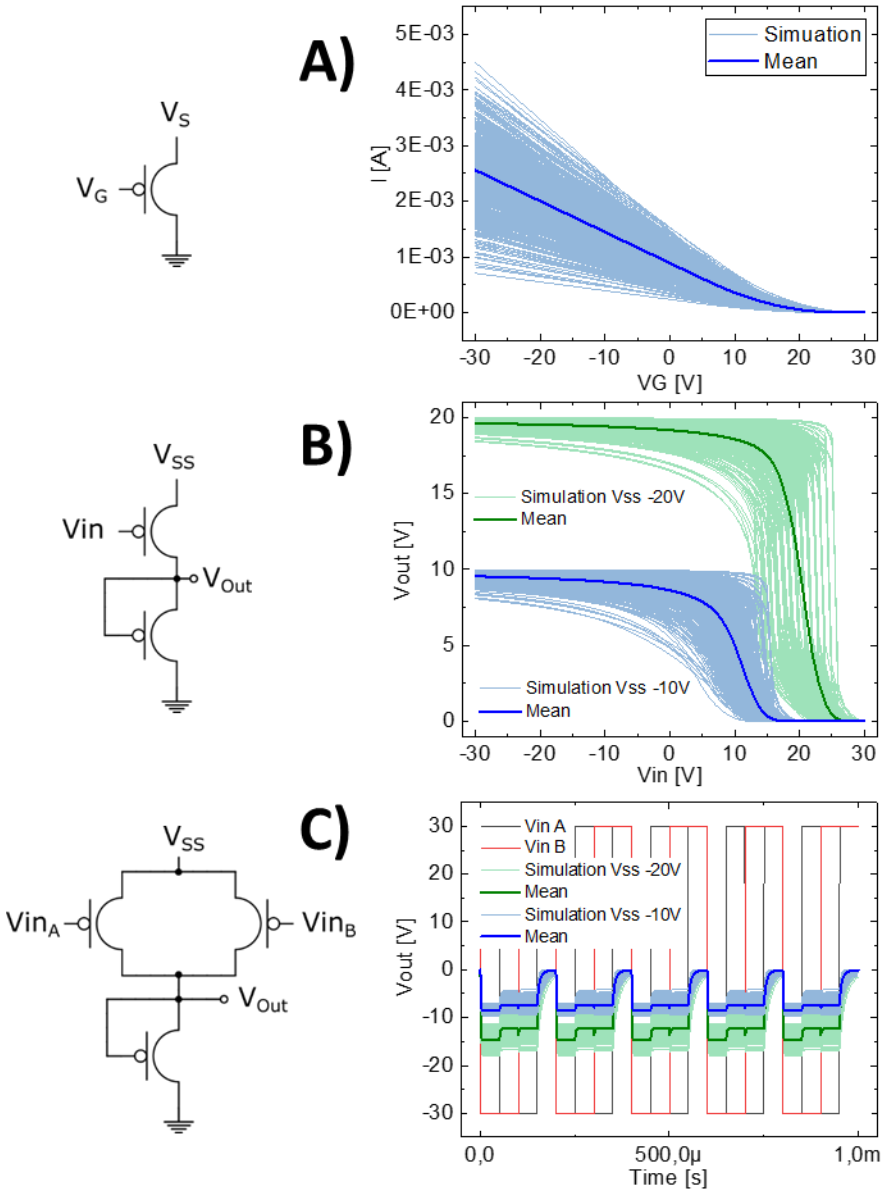


Figure 89. Circuit schematics and 500 Monte Carlo simulations for OTFT **A)**, inverter circuit **B)**, and NAND gate **C)**.

5.3 Robust design

A very well-known issue regarding OE devices is the device variability when using the same fabrication technique [14] or with different transistor architectures [16] where the mobility in the same transistor geometry can vary by almost 29%.

Different methodologies have been studied in order to mitigate the variability or reduce the nonidealities in the device that impact to the final systems. These include structures like Dual-Gate devices [3], [17]–[19], Electrolyte-Gated OTFT (EGOTFT) [20]–[25], pseudo CMOS configuration [26]–[29], coil or round shaped

electrodes [30], [31], Floating-Gate [32]–[35], dual threshold voltage devices [10], [36], [37] and also the combination of EGOTFT with dual threshold response [38]. Furthermore, special designs that allow the interconnection of the devices in post-fabrication system configuration have been proposed: inkjet-configurable arrays [39], programmable logic circuits [40] or the user-customizable logic paper with sea-of-transmission-gates [41]. Regarding fabrication techniques, different studies have been made on the differences between materials and material processing parameters for screen printing [42]. A similar study was performed on dual gate transistors and different organic semiconductors, p- and n-channel types [43]. One of the open issues is the hysteresis of the OTFT and in this regard, few studies with different materials have been published in the literature [44].

In respect of improvements of device characteristics, the Source-Gated Transistors (SGT) [45] configuration demonstrated the development of better performance devices based on silicon technology. The same approach was applied in organic devices with promising results [46], offering a lower voltage operation range than others while using the same materials.

5.3.1 *Inspection*

In order to obtain a mature product to sell and distribute to the costumers, the inspection section is mandatory. In the electronic industry two main types of inspections are done, optical and electrical.

Optical test is very popular in the organic and printed electronic fields, since it provides a detailed information about the problem in the device. Different works had been presented, [47]–[49], on the basis of capturing images of the system, using different techniques, and base on automatic image detection scripts, the defects are highlighted and reported in order to improve the manufacturing step.

Regarding the electrical performance test, it requires of more specialized hardware and instrumentation to be performed and few works had been done regarding devices, [14], and circuits [50].

At the TDK4PE both methodologies had been implemented for error detection [51], [52] and compensation with different pattern fabrication methodologies [53]

5.3.2 *Robust Dual Threshold circuit*

Using the device fabricated by NeuDrive at the Centre for Process Innovation (CPI, Sedgefield, UK) using the Gen2 photolithography facilities. The Corbino and interdigitated OTFTs employ top gate bottom contact (TGBC) architecture

had been used for this study of dual threshold circuit. The results had been published in a journal [10].

The devices were characterized with the requirements established for the model development, performing a wide range of values for the gate or drain voltage applying potential from −30 to 30 V. Using this procedure, experimental data on key parameters were successfully extracted. By fixing the polarization of the transistor with the same V_{GS} and V_{DS} the saturation region is assured, in our case −20 V, allowing implementation of the well-known extraction procedure for the saturation region of the transistors [54]. This procedure is based on plotting the square root of the drain current versus the gate voltage. In the polarization point of $V_{GS} = V_{DS}$, a straight line is plotted until the x-axis intercept where the threshold voltage value is extracted, see **Figure 90**. The hole mobility was obtained dividing the slope value, in the polarization point of $V_{GS} = V_{DS}$, by the device total capacitance. Finally, the I_{ON}/I_{OFF} ratio was extracted from the ratio between the maximum current and the minimum current.

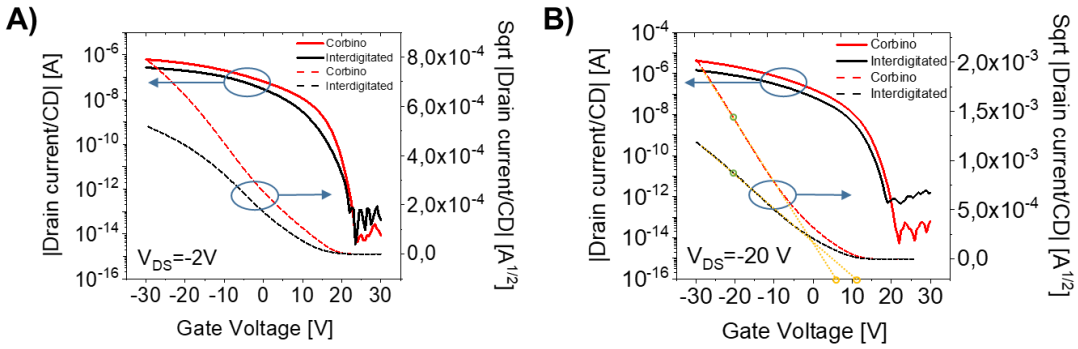


Figure 90. Square root and logarithmic scale transfer curves of both geometries types for the two behaviour of the transistors: **A)** lineal region, **B)** saturation region including the threshold voltage extraction procedure representation.

The dimensions of the Corbino devices were calculated as proposed in [55]. Defining R_2 as the bigger radius and R_1 the smaller one, the equivalent length of the device can be defined as:

$$L = (R_2 - R_1) \tag{11}$$

while the width of the transistor is determined with:

$$W = \frac{2 \cdot \pi}{\ln\left(\frac{R_2}{R_1}\right)} \cdot (R_2 - R_1) \tag{12}$$

The model implemented is defined in the Device Modelling chapter of this thesis where a compact model based on Shichman-Hodges Model [56], also known as MOSFET Level 1, is developed under our automatized PDK, once the device is fitted with the model, it is introduced in a Verilog-A module ready to be implemented in Virtuoso from Cadence.

All the electrical measurements were performed in ambient conditions and ambient light. The electrical characterization of the OTFTs was carried out using an Agilent B1500A Semiconductor Analyzer. The images were acquired using a light microscope DM4000 from Leica.

5.3.2.1 *Interdigitated and Corbino OTFTs*

For most of the basic research, the inverted/staggered and co-planar OTFT structures are the most commonly reported devices [57]. OTFTs can be implemented in different structures depending on the relative positions of the electrodes. Moreover, the electrodes in interdigitated configuration were predominantly adapted over the development of OTFT to account for the low conductivity of OSC. In this configuration, the source and drain electrodes are in a form of a comb, such that the finger of the drain comb is interdigitated with the fingers of the source comb providing larger current flow by increasing the channel width. Furthermore, it is worth mentioning that in the interdigitated geometry used in this work the gate layer totally overlies the source and drain electrodes. **Figure 91 Ai, Aii** depicts the scheme and an optical image of the interdigitated electrodes fabricated in this work, respectively. The main advantage of this configuration is their efficiency concerning the ratio between the transistor surface and the transistor width [39]. However, such geometry is not entirely satisfactory in terms of performance since great efforts were made to enhance the alignment of OSC crystal perpendicularly along the Drain and Source (D/S) electrodes during the OSC deposition such as undergoing a nitrogen flow, temperature, and varying the solvent nature and ratio [58]–[60]. In order to overcome this limitation and for the sake of fabrication simplicity, OTFTs with circular channel, called Corbino OTFTs, are commonly proposed. The circular geometry experiences all orientations of the crystals providing less device variability. Although one intrinsic feature of Corbino geometry is a low gate-drain overlying area over their interdigitated geometry counterpart, in this work, the Corbino devices present an overlapped gate-source/drain capacitance of 2.6×10^{-4} cm^2 while the interdigitated devices present 1.4×10^{-5} cm^2. **Figure 91 Bi** and, **Bii** shows a cross-section and the optical image of interdigitated and Corbino geometries, respectively.

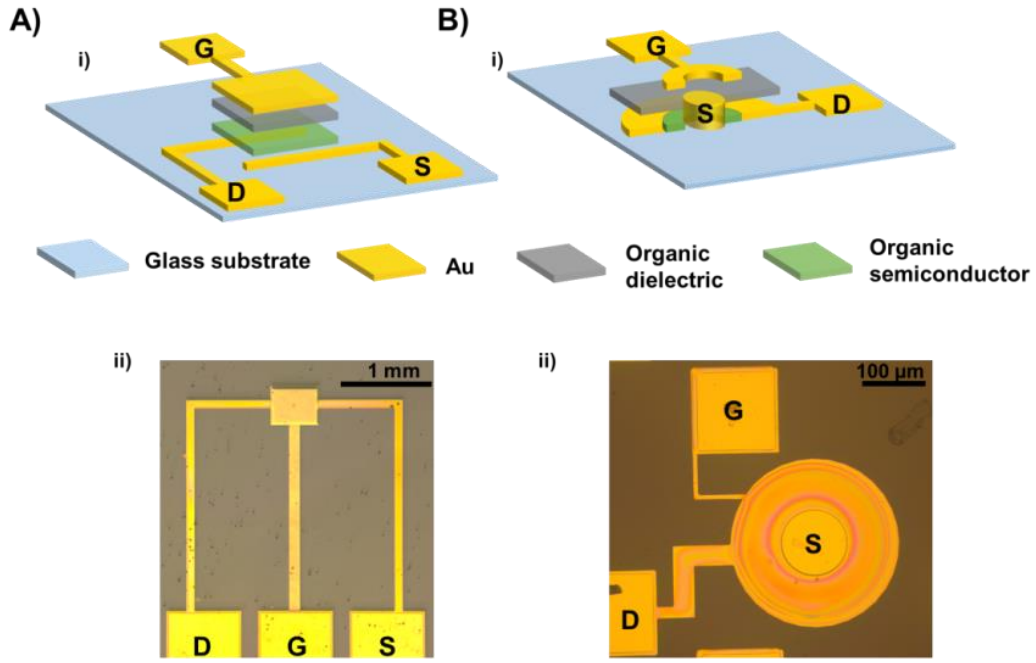


Figure 91. **A)** i) 3D scheme of the Interdigitated geometry and ii) its optical image; **B)** 3D scheme of the Corbino geometry and ii) its optical image. D, G and S refer to drain, gate and source electrodes, respectively.

Interdigitated and Corbino OTFTs were electrically characterized with a W/L of 40 (W = 160 µm/L = 4 µm) and 34 (W = 680 µm/L = 20 µm), respectively. For a better understanding of the device performances according to the geometry, the transfer curves were compared by normalizing the drain current with the W/L ratio, called Channel Dimension (CD). Since the devices were fabricated simultaneously on the same substrate, they show the same layer thicknesses and characteristics, thus, the observed differences in the transfer-output electrical characteristics are solely attributed to OTFT geometry.

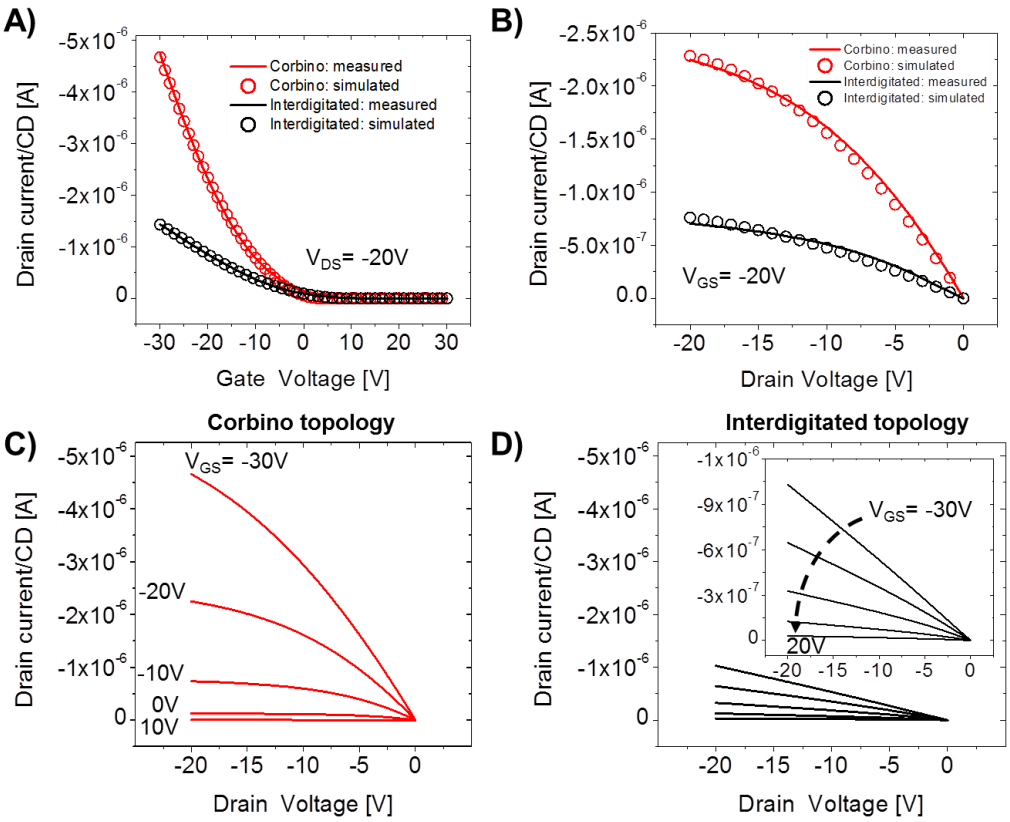


Figure 92. Experimental transfer **A)** and output **B)** characteristics for Corbino and interdigitated geometries normalized to Channel Dimension (CD) for V_{DS} = –20 V and V_{GS} = –20 V, respectively. The circular symbol refers to the theoretical transfer and output characteristics simulated by using a MOSFET level 3. **C)** Experimental output characteristics of Corbino geometry devices. **D)** Experimental output characteristics of interdigitated geometry devices where gate voltage (V_{GS}) was swept by −10 V from −30 V to 20 V. The output graph for interdigitated geometry is rescaled in the inset graph for better comparison. The channel length is 4 µm and 20 µm for interdigitated and the Corbino devices, respectively. Both have almost the same W/L ratio.

The measured and simulated transfer and the output characteristics of the interdigitated and Corbino OTFTs are shown in **Figure 92**. As can be observed in **Figure 92A**, the model correctly predicts with high precision the transfer curves for both geometries. In addition, the simulated output curves fit well with the measurement by providing a smooth linear-to-saturation transition, as shown in **Figure 92B**. Thus, the used model can be widely applied to OTFTs with interdigitated and Corbino geometries serving as a practical and versatile tool for organic-based circuit development. **Figure 92C** and **Figure 92D** show the measured output electrical characteristics for both geometries. The maximum drain current, named as I_{ON}, is significantly larger for Corbino devices than interdigitated devices, as can be observed in the zoom-in in **Figure 92D**, presenting values of 4.8 µA and 1.4 µA, respectively, for V_{DS} = –20 V and V_{GS}= –20 V. The same tendency is corroborated in the linear regime as can be seen in the transfer curve in **Figure 93A**, where the higher current is attributed to the Corbino geometry. Despite the fact that effective carrier mobility is affected by the dimensions of the channel length, the Corbino OTFTs tends slightly to saturate.

In contrast, the output drain current of interdigitated OTFTs showed a linear increase with V_{DS} and did not saturate. The unsaturated output characteristics in interdigitated devices were also clearly of larger channel length (see **Figure 93B**), thus, this phenomenon was not totally governed by short-channel effects. Indeed, the output characteristics of both geometries exhibited an obvious I_{DS} offset at V_{GS} = 0 V indicating an appreciable conduction, more pronounced in interdigitated OTFTs, due to a parasitic conduction path from the drain to the source. Due to this fact, the depletion mode current, which is called I_{OFF}, can be achieved by applying a positive voltage such that the conduction is suppressed. The depletion mode current in interdigitated geometry was reached by applying a V_{GS} = –20 V while in Corbino geometry the voltage applied was reduced to V_{GS} = –10 V, as can be compared in **Figure 92C** and the inset of **Figure 92D**. The I_{OFF} displayed are about one order of magnitude larger for interdigitated compared with Corbino devices, for V_{GS} = 0 V and V_{DS} = –20 V. In comparison with the Corbino devices reported previously [61], the circular devices developed in this work yielded similar output curves regardless the bias configuration, i.e., the inner-drain or outer-drain condition, see **Figure 94**.

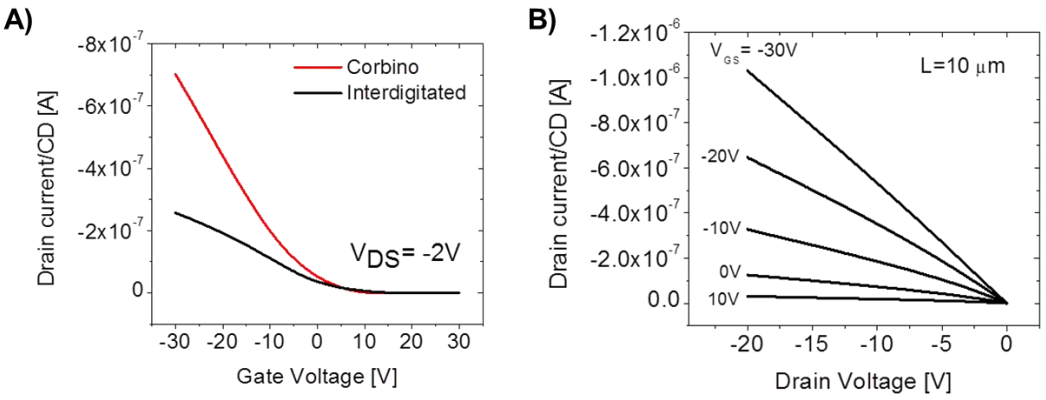


Figure 93. **A)** Experimental transfer characteristics for Corbino and interdigitated geometries normalized to Channel Dimension (CD) for V_{DS} = -2 V. **B)** Experimental output characteristics of interdigitated geometry devices where gate voltage (V_{GS}) were swept by -10 V from -30 V to 10 V. The channel length is 10 µm.

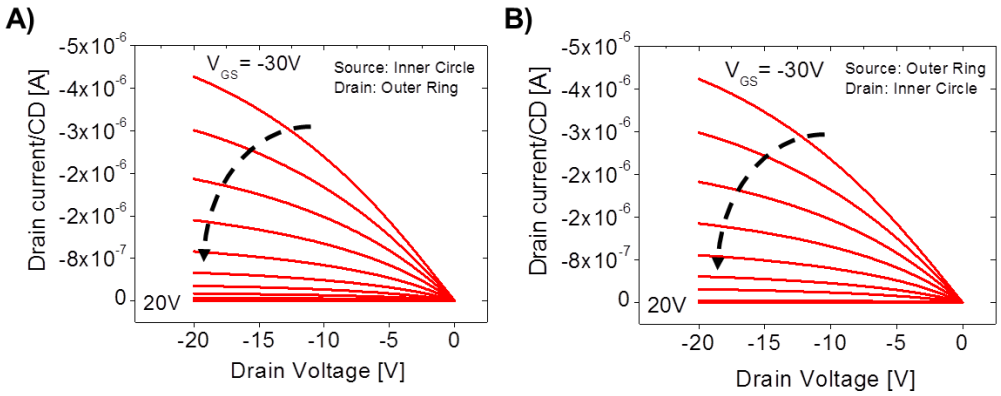


Figure 94. Output characteristics of the Corbino TFT for the two drain-bias conditions: **A)** inner circle as source and outer ring as drain, **B)** inner circle as drain and outer ring as source.

In order to gain insight into the electrical performance of both geometries, effective mobility, V_T, and I_{ON}/I_{OFF} current ratio were investigated as a figure of merit of interdigitated and Corbino geometries as shown in **Figure 95A-C**, respectively. Notably, there is a big difference in the effective hole mobility between the devices with different geometries. This result is due to the Corbino geometry despite presenting higher channel length compared with interdigitated OTFTs. The extracted effective hole mobility for Corbino geometries is about 1.61 $cm^2/V{\cdot}s$, and for interdigitated devices is about 0.71 $cm^2/V{\cdot}s$. Clearly, the OTFTs with Corbino geometry performed V_T closer to 0 V in the 4–8 V range, whereas interdigitated geometry performed V_T ranging from 8 to 14 V. Despite showing different threshold voltage for each geometry, the turn on voltage is the same for both devices since they share the same materials and fabrication procedure. Turn-on voltage has been extracted from the maximum point of the derivative in the logarithmic scale of the transfer curve and this result is included in **Figure 96**. Corbino devices present less variability of V_{ON} values than the interdigitated geometry devices. Regarding this difference, both types have very similar values for the turn on voltage, which is linked to the materials of the devices. Both devices work in accumulation mode, a result in good agreement with the improvement of the effective hole mobility in Corbino devices, which makes the V_T nearer zero. Interestingly, in the Corbino OTFTs, the V_T and effective hole mobility possess uniformity in terms of electrical parameter dispersion, which indicates that circular channel geometry is more robust in delivering good performance over large areas despite the polycrystalline nature of the small-molecules.

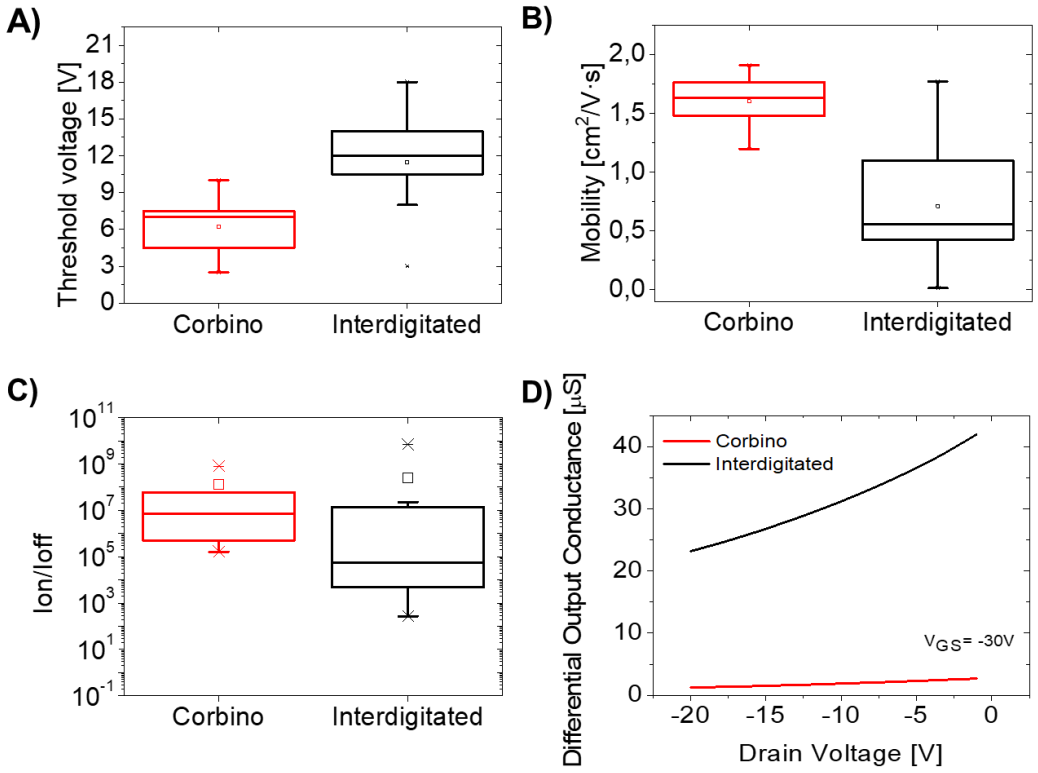


Figure 95. Electrical parameters such as **A)** threshold voltage, **B)** effective hole mobility and **C)** I_{ON}/I_{OFF} ratio for Corbino and interdigitated geometries. The central mark represents the median, box limits indicate the 25th and 75th percentiles, and whiskers extend to the 5th and 9th percentiles. **D)** Differential output conductance as a function of drain voltage at V_{GS} = −30 V.

A large number of methods have been developed to reduce the OTFT's current variability induced by random grain orientations of the organic semiconductor [62]–[64]. The semiconductor used in this work, FlexOS^{TM}, presents large crystal sizes in the range of tens of micrometres. As the grain structures have different grain orientations, the extreme grain-to-channel alignments were solved by a circular-shaped channel providing higher effective mobility and thus, lower V_T. The channel length is in the range of the grain domains: L= 4 µm and 20 µm for interdigitated and Corbino geometries, respectively. In order to measure the uniformity of the devices, the Relative Standard Deviation (RSD), defined as the ratio of the standard deviation to the mean drain current, was used. In particular, our results show that the overall RSD in drain current for interdigitated OTFT and Corbino OTFT were found to be 65.18% and 12.4%, respectively. Apart from the reduction in variability, an enhanced effective mobility and threshold voltage were achieved for Corbino OTFTs. Other electrical parameters of the devices have been studied as can be seen in **Figure 95C**, where the I_{ON}/I_{OFF} ratio is degraded for interdigitated devices owing to the presence of parasitic current in the *OFF* state. The I_{ON}/I_{OFF} ratios for Corbino geometries are about (10^7), two orders of magnitude higher than those of interdigitated devices. For logic gates, the I_{ON}/I_{OFF} ratio remains an important parameter that must be taken into account. Thus, a high current modulation ratio is a more important requirement than the high mobility for programmable

electronic circuits [40], [60], [65]–[67]. This behaviour is supported by the fact that Corbino geometry eliminates parasitic sources to drain current flows, hence, allowing an enhanced I_{ON}/I_{OFF} ratio. This phenomenon, previously reported in [68], is explained by the increment of the differential output conductance of Corbino devices, which is defined as $\delta I_{DS}/\delta V_{DS}$ and can be described as follows: For circular OTFTs, the W/L relationship remains fairly constant because the channel length modulation is compensated by the channel width modulation. Hence, beyond the pinch-off, the differential output resistance of the interdigitated TFT is finite; whereas, that of the Corbino TFT is infinite, which is in agreement with previous works [68], [69] and with the results obtained in **Figure 95D**.

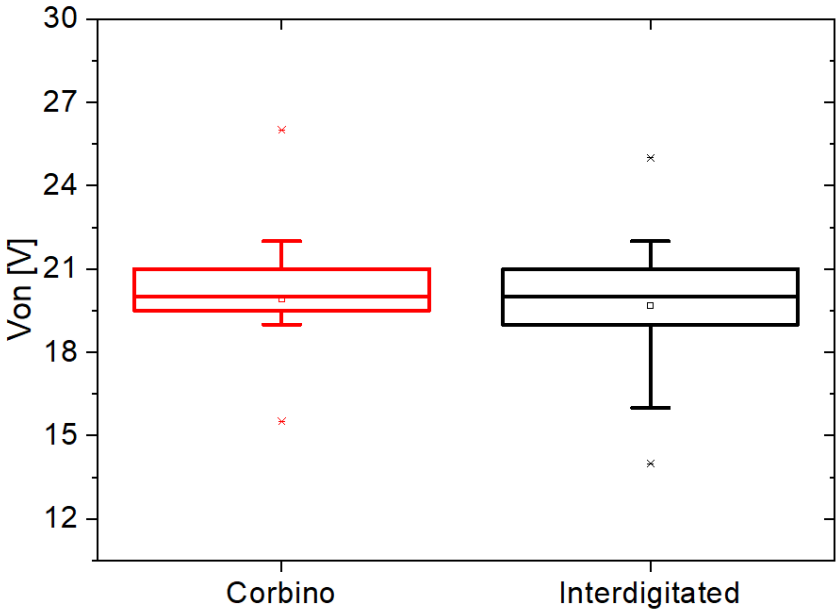


Figure 96. Turn on voltage of both geometries from the curve transfer curve with V_{DS}= -20 V. Central mark the median, box limits indicates the 25th and 75th percentiles, whiskers extend to 5th and 9th percentiles.

To conclude, these results reflect the fact that the electrical performances actually correlate with the overall geometric parameter ($\mu_{eff}C_{INS}W/L$) as supported by the higher the effective hole mobility (μ_{eff}), the higher the V_T and, the higher the I_{ON}/I_{OFF} ratios for Corbino geometry. For these reasons, and as a novelty compared with widely-reported logic gates based on interdigitated OTFTs, an inverter logic gate was implemented in further studies in this work.

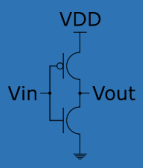
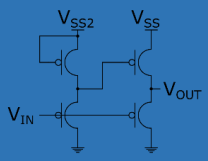
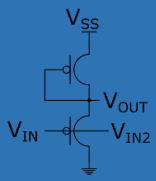
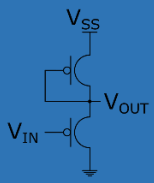
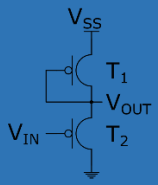
5.3.2.2 *Unipolar Organic Dual-Geometry Threshold Voltage Inverter*

The Inverter is considered to be the most basic logic circuit element for Complementary Metal-Oxide Semiconductor (CMOS) technology [70]. However, unipolar logic circuits are widely employed in the organic electronics field.

Unipolar based circuits which present either n-type or p-type OSC, require a pull-up (n) or pull-down (p) load transistor polarized in *ON* state and, an input-

controlled drive transistor which logically inverts its input [71], [72]. Therefore, for a low voltage (in terms of Boolean algebra, it is known as ‘0’) the input produces a high voltage (in terms of Boolean algebra, it is known as ‘1’) at the output, and vice versa [73]. In order to obtain a pull-down load transistor different geometries can be implemented. One of the most common geometries is based on the short-circuit of the gate and drain terminals yielding a fixed gate-to-source voltage, i.e., V_{GS} = 0 V, which turns the load transistor into a diode. In fact, this configuration is referred to as diode-load or depletion-mode load configuration [74], [75]. Based on the results of several works [26] which demonstrated that higher gain can be achieved by diode-load topology, this work will consider a diode-load topology for the inverter.

Table 17. Comparison of different topologies of OTFT design styles for basic inverters with key parameters.

	CMOS	Pseudo-CMOS	Dual-Gate	Diode-Load	Dual-Threshold
Inverter topologies					
Transistors	2	4	2	2	2
Power rails	2	3	3	2	2
Noise Margin	Most Robust	High Robust	Robust	Poor Robust	Medium Robust
Voltage swing	Full Swing	Full Swing	Non-Full Swing	Non-Full Swing	Almost-Full Swing
Power	Dynamic	Static and Dynamic	Static and Dynamic	Static and Dynamic	Static and Dynamic
Device Type	Complementary type	Mono-type	Mono-type	Mono-type	Mono-type

Different inverter topologies have been presented in the literature for monotype systems as shown in **Table 17**. From the simplest one using only one transistor and a resistor, to a more complex system where multiple devices are required. The most employed inverter topology for CMOS [76] technology involves two complementary transistors, meaning n-channel and p-channel. The advantage of this topology is full swing in the voltage achieved due to the alternative switching between *ON* and *OFF* state of the load and driver. Furthermore, this configuration allows a high gain with a significant robustness to the noise margin. The power consumption reaches minimum values because of the negligible power consumption in the static state of the inverter but, as a drawback, the fabrication processes involved are complex. For the monotype

devices, the pseudo-CMOS [26], [77] approach is the most robust topology since the polarization of the last transistor stage allows them to achieve full swing at the output. Despite this benefit, this topology requires four transistors and more power rails increasing the power consumption, which is detrimental for energy efficiency. In order to reduce the number of transistors and power sources required, the diode-load [78]–[81] is used because it operates with two unipolar transistors. However, this topology is less robust and presents non-full swing voltage at the output. Using dual-gate devices, [18], [82], [83] the diode-load configuration can have improved noise margins since the drive transistor is more robust against noise. The drawback of dual-gate transistors is the requirement of a more complex fabrication process and the inclusion of an additional power rail in the design.

The solution presented in this work is the use of a dual-threshold configuration [36], [37] which provides a lower noise margin and higher voltage swing at the output compared to the diode-load and the dual-gate topology, respectively. Dual-threshold technology has been studied for several years and applied to the silicon technology, achieving power consumption reductions [84], [85] and increasing the performance of the system in different aspects as delay [84], [86], robust designs [87], asynchronous circuits [87], asynchronous circuits [88], speed improvement [89] or glitch minimization [90]. The interdigitated and Corbino devices developed in this work present different electrical characteristics, such as V_T. Taking advantage of this behaviour, a dual-threshold configuration was implemented using these two geometries in order to obtain enhanced performance and reduced power rails. An interesting feature of this approach is the extreme simplicity for fabricating logic gates because the electrical parameters of the transistors are totally dependent of its geometry, allowing a unique manufacturing process for the entire circuit area.

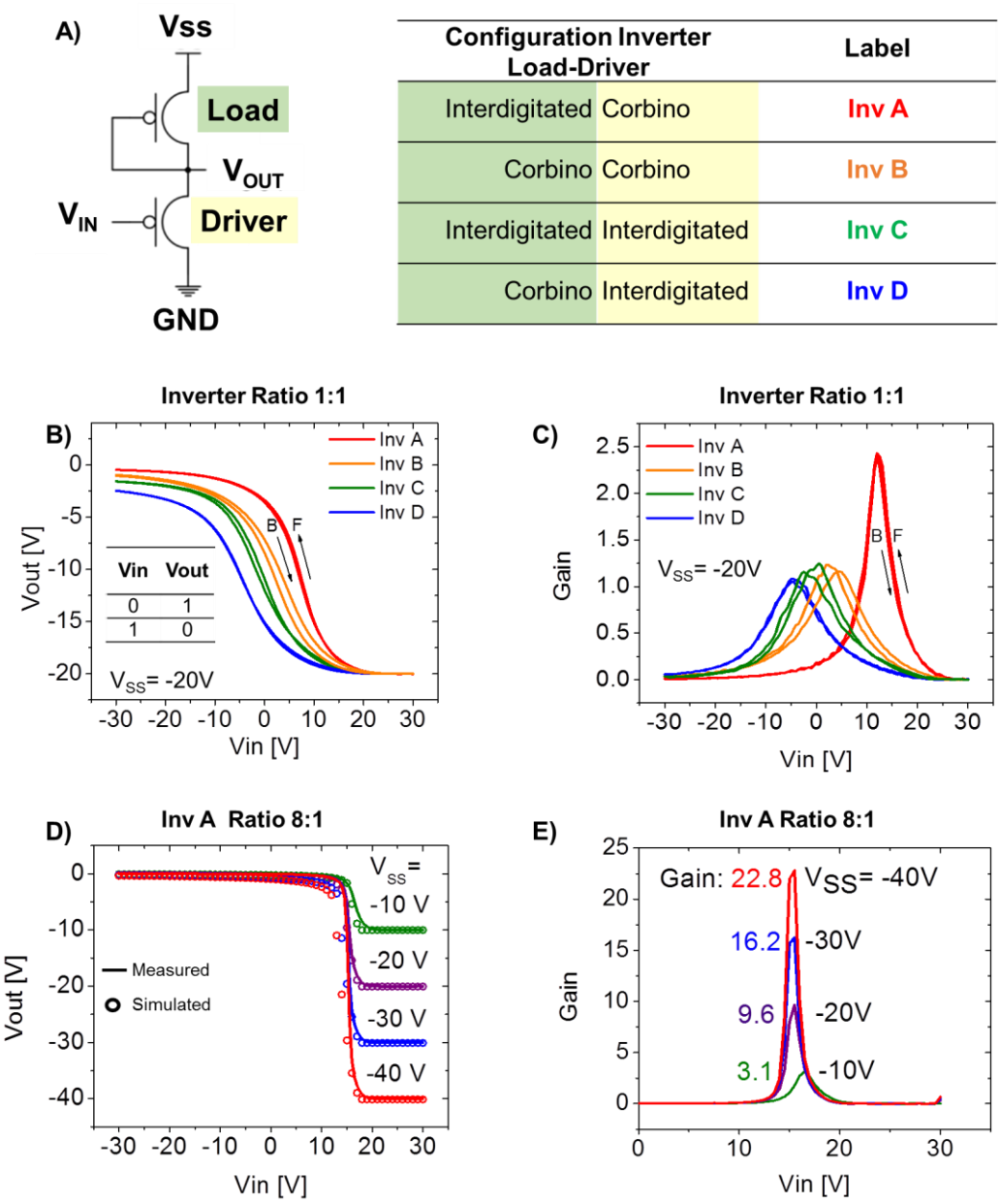


Figure 97. A) Inverter circuits by using different combinations of transistor geometries: **B)** Voltage transfer characteristics (VTC); **C)** and gain. **D)** VTC for Inv A geometry with a ratio 8:1; and **E)** the respective gain. ”F” and “B” denote forward and backward sweeps, respectively.

Figure 97A shows the schematic of the inverter. The load transistor is biased to the *ON* state, which allows the current to flow through itself by providing low resistance and the driver transistor switches between *ON* and *OFF* state controlled by the input. A figure of merit of the inverter circuit is the gain, which is defined as the maximum slope of the transfer curve of the system. Regarding gain, four different combinations of the two geometries for the driver and load were configured and characterized. The dimensions ratio, W/L, of the devices were equal (ratio 1:1) to be sure that the results were not influenced by the dimensions, as can be seen in **Figure 97B**. It can be noted that the configurations with a single type of geometry, i.e., interdigitated-interdigitated or Corbino-Corbino, provide higher hysteresis than the others. The best combination

obtained was placing the interdigitated geometry as a load and the Corbino geometry as the driver (called Inv A), where the gain was double the rest of circuit configurations, as shown in **Figure 97C**. Moreover, this combination geometry offered the full output voltage swing. Taking into account the driver transistor commutating between the *ON* and *OFF* states, the Corbino geometry as used as a driver because it provides higher performance than the interdigitated geometry, in terms of the I_{ON}/I_{OFF} ratio, allowing high current in the *ON* state and a negligible current in the *OFF* mode. Furthermore, the interdigitated transistor working as a load provided lower output resistance and, thus, a lower voltage drop at the output of the system allowing it to reach ground (GND) and V_{SS} values. Additionally, both geometries presented different threshold voltages, which induced a more resistive load device when the driver was in an *ON* state. These behaviours occurred owing to the lower V_{SD} and resistance in the *OFF* state of the driver, permitting a full swing of the output voltage thus reducing the hysteresis of the inverter.

To assess the maximum gain obtained by the topology of Inv A, a variation on the ratio of dimensions between the load transistor and the drive transistor was implemented by increasing the driver 8 times with respect to the load, as can be seen in **Figure 97D, E.** The study of the electrical behaviour of the inverter for four different V_{SS} revealed a link between the power supply and gain. In fact, the increased gain correlated with a higher power supply and at the same time delivered higher swing and higher slope. Moreover, the simulation of electrical behaviour for Inv A depending on the V_{SS} was implemented in Virtuoso and by introducing the generated models of each geometry, as can be observed in **Figure 97D**. Well-fitting measurements at the transitions were obtained for low V_{SS}, meanwhile the model correctly predicted the V_{SS} and GND values for all V_{SS}. The increment in the ratio between the driver and the load provided almost four times higher gain compared with the previous 1:1 ratio. This configuration presented a gain of 22.8 of the V_{SS} to −40 V, as can be observed in **Figure 97E**.

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6 RFID System Design

RFID is a communication system used in tags, cards and transponders with the objective to establish a communication for the non-contact identification that allows simultaneous detection of multiple tags. The use of electromagnetic waves, distributed in several free bands, allows the implementation of this technology without the need to request any commercial license. The radio electric spectrum used is divided into frequency bands. For low frequencies the range of 120-150 kHz (LF - Low Frequency) is used, while for high frequencies the 13.56 MHz band (HF - High Frequency) is used, at ultra-high frequencies (UHF - Ultra High Frequency) the bands from 868 to 965 MHz and the microwave spectrum operates at 2.45 GHz. Low and high frequency bands can be used globally without the need for a license since they are free to use.

6.1 RFID basics

RFID standards cover four different areas: air interface, data content, certification and system application. The main protocols developed for communication between the reader and tag are depicted and classified in **Figure 98** where International Organization for Standardization (ISO) 14223 is localized in LF, in HF we can find the protocols ISO 14443, ISO 15693, ISO 18000-3, in UHF the ISO 18000-6C and for microwave ISO 18000-7. Depending on the application desired and the restriction of the reading range, some frequency bands will be more appropriate than others, and one protocol should be prioritized over another.

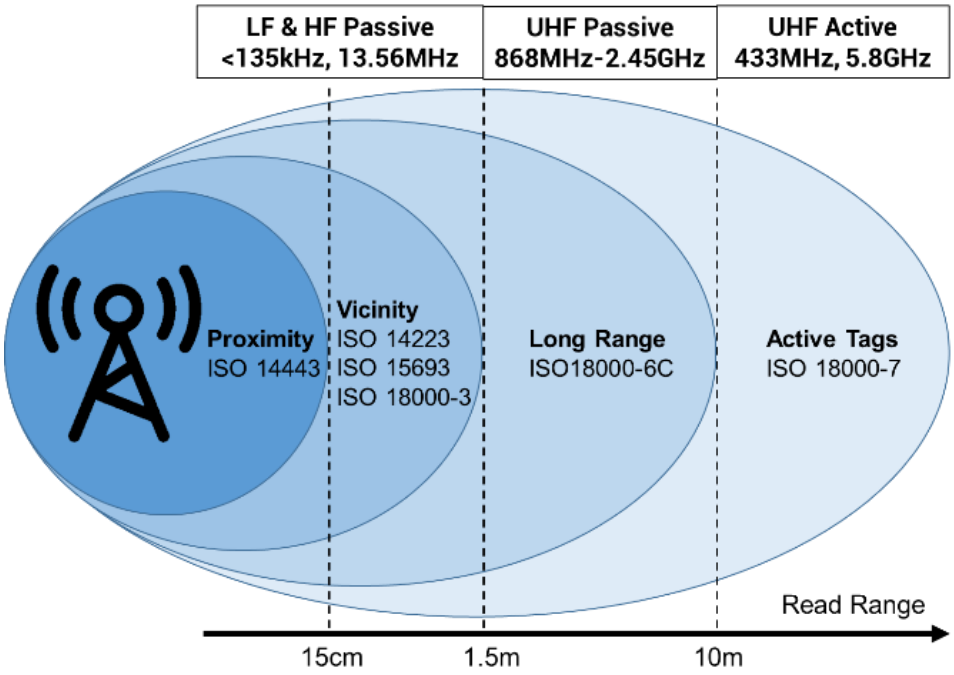


Figure 98. RFID protocols classification with reading distance.

In the radio frequency tags, two large groups must be distinguished: passive tags and active tags. Passive tags are characterized by not having any type of internal energy source, obtaining the necessary energy from the reader system, unlike active tags that have their own power source such as a battery or are powered by the electrical network. Active tags tend to provide a greater reading distance than passive tags (≈ 100m vs 10m). RFID technology is not new in the world of retail, some clothing stores have been incorporating this system for years with a reusable tag format, with which they must damage clothing in order to be incorporated, in addition to being a system that it cannot be implemented in other areas such as food or very low-cost products. This technology has many limitations and does not allow inventory control and tracking. Conventional RFID tags are beginning to be hybridized with printing technologies in order to provide flexibility to the antenna while keeping the computing center in silicon. The elaboration of these tags is based on the union of an integrated circuit made with unencapsulated silicon on an antenna made of laminated metal for mass production. The hybridization of the components must be performed with alignment techniques and conductive pastes.

The proximity RFID technology based on the ISO 14443 standard is called Near Field Communication (NFC). This technology exploits the reduced operating range for the sake of safety. This concept has been applied, with variations, to bank cards (contactless cards) or transport vouchers by applying a simpler variant of the 14443 standard. If an NFC-RFID tag can only be read from less than 10cm, it means that its content cannot be accessed from medium or long distances and the user can rely on it to store sensitive financial information without fear that it might be intercepted by an external system at a distance.

Regards the advantages of the organic and printed electronics, the technology does not have the same level of integration or maturity as silicon-based electronics. For this reason, the systems that are being developed based on organic electronics must be of less complexity, lower integration density and not so robust. If a silicon RFID chip can contain 3000 transistors and several Kb of reprogrammable memory, in the case of organic electronics, today, the designed organic systems have a maximum of 300 transistors and are programmed in the fabrication step. This forces us to think and propose more basic RFID architectures and optimize the transistor number. Despite this, the main reasons that justify the development of completely organic tags is the lower cost they offer. This low cost will allow the implementation of tags to any product obtaining a better and faster stock control.

Several solutions where organic electronics are combined with RFID devices had been presented by universities, technology centers and companies. Some of these solutions are complete (full NFC-RFID tag) or partial (some component of the system) and were developed as proof of concept of the technologies used and the technological capabilities of the entities involved. In the case of partial solutions, the range covers from antennas to transponders, through rectification stages and digital electronics, or circuits such as ring oscillators, which are essential for the correct working of digital circuits since they allow the generation of the necessary clock signal. In the case of ring oscillators, the maximum frequency obtained today is around 1 MHz [1]. Parts of an 8-bit microprocessor have also been developed [2]. On an industrial level, Philips research division developed an RFID tag for the 13.56 MHz frequency, integrating all the circuitry from inverters to logic gates and flip-flops with a 64-bit signal modulator [3]. Due to the low complexity of the circuits presented, RFID tags are not capable of implementing anti-collision protocols to avoid errors when a reader system reads more than one tag at a time. Despite this, there are some developments of elementary blocks for the elaboration of a 64-bit passive tag with organic technology to implement a protocol that allows obtaining the simultaneous reading of multiple tags [4].

IMEC research center, have developed several versions of NFC tags with different design strategies and based on pentacene-based p-type transistor devices manufactured on a flexible substrate. The first version is based on a 64-bit tag that operates at 787 b/s [5], while the second version reaches 128 bits with and improve the transfer speed until 1529 b/s [6]. **Figure 99** shows several implementations of the 12-bit code generator with which they achieve data rates that exceed the speed necessary to fulfill with the NFC ISO15693 sub-standard that requires 26.48 Kbit/s. The other NFC ISO14443 sub-standard requires data rates of 106 Kbit/s which is only known from Thinfilm/Kovio tags that meet these requirements where the maximum supported data structure is 16 bits.

	Diode-load	Dual-gate M2	Dual-gate M3	Pseudo CMOS
# TFTs/inv	2	2	2	4
Footprint inverter [μm^2]	19350	40300	19350	65812
Chip area transponder [mm^2]	2.70x2.98 (8.046)	3.91x3.87 (15.132)	2.70x3.14 (8.478)	4.69x3.36 (15.759)
# TFTs	218	218	218	436
# supplies	2	3	3	3
# litho	6	6	8	6
NM	Lowest <7.4% VDD/2	Tunable, ~36% VDD/2	Tunable, ~40% VDD/2	Tunable, ~24% VBIAS/2
Max. data rate	71.6kbit/s	11.3kbit/s	25.8kbit/s	43.9kbit/s
Substrate	Foil	Foil	Foil	Foil

Figure 99. Implementation of the 12-bit code generator as ROM memory [7].

Also, and based on organic materials with p and n type semiconductors, a 4-bit tag has been developed that responds to a maximum frequency of 196 Hz [8]. This solution is quite novel since generally everything that has been done until now is based on p-type transistors that are more stable combined with higher performances. Systems developed with p and n type transistors (CMOS) are not very widespread, with ThinFilm Electronics ASA (formerly Kovio) being the company with the most experience in implementation. The technologies used in the previous demonstrators are manufacturing technologies based on photolithographic processes based on organic materials on flexible substrates, therefore, they are not printing or additive manufacturing technologies, but conventional clean room technologies are used. This forces the organic and flexible chip to be manufactured separately with photolithography technologies, and, on the other hand, the antenna and rectifier assembly with printing technologies, finally proceeding to their hybridization to reach the final product. But some novel solutions of more advanced RFID Tags have been manufactured entirely with printed electronic technology integrating the use of antennas with integrated rectifiers, humidity sensors [9] and electrochromic displays [10]. **Figure 100** shows an RFID tag at a maximum frequency of 2 Hz to be used in biosensors through voltammetry measurements. This solution was developed with rotary technology (roll-to-roll) also showing the content of the tag on a printed display. These solutions go beyond the simple concept of RFID tag and are proposed as Point-of-Care (PoC) platforms for reading biosensors, presentation of results on the same tag and use of RFID for circuit power and acquisition. of the data by an external system such as a smartphone.

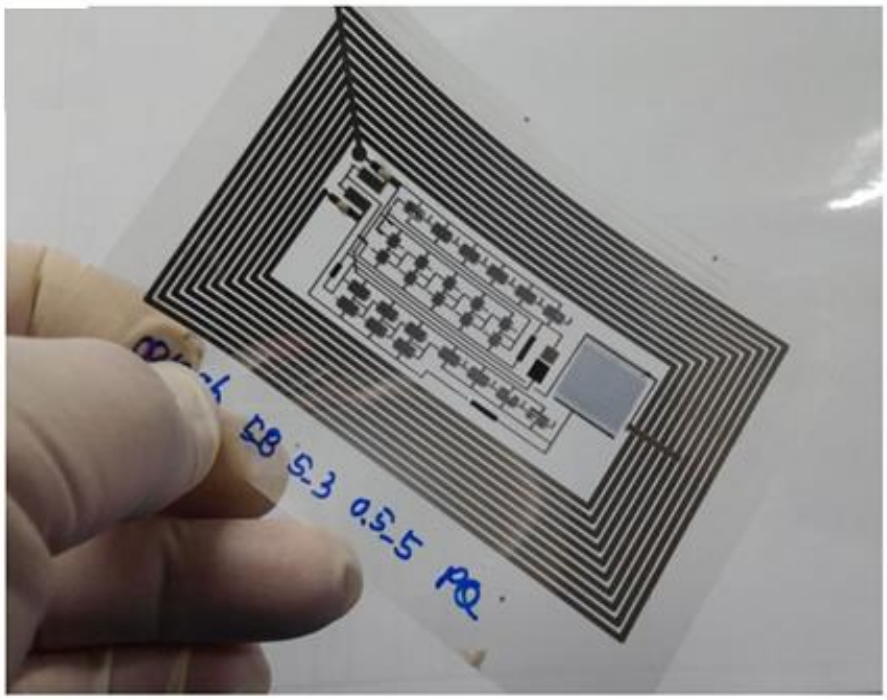


Figure 100. Flexible point-of-care system with reading/feeding by NFC and presentation of results on electrochromic display [11].

Although it is a very interesting technology, there is still no company with real production capacity that can offer a rotatory manufacturing of organic electronic circuits. Despite this, research is focused on this direction and all the know-how generated in materials, devices, electronic design and systems is fully compatible and reusable when the production technology is mature.

The manufacture of compatible NFC tags with any of the NFC sub-standards requires the use of manufacturing technologies that provide better resolution and registration, thus allowing the manufacture of transistor devices with higher characteristics, with unreachable channels of around 5 µm for printing technologies today, although less complex versions are being developed with printing technologies which will lower the cost barrier since rotary manufacturing can be extremely low cost. 12 or 16-bit tags compatible with the NFC ISO 15693 sub-standard can be developed with circuits of between 200 and 500 transistors. The tags compatible with the NFC ISO 14443 sub-standard are also compatible with the EPC GS1 standard (having more than 96 bits) but their implementation requires circuits with more than 2,000 transistors and more complex technologies. The following table summarizes, by way of example, some of these systems published in the literature in recent years.

	LTPS-CMOS (This work)	IGZO-Pseudo CMOS-SAL (ISSCC 2017) [1]	IGZO-Pseudo CMOS-SAL (ISSCC2016) [2]	IGZO-Diode-load (ETRI2013) [3]
# TFT/inv	2	4	4	2
Footprint inverter [um2]	5244	29277	36425	N/A
Chip area [mm2]	6.39x4.98 (31.82)	6.03x8.38 (50.55)	3.42x3.19 (10.88)	3.9x1.5 (5.85)
#TFTs	2002	1712	438	222
#supplies	2	3	3	2
Memory	112-bit	128-bit	12-bit	16-bit
16bit CRC	Self generated from circuit	built-in 128bit ROM	No	No
Clock generation	Division from carrier	Division from carrier	19-stage ring osc	9-stage ring osc
Data rate	105.9kbit/s (fc/128)	105.9kbit/s (fc/128)	396.5kbit/s	3.2kbit/s
Subcarrier frequency	847.5kHz (fc/16)	847.5kHz (fc/16)	None	None
ISO compliant	ISO-14443-A NFC	ISO-14443-A NFC	No	No
Power consumption	<1mW	7.5mW		
Substrate	PI- foil	PI-foil	PEN-foil	Glass

Figure 101. Some examples of NFC tags reported by IMEC [12].

6.2 RFID Architectures

Getting our focus on passive RFID tags, a minimum schematic of building blocks can be done based on a rectifier, clock generator/extractor, code generator, memory, data encoder and data modulator. **Figure 102** summaries these blocs and the behaviour between them.

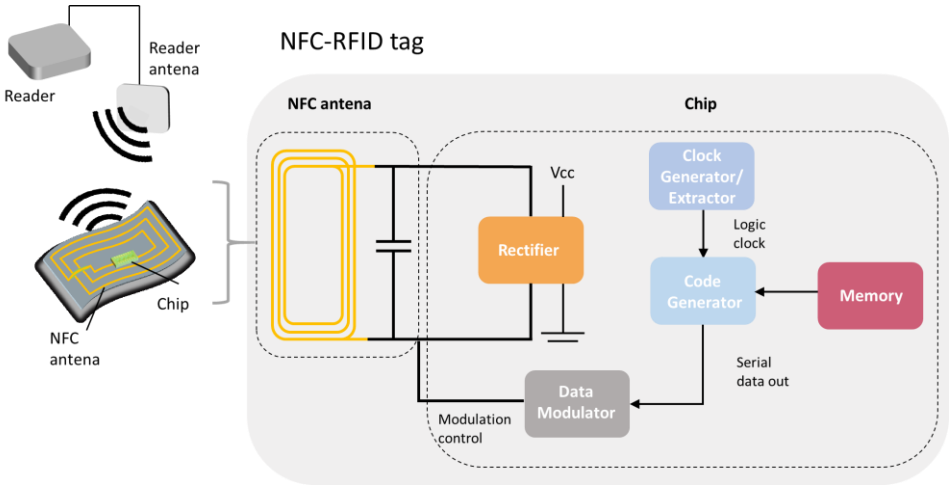


Figure 102. Basic blocs of a passive RFID tag and their workflow.

Focusing on the chip part, rectifying the incoming signal to feed the passive tag is the first step in the circuit operation. Passive RFID tags do not carry any power and the energy is obtained from the power radiated by the reader system.

In the current literature, antennas at these frequencies with a rectification stage have already been implemented to obtain a DC voltage in the organic electronics field [13].

Different architectures can be used to transform alternating waves to a continuous potential, where bridge rectifiers based on diodes or transistors are used. There are two types of rectifiers, half-wave and full-wave, half-wave rectifiers recover only half of the energy they receive from input while full-wave rectifiers rectify the entire input signal but have a greater complexity. The two rectifying architectures are depicted in **Figure 103**.

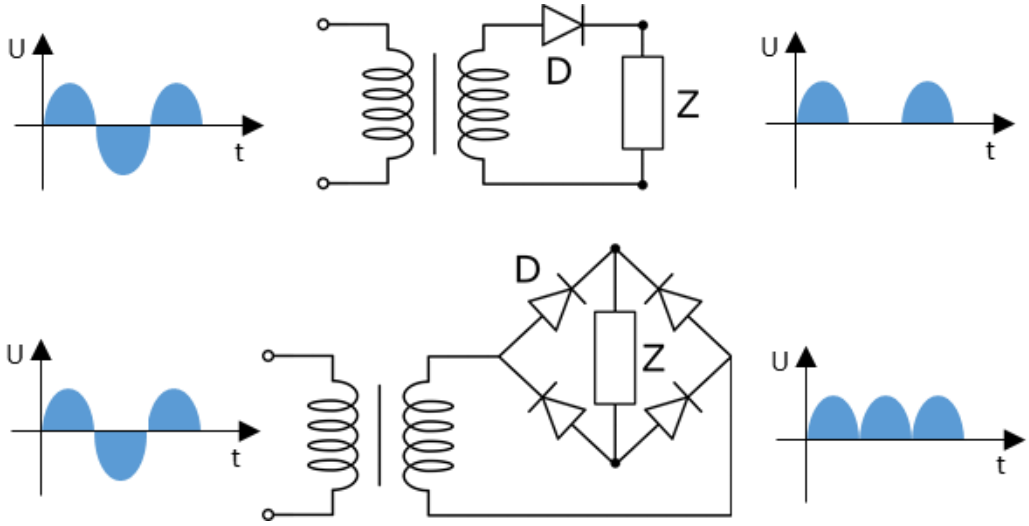


Figure 103. A) Half-wave rectifier **B)** Full wave rectifier.

Currently there are three configurations to make rectifiers: i) vertical Schottky type junction, ii) p-n junctions and iii) transistor with diode configuration. However, Schottky-type diodes have been the most used device for their simplicity in manufacturing compared to transistors and p-n junctions. The Schottky type junction is based on the use of a rectifying metal in contact with an organic semiconductor and an ohmic metal (the final structure being metal-semiconductor-metal). Rectification arises from the difference in work functions between these two, favouring the passage of current only in one direction and blocking the flow in the opposite case. To achieve this operating regime, different solutions have been investigated such as the introduction of monolayers to misalign the work function of the metal itself with respect to the semiconductor. Other approaches are based on the use of two conductive materials with a misaligned work function at each semiconductor contact. In addition to organic semiconductors, the use of oxide-based semiconductors has also been proposed due to their high mobility, providing a higher operating frequency. As an example of flexible diodes, **Figure 104**A shows the effect of the introduction of the PFBT-based monolayer in the gold electrode to improve rectification reaching a cut off frequency of 13.56 MHz with an output potential of 14 V [14]. Another recurrent solution is rectification based on the use of the gold-organic semiconductor-

aluminium stack due to the misalignment of the aluminium with the semiconductor. At work [15], they manage to rectify a 13.56 MHz signal, providing a DC voltage of 5.1 V with a resistance of 10 MΩ (**Figure 104**B). Apart from organic semiconductors, oxide-based semiconductors have been used for the manufacture of p-n and Schottky diodes reaching higher operating frequencies. An example is the work [16] where the semiconductor is based on MoO3 producing rectification at 1.24 GHz with an output potential of 3.8 V (**Figure 104**C).

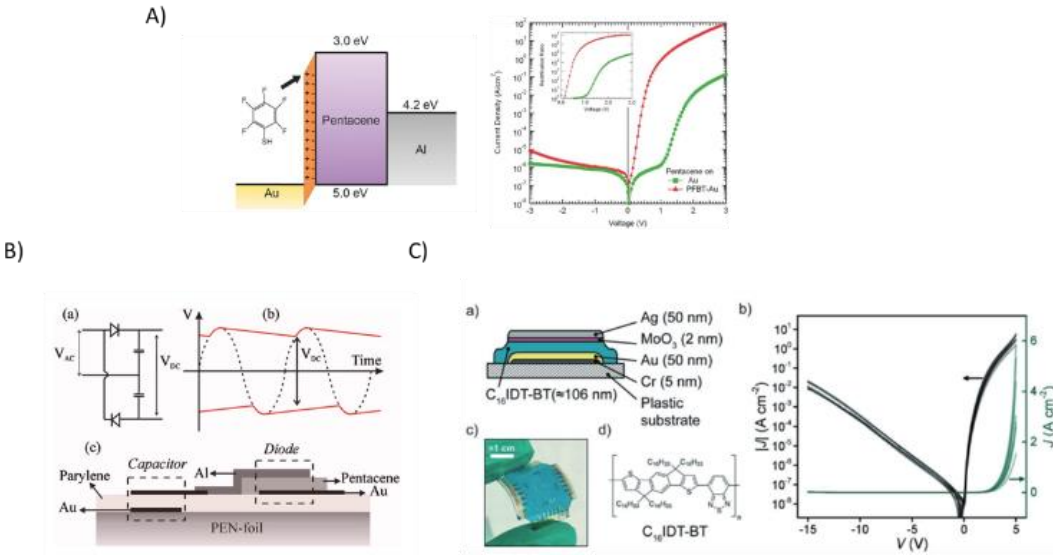


Figure 104. Different configuration of organic and flexible diodes [16].

Clock generator/extractor is the part in charge of synchronize all the other logic components, generating or extracting the clock signal where all the modules will be attached. Clock extractor can be thought as the straight way to obtain a clock signal since it allows working in synchronization with the reader, it is based on a series of frequency divisors. But it requires devices that work at least at the reader emission frequency, in case of NFC at 13,56 MHz, for the moment any publication had achieved this frequency with transistor devices that allow to implement the frequency divider in the organic field, making this a technological barrier for the clock extractor implementation. With this issue the used implementation in organic tags is the clock generation, usually with ring oscillator architectures since the simplicity of implementation of this logic module. Ring oscillators are based on a chain of inverters, it generates a clock signal at a specific frequency allowing generating a digital clock signal independent of the RF signal. Moreover, ring oscillator circuit is very used to evaluate the characteristics of manufactured transistors, so it is a simpler option to implement. Both architectures are shown at **Figure 105**.

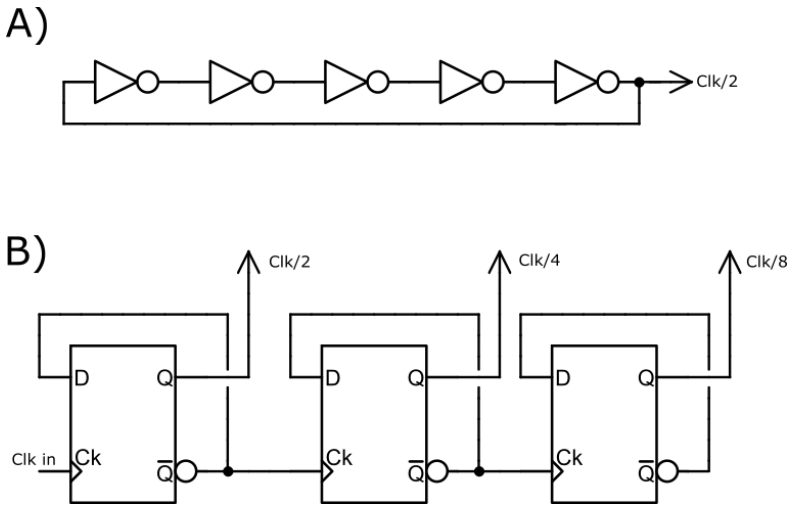
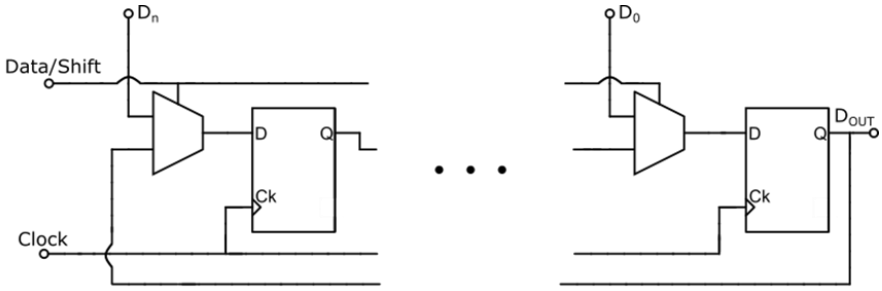


Figure 105. Different architectures for clock signal generation, **A)** ring oscillator, **B)** frequency divider.

The maximum frequency obtained from a ring oscillator with organic materials is 1 MHz [1]. But there are many examples in the scientific literature with different characteristics and benefits.

Programmable Read Only Memory (PROM) is the best memory type for a fixed identifier tag, since it only can be programmed in the fabrication step, avoiding future inscription of fraudulent codes. This memory is based on the use of fuses that burned or keep during the fabrication step, generating a fixed and non-reprogrammable code. The memory is usually accessed through multiplexers allowing the access row-by-row and column-by-column to the data. Other option to fuses is the inkjet-configurable gate arrays [17], where using a deprogrammed base design that will be configured in the final manufacturing phase using inkjet technology. The system would be programmed by depositing small drops of conductive ink (normally in volumes of 1 to 10 pL) that make up the digital identifier of the tag. If no drop is deposited, the code will be read as “0” and if drop is deposited, a “1”. This system can allow very high-speed programming and is extremely simple and additive.

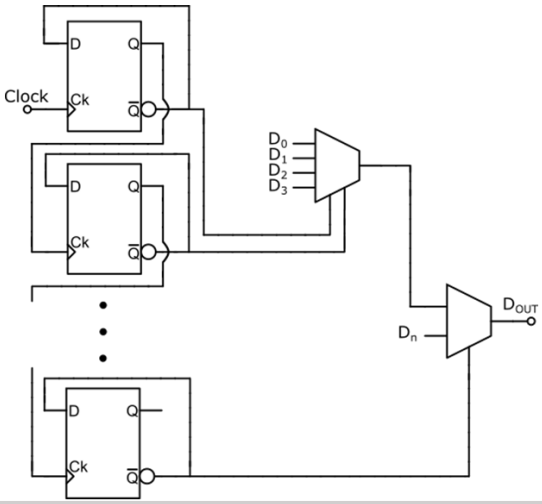
The memory will be accessed by the code generator that will send the data sequentially to the modulator. The code generator can be implemented in multiple ways one of the simplest is using shifters with a Parallel Input and Serial Output (PISO). This implementation is based on the use of shifters constructed with D type Flip-Flops and multiplexers, generic circuit shown in **Figure 106**. All the bits of tag identification (ID) are loaded in the start using the data/shift signal, then this signal changes and the bits shift to the output of the code generator one by one in the following clock cycles.



bit	MUX	Flip Flop	NAND	TFT
8	8	8	64	272
16	16	16	128	544
32	32	32	256	1088
64	64	64	512	2176
96	96	96	768	3264
128	128	128	1024	4352

Figure 106. PISO code generator and a table of the transistor scaling with the bits.

Other option is the use of a counter and a set of multiplexers, accessing point by point to the memory. The counter can be implemented using D type Flip-Flops and a series of multiplexers configured with the tag ID, an example circuit can be seen in **Figure 107**. The counter selects with each iteration one input of the different multiplexers of the second stage, providing at the output of the code generator the tag ID.

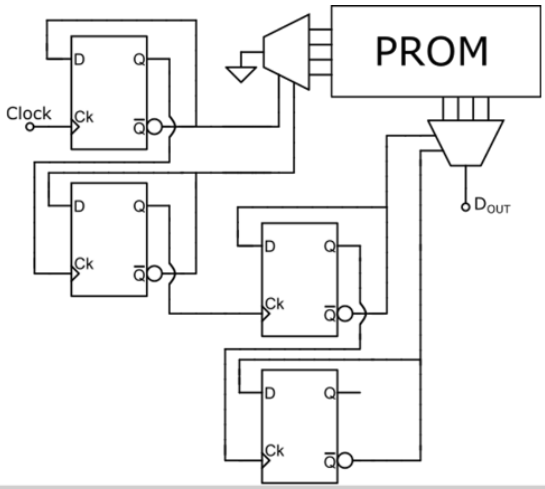


bit	MUX	Flip Flop	NAND	TFT
8	5	3	32	134
16	10	4	56	232
32	20	5	100	410
64	40	6	184	748
96	80	7	348	1406
128	80	7	348	1406

Figure 107. Counter and multiplexer architecture for the code generator.

Using the same schemes of counters but with a more efficient way to access to the tag ID is the counter and PROM option where the tag ID is stored in a

PROM memory that is accessed with one demultiplexer for the rows and another multiplexer for the columns where the line selector are connected to different points of the counter, providing a serial output of the tag ID at the output of the code generator, this more optimized circuit can be seen in **Figure 108**.



bit	MUX	Flip Flop	NAND	TFT	TFT ROM	Total
8	3	3	28	118	8	126
16	4	4	32	136	16	152
32	5	5	40	170	32	202
64	6	6	48	204	64	268
96	7	7	56	238	96	334
128	7	7	56	238	128	366

Figure 108. Counter and PROM architecture for the code generator.

These architectures can be compared with the state of the art circuits with organic RFID circuits [3], [18]–[20]. Big differences can be spotted between the architectures as the bits of the tag ID increases being the best architecture the counter with the PROM memory, see **Figure 109**.

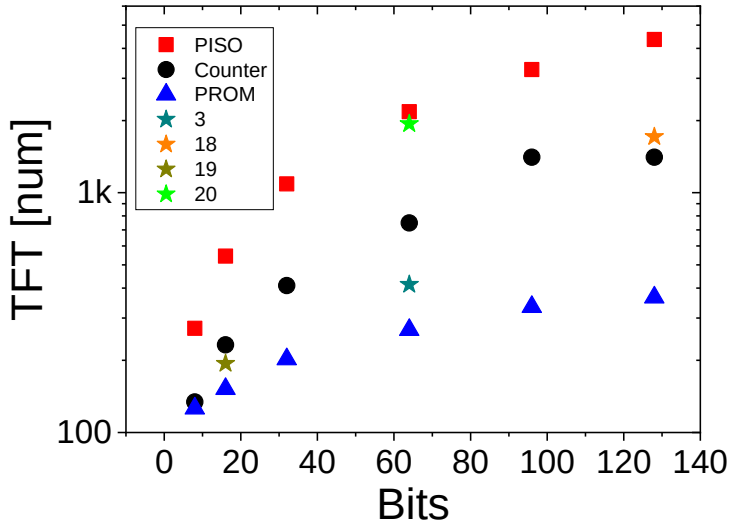


Figure 109. Benchmark of the architectures.

The return of information to the reader system is carried out by means of the signal modulator. This system allows configuring the signal emitted by the tag back to the reader system with the information modulated with the protocol used. Some works use their own coding for the encapsulation of the frame with 4 bits at the beginning of the header followed by the 4 bits of tag information using non-zero return encoding [8]. Other work has focused on a 64-bit Manchester encoding for this signal modulation [3]. The signal modulator block is usually implemented with a single transistor connected to the antenna and the supply voltages between the source and drain terminals. The gate is connected to the output of the code generator modifying the impedance of the receiver coil depending on the ID transmitted.

The use of Cyclic Redundancy Check (CRC) can be hardwired or pre-programmed in the memory allowing the saving of 1/3 of the total number of the TFT that involves the CRC generator, providing a reduction of the tag power consumption, this methodology had been already tested in [21].

Once the signal is sent from the tag to the reader two types of data collision can happen: (1) two readers accessing to the same tag, this can be solved using a single reader, and (2) multiple tags collision in the same reader, where different solutions can be implemented, the two types are depicted in **Figure 110**.

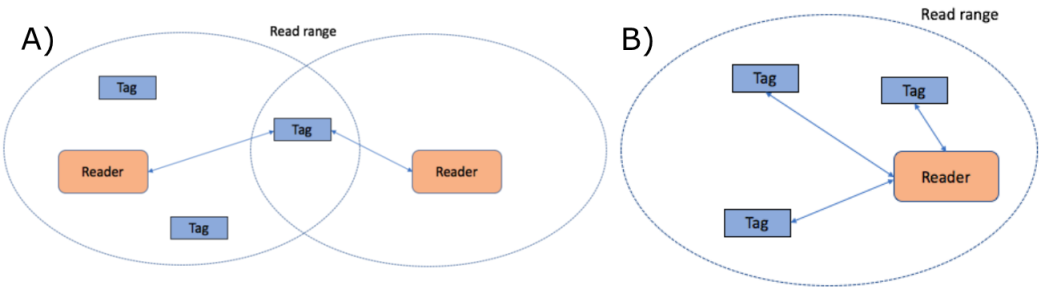


Figure 110. A) Reader collision **B)** Tag collision [22].

For avoiding the tag collision four different strategies can be follow: Space Division Multiple Access (SDMA), Frequency Division Multiple Access (FDMA), Code Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), represented in **Figure 111**.

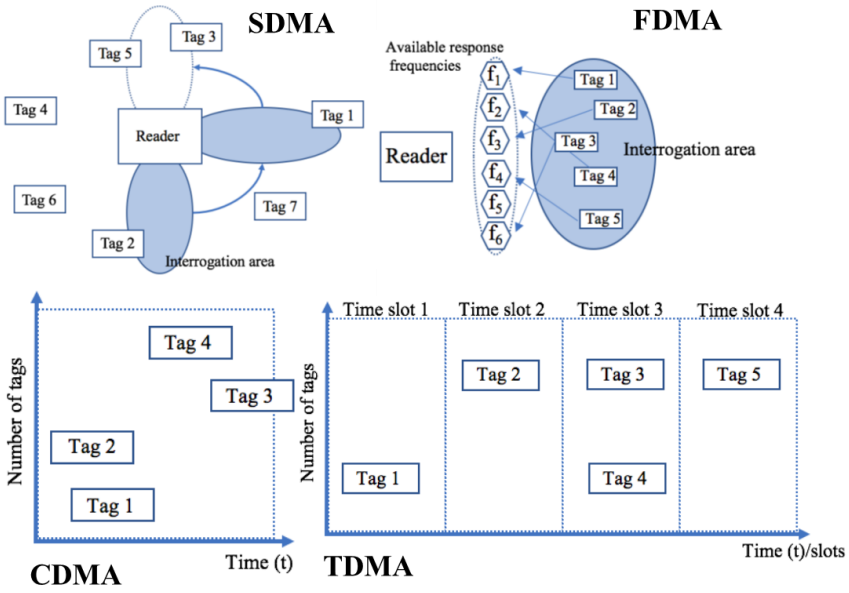


Figure 111. Four types of tag anticollision, SDMA, FDMA, CDMA and TDMA.

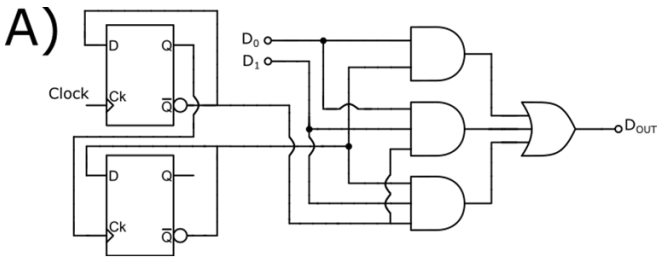
SDMA protocol is a simple solution to apply, only if the application allows it, this reduces this protocol to a small group of applications since the tags have to be distributed in the space around the reader system, while this is addressed for reading. Additionally, it requires of the use of expensive and complex antennas. In the FDMA access method, the tag uses different frequencies, making the reader system highly complex and that each tag has a transmitting antenna at that specific frequency, this solution has a limited use in applications and is not widely used. CDMA solution is based on the increase of the identification number of tags, allowing them to have high security on the identification in the reader system. This makes the tag more complex while allowing the identification of multiple simultaneous tags. TDMA is the cheapest and most widely used solution of all, but it requires the implementation of many more anti-collision algorithms. The transmission channel is divided in time slots for each tag where only one device per slot emits, in this way the reader ensures that it can detect the tag multiple times avoiding interference from another. Another option is that the tag only responds if it is asked. But this approach is a slow solution for the identification of a large number of tags.

TDMA presents different solutions to be used, the most popular and effective is the Aloha protocols, divides in four different types: Pure Aloha (PA), Slotted Aloha (SA), Frame Slotted Aloha (FSA) and Dynamic Frame Slotted Aloha (DFSA), a representation and comparison table can be found in **Figure 112**.

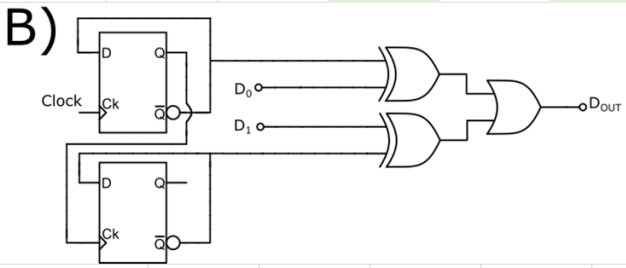
Protocol Name	PA	SA	FSA	DFSA
Protocol feature	Tags transmit after random time to the reader. In the case of a collision tags will retransmit after a random delay.	Tags transmit their ID in synchronous time slots. In case of a collision, tags retransmit after a random delay.	Each tag responds only once per frame.	Tags transmit once per frame. The reader uses a tag estimation function to vary the frame size.
Disadvantages	In a dense tag environment the the number of collision increases significantly.	In a dense tag environment the the number of collision increases significantly. The reader requires synchronization with tags.	It uses a fixed frame size and does not change the size during the identification process.	It cannot move into the next frame at any time based on the situation of collision without finishing the current frame.
RTF/TTF	TTF	RTF	RTF	RTF
Efficicency	18.4%	36.8%	36.8%	42.6%
System cost	Very low	Low	Expensive	Expensive
Complexity	Very simple	Simple	Medium	High

Figure 112. Different aloha protocols represented on how they work. Table with comparison of characteristics of the protocols.

To implement the simplest aloha protocol, the PA, two different circuits are presented for generating the random delay of each tag based on the identifier of itself. Both solutions are based on the use of counters and logic gates but the logic are different, depending the requirements of the desired PA can be used one or the other since the final number of Thin Film Transistor (TFT) are very similar in both cases since the logic part is can be optimized by using Karnaugh method, **Figure 113**.



Enable Random ID<Counter						
bit	Gates	Flip Flop	AND	TFT	Delay bits cou	TFT total
2	11	2	47	192	2	228
3	19	3	73	298	3	352
4	22	4	94	384	4	456
8	44	8	188	768	5	858
16	88	16	376	1536	6	1644
32	176	32	752	3072	7	3198



Enable Random ID=Counter						
bit	Gates	Flip Flop	AND	TFT	Delay bits cou	TFT total
2	9	2	45	184	2	220
3	14	3	68	278	3	332
4	19	4	91	372	4	444
8	36	8	180	736	5	826
16	69	16	357	1460	6	1568
32	134	32	710	2904	7	3030

Figure 113. A) Delay generator comparator for tag ID < than counter **B)** Delay generator comparator for tag ID = than counter.

6.3 RFID tag simulation

Using the data provided by SmartKem of their dual gate transistors, combined with our automatic modelling methodology, a DC model had been generated and optimized. Regards is not a complete model due to the lack of enough characterization data, we decided to simulate and include an RFID tag with 16-bit identifier to test the quality of the fabrication process in this early stage. It is expected to characterize a huge number of devices and extract a better model with parameter variability and AC behaviour based on the devices designed in the Layout Design chapter of this thesis.

In this first step for the circuit simulation, the transfer curve of dual gate OTFT had been used combined with the model developed in the Device Modelling chapter of this thesis, with an accumulated error in the modeling section lower than 0.01% in the transfer curve, the model and the OTFT schematic is shown on **Figure 114**.

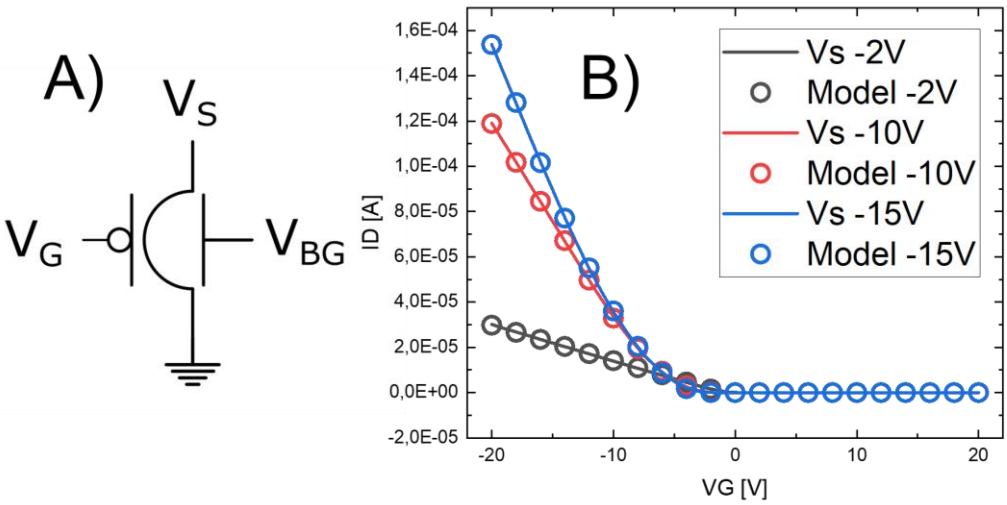


Figure 114. A) Dual gate OTFT schematic, **B)** Experimental (line) vs model (dots) transfer curve, back gate biased at -2 V.

Using the generated model, NAND gate was configured, **Figure 115A** and **Figure 115C**. With the two inputs, A and B, on the top gates while the bottom one is configured as a resistance. All the back gates of the devices are connected together allowing a single configuration to determine the threshold voltage level. The simulation results show a high level of the output only when both inputs are in low state, in all the other cases the output is in low state, **Figure 115B**.

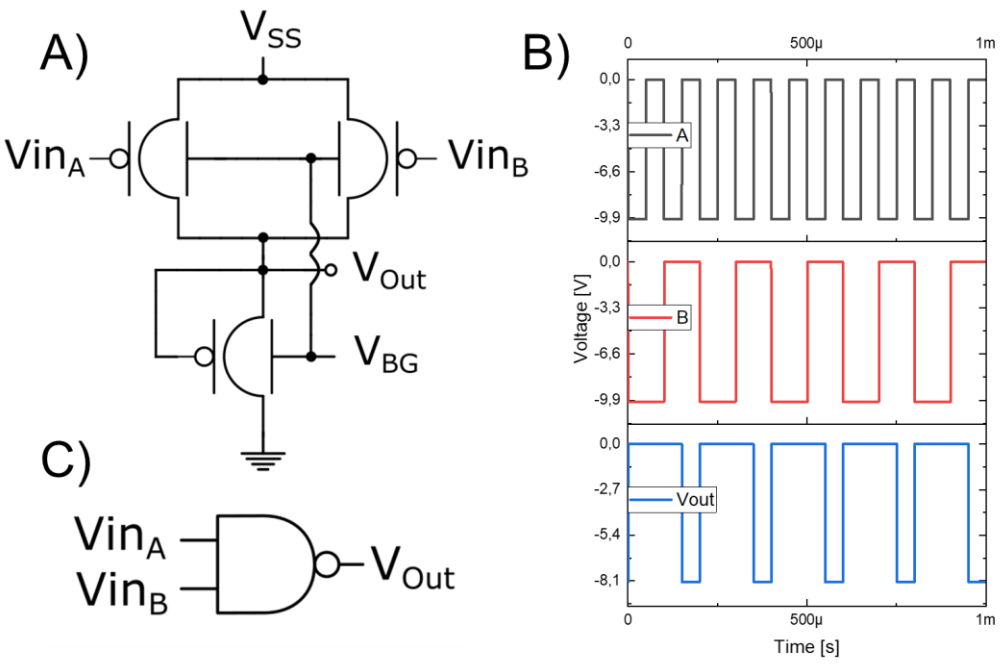


Figure 115. A) NAND Gate with 2 inputs with common back gate, **B)** simulations results of NAND gate for a back gate of -2 V and Vss of -10 V and **C)** NAND gate symbol.

For choosing the best geometry ratio for the logic gate, a limit for each device had been imposed and using optimization method usual in the silicon technology,

a global optimization related to the OTFT dimensions had been performed with the objective to obtain the maximum output voltage. The optimization step had been configured to stop when there is no improvement in the last 100 iterations. This step provides a result for the two top devices a total width of 4000 µm and a channel length of 4 µm, while the bottom transistor have a total width of 80 µm and a channel length of 10 µm. The optimization and work report can be seen in **Figure 116**.

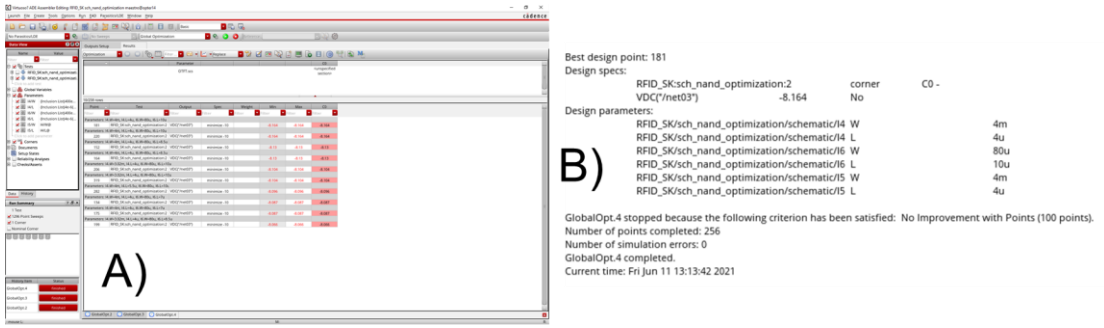


Figure 116. A) Results of the global optimization of device geometries and **B)** work report.

With the NAND gate symbol created and the optimized dimensions, the first logic circuit to be simulated is a Flip-Flop type D, with Q and Not Q outputs, **Figure 117A** and **Figure 117C**. The circuit had been configured with NAND logic gates regards the low transistor number optimization of this distribution, it provides high reliability. The simulation of the system shows that the Q state is equal to the D state of the previous clock transition, moreover the NQ output is the complementary signal to the Q output, **Figure 117B**.

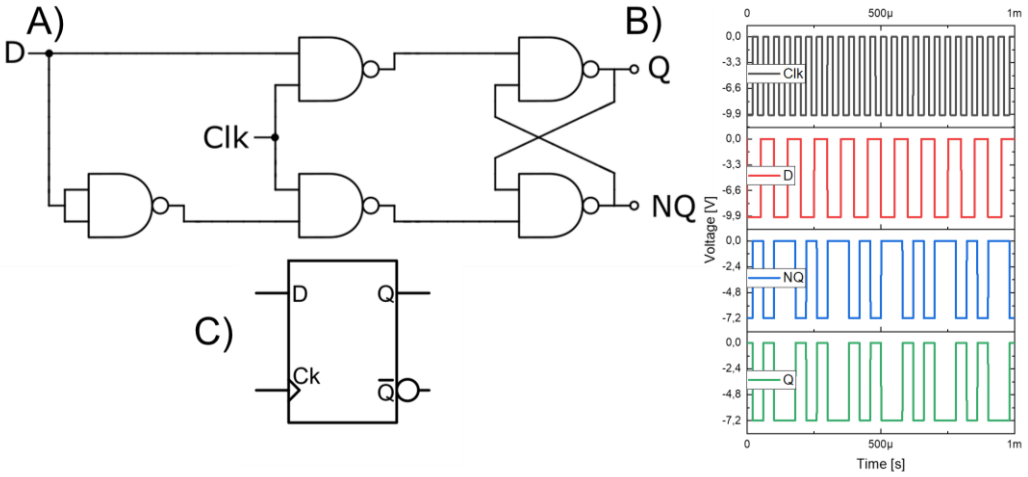


Figure 117. A) Flip-Flop type D with NAND gates, **B)** circuit simulation results and **C)** circuit symbol.

Using the D type Flip-Flops a 4 bits counter had been designed with four flip flops connected in clock series, the output of the first is going to the clock of the next one, **Figure 118A**. The simulation results, **Figure 118B**, shows the proper

working of the counter with the Less Significant Bit (LSB) at the position b_0 which each cycle makes that the next bit increments.

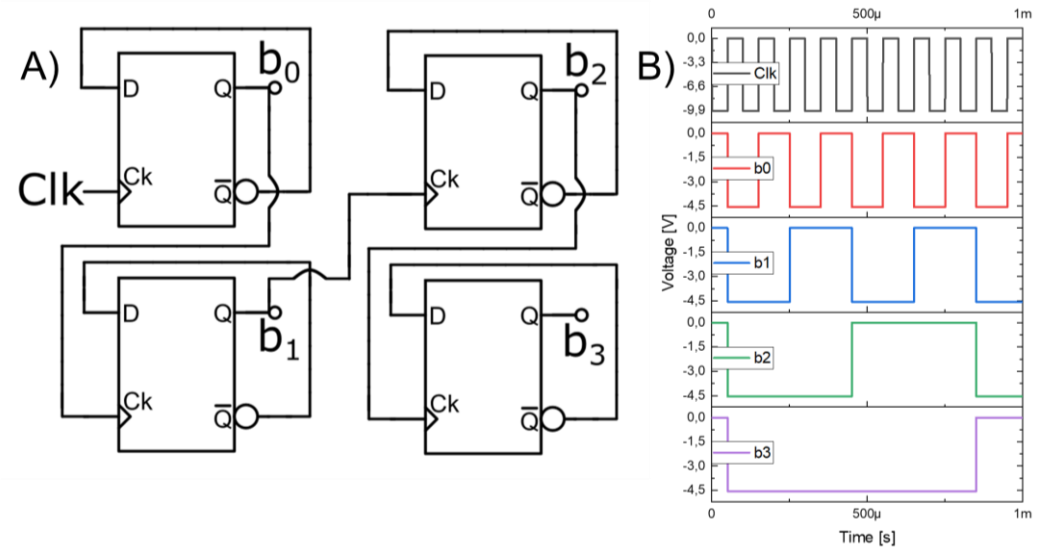


Figure 118. A) 4-bit counter based on D type Flip-Flops and **B)** circuit simulation results.

For the ID code addressing, multiplexers are used for allowing the access of the 16 bits of the tag ID using reduced number of transistors with high reliable behaviour, **Figure 119A** and **Figure 119C**. In this simulation, I_0 input is connected to -5V and I_1 is connected to -10 V, having the output connected to I_0 when selection signal is low and to I_1 when is in high state, **Figure 119B**.

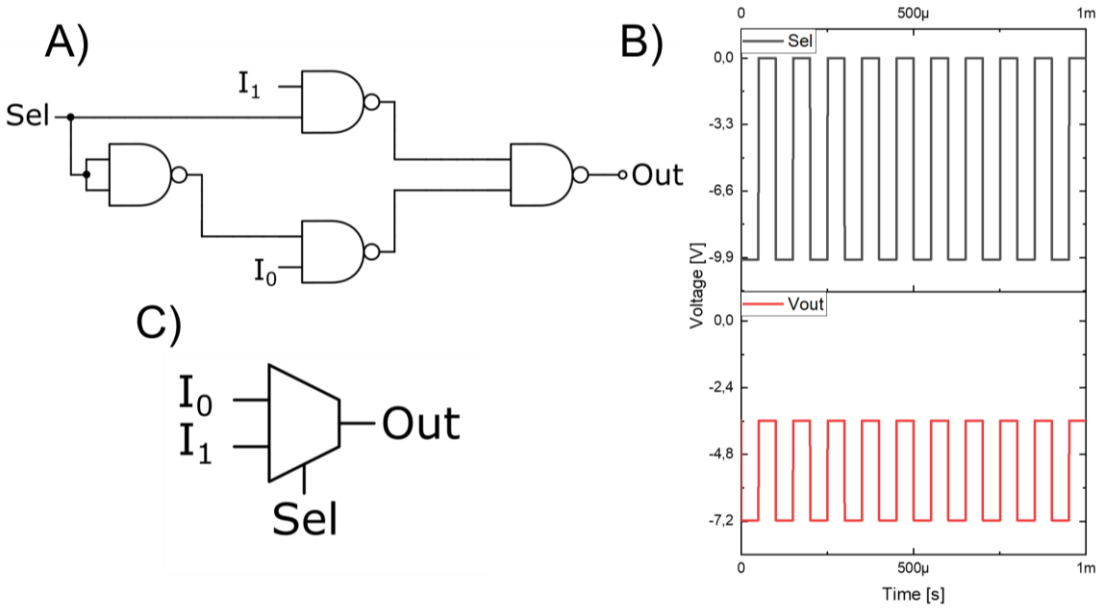


Figure 119. A) Two input multiplexer based on NAND gates, **B)** circuit simulation results and **C)** circuit symbol.

Based on three two input multiplexers, a four inputs multiplexer is configured, **Figure 120A** and **Figure 120C** and simulated. Inputs 0 to 3 are connected to -2.5 V, -5 V, -7.5 V and -10 V respectively, the output voltage follows the selection signals as expected, being selection 0 the LSB, **Figure 120B**.

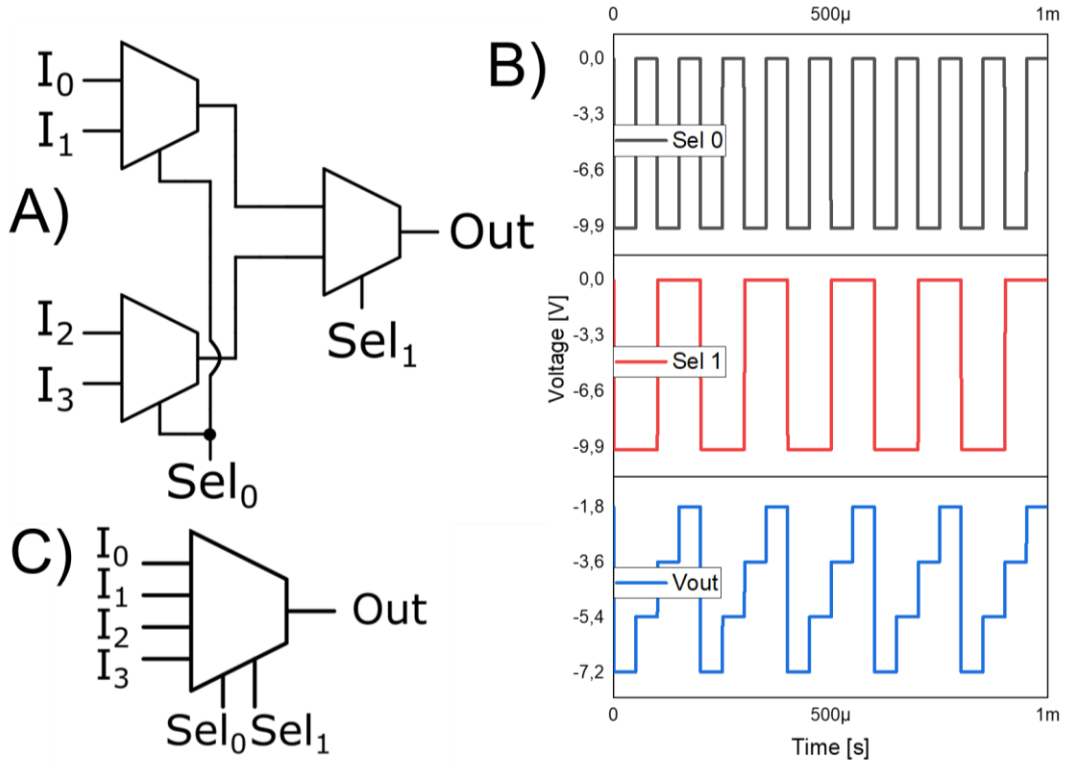


Figure 120. A) Four input multiplexer based on two input multiplexers, **B)** circuit simulation results and **C)** circuit symbol.

Demultiplexer structure had been designed following the same methodology than the multiplexer but with single input and multiple outputs, **Figure 121A** and **Figure 121C**. With select 0 as the LSB combined with select 1 each output is activated sequentially, **Figure 121B**.

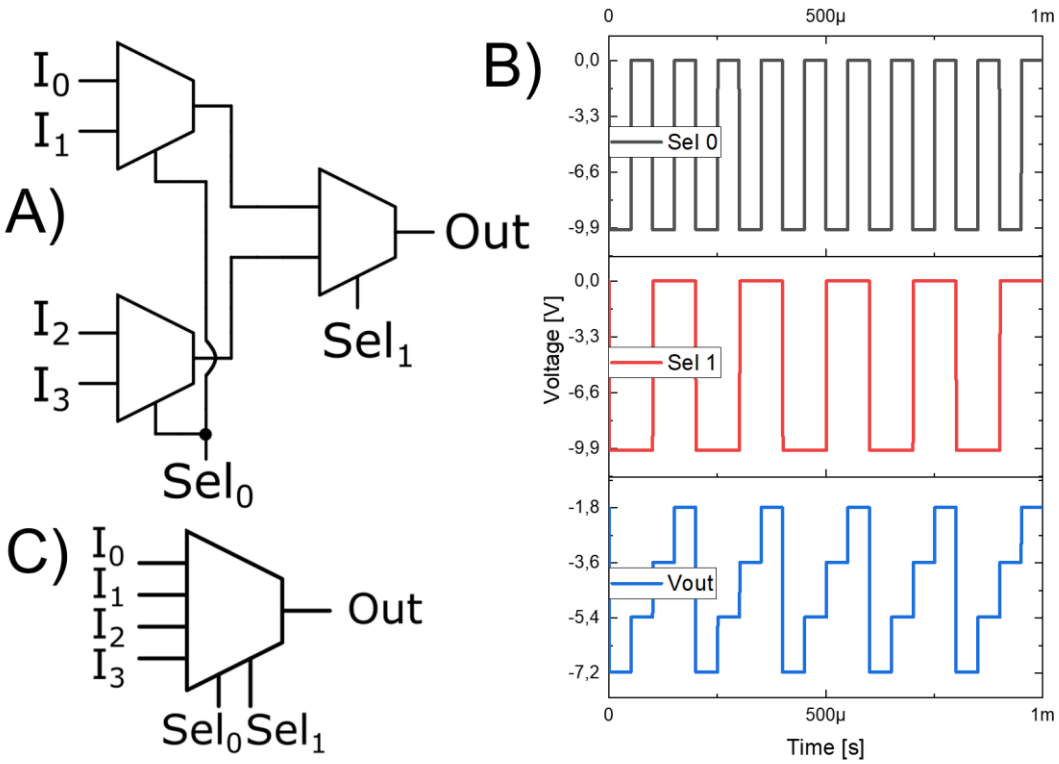


Figure 121. A) Four output demultiplexer based on two output demultiplexers, **B)** circuit simulation results and **C)** circuit symbol.

The final 16 bits RFID system schematic is composed by a 4 bit counter, one demultiplexer of four outputs, one multiplexer of four inputs combined with a PROM with special design for inkjet printing ID programming, **Figure 122A**. The tag had been simulated with an ID of 101000000000, showing the two differentiated states at the output with the expected code repeated two times, **Figure 122B**. The design is monotype, with only p-type transistor devices, and it is fully functional since the resulting output is around half of the supply voltage. Operating frequency of this devices is not clear since the AC model have not been developed for the moment.

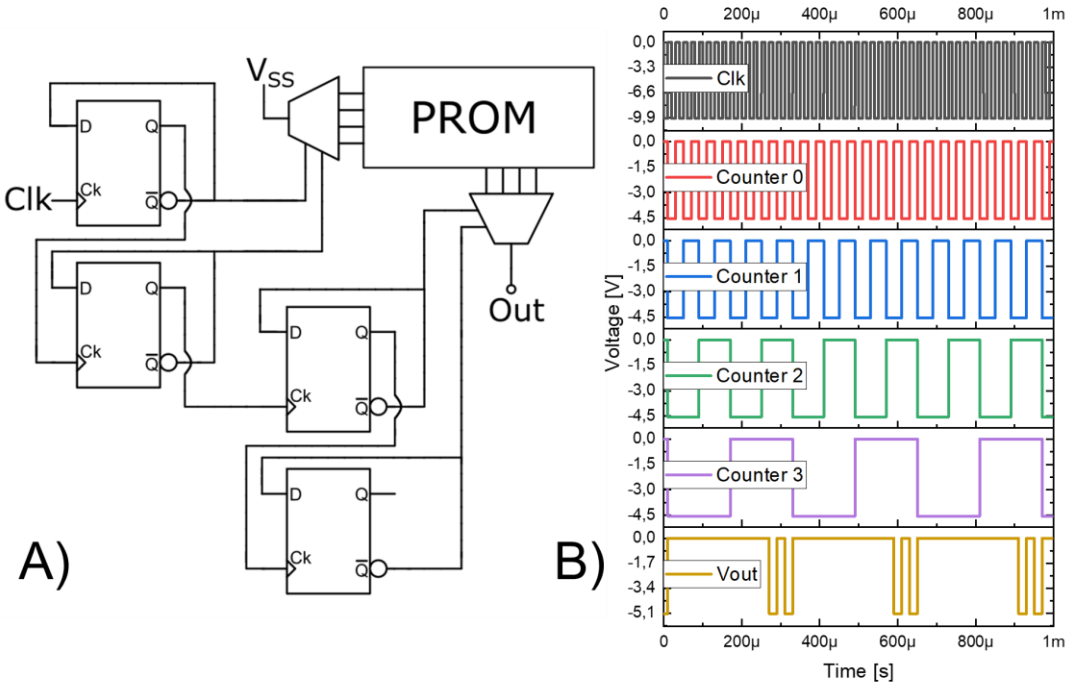


Figure 122. A) Final schematic of 16 bits RFID and **B)** Simulation of the final system.

The decision between two different approaches: reducing the number of transistor or have good reliability have affected to the different sub-circuits designed and simulated. This selection had been influenced by the low data available that does not allow the development of a reliable OTFT model making the risk of device minimization step very high. For this first version of RFID tag, a more conservative perspective had been adopted with focus on the system proper work.

6.4 RFID tag layout design

With the optimized NAND gate dimension obtained, a basic cell had been designed to be implemented in the layout of the RFID tag. The distribution of the contacts in an example with pads can be seen in **Figure 123**.

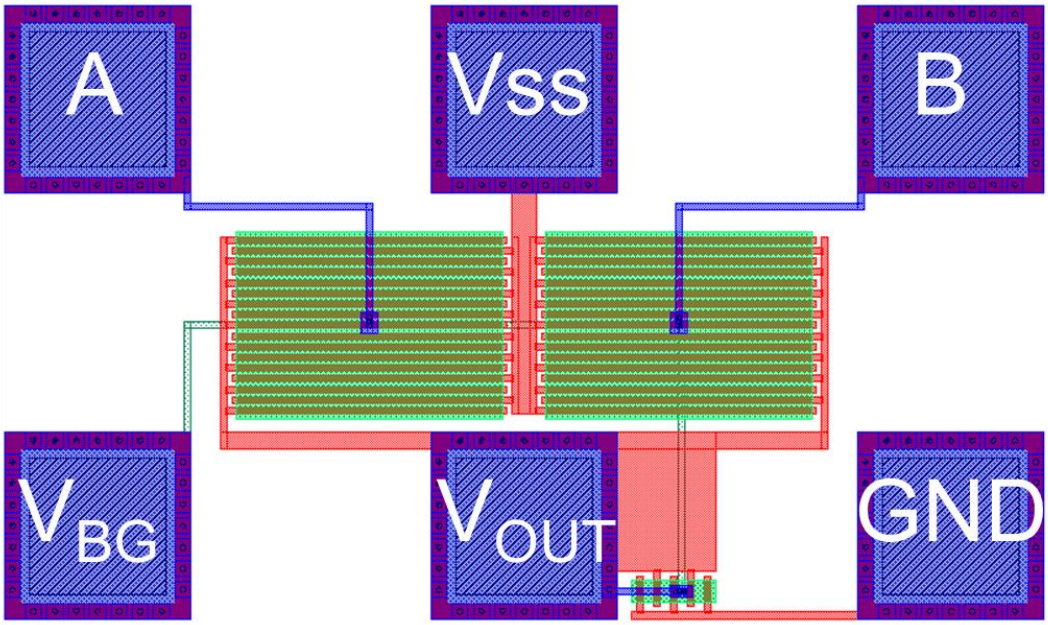


Figure 123. NAND gate layout with pads distribution.

Based on the NAND logic gate, the D- type Flip Flop is implemented with the appropriated connection between the five NAND gates that configurates it. All the inputs/outputs are identified in the pads incorporated for the testing in **Figure 124**.

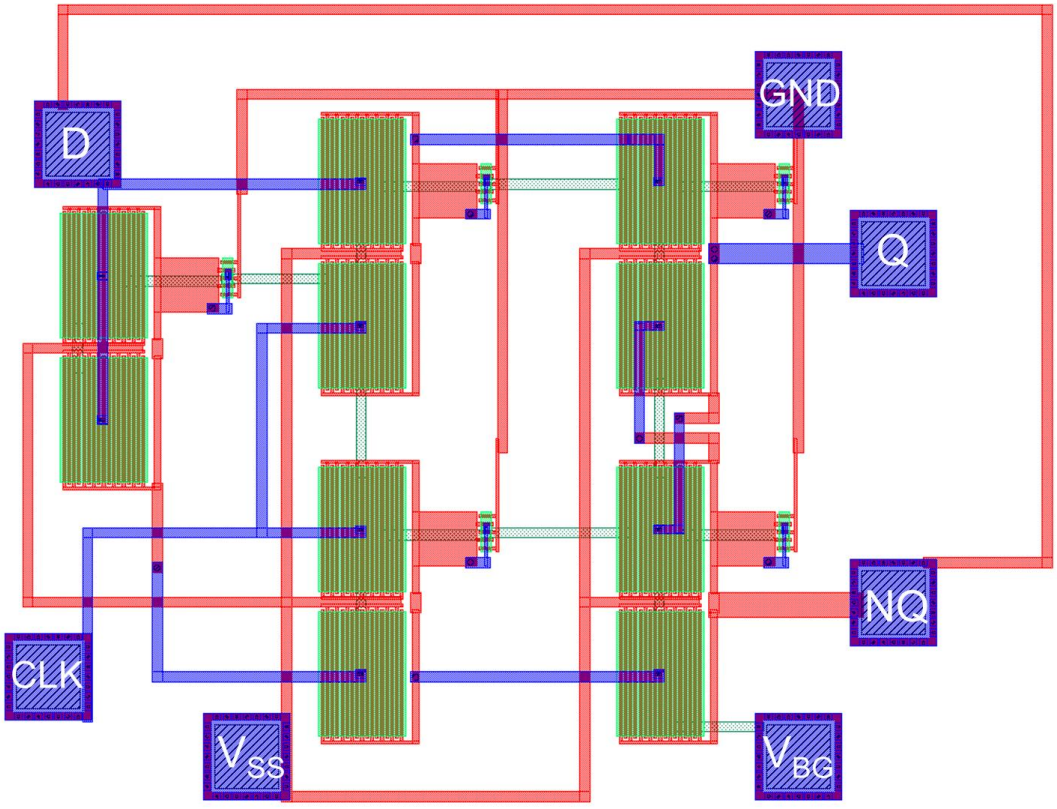


Figure 124. D-type Flip-Flop layout with pads distribution.

With the D-type Flip-Flop implemented, a 2-bit counter had been designed concatenating 2 Flip-Flops, **Figure 125A**. Same methodology for a 4-bit counter with 4 Flip-Flops had been done with two 2 bits counters concatenated to obtain the final 4 bit counter **Figure 125B**, the layout is distributed with different pads to being used as test points, plus the supply of each sub counter had been separated in order to test the circuit in small parts. Each counter has in the test pads the input/output definition.

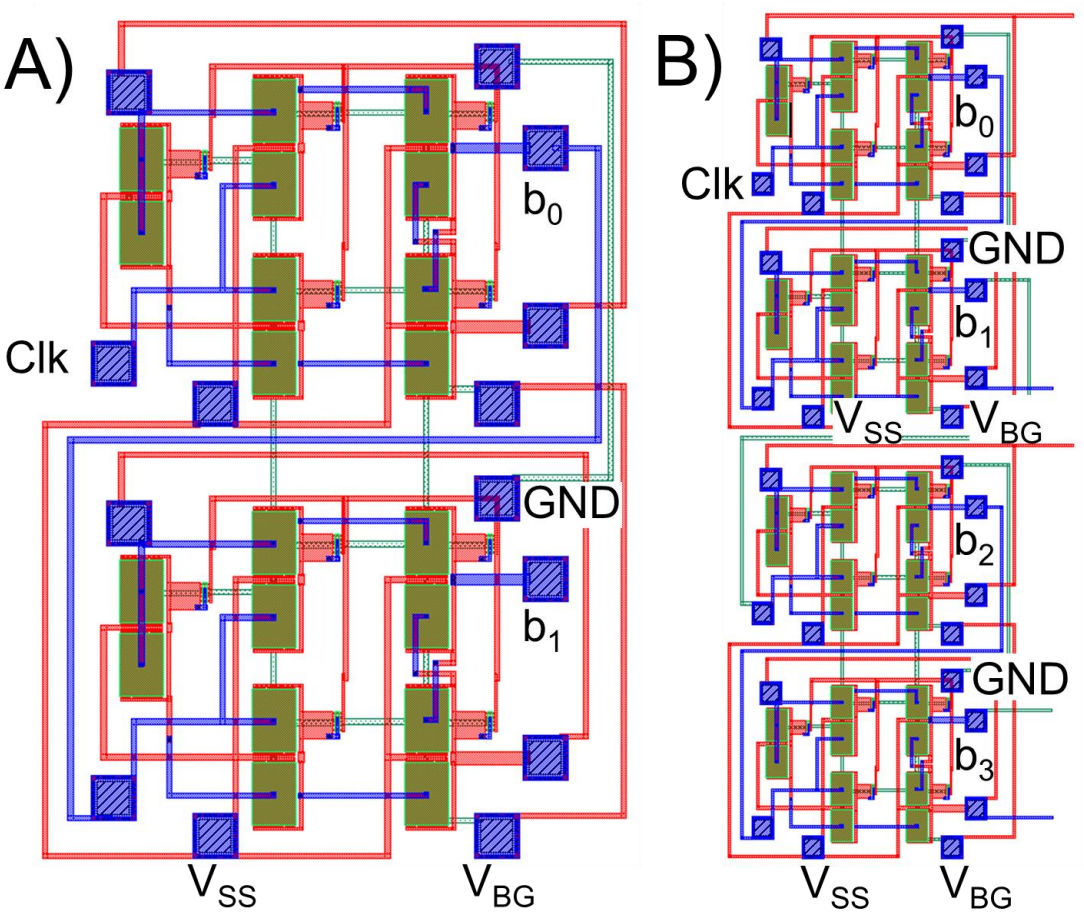


Figure 125. A) 2-bit counter layout and **B)** 4-bit counter layout.

Multiplexer and demultiplexer had been done with the same layout since one is the mirror representation of the other. The layout representation has started with a 2-input multiplexer, can be seen in **Figure 126A** with the test points pinpointed, to be latter combined with three 2-input multiplexer that generates a 4-input multiplexer, shown in **Figure 126B** with the test points marked.

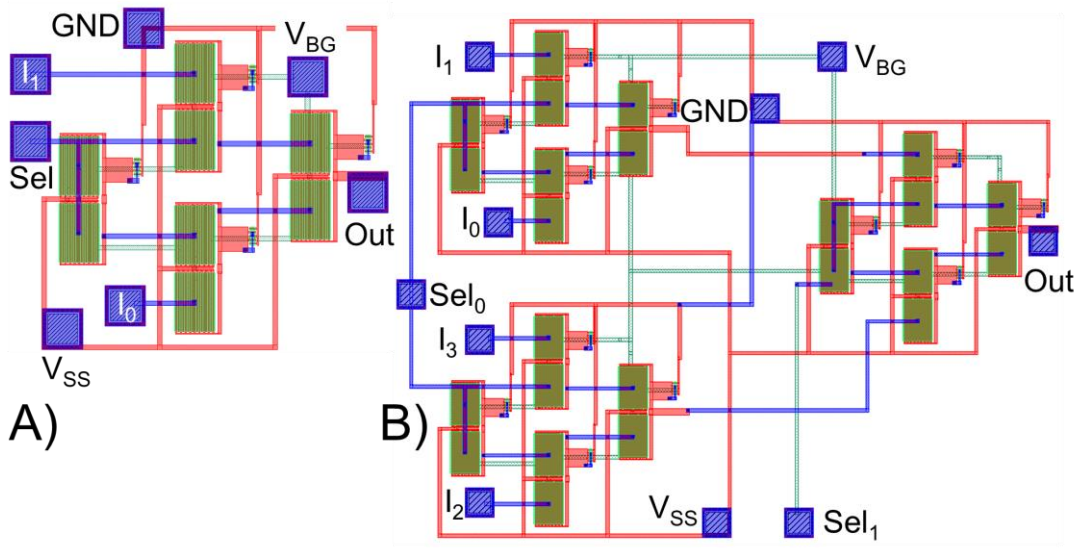


Figure 126. A) 2-input multiplexer layout and **B)** 4-input multiplexer layout.

Some auxiliar structures had been incorporated in order to make functional the tag. A ring oscillator based on 7 concatenated inverters will generate the clock signal for the tag, **Figure 127A**. Moreover, a printable PROM had been incorporated which have some predefined code and can be modified through an inkjet printer using conductive ink. An auxiliar row of memory structures had been introduced in order to facilitate the calibration of the inkjet printer in the programming step. The outputs of the demultiplexer are connected to each row while the inputs of de multiplexer are connected to each column as shown in **Figure 127B**.

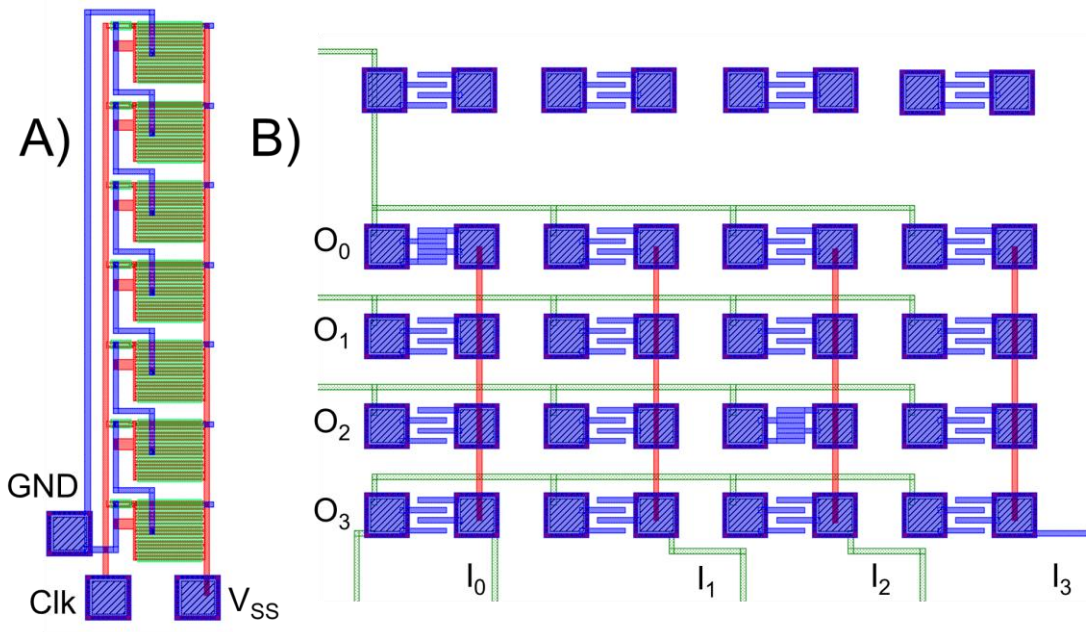


Figure 127. A) 7 stage ring oscillator and **B)** Inkjet PROM.

The final RFID tag is implemented with the different subsystems combined and the appropriated connections. Two versions had been done implementing the two different clock generation approaches, **Figure 128A**, shows the layout of the complete RFID tag with internal clock generation while, **Figure 128B**, is implemented with an external clock.

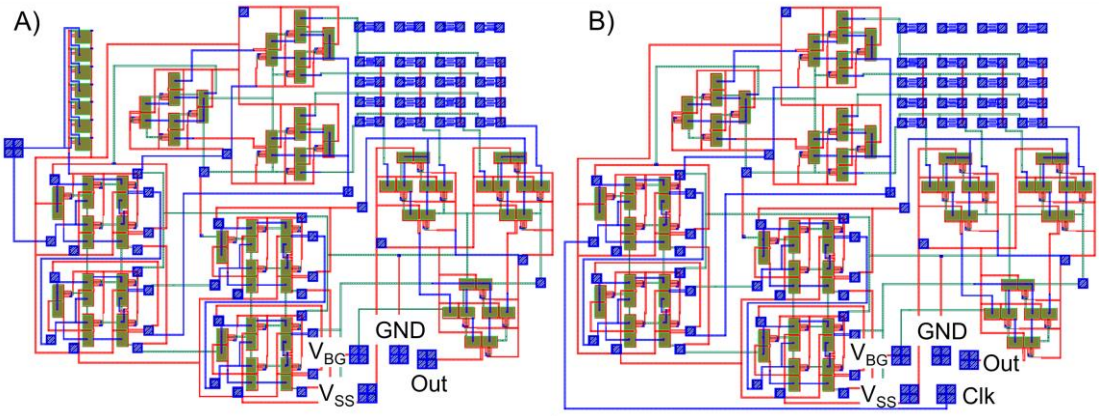


Figure 128. A) 16-bit RFID system layout with internal clock and **B)** 16 bit RFID system layout with external clock.

The final layout involves a total number of devices ranging from 146 OTFT with the internal clock generator, and 132 OTFT with the external clock signal. The total size of a single design is around 63 mm^2. Transistor number and mostly tag size can be optimized in order to make the integration level higher achieving more circuits in the same area, but since this is a first version the option of having multiple test points and an easy way to differentiate between the different subcircuits allows us a better understanding on how the circuit works.

All the circuits had successfully passed the DRC and LVS steps in order to check and correct any issues that could appear with this semiautomatic pick and place done. With the few current information about the manufacturing process and the resulting devices, the parasitic extraction step is not possible to be performed and had been skipped going with the design presented to the Tape out step. A full design of the wafer can be seen in **Figure 41**.

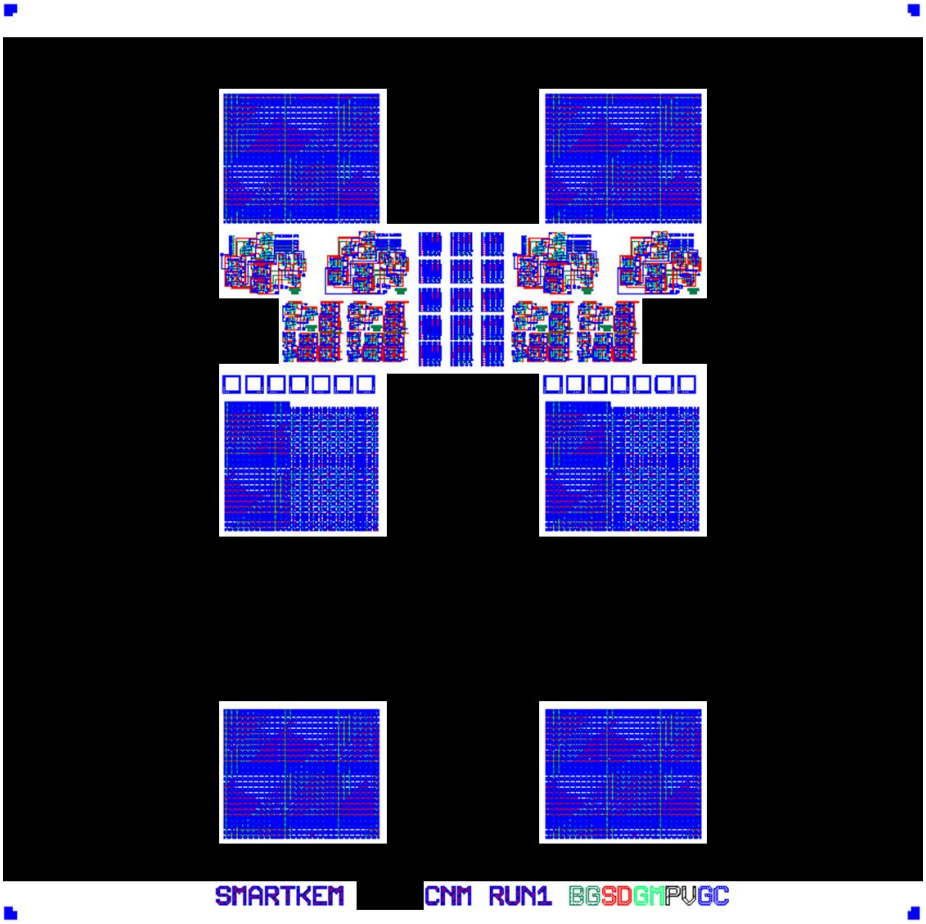


Figure 129. Run layout with 4 large dual gate OTFT in the sides complemented with the two central arrays with individual transistors and NAND gates. DRC structures and technology validators are incorporated together with dummy hybridization pads and circuits for testing.

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7 Conclusions

Organic electronics have demonstrated being a very promising technology since it provides some key advantages compared to silicon-based conventional technologies thus allowing for disposable health tags, wearables and IoT flexible sensors, among other applications. PDKs are an indispensable tool in the world of silicon-based circuits allowing the quick and scalable design procedure in order to predict the performance and behaviour of the system before the manufacturing step. This approach has started to be successfully implemented in OE field in order to speed up an appropriated development of the technology.

Most of the electronic systems published to this day have been fabricated without any simulation step due the simplicity of the circuit or the unavailability of simulation models. Also, the very quick and low-cost of the prototype fabrication, easily allows multiple iterations of the system thus permitting the optimization based on empiric results. Despite of that, the trial-and-error method is not an option for an industrial scale-up and the use of an organic PDKs is becoming a more popular option for system design in the organic community. This will allow the optimization of the circuits achieving more robust and reliable systems required for the development of more complex circuits. Since organic electronics is a very heterogeneous field, including large diversity of fabrication technologies, materials formulations and also silicon die hybridization procedures, the need for such tools has becomes crucial. However, today there is no EDA tool that can cover all the required aspects, from the model generation through the device simulation, parasitic extraction and circuit optimization to the final layout implementation causing researchers to work using multiple options.

The main objectives of this thesis includes device characterization, modeling and layout design based on organic devices complemented with an automatic PDK have been amply achieved, despite of the fact that the RFID tag

characterization have not been performed due to delays in manufacturing. Nevertheless, the simulation and design of complex circuits have been demonstrated. All the other sub-objectives, that involves: the elaboration of automatic methodologies and tools, the study of the model parameter variability, the development of an industrial compact model, the study of alternative robust designs and finally the development of analog and digital circuits, had been accomplished with a high level of automatization allowing a quick evolution of the work done.

In this thesis, we have reported a general view of the available Organic PDKs, allowing an easy comparison between them, combined with an analysis in the implementation of the models used and their characteristics. Moreover, most relevant circuits simulated and fabricated had been classified and a ring oscillator benchmark presented. Based on the available PDKs in the OE field combined with the organic technologies available for manufacturing, the decision to develop a more appropriated PDK was taken. Taking advantage of the institute equipment and the team knowledge, the PDK developed within this work had been doted of multiple automatic methodologies to follow the future evolution of the OE devices. Based on the automation part, improvements in the model with parameter variability, ambient conditions and degradation had been incorporated to the compact model presenting the first industrial model of the OE field.

With the automatization setup, a huge number of devices had been characterized and modelled, a work never done before in this field at this scale, obtaining very important information about this type of devices and their parameter variability.

Using the PDK developed, a 16-bit RFID tag had been simulated, optimized and designed pursuing to be one of the cheapest RF tag implementations and thus allowing the implementation of this technology to all type of products and giving the costumers new ways to interact in their everyday life.

The State of the Art chapter offers a detailed introduction on the field from a device and circuit perspective, with the different materials and fabrication techniques that are usually involved to manufacture the multiple circuits presented. Combined with an introduction to the system automation and their benefits and an overview of the PDK status in the OE field taking into account the models, tools and some of the simulated circuits.

Layout Design chapter shows the two freeware software tools used for the device and circuit design and the implementation of multiple PCells including its use to automatically generate arrays of devices and circuits for the characterization step. This procedure had already been implemented in the two layout editors used for different technologies.

The model generation had been presented in the Device Modelling chapter where an overview of characterization and modelling techniques have been

introduced, and the automatic characterization system working principals explained, allowing the report generation and model generation steps. These results had been applied to OTFT, where the parameters extraction had been detailed and the DC model generation exposed. The OTFT AC behaviour had been also studied with a complete work about the parameters extraction to be implemented in the Verilog model. A study of the parameter variability on organic devices is exposed.

Device Simulation chapter introduces the use of EDA tools for the device simulation and the implementation of the industrial model generated. The different studies done for the development together with the device and some circuit simulations are shown demonstrating that the classic EDA tools can be adapted to this new technology and take advantage of it. Moreover, robust design study is done with dual threshold device for the maximization of the gain in an inverter circuit.

Using all the potential of the PDK developed, in the last chapter about RFID System Design, an introduction to the RFID technology is done combined with the multiple architectures that can be implemented to make an RFID tag. Based on the most optimal and robust logic gate, simulation of the different parts had been performed in order to obtain a final reliable tag. The final layout of the 16-bit RFID tag is presented together with all the subcircuits that configures it.

As a summary, this thesis dissertation is a strong contribution in the long way required for the industrialization of the organic electronics technology. The different methodologies and resources proposed combined with the knowledge generated based on the device characterization can be considered as an outstanding result of this thesis work, together with the final 16 bits RFID tag that can provide a real change in the everyday life of the costumers, due the low cost that it is expected to have.

7.1 Outlook

In the near future, different challenges need to be solved for a proper development of the organic electronic technologies. First of all, there is a lack of a stable processing of the devices since they are continuously improving manufacturing, resulting in better devices with improvements coming from the fabrication techniques or the materials. This situation produces that the models generated gets out of date in a very short period of time. The use of BB or GB models with a defined automatized methodology can provide a good solution for these non-stabilized fabrication procedures. Variability and aging have not been widely studied, few publications were reported in this field, critical for the commercialization step, since the organic materials use to have a shorter lifetime than inorganic ones.

The unavailability of full commercial organic PDKs is related to the same reason than the model generation issue. When the fabrication process start being stable the EDA software companies will invest more efforts into the OE technology. The development of new tools will be required since organic electronics shows new and exciting advantages which will allow to complement silicon technologies, not compete with them. With the adoption of PDKs in OE, complex circuits will start to become common, allowing the development of new products focused on low power and low cost, creating new markets and services.

With these perspectives, and the emerging of the first OE foundries, it is expected to expand the methodologies developed in this thesis to other manufacturing processes allowing more accurate models that will bring the simulation of more and more complex systems to the Organic Electronics field.

Some issues remain pending on the RFID system designed such as the integration of the modulator and the rectification steps for achieving a complete passive tag. In the near future, CRC will be included in the tag ID and the Pure Aloha anticollision system also, allowing the lecture of multiple tags in the same area.