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Low-Power High-Resolution ΔΣM for Next Generation Space Analog-to-Digital Converters

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Memòria de Tesi
presentada per optar al títol de

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Francesc Serra-Graells, Professor Titular del Departament de Microelectrònica i Sistemes Electrònics, Universitat Autònoma de Barcelona, i Michele Dei, Department of Information Engineering, Università di Pisa,

Certifiquen

que la Memòria de Tesi *Low-Power High-Resolution ΔΣM for Next Generation Space Analog-to-Digital Converters* presentada per Alejandro Suanes Pérez per optar al títol de Doctor en Enginyeria Electrònica i de Telecomunicació s'ha realitzat sota la seva direcció a Institut de Microelectrònica de Barcelona pertanyent al Centro Nacional de Microelectrónica del Consejo Superior de Investigaciones Científicas i ha estat tutoritzada en el Departament de Microelectrònica i Sistemes Electrònics de la Universitat Autònoma de Barcelona (UAB).

Directors	Francesc Serra-Graells	.....
	Michele Dei	.....

....., a ..... de ..... de .....

To those I hold in my brightest memories.

Resum

El principal objectiu d'aquesta tesi doctoral és el disseny d'ADCs de baix consum i alta resolució de tipus $\Delta\Sigma$ per a aplicacions d'espai, tot i que les contribucions són vàlides per a escenaris de sensat de propòsit general on es requereix un gran rang dinàmic. L'estratègia $\Delta\Sigma$ s'ha escollit com a punt de partida degut al seu alt rendiment i fiabilitat. En particular, les implementacions amb capacitats commutades (SC) són d'especial interès en el treball presentat, les quals es construeixen mitjançant l'ús de nous circuits.

Amb la intenció de definir el procés d'optimització i de facilitar al dissenyador la realització de les tasques tant com sigui possible, s'ha desenvolupat una metodologia de disseny basada en models matemàtics. A més, aquesta metodologia s'han combinat amb tècniques de disseny especials per incrementar la robustesa dels circuits CMOS enfront de la radiació.

Una limitació important en dissenys d'ADCs de baixa freqüència i alta resolució és el soroll *flicker*. Per prevenir la degradació de la resolució causada per aquest efecte, es proposa un mecanisme de cancel · lació de soroll *flicker* mitjançant circuits de capacitats commutades. Aquesta modificació del modulador $\Delta\Sigma$ ($\Delta\Sigma$M), en conjunt amb altres noves tècniques i circuits, permeten obtenir una bona optimització del consum de l'ADC i mantenir les seves prestacions.

L'arquitectura $\Delta\Sigma$M Multi-bit proposta s'ha implementat en els tres nodes de tecnologies CMOS 180 nm, 65 nm i 22 nm. El propòsit d'aquest estudi de portabilitat implementacions és descobrir els reptes de disseny que suposa la migració tecnològica, permetent així validar la metodologia de disseny i explorar els potencials beneficis de l'escalat, tant tecnològic com de la tensió d'alimentació.

Un $\Delta\Sigma$M SC de 0.8mW 50kHz 94.6dB-SNDR lliure de *bootstrapping* i amb cancel · lació de soroll *flicker* s'ha fabricat en una tecnologia CMOS de 180 nm i s'ha caracteritzat experimentalment. Les mesures mostren una millora en l'estat de l'art de la FoM en comparació amb convertidors de característiques similars publicats a la literatura. Els resultats també mostren una baixa variabilitat entre diferents mostres, demostrant la robustesa del disseny enfront a la tecnologia. A més, la robustesa d'aquests xips enfront de radiació s'ha comprovat mitjançant un test de dosi total de radiació. Els resultats mostren que l'ADC $\Delta\Sigma$M pot suportar com a mínim nivells de radiació adequats per a la majoria de missions espacials.

La implementació CMOS de 65 nm del $\Delta\Sigma$M incorpora el suport digital compost pel filtre delmador i un perifèric per a comunicacions per bus, i s'ha integrat com un bloc IP per un nucli digital RISC-V. Aquest disseny s'està fabricant en l'actualitat.

Una altra contribució d'aquest treball és el desenvolupament d'una nova arquitectura de $\Delta\Sigma$M que incorpora funcions de control de guany automàtic (AGC) fent ús de la tècnica *analog floating-point*. Un ADC $\Delta\Sigma$ de tipus *Floating Point* amb AGC lliure de distorsió i 1.1mW 50kHz 100dB-DR també s'ha fabricat en un node CMOS de 180 nm i s'ha testat experimentalment. Els resultats obtinguts mostren el correcte ús del mecanisme *floating-*

point, obtenint així una extensió en el rang dinàmic de l'ADC. També s'ha desenvolupat un sistema de test específic per tal de tancar el llaç de control AGC mitjançant processat digital sintetitzat en una plataforma FPGA.

Resumen

El principal objetivo de esta tesis doctoral es el diseño de ADCs de bajo consumo y alta resolución del tipo $\Delta\Sigma$ para aplicaciones de espacio, aunque las contribuciones son válidas para cualquier escenario de sensado de propósito general donde se requiera un gran rango dinámico. La estrategia $\Delta\Sigma$ ha sido escogida como punto de partida debido a su alto rendimiento y fiabilidad. En particular, las implementaciones con capacidades conmutadas (SC) son de especial interés en el trabajo presentado, las cuales se construyen mediante el uso de novedosos circuitos CMOS.

Con la intención de definir el proceso de optimización y facilitar al diseñador la realización de tareas tanto como sea posible, se ha desarrollado una metodología de diseño basada en modelos matemáticos. Además, se ha combinado esta metodología con técnicas de diseño especiales para incrementar la robustez de los circuitos CMOS frente a la radiación.

Una limitación importante en diseños de ADCs de baja frecuencia y alta resolución es el ruido *flicker*. Para prevenir la degradación de la resolución causada por este efecto, se propone un mecanismo de cancelación de ruido *flicker* mediante circuitos conmutados. Esta modificación del modulador $\Delta\Sigma$ ($\Delta\Sigma$M), junto a otras nuevas técnicas y circuitos, permiten obtener una buena optimización del consumo del ADC y mantener sus prestaciones.

La arquitectura $\Delta\Sigma$M Multi-bit propuesta se ha implementado en los tres nodos de tecnología CMOS 180 nm, 65 nm y 22 nm. El propósito de este estudio de portabilidad es descubrir los retos de diseño que supone la migración tecnológica, permitiendo así validar la metodología de diseño y explorar los beneficios potenciales del escalado tanto tecnológico como de la tensión de alimentación.

Un $\Delta\Sigma$M SC de 0.8mW 50kHz 94.6dB-SNDR libre de *bootstrapping* y con cancelacion de ruido *flicker* ha sido fabricado en una tecnología CMOS de 180 nm y caracterizado experimentalmente. Las medidas muestran una mejoría en el estado del arte de la FoM en comparación con otros convertidores de características similares publicados en la literatura. Los resultados también muestran una baja variabilidad entre diferentes muestras, demostrando la robustez del diseño frente a tecnología. Además, la robustez de estos chips frente a radiación ha sido comprobada mediante un test de dosis total de radiación. Los resultados muestran que el ADC $\Delta\Sigma$M puede soportar como mínimo niveles de radiación adecuados para la mayoría de misiones espaciales.

La implementación CMOS de 65 nm del $\Delta\Sigma$M incopora el soporte digital, compuesto por el filtro diezmador y un periférico para comunicaciones por bus, y ha sido integrado como un bloque IP para un núcleo digital RISC-V. Este diseño se está fabricando actualmente.

Otra contribución de este trabajo es el desarrollo de una nueva arquitectura $\Delta\Sigma$M que incorpora funciones de control automático de ganancia (AGC) basada en el concepto *analog floating-point*. Un ADC $\Delta\Sigma$ de tipo *Floating Point* con AGC libre de distorsión y 1.1mW 50kHz 100dB-DR también se ha fabricado en un nodo CMOS de 180 nm y testeado experimentalmente. Los resultados obtenidos muestran un correcto uso del mecanismo *floating-point*, obteniendo así una extensión en el rango dinámico del ADC. También se

ha desarrollado un sistema de test específico con el fin de cerrar el lazo de control AGC mediante procesado digital sintetizado en una plataforma FPGA.

Abstract

The focus of this PhD thesis is placed in the design of low-power high-resolution ΔΣADCs intended for space applications, but contributions are valid for any general-purpose sensing scenarios where a wide dynamic range is required. The ΔΣ strategy is chosen because of its high performance and reliability. In particular, switched-capacitor implementations are of interest in this work, which are realized by making use of novel CMOS circuits.

In order to define the optimization process and facilitate the designer's tasks as much as possible, a mathematical framework and methodology is developed. In addition, special design techniques are also combined with this methodology with the intention of increasing the robustness of the CMOS circuits against radiation.

One important limiting factor in low-frequency high-resolution ADCs is flicker-noise. In order to prevent resolution loss caused by this effect, a switched-capacitor flicker-noise cancellation mechanism is proposed. This modification of the ΔΣmodulator (ΔΣM), in conjunction with other novel circuits, allows for a good power optimization of the ADC while keeping its high performance.

The proposed Multi-Bit ΔΣM architecture is implemented in the three CMOS technology nodes 180 nm, 65 nm, and 22 nm. The aim of this portability study is to show the design challenges of technology migration, to check the validity of the design methodology, and to explore the potential benefits of both the technology and supply voltage downscaling.

A 0.8mW 50kHz 94.6dB-SNDR bootstrapping-free SC ΔΣM ADC with flicker-noise cancellation is fabricated in standard 180 nm CMOS technology and experimentally characterized. The measurements show an improvement of the state-of-the-art FoM compared to other published SC ΔΣM realizations. These results also present very low variability between samples, demonstrating the robustness of the design technique versus technology. Furthermore, the robustness against radiation has been also measured via total irradiation dose tests. The results show that the ΔΣM ADC can withstand an irradiation dose level rated for most space missions.

The 65 nm CMOS ΔΣM design incorporates a digital backend, including the decimation filter and the bus peripheral, and it is integrated as an IP block for a digital RISC-V core. This design is currently under manufacturing.

Another contribution of this work is the development of a new ΔΣM architecture incorporating automatic gain control (AGC) capabilities based on the analog floating-point concept. A 1.1mW 50kHz 100dB-DR Floating-Point ΔΣM ADC with distortion-less AGC has also been fabricated in standard 180 nm CMOS technology and experimentally tested. The measurement results demonstrate the correct operation of the Floating-Point mechanism, achieving the desired dynamic-range extension. A specific test system is also developed in order to close the AGC loop through digital processing synthesized in a FPGA platform.

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I want to thank my friends for all the good times they have given me; some needed respites during all these years.

Finally, I want to thank my family for always being there, no matter when or where, and expecting nothing in return.

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List of Acronyms

ΔΣM delta-sigma modulator

ADC analog-to-digital converter

AFP Analog Floating Point

AGC automatic gain control

AM amplitude modulated

AMBA Advanced Microcontroller Bus Architecture

ASIC application specific integrated circuit

AXI Advanced eXtensible Interface

BEC bubble error correction

CDS correlated double sampling

CIC cascaded integrator-comb

CIFB cascade-of-integrators feed-back

CMFB common-mode feedback

CMOS complementary metal-oxide semiconductor

CPU central processing unit

CT continuous-time

DAC digital-to-analog converter

DC direct-current

DEM dynamic element matching

DNL differential non-linearity

DR dynamic range

DRC design rule checker

DSP digital signal processor

DT discrete-time

DUT device under test

DWA dynamic weighted averaging algorithm

EMI electromagnetic interference

ENOB effecitive number of bits

ESA European Space Agency

ESTEC European Space Research and Technology Centre

FIFO first-in, first-out

FIR finite impulse response

FoM figure-of-merit

FPGA field programmable gate array

FS fullscale

GBW gain-bandwidth product

HDL hardware-description languages

IC integrated circuit

ICT information and communications technology

IEEE Institute of Electrical and Electronics Engineers

INL integral non-linearity

IoT Internet-of-Things

IP intelectual property

kTC Jonhson-Nyquist capacitive noise

LDO low-dropout regulator

LLT logic level translator

LSB least significant bit

LVS layout versus schematic

MASH multi-stage noise-shaping

MBU multiple-bit upset

MCU multiple-cell upset

MiM metal-insultator-metal

MoM metal-oxide-metal

MOS metal-oxide semiconductor

MOSFET metal-oxide semiconductor field-effect transistor

NMOS N-channel MOS

NTF noise transfer function

OpAmp operational amplifier

OSR oversampling-ratio

OTA operational transconductance amplifier

PC personal computer

PCB printed circuit board

PGA programmable gain amplifier

PL programmable logic

PMOS P-channel MOS

PS processing system

PSD power spectral density

PVT process, supply voltage and temperature

RISC reduced instruction set computer

rms root-mean-square

RTL register transfer language

SAR successive approximation register

SC switched-capacitor

SDR signal-to-distortion ratio

SEB single event burnout

SEDR single event dielectric rupture

SEE single event effect

SEFI single event functional interrupt

SEGR single event gate rupture

SEHE single event hard error

SEL single event latch-up

SESB single event snap-back

SET single event transient

SEU single event upset

SFDR spurious-free dynamic range

SNDR signal-to-noise-to-distortion ratio

SNR signal-to-noise ratio

SOA switched-OpAmp

SoC system-on-chip

SQNR signal-to-quantization-noise ratio

SR slew rate

STF signal transfer function

SVMA switched variable-mirror amplifier

TID total ionizing dose

TMR triple modular redundancy

TNID total non-ionizing dose

VLSI very large-scale integration

VMA variable-mirror amplifier

Introduction | 1

1.1 Motivation

The current evolution of the information and communications technology (ICT) has led into the convergence of many traditional fields, such as real-time analytics, health monitoring, machine learning, sensory systems, embedded systems, etc..., into complex applications which share data with one another over some kind of network and even the Internet. This is the so called Internet-of-Things (IoT) paradigm, which is currently the focus of the industry and its expanding at a high rate [1]–[3].

This growing market demands sensors with increasingly better performance (e.g. resolution), increased autonomy (i.e. low power consumption), and high-speed capabilities. A key component in any sensory system is the analog-to-digital converter (ADC), since its performance often determines the capabilities of the whole sensory system. In many applications, the ADCs are integrated along with all the analog front-end and digital back-end in the same chip. This is usually known as an application specific integrated circuit (ASIC) [4], [5], and some may even integrate the sensors themselves when possible [6], benefiting from increased compactness and robustness. This is one of the many reasons why developing state-of-the-art ADCs in standard complementary metal-oxide semiconductor (CMOS) technologies is attractive.

The continuous node downscaling in the CMOS technology results in reduced transistor channel length and supply voltage. Despite its inherent benefits, such as lower power consumption and higher speed, it poses increasingly challenging issues in the design of ADCs. This is due to the degradation of the transistor analog performance, increased process mismatch, and reduction of the available voltage range [7].

Currently, the focus research trends and highest state-of-art figures belong to successive approximation register (SAR) ADCs, in the moderate-to-high-resolution range [8]–[18], and continuous-time (CT) delta-sigma modulator ($\Delta\Sigma$M) ADCs, in the high-resolution range [19]–[33]. Despite having a lower performance with regard to their CT counterpart, switched-capacitor (SC) $\Delta\Sigma$Ms are also attractive because of their high-robustness to technology mismatch and the reduced design complexity [34]–[47]. Many SAR and CT $\Delta\Sigma$M designs are also able to achieve such high-performance values because of the

employment of on-line or off-line calibration techniques, at the cost of increased design complexity and manufacturing costs. Since calibration-free circuits are of interest for most remote smart-sensing applications, this is another reason why SC $\Delta\Sigma$Ms are an attractive choice.

The general design points of SC $\Delta\Sigma$Ms are well understood in the literature [48]. Nonetheless, different designs suffer from peculiar effects that must be carefully considered. For this reason, it is of interest to develop a design methodology in order to ease the design process to the engineer, and even automate some of the design tasks. This methodology should also be valid when migrating the design to different CMOS technology nodes, with special interest on high scalability. Moreover, having a properly described methodology is beneficial regarding the power optimization of the design, allowing for a better performance at a lesser design cost and time.

Another interesting subject is the fact that many sensors used in the industry often generate very weak signals. This is traditionally solved by a signal conditioning stage at the output of the sensor, which amplifies its signal to the appropriate ADC input range. In applications where the sensor signal undergoes large variations of its dynamic range (DR) this is typically handled by automatic gain control (AGC) systems. They make use of a programmable gain amplifier (PGA) at the sensor output controlled by the backend digital signal processor (DSP), which adjusts the PGA gain using feedback, to keep the signal range under control. Classic AGC applications make use of time constants, which adjust the trade-off between AGC sensitivity and response speed [49]. An interesting question arises when considering if this functionality can be incorporated in the ADC architecture itself, and what advantages it can enjoy versus classic AGC implementations.

Placing the focus on space applications, the same can be said about the necessity of ADCs. The space environment, however, is harsh to electronic systems due to the high levels of irradiated particles coming from different sources, the most notable the sun. For this reason, integrated circuits (ICs) intended for space missions require to be properly designed in order to be protected from many radiation effects that would put the application in danger. Incorporating these new design guidelines into the regular IC design flow and carrying out tests to check the effects of radiation on the chips is indeed an interesting topic.

All of the described factors contribute to the motivation of this PhD thesis. The work on the high-resolution ADCs for space missions, in the scope of the project funded by the European Space Agency (ESA)-European Space Research and Technology Centre (ESTEC) under the contract 4000124840/18/NL/MH denominated "***Lo**w-power **Hi**gh-resolution **Ra**d-hard ADCs for Space Applications (LOHIRA)*", provided the main contributions of this PhD thesis.

1.2 State-of-Art of High-Resolution ADC

In this section, the basic concepts and metrics of ADCs will be explained, in order to provide a basic background and understanding of analog-to-digital conversion. The understanding of these metrics will allow the classification of different ADCs types and architectures

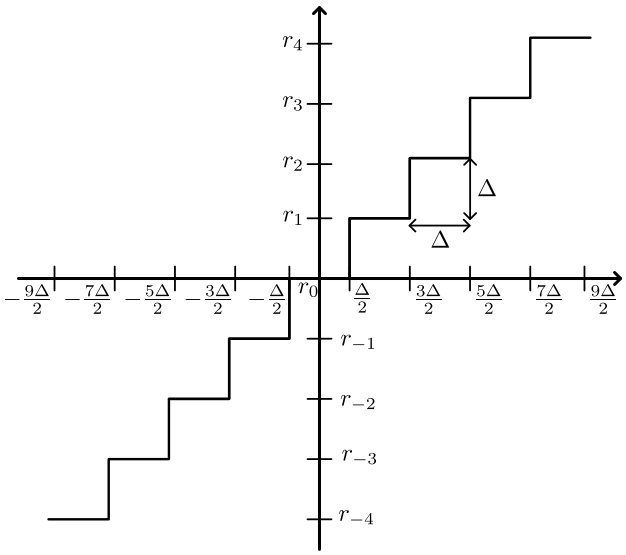

Figure 1.1 | Amplitude transfer function of an ideal uniform quantizer for a 9-level case.

based on a single figure-of-merit (FoM). This metric combines several performance and resource parameters into a single number for comparison purposes. Finally, a review of the ADC state-of-art and the most important ADC types is presented to give a good understanding of their strong and weak points and their suited applications.

1.2.1 Basic ADC Concepts and Metrics

Quantization Noise and ADC Resolution

The purpose of an ADC is to digitalize a continuous-time signal in a way so that data can be stored, processed, and communicated using digital systems. To achieve this purpose, the digitalization can be understood as a two-step operation: time-discretization and amplitude-discretization.

The most typical case of amplitude-discretization is uniform quantization [50], in which a set of equally spaced levels are defined. Non-uniform quantizers can also be used and may perform better depending on the application [51]. The transfer function of an ideal uniform quantizer is depicted in Fig. 1.1. The difference in amplitude between these levels is called the quantization step or least significant bit (LSB), and it is given by:

$$\Delta = \frac{\mathrm{FS}}{L-1} = \frac{\mathrm{FS}}{2^{\mathrm{N}}-1}, \tag{1.1}$$

where FS is the quantizer full-scale, or maximum peak-to-peak signal amplitude, L is the number of quantization levels, and N is the number of quantization bits, when the number of levels can be expressed as a power of 2, which is something usual.

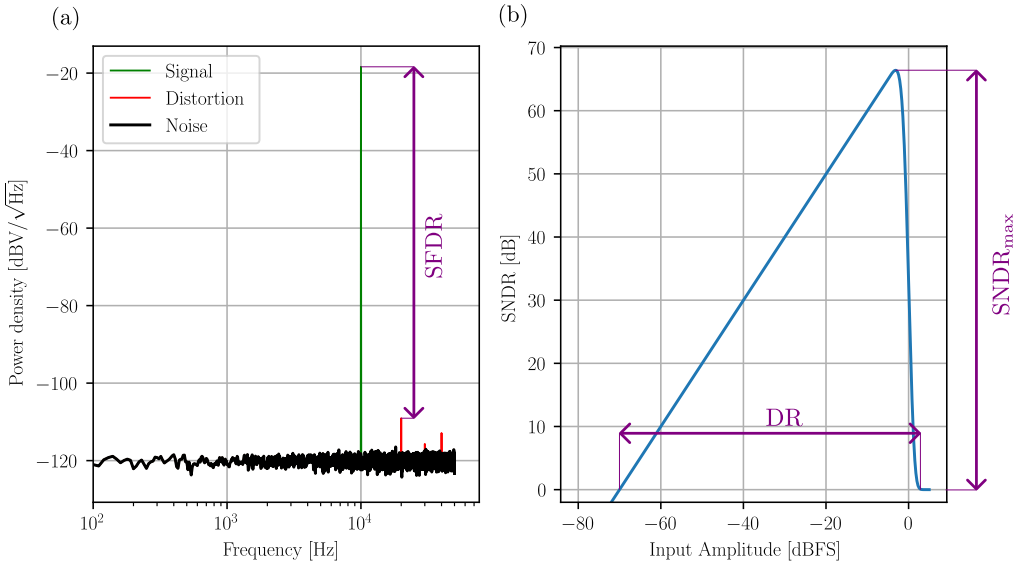

Figure 1.2 Example of an ADC PSD function (a) and a typical SNDR curve (b). Typical ADC parameters are also annotated in the graphs.

In an ideal quantizer, the maximum amplitude error committed by the quantization process is delimited to $\pm\Delta/2$. By making a series of assumptions about the input signal that usually hold true for common applications [52], [53], the quantization error, or quantization noise, can be modeled as a white noise process with a total power given by:

$$\mathrm{QN} = \frac{\Delta^2}{12}. \tag{1.2}$$

The maximum resolution of an ideal ADC, which basically consists on an ideal sampler and quantizer, is then given by the signal-to-quantization-noise ratio (SQNR), a ratio between the signal power and the quantization noise power. It can be computed using (1.1) and (1.2). The ADC input is assumed to be a pure harmonic signal, so its root-mean-square (rms) value is used to compute the signal power:

$$\begin{aligned} \mathrm{SQNR} &= \frac{\mathrm{FS}^2/8}{\mathrm{QN}} \approx \frac{3}{2}2^{2N}, \\ \mathrm{SQNR}\ [\mathrm{dB}] &= 6.02\mathrm{N} + 1.76\ [\mathrm{dB}], \end{aligned} \tag{1.3}$$

where it was assumed $2^{\mathrm{N}} \approx 2^{\mathrm{N}} - 1$, for $\mathrm{N} \gg 1$. Equation (1.3) states that each additional bit ideally increments the resolution by 6.02 dB.

When considering real ADCs, quantization noise is not the only error source degrading the resolution. Another term, the signal-to-noise ratio (SNR), encompasses all types of noise introduced by the ADC. Since the resolution might be measured at amplitudes other than the ADC full-scale, a more general expression replaces this term by the signal power

at any amplitude, S_{in}:

$$SNR = \frac{S_{in}}{QN + \sigma_n^2}, \tag{1.4}$$

where σ_n is the rms integrated power of all the in-band noise introduced by the ADC, with the exception of quantization noise.

Real ADCs also distort the input due to several non-linear circuital effects. Due to its deterministic nature, distortion is usually considered as a separate term as noise, and thus measured by its own metric, the signal-to-distortion ratio (SDR), defined as:

$$SDR = \frac{S_{in}}{\sigma_d^2}, \tag{1.5}$$

where σ_d is the total rms power of the frequency components located at multiples of the input tone, or harmonics.

Another used distortion metric is the spurious-free dynamic range (SFDR), which relates the input signal power to the power of the largest harmonic H_{max}. This term is defined as:

$$SFDR = \frac{S_{in}}{H_{max}}. \tag{1.6}$$

A metric taking into account all of the other measurements is the signal-to-noise-to-distortion ratio (SNDR), which includes all kind of error sources affecting the ADC resolution. For this reason, it is the most significant term when describing the effective resolution of an ADC:

$$SNDR = \frac{S_{in}}{QN + \sigma_n^2 + \sigma_d^2}. \tag{1.7}$$

Another common term is the DR, which describes the range of input power for which the sampled signal is above the error power level:

$$DR = \frac{S_{max}}{S_{min}}, \tag{1.8}$$

where S_{min} and S_{max} are the minimum and maximum input power values for which the SNDR is greater than 0 dB. For an ideal ADC this value is equal to the SQNR, but in real ADCs the DR is usually larger than the SNDR.

Finally, since it is typical to express the resolution as a number of bits, it is possible to obtain a definition similar to (1.3) but using the SNDR instead of the SQNR. This metric is called effecitive number of bits (ENOB), and it is defined as:

$$ENOB = \frac{SNDR - 1.76}{6.02}. \tag{1.9}$$

An example of typical ADC measurements is shown in Fig. 1.2. From the power spectral density (PSD) in Fig. 1.2a, the SFDR can be obtained by visual inspection, and the SNR, SDR, and SNDR can be computed by integrating the in-band power of the different elements. The SNDR in Fig. 1.2b is the result of computing the SNDR from the PSD

measurements at different input amplitudes. The maximum SNDR and the DR can be extracted from this graph by visual inspection.

There exist another kind of resolution metrics; static metrics, such as the differential non-linearity (DNL) and integral non-linearity (INL). These metrics aim to describe the resolution of an ADC by looking at deviations in the transfer function from the ideal. However, they cannot be applied to ADCs with memory such as ΔΣMs, since a static transfer function does not exist in this case. Dynamic metrics, such as the ones presented in this section, can be applied to any kind of ADC. Since the focus of this PhD thesis is the ΔΣM architecture, static metrics will not be discussed further.

Oversampling

The Nyquist Theorem states that, in order to be able to recover a signal from its discrete-time samples, the sampling frequency must be greater or equal than the Nyquist frequency, which is twice the value of the signal bandwidth [54]:

$$f_{\text{samp}} \geq f_{\text{nyq}} = 2\text{BW}. \tag{1.10}$$

While making $f_{\text{samp}} = f_{\text{nyq}}$ proves sufficient to avoid aliasing, there are some benefits that can be obtained from using a sampling frequency greater than f_{nyq}. This condition is called oversampling, and the oversampling-ratio (OSR) is defined as the ratio between the sampling frequency and the Nyquist frequency:

$$\text{OSR} = \frac{f_{\text{samp}}}{f_{\text{nyq}}}. \tag{1.11}$$

In (1.2), the quantization noise power was defined to be only dependent on the quantization step value, which in turn depends on the ADC fullscale (FS) and its number of bits/levels. The quantization noise power density, however, is dependent on the sampling frequency because the quantization noise power is equally distributed over all the range of discrete-domain frequencies:

$$\text{QN}_{\text{den}} = \frac{\text{QN}}{f_{\text{samp}}/2}. \tag{1.12}$$

The total in-band noise power can be found by integrating the noise density over the ADC bandwidth. In this case, the noise density is a constant over all the frequency range, so:

$$\begin{aligned} \text{QN}_{\text{ib}} = \text{QN}_{\text{den}} \cdot \text{BW} = \text{QN}\frac{f_{\text{nyq}}}{f_{\text{samp}}}, \\ \text{QN}_{\text{ib}} = \frac{\text{QN}}{\text{OSR}}. \end{aligned} \tag{1.13}$$

Therefore, the in-band noise power is inversely proportional to the OSR. This is graphically shown in Fig. 1.3, where the same noisy signal is sampled using a different OSR. It can be seen that, for an OSR larger than one, part of the noise power is distributed outside the defined bandwidth, reducing thus the in-band noise. The noise outside the bandwidth can be removed by using adequate digital filtering. This is also true for other noise sources

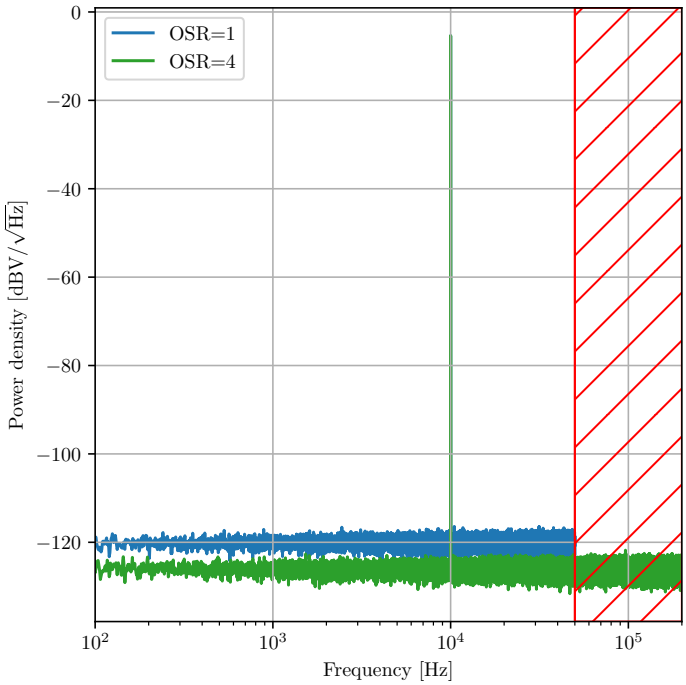

Figure 1.3 Example of oversampling on a harmonic signal with added white noise. The same signal is sampled at Nyquist rate (OSR=1) in blue and oversampled (OSR=4) in green. Red shadowed area is outside the bandwidth of interest.

that distribute equally over all the spectrum, e.g. Jonhson-Nyquist capacitive (kTC) noise, so they also benefit from oversampling at the cost of increased power consumption.

This mechanism is exploited in depth in some ADC architectures, such as $\Delta\Sigma$Ms, which make use of high oversampling ratios in addition to noise shaping transfer functions to reduce the in-band quantization noise even further [55]. Recent SAR ADCs are also incorporating noise shaping techniques to improve resolution, albeit using low OSR values [9], [10], [12], [17], [18]. This kind of ADCs are called "Oversampling ADCs", whereas traditional ones are called "Nyquist-rate ADCs".

ADC Figures-of-Merit

In Section 1.2.1, the most commonly used metrics were defined to help quantify the resolution of an ADC. Two other important ADC parameters are the power consumption, P_d, and the bandwidth, BW, usually expressed as the Nyquist frequency according to (1.10).

There exist many different applications for which uneven ADC requirements are needed. Some applications require extremely high resolution, others might require the sampling of signals with very large frequency and others might require the integration of many ADCs for multi-channeling purposes, requiring thus low power consumption. With this in mind, it is hard to tell if an ADC is better than another because the different performance metrics cannot be compared in a straight forward way. This is the motivation for the use of FoMs; to provide an useful metric to compare different ADCs and to be pushed to the limit by the research efforts [56].

One of the commonly used FoMs is the Walden FoM [57]:

$$\mathrm{FoM_W} = \frac{P_\mathrm{d}}{f_\mathrm{nyq} 2^\mathrm{ENOB}} \ [\mathrm{J/conv}]. \tag{1.14}$$

The three important performance metrics that have been discussed are included in the equation. Therefore, a good summary of the global ADC performance can me inferred from this value. The number given by this FoM represents the energy required to make the conversion per sample and per level, so the lower this number the better the ADC.

By inspecting this FoM, it can be seen that decreasing the power by $\times 2$ yields the same improvement as increasing the ENOB by $+1$, or increasing the bandwidth by $\times 2$. The relationship between power and speed usually holds in practice, but the relationship between resolution and power starts differing as the resolution increases. For example, for many high-resolution ADCs, kTC noise sets the maximum achievable resolution, and in order to increase the ENOB by 1-bit the power consumption has to be increased by $\times 4$ [58]. For this reason, the Walden FoM does not provide a fair evaluation of high-resolution ADC. This motivated the creation of the Schreier FoM, which takes all of the above discussion into account by establishing the following definition:

$$\mathrm{FoM_S} = \mathrm{SNDR} + 10 \log \frac{f_\mathrm{nyq}}{2P_\mathrm{d}} \ [\mathrm{dB}]. \tag{1.15}$$

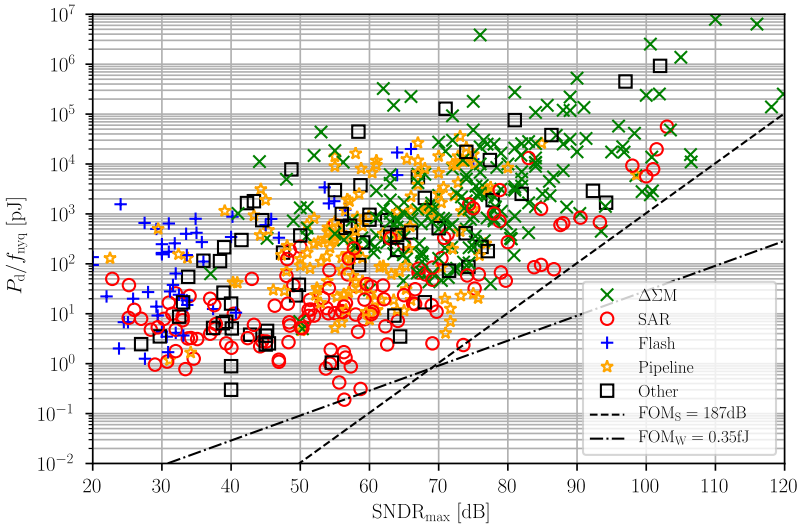

Figure 1.4 | State-of-art ADC chart. Current FoM limits are shown in dashed lines.

According to this equation, the power has to be increased by $\times 4$ in order to obtain a +6.02 dB FoM improvement (i.e. 1-bit ENOB increase), so this FoM is more coherent with the practical design issues of high-resolution ADCs.

1.2.2 State-of-Art ADCs

As mentioned in Section 1.2.1, FoMs are the metric used to evaluate the ADC performance. There are different types of ADC architectures, each excelling in different areas. The principles of operation of each architecture are always the same, but the research tries to incorporate new or more efficient techniques along with more optimal circuits in order to break the current state-of-the-art FoM limit.

The state-of-art ADCs can be plotted into the graph shown in Fig. 1.4 [59], representing the ADCs published in the IEEE International Solid-State Circuits Conference (ISSCC) and the Symposium on VLSI Technology and Circuits. The chart graphically represents the ADC resolution, in the x-axis, and the energy-per-Nyquist sample, in the y-axis. The current state-of-art FoM is delimited by the dashed lines, which represent the points with a same FoM value. The improvement trend moves perpendicular to the lines. Currently, the Schreier FoM limit is placed at 187dB, whereas the Walden FoM limit is at 0.35fJ/conv.

A distinction is made between the different base ADC architectures [60]. Flash ADCs have fallen behind other architectures, but they still have a place for ultra-high-speed applications [61]–[65]. Pipeline ADCs cover the range of applications requiring high-speed but also higher resolution than the one offered by flash types [66]–[69]. SAR ADCs exhibit the best balance between all the performance metrics [19]–[33], covering a wide

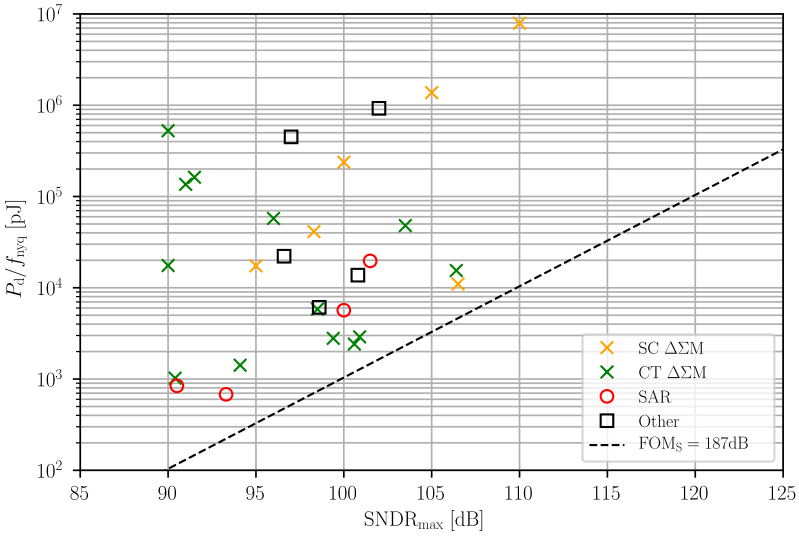

Figure 1.5 State-of-art ADC chart showing only high-resolution ADCs (SNDR $\geq$ 90 dB) with general purpose bandwidth (BW $\geq$ 20kHz).

range of applications and currently achieving the highest Schreier FoM value [8]. Finally, ΔΣMs cover the very high resolution application range, also achieving high FoM values [21]–[47], [70]–[83]. In addition, there exist additional architectures not shown in the chart individually, such as integrating ADCs, which are very efficient for low-speed applications and can potentially achieve very high resolution. The different characteristics of these ADC families are summarized in Table 1.1.

Out of all the ADCs shown in Fig. 1.4, it can be appreciated that only a small percentage of them are located in the very high resolution region (SNR $\geq$ 90 dB). Furthermore, if only the ADCs with an audio-range or wider bandwidth (i.e. general purpose ADCs) of this region are selected, then the total number of published ADCs is less than thirty, as depicted in Fig. 1.5 [14]–[18], [21]–[33], [43]–[47], [70], [71], [78]–[80]. In addition, the Schreier FoM, although competitive in some designs, does not achieve the best FoM values. The reason for this is that the design of such high resolution ADCs intended for general purpose applications is not trivial, and achieving such performance requires design trade-offs that are not positively accounted for even by the Schreier FoM.

ADC Type	Strength	Weakness	Applications
Flash	Highest speed	Lowest resolution Power hungry Large area	High-speed instrumentation
Pipeline	High speed Moderate resolution	Low power efficiency Latency Complex design	High-speed instrumentation
SAR	Best power efficiency Minimalist design	Moderate speed Requires calibration	Industrial measurement Data acquisition Audio processing
ΔΣM	Highest resolution	Requires digital support Moderate speed	Industrial measurement Data acquisition Audio processing
Integrating	Potentially high resolution Low complexity	Slower as resolution increases	Low-speed industrial measurements

Table 1.1 | Qualitative comparison of the main ADC families.

1.3 Objectives and Scope

Following the motivation factors given in Section 1.1, the working hypotheses that build the basis of this PhD thesis can be summarized in the following statements:

- A high-resolution, low-power, moderate-bandwidth, calibration-free, state-of-the-art ADC can be fabricated in standard CMOS technology.
- It is possible to design state-of-the-art SC ΔΣMs with a competitive FoM not so far behind their CT ΔΣMs counterparts, with the advantages of enjoying increased robustness.
- A design methodology can be derived for the design and optimization of low-power SC ΔΣM ADCs.
- Such ADCs can be made suitable for space applications by the employment of a special design guidelines in order to increase their radiation robustness.
- It is possible to incorporate AGC capabilities into the SC ΔΣM architecture by implementing the appropriate ADC modifications.

In order to demonstrate whether these hypotheses are true or not, the research work presented in this PhD thesis can be defined according to the following objectives:

- A mathematical framework derived from circuital analysis in conjunction with high-level modeling and simulation, and a design methodology for the design of low-power SC ΔΣM ADCs.
- A state-of-the-art, high-resolution SC ΔΣM with a high, experimentally measured Schreier FoM.
- A flicker-noise cancellation mechanism for resolution enhancement in SC circuits.

- State-of-the-art, low-power circuits and techniques from the literature employed in order to improve the ADC performance, such as multi-bit quantization.
- The robustness of the SC ΔΣM architecture explored by porting the design into lower CMOS technology nodes, as well as the validation of the design methodology.
- Increase of the radiation-hardness of the ADC by incorporating rad-hard techniques into the design methodology, together with radiation tests in order to validate it.
- A full ADC intelectual property (IP) realization including the hardware implementation of the decimation filter and bus peripheral.
- A new SC ΔΣM architecture incorporating AGC capabilities.

As the statements above show, the scope of this PhD thesis focuses on SC ΔΣMs. The contributions from this work attempt to show that SC ΔΣMs are a viable choice when designing high-resolution ADCs and that there are many advantages to be obtained from making this choice. Many applications, such as high-quality audio processing, scientific measurement, space missions, etc... can benefit from the ADCs contributed by this work, and the proposed techniques for SC circuits may open new paths in the high-resolution research field.

ΔΣ Modulation Principles and Modeling | 2

In this chapter, the focus is placed in the ΔΣM ADC family. The mathematical fundamentals of this ADC type are explained, with the help of the basic concepts described in Chapter 1. There exist many ΔΣM architectures, so this explanation is followed by a review of the most popular choices, spanning from the simplest ΔΣM to the current state-of-the-art architectures exhibiting the best FoM numbers. Next, a discussion about the possible ΔΣM implementations is put on view, describing their strong and weak points. Last but not least, the derivation of mathematical models for a key SC ΔΣM building block, the SC integrator, is given in detail. Several second-order circuital effects having influence in the ADC performance are also explained and quantified.

2.1 ΔΣM Architectures

There exist a large amount of ΔΣM architectures in the literature, suited for different kind of applications. In this section, a review of the best known architectures is presented, explaining their principle of operation, their advantages and disadvantages, and the design issues that can be found when dealing with the design of such solutions. To start with, the most basic ΔΣM architecture is explained to give a good understanding of the working principle of any kind of ΔΣM.

2.1.1 First Order ΔΣM

ΔΣMs are based on the oversampling principle, as briefly mentioned in Section 1.2.1. The main idea behind a ΔΣM is to make an efficient use of oversampling so that in-band quantization noise is reduced much more than it would just by using oversampling in a regular ADC. To achieve this, the ΔΣM architecture is constructed in a way so that a noise shaping function is applied to the quantization noise. The most basic ΔΣM architecture, called first-order ΔΣM, is shown in Fig. 2.1a. It makes use of a single-bit quantizer, a

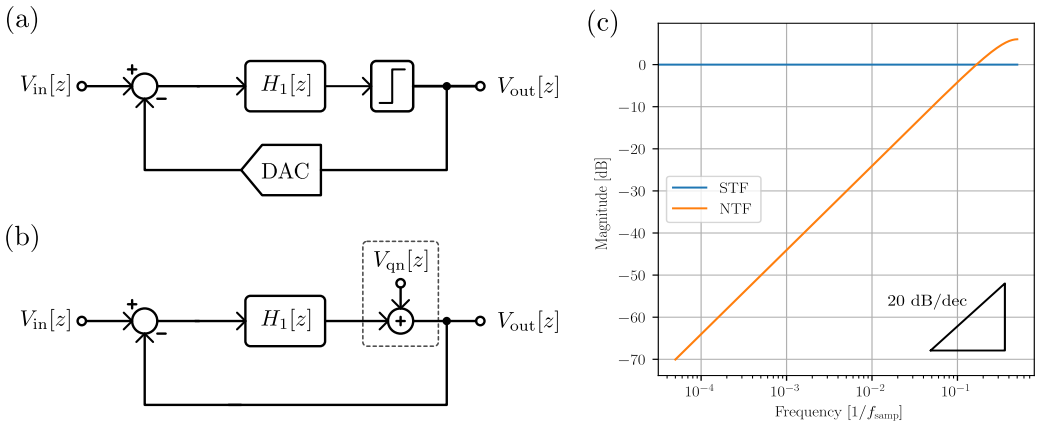

Figure 2.1 General case, first-order ΔΣM architecture (a), linear model (b) and plot of the magnitude of its characteristic transfer functions (c).

feedback digital-to-analog converter (DAC), an adder at the input, and a some transfer function along the signal path, called loop filter.

Its operation consists on applying negative feedback by subtracting the output of the quantizer back at the input, so the actual input of the loop filter is effectively the quantization error. Solving the circuit in Fig. 2.1b yields the following equation in the Z-domain:

$$V_{out}[z] = V_{in}[z] \overbrace{\frac{H_1[z]}{1+H_1[z]}}^{\text{STF}} + V_{qn}[z] \overbrace{\frac{1}{1+H_1[z]}}^{\text{NTF}}. \tag{2.1}$$

This expression shows different transfer functions for the input signal and the quantization noise: the signal transfer function (STF) and noise transfer function (NTF), respectively. The only unknown is what value should $H_1[z]$ take. The idea is to choose a suitable function so that STF = 1, i.e. all-pass, and NTF shows some attenuation in the frequencies of interest, which are the low frequencies for regular ΔΣMs. This suitable function turns to be the transfer function of an integrator:

$$H_1[z] = \frac{z^{-1}}{1-z^{-1}}, \tag{2.2}$$

where an extra delay, z^{-1}, has been added to account for the latency of analog circuit integrator implementations. Substituting this into (2.1) results in:

$$V_{out}[z] = V_{in}[z] \overbrace{z^{-1}}^{\text{STF}} + \text{QN}[z] \overbrace{(1-z^{-1})}^{\text{NTF}}, \tag{2.3}$$

so the STF is just a delay respect to the input and the NTF is a high-pass shaping function with a slope of 20 dB/dec.

The magnitude of both transfer functions is plotted in Fig. 2.1c, where it is clearly visible that the NTF will largely decrease quantization noise at low frequencies, so the ΔΣM

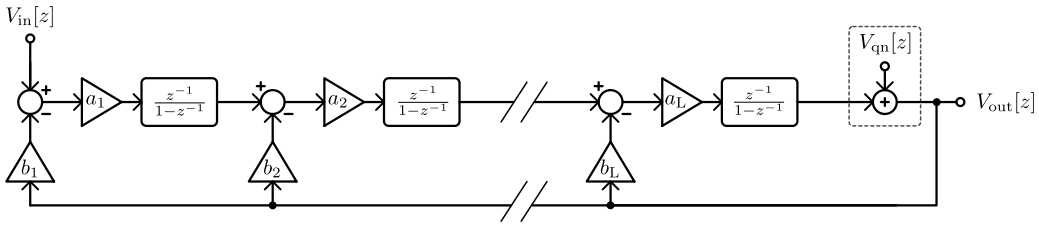

Figure 2.2 | General CIFB ΔΣM architecture.

will exhibit an ENOB larger than the actual number of quantization bits after filtering the high-frequency noise components. Indeed, it can be shown that the improvement in resolution increases at a rate of 1.5 bit/oct(OSR) [48].

2.1.2 L-Order CIFB ΔΣM

Using a first-order ΔΣM moderate-resolution ADCs can be obtained, but a sharper NTF is necessary to achieve higher resolution values. With this intention, the first-order structure is replicated L times to increase the order of the loop filter. Gain coefficients are also added to the integrators and the feedback paths in order to adjust the position of the loop poles. This architecture is known as a cascade-of-integrators feed-back (CIFB) ΔΣM [48] and its general structure is shown in Fig. 2.2.

Each additional integrator stage increases the order of the loop filter by 1, resulting in resolution improvement of $(L + 0.5)$ bit/oct(OSR) for an L-order ΔΣM, and a NTF slope of $L \cdot 20$ dB/dec. Nonetheless, this seemingly limitless SQNR improvement cannot go on forever, because increasing the loop filter order is problematic not only in the sense of increasing the design complexity, but also because stability issues already show up. As the ΔΣM order increases, more poles dependent on the architecture coefficients appear, so finding stable solutions becomes harder and the variations due to mismatch or second-order effects may become critical, requiring careful robustness verification at circuital level.

For this reason, the order of ΔΣMs is usually limited to $L \leq 5$. In order to find optimal coefficients, search algorithms or mathematical methods can be employed [84].

2.1.3 Feedforward ΔΣM

A drawback of the CIFB architecture is that, since STF $\neq 1$, the error signal $V_{\text{error}} = V_{\text{in}} - V_{\text{out}}$ at the input of the first integrator is not exactly equal to the shaped quantization noise. By taking as an example the first order CIFB architecture:

$$V_{\text{error}}[z] = V_{\text{in}}(1 - z^{-1}) - V_{\text{qn}}(1 - z^{-1}), \tag{2.4}$$

so the input is not totally removed from the loop filter path and after the first integration it will regain its amplitude. This makes the output swing of the integrators to be large

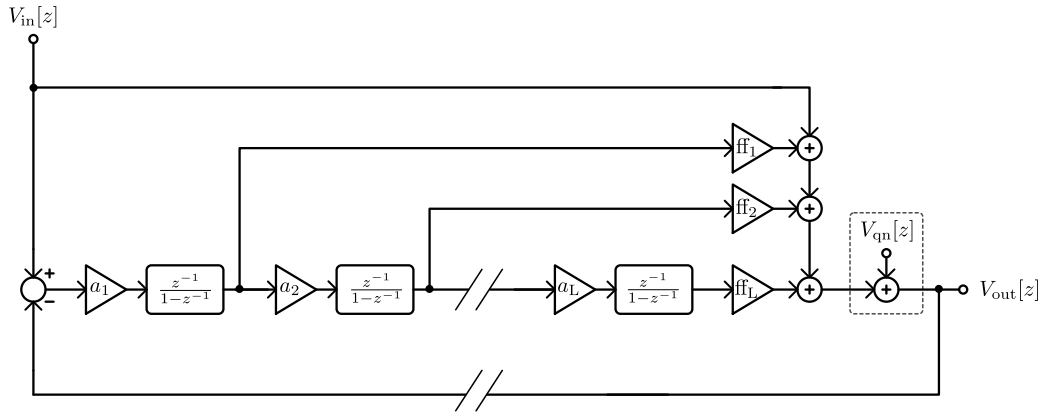

Figure 2.3 | General feedforward ΔΣM architecture.

and it requires building circuital blocks with higher performance, translating in full-scale limitations and higher power consumption in the end.

The feedforward ΔΣM architecture, illustrated in Fig. 2.3, is devised to solve this issue, among other advantages it provides [85]. By taking as an example a first-order feedforward ΔΣM, the solution of the circuit yields:

$$V_{\text{out}}[z] = V_{\text{in}}[z] \cdot \overbrace{1}^{\text{STF}} + V_{\text{qn}}[z] \overbrace{(1 - z^{-1})}^{\text{NTF}}, \tag{2.5}$$

so, in this case, the STF is exactly one while keeping the same NTF. The error signal is then:

$$V_{\text{error}}[z] = -V_{\text{qn}}(1 - z^{-1}), \tag{2.6}$$

and now the integrator only needs to handle the shaped quantization error. This greatly reduces the integrator output swing and allows for a better power optimization at circuit level. Another advantage of the feedforward architecture is that only one feedback path is needed to ensure loop stability, simplifying the circuit design by reducing the number of adders.

For these reasons, the feedforward architecture is more power efficient than the CIFB architecture, being a suitable architecture for low-power implementations.

2.1.4 MASH ΔΣM

The previous ΔΣM architectures are based on noise shaping functions to improve the SQNR. An alternative architecture called multi-stage noise-shaping (MASH) ΔΣM combines noise-shaping with noise-cancellation techniques to improve resolution [80], [81].

A particular two-stage MASH implementation, using first-order ΔΣMs, is shown in Fig. 2.4a and the general MASH architecture in Fig. 2.4b. The idea behind MASH is to cascade multiple, low-order ΔΣM whose input is the quantization error of the previous

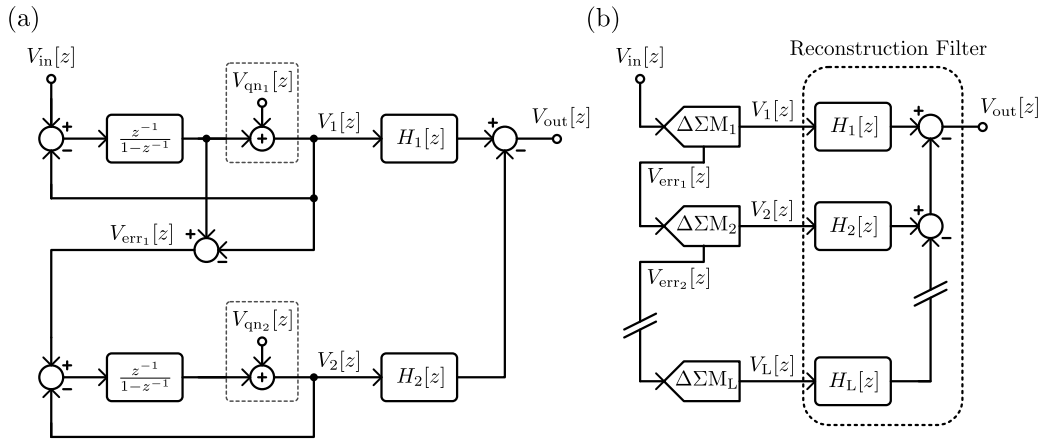

Figure 2.4 | Two-stage MASH ΔΣM (a) and general M-stage MASH ΔΣM architecture (b).

stage (with the exception of the first stage). The outputs from each stage are then run through different transfer functions and subtracted in what is called the reconstruction filter. By analizing the circuit in Fig. 2.4, we obtain:

$$\begin{aligned} V_{\text{out}}[z] = {} & V_{\text{in}}[z]\text{STF}_1[z]H_1[z] + V_{\text{qn}_1}[z]\left(H_1[z]\text{NTF}_1[z] - \text{STF}_2[z]H_2[z]\right) - \\ & - V_{\text{qn}_2}[z]\text{NTF}_2[z]H_2[z]. \end{aligned} \tag{2.7}$$

In order to cancel the noise contribution from the first ΔΣM, the transfer functions of the reconstruction filter should be:

$$\begin{aligned} H_1[z] &= \text{STF}_2[z], \\ H_2[z] &= \text{NTF}_1[z]. \end{aligned} \tag{2.8}$$

The final transfer function of the MASH ΔΣM is then:

$$V_{\text{out}}[z] = V_{\text{in}}[z]\text{STF}_1[z]\text{STF}_2[z] - V_{\text{qn}_2}[z]\text{NTF}_1[z]\text{NTF}_2[z], \tag{2.9}$$

$$V_{\text{out}}[z] = V_{\text{in}}[z]z^{-2} - V_{\text{qn}_2}[z](1-z^{-1})^2, \tag{2.10}$$

so a second-order transfer function is obtained by using two first-order modulators. If second-order modulators were used as building stages, then a fourth-order ΔΣM would be obtained with the benefits of enjoying the stability robustness of the second-order ΔΣM architectures.

The issue with the MASH approach is its large sensitivity to mismatch; imperfections in the analog feedforward path would cause the transfer functions of each stage to be different to the implemented reconstruction filter, so (2.8) would not hold, and the noise terms would not cancel perfectly. This is known as noise leakage, and hampers the maximum resolution achievable with this architecture. Therefore, increasing the number of stages becomes increasingly less efficient in practice.

A slightly modified MASH topology, called Sturdy-MASH, improves this sensitivity to imperfections in exchange for a slight resolution loss [82].

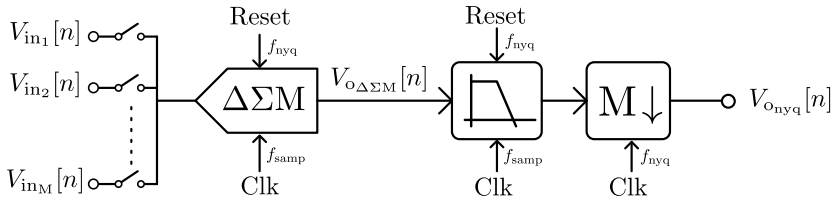

Figure 2.5 | General architecture of incremental ΔΣMs with input multiplexation. ADC memories are reset at Nyquist rate.

2.1.5 Incremental DSM

Many instrumentation applications require fully-integrated sensor interface circuits with high-resolution capabilities, many including the sensor itself. Often, they are battery powered or require a very stable temperature, so power consumption is a concern. Some other requirements are very low offset and gain errors and multiplexing capabilities for the integration of a large number of sensors in arrays.

Integrating ADCs are usually suitable for this kind of applications, but they have the disadvantage of being very slow, so they have a limited bandwidth. Traditional oversampling ΔΣM, on the other hand, are more power hungry and generally present offset and gain errors. They also have memory and require digital filters which add significant latency, so multiplexing requires the use of specific architectures which replicate memories, making them not very attractive for a system with a large number of channels.

Incremental ΔΣM are aimed for this kind of applications. The main idea behind incremental ΔΣMs is to reset the system memories at Nyquist rate, as depicted in Fig. 2.5. This changes the character of the ADC from a continuously running converter to an intermittently operated one, allowing easy multiplexing, the use of sleep mode to reduce power dissipation and an easy speed–power trade-off [72]–[79].

2.1.6 Zoom ΔΣMs

Zoom ΔΣMsbelong to the classic two-step or sub-ranging ADC architectures [86], illustrated in Fig. 2.6a. Both are based in a coarse-fine operation, where the first ADC output is subtracted to the input so the second ADC only quantifies the residue from the previous stage. The only difference between them is the amplification of the coarse error at the fine stage input in two-step ADCs.

In any case, assuming the coarse residue amplitude is matched to the fine full-scale, $\text{K}_\text{R} = V_{\text{FS}_\text{f}}/V_{\text{FS}_\text{c}} 2^{N_\text{c}}$, and the output is:

$$V_{\text{out}} = (V_{\text{in}} + V_{\text{qn}_1}) + (-\text{K}_\text{R}\text{V}_{\text{qn}_1} + V_{\text{qn}_2})/\text{K}_\text{R} = V_{\text{in}} + V_{\text{qn}_2}\frac{V_{\text{FS}_\text{c}}}{V_{\text{FS}_\text{f}}}\frac{1}{2^{N_\text{c}}}, \tag{2.11}$$

so the final quantization noise power is given by:

$$\text{QN}_{\text{rms}} = \text{QN}_{2_{\text{rms}}}\frac{V_{\text{FS}_\text{c}}}{V_{\text{FS}_\text{f}}}\frac{1}{2^{N_\text{c}}} = \frac{V_{\text{FS}_\text{c}}}{\sqrt{12}\cdot 2^{N_\text{c}+N_\text{f}}}\ [\text{V}_{\text{rms}}], \tag{2.12}$$

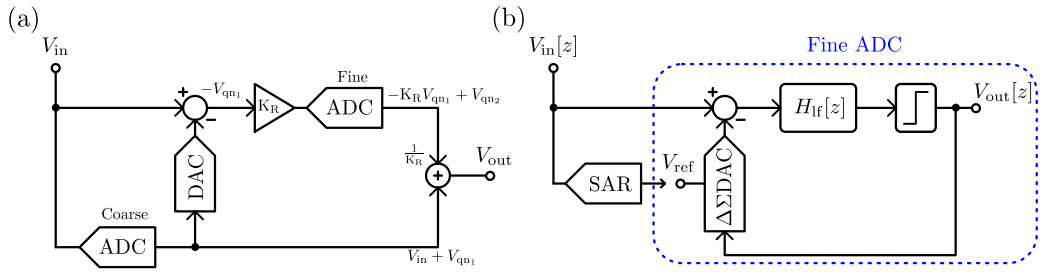

Figure 2.6 Classic two-step ADC architecture (a) and zoom ΔΣM architecture (b), where coarse SAR ADC is used to tune the DAC reference voltage of the fine ΔΣM.

which is equivalent to that of an ADC with a number of bits equal to the sum of both coarse and fine converters.

This strategy allows building high-resolution ADCs with two lower-resolution converters as building blocks, which in practice are much easier to implement. However, this classic architecture suffers from offset and linearity errors introduced by the amplification, subtraction, and DAC, thus requiring individual calibration [83].

The zoom ΔΣM uses an incremental ΔΣM architecture as the fine ADC, and the coarse subtraction is done by adjusting the DAC reference voltage instead of computing the residue [40], [87], as shown in Fig. 2.6b. This eliminates the errors caused by residue computation and makes resolution only dependent on the accuracy of the fine ADC and its references, allowing for an ultra-low-power implementation for the coarse ADC, typically a SAR. DAC linearity can also be improved using dynamic element matching (DEM) techniques [88], taking advantage of the oversampling employed by the incremental ΔΣM.

The main drawback of this architecture is its low-speed due to the two-step operation of both ADCs, being only suitable for quasi-static measurements. The dynamic-zoom ΔΣM architecture emerged in order to extend the use of zoom ΔΣM to audio-level bandwidth applications [41], [46]. In dynamic-zoom, the ΔΣM works at oversampling rate and both ADCs work concurrently, improving thus the speed capability of the architecture and achieving very high FoM values [33], [41], [42], [46], [47].

2.1.7 Multi-Bit Quantization

The single-bit quantizer of any ΔΣMs architecture can be replaced by a multi-bit quantizer [34]. Using a multi-bit quantizer has several advantages, the most obvious the direct improvement in the SQNR due to the reduction of quantization noise, given by (1.2).

The reduction in quantization noise also has power saving implications. In first place, the OSR can be reduced for a same target resolution resulting in a smaller energy per Nyquist sample. In second place, by looking at (2.6), we can see that the input of the integrator in the feedforward architecture is proportional to the quantization noise. Reducing the quantization noise power, then, has as consequence the reduction of the integrator output

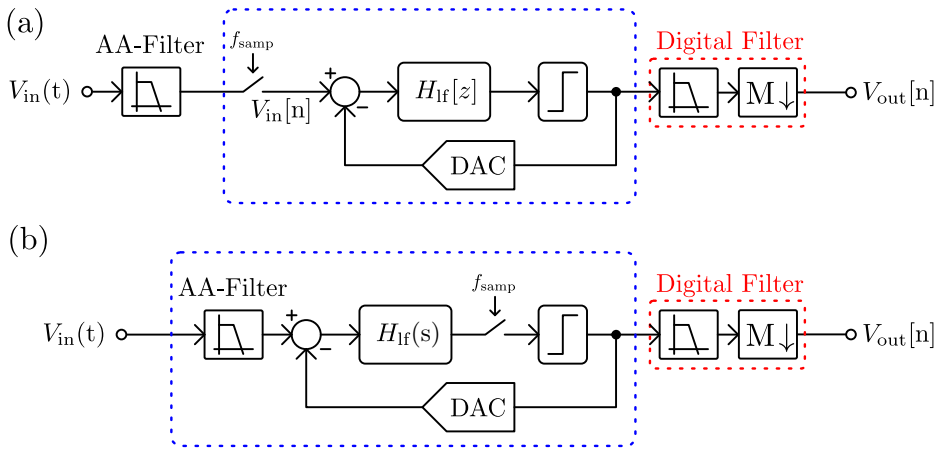

Figure 2.7 SC (a) and CT (b) ΔΣM tipical architectural implementations. The ADC is delimited by the blue line and the digital filter by the red line.

swing, allowing for a better power optimization of its operational amplifiers (OpAmps).

The main downside of multi-bit quantization is the introduction of tonal distortion at the feedback DAC output due to element mismatch, contrasting with the inherent linearity of a single-bit quantizer. This error can be very harmful because it is not shaped by the loop-filter and directly added to the input.

In order to increase the robustness of the design, mismatch shaping techniques such as DEM should be applied [88]. Random DEM transforms the tonal distortion into a white noise spectrum, so some of the noise can be removed by taking advantage of oversampling. When random DEM is insufficient, dynamic weighted averaging algorithm (DWA) also adds a shaping function to mismatching errors, greatly reducing its impact on resolution [89], [90].

Another drawback is the increased complexity of the DAC and quantizer blocks. Typically, a flash-type quantizer is implemented because of its high speed, so the number of comparators will increase with the number of levels and so will the power consumption of the quantizer. In order to obtain a positive power balance, power efficient quantizers should be implemented [91].

2.2 SC vs CT Architecture Implementations

There exist two types of implementation for the architectures presented in the previous section: switched-capacitor (SC), i.e. discrete-time (DT), and continuous-time (CT) circuits. The main architectural difference is the location where signal sampling occurs: in SC ΔΣMs, the signal is sampled at the ADC input so all the analog processing is done in a discrete-time fashion (see Fig. 2.7a), where as in CT ΔΣMs the signal is sampled at

the output quantizer, and all analog processing is continuous (see Fig. 2.7b) [48]. While the difference might seem small, it makes for important operational changes both at architectural and circuital levels.

As shown in Section 2.1, integrators are a basic ΔΣM building block. In SC ΔΣMs, the integrators are based on the transfer of charge between capacitors. This has the advantage of having well defined coefficients by the capacitor ratios, providing high-robustness against process, supply voltage and temperature (PVT) corners [34]–[47]. The CT integrator coefficients, instead, depend on the absolute time constants defined by resistors or the transconductance of operational transconductance amplifiers (OTAs) and the integrator capacitors. For this reason they are much more sensitive to technology mismatch and variations, often requiring calibration [19]–[33].

On the other hand, an important disadvantages in SC ΔΣMs are the introduction of sampled kTC noise at the input stage, which will limit the maximum resolution. CT integrators do not suffer from this problem, because there is no actual sampling at the input stage. Their in-band noise density is determined instead by the thermal noise formula, and can be decreased by decreasing the resistor values in contrast to increasing the capacitor sizes as in SC, resulting in increased power efficiency.

Furthermore, the integrator low-pass transfer function helps removing high-frequency noise coming from the input, so CT implementations provide inherent anti-aliasing. This does not happen in SC circuits because the bandwidth of the input sampler needs to be higher than the sampling frequency to correctly settle the input, so this sampler causes aliasing before it could be filtered by a subsequent stage. For this reason, an anti-aliasing filter is needed at the driving stage of SC ΔΣMs.

CT ΔΣMs suffer from what is called excess loop delay [92], due to the non-zero propagation time from the quantizer input to the feedback DAC. Excess loop delay modifies the system transfer function and may create additional poles, degrading the resolution of the ADC and potentially causing instability. Compensation techniques are needed to deal with this problem [92], [93]. In SC ΔΣMs this is not a problem unless the delay is very large.

Another issue with CT ΔΣMs is its sensitivity to clock jitter [94]. While SC ΔΣMs also suffer from jitter noise contribution at the input sampler, it is small and has little impact in the overall resolution. CT ΔΣMs, however, have an important jitter contribution at the feedback DAC output.

In general, we can say that CT ΔΣMs offer a better performance and higher FoMs than SC ΔΣMs, at the cost of increased design complexity and lower robustness. The characteristics of each kind of implementation are summarized in Table 2.1.

2.3 Modeling of SC ΔΣM

The design of the input stage of a ΔΣM is the most crucial part in the design of the ADC. The reason for this is that the circuit non-idealities cause a direct addition of errors to

Feature	SC ΔΣM	CT ΔΣM
Anti-aliasing filter	Requires front-end	Built-in
Noise	kTC	Thermal noise
Jitter sensitivity	Low	High
Required OpAmp BW	High	Low
Excess loop delay	No effect unless very high	High impact on stability
Coefficient robustness	High	Low
Calibration	Not necessary	Often required

Table 2.1 | Qualitative comparison between SC and CT ΔΣM architectural implementations.

the input. These errors do not benefit from noise-shaping transfer functions, unlike the quantization error as given by (2.3), so they are especially harmful at this stage.

The non-idealities introduced at subsequent integration stages do enjoy noise shaping by the feedback loop, so their design constraints are strongly relaxed. Nevertheless, this does not apply to the input stage design, so special care has to be taken in its circuit implementation, particularly when aiming for high-resolution ADC designs.

Some of the key non-idealities affecting SC ΔΣMs [48], mainly when dealing with high-resolution designs, are: kTC noise, OpAmp noise (e.g. CMOS flicker noise), OpAmp finite gain-bandwidth product (GBW), OpAmp finite and non-linear gain, switch charge injection, clock feed-through, parasitic capacitance, and technology mismatching.

In this section, a mathematical framework for the design of SC integrators is presented. The equations derived here will be of help in the overall design methodology of the proposed SC ΔΣM.

2.3.1 Basic SC Integrator Topology

The topology of a typical fully-differential SC integrator is shown in Fig. 2.8. A fully-differential topology is preferred because of improved robustness against errors of common-mode nature and also because it offers a 3 dB DR net improvement respect to a single-ended topology, as it will be shown later.

The circuit works in two different operation stages or phases: sampling-stage (phase 1), where the input signal is sampled onto the sampling capacitor C_s, and integration stage, where the charge is transferred and accumulated at the integration capacitor C_i (phase 2). The feedback DAC voltage is also subtracted during the integration stage. The capacitor C_l represents the capacitive load from the next stage and the own OpAmp output parasitic capacitance.

The amplifier is not needed during the sampling phase, so it is a good idea to turn it off during this time to prevent it from draining power from the supplies. Of course, the amplifier cannot be disabled by regular means, such as disconnecting it from the supplies, because a fast start-up is required when transitioning between phases. For this reason,

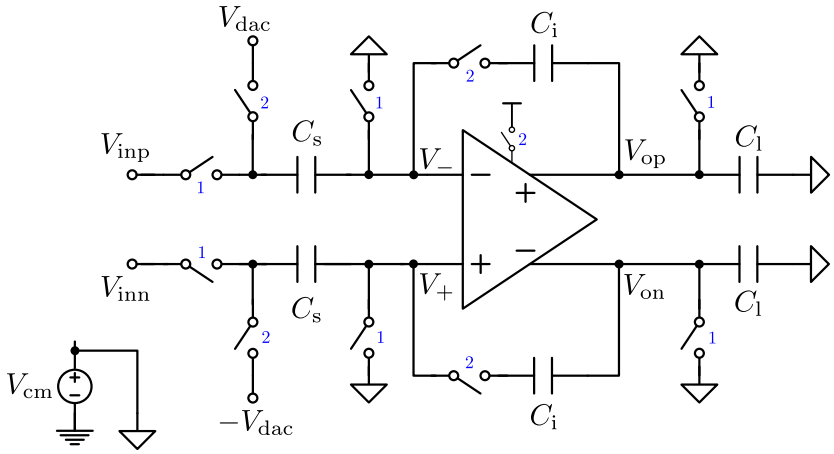

Figure 2.8 | Fully-differential SC integrator topology. Blue numbers indicate the phase when the switch is closed.

special OpAmp topologies with on-off capabilities called switched-OpAmps (SOAs) are used, in order to limit the OpAmp duty-cycle to the duration of the integration stage [95]. Power consumption is then reduced to 50% when both phases have equal duration, which is the common practice.

Another important benefit of using a SOA implementation is that it allows the removal of switches at the OpAmp output, which would be necessary if the SOA capability was not implemented, avoiding thus non-linear effects due to voltage-dependent switch-resistance.

Fully-differential OpAmps also require some sort of common-mode feedback (CMFB) mechanism to establish a known output common-mode, V_{cm_0} [96]. In SC CMFB implementations, the output common-mode level is pre-charged when the OpAmp is in its off-phase to established a desired operation level [97].

In fully-differential circuits, the information resides in the differential signals, so we usually do not care about common-mode during the analysis. In these cases, we can use superposition on the differential sources and apply the odd-symmetry theorem to simplify circuit analysis.

As an example, Fig. 2.9 shows the integrator during sampling stage and its equivalent two half-circuits. The full solution is found just by solving one of the half-circuits and using the following relationships given by symmetry:

$$\begin{aligned} V_{x_p} &= -V_{x_n}, \\ V_{x_{diff}} &= V_{x_p} - V_{x_n} = 2V_{x_p}. \end{aligned} \tag{2.13}$$

When dealing with uncorrelated noise sources, the circuit is not perfectly symmetric in terms of voltage because of the randomness of the signals, so (2.13) does not hold. However, the circuit is still symmetric in terms of power and the following relationships

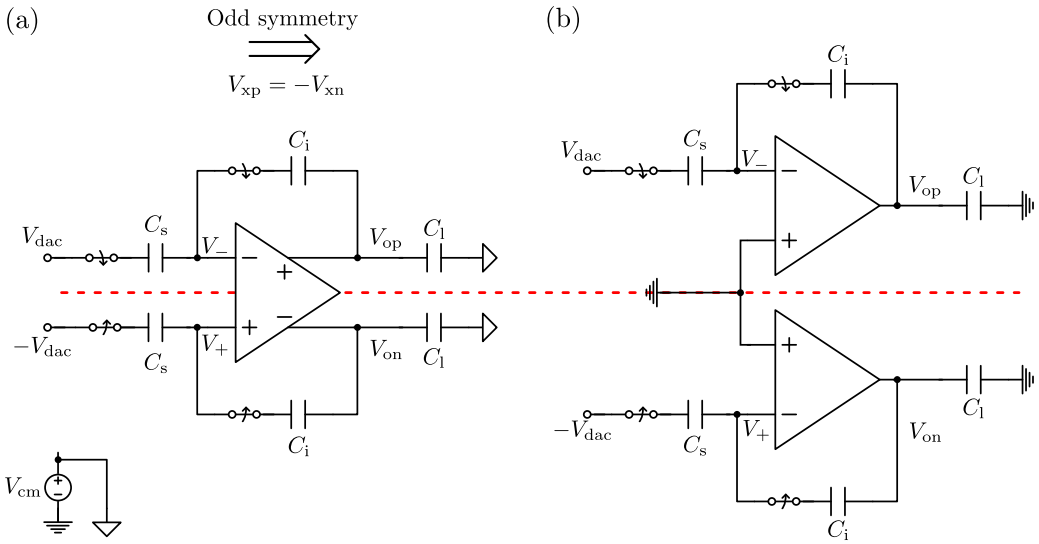

Figure 2.9 | SC integrator during integration stage (open switches omitted) (a), and equivalent odd-symmetry circuit (b).

can be used:

$$\begin{aligned} \sigma^2_{V_{x_p}} &= \sigma^2_{V_{x_n}}, \\ \sigma^2_{V_{x_{diff}}} &= 2\sigma^2_{V_{x_p}}, \end{aligned} \tag{2.14}$$

where σ_x^2 is the variance or expected power of the signal and is computed as: $\sigma_x^2 = E\left[(X - E[X])^2\right]$.

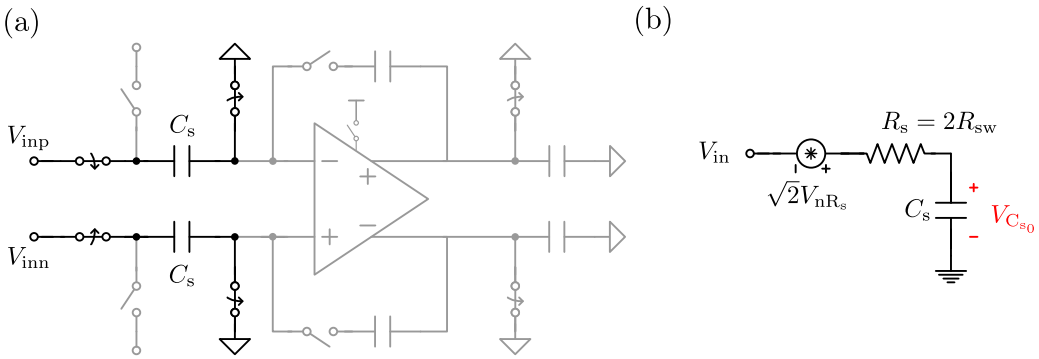

Figure 2.10 | SC integrator during sampling stage (a), and simplified differential signal model (b).

2.3.2 Sampling Stage Analysis

The state of the circuit during the sampling phase is shown in Fig. 2.10a, and its simplified differential model in Fig. 2.10b, found by using odd symmetry theorem and equations (2.13) and (2.14). These circuits consist on a basic RC sampler with a noisy voltage source modeling the thermal agitation of the resistor carriers.

Solving the circuit with the Laplace Transform yields the following transfer function for both noise and signal:

$$R_{\mathrm{s}} = 2R_{\mathrm{sw}}, \tag{2.15}$$

$$\omega_{\mathrm{s}} = \frac{1}{R_{\mathrm{s}}C_{\mathrm{s}}}, \tag{2.16}$$

$$H_{\mathrm{s}}(s) = \frac{V_{\mathrm{Cs_0}}}{V_{\mathrm{in}}} = \frac{1}{1+s/\omega_{\mathrm{s}}}, \tag{2.17}$$

which is a first order low-pass filter. The sampler resistance R_{s} is equal to the series equivalent of the individual resistance of each non-ideal switch R_{sw}. The angular sampler bandwidth is given by ω_{s}. The total integrated noise power is calculated as follows:

$$\begin{aligned} N_{\mathrm{xx_{R_s}}} &= 4K_{\mathrm{T}}TR_{\mathrm{s}}, \\ \sigma^2_{\mathrm{n_{Cs}}} &= \int_0^\infty 2N_{\mathrm{xx_{R_s}}}|H_{\mathrm{s}}(j\omega)|^2\,df, \\ \sigma^2_{\mathrm{n_{Cs}}} &= 2\frac{K_{\mathrm{T}}T}{C_{\mathrm{s}}}, \end{aligned} \tag{2.18}$$

where T is the temperature and K_{T} is the Boltzmann constant. This is the well known kTC equation [98], widely used in discrete-time sampling systems. The $\times 2$ factor comes from the fact that a fully-differential topology doubles the amount of noise power in the circuit, as given by (2.14). On the other hand, the signal full-scale amplitude is also doubled, according to (2.13), so we have a 3dB net improvement in DR as previously advanced:

$$\mathrm{DR_{fd}} = \frac{\left(2\mathrm{FS_{se}}/\sqrt{2}\right)^2}{2N_{\mathrm{se}}} = \frac{4S_{\mathrm{se}}}{2N_{\mathrm{se}}} = 2\mathrm{DR_{se}} = \mathrm{DR_{se}} + 3\mathrm{dB}, \tag{2.19}$$

where S_{se} is the single-ended signal power, N_{se} is the single-ended noise power, and $\mathrm{DR_{fd}}$, $\mathrm{DR_{se}}$ stand for the fully-differential and single-ended dynamic ranges, respectively.

It is assumed that $f_{\mathrm{in}} \ll f_{\mathrm{samp}}$ when using a moderate to high OSR, so the input signal will barely change during the sampling period and can be approximated by a DC signal for analysis purposes. The response of the sampler is shown in Fig. 2.11, and given by the following equation:

$$\begin{aligned} \tau_{\mathrm{s}} &= 1/\omega_{\mathrm{s}} = R_{\mathrm{s}}C_{\mathrm{s}}, \\ V_{\mathrm{C_s}}(t) &= V_{\mathrm{DC}}[1 - e^{-t/\tau_{\mathrm{s}}}]. \end{aligned} \tag{2.20}$$

This transient response is plotted in Fig. 2.11, and it is shown that the signal reaches 99.3% of its finally value at a time of 5τ. Considering the available sampling time is

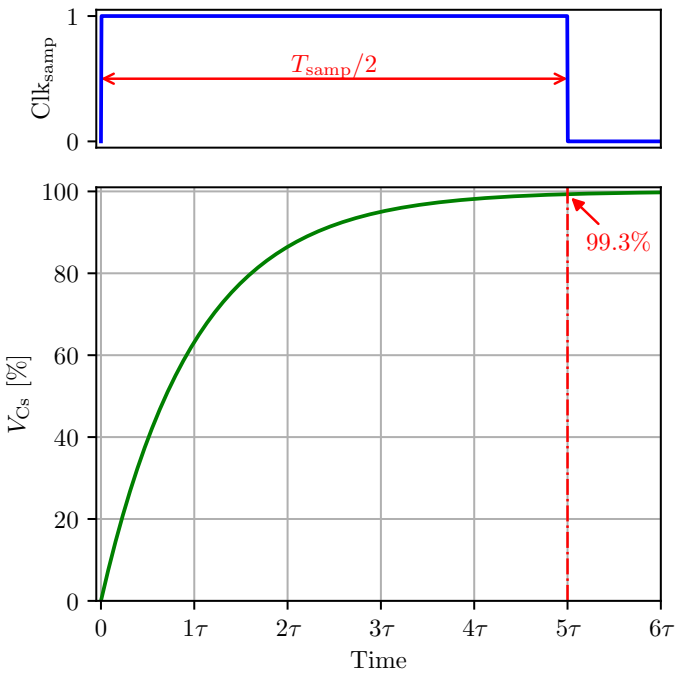

Figure 2.11 | Typical SC input sampler transient response.

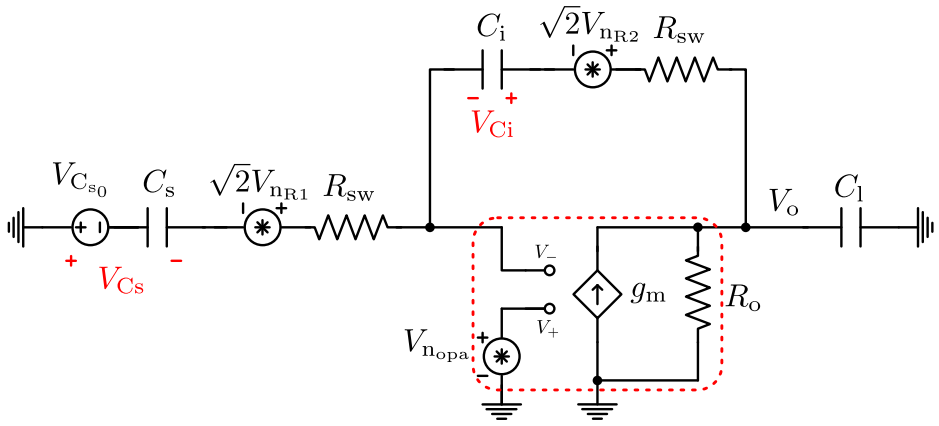

Figure 2.12 | SC integrator linear model with noise sources.

$T_\mathrm{samp}/2$, we can get a design equation by equating the two values:

$$\begin{aligned} T_\mathrm{samp}/2 &= 5\tau_\mathrm{s}, \\ \mathrm{f_s} &= \frac{5}{\pi} f_\mathrm{samp} \approx 1.6 f_\mathrm{samp}, \end{aligned} \tag{2.21}$$

so the sampler bandwidth, $\mathrm{f_s}$, has to be 1.6 times greater than the sampling frequency, f_samp, to achieve that level of accuracy.

The required settling accuracy depends on the resolution we are trying to achieve; for some designs we can get away with an accuracy less than 99.3%, but the 5τ rule is a good rule-of-thumb to follow before design optimization. This rule-of-thumb is also applicable to find the required closed-loop OpAmp bandwidth during the integration stage.

2.3.3 Integration Stage Analysis

The SC integrator linear model for the differential signal is depicted in Fig. 2.12. Switches have been replaced here by an equivalent series resistance and the OpAmp is modeled by a voltage-controlled current source with finite output impedance. The noise sources from the resistive elements and the OpAmp are also shown explicitly and have been scaled accordingly using (2.14). The direct-current (DC) source represents the stored charge from the sampling stage. The feedback DAC voltage is assumed to be zero for simplicity, but the same STF as for the sampled charge applies to this voltage source, with opposite sign.

The circuit can be solved by applying the superposition theorem to each source in the circuit. In the first place, the DC STF can be found using the principle of conservation of charge. Since the DC source $V_{\mathrm{C_{s0}}}$ already represents the capacitor charge, the capacitive element C_s is empty. The integration capacitor is also assumed empty for simplicity.

Therefore, the charge at the node V_- is:

$$Q_{\mathrm{V_-}}^{(1)} = Q_{\mathrm{V_-}}^{(0)}, \tag{2.22}$$

$$-Q_{\mathrm{C_s}} - Q_{\mathrm{C_i}} = 0. \tag{2.23}$$

Solving the equation for the integration capacitor voltage, V_{C_i} (and not the output voltage, since the information is in the stored charge) yields the following DC STF or integrator gain:

$$a = \frac{V_{C_i}}{V_{C_{s0}}} = \frac{C_\mathrm{s}}{C_\mathrm{i}}. \tag{2.24}$$

This equation shows that the architectural level gain coefficients from Fig. 2.2 and Fig. 2.3 are implemented by adjusting the sampling and integration capacitor matching ratio accordingly. The integrator gain is related with the feedback coefficient, β by:

$$\begin{aligned} \beta &= \frac{C_\mathrm{i}}{C_\mathrm{s} + C_\mathrm{i}} = \frac{1}{1+a}, \\ a &= \frac{1}{\beta} - 1. \end{aligned} \tag{2.25}$$

All of the noise source NTFs can be found by using the Laplace Transform on the elements. The analysis is somewhat complex, but in the end closed expressions can be found for all the transfer functions with the only assumption that $A_\mathrm{DC} \gg 1$, which is the OpAmp open-loop DC gain and is given by $A_\mathrm{DC} = g_m R_o$. The different NTFs are:

$$H_\mathrm{nR1}(s) = -a\frac{1 + s/\omega_{z11}}{(1 + s/\omega_\mathrm{p1})(1 + s/\omega_\mathrm{p2})}, \tag{2.26}$$

$$H_\mathrm{nR2}(s) = \frac{-a}{A_\mathrm{DC}}\frac{1 + s/\omega_{z12}}{(1 + s/\omega_\mathrm{p1})(1 + s/\omega_\mathrm{p2})}, \tag{2.27}$$

$$H_\mathrm{nopa}(s) = a\frac{1}{(1 + s/\omega_\mathrm{p1})(1 + s/\omega_\mathrm{p2})}. \tag{2.28}$$

The poles and zeroes for these transfer functions are, respectively:

$$\omega_\mathrm{p1} \approx \beta\omega_\mathrm{t}, \tag{2.29}$$

$$\omega_\mathrm{p2} \approx \frac{C_\mathrm{eq}}{\beta C_\mathrm{l}}\frac{\omega_\mathrm{sw}}{2}, \tag{2.30}$$

$$\omega_\mathrm{z11} = \omega_\mathrm{t}\frac{C_\mathrm{eq}}{C_\mathrm{l}} = \frac{C_\mathrm{eq}}{\beta C_\mathrm{l}}\omega_\mathrm{p1}, \tag{2.31}$$

$$\omega_\mathrm{z12} = \frac{\omega_\mathrm{t}}{A_\mathrm{DC}}\frac{C_\mathrm{eq}}{C_\mathrm{l}} = \frac{C_\mathrm{eq}}{\beta C_\mathrm{l}}\frac{\omega_\mathrm{p1}}{A_\mathrm{DC}}, \tag{2.32}$$

and the approximations for the poles are valid as long as $\omega_\mathrm{sw}/2 \gg \beta\omega_\mathrm{t}$. The transfer function variables are related to the model parameters by:

$$A_\mathrm{DC} = g_\mathrm{m} R_\mathrm{o}, \tag{2.33}$$

$$C_\mathrm{eq} = C_\mathrm{l} + \beta C_\mathrm{s}, \tag{2.34}$$

$$\omega_\mathrm{t} = \frac{g_\mathrm{m}}{C_\mathrm{eq}}, \tag{2.35}$$

$$\omega_\mathrm{sw} = \frac{1}{R_\mathrm{sw} C_\mathrm{s}}, \tag{2.36}$$

where C_{eq} is the equivalent OpAmp load, ω_{t} is the open-loop GBW angular frequency, and ω_{sw} is the switch-sampling capacitor bandwidth. Note that the latter is related to the sampler bandwidth ω_{s}, but it is not exactly the same.

The total integrated noise power at the integration capacitor can be found by integrating the product of the noise density by the squared magnitude of its NTF. The contribution from each source is exactly (whether the pole approximation holds or not):

$$\sigma^2_{\mathrm{nR1_{Ci}}} = a^2 \frac{K_{\mathrm{T}}T}{C_{\mathrm{s}}} \frac{\frac{\beta C_{\mathrm{l}}}{C_{\mathrm{eq}}} + \frac{\beta\omega_{\mathrm{t}}}{\omega_{\mathrm{sw}}/2}}{1+\frac{\beta\omega_{\mathrm{t}}}{\omega_{\mathrm{sw}}}}, \tag{2.37}$$

$$\sigma^2_{\mathrm{nR2_{Ci}}} = a^2 \frac{K_{\mathrm{T}}T}{C_{\mathrm{s}}} \frac{\frac{\beta C_{\mathrm{l}}}{C_{\mathrm{eq}}}}{1+\frac{\beta\omega_{\mathrm{t}}}{\omega_{\mathrm{sw}}}}, \tag{2.38}$$

$$\sigma^2_{\mathrm{nopa_{Ci}}} = a^2 \frac{N_{\mathrm{xx_{opa}}}}{4} \frac{\beta\omega_{\mathrm{t}}}{1+\frac{\beta\omega_{\mathrm{t}}}{\omega_{\mathrm{sw}}}}. \tag{2.39}$$

The final expression for the voltage across the integration capacitor can be expressed as:

$$\begin{aligned} V_{\mathrm{C_i}} &= \mathrm{STF}\cdot V_{\mathrm{Cs0}} + V_{\mathrm{nR1_{Ci}}} + V_{\mathrm{nR2_{Ci}}} + V_{\mathrm{nopa_{Ci}}}, \\ V_{\mathrm{C_i}} &= a(V_{\mathrm{in}} + \overbrace{V_{\mathrm{n_{Cs}}} + V_{\mathrm{nR1_{Ci}}}/a + V_{\mathrm{nR2_{Ci}}}/a + V_{\mathrm{nopa_{Ci}}}/a}^{\text{Total input referred noise}}), \end{aligned} \tag{2.40}$$

$$V_{\mathrm{C_i}} = a(V_{\mathrm{in}} + V_{\mathrm{n_{inref}}}), \tag{2.41}$$

$$V_{\mathrm{n_{inref}}} = V_{\mathrm{n_{Cs}}} + V_{\mathrm{nR1_{Ci}}}/a + V_{\mathrm{nR2_{Ci}}}/a + V_{\mathrm{nopa_{Ci}}}/a, \tag{2.42}$$

so all the noise can be treated as a single noisy source referred at the input. The total noise power can be found by substituting each individual noise source in (2.42) and computing its variance. Taking into account that all noise sources are uncorrelated, the result is:

$$\sigma^2_{\mathrm{n_{inref}}} = \overbrace{2\frac{K_{\mathrm{T}}\mathrm{T}}{C_{\mathrm{s}}}\left(1+\frac{\frac{\beta C_{\mathrm{l}}}{C_{\mathrm{eq}}}+\frac{\beta\omega_{\mathrm{t}}}{\omega_{\mathrm{sw}}}}{1+\frac{\beta\omega_{\mathrm{t}}}{\omega_{\mathrm{sw}}}}\right)}^{\text{kTC noise}} + \overbrace{\frac{N_{\mathrm{xx_{opa}}}}{4}\frac{\beta\omega_{\mathrm{t}}}{1+\frac{\beta\omega_{\mathrm{t}}}{\omega_{\mathrm{sw}}}}}^{\text{OpAmp noise}}. \tag{2.43}$$

The expression $\beta C_{\mathrm{l}}/C_{\mathrm{eq}} \leq 1$ always holds, so the maximum noise power is delimited by:

$$\sigma^2_{\mathrm{nmax_{inref}}} = 4\frac{K_{\mathrm{T}}\mathrm{T}}{C_{\mathrm{s}}} + N_{\mathrm{xx_{opa}}}\frac{\beta\omega_{\mathrm{t}}}{4}. \tag{2.44}$$

This expression may be familiar, and it sets a worst-case scenario that is helpful for the design. Nevertheless, according to (2.43), kTC noise contribution can be reduced down to $2K_{\mathrm{T}}\mathrm{T}/C_{\mathrm{s}}$ by reducing the factor $C_{\mathrm{l}}/C_{\mathrm{eq}}$ as much as possible and making $\beta\omega_{\mathrm{t}}/\omega_{\mathrm{sw}} \approx 0$. This can be understood as having a very small noise density because of oversized switches, and since the integrator bandwidth will be limited by the OpAmp, the contribution during integration will be much smaller than kTC, so we only have the kTC contribution coming from the input sampling stage.

The other contribution can be understood as the OpAmp noise density multiplied by the low-pass equivalent noise bandwidth of the circuit $\beta\omega_{\mathrm{t}}/4$. This contribution can also

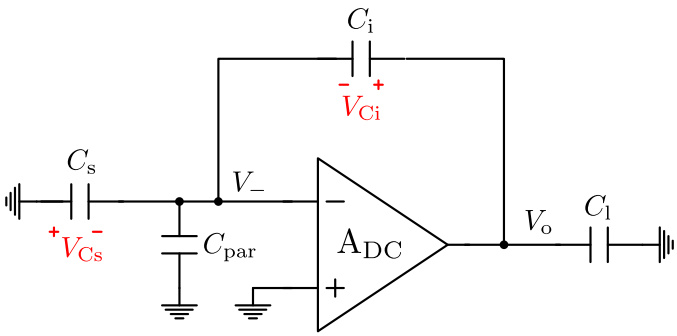

Figure 2.13 SC integrator model with finite-gain OpAmp and input parasitic capacitance.

be reduced if the poles from the NTFs are close to each other, because the equivalent noise bandwidth will decrease.

Finally, the maximum input referred in-band noise power can be found dividing (2.44) by the OSR:

$$\sigma^2_{\mathrm{nmax_{ib}}} = \overbrace{4\frac{K_\mathrm{T}\mathrm{T}}{C_\mathrm{s}}\frac{1}{\mathrm{OSR}}}^{\text{kTC noise}} + \overbrace{\frac{N_{\mathrm{xx_{opa}}}}{\mathrm{OSR}}\frac{\beta\omega_\mathrm{t}}{4}}^{\text{OpAmp noise}}, \tag{2.45}$$

this design equation will be used to calculate the minimum value of the sampling capacitor that is needed for a given resolution requirement, and the maximum allowed OpAmp noise.

2.3.4 OpAmp Non-Idealities

As mentioned at the beginning of Section 2.3, there are many OpAmp non-idealities that affect the performance of ΔΣMs, most of them taking place at the first-stage amplifier. Some of them are quite complex and their effects can only be evaluated by high-level modeling or even require a full electrical simulation, but it is possible to derive some design equations for the most important OpAmp parameters by examining some of these non-idealities.

Finite Gain and Input Parasitic Capacitance

The OpAmp input parasitic capacitance and finite gain have an impact in the accuracy of the integration coefficient. The circuit model is shown in Fig. 2.13, and can be solved using the principle of conservation of charge, previously shown in (2.23). The solution for the integrated voltage now taking into account parasitics and previously stored voltage in

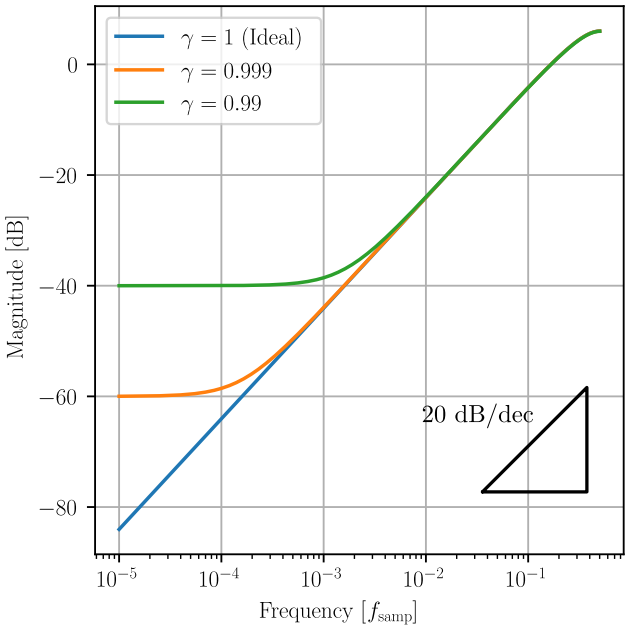

Figure 2.14 | NTF of a first-order ΔΣM with a leaky integrator showing the behavior for different γ values.

the integration capacitor, $V_{\mathrm{C_i}}[\mathrm{n}-1]$, is:

$$V_{\mathrm{C_i}}[\mathrm{n}] = \gamma a V_{\mathrm{in}}[\mathrm{n}] + \gamma V_{\mathrm{C_i}}[\mathrm{n}-1], \tag{2.46}$$

$$\gamma = \frac{1+A}{1+A+a(1+C_{\mathrm{par}}/C_{\mathrm{s}})}, \tag{2.47}$$

and the integrator transfer function is:

$$H_{\mathrm{int}}[z] = \frac{a\gamma z^{-1}}{1-\gamma z^{-1}}, \tag{2.48}$$

so the ideal integrator has become a leaky integrator due to the gain error introduced by non-idealities. The negative effects of a leaky integrator in the overall ΔΣM NTF from Fig. 2.1 can be seen in Fig. 2.14, where the low-frequency attenuation stops at some point, being worse the lower γ is. In addition, γ factor also modifies the nominal value of the coefficient, so the pole frequencies may shift potentially causing instability problems, especially for high-order ΔΣMs.

Finite Bandwidth

Finite OpAmp bandwidth has a similar effect as gain-error, incurring in coefficient mismatch but not integrator leakage. Recalling that the integrator STF expression follows (2.26),

the value of the closed-loop bandwidth is then given by (2.29). By looking back at (2.21), we can define a similar rule-of-thumb for the required amplifier GBW:

$$\begin{aligned} T_{\text{samp}}/2 &= 5\tau_{\text{opa}}, \\ \text{GBW} &= \frac{5}{\pi\beta} f_{\text{samp}} \approx \frac{1.6}{\beta} f_{\text{samp}}. \end{aligned} \tag{2.49}$$

Again, the required settling accuracy depends on the allowed variation for the coefficients to keep the loop filter stable, something that can be found via high-level functional simulations.

Slew Rate

Another important non-linear effect that can be evaluated is the slew rate (SR). By taking the derivative of (2.20) and evaluating the maximum (located at $t = 0$):

$$\text{SR}_{\max} = \left.\frac{\mathrm{d}V(t)}{\mathrm{d}t}\right|_{\max} = \frac{\Delta V_{\text{out}}|_{\max}}{\tau_{\text{int}}} = \Delta V_{\text{out}}|_{\max}\,\beta\omega_{\text{t}}, \tag{2.50}$$

where $V_{\text{out}}|_{\max}$ is the maximum variation at the output of the OpAmp and can be obtained from high-level functional simulations. Another useful way to express the slew rate is in terms of maximum current, diving by the equivalent load capacitance seen by the amplifier (2.34):

$$I_{\text{o}_{\max}} = \frac{\text{SR}_{\max}}{C_{\text{leq}}} = \frac{\Delta V_{\text{out}}|_{\max}}{C_{\text{leq}}}\beta\omega_{\text{t}}. \tag{2.51}$$

In order to avoid slew rate limitations, the OpAmp should have an output current drive greater than the value given by (2.51).

Noise

The OpAmp white noise contribution has already been accounted for in the general integrator analysis and is given by (2.45). Flicker contribution is more problematic, especially as the transistor size decreases, and harder to model. Circuit techniques based in auto-zeroing or correlated double sampling (CDS) [99] can be used in order to cancel offset and flicker noise effects. A specific implementation of CDS for SC integrators will be proposed in Section 3.3.

2.3.5 Switch Non-Idealities

Resistance Non-Linearity

Switches built with CMOS transistors suffer from resistance non-linearity respect to the input voltage. As V_{gs} voltage approaches the transistor threshold, resistance increases drastically. In order to cover a wide range of voltages, a combination of N-channel MOS

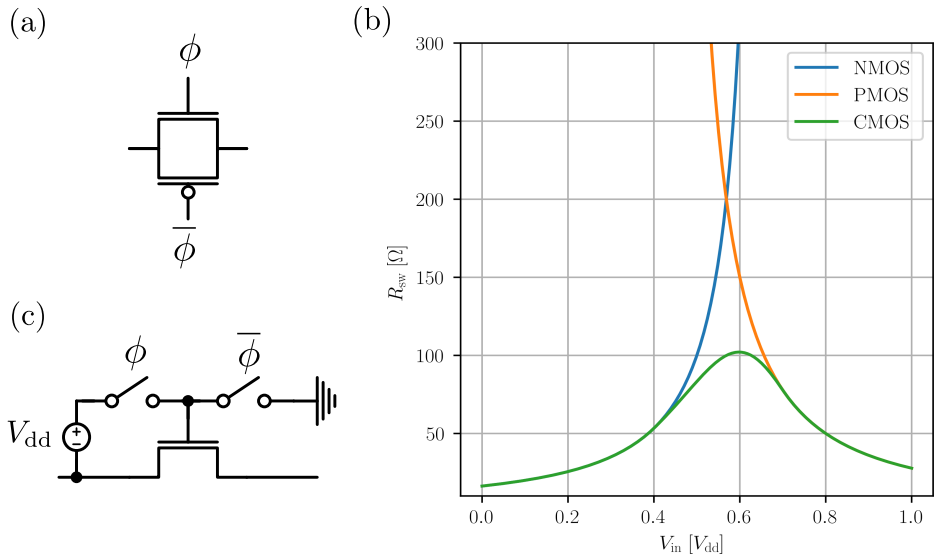

Figure 2.15 | CMOS switch (a), characteristic CMOS non-linear resistance (b) and bootstrapped switch principle (c).

(NMOS) and P-channel MOS (PMOS) transistors is used to build a CMOS switch, as depicted in Fig. 2.15a.

The resistance is now kept low for all the voltage range, but still highly non-linear, as seen in Fig. 2.15b. As long as the maximum resistance is low enough to allow the circuit to settle, this is not a problem in SC circuits because the signals are already sampled and held (i.e. static from the perspective of the sampling clock). There is one exception to this rule and it is located at the input switches, which handle a dynamic signal and can introduce considerable distortion at high input frequencies.

A solution for this is the use of bootstrapped switches [100], [101]. The basic idea behind a bootstrapped switch is to always keep a constant V_{gs} so the resistance is also kept constant, as depicted in Fig. 2.15c. The downside of these topologies is an increased switch complexity and area and over-stress of the devices resulting in the reduction of its lifetime [102], since the voltage in internal nodes can surpass the nominal supply level.

Charge Injection and Clock Feedthrough

Charge injection in analog switches consists on a level change in the charge of a storage capacitor caused by the intrinsic channel capacitance of NMOS and PMOS transistors that make up the analog switch. Clock feedthrough follows the same principle, but it is instead caused by the extrinsic gate-diffusion parasitic capacitances. When the switch is turned off, the gate voltage on the parasitic metal-oxide semiconductor (MOS) capacitor changes and, since the transistor is now in cut-off, the parasitic charge previously stored in the switch moves into the sampling capacitor, as shown in Fig. 2.16. The error introduced

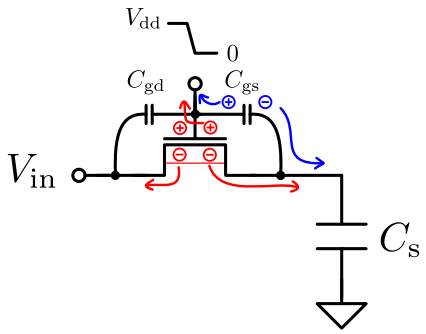

Figure 2.16 | Charge injection (red) and clock feedthrough (blue) effects in a SC circuit caused by MOS switches.

by these mechanisms is:

$$V_{C_s} = V_{in} - \overbrace{V_{dd}\frac{C_{gs}/C_s}{1+C_{gs}/C_s}}^{\text{Clock feedtrough error}} - \overbrace{\frac{Q_{ch}/2}{C_s}}^{\text{Charge injection error}}. \tag{2.52}$$

These effects would not be so problematic if not for the fact that C_{gs} is a highly non-linear capacitor which depends on the transistor voltage, V_{gs}. The same applies to the intrinsic channel charge, Q_{ch}. The injected charge will then be signal dependent, introducing distortion.

In order to mitigate these effects, a compensation switch can be used to absorb the charge injected by its complementary switch [103]. A better solution makes use of clock sequencing: opening first switches working at a constant voltage always injects a constant amount of charge, which simply translates into a voltage offset, and prevents the critical switches from having an injection path for the non-linear charge [73].

2.3.6 Design Equations

Table 2.2 summarizes all the design equations that have been derived in Section 2.3.

Parameter	**Equation**	**Description**
a	$\frac{C_\mathrm{s}}{C_\mathrm{i}}$	Integrator gain
β	$\frac{1}{1+a}$	Feedback factor
f_s	$1.6 f_\mathrm{samp}$	Required sampler bandwidth
$\sigma^2_{\mathrm{kTC_{ib}}}$	$4\frac{\mathrm{kT}}{C_\mathrm{s}}\frac{1}{\mathrm{OSR}}$	In-band kTC Noise power
C_leq	$\beta C_\mathrm{s} + C_\mathrm{l}$	Equivalent OpAmp load
GBW	$1.6/\beta \cdot f_\mathrm{samp}$	Required OpAmp GBW
$\sigma^2_{\mathrm{opa_{ib}}}$	$\frac{N_{\mathrm{xx_{opa}}}}{\mathrm{OSR}}\frac{\beta\omega_\mathrm{t}}{4}$	In-band OpAmp noise power
$I_{\mathrm{o}\max}$	$\frac{\Delta V_\mathrm{out}\lvert_\mathrm{max}}{C_\mathrm{leq}}\beta\omega_\mathrm{t}$	Required OpAmp output drive

Table 2.2 | SC integrator main design equations.

Multi-Bit ΔΣM with Flicker-Noise Cancellation | 3

In this chapter, a Multi-Bit low-power high-resolution ΔΣM is proposed. The architectural design process is explained, including the selection of the ΔΣM architectural coefficients, and it is backed by high-level simulations. This is followed by the circuit implementation of this architecture is presented at block level explaining the key points of the design. A flicker-noise cancellation modification for the first integrator is then introduced and explained in detail. Then, state-of-the-art circuit topologies used to build the ADC blocks are presented and some non-ideal effects that have influence in the overall design are explored. To finalize, all the design process is summarized into a design methodology focused on low-power optimization for a given bandwidth and resolution specification. Additional design guidelines intended for IC radiation hardening are given at the end of the chapter.

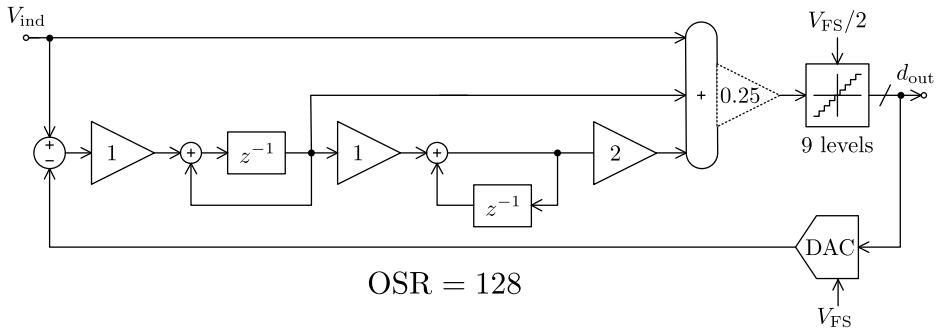

Figure 3.1 | High-level architecture of the proposed second order feedforward Multi-Bit ΔΣM.

3.1 Low-Power SC ΔΣM Architecture

In Section 1.3, the design of a high-resolution, low-power ADC was stated to be one of the objectives of the work presented in this PhD thesis. Another objective was to prove that SC ΔΣMs are a viable option in terms of performance; for that reason, a SC implementation has been chosen, among the other advantages this implementation offers (see Section 2.2). At this point, the requirements of the ΔΣM can be defined more specifically as follows:

1. SC implementation.
2. No calibration nor switch bootstrapping.
3. High-resolution (16 bit or greater).
4. General purpose bandwidth (50 kHz).
5. Low-power consumption (mW range).

In order to comply with the above requirements, the different architectures described in Section 2.1 have been studied. The favored choice was a second-order feedforward ΔΣM using a 9-level quantization. This architecture is illustrated in Fig. 3.1.

By using a second-order loop filter, the architecture is inherently stable and the small number of integration stages translates into a smaller power consumption. Multi-bit quantization makes up for the reduced resolution of the second-order loop filter, requiring only a moderate OSR of 128 so that the resolution requirements are satisfied, or equivalently $f_{\text{samp}} = 12.8$ MHz for the given bandwidth. The feedforward paths largely decrease the output swing of the integrators, relaxing OpAmp requirements and resulting in a lower power consumption.

The coefficient values were obtained from a high-level parametric optimization sweep. The idea behind it is to simulate the architecture many times, using different coefficient values and measuring the most important architectural level parameters. The parameters that can be extracted at this level are the SQNR and the statistical amplitude distributions of the internal state-variables. The amplitude of this signals will determine the output swing and SR requirements of the OpAmp circuits, so it is of interest to reduce this amplitude as much as possible.

A two-dimensional example of this is shown in Fig. 3.2, for a clear visualization of the process. In this example, the first and second integrator coefficients are swept while the rest of coefficients are kept to the known optimal value. Actually, neither of these values is known and all the variables should be swept at the same time, creating a N-dimensional space that cannot be plotted. With the purpose of showing the optimization process visually, the example is kept to two variables.

As stated above, the resolution of the design should be greater than 16 bit or, equivalently from (1.9), about 98 dB. In practice, the resolution will be mainly limited by kTC noise. Because of this fact, the SQNR should be constrained to a higher level than the required

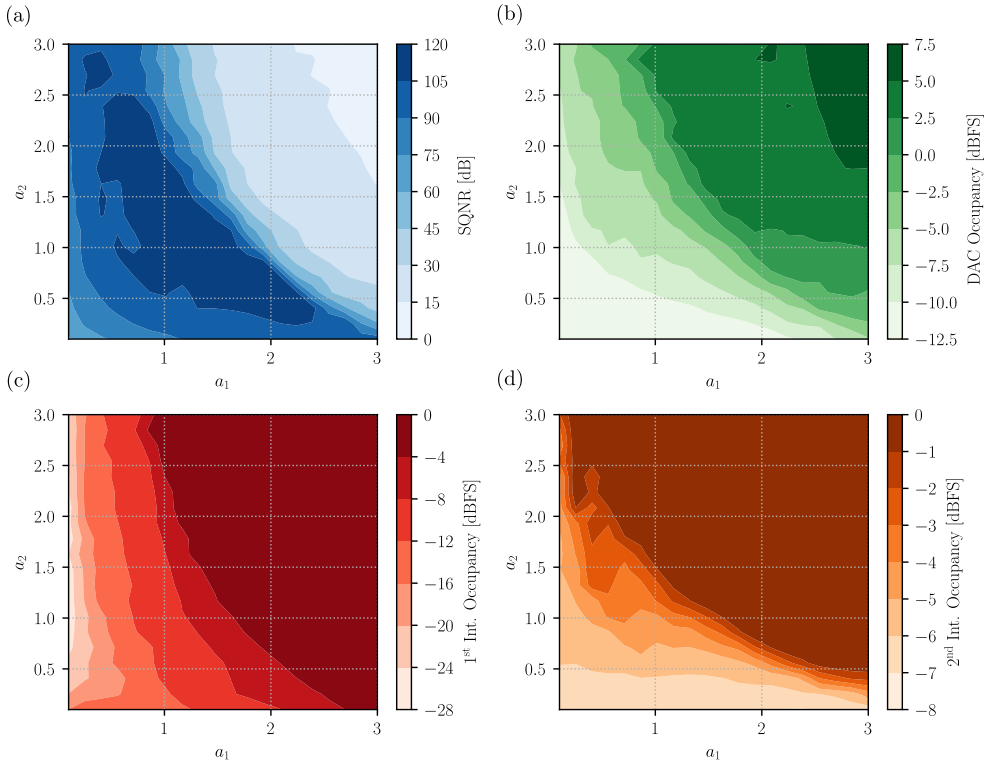

Figure 3.2 Example of a 2-D coefficient sweep while evaluating different architectural parameters: SQNR (a), and DAC (b), first integrator (c), and second integrator (d) occupancies respect to the full-scale. In this example, the integrator gain factors are swept while the rest of the parameters are kept to the optimal value found in the global sweep.

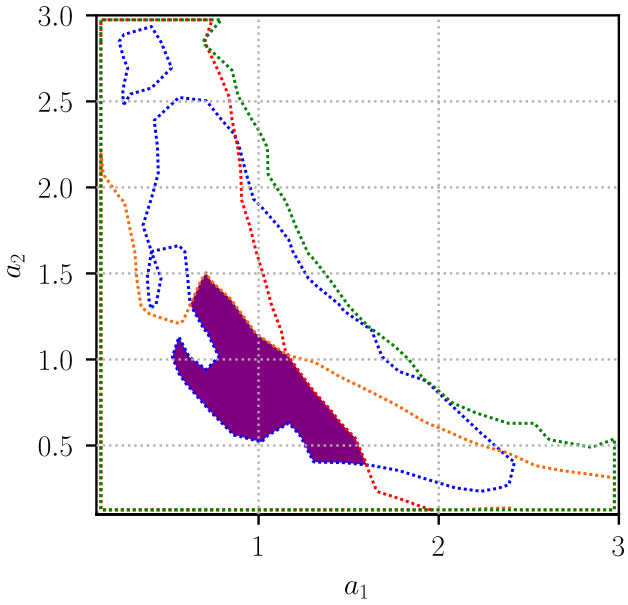

Figure 3.3 Optimal coefficient region (in purple) from the simulations at Fig. 3.2 complying with the contraints: SQNR > 105 dB, DAC level < 0 dBFS, first integrator level < −8 dBFS and second integrator level < −5 dBFS.

resolution. Otherwise, when considering the contributions from several noise sources, the resolution will drop (i.e. when two contributions have the same power level, there is an overall 3 dB loss). A safe margin of 6 dB or greater should be chosen so that the quantization noise contribution is small in comparison with the rest of the noise coming from other circuit sources. So the region of suitable coefficients should comply with the condition SQNR ≥ 104 dB.

The amplitude level of the internal state-variables is specially important at the first stage, since non-linear effects have the biggest impact on overall resolution here. In particular, high DAC signals level will have an impact in the linearity of the input switches. Also, by taking the derivative of this voltage and calculating its maximum value, the maximum output variation of the first OpAmp can be calculated, according to:

$$\Delta V_{\text{out1}}|_{\max} = a_1 \, \Delta V_{\text{DAC}}|_{\max} \,, \tag{3.1}$$

which is used to define the slew-rate requirements, given by (2.51). The same applies for the second integrator when taking into account the derivative the first integrator output level, and so on for subsequent stages. In addition, this information also tells what the required amplifier voltage swing should be.

By constraining these parameters, a region with valid coefficient sets can be obtained. This is graphically shown in Fig. 3.3, where the region is delimited by the purple area. The constraints are SQNR > 105 dB, DAC level < 0 dBFS, first integrator level < −8 dBFS and second integrator level < −5 dBFS. Any coefficient set can be chosen, but there are

some considerations related to the circuit implementation that should be taken. The first is the fact that the integration capacitor will grow in size when the coefficient values are smaller than one, as stated by (2.24), thus increasing the OpAmp load and making the design of a fast amplifier more costly. The second reason is that the coefficient values should be rational numbers from a practical implementation point of view. By doing this, proper matching techniques can be used at layout design level to increase the robustness.

It is also noticeable that the safe region of valid coefficients is wide. This is a positive fact, and it means the variations in the coefficients due to mismatch, settling errors, etc... will have little impact in the performance of the ADC, as the actual manufactured coefficients will still belong in the optimal region. In consequence, individual chip calibration is not needed. All these considerations resulted in the choice of the values $a_1 = a_2 = 1$.

By looking again at the architecture in Fig. 3.1, some differences from the standard feedforward architecture shown in Section 2.1 are seen. These differences come mainly from the circuital implementation and have been back-annotated to the architectural design, since they have a big impact on the ΔΣM. In the first place, the SC implementation operates in half-period cycles, so modeling the delays is a bit more complex than just assuming each integrator has one cycle latency. Nevertheless, after simplifying, the equivalent architecture exhibits a delay at the first integrator stage, but not at the second one.

In second place, there is an extra coefficient at the quantizer input. This coefficient models the attenuation of the passive SC adder to be introduced in Section 3.4.3. This attenuation is equal to the inverse sum of all the feedforward coefficients, $\mathrm{ff}_{\mathrm{atten}} = 1/(\mathrm{ff}_0 + \mathrm{ff}_1 \cdots + \mathrm{ff}_n)$, as it will be shown later. Because of the multi-bit quantization, this attenuation has an important effect on the ΔΣM behavior. In fact, the presented architecture does not work if this attenuation is not partially compensated. This is the reason why the quantizer and DAC full-scale values are different. Whereas the feedback DAC maximum swing sets global ADC full-scale, the quantizer full-scale can be trimmed to introduce an equivalent amplification factor at the feedback DAC, given by:

$$A_{\mathrm{DAC}} = \frac{V_{\mathrm{FS_{DAC}}}}{V_{\mathrm{FS_{qn}}}}. \tag{3.2}$$

The effects of this quantizer full-scale trimming are shown in Fig. 3.4. Because of the adder attenuation, when the quantizer FS is the same as the DAC FS, the resolution drops heavily. The reason for this behaviour is that the low signal level at the quantizer input prevents the higher codes from activating, so the quantization noise starts to grow until the amplifiers saturate. By decreasing the quantizer FS, the level distance is reduced and the issue is solved. If it was decreased too much the quantizer would overflow and a similar problem would appear.

From the simulation, it is apparent that there is a region where the resolution is at its maximum. Over all this region there are two points of special interest: one at $0.25V_{\mathrm{FS_{DAC}}}$, where the second integrator level is at its lowest, and another at $0.5V_{\mathrm{FS_{DAC}}}$, where the same happens for the first integrator. Since the design of the first integrator is more critical, the decision was to use $V_{\mathrm{FS_q}} = 0.5V_{\mathrm{FS_{DAC}}}$.

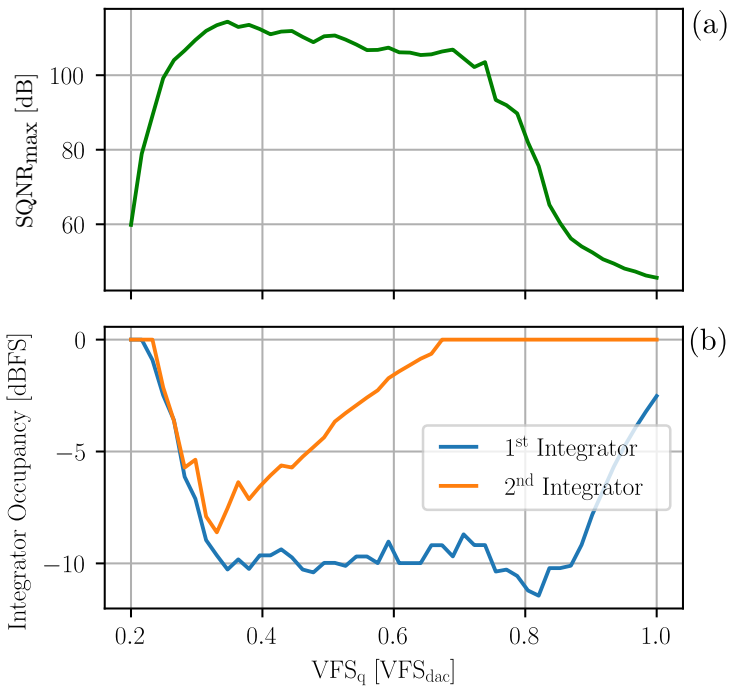

Figure 3.4 SQNR (a) and integrator signal level (b) of the Multi-Bit ΔΣM architecture of Fig. 3.1 as a function of the quantizer full-scale level.

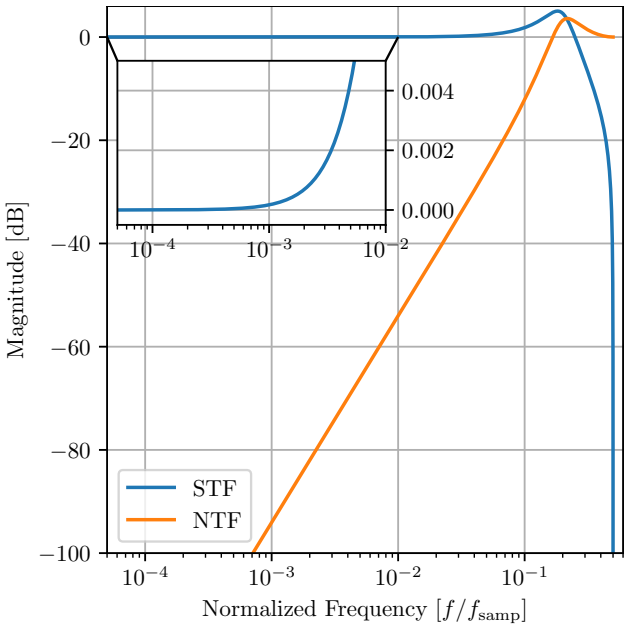

Figure 3.5 Characteristic transfer functions of the Multi-Bit ΔΣM architecture of Fig. 3.1. The zoomed inset shows the STF magnitude at the frequencies of interest.

At this point, all the ΔΣM coefficients are known, and the characteristic transfer functions from the architecture in Fig. 3.1 can be obtained:

$$\mathrm{STF}[z] = \frac{1 + z^{-1}}{2 - z^{-1} + z^{-2}}, \tag{3.3}$$

$$\mathrm{NTF}[z] = \frac{(1 - z^{-1})^2}{2 - z^{-1} + z^{-2}}. \tag{3.4}$$

It seems that the STF is not equal to one, contrary to the expected from a feedforward architecture. This is an effect of the quantizer attenuation, which changes the position of the poles, since it was not completely compensated by the full-scale choice. Nevertheless, the STF is virtually equal to 1 at the frequencies of interest, and only takes different values at very high-frequencies beyond the defined bandwidth. The NTF does show the 40 dB slope expected from a second-order architecture. A plot of these transfer functions is supplied in Fig. 3.5.

After all these considerations, we can include an important topological effect in the architectural model; kTC noise. Its introduction will give a hold of the actual ΔΣM resolution. kTC noise can be modeled by introducing an additional noise contribution at the input with total power according to (2.45). For a sampling capacitor of $C_\mathrm{s} = 8$ pF and assuming kTC noise dominates, the expected resolution is SNR $\approx$ 105 dB. The architectural level simulations in Fig. 3.6 show the difference when kTC noise is included or not. The obtained value is close to the calculated SNR, understanding there is some

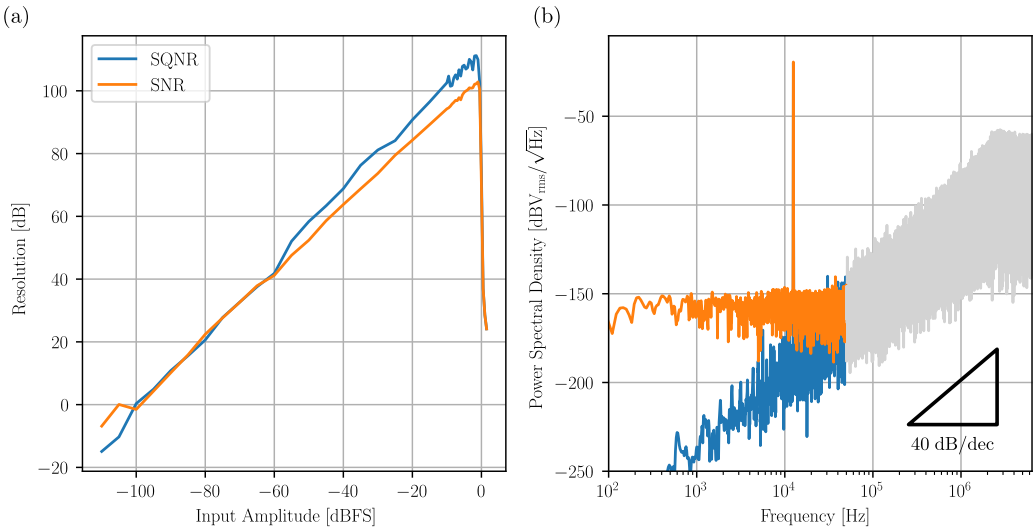

Figure 3.6 Simulated Multi-Bit ΔΣM resolution (a) and PSD at the optimal amplitude point at -1 dBFS (b) with and without kTC noise contribution.

loss because the full-scale cannot be reached due to amplitude saturation and because quantization noise has not been taken into account in the calculation.

The state-variable dynamics are shown in Fig. 3.7. As expected for a feedforward architecture, the first integrator output does not have a high input content, therefore its range is highly reduced with the corresponding benefits of low-power operation. The second integrator output does have a resemblance to the input and a higher voltage swing. This is due to the fact that the STF is not purely equal to 1. For this reason, the input tone appears again at the output of the integrators after a couple of integration stages. Nevertheless, the design constraints of the second integrator are strongly relaxed because the errors at that point are noise shaped.

3.2 Circuit Topology

Following the ΔΣM architecture proposal with the corresponding optimal coefficients, it is time to make its CMOS circuital implementation. As already mentioned, it was decided that the implementation would be SC as an objective of this PhD work. Nevertheless, the design a suitable CT implementation could be another interesting research line, with its own advantages and downsides.

The SC topology of the presented architecture is shown in Fig. 3.8. The circuit can be broken down into several functional blocks:

- First stage integrator and feedback DAC.

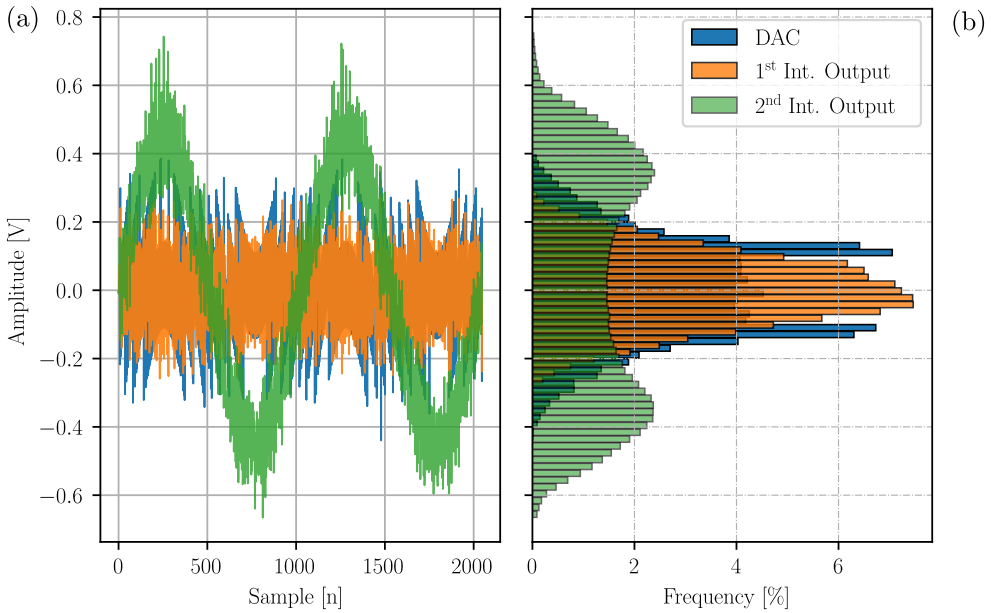

Figure 3.7 | State-variable dynamics (a) and probability distribution (b) from the Multi-Bit ΔΣM architecture of Fig. 3.1.

- Second stage integrator.
- Two SOA designs for the integration stages.
- Feedforward adder amd multi-bit quantizer.
- Single comparator design for the quantizer.
- Digital assistance (phase control, error correction, mismatch shaping and output encoding).

The operation of the integrators has been thoroughly described in Section 2.3. When two integrator stages are chained together, they operate in a pipeline manner (e.g. when the first stage is integrating, the second stage stores that result into its sampling capacitor). The integrator capacitor ratios have been calculated using (2.24). The calculation of the quantizer capacitor ratios will be explained in Section 3.4.3, as a better understanding of the multi-bit quantizer is needed. The absolute values of each set of elements can be derived from the equations in Table 2.2 and also some constraints that can be found from the high-level modeling of the multi-bit quantizer, which will depend on the particular CMOS technology.

The digital control chronogram is also shown in Fig. 3.8. The CMOS switches are depicted as numbered boxes, the numbers representing the clock phase by which they are driven. Strictly, only three phases are needed for a functional circuit, but two additional phases have been added to provide switch sequencing and thus mitigate switch charge injection effects, as explained in Section 2.3.5. The shadowed areas indicate the time

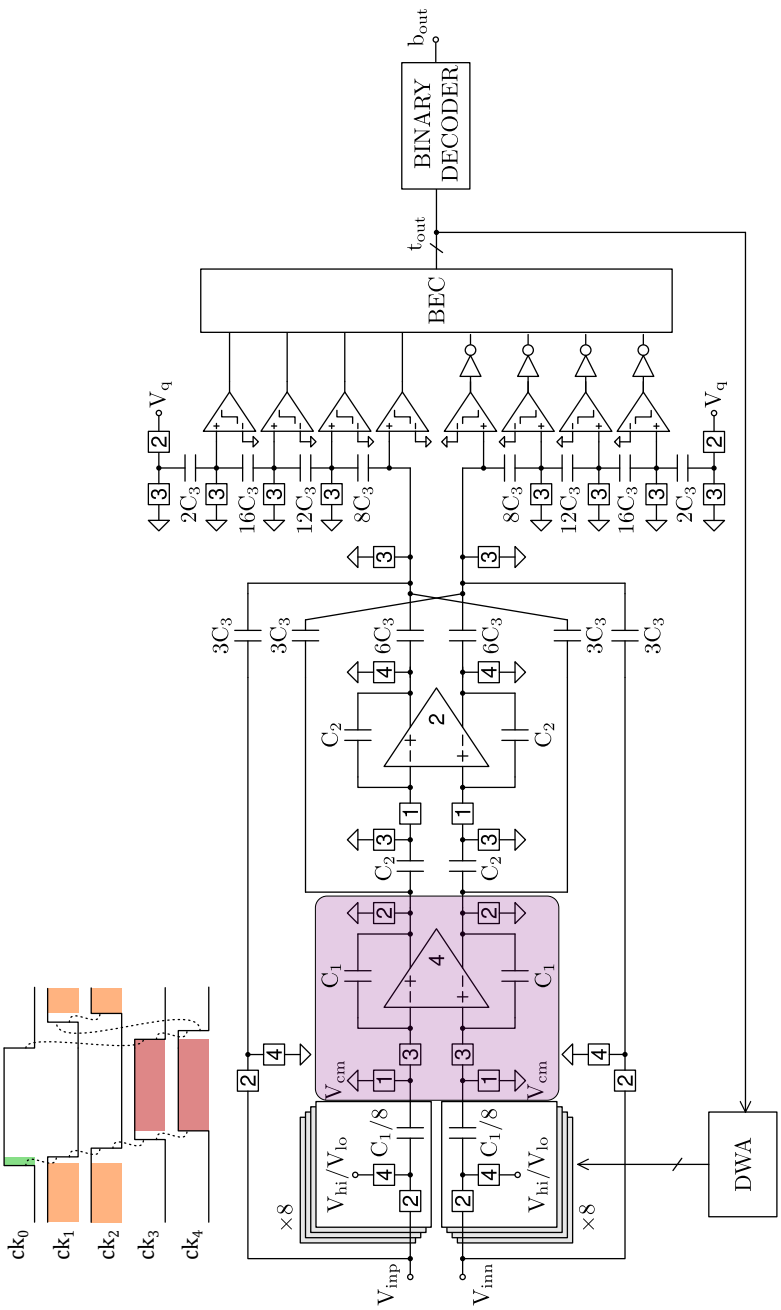

Figure 3.8 Circuital implementation of the Multi-Bit second-order ΔΣM of Fig. 3.1. Numbered boxes represent CMOS switches and their master clock phase. The purple shadowed area will be replaced by the flicker noise cancellation modification proposed in Section 3.3.

during which the amplifiers are turned on. Green is the time frame for the comparators and quantization and it is very small percentage of the period, so the comparators must be fast enough to settle during this time. Orange and red depict the on-time for the first and second integrator and SOAs, respectively, which corresponds to the integration phases. From this, it can be clearly seen that we are dealing with half delays instead of the usual full delays used at modeling.

The circuit requires four different voltage references use to set the full-scale levels of the feedback DAC and quantizer. V_{cm} stands for the common-mode, or input signal baseline, which is usually set at $V_{\mathrm{dd}}/2$. The DAC (and global) full-scale is determined by:

$$V_{\mathrm{FS_{DAC}}} = V_{\mathrm{hi}} - V_{\mathrm{lo}}. \tag{3.5}$$

Also, the following relationship must also be held to keep a coherent common mode at the output of the feedback DAC:

$$V_{\mathrm{cm}} = \frac{V_{\mathrm{hi}} + V_{\mathrm{lo}}}{2}. \tag{3.6}$$

A similar equation can be derived for the quantizer full-scale, in this case:

$$V_{\mathrm{FS_q}} = 2\left(V_{\mathrm{cm}} - V_{\mathrm{loq}}\right). \tag{3.7}$$

$V_{\mathrm{FS_{DAC}}}$ should be made as large as the nominal supply voltage and transistor threshold voltage of the CMOS technology allows. Ideally $V_{\mathrm{hi}} = V_{\mathrm{dd}}$ and $V_{\mathrm{lo}} = 0$, so $V_{\mathrm{FS_{DAC}}} = 2V_{\mathrm{dd}}$. However, choosing reference values too close to the supply rails is not feasible due to switch-resistance non-linearity and especially due to the output range limitations of the SOAs, so a compromise has to be found to keep a good ADC linearity.

Regarding the digital part of the implementation, different functionalities can be distinguished such as a bubble error correction (BEC) combinational logic, a thermometric to binary decoder and data register, and a DWA module. The employment of DWA (or alternative DEM methods) is a must, since the DAC error is introduced directly added to the input. Thus, the accuracy of the DAC elements must be as high as the target ADC resolution, regardless of the number of DAC levels, in order to prevent resolution degradation. This is shown in Fig. 3.9, where the simulation results show the degradation of the ADC resolution due to mismatch for different DEM self-calibration methods. If DEM is not implemented, element mismatch must be smaller than the LSB (e.g. $< 1/2^{16}$ for a 16-bit ADC) to prevent degradation, something unfeasible in practice. The drawbacks of adding this digital self-calibration module are minimal, specially in technologies with very small transistor channel length, due to its low cost in area and power.

BEC is not strictly needed for a good ADC performance; a good design already requires a low comparator offset, so bubbles are virtually impossible to show. Nevertheless, it does help preventing some types of single event effects (SEEs) caused by radiation and errors caused by noise spikes. Since its cost in area and power is negligible, it is a good addition to the implementation. Although not depicted in the schematic, there is also a clock generator module used to generate all the phase control signals of the circuit from a single external master clock.

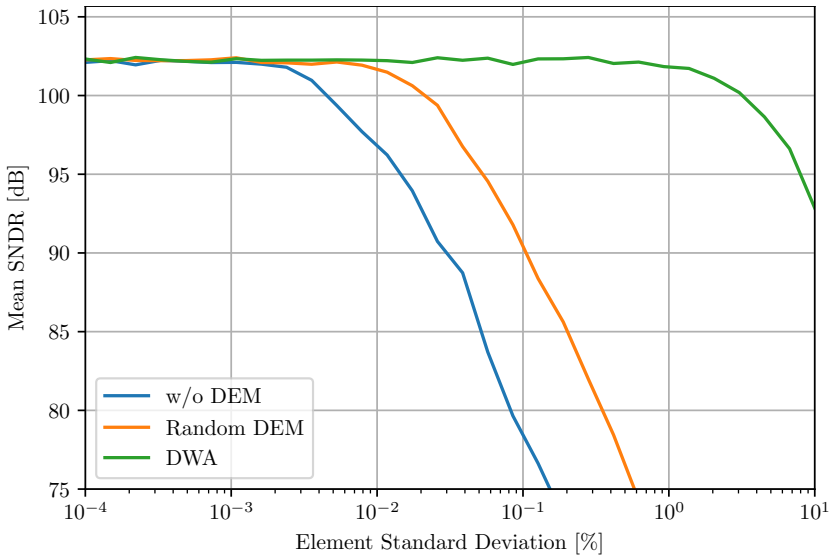

Figure 3.9 | Effect of DAC mismatch in the overall ΔΣM SNDR for different DEM implementations.

3.3 Built-In Flicker Noise Cancellation

As mentioned in Section 2.3.4, CMOS amplifiers tend to suffer from $1/f$ noise or flicker noise, which is critical in low-frequency sensing applications. This effect comes from the trapping of charges in the insulator-semiconductor interface of the MOS transistor channel [104]. Flicker-noise can be limiting to the resolution of systems due to an increasingly higher noise density at low frequencies.

Indeed, this is the case in some of the designs presented in this PhD thesis. Reducing amplifier flicker noise by conventional means requires increasing transistor area, which results in several optimization issues such as the increase in parasitic capacitance, resulting in reduction of speed and instability which may or may not be compensated by increasing the power consumption. In any case, this leads to a non-optimal amplifier design. For this reason, it is deemed appropriate to devise a modification to the first stage integrator in order to cancel flicker noise in an efficient way. This is not needed for the rest of integration stages because the inherent noise-shaping of the ΔΣM takes care of the low frequency noise contributions from those amplifiers.

There exist many classic offset and low-frequency noise cancellation techniques, such as auto-zeroing, CDS, or chopper stabilization [99]. These techniques can take many forms, depending on the target circuit or application. The proposed cancellation technique for this design is based on CDS, since it is highly compatible with SC circuits. There are some CDS proposals applied to SC integrators, but either they are very specific to some particular design, like pipeline ADCs [105], [106] or pixel sensors [107], or they present drawbacks such as needing extra hold capacitors or a 100 % amplifier duty cycles [99], [108].

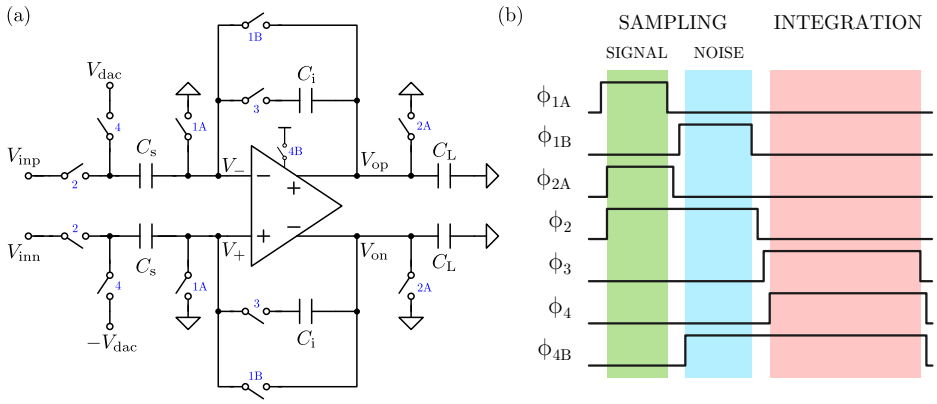

Figure 3.10 | Fully differential integrator circuit incorporating CDS-based flicker-noise cancellation (a) and control chronogram (b).

The proposed integrator stage incorporating CDS-based flicker-noise cancellation is shown in Fig. 3.10a. The only modification to the analog circuitry is the addition of a switch providing a feedback path used to connect the amplifier in a follower configuration. The rest of modifications consist on a more complex clocking scheme, which can be understood as a 3-stage operation: signal sampling, noise sampling and integration (see Fig. 3.10b). This minimalist analog approach is very helpful in keeping the analog domain circuits as simple as possible so that no extra parasitic effects appear. The complexity of this proposal resides in the generation of the control signals, but the issues arising from the digital domain are lesser and much easier to solve.

Fig. 3.11 shows the different states of the CDS circuit with an equivalent single-ended model to better understand its operation. During the first stage of Fig. 3.11a, the sampling capacitor is connected to the input and pre-charged to the signal amplitude, hence why its called signal sampling stage. Since the allocated time is smaller than for a regular sampling phase (i.e. half a period), the settling accuracy will be smaller. Nevertheless, the settling value should reach a decent level of accuracy, storing most of the necessary large-signal charge. The amplifier is off during all this time, so power consumption is neglected. At the same time, the output of the amplifier is connected to the common-mode in order to pre-charge its CMFB (recall that in reality it is a fully-differential OpAmp). The sampled voltage at this stage is:

$$V_{\text{samp}}[\text{n} + \phi] = \alpha V_{\text{in}}[\text{n} + \phi], \tag{3.8}$$

where α is the initial settling accuracy and ϕ is the duration of the first stage, relative to the period.

Once the second stage starts in Fig. 3.11b, the switches change position so that the amplifier is put in a follower configuration. At this point the amplifier turns on, so its overall duty cycle will be greater than the one for a regular integrator (i.e. > 50 %). By doing this, the input tracking is now finished through the amplifier, with the benefit of introducing the amplifier noise into the process. The stored voltage at this point is:

$$V_{\text{samp}}[\text{n} + 1/2] = V_{\text{in}}[\text{n} + 1/2] - V_{\text{n}_{\text{opa}}}[\text{n} + 1/2]. \tag{3.9}$$

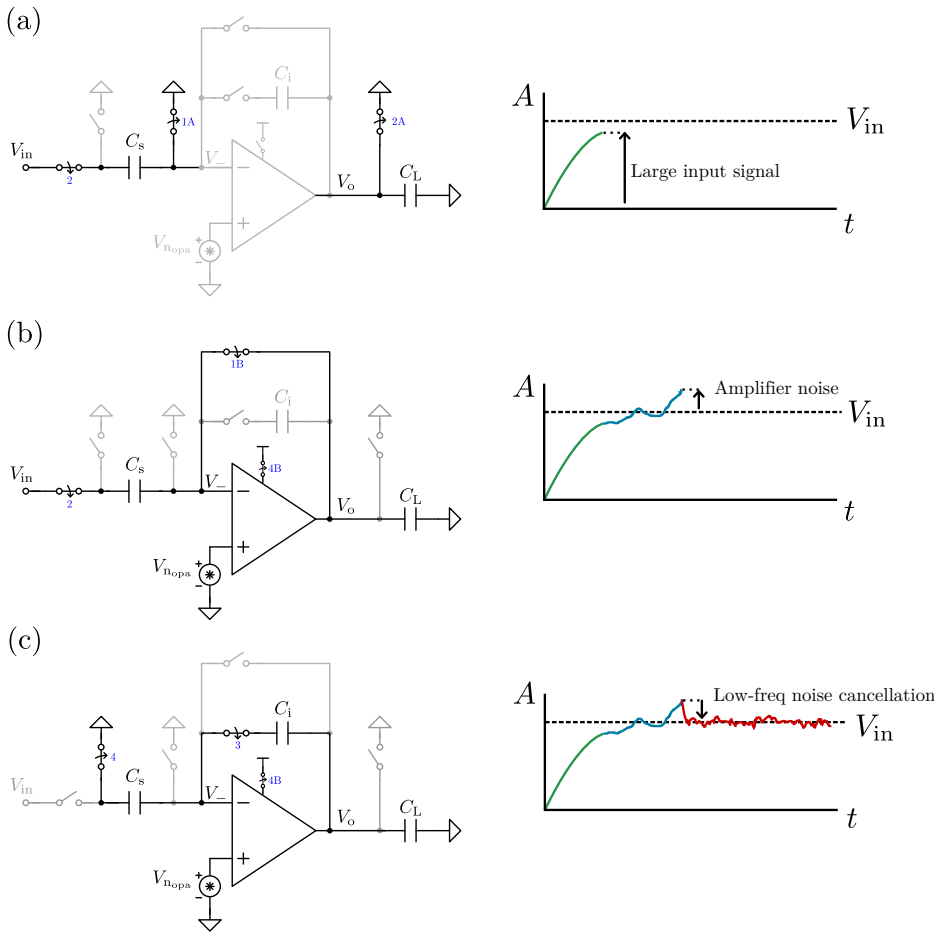

Figure 3.11 | Flicker-noise cancellation operation: signal sampling (a), noise sampling (b) and integration with noise cancellation (c).

In reality, in order to get a suitable NTF for the amplifier noise, only the second and third stages are needed. The purpose of the first stage comes from the fact that the amplifier will have a limited bandwidth and SR. So, with the aim of preventing slewing issues, the signal sampling phase is introduced first for the capacitor to be almost fully charged. By doing this, the voltage difference to be settled by the OpAmp will be small enough to avoid slewing issues. Otherwise, if there was no signal sampling phase, the amplifier would require very high slew-rate requirements as well as a 100 % duty cycle, meaning an increased power consumption.

Ideally then, the most optimal choice would be to keep the noise sampling stage to a duration close to zero; just large enough so the amplifier noise is sampled, whereas the signal was already sampled at the signal sampling stage. In practice, however, this is not a good idea, because the amplifier requires some start-up time for its stabilization. The amplifier needs to be in a stable state so that the sampled noise is correlated to that during the integration stage, and also to correctly settle the glitches from the switching transition. For this reason, a 25 % duty cycle has been chosen as the duration of each sub-sampling phase, offering a good trade-off between accuracy and power consumption. This choice also allows for an easy an robust clock generation, as will be shown in Section 3.4.1. The drawback is that the total amplifier duty cycle is now 75 % instead of the 50 % of a regular integrator.

To finalize the process, a regular integration stage is executed as in Fig. 3.11c, resulting in the following transfer function for the integrated voltage:

$$V_{\mathrm{C_i}}[\mathrm{n}+1] = a\left(V_{\mathrm{in}}[\mathrm{n}+1/2] + V_{\mathrm{n_{opa}}}[\mathrm{n}+1] - V_{\mathrm{n_{opa}}}[\mathrm{n}+1/2]\right), \tag{3.10}$$

or expressed in a clearer way:

$$V_{\mathrm{C_i}}[\mathrm{n}] = a\left(V_{\mathrm{in}}[\mathrm{n}-1/2] + V_{\mathrm{n_{opa}}}[\mathrm{n}] - V_{\mathrm{n_{opa}}}[\mathrm{n}-1/2]\right). \tag{3.11}$$

By looking at (3.11) in the Z-domain:

$$V_{\mathrm{C_i}}[z] = a\left(V_{\mathrm{in}}[z]\overbrace{z^{\frac{-1}{2}}}^{\mathrm{STF}} + V_{\mathrm{n_{opa}}}[z]\overbrace{\left(1-z^{\frac{-1}{2}}\right)}^{\mathrm{NTF}}\right), \tag{3.12}$$

so a first-order shaping function for the OpAmp noise has been created while maintaining the the same STF, which is only a half-delay.

Notice that the CDS distance is only half a sample. In the discrete domain it does not make sense to have non-integer samples. Delays smaller than one mean the CDS is happening at a rate faster than the actual sampling rate of the system. In this case, the shaping function is being applied at a frequency which is twice the actual sampling frequency of the ADC, $f_{\mathrm{CDS}} = 2f_{\mathrm{samp}}$. Since the amplifier noise spectrum exhibits a combination of flicker and white noise, the fact we have this oversampled CDS has some implications.

Firstly, the noise shaping function will effectively remove the low frequency noise, which is the main objective of this modification. The shaped white noise, however, will be aliased

down to the sampling frequency of the ADC. After the aliasing, the shaped noise becomes white again, so its power is equally distributed. By calculating then the integral of the NTF in the CDS frequency domain, it is possible to see what happens to the input referred white noise power:

$$\begin{aligned}\sigma_{\mathrm{n}}^2 &= \int_{-f_{\mathrm{CDS}}/2}^{f_{\mathrm{CDS}}/2} N_{\mathrm{xx_{opa}}} \left|1 - e^{-j2\pi f/f_{\mathrm{CDS}}}\right|^2 df = \\ &= N_{\mathrm{xx_{opa}}} \int_{-f_{\mathrm{CDS}}/2}^{f_{\mathrm{CDS}}/2} \left[1 - \cos\left(2\pi f/f_{\mathrm{CDS}}\right)^2\right] df = \\ &= 2N_{\mathrm{xx_{opa}}} f_{\mathrm{CDS}} = 2\sigma_{\mathrm{n_{opa}}}^2,\end{aligned} \tag{3.13}$$

so finally the total in-band noise power is given by:

$$\sigma_{\mathrm{n_{ib}}}^2 = \frac{2\sigma_{\mathrm{n_{opa}}}^2}{\mathrm{OSR}}. \tag{3.14}$$

The conclusion is that, in exchange for the removal of flicker noise, white noise power has doubled. This is usually not a problem because kTC noise is usually much larger than amplifier white noise, so it dominates even if the amplifier noise contribution is doubled and resolution is not affected. Nevertheless, this condition should be carefully asserted, since it will depend on the particular design specifications and CMOS technology.

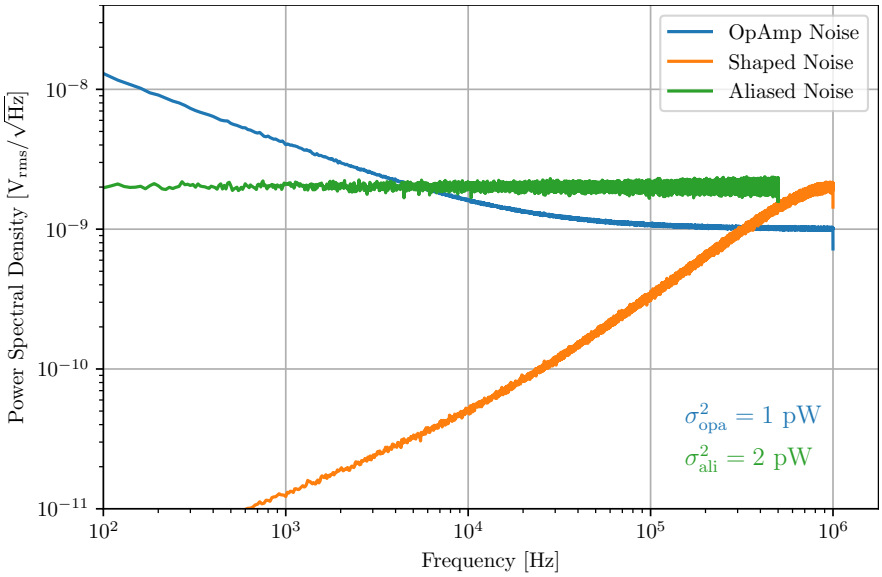

Figure 3.12 High-level simulation showing the frequency transformations of the amplifier noise due to the CDS operation. The amplifier power level here is used as an example and does not relate to actual measurements.

For the sake of adding clarity to this explanation, the frequency transformations that the amplifier noise undergoes are shown in the high-level simulation example from Fig. 3.12.

In the end, it can be seen how flicker-noise is removed but the total noise power is doubled after the aliasing of white noise. Final noise power density is given by $2\sigma^2_{\text{opa}}/(f_{\text{samp}}/2)$.

An interesting idea would be to build a circuit exhibiting a CDS NTF with the form $x[\text{n}] - x[\text{n}-1]$. This kind of transfer function would result in a similar noise shaping but, because there would be no aliasing, the amplifier low-frequency noise would be effectively removed. This is out of the scope of this work however, because the added complexity of the supposed circuit is not worth implementing for the designs at hand, since amplifier white noise is not a limiting factor.

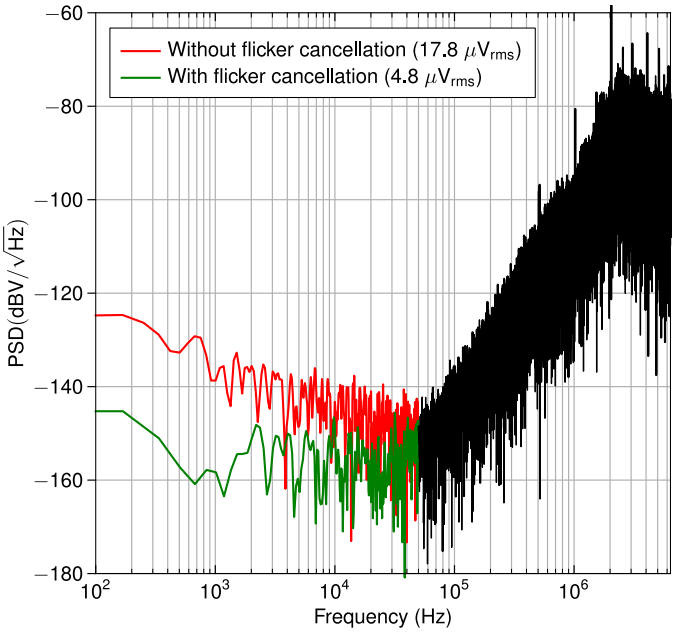

Figure 3.13 Electrical noise floor simulation of a specific ΔΣM implementation from Fig. 3.8 with and without the proposed flicker-noise cancellation mechanism.

An electrical simulation demonstrating the correct operation of the proposed flicker-noise cancellation scheme for a specific ΔΣM implementation is shown in Fig. 3.13. The simulation shows the noise floor of the ΔΣM, with and without the modification. It is clearly seen that flicker-noise was the main resolution limiting factor. After applying the flicker-noise cancellation proposal, the in-band rms noise power is reduced by almost a factor of 4. In exchange, we have only increased the power consumption of the first amplifier by 50 %. Even if we assume all the power of the ADC is increased by the same factor, the resulting net Schreier FoM improvement using (1.15) can be calculated to be $\approx +10$ dB, so the modification is well worth it.

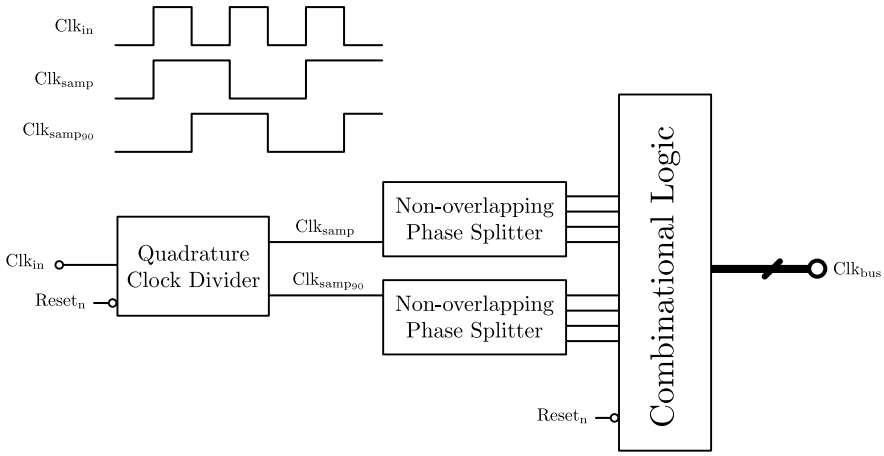

Figure 3.14 | General schematic of the clock generator module.

3.4 Low-Power CMOS Circuits

After the definition of the ΔΣM architecture and topological implementation, the remaining step in the schematic design is the realization of the circuit blocks at transistor level in the most optimal way. In particular, we will be looking at the design of the digital clock generation, the design of suitable SOAs to be employed by the integrator stages, and the design of the SC multi-bit quantizer and its comparators.

3.4.1 Clock Generation

The main purpose of the clock generator module is to supply all the clock signals managing the control of the analog ΔΣM core. All the signals will be generated from a single master clock and a reset signal, used to enable the system or leave it at a known initial state.

The overall picture of the clock generator is shown in Fig. 3.14. As mentioned in Section 3.3, the choice of using a 25 % duty cycle for the duration of the sub-sampling phases for the flicker-noise cancellation operation simplifies the design of this module. The idea behind this structure is to use an input clock with a frequency $f_{\text{in}} = 2f_{\text{samp}}$, so that the 25 % duty cycle phases can be generated in a very robust way from a clock division. With this purpose, a quadrature clock divider is placed as the first stage in order to generate two, 90-degree shifted clocks working at the sampling rate.

From these two clocks, two different sets of non-overlapping clock phases are generated by the use of non-overlapping phase splitters [109]. An example of this circuit is shown in Fig. 3.15, but it can be modified to output as many phases as needed. The idea behind this circuit is to establish a feedback loop between the related clocks so that the changes in state can only happen sequentially. In this way, it is ensured that there are no overlaps that would cause some switches to close or open at the same time, breaking the correct analog behavior of the SC ΔΣM. The non-overlapping time will depend on the delays set

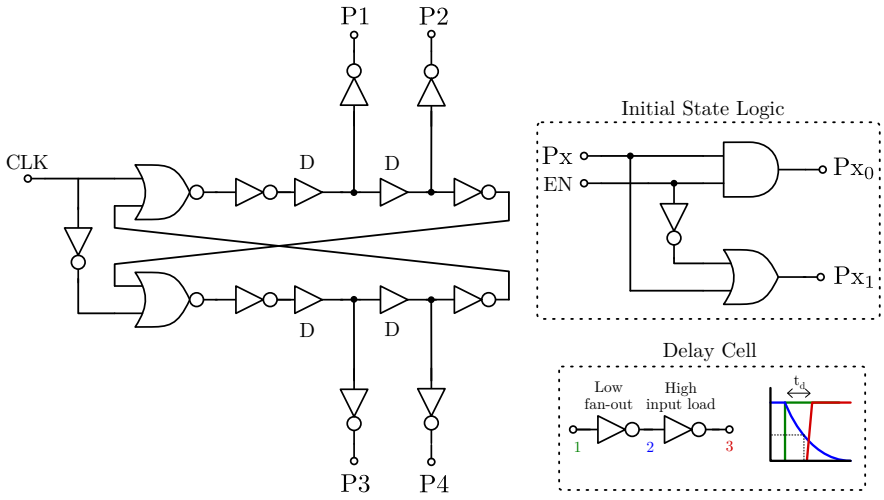

Figure 3.15 | Example of a 4-phase non-overlapping phase splitter.

by the gates in the loop. Actual standard delay cells can be added along the paths to provide a larger non-overlapping time.

Finally, a combinational module is used in order to generate all the control signals from Fig. 3.10b. Using basic logic operations, the different stages can be delimited from the existing non-overlapping phases. Another purpose of this block is to establish the initial phase values when the circuit is disabled and also to provide a buffering stage so that the analog switches can be driven correctly.

3.4.2 Class-AB SVMA

The variable-mirror amplifier (VMA) is an OpAmp architecture mainly characterized by generating all Class-AB current in the output transistors only, exhibiting very low technology sensitivity and avoiding the need of any internal frequency compensation mechanism [110]. Hence, this architecture is suitable for low-power SC circuits. Of the two types of VMA architectures, the type-II is preferred since it avoids the use of a crossed transistor which requires an extra bias reference.

A SOA modification [95] is applied to the basic architecture to allow amplifier on-off switching, along with a SC CMFB mechanism. The resulting type-II switched variable-mirror amplifier (SVMA) topology is shown in Fig. 3.16. All transistor bulk terminals are connected to their respective supply rails. Two complementary differential pairs are introduced here as input transconductors in order to split input signal into two paths for separate Class-AB control of NMOS and PMOS output transistors. This increases the gain of the amplifier and extends the input and output voltage range. Dashed boxes indicate required technology, temperature, and size matching between elements for a correct operation.

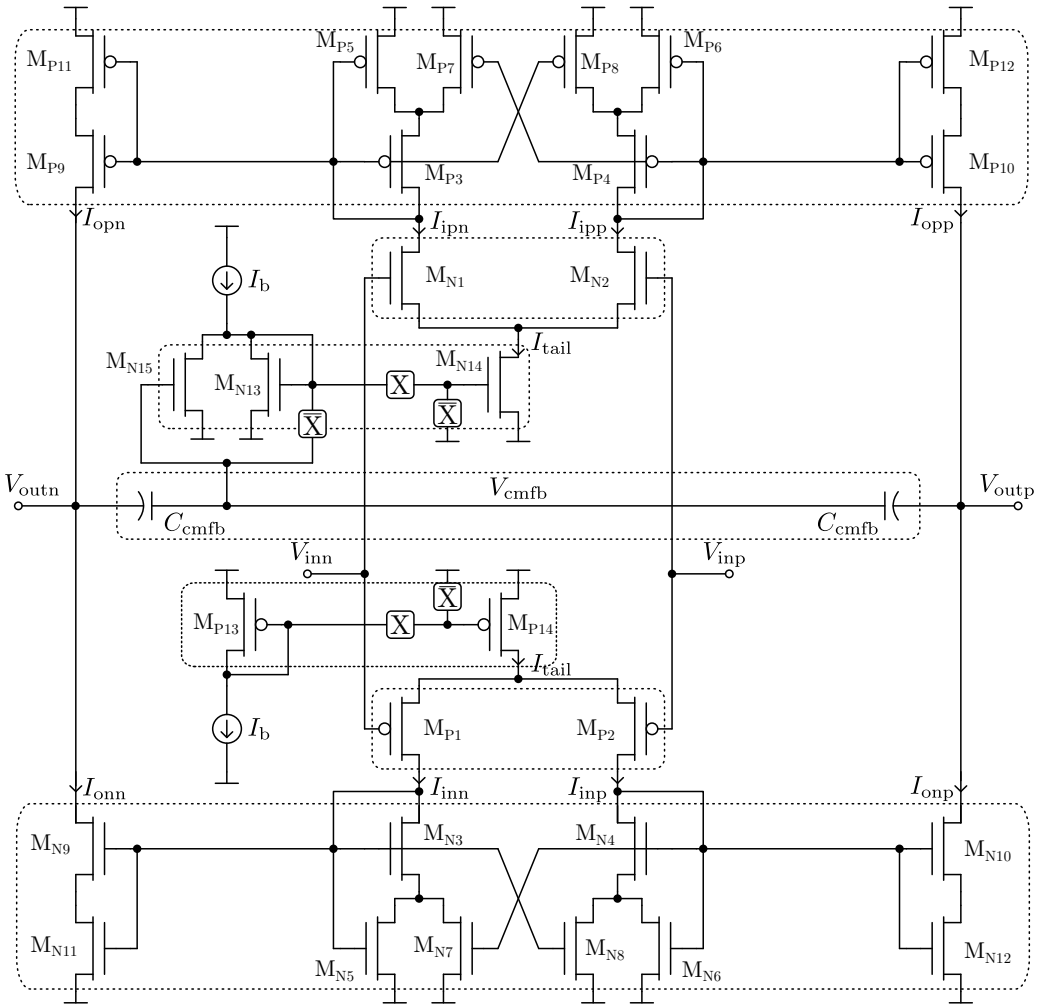

Figure 3.16 | Type-II SVMA circuit topology used in the OpAmps from Fig. 3.8. Dashed boxes indicate element matching groups.

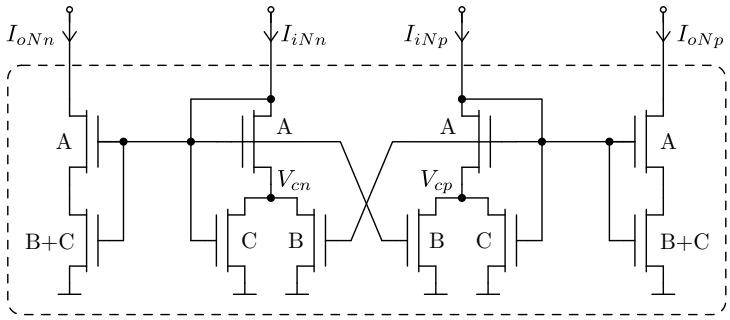

Figure 3.17 | Type-II variable current mirror from the SVMA in Fig. 3.16.

The core of this circuit is the variable current mirror, shown in Fig. 3.17. When all the tail current goes through one of the branches (e.g. $I_{\text{inp}} \approx I_{\text{tail}},\ I_{\text{inn}} \approx 0$), the circuit behaves as a current mirror with an output current given dependent only on the device matching ratios:

$$I_{\max} \simeq I_{\text{tail}} \frac{1 + \frac{A}{C}}{1 + \frac{A}{B+C}}. \tag{3.15}$$

The Class-AB peak modulation index can then be defined as:

$$k_{\text{AB}} = \frac{I_{\max}}{I_{\text{tail}}} = 1 + \frac{1}{C} \frac{AB}{A + B + C}. \tag{3.16}$$

Pushing this factor too much will increase the parasitic capacitance at the transistor gates and move the parasitic pole to low frequencies, causing stability issues. The following unified rule of thumb can be applied in order to reduce the effects of the parasitic pole [110]:

$$A = B + C. \tag{3.17}$$

By substituting the above design rule in (3.16), the optimum Class-AB peak modulation becomes:

$$k_{\text{AB}} = 1 + \frac{B}{2C}. \tag{3.18}$$

Since the proposed VMA design is a fully-differential OTA, the output common-mode is not well defined and a CMFB mechanism must be introduced in order to establish the desired output common-mode. A SC implementation is made with the capacitors and the split-N current mirror seen in Fig. 3.16. The purpose of this circuit is to set the output common mode to a desired value and to correct its variations using negative feedback. To do this, the capacitors are first pre-charged to the desired operation point by using the switches depicted in Fig. 3.16 and connecting the output to the desired common mode. The current the mirror factor is simply:

$$K_{\text{mirror}} = \frac{m_{\text{N14}}}{m_{\text{N13}} + m_{\text{N15}}}. \tag{3.19}$$

When the amplifier is turned on, any variations in the output common mode are corrected by adjusting the N-stage bias current. The solution for the open-loop small-signal CMFB

gain is given by:

$$A_{\mathrm{cmfb}} = \frac{\Delta V_{\mathrm{cmo}}}{\Delta V_{\mathrm{cmfb}}} = -\frac{1}{2}\left(\frac{m_{\mathrm{N15}}}{m_{\mathrm{N13}}} g_{\mathrm{m_{N14}}}\right) R_{\mathrm{out}}, \tag{3.20}$$

where $g_{\mathrm{m_{N14}}} = \sqrt{I_{\mathrm{tail}} m_{\mathrm{N14}} \left(\frac{W_u}{L_u}\right)}$ is the transconductance of the tail transistor. The CMFB capacitors close the loop by forcing:

$$\Delta V_{\mathrm{cmfb}} = \Delta V_{\mathrm{cmo}}, \tag{3.21}$$

so any variation in the output common mode will translate in the same variation of the control voltage. Thanks to the negative feedback from (3.20), the variations in these voltages are forced to be zero when there are no other factors involved. When such factors exist, like for example the dependency with input common mode due to non-zero common mode gain A_{cmi}, the CMFB gain will try to correct these variations, as given by:

$$\Delta V_{\mathrm{cmo}} = \Delta V_{\mathrm{cmi}} \frac{A_{\mathrm{cmi}}}{1 + A_{\mathrm{cmfb}}}. \tag{3.22}$$

Therefore, increasing the ratio $m_{\mathrm{N15}}/m_{\mathrm{N13}}$ or the tail transconductance, $g_{\mathrm{m_{N14}}}$ will increase the accuracy of the output common-mode. The value of m_{N14} will be fixed by (3.19) and I_{tail} is fixed by the OpAmp requirements, so in order to improve the tail transconductance the unit transistor size ratio, W_u/L_u should be increased. Nevertheless, if the CMFB gain is too high it can also generate common-mode instability due to the existence of parasitic poles in the common mode feedback loop. By increasing the value of the feedback capacitors this effect can be compensated, although the load capacitors are usually larger so they probably fulfill this role already. In the end, the sizing of the CMFB capacitors should be determined by the maximum affordable leakage currents and charge injection effects introduced by the MOS switches.

A strategy for the design and low-power optimization of the SVMA for a given set of ΔΣM requirements will be presented in Section 3.5.

3.4.3 SC Multi-Bit Quantizer

As explained in Section 2.1.7, the use of multi-bit quantization entails a direct improvement in the SQNR of the ADC. This improvement comes from the reduction of quantization noise, which is inversely proportional to the number of quantization levels. In addition, the quantization noise reduction results in a lower integrator output swing, allowing for more relaxed amplifier requirements, which in turn mean lower power consumption, as already mentioned. In contrast, some issues such as the increased complexity of the design and the non-linearity of the feedback DAC appear. DAC non-linearity can be addressed by means of calibration or digital correction techniques, like DEM [88]–[90].

The single-ended topology of the multi-bit quantizer used in this ΔΣM implementation is shown in Fig. 3.18a [91]. A fully-differential implementation can be built by duplicating this circuit and inverting the value of the comparator outputs for the negative half. The operation of the circuit is as follows: When ϕ_1 is active, all the capacitors are shorted to the common-mode and discharged. When ϕ_2 is on, C_0 bottom plate is connected to the

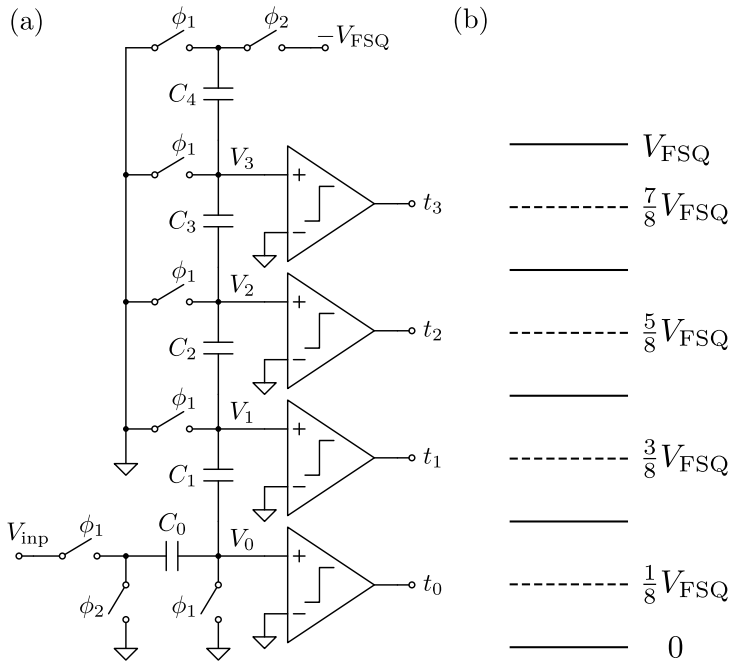

Figure 3.18 Single-ended schematic of the SC multi-bit quantizer used in the design of the ΔΣM in Fig. 3.8a and equivalent quantization levels set by the capacitor ratios (b).

input signal and the other extreme of the ladder to the negative full-scale value, $V_{\mathrm{FS_q}}$. This causes the charge to redistribute, and the quantizer levels are then set depending on the capacitor ratios. It is important to highlight that all comparators latch at the same input common-mode reference, so a single comparator design can be used for all the comparator instances in the multi-bit quantizer, which is advantageous in terms of matching and design time.

The general solution for the capacitor ratios as a function of the fully-differential number of levels L to implement the quantization thresholds shown in Fig. 3.18b is given by:

$$\frac{C_j}{C_0} = \begin{cases} \frac{4(j+n)^2-1}{4n(1+2n)} & j \in [1...n-1] \\ \frac{4n-1}{2n(2n+1)} & j = n \end{cases}, \tag{3.23}$$

where $n = (L-1)/2$ and C_0 represents the sum of all capacitors coming from the ΔΣM feedforward paths:

$$C_0 = \sum_{i=0}^{N} C_{ff_i} = C_u \sum_{i=0}^{N} \mathrm{m}_{ff_i} = C_u \mathrm{m}_0, \tag{3.24}$$

where C_u is the unitary element capacitor and m_0 is defined as the sum of all the elements. In reality, C_0 is split into a capacitor array connected to the signal input and to the output of each integration stage of Fig. 3.8, effectively acting as a passive adder right before the quantizer. Each feedforward gain factor is determined by the ratio of the specific feedforward capacitor with the total array capacitance:

$$K_{\mathrm{ff_i}} = \frac{C_{ff_i}}{C_0} = \frac{\mathrm{m}_{ff_i}}{\mathrm{m}_0}. \tag{3.25}$$

From this equation, it is obvious that the adder attenuation factor is equal to $1/\mathrm{m}_0$, so it can be calculated and back-annotated into the ΔΣM architecture of Fig. 3.1. For the 9-level design case, the exact ratios can be found to be:

$$\frac{C_1}{C_0} = \frac{11}{16}, \qquad \frac{C_2}{C_0} = \frac{143}{144}, \qquad \frac{C_3}{C_0} = \frac{65}{48}, \qquad \frac{C_4}{C_0} = \frac{5}{24}. \tag{3.26}$$

Since the least common multiple of all the values of C_0 is too large for practical layout design, the above physical ratios need to be rounded down. This is possible due to the high robustness of the circuit against errors, as shown in Fig. 3.19, where the quantizer has been modeled and incorporated into the architectural level model. The simulation using different values of C_0 shows that it is possible to choose a small C_0 multiplicity with no meaningful resolution losses. The chosen multiplicity for the proposed design was $C_0 = 12$, resulting in the following ratios which are the ones annotated in Fig. 3.8:

$$\frac{C_1}{C_0} = \frac{8}{12}, \qquad \frac{C_2}{C_0} = \frac{12}{12}, \qquad \frac{C_3}{C_0} = \frac{16}{12}, \qquad \frac{C_4}{C_0} = \frac{2}{12}. \tag{3.27}$$

Of course, this may only hold true for this specific design. The results of the simulations may change depending on the target resolution, the supply voltages, etc..., so careful modeling should be carried out in order to find the optimal multiplicity values.

The only remaining step left in the design of the quantizer is the correct scaling of all the capacitors by the absolute value of C_0, while maintaining the previously calculated

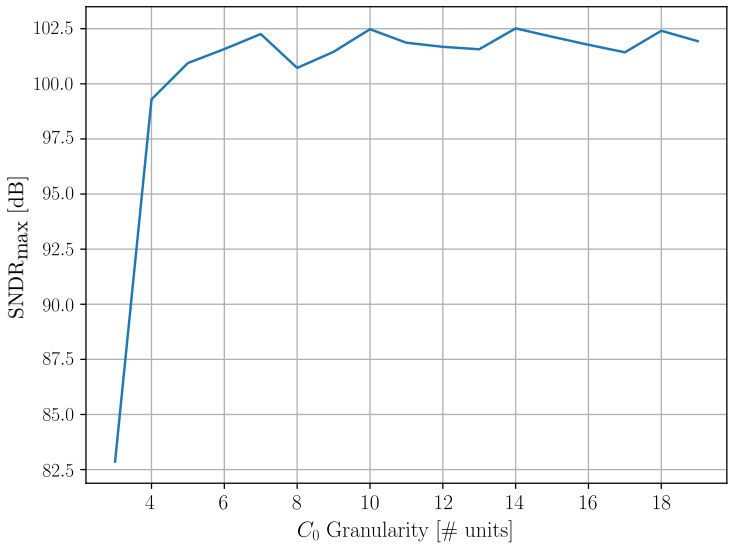

Figure 3.19 | High-level simulation showing the maximum SNDR versus C_0 granularity for the ΔΣM in Fig. 3.1.

ratios. A compact size will result in smaller area and low dynamic power consumption, but the capacitors should be large enough so that the parasitic capacitance at the quantizer nodes has no impact in the resolution. For this reason, it is necessary to model the effects of parasitic capacitance at the quantizer nodes, which may come from the comparator input stage and the layout routing.

An example of the impact of this capacitance on the resolution is shown in Fig. 3.20. From this simulation, the maximum ratio C_{par}/C_0 can be found. Then, after C_{par} is known, the optimal C_0 value can be calculated. For this reason, it is preferred to start with the comparator design so that this information is available. The value of the parasitic capacitance due to routing cannot be known precisely at this design stage, but an estimation can be done so that safe margins can be properly applied.

Comparator Design

Only a single comparator circuit design is needed for the multi-bit quantizer of Fig. 3.18, as explained previously. The type of comparator suitable for this kind of operation is a latched comparator, which will only trigger when the corresponding clock demands it. These comparators are characterized by a very high speed and a very low static power consumption.

The comparator design challenge consists on finding the best trade-off for the following parameters: speed, parasitic input capacitance, and input offset. In the first place, the comparator offset effects have to be modeled at architectural level. An example of this is shown in Fig. 3.21, where the resolution of the ΔΣM is statistically predicted by means of Monte Carlo simulations, using comparators with different input offset standard deviation

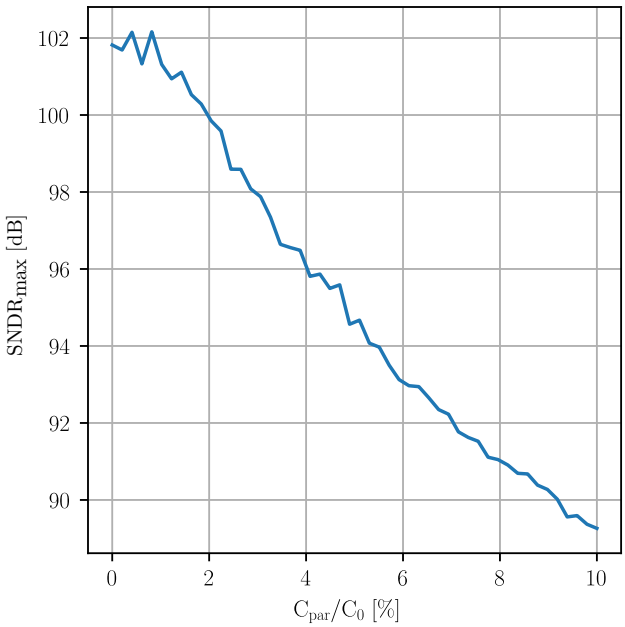

Figure 3.20 | High-level simulation showing the effects of quantizer parasitic capacitance on the resolution of the ΔΣM in Fig. 3.8.

for each of the Monte Carlo sweeps. For each of the sweeps, the mean ΔΣM resolution and its standard deviation is calculated an annotated. In the end, a relationship between the offset standard deviation and the ΔΣM resolution (i.e. mean and standard deviation) can be effectively extracted. This relationship sets the maximum allowed offset standard deviation, which can be used as a design parameter.

In order reduce comparator offset, the area of the transistors has to be increased, especially the input pair. The downside is that the input parasitic capacitance will grow, so the value of C_0 will have to be increased. In any case, the offset constraint should be solved before the parasitic capacitance is addressed.

Finally, the comparator must be fast enough to make a logical decision in the available time frame and avoid metastability issues [111]. This is set by the design of the clock generator: the duration of the time-frame can be modified depending on the implemented delays. A good rule of thumb is to build a comparator with a delay $t_{\mathrm{d_{comp}}} < 0.01 T_{\mathrm{samp}}$ for an input amplitude equal to the ΔΣM resolution.

The comparator used in the designs from this work is known as the StrongARM comparator [112]–[114] depicted in Fig. 3.22. It is a very simple topology, but proves to be enough to satisfy the requirements of the designs in this work. More complex comparator topologies may be necessary for designs with different requirements [115], in particular the use of self-calibration techniques to remove comparator offset when critical.

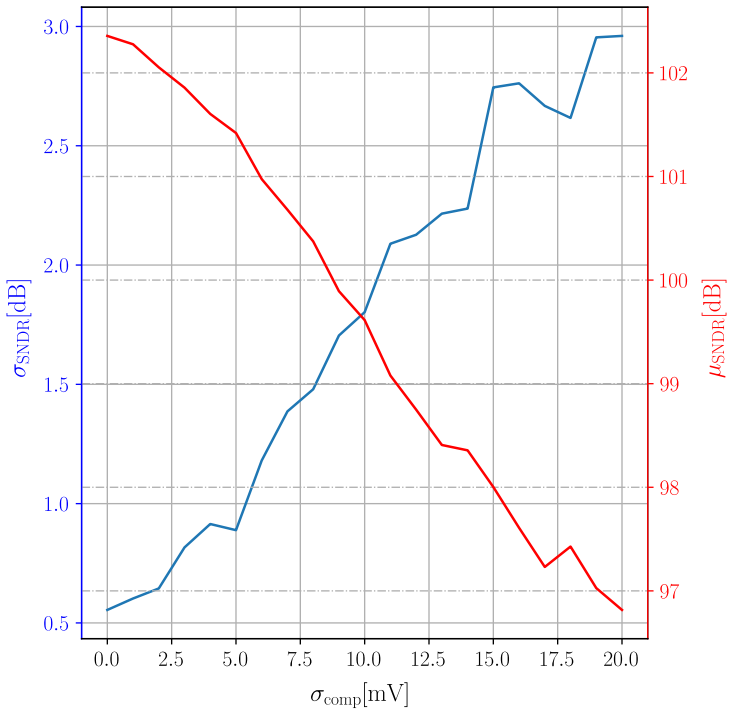

Figure 3.21 | High-level simulation of the effects of comparator offset in the ΔΣM from Fig. 3.1. The red and blue axes describe the mean resolution and standard deviation, respectively, given a certain standard deviation for the comparator input offset.

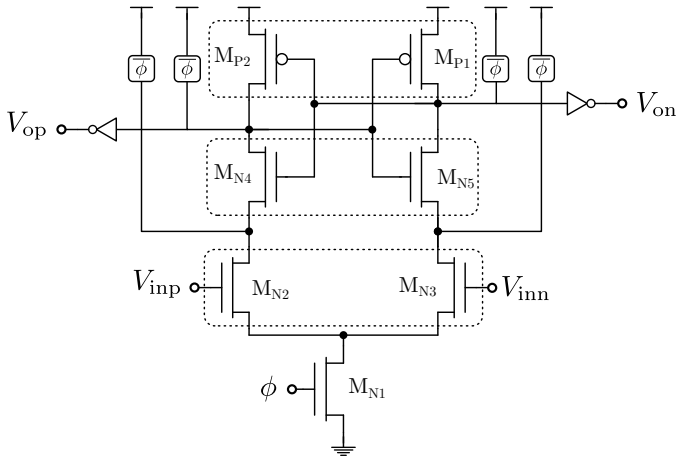

Figure 3.22 | NMOS-input StrongARM comparator circuit topology.

3.5 Design Methodology

At this point, all the fundamental principles and building blocks that take part in the design of the proposed SC ΔΣM have been explained. Given the large quantity of information, it is appropriate to summarize the design steps into an algorithm that can be followed sequentially in order to help the designer with the required tasks. A top-down design methodology is shown in Fig. 3.23, with general tasks valid for any kind of SC ΔΣM and most analog and mixed-signal ICs. Three different design phases can be distinguished: architectural design, schematic design, and full-custom layout design.

At the architectural design phase, the system is modeled mathematically with the help of specific hardware-description languages (HDL) or adapted programming languages (e.g. scientific Python). The main variables of the design are identified and optimal values are searched while checking for the fulfillment of the functional specifications. For example, this was explored when finding the optimal coefficients of the proposed multi-bit ΔΣM architecture in Section 3.1. At this stage, some constraints affecting the schematic design already appear and must be accounted for.

Once the specifications are satisfied at architectural level, the next step is to choose the electrical topology of the circuit. This selection must be done wisely, taking into account the possible issues the topology can introduce when trying to move the architectural design to the circuit implementation. In order to help with this selection, high-level non-idealities from the topology should be modeled and incorporated to the high-level architectural models, when possible. By doing this, the topology can either be discarded or validated and, in the later case, important topological information, which will be helpful at the design of the schematic blocks, can be extracted.

The next stage is the schematic design, which is specific for each of the circuit blocks. This stage will be explained in detail for the ΔΣM presented in this work shortly. The information obtained from architectural level simulations is used at this stage to design each of the blocks in the schematics. After the schematic design is validated, layout design can start. The physical design is validated by asserting that the layout description of the circuit corresponds to the schematic, via a layout versus schematic (LVS) tool. Then, it must be ensured that the layout complies with the manufacturing rules provided by the foundry, using a design rule checker (DRC) too. After this, the layout can be extracted to obtain a schematic representation of the parasitics that will be introduced by the CMOS manufacturing process. This extracted schematic is simulated so that the proper operation of the circuit can be checked again, now with a higher degree of reliability. If parasitics have degraded the performance in excess, then changes should be made to the mask layout and even to the schematic when no solution is found at the layout stage. Once the simulations validate the correct performance of the layout, the design is ready for tape out.

The specific steps for design of the SC ΔΣM analog core are summarized in the methodology from Fig. 3.24. At this point, all the information from high-level simulations is available.

The first step is to set the matching groups and capacitor rations, which are set by

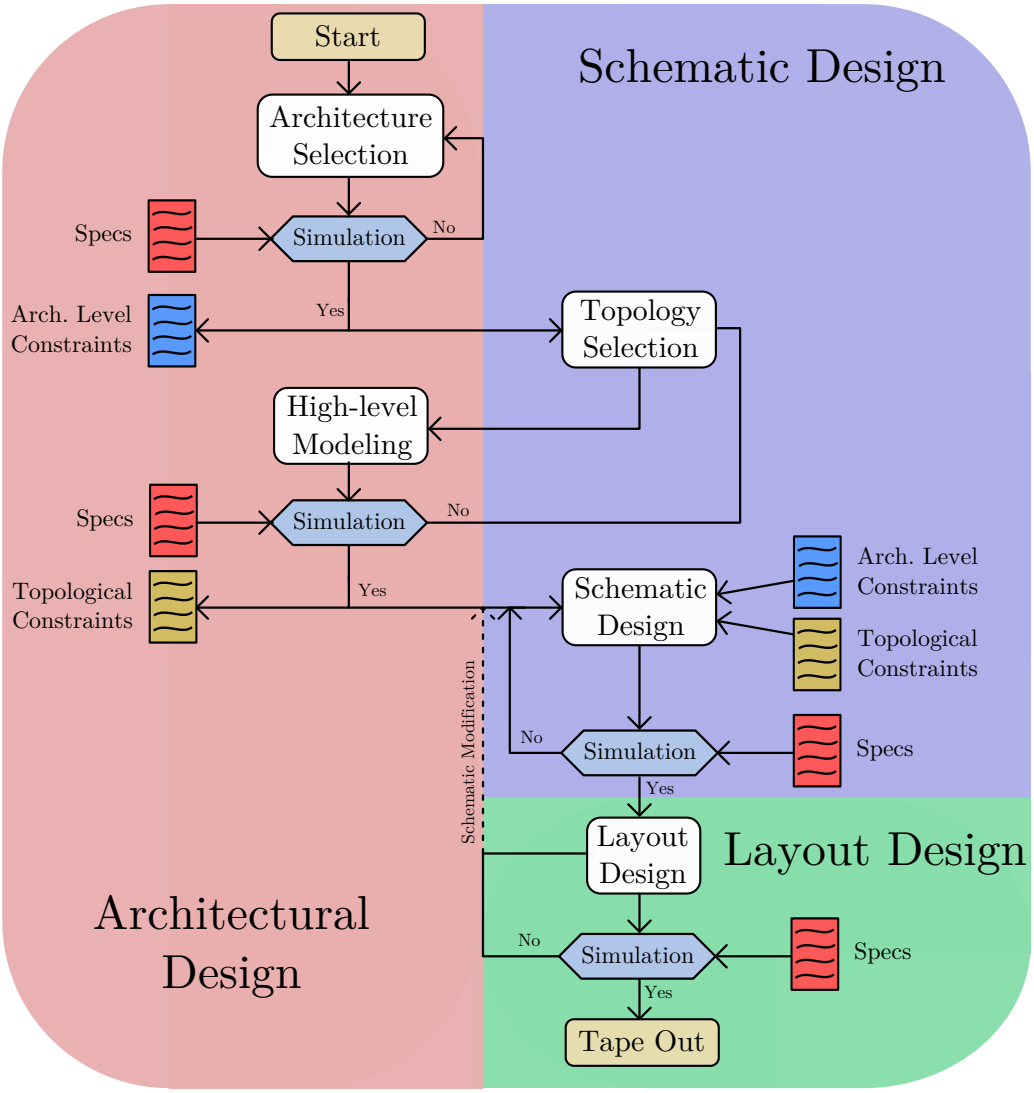

Figure 3.23 General top-down design methodology for full-custom analog and mixed-signal ICs.

the already known coefficient values. The same must be done for the multi-bit quantizer capacitors, whose ratios were already calculated in Section 3.4.3. Next, the absolute value of the sampling capacitor can be found by calculating the maximum allowed noise for a given resolution specification, using (2.45). The second stage capacitors can be sized just by downscaling the capacitors of the first stage by some factor. Noise is not a problem for practical values of these capacitors, but only mismatch and parasitics.

The next step is the single design of the comparator circuit. This block must comply with the speed and offset requirements set from the topological constraints. The fulfillment of the offset requirement will determine the input parasitic capacitance of the comparator. Once a suitable comparator has been built, the parasitic capacitance can be measured so that the information can be used to size the quantizer unit capacitors, by using the constraint C_{par}/C_0 obtained from topological modeling.

At this point, all the capacitor values are solved, so its time to size the SC switches, The design of CMOS switches consists on finding a suitable resistance value so that the RC branches of the circuit comply with the minimum required bandwidth. The suitable ratio between the NMOS and PMOS transistors should be found as well with the purpose of increasing the linearity of switch resistance as much as possible. Oversizing the transistors is not the best idea, since it will increase charge injection effects and also increase the fanout requirements of the digital drivers.

The last step is to design the SVMAs. Since the topology is somewhat complex, a specific design algorithm has been developed for this block, as shown in Fig. 3.25.

The design and optimization of the SVMA consists on satisfying the noise, speed, stability, and gain requirements while keeping the power consumption of the amplifier to a minimum. The key design parameter of the SVMA is the factor k_{AB}. By increasing this factor, the speed of the amplifier will improve without requiring additional power consumption. However, increasing k_{AB} requires increasing the multiplicity of several core transistors following (3.18), so a parasitic pole will appear, affecting the stability of the amplifier. Therefore, the design optimization consists in finding the optimal k_{AB} value among other design variables.

Fig. 3.25a shows the proposed algorithm to follow in an attempt to find the optimal values from a starting point. An example of an optimization process is shown in Fig. 3.25b. In this example, the starting values exceed the requirements, so the power consumption in the form of a tail current is decreased after some iterations where as other variables such as k_{AB} change to compensate the reduction in current. In the end, a better design point is found where the current consumption has been reduced and the specifications are enough to fulfill the requirements. After a large number of iterations, all the design parameters would converge to an optimal value, as it starts to happen at the end of the given example.

The last step in the schematic design is the implementation of the digital blocks. At this stage, the classic semi-custom design methodology for digital ICs can be followed to ensure that the timing and logical functionality of the blocks is correct. Some of the blocks can even be synthesized and placed-and-routed to relieve the designer from additional full-custom work [116].

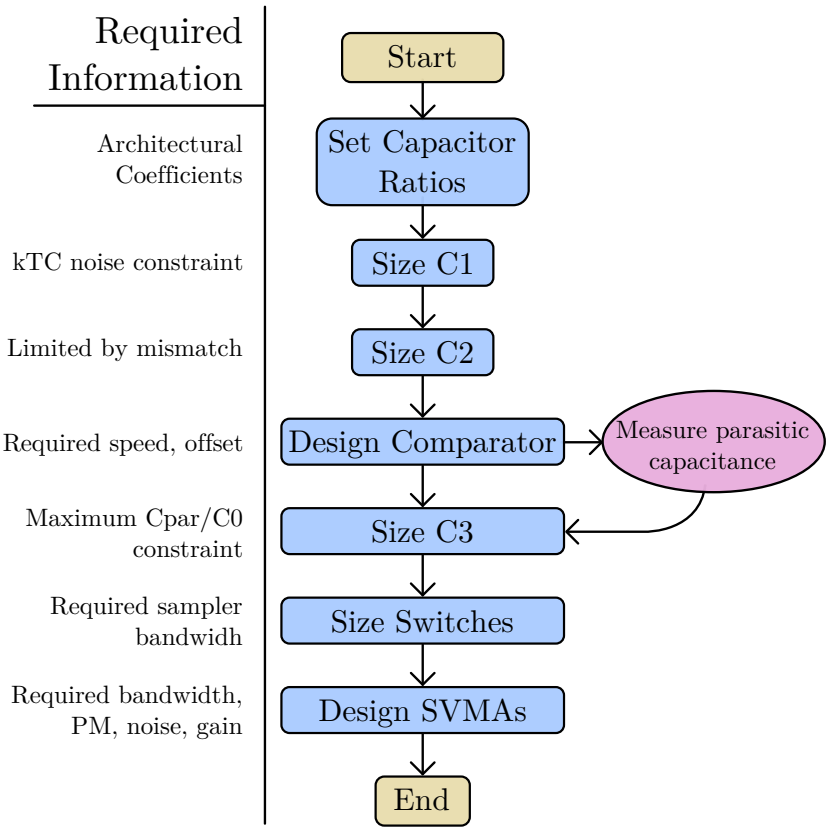

Figure 3.24 Schematic design methodology for the analog core of the multi-bit SC ΔΣM proposed in this chapter.

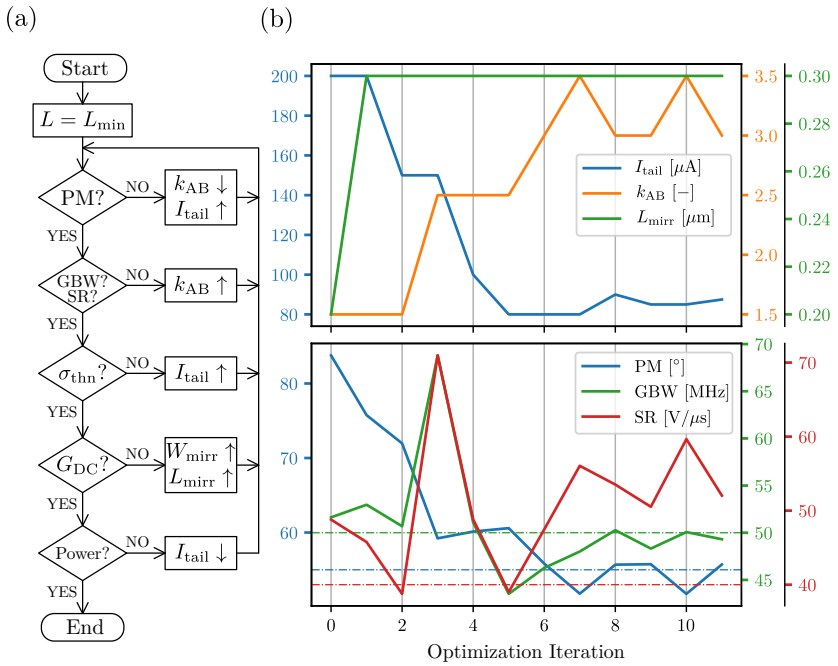

Figure 3.25 | SVMA design algorithm for power optimization (a) and example of the optimization process (b).

Finally, after the schematic design has been validated, the layout design phase can start. At this stage, general design strategies for device matching and reduction of parasitics should be followed [117]. For the ΔΣM specific design, it is also important to provide a good isolation between the analog and digital routing, as well as reducing the parasitic capacitance as much as possible on the most critical nodes (e.g. multi-bit quantizer, OpAmp inputs). Analog and digital supplies need to be isolated to prevent supply coupling from the digital circuitry to the critical analog parts, dedicating a different supply rail for each of them. The analog and digital ground nodes are also isolated at block level but joined again at chip level by higher impedance paths, since ground must be common for both supply domains. By doing this, the current flow is well controlled and cross-domain couplings are avoided.

3.5.1 Mitigation Techniques for Radiation Effects

As stated in Section 1.3, an objective of this PhD thesis is the design of ADCs suitable for space applications. The space environment is full of radiation sources that can damage the electronic circuits [118]. On Earth, these circuits are protected by its atmosphere and magnetic field, but at open space this protection is lost. Long-term space missions will require the ICs to endure this conditions for long periods of time, accumulating thus large radiation doses that will degrade the circuits even to the point where they cease to work. For this reason, radiation hardening design methodologies should be applied to ICs

Cumulative	SEE	
	Non-Destructive	**Destructive**
TID	SET	SEL, SESB
	SEU	SEHE
TNID	MCU, MBU	SEB
	SEFI	SEGR, SEDR

Table 3.1 Summary of the most important radiation effects in electrical components.

intended for these kind of missions.

The radiation effects in ICs can be classified into cumulative effects and SEEs [119]. Cumulative effects include total ionizing dose (TID) and total non-ionizing dose (TNID). TID effects are induced by ionizing energy coming from radiation exposure, creating electron-hole pairs in the component material. This charges get trapped in dielectric layer producing undesired effects on the IC, such as metal-oxide semiconductor field-effect transistor (MOSFET) threshold voltage shift, leakage currents, and timing skews. TNID, instead, are induced from the non-ionizing transfer of energy, eventually creating damage to the semiconductor crystal lattice. This produces a variety of effects in bipolar devices and all kinds of opto-electronics. Typically, ASICs and field programmable gate arrays (FPGAs) are not affected by TNID.

SEEs can be induced by the deposit of an ionizing particle in the circuit. They are classified into non-destructive and destructive SEEs, depending if the effect is temporary or if it has done some permanent damage. Some of the non-destructive effects are: single event transient (SET), which induces a transient voltage spike at some node in the circuit, single event upset (SEU), consisting on a single bit flip of some storage element induced by a single particle, multiple-cell upset (MCU) and multiple-bit upset (MBU), similar to SEU bit affecting several cells or bits, respectively, and single event functional interrupt (SEFI), which causes the component to reset, lock-up, or malfunction. Some destructive SEEs are: single event latch-up (SEL), which triggers the parasitic PNPN (or NPNP) bipolar structures in CMOS producing latch-up, single event snap-back (SESB), less common but similar to SEL, which triggers a parasitic NPN (or PNP) bipolar, single event hard error (SEHE), which damages permanently a storage cell, single event burnout (SEB), which is similar to SEL but affects power transistors and is potentially destructive, and single event gate rupture (SEGR) or single event dielectric rupture (SEDR), which cause the rupture of the gate oxide or any dielectric layer, respectively. All these effects are summarized in Table 3.1.

Out of all the errors described, the most important errors affecting ADCs are: TID, SEL, SEGR or SEDR and SEFI. SEU and SET effects may also be important, but the proposed $\Delta\Sigma$M architecture is inherently robust to this kind of errors; a transient error resulting in the corruption of a data sample will translate into a high-frequency error which can be filtered out due to the high OSR employed by the $\Delta\Sigma$M loop.

In order to mitigate these effects, several actions have been taken into account different design levels. At technology selection stage, triple-wells have been selected as they have

Mitigation Actions	**Mitigated Errors**	**Reference**
Triple-well structure	SEL, MCU/MBU, SEFI	[120], [121]
TMR	SET, SEU, SEFI	[122]
Differential design	SET	[123]
Guard-ring structures	SEL	[124]
Node separation and Inter-digitation	SET, SEU, SEFI	[125]

Table 3.2 | Summary of the mitigation actions taken during the full-custom design of the multi-bit SC ΔΣM in Fig. 3.8.

been proven to reduce the effects of SEU and SEL [120], [121]. At schematic level, redundancy has been added to the digital memory storage elements by using a triple modular redundancy (TMR) logic structure [122]. Because the number of storage cells in the design is very small, this could be implemented at low cost. Regarding the analog domain, the use of a fully-differential topology helps mitigating the effects of SET [123]. At layout design stage, the use of guard-rings has been employed in order to improve robustness to SEL [124]. Critical node separation, inter-digitation and other matching techniques have also been used, improving robustness to SET and SEU [125]. The summary of the mitigation actions taken during the design of the ΔΣM from Fig. 3.8 can be found in Table 3.2.

Floating-Point ΔΣM with Distortion-Less AGC | 4

In this chapter, a new ΔΣM architecture incorporating AGC capabilities is proposed. An introduction to classic AGC strategies is first given, highlighting the fundamentals of operation and their limitations. Next, the Floating-Point ΔΣM architecture is presented, explaining the most important design points and the non-idealities the architecture suffers from. Finally, a SC implementation for the proposed architecture is detailed, showing the necessary circuit modifications to be applied to a regular ΔΣM in order to incorporate the novel AGC solution.

4.1 Sensing Scenario

Many common ubiquitous smart sensing applications demand ADCs exhibiting low-power operation, a bandwidth in the kHz range, and capable of handling large DR signals. This is the case of applications such as audio sensors or biomedical devices acquiring electrophysiological signals, among others. A common approach for extending the DR of the ADC is to increase its maximum SNDR. However, since the instantaneous SNDR requirements in these scenarios are typically much lower than the overall signal DR, this approach can impose unnecessary penalties in terms of power consumption.

Typically, AGC is employed in this kind of applications. The principle behind AGC is to adapt the amplitude of the signal driving the ADC to its rated full-scale value by applying a variable gain to the sensor signal, as depicted in Fig. 4.1a. The classic implementation consists on a PGA at the input, followed by the ADC. The ADC data is usually managed by some digital signal processor (e.g. DSP) which adjusts the gain of the PGA so that the signal is adapted to the optimal ADC input requirements, as shown in Fig. 4.1b [126]. By doing this, the overall DR of the ADC is extended. This solution, however, presents some disadvantages. The most obvious is the addition of the PGA, which will increase the design complexity and power consumption, since its performance should be better than the ADC itself to avoid resolution loss. Otherwise, extra noise and distortion may appear. Another disadvantage is that important signal distortion will appear when switching around the

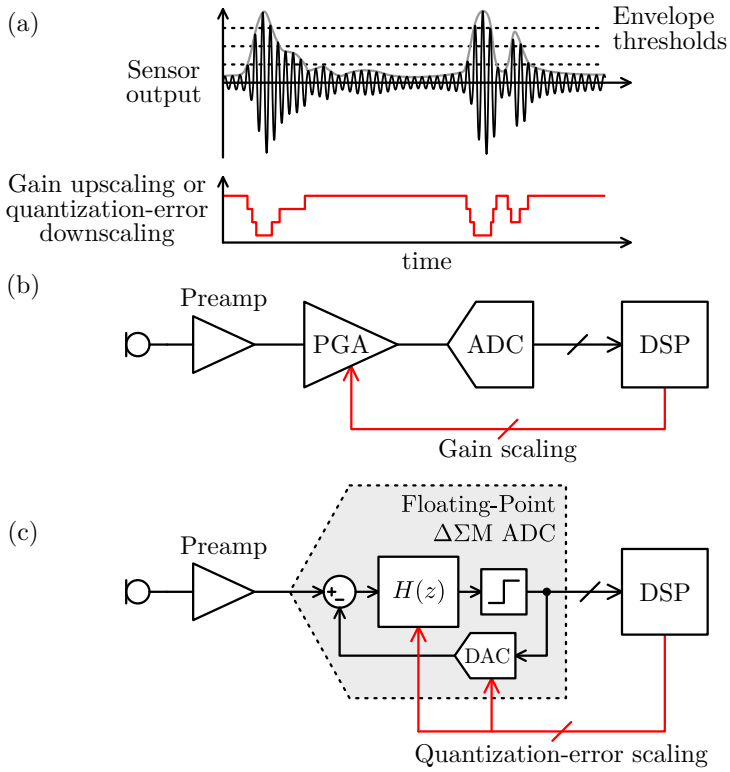

Figure 4.1 Example of a high DR signal and the feedback gain calculated by the DSP (a), classic AGC system (b) and proposed ΔΣM with built-in AGC (c).

PGA gain if there are state variables in the basic ADC functionality, as the is the case in ΔΣM [127].

To illustrate this issue, a simulation example for the classic AGC system of Fig. 4.1b is given in Fig. 4.2. The PGA of this system has non-zero values for the attack and release times, meaning it needs some settling time from the moment the amplitude control rises or lowers, respectively, to the moment the output gain actually reaches its desired value. This is actually desired for applications such as audio; the settling time constants prevent discontinuities from appearing at the AGC output that would sound annoying when driving a speaker. However, for other applications where the signal is re-scaled back to the original amplitude, because recovering the original amplitude might be needed, the discontinuities will appear (see Fig. 4.2a). The PSD of this signal in Fig. 4.2b shows heavy harmonic contents in the spectrum due to the AGC operation.

The proposed approach in this work takes inspiration from a technique named Analog Floating Point (AFP) [127] by analogy to the floating point representation of numbers in the digital domain. The key of AFP resides in updating the state variables of the ADC in accordance to the applied AGC feedback gain. If this was not done, when the input gain changes from k_{n} to $k_{\mathrm{n+1}}$, the state variables become smaller relative to the input by a

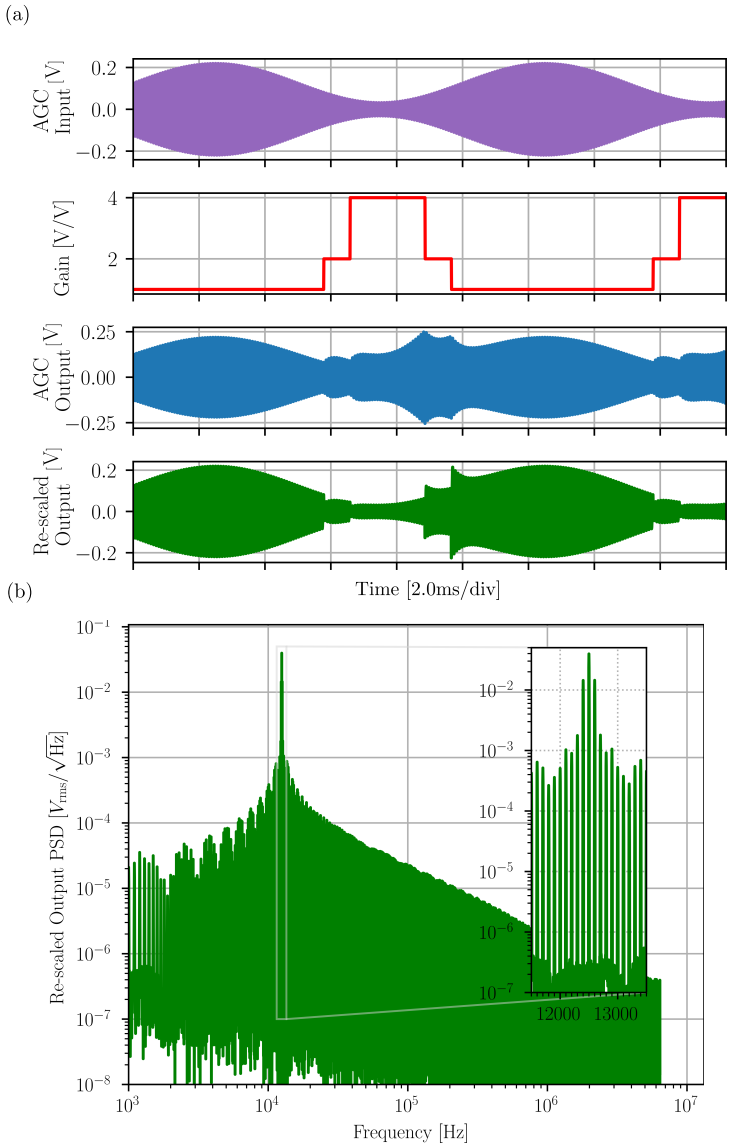

Figure 4.2 | Simulation example of the classical AGC system of Fig. 4.1b when applied to an AM signal. Time-domain signals (a) and PSD of the reconstructed signal (b).

factor k_n/k_{n+1}, being this lack of coherence the cause of the distortion explained in the introduction.

This strategy is applied to SC ΔΣM architectures, with the addition of also incorporating the input gain stage inside the same architecture in order to allow the direct implementation of AGC loops following Fig. 4.1c. By doing this, the finite bandwidth issues of the PGA are also prevented. The derivation of this architecture comes from the idea of scaling the quantization error, instead of the input signal, to achieve the DR range extension. By following this approach, an equivalent architecture employing the AFP technique will be obtained, in which all the internal ΔΣM state variables will be updated accordingly to the dynamic gain, as it will be shown shortly.

This new architecture achieves the desired DR extension without the cost of increasing SNDR by the same amount. Thanks to the removal of the PGA as the input gain stage power consumption is kept at a minimum, being a suitable architecture for low-power and large DR applications. Also, it will be shown that the proposed tuning of the quantization error does not imply any change in the quantizer itself, so the technique can be used either with single or multi-bit architectures.

4.2 Floating-Point Architecture

As explained, the main idea of classic AGC is to amplify the signal at the input of the ADC in order to improve the SNDR and increase the overall DR. This approach has two important disadvantages: firstly, the modification is done in the signal path, so extra noise and distortion will be added to the input due to non-idealities in the PGA realization and, secondly, because ΔΣM rely on internal state variables (i.e. memory), simple amplification at the input without the updating of these state variables will result in extra distortion.

For these reasons, the approach followed in the derivation of the Floating-Point ΔΣM architecture is to scale down the quantization noise instead of scaling up the signal amplitude. In order to illustrate the adoption of Floating-Point ΔΣM architectures, the discrete-time single-bit third-order feed-forward linear model in Fig. 4.3 is taken as basis for the implementation. The optimal coefficients are obtained by following the same procedure explained Chapter 3 in the design of the Multi-Bit ΔΣM. In any case, the Floating-Point modification can be extended to any architecture.

In Fig. 4.3a, $k_{fp}[n]$ has been introduced to dynamically downscale the quantization noise $V_{qn}[n]$. Nevertheless, the realization of this scaling factor would require increasing the number of quantizer levels by the same factor. This would be equivalent to realizing a multi-bit ADC and changing the levels dynamically; something that would not make sense, since this is equivalent to increasing the maximum SNDR and the optimal solution would be to always use the maximum number of levels. Besides, this realization would do nothing regarding kTC noise scaling, which is the most important practical aspect limiting the resolution, as introduced later on.

In order to find a suitable implementation, the scaling factor $k_{fp}[n]$ can be propagated around the architecture while keeping its mathematical equivalence, until arriving to the

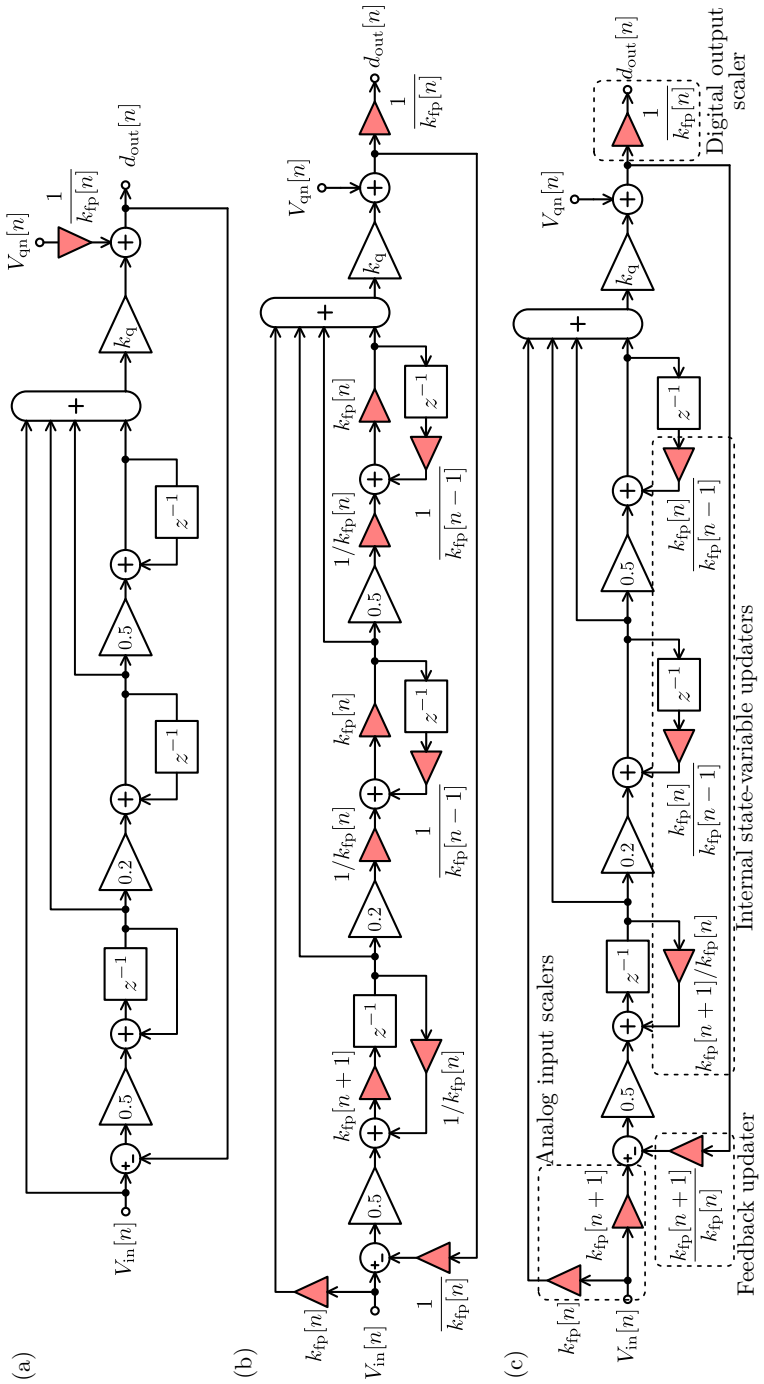

Figure 4.3 Linear model of a single-bit third-order ΔΣM architecture with scalable quantization (a), correction propagation (b) and proposed realization (c).

architecture shown in Fig. 4.3c which is oriented to proper circuital implementation. From the resulting circuit, several new blocks can be distinguished. Firstly, the two scaling coefficients at the analog input essentially play the role of a PGA in classic AGC by scaling the input amplitude. As proposed in Section 4.3, these coefficients will be implemented through the SC input sampler itself to provide distortion-less amplification and kTC noise scaling as well. Secondly, the inverse factor is required at the digital ΔΣM output in order to recover the original amplitude, as would be expected. This scaling factor can be easily applied by the DSP back-end or even implemented in silicon just by applying some bit-wise shifting if power-of-two factors are chosen.

So far, these is how classic AGC operates, but the proposed approach results in additional blocks: the so called feedback updater and internal state variable updaters. These coefficients have a transient nature; their value is only different to 1 when the gain transitions. The purpose of such coefficients is to properly scale the internal state-variables of the ΔΣM so that the gain change goes unnoticed and coherence is maintained. By doing this, the switching noise and distortion from the AGC feedback is prevented.

The circuit implementation of these feedback and memory updaters can be strongly simplified if (1); the discrete set of k_{fp} values follows a geometric progression of common ratio r, like for example $k_{\mathrm{fp}} \in 1, 2, 4, 8, ...$ (i.e. $r = 2$), and (2); the upscaling and downscaling sequences in $k_{\mathrm{fp}}[n]$ strictly respect the progression sorting, like $k_{\mathrm{fp}}[n] = [2, 4, 8, 4, 8, 4, 2, 1...]$. Then, any updater coefficient from Fig. 4.3c can only take two possible values (besides $\times 1$): $\times r$ or $\div r$ ($\times 2$ or $\div 2$ for the previous example). Condition (2) allows just one-step change of $k_{\mathrm{fp}}[n]$ per sample, but this limitation does not affect the practical operation of the AGC thanks to the oversampling employed by the ΔΣM.

By simulating the architecture in Fig. 4.3c, the characteristic SQNR curve of the ADC architecture is obtained in Fig. 4.4. This particular implementation has a set of three scaling factors: $k_{\mathrm{fp}} \in 1, 2, 4$. Actually, the composition of Fig. 4.4 is built by setting k_{fp} to each different factor and then sweeping the input signal amplitude. The red line shows the best SQNR that could be achieved at each input amplitude by using an optimal AGC control from the DSP stage. This would correspond to increasing the scaling factor by 2 after a 6 dB input power loss. By doing so, the SQNR is restored back to its maximum value and, if an infinite number of scaling factors was implemented, it would be possible to sustain this recovery process indefinitely. Therefore, the maximum achievable DR when only taking into account quantization noise is:

$$\mathrm{DR} = \mathrm{SQNR}_{\max} + 6 \log_2 k_{\mathrm{fp}_{\max}} \ [\mathrm{dB}]. \tag{4.1}$$

This expression only holds when quantization noise is the dominant contribution. The next section will show the effects of kTC and the way they are mitigated.

4.3 SC Circuit Implementation

Fig. 4.5a presents the fully-differential topology proposed for the single-bit third-order Floating-Point SC ΔΣM. The implementation requires three SOAs, which are implemented

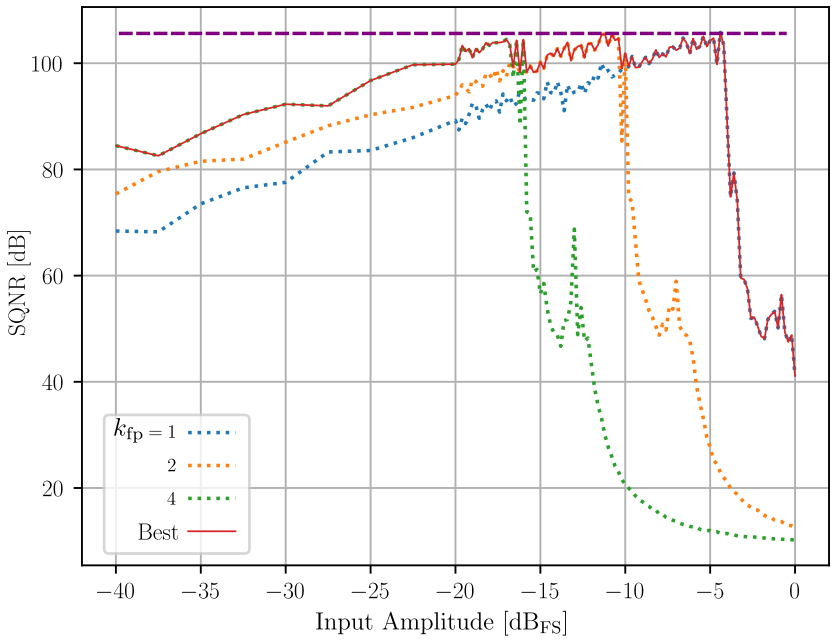

Figure 4.4 Simulated SQNR from the architecture in Fig. 4.3 for each k_{fp} scaling factor. The continuous red line shows the best resolution achievable at each input amplitude point with an optimal AGC control.

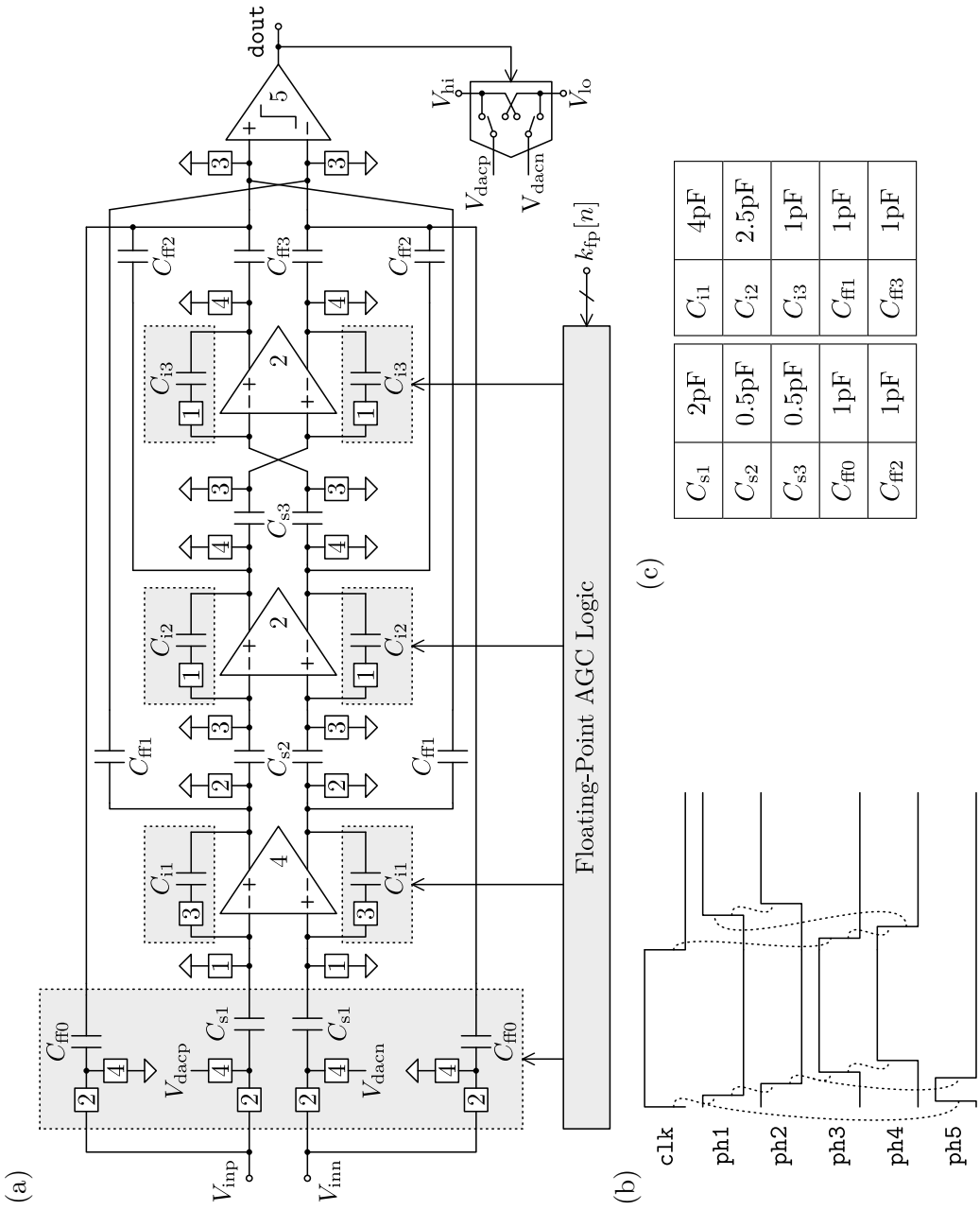

Figure 4.5 Simplified schematic of the single-bit third-order SC Floating-Point ΔΣM circuit (a), phase switching scheme (b) and capacitors sizing (c).

using the Class-AB single-stage VMA topology described in Section 3.4.2. Since a single-bit quantizer is employed, only a simple comparator is required. The StrongARM topology is selected for this design, as well. The capacitors values are shown in Fig. 4.5c, and its sizing follows the same methodology that was explained in the design of the Multi-Bit $\Delta\Sigma$M in Chapter 3, with the exception of the multi-bit quantizer.

The SC circuit operates at a nominal sampling frequency of 12.8 MHz (i.e. OSR = 128 for 50 kHz bandwidth), following the multi-phase clock scheme of Fig. 4.5b for the purpose of minimizing non-linearity caused by switch charge injection. The input signal is sampled into the first-stage sampling capacitor when the master clock is low, and integrated when it is high. As the first-stage integration takes place, the resulting value is sampled into the second and third-stage sampling capacitors, both of which work synchronously. The comparator is triggered at the end of the first-stage sampling phase, so that the single-bit feedback DAC is updated before the first-stage integration starts.

This classic implementation can then be modified with the purpose of implementing the scaling set $k_{\text{fp}} \in 1, 2, 4$ and providing AGC capabilities to the ADC. The circuits blocks to be modified are depicted by shadowed boxes. The following sections explain the operation principles of these modifications so that the coefficients from Fig. 4.3c can be implemented.

4.3.1 Input Scaler and Feedback Updater

One of the circuit modifications required by the Floating-Point $\Delta\Sigma$M is the addition of the input scaler and feedback updater. The purpose of this block is to provide input amplification to the input sampler and the feedforward path, similar to the role of a PGA, and also to provide the correct scaling at the feedback DAC necessary for the state variable updates during gain transitions.

The particular implementation for the scaling set $k_{\text{fp}} \in 1, 2, 4$ is shown in Fig. 4.6. The input scaling is embedded by substituting the sampling and feedforward capacitors by a capacitor array. This allows increasing the input capacitance when necessary using the adequate control signals. For example, when the gain scaling factor is incremented by $\times 2$, the input sampling capacitance is doubled so that the sampled charge is also doubled. Since the integration capacitor value always remains constant, this effectively means the sampled signal will be scaled by $\times 2$ once it is integrated. The value if this integrator capacitor is calculated using the base value of the sampling capacitors:

$$C_{\text{i1}} = \frac{C_{\text{s1}}}{a_1}, \tag{4.2}$$

so, when amplification is chosen, the effective integration coefficient is:

$$A_1 = k_{\text{fp}} \frac{C_{\text{s1}}}{C_{\text{i1}}} = k_{\text{fp}} a_1, \tag{4.3}$$

scaling up the input signal by k_{fp}. At this point, the important effect kTC noise has in this architecture can be introduced. In fact, kTC not only limits the maximum resolution of the ADC, but also the efficiency of the Floating-Point gain. By looking at the circuit in

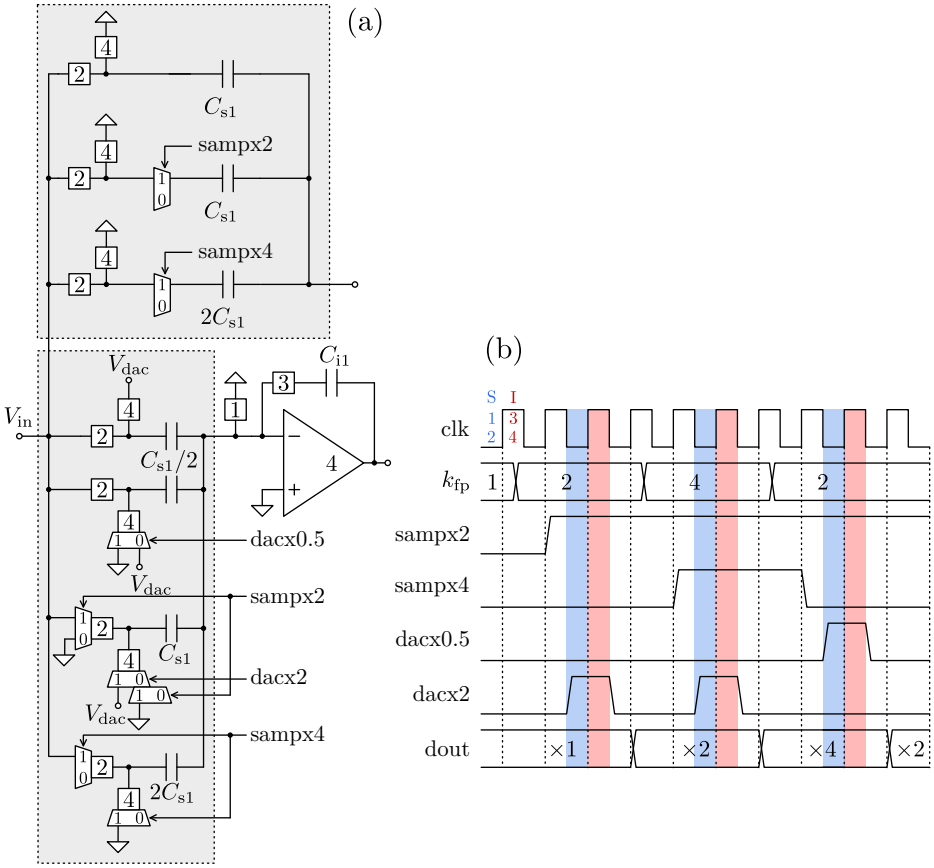

Figure 4.6 Single-ended circuit (a) and operation (b) of the Floating-Point ΔΣM input scaler and feedback updater. Blue and red shadowed regions show the instants of gain transition during sampling and integration stages, respectively.

Fig. 4.6, it is clear that the total sampling capacitance is related to the scaling factor by:

$$C_{\mathrm{s1_{tot}}} = k_{\mathrm{fp}} C_{\mathrm{s1}}, \tag{4.4}$$

so the total in-band kTC noise power coming from the sampling process becomes:

$$\sigma^2_{\mathrm{kTC_k}} = \frac{1}{\mathrm{OSR}} \frac{k\mathrm{T}}{k_{\mathrm{fp}} C_{\mathrm{s}}} = \frac{\sigma^2_{\mathrm{kTC_1}}}{k_{\mathrm{fp}}}, \tag{4.5}$$

where $\sigma^2_{\mathrm{kTC_1}}$ is the refence level when $k_{\mathrm{fp}} = 1$ (i.e. when only the base capacitor is employed). From this equation it can be stated that kTC noise power is reduced by 3 dB each time the Floating-Point gain factor is doubled. This noise contribution is also amplified by the scaling coefficient that is applied to the input signal so in the end, assuming kTC noise is the dominating contributor, the SNR can be calculated as:

$$\mathrm{SNR}_k = \frac{k^2_{\mathrm{fp}} S_{\mathrm{in}}}{k^2_{\mathrm{fp}} \sigma^2_{\mathrm{kTC_k}}} = k_{\mathrm{fp}} \frac{S_{\mathrm{in}}}{\sigma^2_{\mathrm{kTC_1}}} = k_{\mathrm{fp}} \mathrm{SNR}_1, \tag{4.6}$$

being SNR_1 the reference when $k_{\mathrm{fp}} = 1$. Equation (4.6) shows that the actual SNR improvement that can be achieved by doubling the scaling factor is only 3 dB. If kTC noise is not the dominating contributor, the improvement could increase up to 6 dB when quantization noise assumes this role. Nonetheless, this is usually not the case in high-resolution ADCs. The simulation in Fig. 4.7 illustrates the effects of kTC noise in the proposed architecture. The simulation results show a maximum resolution trend following a slope of 0.5dB/dBFS. Hence, the DR improvement of the ADC is determined by the following equation:

$$\mathrm{DR} = \mathrm{SNR}_{\mathrm{max}} + 3 \log_2 k_{\mathrm{fp_{max}}} \ [\mathrm{dB}], \tag{4.7}$$

which states an improvement of 3 dB can be achieved every time the scaling factor is doubled.

Coming back to the discussion in Section 4.2, two conditions were stated when defining the Floating-Point gain sets so that the circuital implementation can be simplified. When these conditions are met, the feedback updater coefficient can only take two possible values besides $\times 1$: $[\times 0.5, \times 2]$, no matter the number of k_{fp} levels implemented. This allows the implementation of the feedback updater without requiring additional capacitors; it only requires one of the unit capacitors to be split into two half-units. By doing this, all the coefficient values can be implemented with the appropriate switch control.

A better explanation on how this coefficient is applied is illustrated Fig. 4.8. For a $2 \rightarrow 4$ gain transition, the control will start the operation at the following sampling stage. At this point, the signals *sampx2* and *sampx4* will enable, prompting the use of a total sampling capacitor $C_{\mathrm{s_{tot}}} = 4C_{\mathrm{s}}$, as described by (4.4), thus providing the $\times 4$ amplification needed at the input (see Fig. 4.8a). Then, at the following integration stage (Fig. 4.8b), the signal *dacx2* is enabled so that the DAC voltage is connected to two of the unit capacitors, applying the necessary $\times 2$ coefficient of the input scaler. Once the transition ends, as long as the Floating-Point gain does not change subsequent cycles will keep *dacx2* disabled, since this transient gain is not necessary during static operation. The sampling capacitors will stay connected to provide input amplification until the gain is changed.

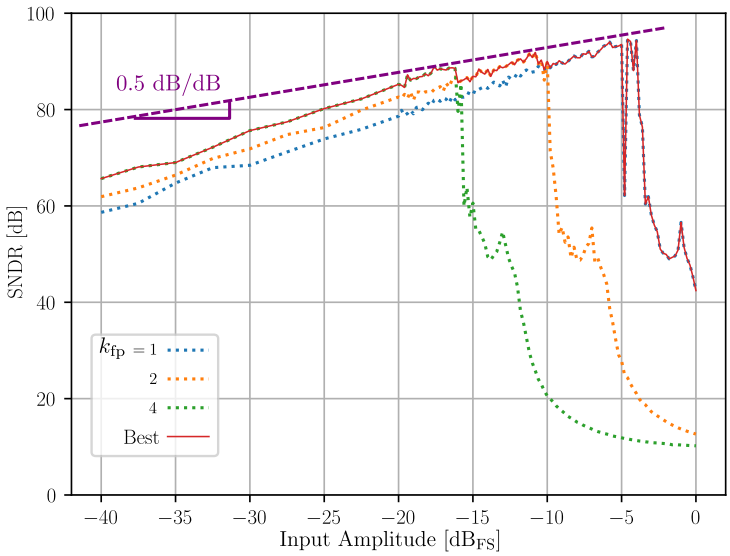

Figure 4.7 Simulated SNR from the architecture in Fig. 4.3, now including kTC noise, for each k_{fp} scaling factor. The continuous red line shows the best resolution achievable at each input amplitude point with an optimal AGC control.

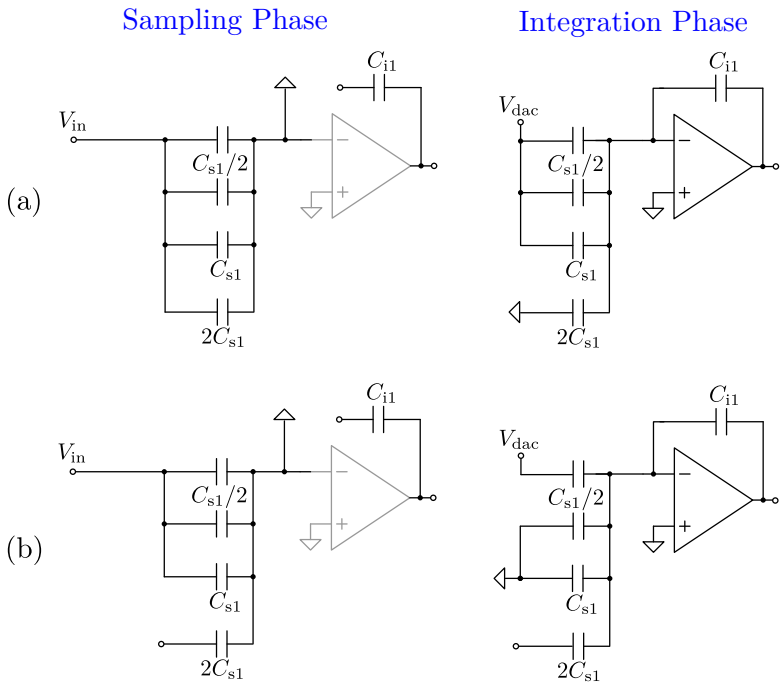

Figure 4.8 First SC integration operation during $2 \rightarrow 4$ (a) and $4 \rightarrow 2$ (b) input gain transitions.

For a $4 \rightarrow 2$ gain transition, instead, the signal *sampx4* will be disabled while keeping *sampx2* enabled in order to reduce the input gain (Fig. 4.8c). At the following integration stage (Fig. 4.8d), the signal *dacx0.5* is enabled and disconnects one of the half-unit capacitors from the DAC voltage. By doing this, the DAC gain is now reduced to $\times 0.5$. Note that the capacitor must be connected to the common mode, not disconnected; this way the stored sampling charge can be transferred to the integration capacitor. The capacitor units that hold no meaningful charge from the sampling stage can be disconnected so the amplifier load is not increased. Again, this operation is only required at the moment of Floating-Point gain transition, and subsequent cycles will keep *dacx0.5* disabled.

The same process could be described for $1 \rightarrow 2$ and $2 \rightarrow 1$ transitions, with the only difference being that more capacitors from the array will be unused, but hopefully the previous examples are sufficient to provide understanding of the $\Delta\Sigma$M input operation.

4.3.2 Memory Updater

Following the same philosophy as the feedback updater, the memory updater coefficients in Fig. 4.3 have a transient nature and its purpose is to update the integrator's state variables according to the Floating-Point control values. By doing this, the information inside the $\Delta\Sigma$M will remain coherent and the AGC distortion will be eliminated.

With this purpose, the circuit modification shown in Fig. 4.9 was implemented at each integrator stage. The modification consists on splitting the integration capacitor into two half-units and adding an auxiliary unit capacitor. The auxiliriary capacitor is necessary for the implementation of the coefficient $\times 2$. When this coefficient needs to be applied, a pre-amplification cycle is first required for the replication of the memory value into this auxiliary capacitor. The contents of this capacitor are added to the integration capacitor at the next integration stage.

Both examples of memory duplication and division are detailed in Fig. 4.9. The memory division simply consists on discharging one of the half-units capacitors by short-circuiting it to common-mode, using the signal *memx0.5* during the sampling stage previous to the integration (see Fig. 4.9a). Then, a regular integration stage follows and the charge is redistributed again, so the integrated voltage is then halved.

The memory amplification, as mentioned before, first requires a pre-amplification phase to replicate the value stored in the integration capacitor. To do this, the auxiliary capacitor is first connected to the OpAmp as a load in the integration stage previous to that when the value has to be updated (see Fig. 4.9b). After this process, both the auxiliary capacitor and the integration capacitor hold the same charge. The remaining step is to move the charge from the auxiliary capacitor to the integration capacitor, which can be done on the next integration stage by connecting the auxiliary capacitor in parallel to the sampling capacitor (see Fig. 4.9c).

The simulation in Fig. 4.11 illustrates the difference when the feedback and memory updaters are implemented or not. In this simulation, the Floating-point $\Delta\Sigma$M is fed with an amplitude modulated (AM) signal and the Floating-Point gain is controlled by an envelope detector. The PSD of the digitally re-scaled signal is measured, showing not only

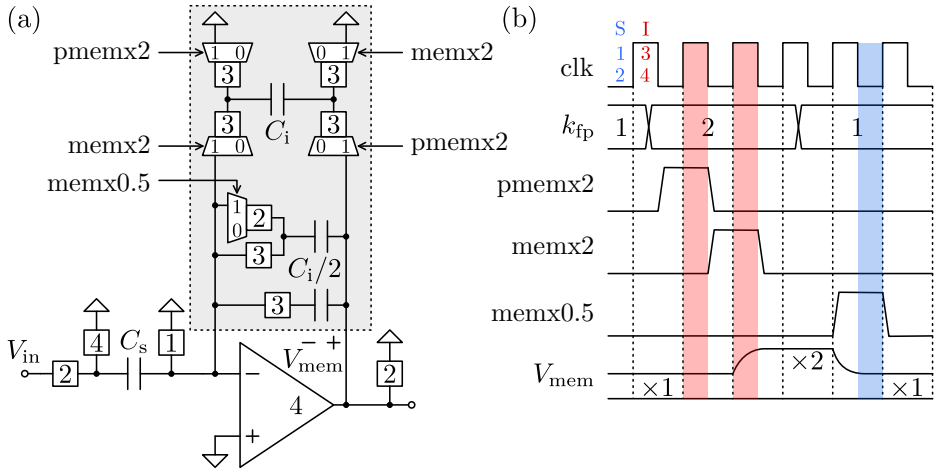

Figure 4.9 Single-ended circuit (a) and operation (b) of the Floating-Point ΔΣM memory updater. Blue and red shadowed regions show the instants of gain transition during sampling and integration stages, respectively.

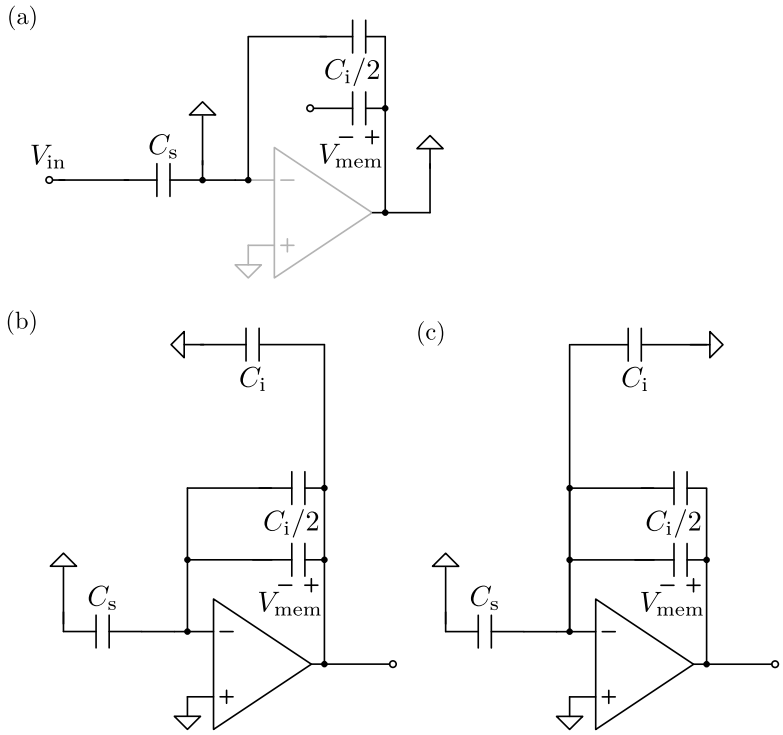

Figure 4.10 SC integrator state during a memory division (a), memory pre-amplification (b) and memory amplification (c).

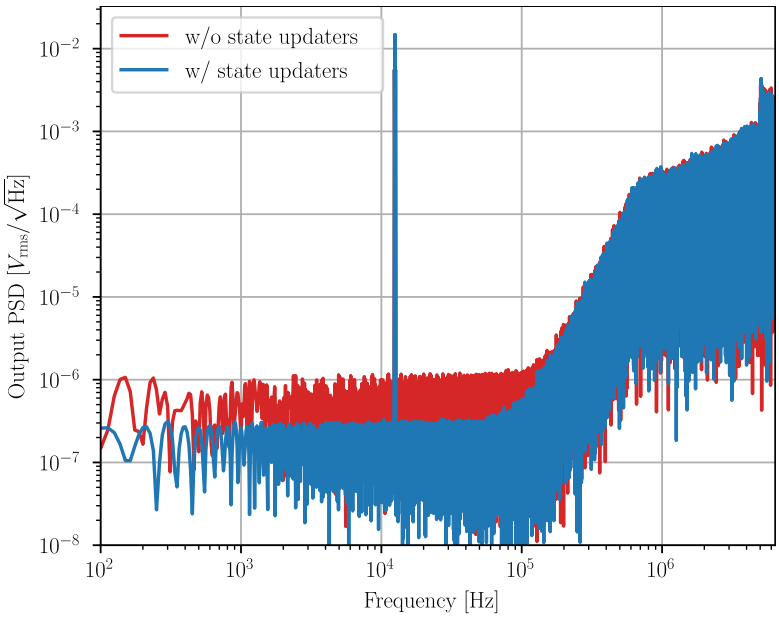

Figure 4.11 Simulated PSD showing the AGC transition noise of a re-scaled output signal, with and without the implementation of memory and feedback updater circuits.

the characteristic ADC noise but also the AGC transient noise. The simulation shows that AGC transient noise power is approximately increased by a factor of 20 when the updater coefficients are not implemented. Distortion does not increase drastically even when the coefficients are not implemented. The reason for this is that, due to the feedforward architecture, the content on the memories of $\Delta\Sigma$M is mainly quantization noise, especially for the input stage which is the most important. For this reason, the error in the state variables translates only to noise instead of distortion when the updater circuits are not implemented.

ΔΣM Realizations in CMOS Technology | 5

In this chapter, several multi-bit ΔΣM realizations from the design proposal of Chapter 3 are implemented in 180 nm, 65 nm, and 22 nm CMOS process nodes. This technology scalability allows to put into use the design methodology presented in Section 3.5 and check its validity and issues. The post-layout circuit performance of each realization is also evaluated, so a good study about the portability of the proposed design can be performed. Next, the process of converting the Multi-Bit ΔΣM core to fully functional IP is also explained, detailing the construction of the decimation filter and the communication bus used for the interconnectivity with a processing system. Finally, an implementation of the Floating-Point ΔΣM from Chapter 4 in 180 nm and its post-layout performance is presented.

5.1 Multi-bit ΔΣM CMOS Scalability in 180 nm, 65 nm, & 22 nm

As stated in Section 1.3, one of the objectives of this work was to demonstrate the potential of SC ΔΣMs. For this purpose, the proposed Multi-bit ΔΣM design has been mapped into several CMOS technology nodes in order to study the effects of technology downscaling and check the validity of the design methodology proposed in Section 3.5.

In this section, three different implementations of the Multi-bit ΔΣM of Fig. 3.8 are presented. The chosen technology nodes are:

- 1.8-V 180-nm 6-metal MiM CMOS process from X-FAB
- 1.2-V 65-nm 9-metal MiM CMOS process from TSMC
- 0.8-V 22-nm 11-metal MoM CMOS process from Global Foundries

Technology Node	**180 nm**	**65 nm**	**22 nm**†	Units
Core Supply Voltage	1.8	1.2	0.8	V
Differential Full-Scale	2	1.2	1	V_{pp}
Sampling Capacitor Size	8	20	20	pF
Bandwidth	50			kHz
OSR	128			-
f_{samp}	12.8			MS/s
Area	0.202	0.186	0.043	mm^2
P_d	741	632	197	µW
$SNDR_{max}$	97.9	99.8	95.6	dB
FoM_S	176.0	178.8	179.6	dB

Table 5.1 Summary table of the main post-layout simulation results of the Multi-bit ΔΣM implementation in different technology nodes. †Note: Resolution specifications were different for this design.

All the target specifications are the same for all designs, i.e. 16-bit ENOB and 50 kHz bandwidth, with the exception of the resolution for the 22 nm node. In this technology, it was decided to lower the resolution specification, since the available experimental results from other chips at that point proved it was quite difficult to measure such a high resolution without high-end lab equipment. As the supply voltage is scaled down this is increasingly difficult, because lower an even noise level from the equipment is required. In exchange for the resolution, a lower power consumption has been achieved in this CMOS implementation.

A summary of the main design parameters and specifications for each target technology can be found in Table 5.1. Some PSD simulations for the resolution calculations are also shown in Fig. 5.1, as well. As explained before, the resolution requirements of the 22 nm design were intentionally chosen to be lower, therefore the sampling capacitors were not upscaled from 65 nm to 22 nm. From these results, it seems apparent that the design does not greatly benefit from the technology downscaling in terms FoM. This is because keeping the same level of resolution while considering the supply voltage downscaling by a factor α requires the increase of the capacitors in the design by $1/\alpha^2$, due to the kTC constraint (2.45). Therefore, the current consumption of the integrator amplifiers will need to be increased by a similar amount, countering some of the reduction in the power consumption due to the supply downscaling. Furthermore, by comparing the two designs exhibiting similar resolution (i.e. 180 nm and 65 nm), the same conclusion can be drawn for the area. Most of the design area is taken by the capacitors, so the supply downscaling will require larger capacitors which means larger area if the technologies have capacitors with similar capacitance per unit area, C_{ua}.

The post-layout maximum resolution corners are summarized in Table 5.2. The slow corners show some resolution loss, especially in lower nodes. The reason for this behaviour is the increase of noise due to temperature and specially the degradation of the OpAmps performance. Fast corners may also present some resolution loss, this time due to the

	ss125	**tt27**	**ff-55**	
180 nm	96.9	97.9	95.8	dB
65 nm	93.2	99.8	97.9	dB
22 nm	91.3	95.6	94.2	dB

Table 5.2 Post-layout SNDR simulation results of the Multi-bit ΔΣM implementation for different technology nodes versus process and temperature corners.

undesired increase of the GBW of the OpAmps, degrading the OpAmp stability. Both effects can be compensated by trimming the bias current of the OpAmps accordingly. In any case, from these results we can support the initial hypothesis stating that SC ΔΣM are quite robust against PVT corners.

Finally, the layout designs for each technology node are depicted in Fig. 5.2, Fig. 5.3, and Fig. 5.4, for the 180 nm, 65 nm, and 22 nm realizations, respectively. The overall size of each layout and the different parts of the design are annotated in the same figures. The 180 nm layout is built with the strategy of reducing routing length as much as possible in order to minimize parasitic capacitance, sacrificing some matching and differential symmetry. The 65 nm and 22 nm designs, instead, are built in a fully-differential fashion, maintaining circuit symmetry as much as possible in exchange for a larger routing. In all the physical designs, digital and analog domains have been isolated as much as possible to avoid cross-domain capacitive and supply couplings.

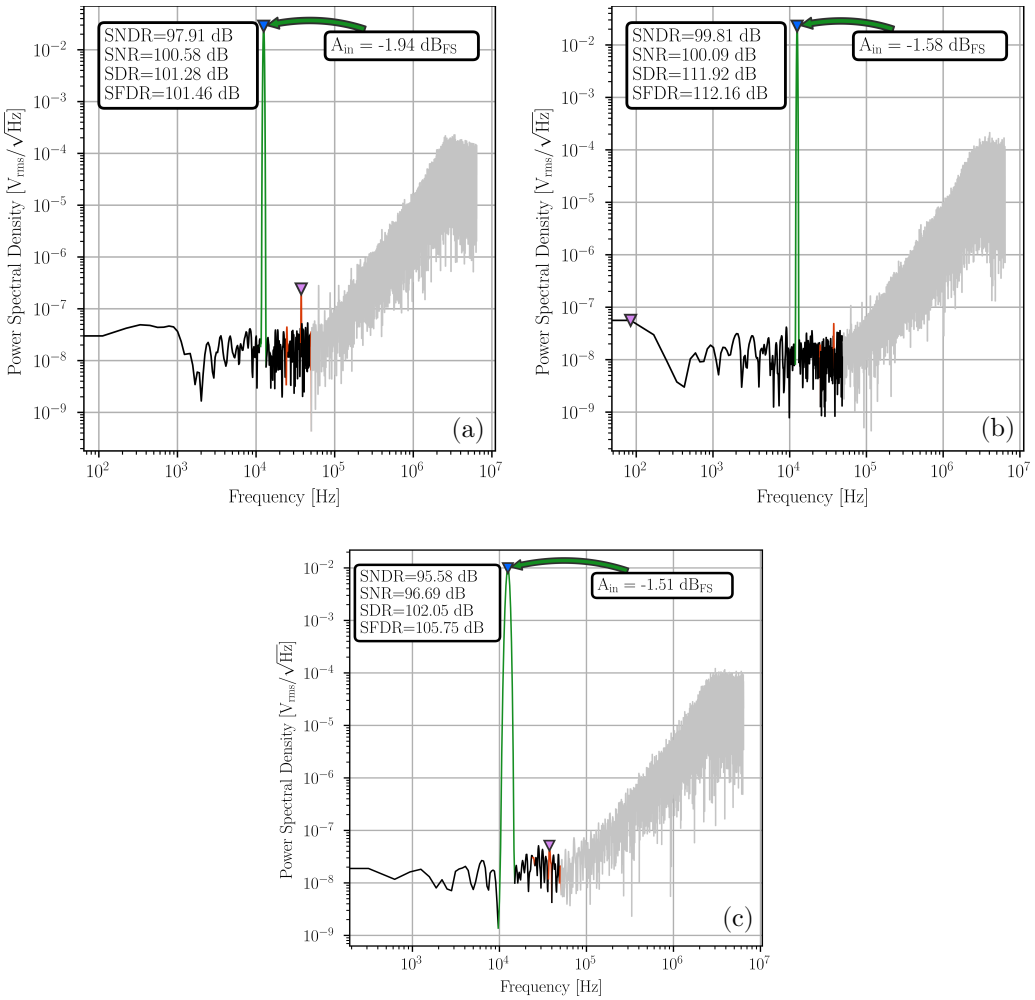

Figure 5.1 Post-layout PSD simulations from the Multi-bit ΔΣM implementation in Fig. 3.8 for 180 nm (a), 65 nm (b), and 22 nm (c) technological nodes, at an input of 12.5 kHz and optimal amplitude for each of the implementations.

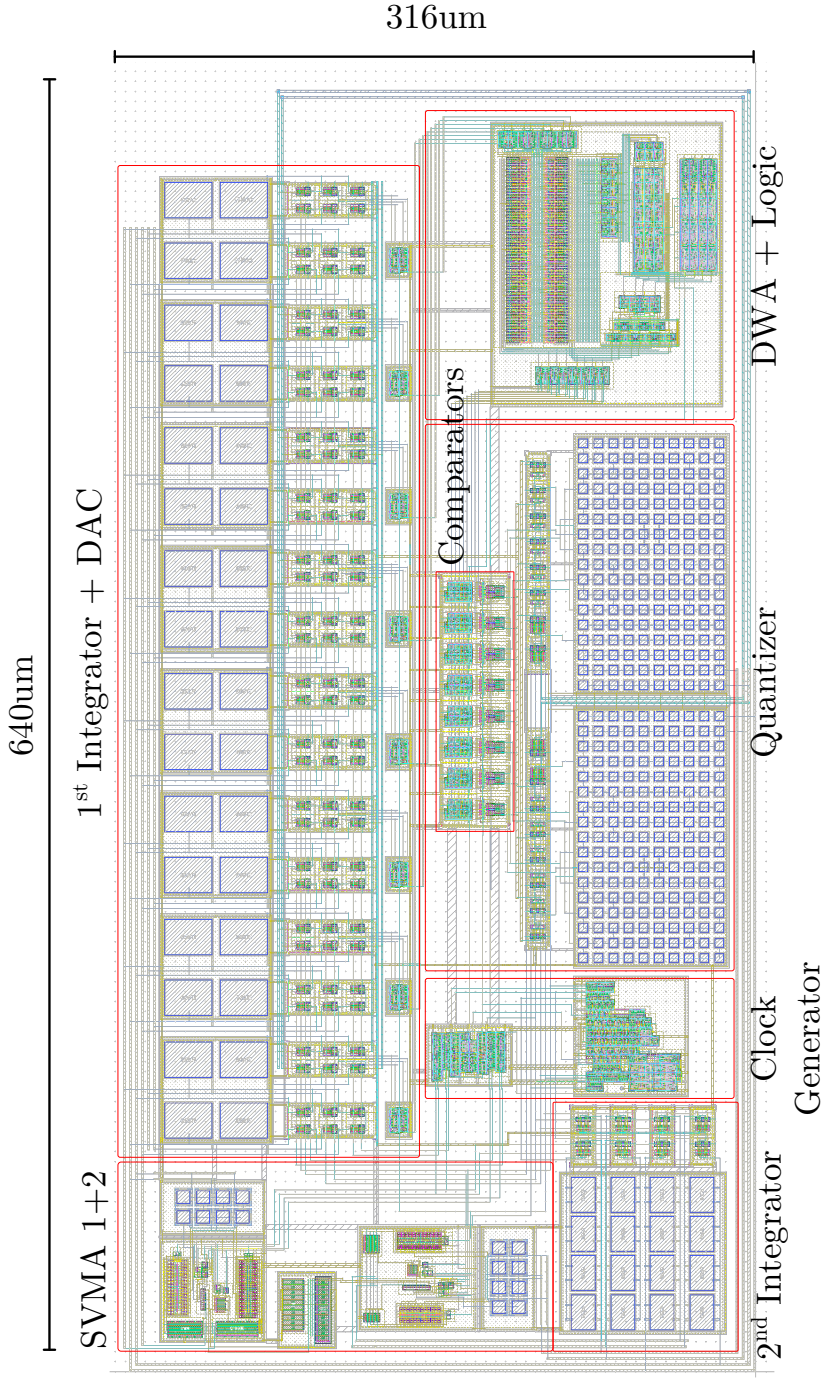

Figure 5.2 | Layout design of the Multi-bit ΔΣM in 180 nm CMOS technology. Total design area is 0.202 mm^2

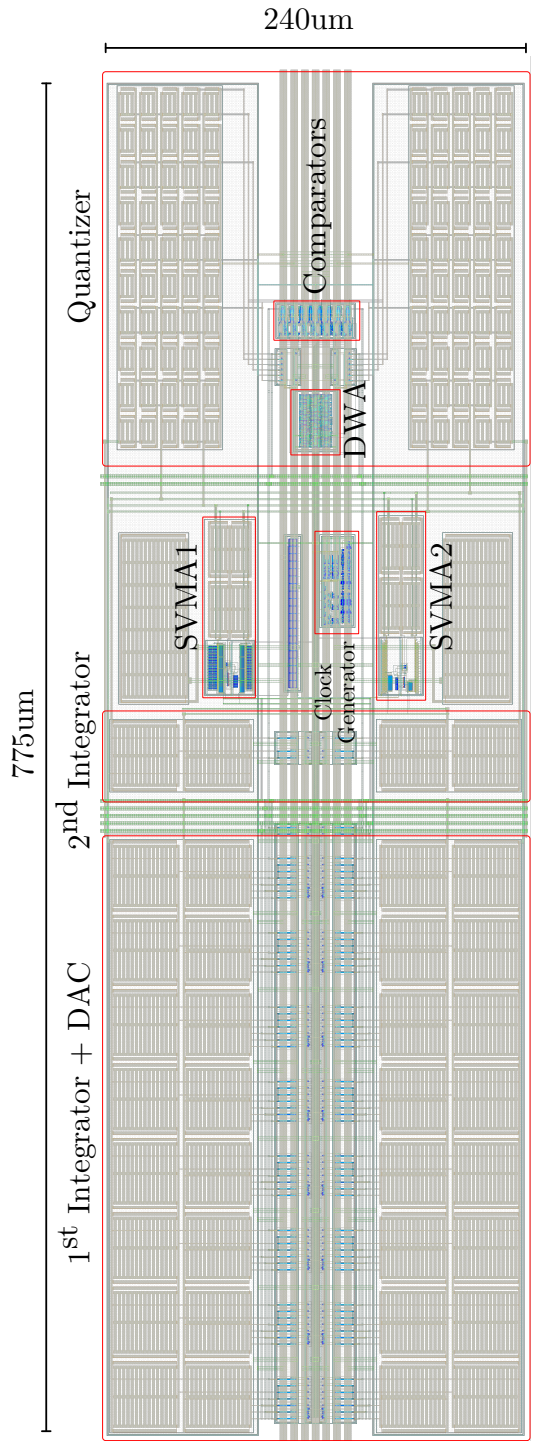

Figure 5.3 | Layout design of the Multi-bit ΔΣM in 65 nm CMOS technology. Total design area is 0.186 mm^2

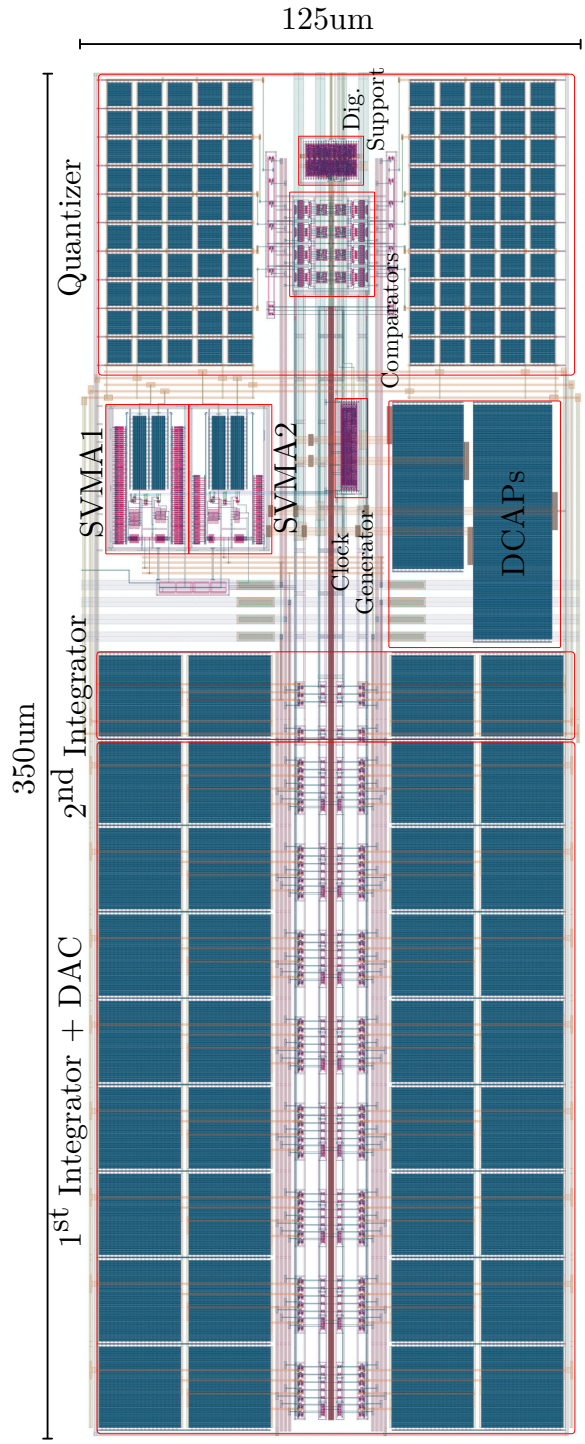

Figure 5.4 | Layout design of the Multi-bit ΔΣM in 22 nm CMOS technology. Total design area is 0.043 mm^2

5.2 IP Focused Design

Chapters 3 and 4 have described the working principle and design process of two different ΔΣMs proposals, suited for different applications. Nonetheless, these designs, while operational, are not ready to be incorporated into a system-on-chip (SoC) comprised of a digital core and they would require several support ICs in order to build a fully functional printed circuit board (PCB).

In this section, two important digital support blocks, such as the output decimation filter and a bus peripheral backend, are developed to provide a standard connectivity to the ADC frontend so that it can be used as an IP block for its incorporation to a larger ASIC based on a microprocessor core.

5.2.1 Decimation Filter

As explained previously, ΔΣMs rely on oversampling in order to reduce the in-band ADC noise, which is typically located at the low-frequency range. All the resolution calculations made until now only take into account in-band noise, but that does not mean the out-of-band noise can be completely ignored. In fact, it has to be removed first in order to obtain a meaningful data sequence in the time domain, and a suitable block to do that is the decimation filter. The purpose of the decimation filter is two-fold: its first objective is to filter the out-of-band noise as best as possible, and the second one is to remove redundant samples from the oversampling process that are no longer needed, with the corresponding of reduction of the data rate.

With this objective in mind, a cascaded integrator-comb (CIC) finite impulse response (FIR) filter [128] has been chosen to be implemented as the digital filter of the Multi-bit ΔΣM design in the 65 nm CMOS realization. This specific topology does not require the use of multipliers or dividers, so it can be built at a very low transistor cost. In contrast, they have the disadvantage of not providing a sharp transition between the pass-band and stop-band. Conventional filters offer better filtering characteristics, but they are more expensive to build and some are limited to a decimation factor of two [129], so many have to be cascaded in order to reduce the data rate to the Nyquist rate. For this reason, a good strategy is to use a CIC filter to go from high to low OSR values and then use a conventional filter to provide a sharp transition between pass-band and stop-band, but now this expensive filter works at a low sampling rate [130].

Nonetheless, only the CIC filter has been implemented in this work. The remaining filtering can be handled by the digital core in charge of the data acquisition, since the sampling rate will be low enough to be manageable by most processors. In this way, the final bandwidth can even be software defined.

The structure of the CIC filter is shown in Fig. 5.5. It consists on a cascade of integrators followed by a cascade of comb stages, which incorporate a subtraction of delayed samples. The comb stages already operate at the downsampled frequency rate, thus applying the decimation. Note that this implementation only requires adders, inverters for the two's complement used in the subtraction, and registers, so the resulting circuit is very

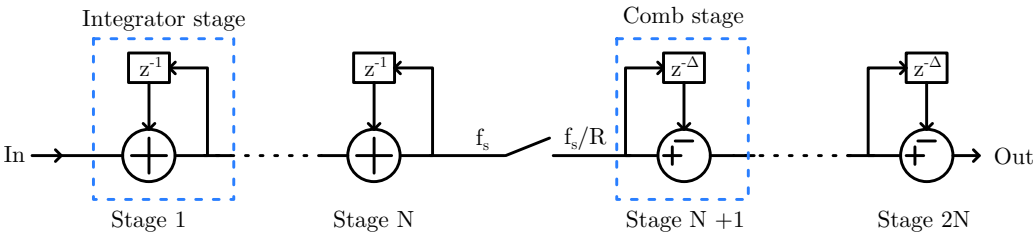

Figure 5.5 | General structure of the CIC decimation FIR filter.

minimalist.

The transfer function of this filter is:

$$H(z) = \left(\frac{1 - z^{-R\Delta}}{1 - z^{-1}}\right), \tag{5.1}$$

and its magnitude:

$$|H(z)| = \left(\frac{\sin(\pi R \Delta f_{\mathrm{i}})}{\sin(\pi \Delta f_{\mathrm{i}})}\right)^{N}, \tag{5.2}$$

where N is the filter order, R is the rate of reduction and Δ is the differential delay (usually set to 1 or 2). From (5.2) it is apparent that the pass-band transition is smooth instead than sharp. However, the filter offers a good selectivity with an attenuation of $N \cdot 20$ dB/dec at the stop-band. The order of the filter needs to be high enough to compensate the rising slope of the $\Delta\Sigma$M quantization noise shaping, and then to give the desired attenuation in the stop-band. The necessary filter specifications and chosen design parameters are summarized in Table 5.3.

Parameter	**Value**
$\mathrm{OSR_{in}}$	128
$\mathrm{OSR_{out}}$	4
L_{stop}	40 dB
N	4
R	32
Δ	1

Table 5.3 | CIC decimator specifications and design parameters.

The final step is to calculate the length of the registers and build the structure using integrator and comb stages. By using some design equations [128], the maximum register growth and the available truncation that can be applied to each stage can be calculated in order to reduce the number of components to a minimum. An output width of 18 was chosen to not introduce additional truncation noise. The register widths obtained for this filter design are summarized in Table 5.4.

The performance of this filter is evaluated together with the 65 nm $\Delta\Sigma$M and the output data PSD can be shown in Fig. 5.6. These simulation results show an acceptable

	I	1	2	3	4	5	6	7	8	O
High-bit	3	24	24	24	24	24	24	24	24	24
Low-bit	0	0	0	0	0	2	3	4	5	7

Table 5.4 | Bit width of the registers used in the integration and comb stages of the decimator.

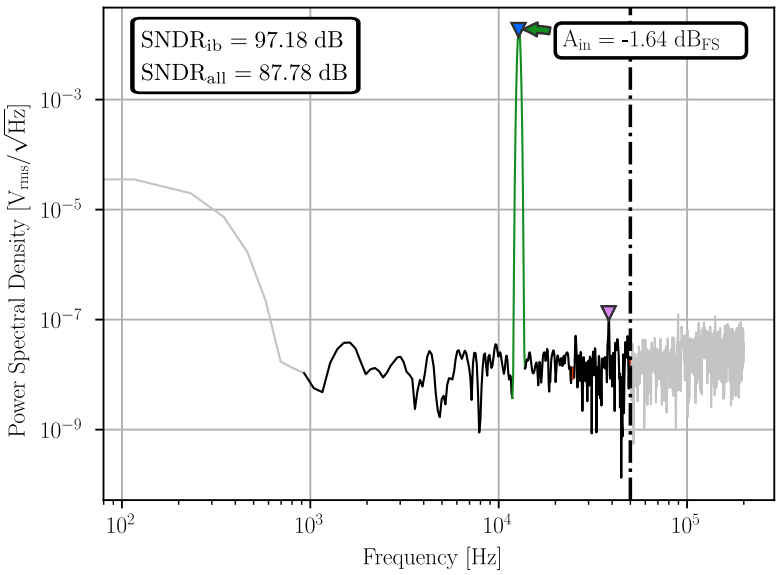

Figure 5.6 | Electrical simulation showing the resolution of the 65 nm ΔΣM design along with the CIC decimator. Low-frequency windowing effects are not taken into account in the calculations.

degradation in the pass-band due by the decimation, staying over the desired 16-bit ENOB. When taking into account the unfiltered out-of-band noise too, it shows a resolution of 87.78 dB. The remaining filtering can be carried out via digital regular post-processing.

5.2.2 AXI-4 Lite Interface

In order to communicate with a processor, some kind of peripheral bus interface is required for the completion of the ΔΣM IP. For this purpose, a standard Advanced eXtensible Interface (AXI) bus protocol has been chosen [131]. Specifically, the bus interface implemented in this work was the AXI-4 Lite interface. Without entering in detail, the protocol comprises of five different communication channels: read address channel, read data channel, write address channel, write data channel and write response channel. Each channel is used for a different purpose and allows for high-speed data transfers and flexible operations. The AXI-4 Lite implementation goes without some features available in the full AXI implementation in order to reduce the complexity of the design, since many of these features are not needed for the IP at hand.

The design consists on the register transfer language (RTL) description of the AXI slave peripheral according to the Advanced Microcontroller Bus Architecture (AMBA) specification [132]. The slave interface is then memory mapped to the processor via the AXI bus, so the registers can be read or written. This implementation needs just two registers: one for the writing of the ADC control configuration and another to read the ADC data and status flags. In order to interface the different clock domains from the ADC and the AXI bus, a first-in, first-out (FIFO) memory is placed in between the ADC output and the peripheral slave interface. The control flags are generated from the FIFO states, allowing to recognize whether the read data is valid or not and whether there has been data-loss due to the overflow of the FIFO caused by an insufficient reading speed by the processor.

The top schematic of the IP, including the peripheral interface, is shown in Fig. 5.7a. The raw data signals coming out of the ΔΣM have also been interfaced to the outside for testing purposes. The meaning of the data in the slave registers is shown in Fig. 5.7b. Some of the configuration bits are connected to the outside of the IP, but most are connected back to the ADC control signals from the outside.

The full layout of the IP design is shown in Fig. 5.8, where the IP has been integrated as a part of a larger system consisting on a RISC-V processor.

5.3 Floating-Point ΔΣM with Distortion-Less AGC in 180 nm

The third-order, single-bit Floating-Point SC ΔΣM with distortion-less AGC from Fig. 4.5 has been implemented in a 180 nm CMOS technology. The maximum gain of the Floating-Point ΔΣM has been chosen to be 4, therefore needing 3 gain levels (i.e. 1, 2, and 4). This is enough to prove the proper operation of the architecture without increasing the complexity of the design in excess. The same design methodology from Section 3.5 is applied to the topology in Fig. 4.5. The flicker-noise cancellation circuit from Section 3.3 is also implemented, since this design presented the same flicker noise problems as the Multi-bit ΔΣM implementation in the same technology.

The summary of the post-layout simulations can be found in Table 5.5. The maximum achievable SNDR when the input is close to the full-scale is 93.2 dB. The Floating-Point gain allows to mitigate the resolution loss in lower amplitude values. For instance, at -17 dBFS the expected SNDR would be ≈ 80 dB due to the reduction in signal power. By using $k_{\mathrm{AGC}} = 4$, an extra resolution of 6 dB is gained, resulting in SNDR = 86.8 dB at that input amplitude level. This fact allows to extend the DR of the ADC up to 103.1 dB. The PSD simulations at different input amplitude values are shown in Fig. 5.9.

The layout of this design is shown in Fig. 5.10, comprising an overall silicon area of $0.238\mathrm{mm}^2$.

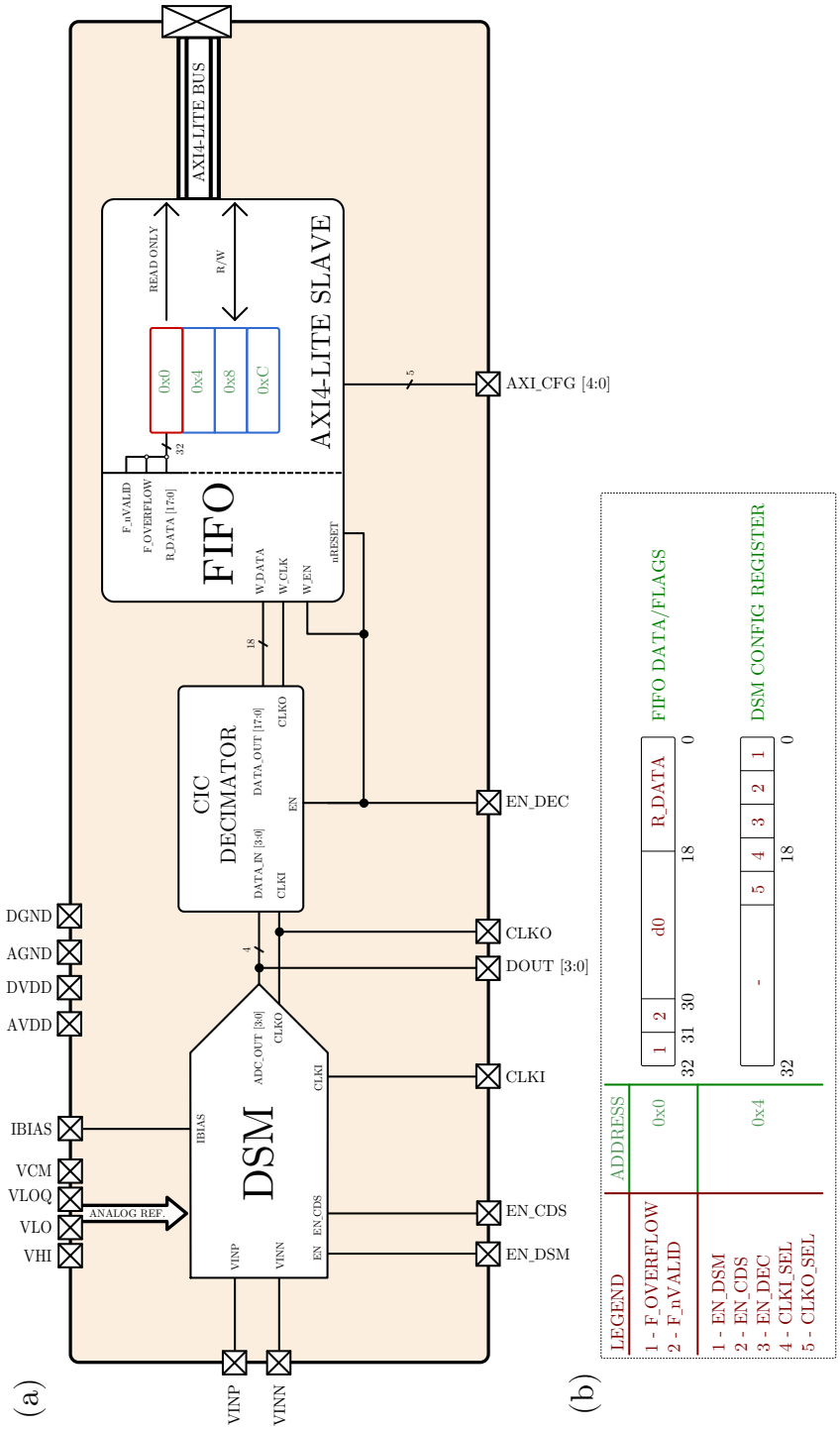

Figure 5.7 | Top schematic of the ΔΣM IP design (a) and meaning of the slave register data (b).

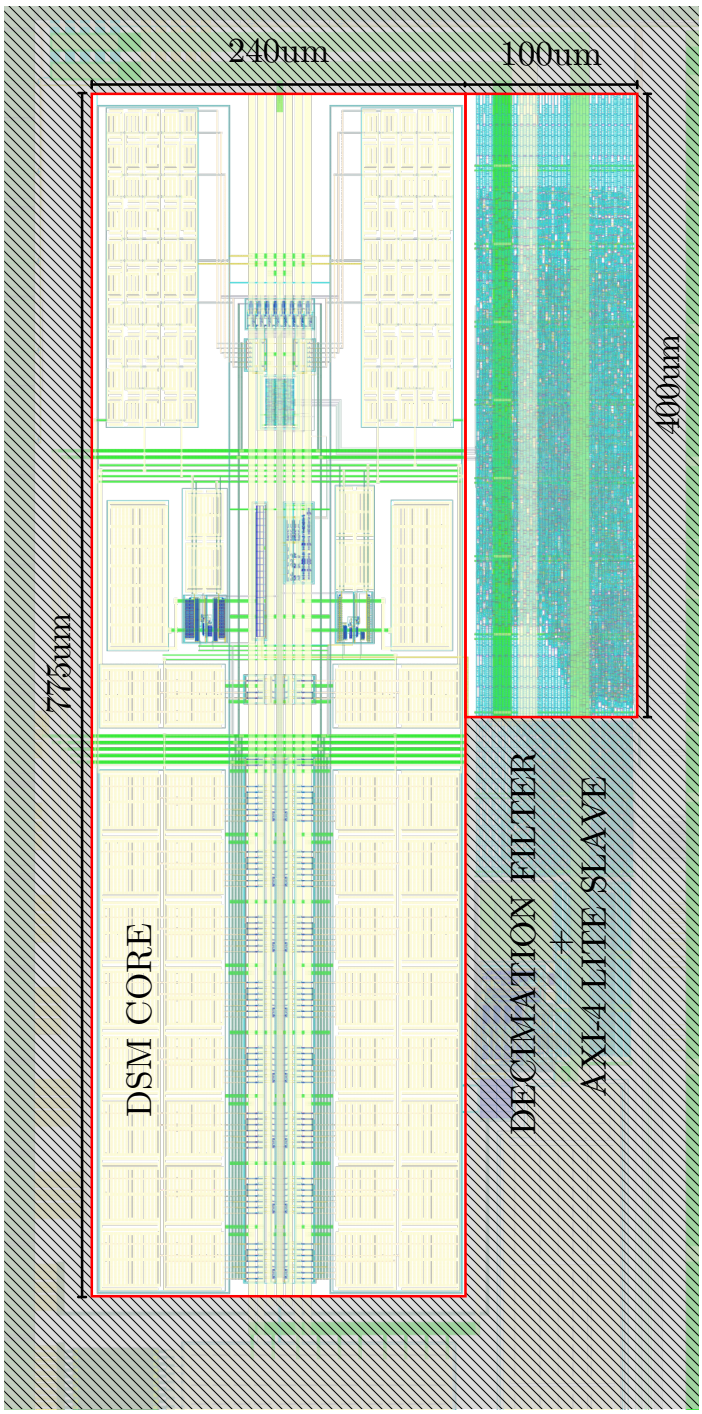

Figure 5.8 Layout design of the Multi-bit ΔΣM IP, including the decimation filter and the AXI-4 Lite slave peripheral, in 65 nm CMOS technology. Overall IP area is 0.226 mm^2.

Parameter	**Value**	**Units**
Technology Node	180	nm
Core Supply Voltage	1.8	V
Differential Full-Scale	2	V_{pp}
Bandwidth	50	kHz
OSR	128	-
f_{samp}	12.8	MS/s
k_{fpmax}	4	-
Area	0.238	mm^2
P_d	825	µW
A_{inopt}	-4	dBFS
$SNDR_{\sim -17\ dBFS}$	86.8	dB
$SNDR_{\sim -4\ dBFS}$	93.2	dB
DR	103.1	dB
FoM_S †	180.9	dB

Table 5.5 Summary of the main post-layout specifications for the Floating-Point ΔΣM implementation from Fig. 4.5 in 180 nm CMOS technology. †Note: This calculation uses DR instead of SNDR.

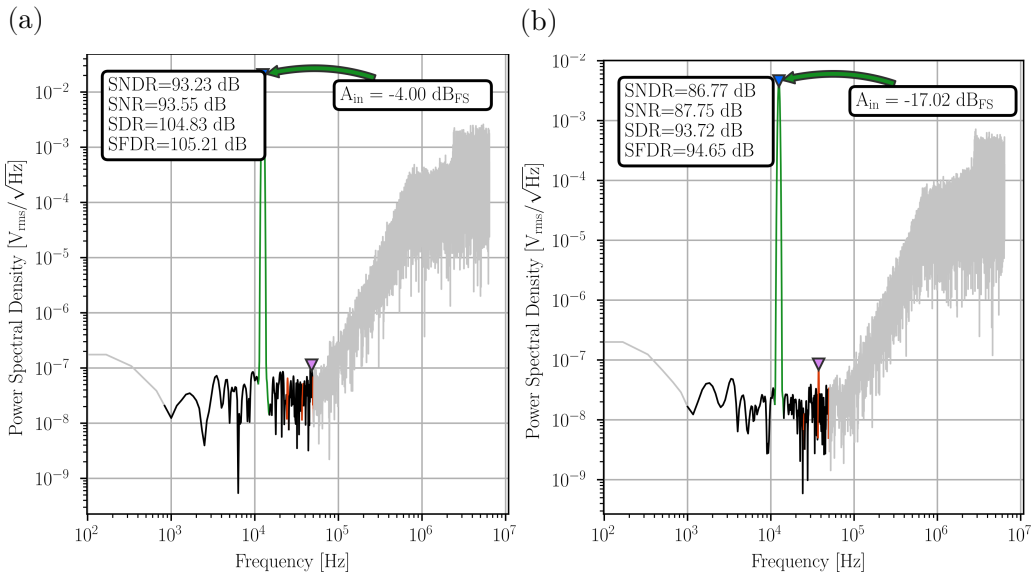

Figure 5.9 Post-layout simulation results of the Floating-Point ΔΣM implementation from Fig. 4.5 in 180 nm CMOS technology, showing the PSD and the maximum achievable resolution at $A_{in} = -4$ dBFS with $k_{AGC} = 1$ (a) and $A_{in} = -17$ dBFS with $k_{AGC} = 4$ (b).

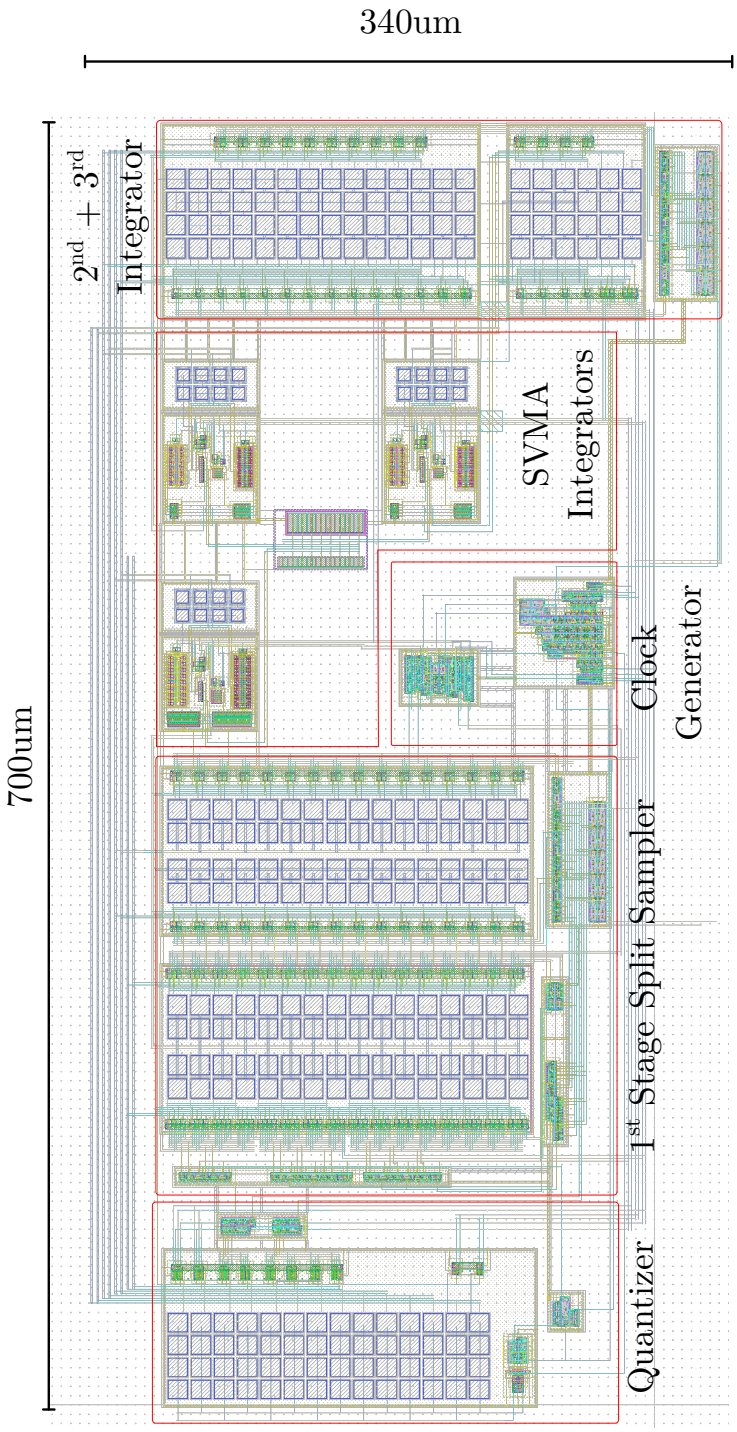

Figure 5.10 | Layout design of the Floating-Point ΔΣM in 180 nm CMOS technology. Overall area is 0.238 mm^2.

Experimental Results | 6

This chapter gives an in-depth description of the experimental test setup, valid for the different ΔΣM designs presented in Chapter 5. The required design tasks required are explained, giving a detailed description of the PCB and FPGA designs. Next, the experimental measurements from a Multi-bit ΔΣM fabricated in 180 nm CMOS technology are presented and the ADC is compared to other state-of-art works using the FoM from (1.15). The same applies for the Floating-Point ΔΣM fabricated in the same 180 nm node, which is likewise measured using a similar test vehicle and then compared to other ADC works.

In addition, the results from a radiation-hardness test for the 180 nm Multi-bit ΔΣM implementation are presented, arriving to the conclusion that the chip can withstand TID levels rated for most space missions.

From these tests, it is demonstrated that robust high-performance ADC IPs can be obtained using the SC ΔΣM architecture and that it is possible to incorporate a distortion-less AGC inside the classic ΔΣM architecture.

6.1 Measurement Setup

The measurement of high-resolution ADCs requires a carefully planned test-setup design. It must take care of the necessary analog conditioning for the correct operation of the ADC and the digital post-processing, storage, control, and communications with a personal computer (PC) so that the user can easily make automated measurements.

A general scheme is illustrated in Fig. 6.1. The main device of the test-vehicle is a custom PCB where the device under test (DUT) and all the analog and digital support components are placed. The ADC stimulus is generated via an external signal generator connected to the PCB, which can be controlled by a PC for the automatization of the tests. A FPGA takes care of the data storage and the transfer to the PC, all controlled by high-level software at the PC side. Finally, the data post-processing is carried out by the PC using several dedicated libraries in order to obtain meaningful measurements.

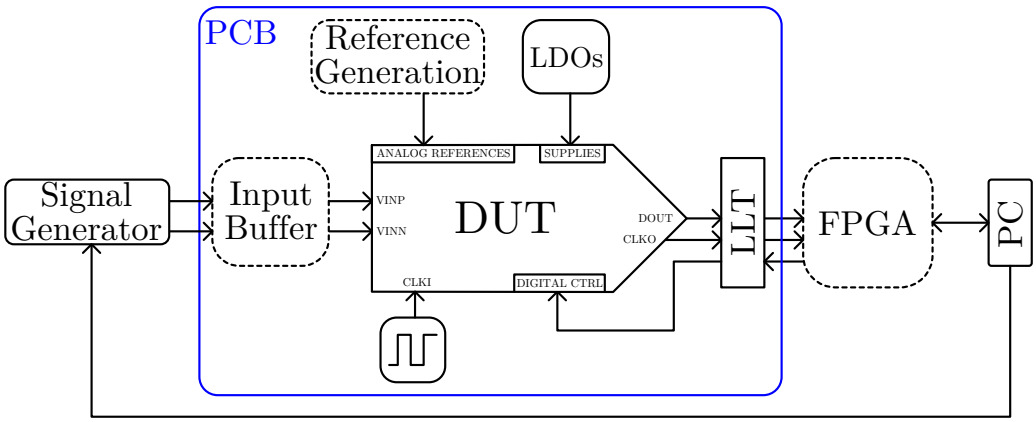

Figure 6.1 | General scheme of the test setup for the ΔΣM ADC designs proposed in this PhD thesis.

The PCB design is the most critical part of the test setup. Special care has to be taken identifying and isolating the analog and digital domains. The general PCB schematic design is illustrated in Fig. 6.1. The analog domain includes an input buffer, used to drive the DUT inputs, a reference generation block, in charge of generating low-noise voltage and current references needed by the DUT, and a set of low-dropout regulators (LDOs), providing power to the core and pad ring of the DUT. The digital domain consists on a crystal oscillator, which provides a low jitter input clock to the DUT, and a set of logic level translators (LLTs) used to interface digital domains with different voltage supply levels, such as the ADC and the FPGA. The rest of digital circuitry is implemented by the FPGA, simplifying thus the PCB design and improving the isolation from digital noise. No depicted in the schematic, there exist additional LDOs used to power-up only the IC components, to further isolate the DUT from any interference due to supply coupling.

An in-depth look at the input buffer is shown in Fig. 6.2. The design uses a low-noise low-distortion fully-differential OpAmp with a gain of $\times 0.1$ set by the feedback resistors. The purpose of the buffer is to provide a high input impedance to the signal generator while providing distortion-less low-impedance driving capabilities to the DUT. The OpAmp also sets the output common mode value to that required by the ADC. Feedback capacitors are also added to provide anti-aliasing filtering. The output consists on a decoupling RC network that ensures stability to the OpAmps and decouples the input sampler of the ADC from switching noise.

The reference generation block is illustrated in Fig. 6.3. Fig. 6.3a shows the voltage reference generation consisting on a LDO together with a resistive ladder. The required taps from the ladder are connected to a low-pass filter in turn connected to a driver stage with a decoupling network at its output. The bias current is created using the structure in Fig. 6.3b, which consists on a buffer and a LDO connected in series with the buffer and a resistor, in order to create a floating voltage supply. The ratio between the LDO voltage and the resistor will set a precision current to be fed to the ADC.

The PCB layout design is especially critical, since we are dealing with a high-resolution

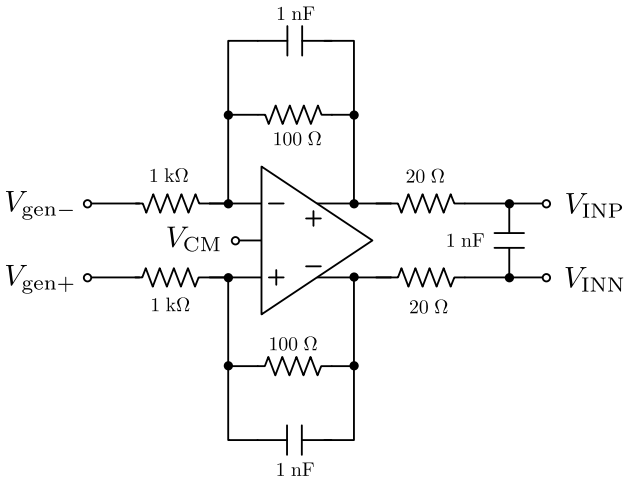

Figure 6.2 | Fully-differential input buffer schematic from the PCB test setup.

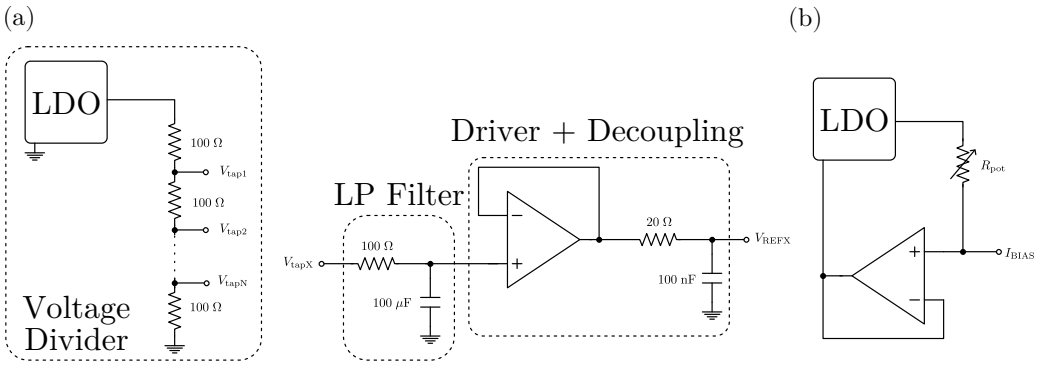

Figure 6.3 | Voltage reference generator (a) and bias current generator (b) circuits from the PCB test setup.

converter working at high-speed, several electromagnetic interference (EMI) effects make an appearance and start taking a toll in the resolution of the ADC. An incorrectly designed PCB can destroy the performance of the ICs and invalidate any measurements taken. The use of ultra-low noise components is essential for the proper characterization of the ADC. Also, special care has to be taken isolating the analog and digital domains and avoiding signal ground-loops, which can result in harmful interference [133], [134].

The test PCB in Fig. 6.4a is the product of all these considerations, made to measure the different $\Delta\Sigma$M IC samples. A 4-layer technology is selected to help with the routing of the signals. Two of the layers are dedicated to ground planes in its entirety so that the continuity of the return currents is ensured, contributing this to the mitigation of EMI by preventing ground-loops. The ICs themselves were soldered onto separate modules containing only decoupling components for easy replacement during the tests, as shown in Fig. 6.4b. These modules are also provided of jumpers to connect external references, if necessary, and measure the IC power consumption.

The FPGA design takes care of the digital back-end implementation and the low-level software necessary to control the ADC and complete data acquisition requests. Two different domains can be distinguished: the programmable logic (PL), which is the actual FPGA core where logic structures can be built, and the processing system (PS), which contains the hard-IP blocks such as the central processing unit (CPU). The two domains are interfaced via an AXI bus.

In Fig. 6.5a, the FPGA design for the Multi-bit $\Delta\Sigma$M is depicted. The PL input is a data packager whose function is to pack several data samples into one memory word to be more manageable by the processor. Then, the same AXI-4 lite slave peripheral implemented in Section 5.2.2 is re-used to build the communications between the PL and the PS. Finally, a custom firmware is programmed into the CPU to handle the data acquisition, the control of the ADC and the communications with the PC.

The FPGA design for the Floating-Point $\Delta\Sigma$M is very similar, but in this case it is also included the AGC necessary logic to close the ADC loop and automatically change the Floating-Point gain depending on the input signal level, as depicted in Fig. 6.5b. To build this AGC, the raw data is first filtered by the CIC decimator presented in Section 5.2.1, which is re-used for this test, so that the out-of-band noise is filtered and the data rate is lowered. This produces a meaningful waveform that can be filtered by a digital envelope detector. From the envelope, the maximum amplitude during a certain interval of time can be detected and suitable Floating-Point gain values can then be established by comparing with the thresholds from a detector.

(a)

(b)

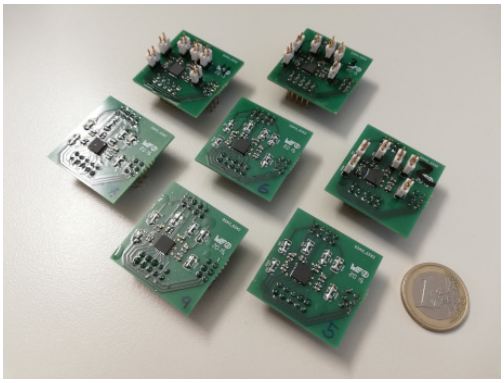

Figure 6.4 | Main test PCB (a) and individual modules with soldered DUT samples on top (b).

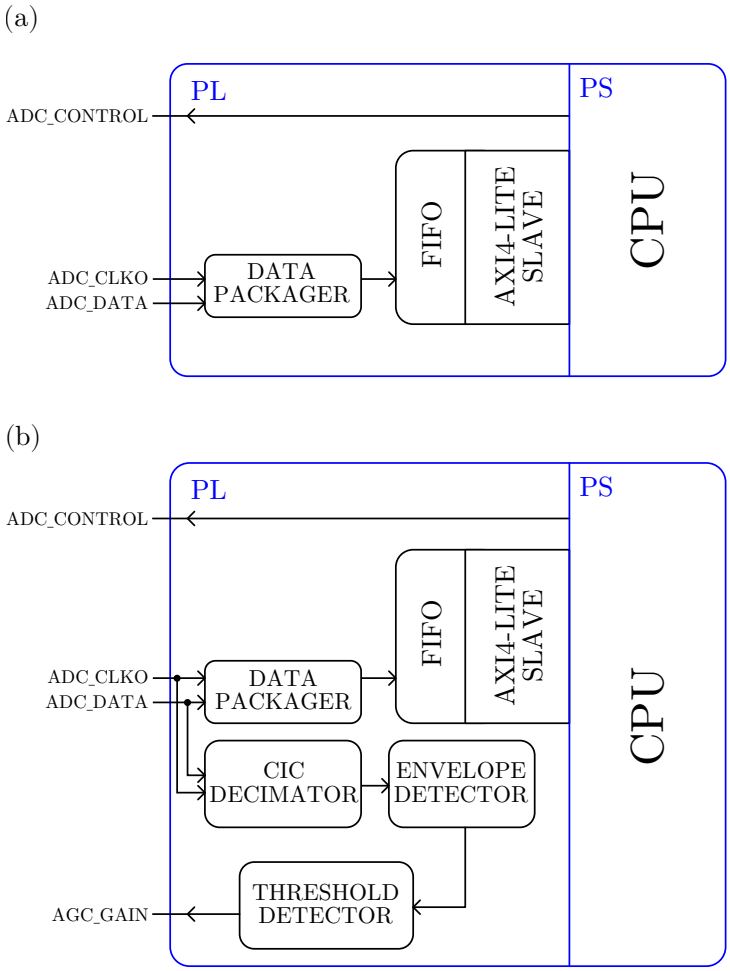

Figure 6.5 FPGA design for the Multi-bit $\Delta\Sigma$M (a) and for the Floating-Point $\Delta\Sigma$M with distortion-less AGC (b).

6.2 Multi-bit ΔΣM Measurement Results

The low-power high-resolution Multi-bit SC ΔΣM circuit has been fabricated in a 1.8-V 0.18-µm 6-metal CMOS technology, occupying 0.2 mm^2 and consuming 445 μA from the combined 1.8-V analog and digital power supplies. A photo of the physical die is shown in Fig. 6.6. As depicted, about half of the circuit area is devoted to the first integrator and the feedback DAC, while the other half is equally distributed between the second integrator, the multi-bit flash quantizer and the digital circuitry.

The test was carried out as depicted by Fig. 6.1. Several experimental measurement attempts with different instrumentation were made. The local measurements at our lab were made using the DS360 ultralow-distortion from Stanford Research Systems Ltd., USA. The best results, however, were measured with the APx555 audio analyzer from Audio Precision Inc., USA, since this instrument provides a noise level low enough to measure the full resolution of the ADC.

Fig. 6.7 shows the experimental PSD of the output for 1-kHz input frequency at -1 dBFS respect to the 2-V_{pp} differential full-scale. This measured PSD profile returns 94.6 dB SNDR in 50-kHz bandwidth and 103.5 dB SFDR. As it can be noticed, no residual flicker-noise is observed at the low-frequency range, and no out-of-band harmonics are present. Fig. 6.8 shows the measured 96 dB peak SNR and 94.6 dB peak SNDR at -1 dBFS , which emphasizes the high linearity of this SC ΔΣM circuit. Regarding power consumption, 45% of supply current is invested in the first integrator, and some optimization margin should be explored to reduce the 33% power budget of the 4-phase clock generator.

The measurements were done for several available samples. As shown by Fig. 6.9, the dispersion in the measured maximum SNDR is small, proving the high-robustness of the design against PVT corners and matching issues.

Finally, this design has been compared to other state-of-art high-resolution ($SNDR_{max} \geq$ 90 dB) general-purpose (BW $\geq$ 20 kHz) ΔΣM ADCs in Table 6.1. The FoM from this table have also been mapped in the state-of-art chart in Fig. 6.10. This ADC has a 172.6 dB FoM, better than the other regular SC ΔΣM and a competitive value respect to the state-of-the-art, demonstrating that high-resolution ADCs can be built through the use of multi-bit low-order single-loop SC ΔΣM architectures without the use of calibration, switch bootstrapping nor resistors.

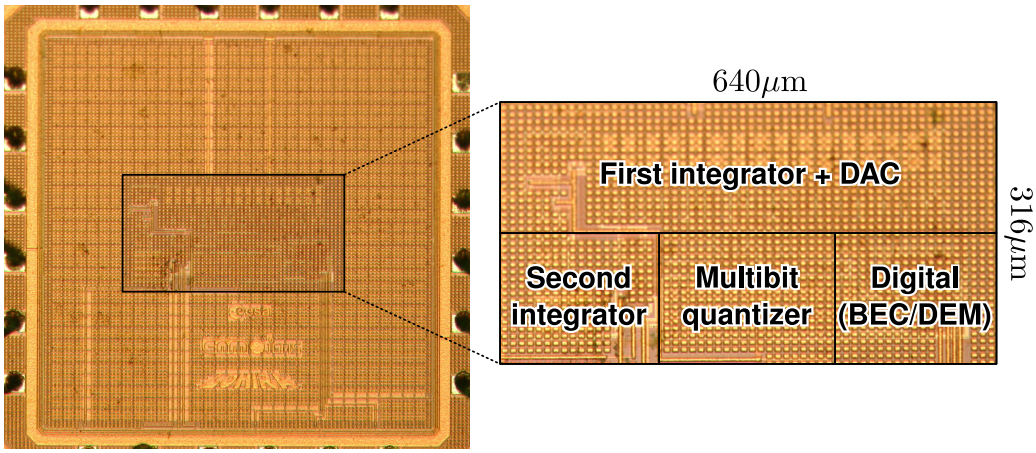

Figure 6.6 | Multi-bit ΔΣM IC fabricated in 180 nm CMOS technology.

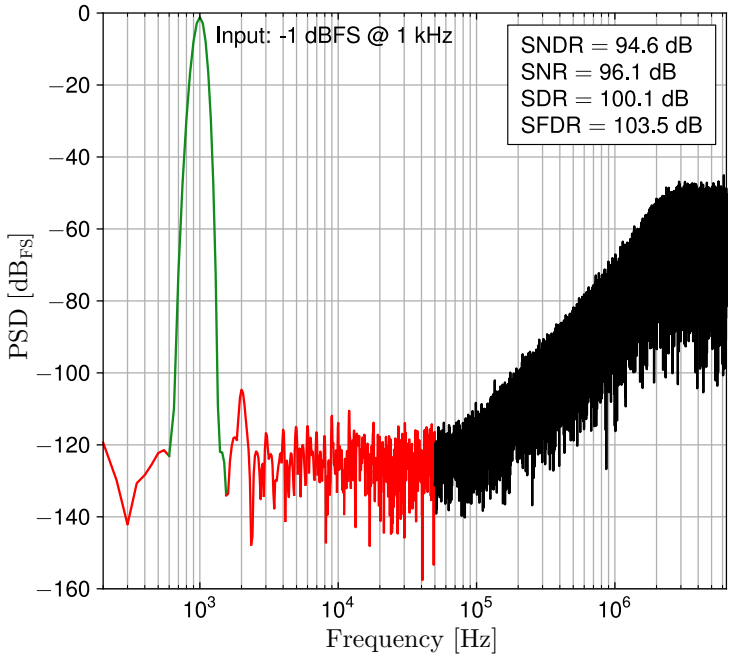

Figure 6.7 | Measured PSD of the Multi-Bit ΔΣM from Fig. 6.6.

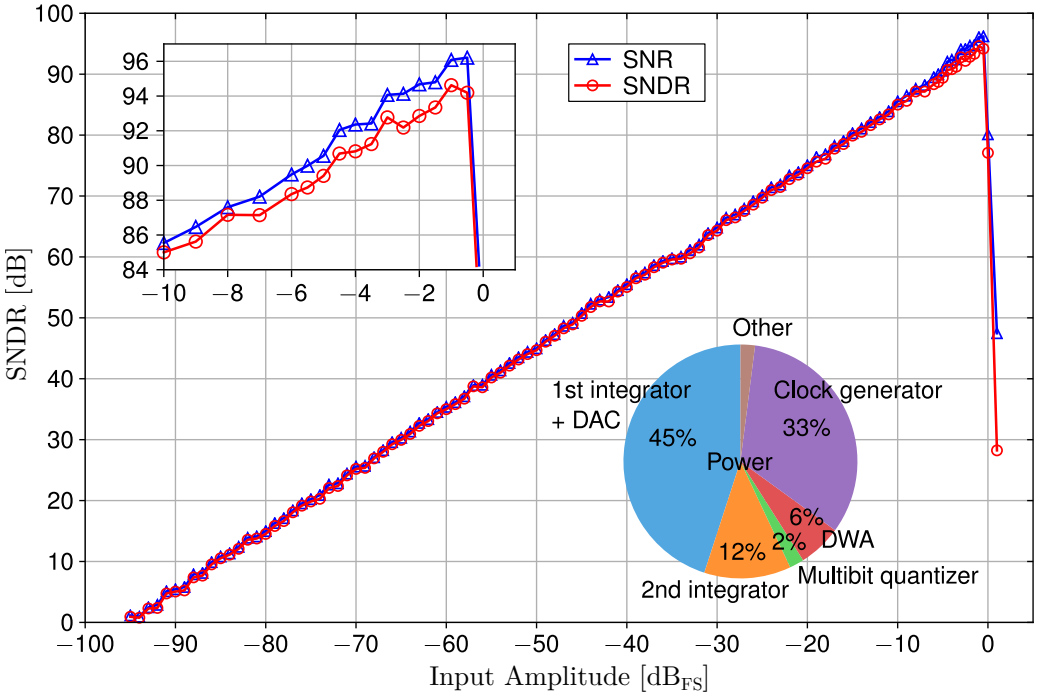

Figure 6.8 | Measured SNDR curve of the Multi-Bit ΔΣM from Fig. 6.6 and power distribution.

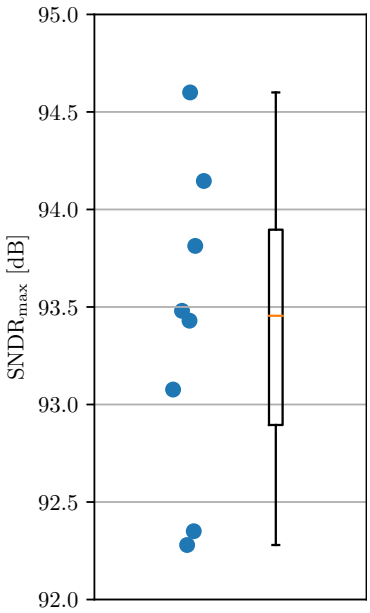

Figure 6.9 | Maximum SNDR measured from several Multi-bit ΔΣM IC samples.

	[27]	[30]	[31]	[44]	[45]	[46]	[47]	[78]	[80]	This Work
ΔΣM Arch.	Loop	Loop	Loop	Loop	Loop	Zoom	Zoom	Incremental	MASH	Loop
Topology	CT	CT	CT	SC	SC	SC	SC	SC	SC	SC
Technology [nm]	65	65	65	350	180	160	160	65	250	180
Supply Voltage [V]	1.2	1.2	1.2	5	0.7	1.8	1.8	1.2		1.8
Diff. Full-scale [Vpp]						3.5			6.6	2
f_{samp} [MS/s]	6.14	8	7.2	5.12	5	11.29	3.5	10.2	20	12.8
Bandwidth [kHz]	24	24	24	20	25	20	20	20	1000	50
Power [mW]	0.068	0.134	0.114	55	0.87	1.65	0.44	0.55	475	0.80
Area [mm^2]	0.14	0.28	0.39	5.6	2.16	0.16	0.27	0.134	20.2	0.2
DR [dB]	98.2	103.5	104.8	111.0	100.0	107.5	109.8	101.8	103.0	96.1
$SNDR_{max}$	94.1	99.4	100.9	105.0	95.0	98.3	106.5	100.8		94.6
FoM_S [dB]	179.6	181.9	183.3	160.6	169.6	169.1	183.1	176.4	166.2†	172.6
Bootstrap-free	Y	N		Y	N	N	N	Y	Y	Y
Calibration-free	Y	Y	N	Y	Y	Y	Y	Y	Y	Y
Resistor-less	N	Y	N	Y	Y	Y	N	Y	Y	Y

†FoM calculated using DR instead of SNDR

Table 6.1 Comparison of high-resolution ($SNDR_{max} \geq 90dB$) general-purpose ($BW \geq 20kHz$) ΔΣMs to the presented Multi-bit SC ΔΣM realization.

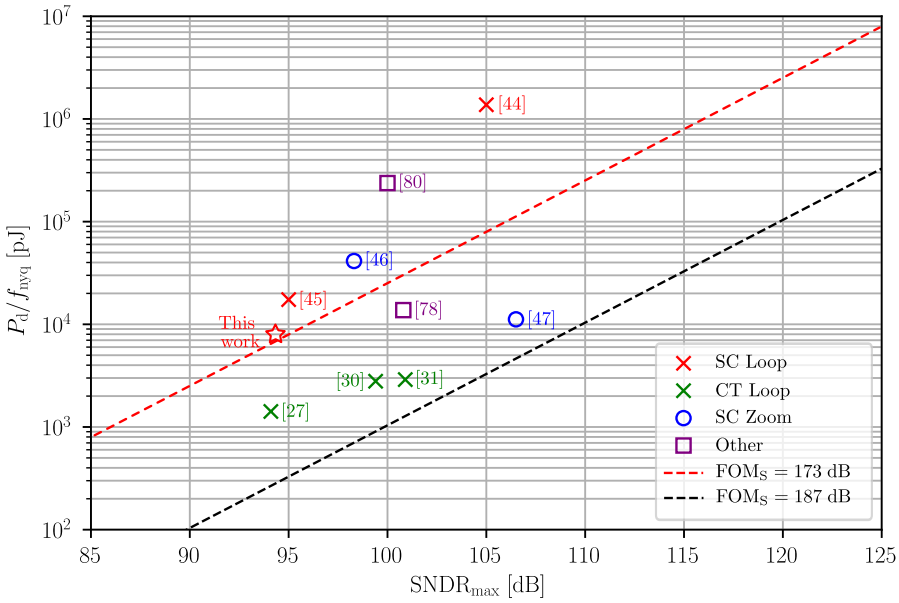

Figure 6.10 State-of-art chart showing the Mulyi-Bit ΔΣMs from Table 6.1. Absolute general FoM$_S$ in dashed black and absolute SC FoM$_S$ in dashed red.

6.2.1 Radiation-Hardness Test Results

The presented ΔΣM samples in Section 6.2 have also undergone a TID test in order to check the deterioration of the ICs under a rad-hard environment, and its suitability for space missions.

The test consists on the bombardment of high-energy particles, emulating the TID the chips would take at space during years of mission. It and was carried out at ESA-ESTEC Co-60 facility [135], which uses the Co-60 isotope as the irradiation source. The facility consists of the radiation cell and a large external control room with fourteen cable feed-throughs that enable the remote monitoring and controlling of experiments. The Co-60 source is placed in a container so that the gamma beam produced by the Co-60 decay exits the irradiator unit through a collimator window into the radiation cell. The DUTs are placed inside the irradiation room in a vertical position in front of the source collimator. A photography of the irradiation setup is illustrated in Fig. 6.11.

The DUTs should be powered and running in normal operation during the irradiation process to better emulate the actual conditions during space missions. Some unbiased samples were also added in the process with the aim of checking differences in the results between biased and unbiased chips. Small biasing boards were designed for this purpose, leaving the test PCB out of the process to avoid damage to the components and therefore corrupting the measurements.

a) b)

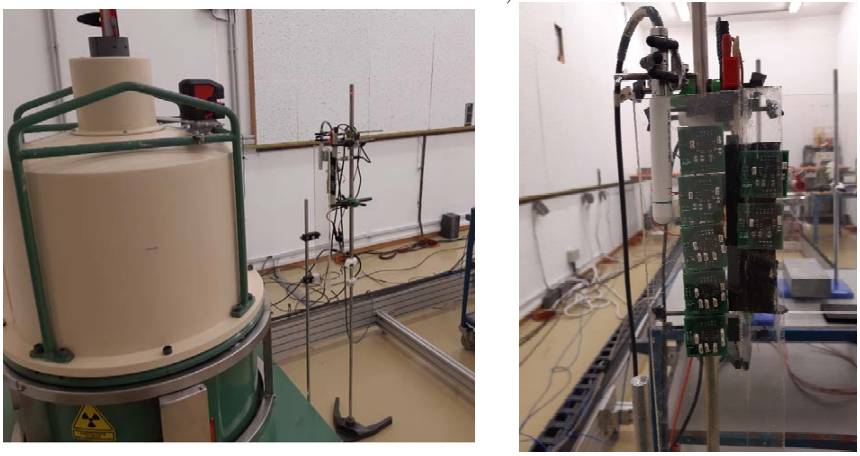

Figure 6.11 Test setup positioning in the irradiation room (a) and front view of the setup (b).

The test plan consisted on applying a total TID of 100 krad, which is the rated value for most space missions, in steps of 20 krad and then measure the ADC parameters at the end of each step before continuing with the irradiation process. It was decided that some of the samples would only receive some of the irradiation steps so that their final TID would be different smaller 100 krad. The purpose of this was to have the availability of a better characterization at different TID levels with superior lab equipment than the available at the Co-60 facility. The final TID each sample received is summarized in Table 6.2.

Sample ID	1	2	3	4	5	6	7
TID [krad]	20	40	60	80	100	100†	100†

Table 6.2 TID received by each of the Multi-bit ΔΣM samples taking part in the irradiation process. †Note: Samples 6 and 7 were unbiased during this process

The current consumption for each sample was measured at each of the irradiation steps, as presented in Fig. 6.12. The analog consumption was set to be slightly higher than in regular operation for these tests. The test shows that the current stays constant at every step for every sample. This is a good indicator of the robustness of the ICs against radiation, demonstrating that additional current paths have not been created due to latch-up or the breakdown of any part of the circuit.

The maximum SNDR for each sample was measured before and after the final irradiation step for each sample, as illustrated in Fig. 6.13. For every case, the variation in the measured resolution is smaller than 1 dB. In some cases the measured resolution after the irradiation is a bit larger and it does not seem to have any relationship with the received TID. The differences can likely be attributed to environmental factors of the laboratory rather than the irradiation process. Finally, the full post-radiation SNDR measurements for every sample are shown in Fig. 6.14.

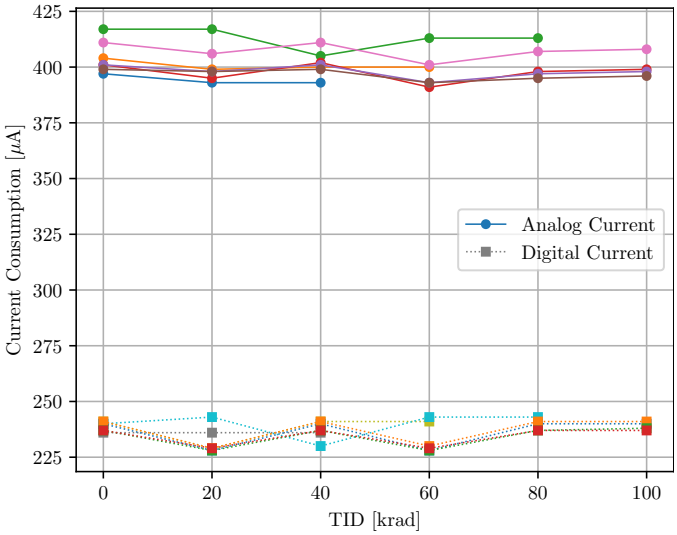

Figure 6.12 Measured current consumption from several Multi-bit ΔΣM IC samples at the different TID steps.

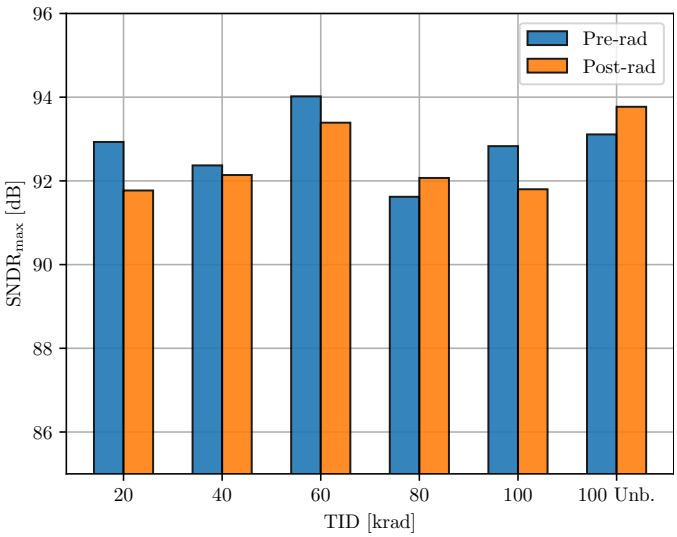

Figure 6.13 Measured maximum SNDR from several Multi-bit ΔΣM IC samples before and after irradiation for different TID.

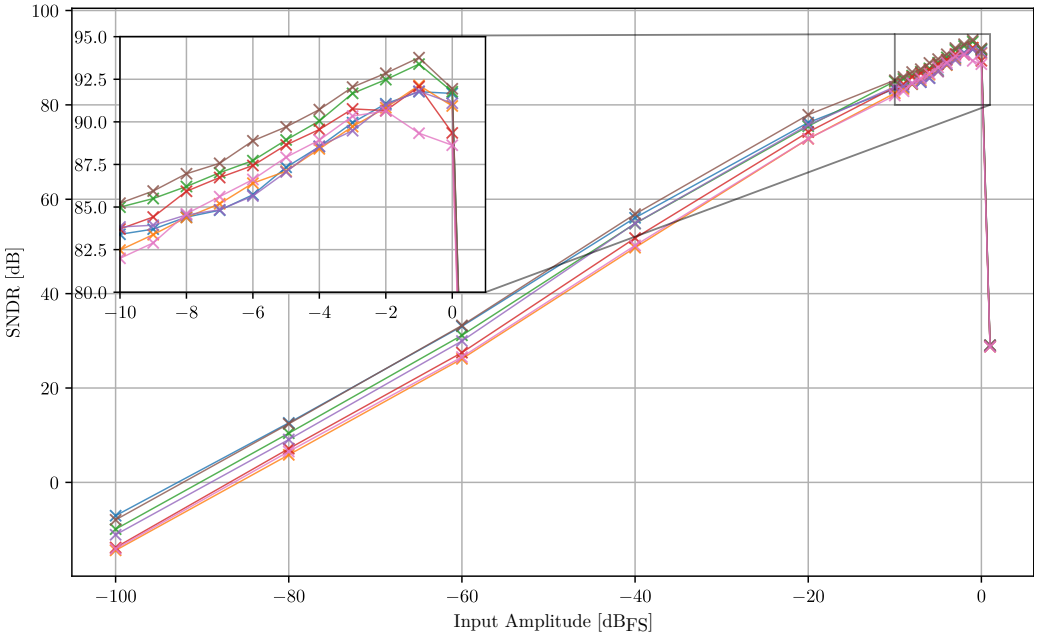

Figure 6.14 | Measured SNDR curves from several Multi-bit ΔΣM IC samples after the irradiation process.

From these measurements is therefore concluded that the ADCs continue to work properly and their performance does not degrade at least up to TID = 100 krad.

6.3 Floating-Point ΔΣM Measurement Results

The chip photo of the Floating-Point SC ΔΣM circuit fabricated in 180 nm 6-metal CMOS technology is shown in Fig. 6.15. The overall circuit occupies 0.24 mm^2 and it consumes 610 μA from the combined analog and digital 1.8 V power supplies.

The test setup followed the illustration in Fig. 6.1. The corresponding SNDR curves from Fig. 6.16a return a combined DR of 100 dB with a peak SNDR of 86.7 dB in a bandwidth of 50 kHz. Fig. 6.16b shows the measured output PSD for each of the three AGC scaling factors at the point −20 dBFS. As expected, the 60 dB/dec quantization noise scales at 6 dB per octave of k_{fp} where as the in-band thermal contributions show a 3 dB change. These measurements where taken using static scaling factors with a harmonic signal at 1.25 kHz.

Fig. 6.17 illustrates the transient operation of the AGC when the loop is closed using the FPGA implementation from Fig. 6.5b, which consists on a CIC decimator, a digital envelope detector and a thresholding block. The input of the system is an AM signal carrier at 12.5 kHz modulated at m=75%, f = 100 Hz, obtained from the 8904A Multifunction Synthesizer from Hewlett Packard, USA. The CIC decimator and the envelope detector

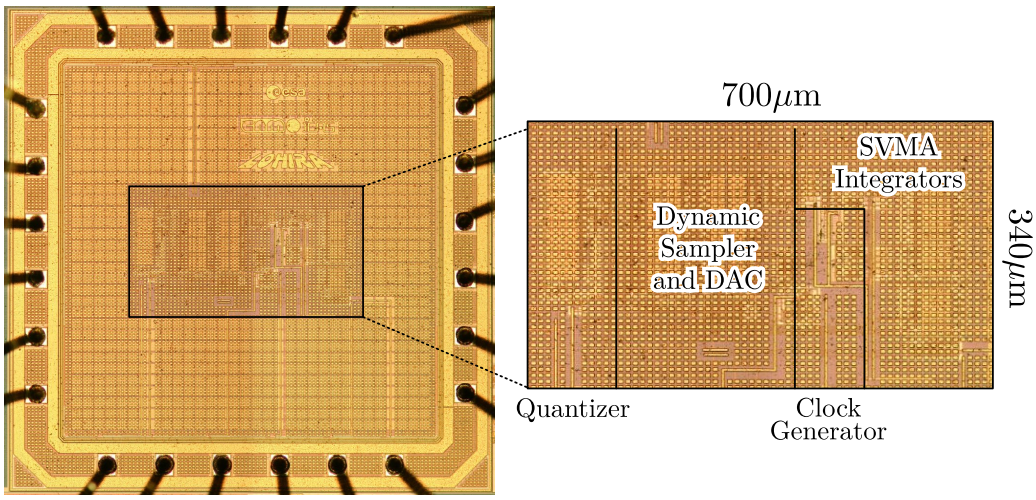

Figure 6.15 | Floating-Point ΔΣM IC, fabricated in 180 nm CMOS technology.

filter the signal so that the amplitude of the envelope amplitude can be measured. Then, the thresholding block sets the appropriate Floating-Point gain by comparing the signal amplitude to the decision thresholds, set at −24 dBFS and −18 dBFS. Thanks to the internal memory updating mechanisms, the restored signal does not show any in-band nor out-band harmonics due to the AGC operation, as shown in Fig. 6.18, a fact that emphasizes the high linearity of the Floating-Point operation in contrast to the classic AGC architecture shown in Fig. 4.2.

Table 6.3 summarizes the performance of the presented circuit in comparison with state-of-art high dynamic-range ΔΣM ADCs, which features a competitive 176.6 dB Schreier FoM when taking into account the dynamic-range instead of the maximum SNDR.

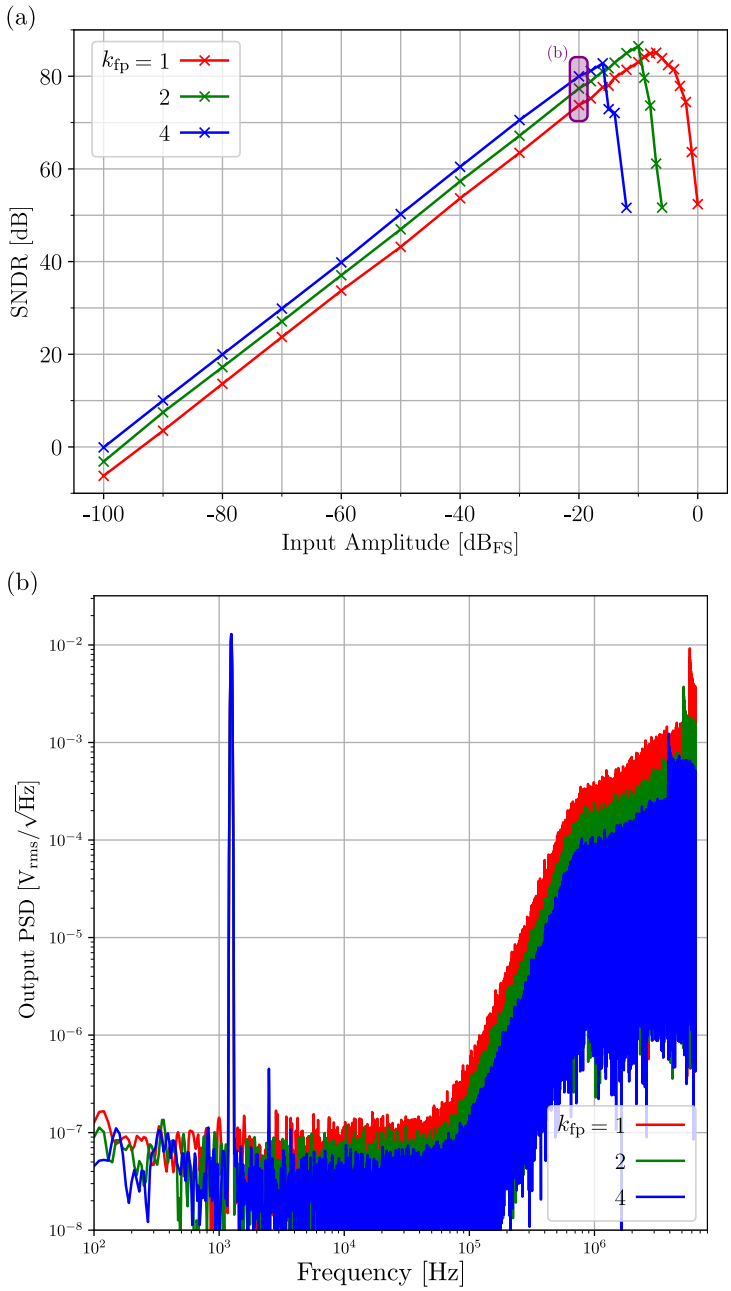

Figure 6.16 | Measured SNDR (a) from the Floating-Point ΔΣM in Fig. 6.15a and PSD at an input of −20 dBFS for each gain factor (b).

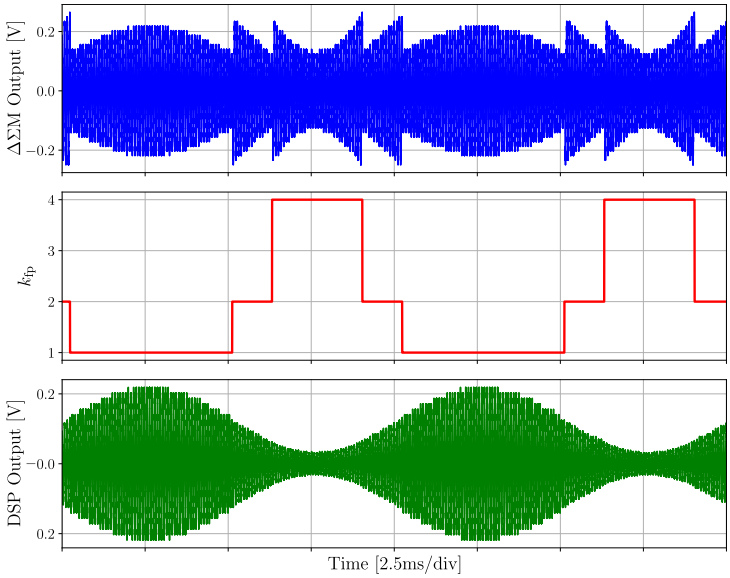

Figure 6.17 | Measured raw output from the Floating-Point ΔΣM in Fig. 6.15 (blue), AGC values after closing the control loop (red) and reconstructed output (green) for a 12.5 kHz harmonic input when 75 % modulated in amplitude at 100 Hz. For clarity purposes, the 1-bit raw data is displayed here after being filtered using a 128-point sliding-window averaging.

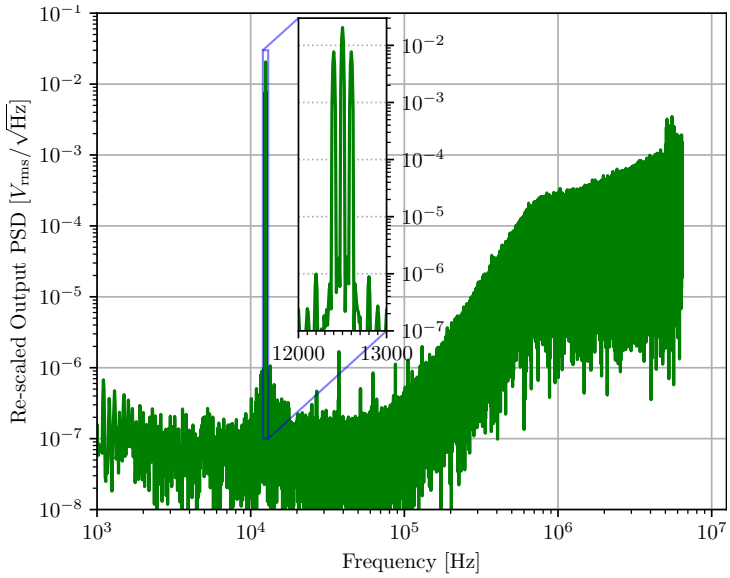

Figure 6.18 | Measured PSD from the raw-data sequence shown in Fig. 6.17.

	[11]	[33]	[39]	[42]	[45]	[47]	[136]	[137]	[138]	This Work
Architecture	SAR	ΔΣM	ΔΣM	ΔΣM	ΔΣM	ΔΣM	Pipe	Pipe	Slope	ΔΣM
Subtype	-	Zoom	Loop	Zoom	Loop	Zoom	Float	Float	Float	Float
Topology	SC	CT	SC	SC	SC	SC	SC	SC	-	SC
Technology [nm]	55	160	350	160	180	160	500	180	180	180
Supply Voltage [V]	2.5/1.2	1.8	5.4	1.8	0.7	1.8	5	1.8	1.8	1.8
f_{samp} [MS/s]	0.512	5.12	640	2	5	3.5	20	60	0.003	12.8
Bandwidth [kHz]	0.25	20	1	1	25	20	10000	30000	1.5	50
Power [mW]	0.028	0.618	12.7	0.280	0.87	0.44	380	300	0.007	1.1
Area [mm^2]	0.068	0.27	11.48	0.25	2.16	0.27	13.76	7.45	0.004	0.20
$SNDR_{max}$	103.0	106.4		118.1	95.0	106.5	59.0	61	49.9	86.7
DR [dB]	109.4	108.5	136.3	120.3	100.0	109.8	90.0	80	116.1	100.0
FoM_S† [dB]	178.9	183.6	185.3	185.8	174.6	186.4	164.2	160.0	199.4	176.6

†FoM calculated using DR instead of SNDR

Table 6.3 Comparison of different ΔΣMs featuring high dynamic-range to the presented Floating-Point ΔΣM.

Conclusions | 7

7.1 Contributions

As a result of the research work presented in this PhD thesis, the main hypotheses given in Chapter 1 have been verified, stating that:

> It is possible to obtain a low-power high-performance calibration-free state-of-art ADC in standard CMOS technology by means of an optimized SC ΔΣM architecture and circuits. This architecture can be migrated to lower node technologies by following a dedicated design methodology. By special rad-hard design guidelines, the resulting circuits can be made suitable for space applications. Also, it is possible to incorporate AGC capabilities into the ΔΣM architecture by introducing some appropriate changes.

The most important contributions from this work that give prove to the above statement can be summarized as:

- Implementation and fabrication of a Multi-bit ΔΣM in a 180 nm CMOS technology exhibiting a competitive FoM from experimental measurements.
- Rad-hard testing of the 180 nm Multi-bit ΔΣM proving the chip can withstand most space missions, at least up to TID = 100 krad.
- Implementation and on-going fabrication of a Multi-bit ΔΣM in a 65 nm CMOS technology and integration as an IP block for a digital core, incorporating the decimation filter and an AXI-4 Lite communication bus. The design exhibits a high FoM from post-layout simulations.
- Implementation of a Multi-bit ΔΣM in a 22 nm CMOS technology, exhibiting a high FoM from post-layout simulations.
- Elaboration of a mathematical framework consisting on design equations and architectural level simulations that can be used to elaborate a design methodology suitable for the design of Multi-bit ΔΣMs in different technology nodes.

- Implementation and fabrication of a Floating-Point ΔΣM with distortion-less AGC in a 180 nm CMOS technology, demonstrating the operation of AGC and exhibiting a remarkable FoM from experimental measurements.

From all the work presented in this PhD thesis, the following contributions have been disseminated through the following publications in journals and conferences:

- A. Suanes, M. Dei, L. Terés and F. Serra-Graells, "A 16-bit 50kHz 177dB-FOMS Calibration-Free Bootstrapping-Free SC Delta-Sigma Modulator IP Block for Low-Power High-Resolution ADCs", in 2020 XXXV Conference on Design of Circuits and Integrated Systems (DCIS), pp 1-6, Segovia, Spain, November 2020. https://doi.org/10.1109/DCIS51330.2020.9268617
- A. Suanes, L. Terés, M. Dei and F. Serra-Graells, "A 0.8mW 50kHz 94.6dB-SNDR Bootstrapping-Free SC Delta-Sigma Modulator ADC with Flicker Noise Cancellation", in IEEE International Symposium on Circuits and Systems (ISCAS), pp 1-5, Daegu, Korea, May 2021. https://doi.org/10.1109/ISCAS51556.2021.9401688
- A. Suanes, L. Terés, M. Dei and F. Serra-Graells, "A 85dB-SNDR 50kHz Bootstrapping-Free Resistor-Less SC Delta-Sigma Modulator IP Block for PVT-Robust Low-Power ADCs", in Integration, Volume 84, 2022, Pages 159-170, ISSN 0167-9260. https://doi.org/10.1016/j.vlsi.2022.02.002

The following publications have been sent to their respective journals, but are still under revision process as of the day of the thesis write-up:

- A. Suanes, L. Terés, M. Dei and F. Serra-Graells, "A 0.8mW 94.6dB-SNDR 172.6dB-FOMS Bootstrapping-Free SC Delta-Sigma Modulator ADC with Flicker Noise Cancellation", submitted to Transactions of Circuits and Systems (TCAS).
- A. Suanes, L. Terés, M. Dei and F. Serra-Graells, "A 1.1mW 50kHz 100dB-DR Floating-Point Delta-Sigma ADC with Distortion-Less AGC", submitted to Journal of Solid-State Circuits (JSSC).

7.2 Future Work

There are still some tasks that could not be finished by the time of deposit of this thesis and some other new opportunities that arouse from the results obtained from this work, which can be summarized as:

- Experimental testing of the 65 nm Multi-bit ΔΣM IP is pending. From the standalone ADC tests to the system tests of the IP, including the decimation filter and the AXI peripheral, and its operation with the digital core.

- The 22 nm Multi-bit ΔΣM is pending of manufacturing, waiting for an available tape-out window.
- Following the IP block testing along with a digital core, different sensors could also be integrated to measure several variables of interest (e.g. processor temperature, sypply current sensing, etc...).
- The use of the Floating-Point ΔΣM for audio applications requiring AGC could be investigated and a closed application could be developed.
- Given the positive results from the TID test of the 180 nm Multi-bit ΔΣM up to 100 krad, this range could be extended beyond that to find out which dose level causes the breaking point of the chip. Also, SEE tests could be undergone in order to check the susceptibility of the chip to these radiation effects.
- The same radiation-hardness tests could be applied to the 65 nm design to check susceptibility differences in this technology node.

The presented Multi-bit ΔΣM designs could be adapted and used as IP blocks in ASIC designs intended for space missions by the ESA, as the founder of this project under the contract 4000124840/18/NL/MH denominated *"**Lo**w-power **Hi**gh-resolution **Ra**d-hard ADCs for Space Applications (LOHIRA)"*.

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