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Low-Power Step-up Circuits for Energy Harvesting



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Abstract

Due to the significant growth of the Internet of Things (IoT), wearable devices and low-power sensors are experiencing exponential demand across various applications, ranging from environmental monitoring to the healthcare and wellness sectors. The demand for self-powered devices and sensors, along with the need for cheaper, faster, and more sustainable fabrication methods, is rising. To tackle these challenges, the current research on printed electronics paves the way for the design of low-cost and flexible devices for harvesting applications, becoming a key enabling technology to develop new applications. The primary way to obtain self-powered devices is to focus on energy harvesting through sustainable power sources, like thermoelectric, solar, vibrations, RF, triboelectric, etc. In sufficiently low-power applications, these energy sources may even eliminate the need for batteries, reducing even more fabrication costs and pollution. In this work, the process of designing an energy harvester that can power a real-life application is explored, as well as the challenges and benefits of using flexible hybrid electronics for this task. The process is addressed holistically, from the introduction of thermoelectric generators, to the DC-DC converters and startup circuits that conform the core of the harvester circuit. Consequently, this thesis work presents the design and optimization of a flexible environmental sensing circuit using flexible hybrid electronics. Furthermore, it presents a novel self-powered oscillator topology, with a startup voltage lower than $10mV$ and a conversion ratio on-par with the state of the art. Additionally, this work introduces a novel DC-DC converter topology, designed to integrate this oscillator circuit as its startup stage, with a startup voltage around $100mV$ and the implementation of a Maximum Power Point Tracking (MPPT) method for greater efficiency, improving over the startup voltage of commercial alternatives. In conclusion, in this thesis work, novel topological designs for low-power energy harvesting based in Thermoelectric Generators (TEGs) were accomplished. The results evidence the importance of a holistic approach from electronic design to manufacturing and validation setups, to build reliable and efficient TEG based systems, which is crucial for their adoption in real applications.

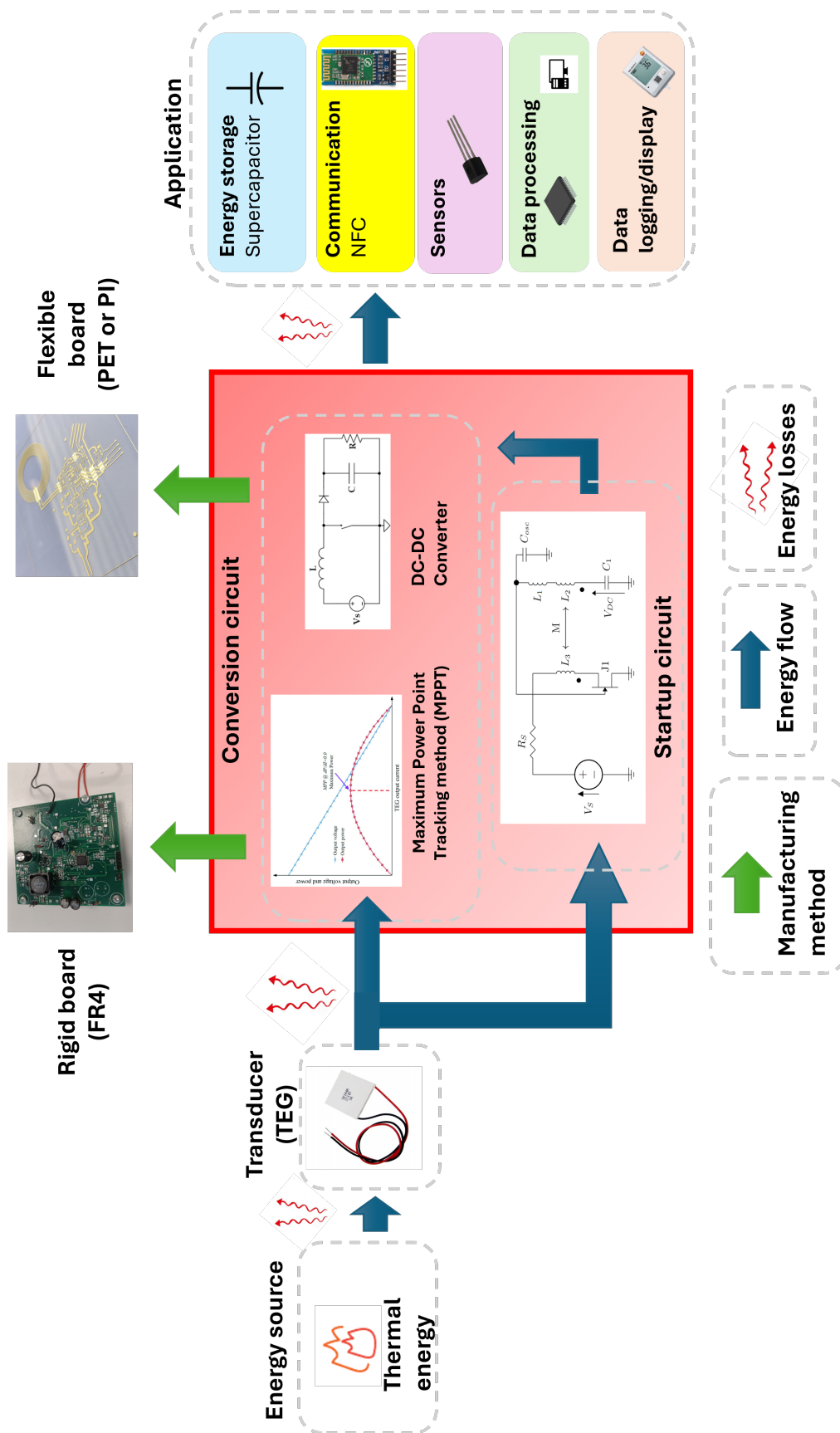


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Chapter 1

Introduction

In this chapter, an introduction to the research field topics related to this thesis work is described to ensure familiarity with the fundamental terms and basic concepts relevant to this work. Each subsequent chapter will begin with a more in-depth introduction to the specific topics under consideration. This approach is designed to gradually build knowledge, introducing complex concepts in a step-by-step manner to facilitate this dissertation readership.

In addition, this thesis is framed in the Marie Skłodowska-Curie Innovative Training Network (ITN) "HORATES" (Hybrid and Organic Thermoelectric Systems), a project based on creating printed hybrid (this is, using both organic and inorganic materials) and organic TEGs to use in energy harvesting applications. Within the HORATES project, the development and optimization of Organic Thermoelectric Generators (OTEGs) are pursued through a holistic, interdisciplinary approach. The project is structured around four scientific Work Packages (WPs), each addressing different aspects of the development process required to realize efficient and scalable OTEG modules. The focus of this thesis, as a result of the work of the author in this project, is on the design and fabrication of the aforementioned circuits, voltage step-up circuits, to harness the energy from low-voltage OTEGs, working in close collaboration with the TEG materials scientists.

1.1 Energy Harvesting

The IoT revolution (Figure 1.1), characterized by a distributed network of interconnected devices, has created a demand for energy harvesting technologies that are both autonomous and sustainable. In many IoT applications, connecting devices to the power grid is impractical, and reliance on batteries is undesirable due to the need for frequent replacements and environmental concerns. While solar power is an established and viable solution in many cases, it is ineffective in environments with intermittent or no light conditions. Here, different forms of ambient energy harvesting, such as solar, thermoelectric, piezoelectric, or triboelectric energy harvesting, among others, can play a crucial role by converting available energy into electricity, enabling the operation of IoT devices in a wide range of settings.

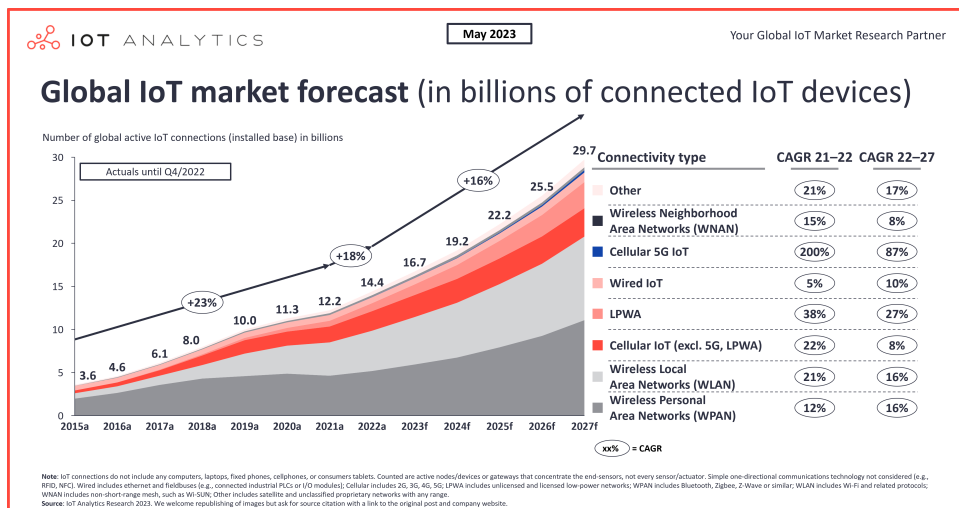


Fig. 1.1: IoT Market Forecast up to 2027. Source: [1]

As the name implies, ambient or environmental energy harvesting consists in harnessing available energy from the environment. To this end, transducers such as photovoltaics cells or TEG, among others, are used to convert different types of energy into electrical energy. Some of the currently relevant energy harvesting sources are [2]:

- Electromagnetic energy (or Radiofrequency (RF)), such as wireless internet, radio, TV signals, etc. [3]
- Thermal, which can be harvested with TEGs when there is a temperature difference between the ends of a thermocouple [4].

- Solar [5].
- Mechanical energy, harvested by an electromechanical transducer such as a piezoelectric [6] or a triboelectric generator [7], among others.

Table 1.1 shows baseline harvested power density levels for different energy harvesting sources. Furthermore, in Section section 1.3, there is an in-depth compilation of the state of the art on printed thermoelectric generators (TEGs), presented in both table and graph formats. Each TEG is categorized based on its maximum output voltage, maximum output power density, and the materials employed in its fabrication.

| Source | Harvested Power Level |
|--------------------------|------------------------|
| Mechanical | |
| Wearable - Piezoelectric | $64.9\mu W/cm^2$ |
| Wearable - Triboelectric | $50mW/cm^2$ |
| Radio Frequency | |
| GSM | $0.1\mu W/cm^2$ |
| WiFi | $1\mu W/cm^2$ |
| TEG | |
| Wearable - with heatsink | $2.2 - 44.4\mu W/cm^2$ |
| Industrial | $1 - 10mW/cm^2$ |
| Solar | |
| Indoor | $10\mu W/cm^2$ |
| Outdoor | $4 - 40mW/cm^2$ |

Table 1.1: Harvested Power Levels from Different Sources. Sources: [8, 9].

Lastly, Figure 1.2 shows estimates of power consumption for different components of a circuit and whole medical devices, as a way for the reader to have an estimate of the capabilities of current TEGs to power devices.

TEG devices work as transducers, generating electrical energy when there is a temperature difference (ΔT) between their thermocouples. The HORATES project encompasses the whole fabrication process, from the synthesis of materials, doping, printing and upscaling (device making), as well as the electronic circuit used to harvest their energy and supply power to an application.

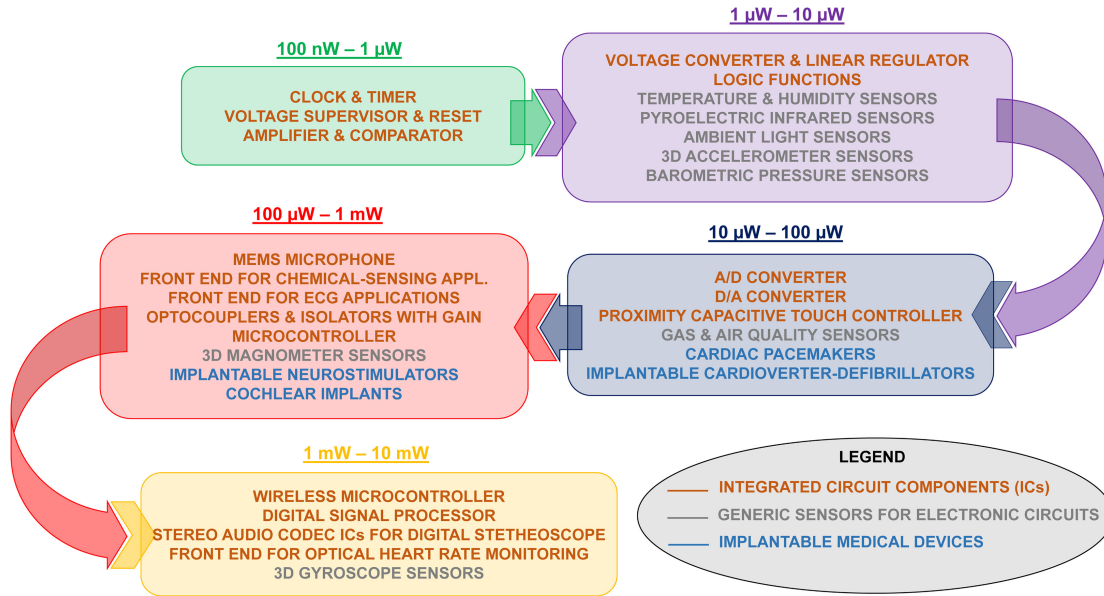


Fig. 1.2: Power consumption of different devices. Source: [10].

The resulting TEGs provide electrical energy in the form of a voltage proportional to ΔT , where the proportionality constant is called the Seebeck Coefficient (α), resulting in $V_{TEG} = \alpha * \Delta T$ [11]. Currently, the Seebeck coefficient of OTEGs is much lower than the one of inorganic TEGs. This results in a low output voltage, normally unable to power any conventional electronic circuit. As a result, an extra circuit is needed to transform the energy harnessed from the generators to a voltage level where it could be used.

Within the HORATES project, the development and optimization of OTEGs are pursued through a holistic, interdisciplinary approach. The project is structured around four scientific Work Packages (WPs), each addressing different aspects of the development process required to realize efficient and scalable OTEG modules. The focus of this thesis, as a result of the work of the author in this project, is on the design and fabrication of the aforementioned circuits, voltage step-up circuits, to harness the energy from low-voltage OTEGs. The basic energy harvesting process is illustrated in Figure 1.3, with the conversion circuit being the focus of this thesis.

The inclusion of a voltage step-up circuit is crucial to harness the energy generated by these ultra-low-power TEGs, since the generated voltage is insufficient to power electronic devices directly, as can be appreciated in Figure 1.4, extracted from one of the articles derived from the HORATES project.

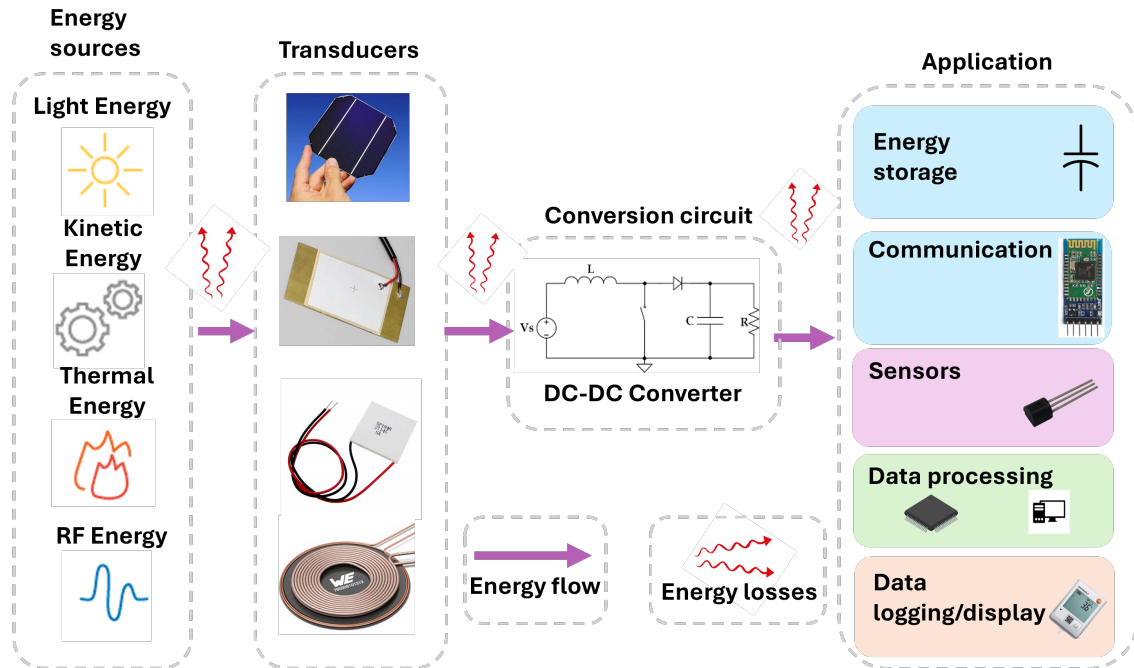


Fig. 1.3: Block diagram of a basic energy harvesting process. The conversion circuit is the focus of this thesis.

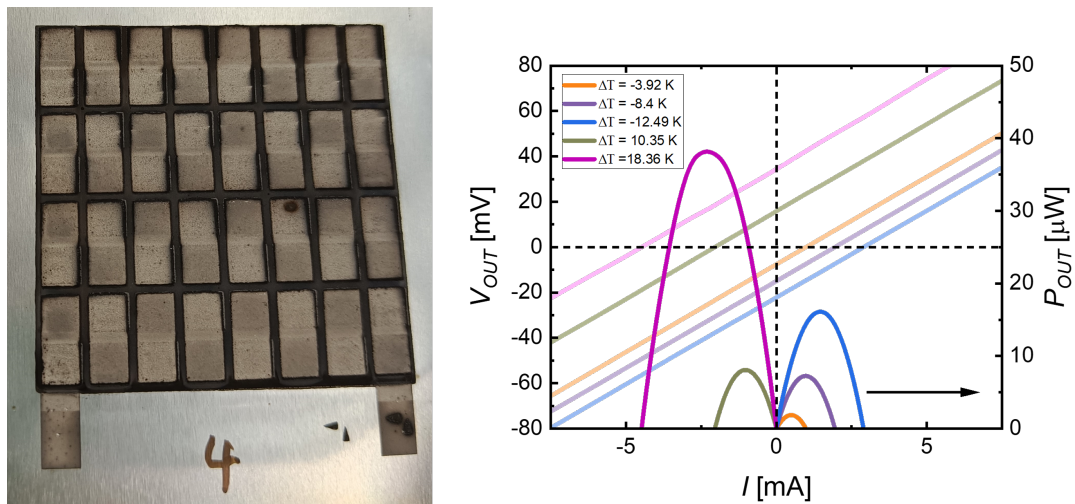


Fig. 1.4: Left: Printed inorganic TEG from the HORATES project. Right: Output power and voltage curves of the TEG. Source: [12].

1.2 DC-DC Converters

These voltage step-up circuits, or step-up converters, are part of a type of circuit called DC-DC converters. DC-DC power converters, are widely abundant as they are found in laptops, mobile phone chargers, power supplies, and a large array of devices.

They take an unregulated DC input signal, and transform it into a regulated DC output signal. They generate a regulated DC voltage transforming the input signal, by altering one of its characteristics, namely, raise the voltage while lowering the current, or lower the voltage while raising the current, with the first method being the relevant one for this topic. This voltage boosting capability makes DC-DC converters attractive for low-voltage energy harvesting. Various techniques exist in the field of DC-DC conversion to achieve voltage amplification, many of them illustrated in Figure 1.5.

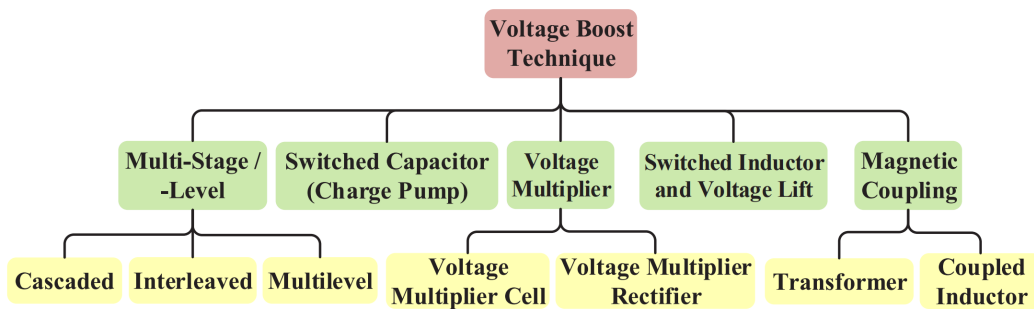


Fig. 1.5: Diagram of voltage boosting techniques. Source: [13] © 2016 IEEE

The most favored or prolific techniques in the literature for low-voltage boosting are the next:

- Switched capacitors, due to their easy on-chip integration, scalability, and high power density. When integrated on-chip, these circuits can integrate multiple stages to obtain a high conversion ratio, while maintaining an acceptable form factor [14].
- Switched inductors, such as boost converters, as they can obtain a relatively high and flexible conversion ratio with overall great efficiencies, while being not very complex circuits. Their efficiency starts to drop for very high Conversion Ratios (CRs) (very low input voltage).
- Voltage multipliers, which are usually used coupled with another of the aforementioned techniques. These circuits consist mainly of diodes and capacitors, although some

may use inductors for extra amplification. In the same way as the charge pumps, these circuits can be cascaded in multiple stages for higher amplification, and they can work when put in the middle of a circuit, amplifying an alternating signal, or at the output, amplifying the voltage and also rectifying it [15].

- Voltage booster circuits based on magnetic coupling, such as flyback converters [16], or self-powered oscillators [17], with the use of transformers or coupled inductors to amplify the voltage, mostly through their turn ratios.

An exhaustive analysis of the existing topologies, as well as a comparison between them, can be found in the work of Forouzesh et al. [13]. Moreover, chapter 4 elaborates on how the basic DC-DC converter topologies operate.

Given the critical role of voltage step-up converters in this application, their design and optimization are of crucial importance. In the context of the HORATES project, where the focus is on creating highly efficient and scalable OTEGs-based energy harvesters (among other applications), the choice of step-up voltage circuits is guided by several factors, including the specific requirements of the low-voltage energy sources and the constraints of a market that is still in its infancy [18].

To address these needs effectively, one of the constraints was to design the circuits using exclusively discrete components, rather than Application-Specific Integrated Circuits (ASICs). This choice is primarily driven by cost considerations and development time, although it has the adverse effect of impacting negatively on the minimum power consumption attainable by the circuits.

In niche markets where the production volume does not justify the expense of custom ASIC development, discrete components offer a more flexible and economical solution. Discrete designs allow for easier adjustments and optimizations tailored to the specific performance needs of the energy harvesting applications, without incurring the high costs associated with ASIC design and fabrication. Besides, to further emphasize this flexibility, all the circuits presented in this thesis are fabricated with Commercial Off-the-Shelf (COTS) components, this is, components that can be bought and used in the circuit without any extra modification. For example, a hand-wound inductor would not be a COTS component, since it had to be modified and it was not bought as it is. Instead, a SMD inductor is a COTS component.

Nonetheless, ASICs have inherently lower power consumption when compared to their discrete counterpart [19], so their performance in low-power applications is going to be always better than that of a discrete circuit.

A summary of the advantages of ASICs and discrete circuits is presented next:

- ASICs
 - Higher performance.
 - Better power efficiency.
 - Greatly reduced footprint/area.
- Discrete circuits
 - Lower initial cost.
 - Higher flexibility in the design and posterior iterations (possibility of reworking the circuit).
 - Lower development time.

Once the decision to design the circuits using discrete COTS components is taken, the next logical step is to evaluate the suitability of the DC-DC converters currently available on the market for this application. A brief introduction to this topic is presented in the next section.

1.3 Commercial DC-DC Converters

As established in the previous section, hybrid and organic TEGs provide low output voltages (usually lower than 100 mV for low-temperature harvesting) and have moderate output resistances (greater than 10Ω) [20–22]. As a way to familiarize the reader with the output voltage and power capabilities of TEGs, a summary of parameters of TEGs in the current literature was done (until 2022), in the form of a table (Table 1.2) and graphical representations (Figure 1.7, Figure 1.6). This summary organizes them by printing method, normalized

Table 1.2: Summary of TEG characteristics from various references

| Ref. | $V_O(\Delta T)$ | $P_{OUT}(\Delta T)$ | ΔT | Maximum output power density | Inorganic/organic | Printing method (if any) |
|------|-----------------|---------------------|------------|-------------------------------|-------------------|--------------------------|
| [23] | 45 mV | 127 nW | 32.5K | - | Inorganic/Printed | Inkjet printing |
| [24] | 32 mV | - | 25K | 30.5 nW/cm ² | Organic/Printed | Inkjet printing |
| [25] | 1.05V | 342 μ W | 150K | 738 μ W/cm ² | Organic/Printed | Blade-coating |
| [26] | 31.2 mV | - | 60K | 1.4 mW/cm ² | Inorganic | - |
| [27] | 8.3 mV | 10 nW | 35K | 0.53 nW/cm ² | Inorganic | - |
| [28] | 260 mV | 4.95 mW | - | 153 μ W/cm ² | Inorganic | - |
| [20] | 1.3 mV/K | 1 μ W | 17.5K | 0.14 μ W/cm ² | Organic/Printed | Electrospraying |
| [29] | 78 mV | 7.9 μ W | 20K | - | Inorganic | - |
| [30] | ~40 mV | - | 60K | 4.1 mW/cm ² | Inorganic/Printed | Screen printing |
| [31] | - | 0.2 μ W | 30K | - | Textile | Rubber stamp printing |
| [32] | 8.8 mV | 138.67 μ W | 9.3K | 5.6 μ W/cm ² | Inorganic | - |
| [33] | 151 mV | 13 μ W | 50K | 0.344 μ W/cm ² | Inorganic/Printed | Screen printing |
| [34] | 11.9 mV | - | 9.2K | 0.64 μ W/cm ² | Hybrid/Printed | Screen printing |
| [35] | 7.38 mV | 123.74 μ W | 1.24K | 8.32 μ W/cm ² | Inorganic | - |
| [36] | 37.2 mV | 192.6 μ W | 50K | 16.7 μ W/cm ² | Inorganic | - |
| [37] | 520 mV | 0.32 μ W | 85.5K | - | Organic/Printed | Screen printing |
| [38] | 17.8 mV | 2.2 μ W | 100K | 10 μ W/cm ² | Organic/Printed | Blade-coating |
| [39] | 40 mV | 0.9 mW | 6K | 12.1 μ W/cm ² | Inorganic | - |
| [40] | 7.1 mV | 157.2 nW | 51.6K | 75 μ W/cm ² | Organic | - |
| [41] | - | - | 20K | 0.266 μ W/cm ² | Hybrid/Printed | Inkjet printing |
| [42] | 43 mV | 33 μ W | 20K | 280 μ W/cm ² | Inorganic/Printed | Dispenser printing |
| [43] | 534 mV | - | 30K | 47.8 μ W/cm ² | Hybrid/Printed | Screen printing |
| [44] | ~26 mV | 4.64 μ W | 44K | 7 μ W/cm ² | Textile | - |
| [45] | 83 mV | 5 μ W | 60K | - | Textile | - |
| [46] | 0.979 mV | 2 nW | 0.6K | - | Textile | - |
| [47] | 44 mV | 16 nW | 50K | - | Textile | - |
| [48] | 0.512 mV | - | 10K | - | Textile | - |
| [49] | - | - | 10.1K | 48.2 nW/cm ² | Organic | - |

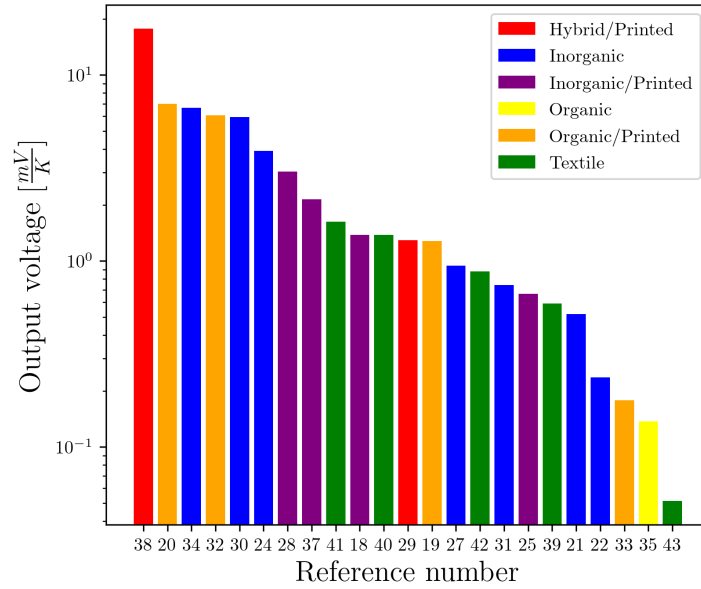


Fig. 1.6: Normalized output voltage of TEGs in Table 1.2

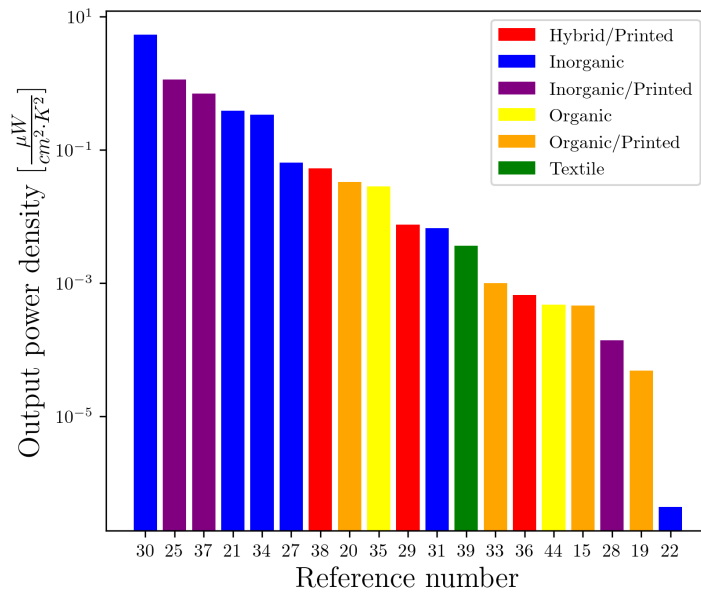


Fig. 1.7: Normalized output power density of TEGs in Table 1.2

output voltage, normalized output power density and type of materials utilized (organic, inorganic or hybrid).

Observing the figures, it is confirmed that the inorganic TEGs lead in normalized output power density, even when comparing among different methods of fabrication. There are some hybrid/organic TEGs leading the output voltage (three, specifically), but that can be attributed to bigger area (since the output voltage is not normalized against the area of the device or the number of thermocouples), or, in the case of the work of Mytafides et al. [25], due to the use of Single-Walled Carbon Nanotubes (SWCNT) as both p-type and n-type thermoelectric material, “resulting in exceptionally high performance”. It is important to note that while these works lead in their maximum output voltage characteristics, they fall behind the inorganic TEGs in power density, indicating a higher output resistance for the former. Finally, for hybrid or organic TEGs, the maximum output voltage observed is approximately $2mV/K$, while the output power density is lower than $100nW/(cm^2K^2)$. This highlights the need for custom-designed DC-DC converters to work with them.

As such, these TEGs need DC-DC converters adapted to these conditions. The commercially available DC-DC converters currently on the market can be separated into two groups. The first group consists of DC-DC converters aimed at low-voltage and low-resistance generators. The reason they can work with low voltages is that they are usually based on topologies with a positive feedback loop, which limits the control that can be exercised over the converter. They tend to have low efficiencies, lack of MPPT methods (methods in charge of maximizing the power extraction efficiency), a narrow input voltage range, and high current draw at the input, limiting their use with sources of moderately high output resistance. A common example of this type of converter is the LTC3108 from Analog Devices, a converter commonly used in literature for energy harvesting applications (Figure 1.8 a), c)) [50].

The second group is aimed at higher voltages ($> 100mV$) and can work with a wider range of output resistances. They usually have good efficiency ($> 80\%$) and count with MPPT methods, but they need a higher voltage to start working, denominated as cold-start voltage. This cold-start voltage only has to be applied to start the DC-DC converter, and after that, it can keep working with the working voltage, which is lower. An example for this group of converters is the BQ25504 from Texas Instruments (Figure 1.8 b)) [51], or the MAX17220 (Figure 1.8 d))[52], used in one of the circuits developed in this thesis.

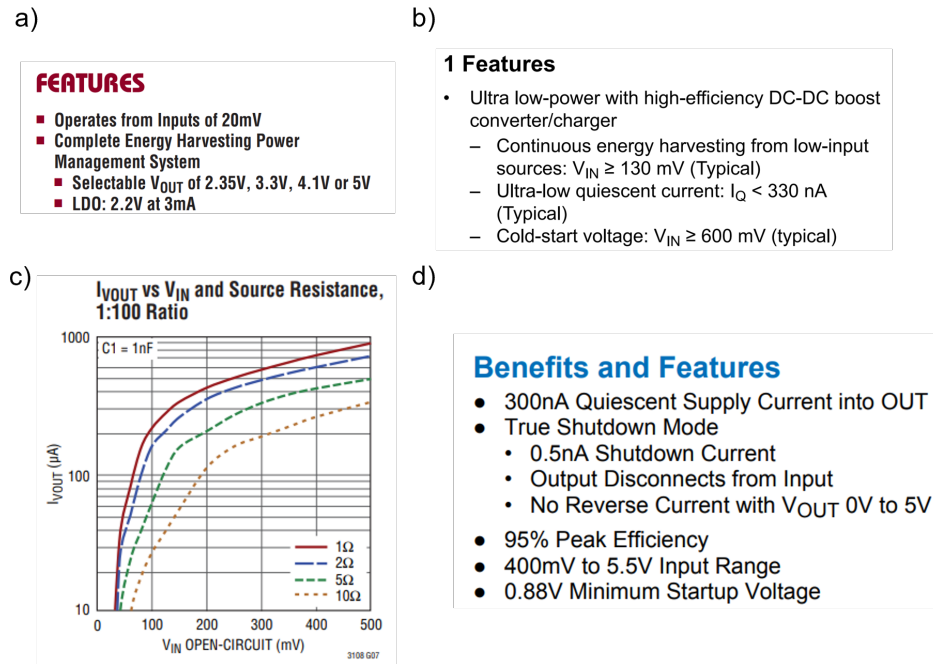


Fig. 1.8: a) Features of LTC3108 [50], b) Features of BQ25504 [51], c) Variation of cold-start voltage for LTC3108 due to generator source resistance, d) Features of MAX17220 [52].

Taking into consideration the characteristics of both groups, commercially available DC-DC converters are not optimum to use with the printed TEGs from the HORATES project. While the first group is apt for the low voltage requirements, they lack efficiency and cannot work with high-resistance generators. Meanwhile, the cold-start voltage of the converters of the second group is usually unattainable in low-temperature conditions (Figure 1.9).

1.4 Startup Circuits

To get the best from these two converter groups, it is essential to address the main issue with the second group: the cold-start voltage. To this end, startup circuits are introduced. Circuits whose function is to start operating with very low voltages, and to have a high CR (voltage amplification), to reach a voltage level apt to start the operation of the main converter (Figure 1.10).

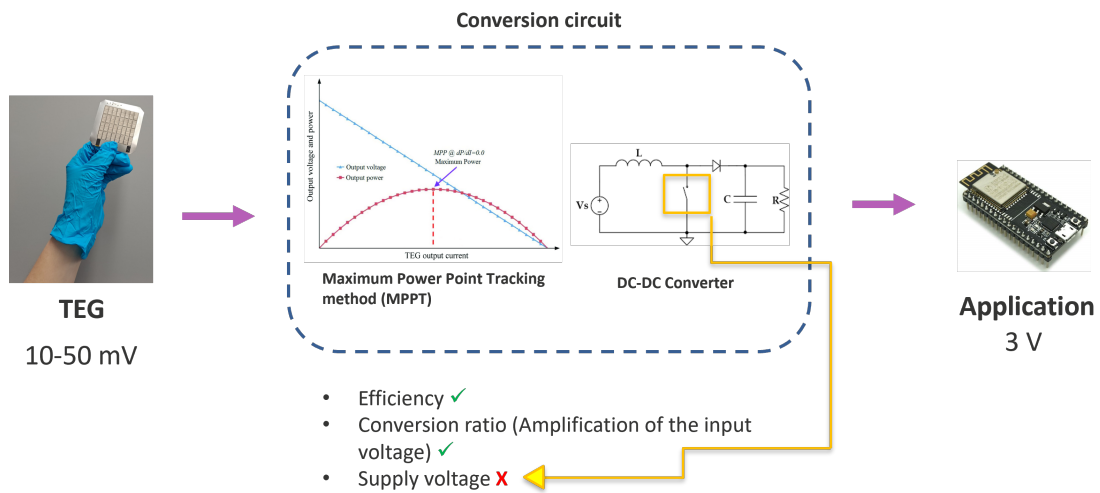


Fig. 1.9: Diagram of a converter in the second group.

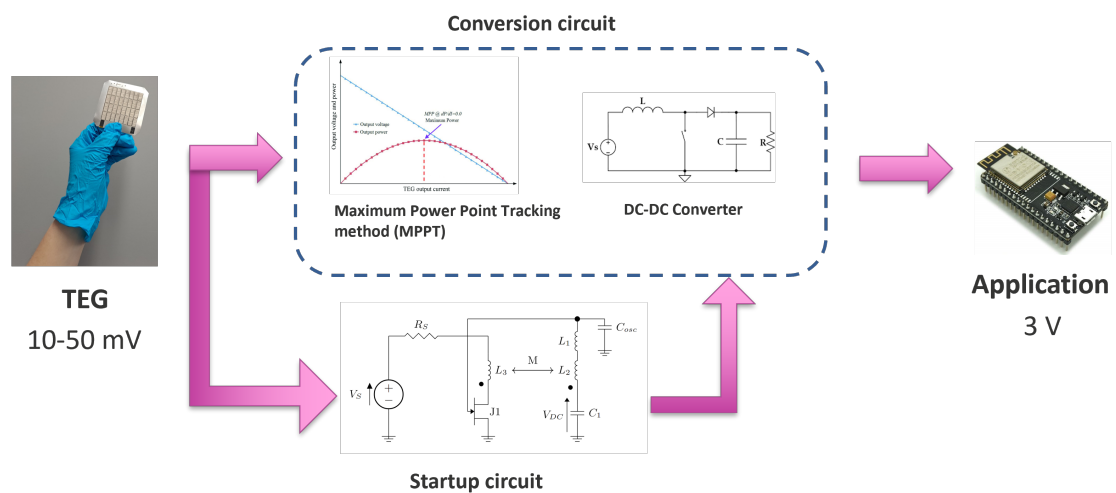


Fig. 1.10: Diagram of a converter in the second group, with the addition of a startup circuit.

While this topic is delved further upon in chapter 3, is worth mentioning that the preferred type of startup circuits when working with discrete circuits seems to be mainly self-powered oscillators, with normally-on transistors as their switching element [53, 17, 54, 55, 16].

A self-powered oscillator is an oscillator circuit that powers itself from the input voltage, without the need of an external supply voltage. The positive feedback of oscillator topologies allows for high levels of voltage amplification, while the use of normally-on transistors (transistors that conduct current when the control voltage is near zero) permits the operation with low voltages. Part of the work presented in this thesis consists of a novel self-powered oscillator topology, seen in Figure 1.11.

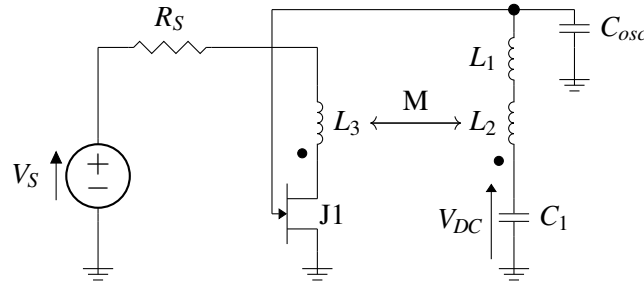


Fig. 1.11: New oscillator topology developed for this thesis.

It is worth noticing in the block diagram of Figure 1.10 that the startup circuit is not in series with the DC-DC converter, as the reader might expect if it is assumed that the startup circuit is used to reach the cold-start (input) voltage of the converter. In such a situation, the system or end-to-end efficiency, η_{ee} , would be equal to the product of the efficiency of the startup circuit and the efficiency of the DC-DC converter. This lowers the system efficiency drastically, as startup circuits are fundamentally similar to converters of the first group, and thus, have low efficiency.

Hence, startup circuits are normally used to charge a capacitor, which is later used to supply power to the main converter. Ideally, after the initial stage, the startup circuit should be disabled to avoid extra power consumption.

When the design is made with COTS DC-DC converters, the startup circuit cannot work in this way, since these converters are supplied directly by the input voltage, and thus, do not have a way to isolate supply voltage and input voltage. Some designs, such as the work

of Xia et al. [56], circumvent this limitation through the use of Single Pole Double Throw (SPDT) switches, as can be appreciated in Figure 1.12.

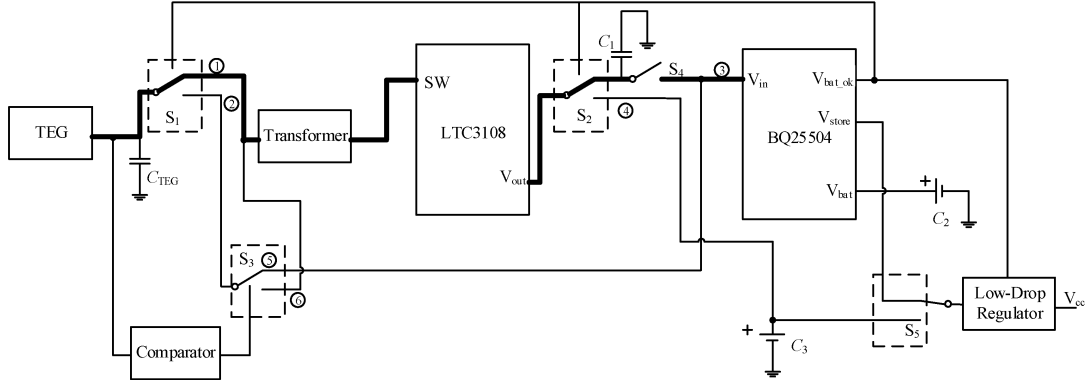


Fig. 1.12: Diagram of a harvester done with commercial DC-DC converters. LTC3108 acts as a startup stage for the BQ25504. Source: [56].

In this case, during the startup stage, the LTC3108 is in charge of boosting the voltage, until a capacitor is charged to the desired voltage. This capacitor is then connected to the input of the main converter, a BQ25504, to surpass the cold-start voltage and enter the normal working regime. Lastly, the input voltage is redirected to only pass through the main converter, essentially shutting down the startup circuit.

The drawback of this approach is that the working voltage of the main converter ($> 130mV$) might still be unreachable for the TEGs used in this project, so the circuit is stuck working only with the LTC3108.

Hence, the work done in this thesis is focused on the design and development of a custom DC-DC converter (diagram block shown in Figure 1.13), tailored for low voltage operation and high efficiency, which can be coupled with a startup circuit without it interfering after the startup stage is completed.

In the next section, the last requirement for the circuits designed for this thesis is introduced.

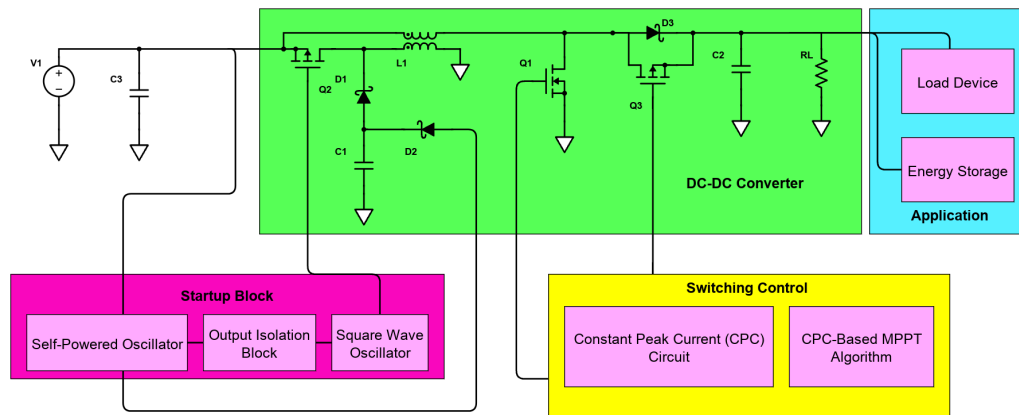


Fig. 1.13: Diagram of the DC-DC converter presented in this thesis.

1.5 Flexible Hybrid Electronics

As the HORATES project is focused on obtaining more sustainable and cheaper devices, utilizing organic materials for the fabrication of the generators instead of inorganic materials, it stands to reason that the design of the harvester has to be sustainable as well.

One way to improve in this aspect is to design the circuits utilizing flexible hybrid electronics. Hybrid electronics is the combination between conventional electronics (silicon-based for active components) and printed electronics. In this case, it encompasses:

- The use of thin, flexible substrates such as Polyethylene Terephthalate (PET).
- Traces deposited/added through printing methods. The traces of the circuit are conformed by conductive and dielectric inks.
- In this case, printed components are not used, just conventional components. These components are mounted over the substrate and connected to the traces by using an ECA.

This fabrication method is an additive process, as opposed to the conventional method for fabricating PCBs, where material is removed to obtain the final design. Since the traces of the circuit are not fabricated by removing material, but by adding them through the use of different printing techniques, these kinds of fabrication processes tend to waste less material,

reducing costs. Besides, since the TEGs used in this work are fabricated through printing methods as well, the use of printed hybrid electronics can facilitate the integration between the generator and the DC-DC converter circuit.

Another advantage, beneficial to this particular application, is that the substrate used can be a flexible and thin material, such as PET. This allows a certain degree of flexibility to the circuits, which can prove useful for circuits used in tight spaces or in wearable applications. While flexible hybrid electronics provide many advantages, they also have some drawbacks, whose impact is application-dependent. Figure 1.14 highlights some of the main advantages and disadvantages of fabricating circuits with flexible hybrid electronics instead of the conventional method (rigid PCBs in an FR4 substrate).

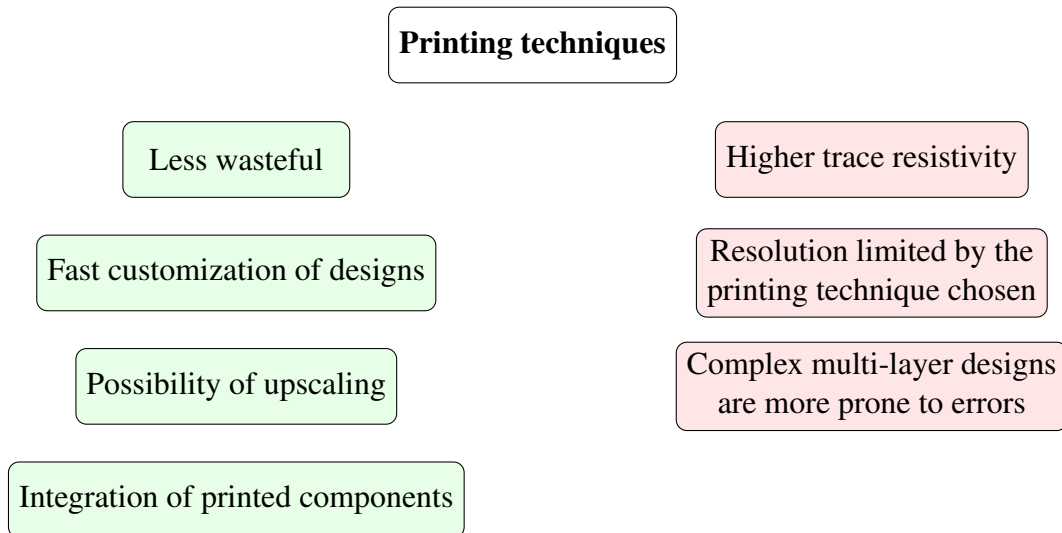


Fig. 1.14: Pros and cons of fabricating a circuit through the use of printing methods. Left: Pros. Right: Cons.

The drawbacks that particularly affect this application are the extra resistivity in traces, since they increase the power losses in a system where the input power is extremely low. The other impactful drawback is the complexity or difficulty to fabricate complex multi-layer designs, since the PCB layout of a DC-DC converter is one of the critical aspects affecting its performance.

In this thesis, a prototype of an energy harvester using a commercial DC-DC converter and designed with flexible hybrid electronics was created and characterized to evaluate the feasibility of this fabrication method for this particular application.

In the following section, the work presented in this thesis is summarized to provide guidance on the various topics discussed.

1.6 Outline of the Work Done - Thesis Organization

The work done by the author of this thesis in the project HORATES consisted of:

1. Design and development of an energy harvester with COTS components, which means commercially available components that are used without modifications. The DC-DC converter used for this device is a commercial converter, the LTC3108. Furthermore, the energy harvester was fabricated over a flexible PET substrate, to demonstrate the feasibility of a harvester circuit in a flexible hybrid electronics application. The results of this work are further elaborated in chapter 2.
2. Design and development of a new self-powered oscillator topology, to work as startup circuit of the newly designed DC-DC converter. The new topology equations are derived, and simulations are presented along with the characterization of a prototype. Furthermore, the oscillator circuit is used to start up a rudimentary boost converter, an early version of the DC-DC converter which resulted from this work. All the content related to the new self-powered oscillator topology is presented in chapter 3.
3. Design and development of a DC-DC converter adapted to work with low-voltage generators, with the self-powered oscillator circuit presented in chapter 3 working as a startup stage which can be shut down after the initial stage. The DC-DC converter implements an MPPT method from literature, originally used in Very Large Scale of Integration (VLSI) circuits but adapted to work in an embedded device. The topology itself is a modification of a boost converter, with added magnetic coupling to complete the startup loop. The DC-DC converter along with the startup circuit are presented in chapter 4.

The chapters follow a logical progression, starting by testing the feasibility of flexible hybrid electronics for thermoelectric energy harvesting by fabricating a harvester circuit with commercial components. The next chapter is dedicated to the start of the development

of a custom DC-DC converter, introducing the creation of a new topology of self-powered oscillator to use as startup circuit. Lastly, the work culminates with the design of a DC-DC converter topology capable of being started by this self-powered oscillator, and the harvester circuit composed by both circuits working together.

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Chapter 2

Flexible Hybrid Electronics

2.1 Introduction

As it was stated in the introduction, Flexible Hybrid Electronics (FHE) are a combination of conventional electronic components (or silicon-based Integrated Circuits (ICs)) with printed electronics, to combine their advantages. Silicon ICs provide performance in computation and signal conditioning, while printed electronics provide flexible and or stretchable substrates and components, with the capability of manufacturing cheap and large-area electronics due to the different printing techniques that can be used, such as screen printing [1], which is the technique used for the circuits in this work [2]. It is also important to note that being an additive fabrication process, printed electronics is more sustainable than the conventional subtractive process. The advantages of printed electronics are summarized in Figure 2.1.

To better understand printed electronics, a summary of commonly used printing techniques, along with their advantages and disadvantages is illustrated. These techniques are:

- Screen printing, which works by pushing inks through a mesh screen onto a substrate, is widely used for printing circuit patterns. Its fast printing speed and ability to print multiple circuits on a single substrate sheet make it suitable for mass production, as it is both efficient and cost-effective. However, its resolution is limited by the screen used,

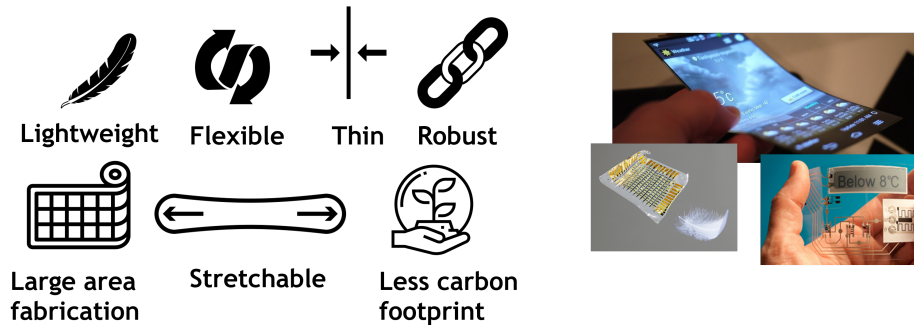


Fig. 2.1: Key advantages of printed and flexible hybrid circuits circuits.

making it less ideal for high-resolution applications. So far in this work, the thinnest traces achieved have been approximately $150\ \mu\text{m}$. Figure 2.2 exhibits a diagram of screen printing, where all its components can be observed. The setup is composed by a frame containing a screen, which has embedded the pattern in its hollow sections (unmasked sections of the screen, as the screen is covered with a photoresist mask, a light sensitive material which can be removed through UV application and post-processing). The ink is deposited over this screen, and it is pushed with a squeegee, passing through the sections of the screen with the engraved pattern, and reaching the substrate.

- Inkjet printing, which uses droplets of ink ejected from a nozzle to create patterns on substrates, and opposite to screen printing, it is capable of printing fine details and complex patterns, although its speed and area are much lower, so it is mostly recommended for prototypes or low-scale productions. Another disadvantage is that the ink formulation must be optimized to be deposited through inkjet printing, as the nozzle might clog. This technique also is compatible with a wide range of materials, including conductive, dielectric, and organic inks, which makes it interesting for bio-compatible applications [3]. The diagram in Figure 2.3 shows a schematic of the inkjet printing technology.

While there are many more printing techniques, these are two of the most commonly used, and serve as introduction for the content in this chapter.

Although in this work they are not used, another advantage already mentioned from printed electronics are printed components. Examples of these type of components that are frequently used in energy harvesting applications are batteries [5], supercapacitors [6, 7] and antennas

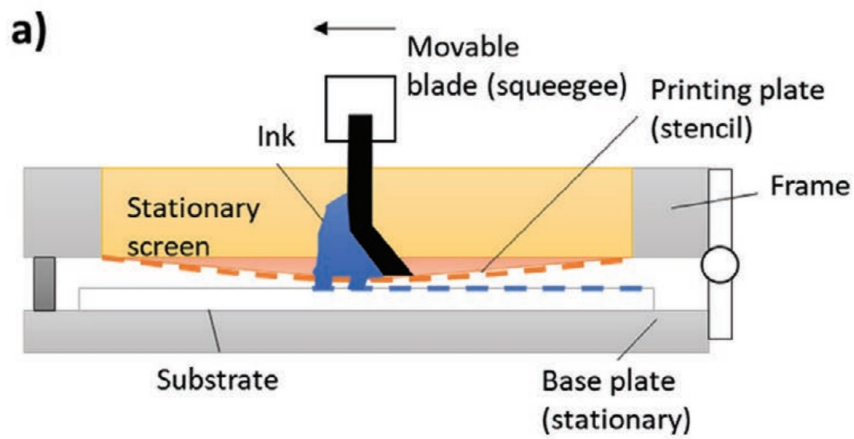


Fig. 2.2: Screen printing diagram. Source: [1].

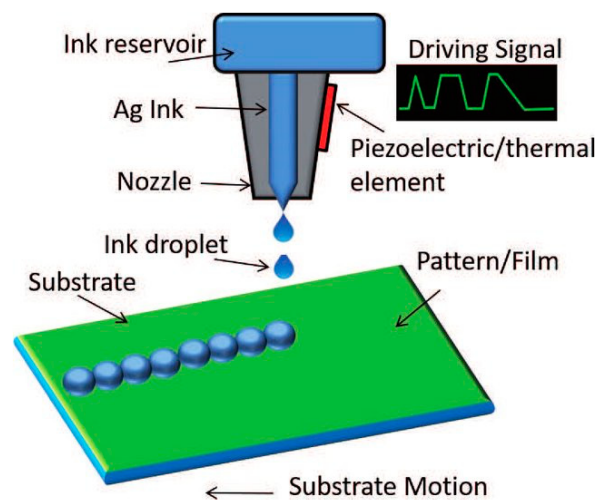


Fig. 2.3: Inkjet printing diagram. Source: [4].

[8]. Some of the current printed supercapacitors and batteries present in literature are shown in Figure 2.4, along with the conventional supercapacitors used in this work. These type of printed components prove useful when flexibility, stretchability or thinness are needed, as conventional supercapacitors are bulky.

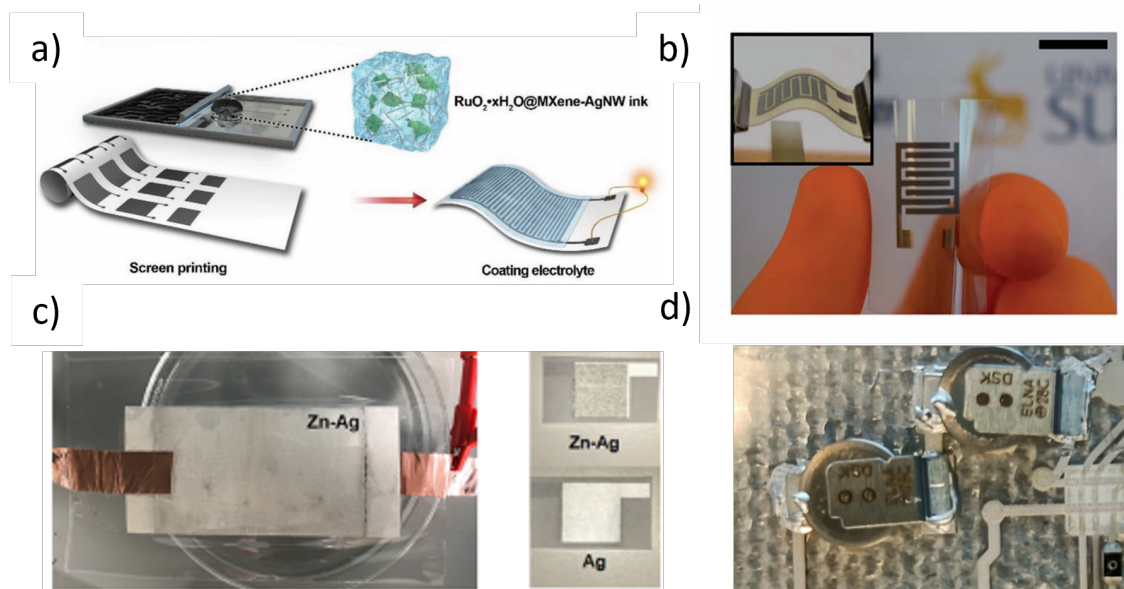


Fig. 2.4: Printed and conventional storage components. a) Screen-printed supercapacitor [7], b) Ink-jet printed supercapacitor [6], c) Paper battery with screen-printed electrodes [5], d) Conventional supercapacitors used in this work, connected to the substrate with Electrically Conductive Adhesive (ECA).

In this work, besides printed electronics, other types of fabrication for circuits over flexible substrates were used, such as the use of copper-clad polyimide substrates, which can be revealed through chemical etching to create circuit designs, as shown in Figure 2.5. The process is the same as with conventional Printed Circuit Boards (PCBs).

In the next section, energy harvesters designed and fabricated with Commercial Off-the-Shelf (COTS) components are presented. The first of them is fabricated over a copper-clad polyimide substrate, while the second one is fabricated in a traditional Flame Retardant Laminate 4 (FR-4) PCB. Lastly, the third one is fabricated using screen-printing over a flexible Polyethylene Terephthalate (PET) substrate, with conductive silver ink and dielectric inks to form the traces or interconnects.



Fig. 2.5: Stages of a PCB being chemically etched to form a circuit pattern. Source: [9].

2.2 Flexible Energy Harvester Circuit - Copper-Clad Polyimide (Horates V2.1)

Aiming to prepare an integrated flexible atmospheric monitoring circuit tag for Internet of Things (IoT) applications, a Thermoelectric Generator (TEG) powered circuit was designed and prepared Figure 2.6 to work as a standalone autonomous device with an atmospheric sensor (BME280 [10]) that includes three sensors: relative humidity, atmospheric pressure and temperature. This circuit will be called Horates V2.1, and this naming convention will be applied to every remarkable circuit from now on, following the "Horates VChapter.Circuit number" format. Furthermore, the circuit names will be added to the glossary along with a brief description for easier referencing during the reading process. It was fabricated over a copper-clad polyimide substrate, using COTS components. It was powered by a commercial TEG [11], and used a commercial atmospheric sensor (BME280 [10]). The circuit was designed to supply power to and read data from said sensor and store the values read in an Electrically Erasable Programmable Read-Only Memory (EEPROM). It was fabricated over a copper-clad polyimide substrate as a compromise between the ability of testing and reworking the board, while having the substrate flexibility and layout restrictions characteristic of a printed design. This last characteristic allowed it to serve as the base for future printed designs.

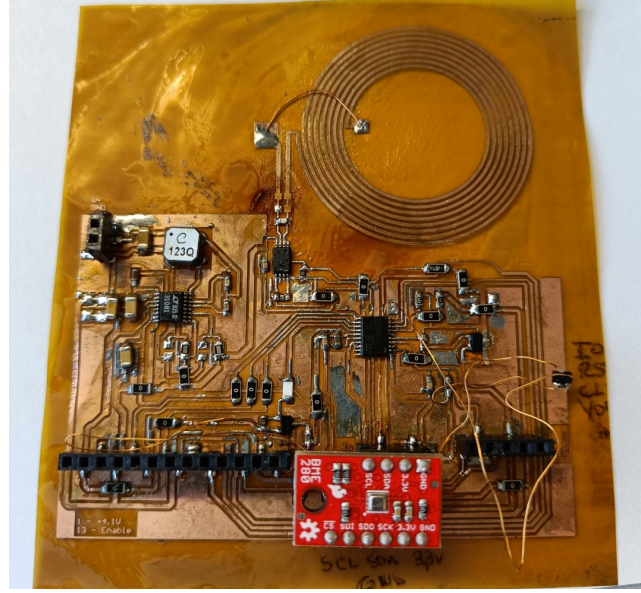


Fig. 2.6: Horates V2.1 flexible atmospheric sensing circuit.

The circuit consists of said sensor, an LTC3108 as the boost converter of the power stage [12], an STM32L031 microcontroller [13], and an ST25DV64K Near Field Communication (NFC) tag IC [14]. The NFC IC has an integrated EEPROM to store data, as well as the capability to harvest energy from NFC and output it through a pin called V_{EH} . The microcontroller can communicate with both the sensor and the NFC tag using Inter-Integrated Circuit (I^2C) communication. The circuit periodically measures the values from the sensor when there is available energy, and then stores the data in the EEPROM of the NFC tag, to be read later when a NFC reader is used. A simple block diagram illustrating how the circuit is organized is shown in Figure 2.7.

The circuit power stage, shown in Figure 2.8 was based on the previously mentioned LTC3108 boost converter [12]. This converter has three outputs, V_{OUT} , V_{OUT2} and V_{LDO} . During startup, the different outputs start in a sequence, with V_{AUX} being the first to charge, as exhibited in Figure 2.9.

For this design, the V_{LDO} output was used to power the whole circuit, since it is prepared for low-power microcontrollers or similar circuits, with an output voltage of 2.2V. This output consists of a low-dropout linear regulator (hence the name of the output) powered by the highest between V_{AUX} or V_{OUT} . V_{AUX} is internally limited to 5.25V, while V_{OUT} is configured to be regulated at 4.1V. This means that most of the time, the LDO output

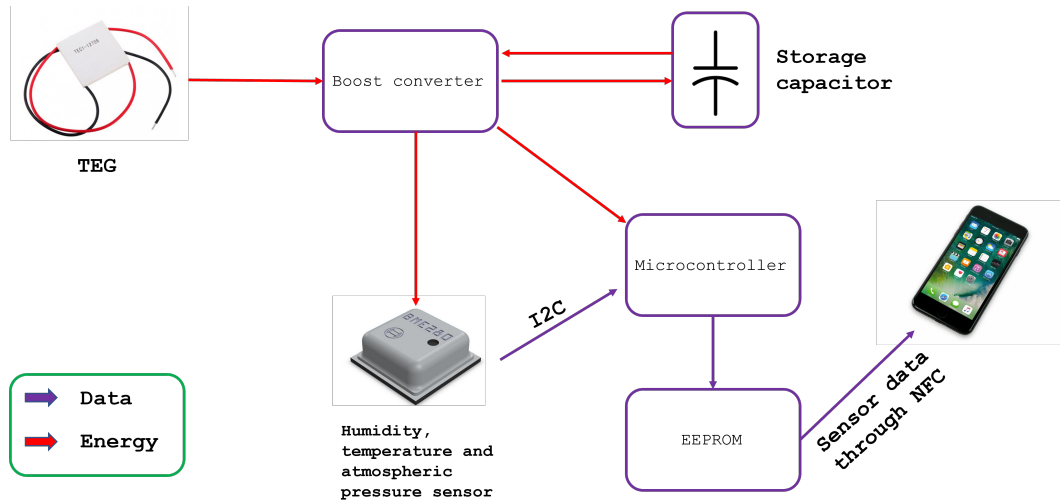


Fig. 2.7: Block diagram of the circuit.

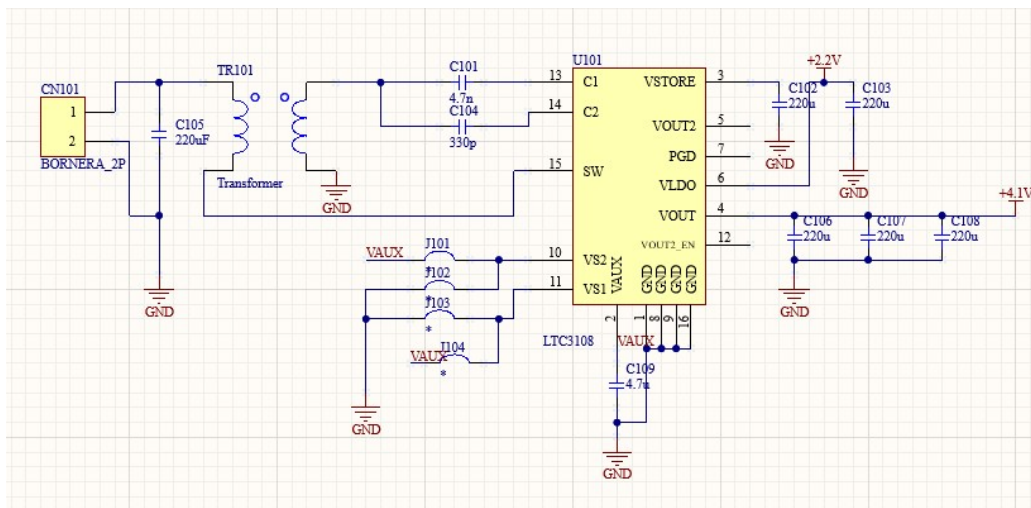


Fig. 2.8: Power stage of the flexible atmospheric sensing circuit.

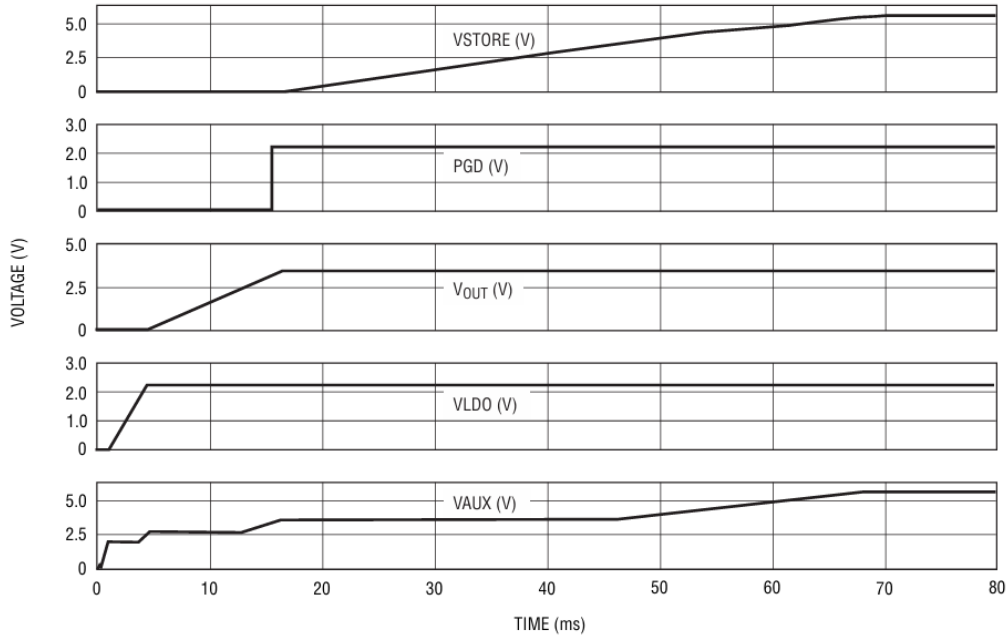


Fig. 2.9: Startup output sequencing. Source: [12].

is powered by V_{AUX} (except the times when V_{AUX} drops below V_{OUT} . Since this output consists of a linear regulator, the efficiency of the conversion, from V_{AUX} to V_{LDO} is equal to $\eta = 100 * V_{LDO}/V_{AUX} = 41.9\%$. As such, for the next designs, V_{LDO} should be reserved only for ultra-low power circuits.

The datasheet recommends connecting V_{OUT} to a storage capacitor or rechargeable battery, to store energy and supply it to the output (V_{LDO}) during bursts of current from the load. Hence, the V_{OUT} output is used as an energy reservoir.

The circuit was tested using the setup shown in Figure 2.10, consisting of a commercial TEG [11] mounted over a hotplate and coupled with a heatsink, connected to the input of the circuit.

In these conditions, the circuit started operating when the TEG presented a $\Delta T \approx 50^\circ\text{C}$ (considering ambient temperature equal to 25°C). The circuit was also tested using a voltage power source for reproducibility, and the startup input voltage was 150mV while the current was 35mA , with a quiescent current (after the output of the LTC3108) of $35\text{ }\mu\text{A}$. After startup, the circuit kept working with an input voltage of 120mV and an input current of 16mA .

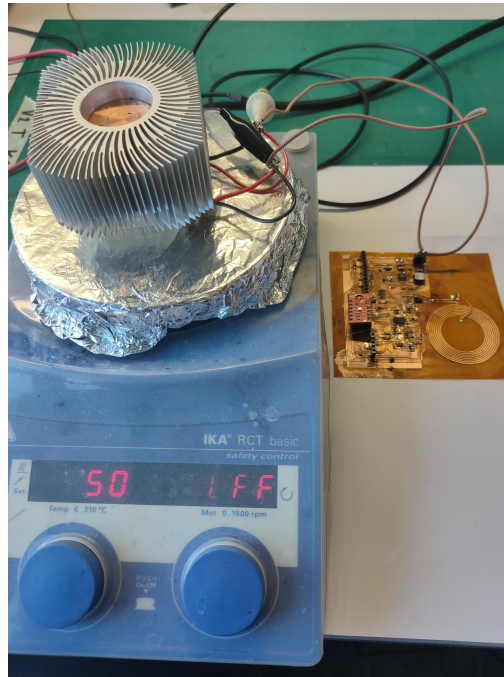


Fig. 2.10: Setup for the circuit. Commercial TEG [11] over a hotplate and coupled with heatsink.

Regarding the NFC interface, readings with a mobile phone could be done from a distance of 4-5 cm (Figure 2.11).

Lastly, a demonstrator, shown in Figure 2.12, was built to present the circuit at the Smart City Expo 2023 [15].

As might be noted by the reader, the startup voltage and current values are high when compared to the values presented in chapter 1. The circuit should have much lower startup values, so a list of the possible causes, with the last one being the main factor, is provided next:

- Incorrect power gating of the NFC IC causing extra power consumption [16]. As seen in Figure 2.13, the IC has an N-channel MOSFET connected between ground and the VSS pin.
- The circuit is constantly powered, even before reaching the desired voltage on the output (V_{LDO} at 2.2V). As learnt after this circuit, when the microcontroller is powered by a supply raising with a low slew rate, the current consumption rises when the voltage



Fig. 2.11: NFC Reading of the sensing circuit.

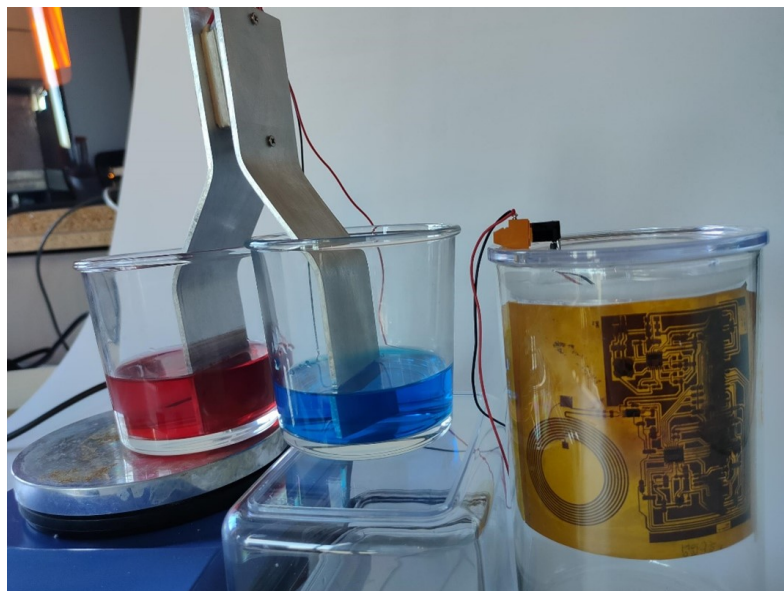


Fig. 2.12: Demonstrator working during Smart City Expo 2023.

is near the minimum supply voltage, as the internal circuits are in an undefined state. With the LTC3108, the PGD output (Power Good) can be used to enable the output once V_{OUT} reaches regulation. This is implemented in the next designs.

- The previously mentioned issue with powering the circuit through the Low Dropout Output (LDO), as the already low efficiency of the boost converter is multiplied by the conversion efficiency between V_{AUX} and V_{LDO} .

These causes are considered and fixed in the next iteration of the circuit, resulting in a reduction of startup power as expected. This next iteration is presented in the following section.

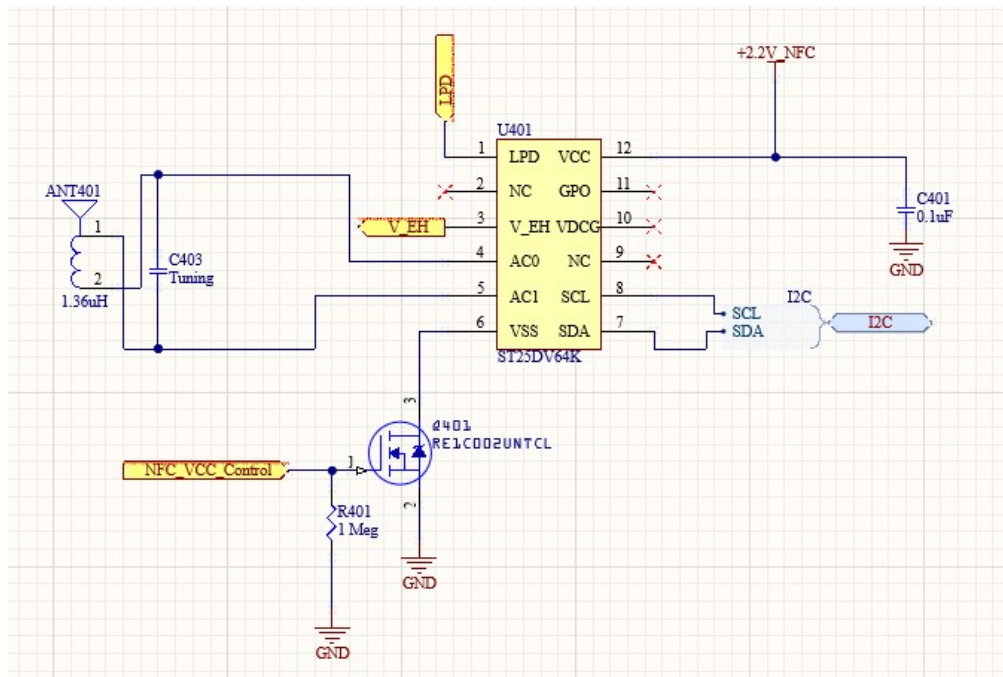


Fig. 2.13: NFC IC with incorrect power gating.

2.3 Rigid Energy Harvester Circuit (Horates V2.2)

and the strategy to validate the contingency strategy is preparing the device in conventional FR4 to avoid the limitations present in the flexible circuit, namely the tracks resistance and the limitation to make layers.

The next iteration of the circuit, denominated Horates V2.2, was made over a rigid substrate (FR-4) as a contingency strategy, to avoid limitations present in flexible circuits, such as the number of layers limitation, and for easier reworking of the circuit. The changes when compared with the previous iteration are presented next, with the two first items being the main changes, directed to solve the issues mentioned previously.

1. The LDO is not used anymore. The circuit is powered through V_{OUT} , while the surplus energy is stored in the supercapacitors connected to V_{STOR} .
2. A ultra-low-power linear regulator is connected in series between V_{OUT} and the rest of the circuit. Since the regulator counts with an EN pin (enable pin), it isolates the circuit until V_{OUT} reaches regulation. The PGD output of the LTC3108 is used to enable the regulator once this condition has been met. This modification helps reduce the power needed for startup, ensuring that the circuit is in a stable condition when V_{OUT} is enabled.
3. A supercapacitor was added to the V_{STOR} output to fulfill the function V_{OUT} was in charge before (working as an energy reservoir).
4. The energy harvesting feature of the NFC tag was enabled. This means that the circuit can recharge its supercapacitor when a reading is being done.
5. The NFC tag is not power-gated anymore. In this iteration, the LPD pin (Low Power Down) is utilized to put the tag in a low-consumption mode.

These changes are reflected in a new block diagram, shown in Figure 2.14.

The new power stage schematic is shown in Figure 2.15. When compared with the previous one, V_{OUT} in this case is programmed to be regulated at +2.3V. Furthermore, the linear regulator is placed in series with V_{OUT} , converting the +2.3V to +1.8V to power the whole circuit.

V_{STORE} now has two supercapacitors in series (to support the voltage in this pin, since it can go up to 5.25V), with 70 mF capacitance each one, for an effective capacitance of $\approx 35mF$. Besides, the energy harvesting output from the NFC tag is now connected through a Schottky

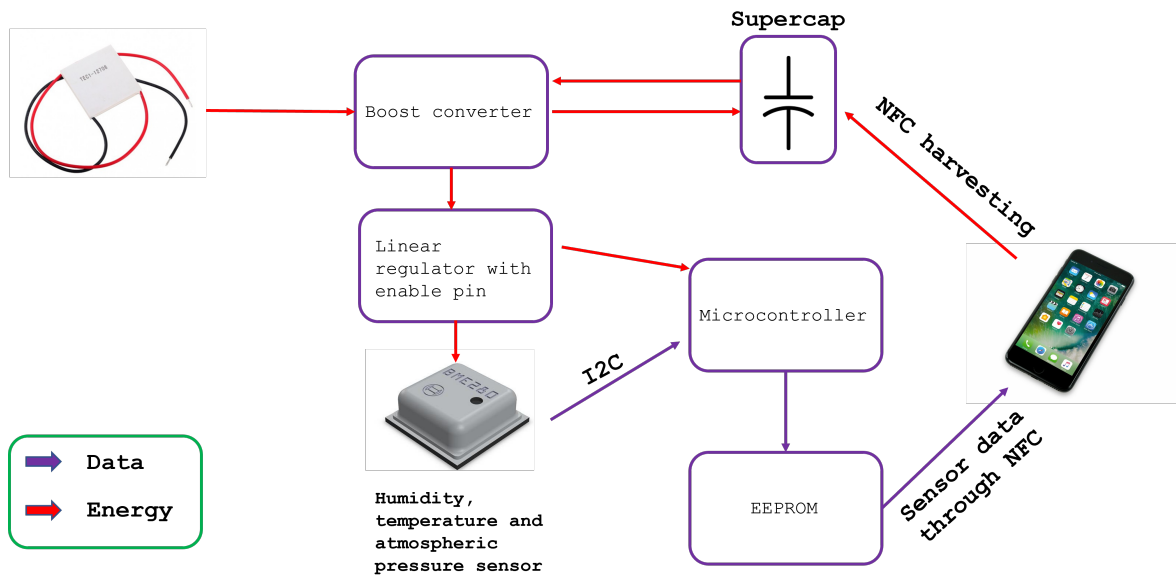


Fig. 2.14: Horates V2.2 block diagram.

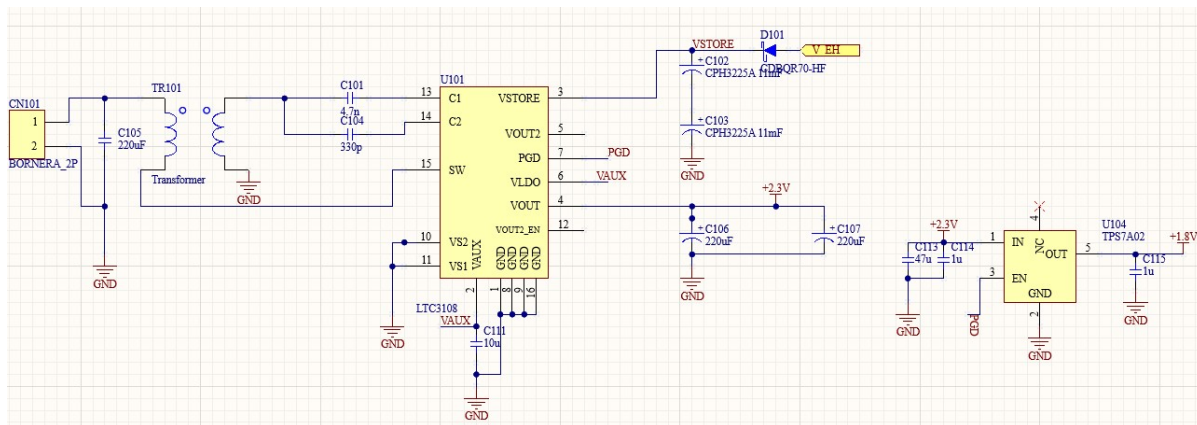


Fig. 2.15: Horates V2.2 power stage.

diode to V_{STORE} , to recharge the supercapacitors with every reading. The diode avoids charge leaking to the NFC tag.

The circuit was characterized using the setup displayed in Figure 2.16 and Figure 2.17. A commercial TEG TEC1-12706 coupled with a heatsink was placed upon a hot plate and connected to the input of the circuit. The voltage of the TEG and the supercapacitor was measured with an oscilloscope PicoScope 2000 Series, while an Agilent 34410A multimeter was used to measure the current consumed by the circuit (after the linear regulator).

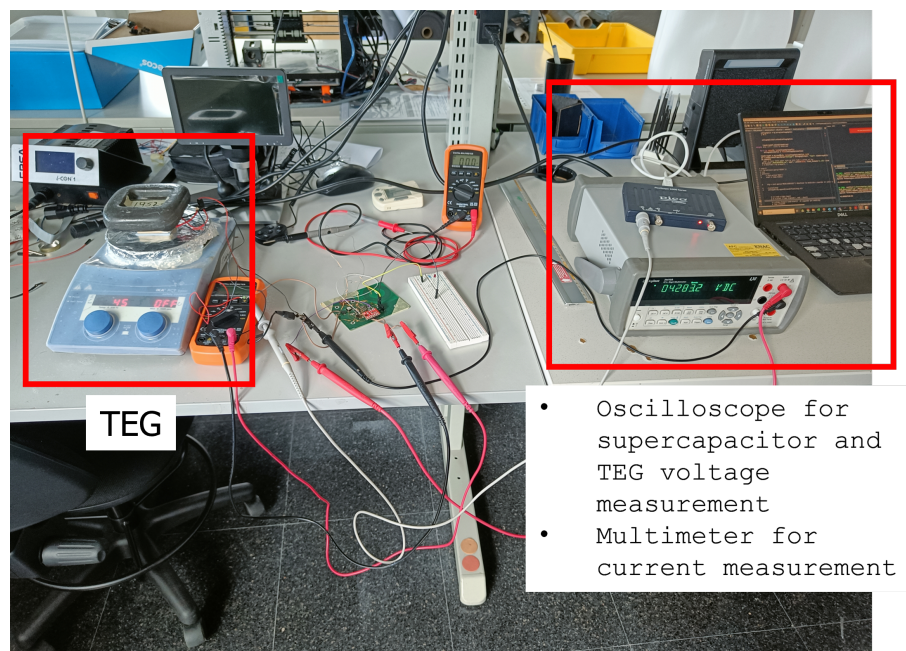


Fig. 2.16: Measurement setup for Horates V2.2 board.

These measurements are presented in Figure 2.18 in the following order, from top to bottom: circuit current, TEG voltage (input voltage of the circuit) and supercapacitor voltage.

The circuit in this case operates with an input voltage between $60mV$ and $75mV$, making sensor readings (and storing the data in the EEPROM) every one minute. At the twenty minutes mark, the TEG is disconnected, and the circuit keeps operating using only the energy previously stored in the supercapacitors. If the decay rate of the voltage is constant over time, then the circuit has approximately 3 hours of extra lifetime after the point it has been disconnected, considering that the supercapacitors stop powering the circuit when they reach $2.5V$ (horizontal red line).

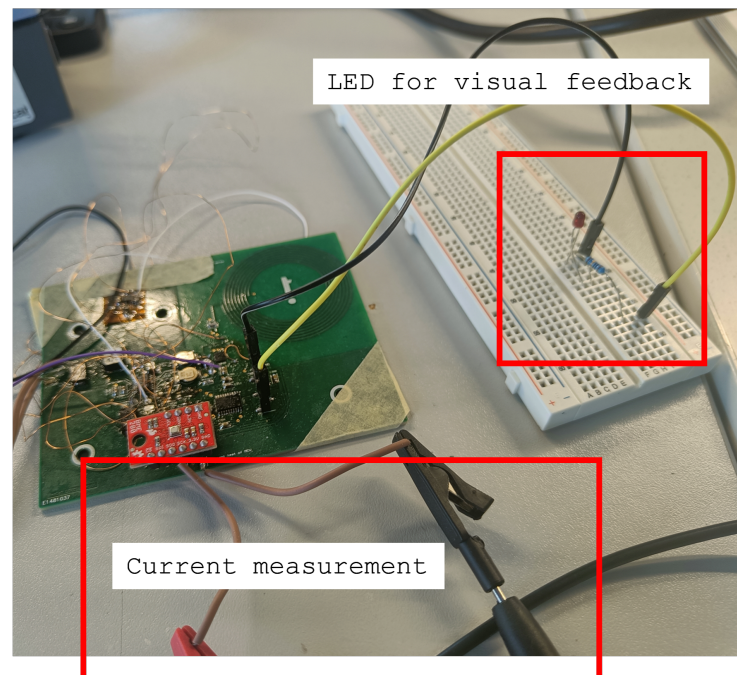


Fig. 2.17: Zoom in the current measurement part of the setup.

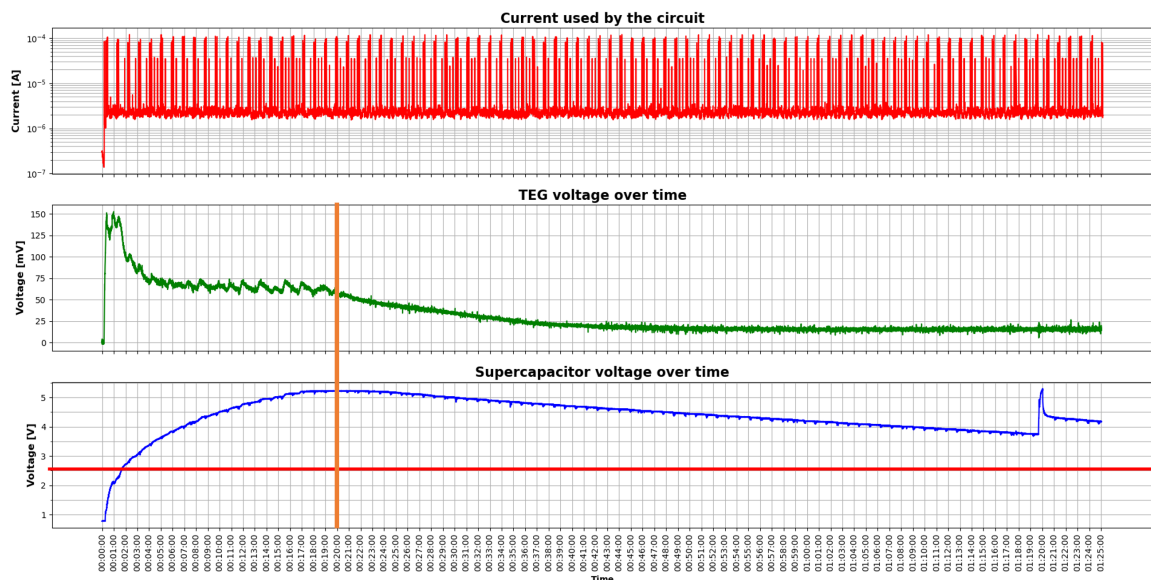


Fig. 2.18: Characterization of the circuit.

Observing the curve of the supercapacitor voltage at around 1 hour and 20 minutes (vertical orange line), the voltage peak is due to data being read through a mobile phone, consequently charging the supercapacitor.

Figure 2.19 shows a zoomed version of the current consumption of the circuit plot. During idle state, the current is around $2\mu A$, basically limited by the consumption of the microcontroller in low-power mode. During I^2C communication, there are current peaks of $100\mu A$. Since these type of measurements (temperature, humidity and ambient pressure) are usually done in periods greater than 20 minutes, the average current consumption can be maintained in a range below $10\mu A$. As an example, if the whole I^2C communication takes about 50 ms, and the measurements are done every 30 minutes, then the average current would be $I_{AVE} = (100\mu A * 50ms + 2\mu A * (30 * 60 * 1000ms - 50ms)) / (30 * 60 * 1000) \approx 2\mu A$, practically equal to the idle current.

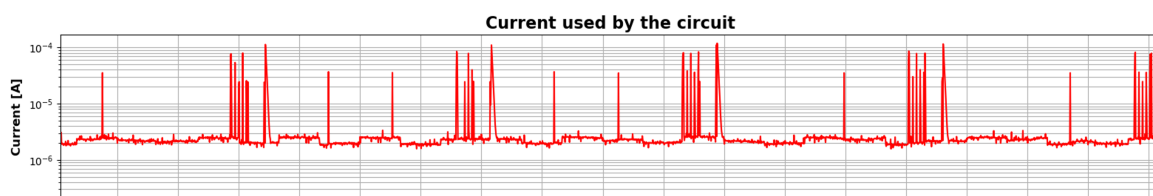


Fig. 2.19: Zoom in the current consumption of the circuit.

Lastly, the circuit was tested with a power supply at its input to measure startup voltage and current. The startup voltage is around $70mV$, while the startup current is around $7mA$, resulting in a startup power of $490\mu W$.

In the next section, the last iteration of the circuit is presented, where the substrate was changed for a PET substrate.

2.4 Flexible Energy Harvester Circuit - PET (Horates V2.3)

Opposite to the last two circuits presented, this iteration denominated Horates V2.3, was made by additive fabrication methods. It was made over a flexible PET substrate, using screen-printing to print the traces conforming the PCB. Furthermore, the atmospheric sensor is now integrated with the board instead of using an external breakout board.

The board has two conductive layers separated by a dielectric layer, all printed over a $125\text{ }\mu\text{m}$ thick PET substrate. Conductive silver ink from DuPont was used for the two conductive layers, and dielectric ink from the same provider for the dielectric layer. The traces were printed through screen-printing, using 120T screens for the first conductive layer, due to the use of thin traces, with a width lower than ($< 300\mu\text{m}$). For the printing process, the PET was pretreated in the oven at 120°C for 30 minutes, while each layer was screen-printed and then cured in the oven at 120°C for 15 minutes, except the last one which lasted 30 minutes at the same temperature. To mount the components, an ECA from EPO-TEK[®] was used. Said adhesive was cured in the oven at 80°C for 3 hours. As the last step, to secure the components, a structural adhesive from LOCTITE[®] was used, and was cured through the application of UV light.

The results of this circuit were presented at the LOPEC 2023 conference in an oral presentation [17].

The three screens used to print this circuit are shown in Figure 2.20, with the designs at the right corresponding to this circuit. Each screen is identified by a color, with the black traces corresponding to the bottom conductive layer, the green/lime ones corresponding to the dielectric layer, and the lavender traces corresponding to the top conductive layer. These screens featured cumulative improvements resulting from the experience gained in other designs, such as:

- Center portion of the screen dedicated to patterns for characterization of the printed traces. From top to bottom:
 - Pattern with footprint of 0Ω resistors to check the contact resistance, or how good is the electrical connection made by the ECA.
 - Pattern for sheet resistance measurement for the three different screens.
 - Pattern to measure thickness of traces with varying printing angles (0° , 45° , 90°) using a profilometer.
 - Pattern to measure thick of traces with varying printing angles and varying layer stack.
 - Left: Pattern to measure possible shorts between the bottom and top conductive layers, when there is dielectric in the middle. Right: Pattern to measure resistivity of tracks in both layers.

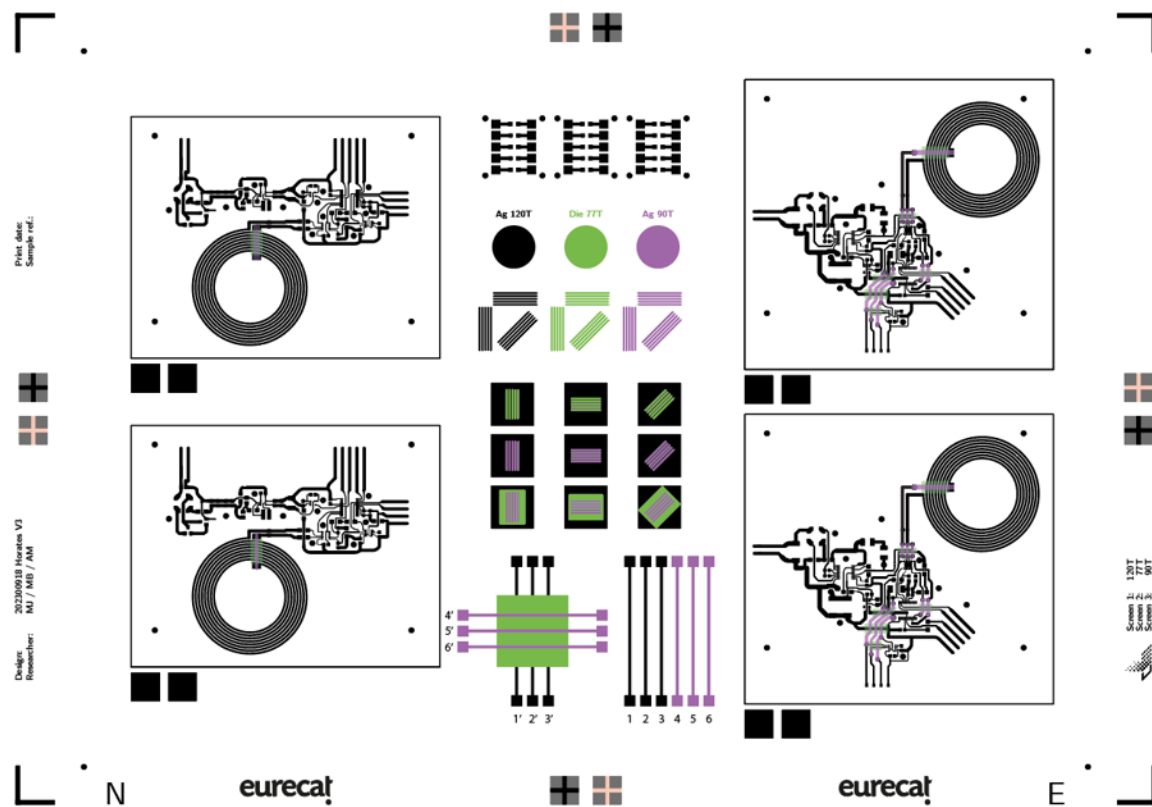


Fig. 2.20: Horates V2.3 Screens with characterization patterns.

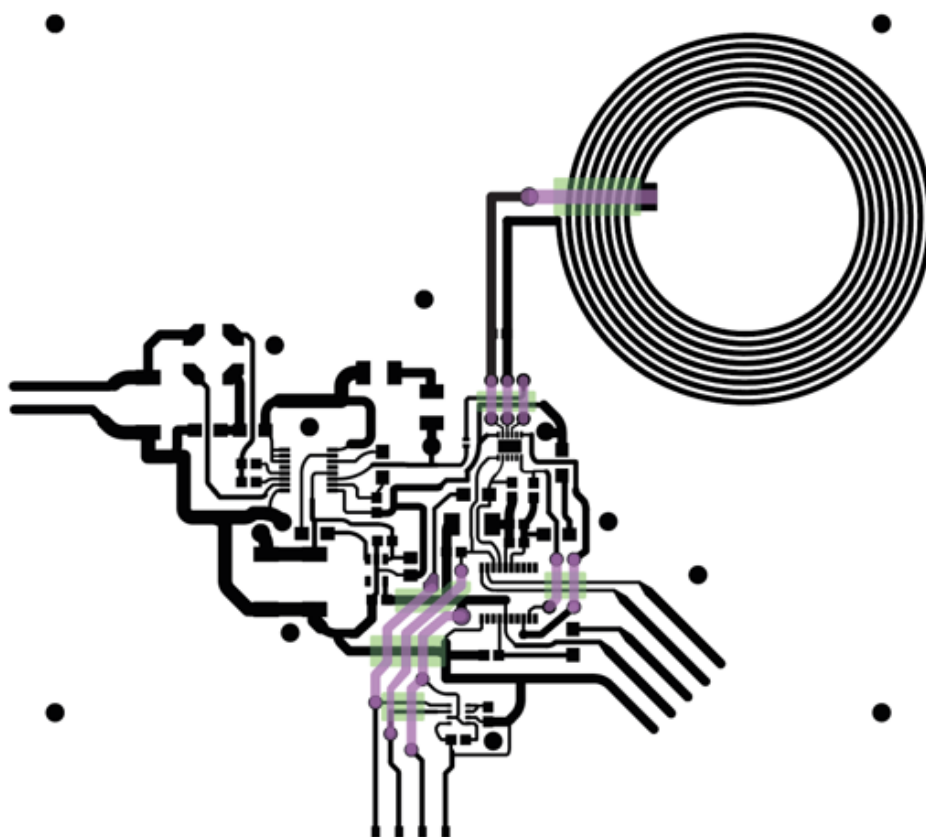


Fig. 2.21: Horates V2.3 design.

- Changed aligning marks to a square and cross format for easier manual alignment.
- Local fiducial marks in critical spots to reduce the effect of height differences along the substrate during the pick & place process. The fiducials are silver circles, refer to Figure 2.22.

These additions aim to provide a comprehensive understanding of the fabrication process and potential areas for improvement.

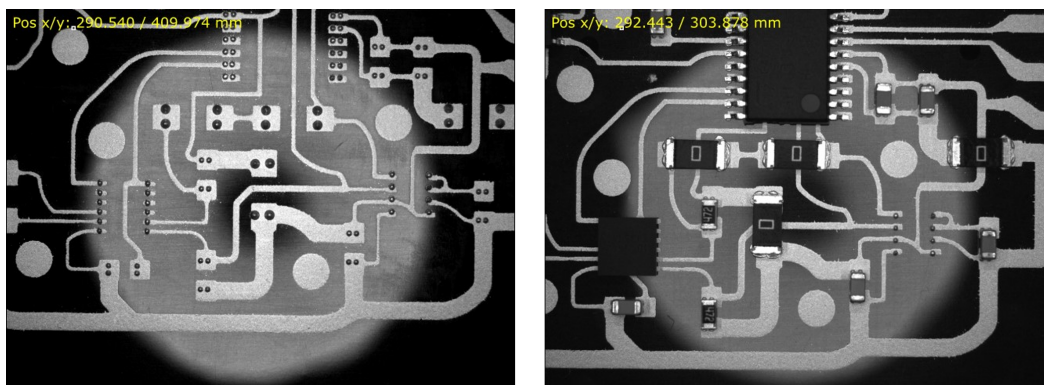


Fig. 2.22: Local fiducial marks for height calibration.

Figure 2.23 displays the final result of the printing and hybridizing process.

For this circuit, the characterization consisted on checking the startup values (current and voltage) using a power source as the input voltage generator, as can be checked in Figure 2.24. The startup voltage is equal to $50mV$, while the startup current is equal to $7mA$, equating to a startup power of $450\mu W$. Furthermore, the power consumed during steady state operation is equal to $360\mu W$.

Lastly, through the characterization patterns, a percentage of functional sheets (this is, sheets with circuits without any short-circuit) was calculated, based on the number of dielectric layers used (one layer or two layers) to insulate the conductive bottom layer from the conductive top layer. The results are exhibited in Figure 2.25. Note that the graph discriminates between UV and thermal. This is because batches of circuits with different inks (one curable using UV and the other one cured in the oven) were made, but no noticeable differences were observed except resistivity differences and the number of functional sheets.

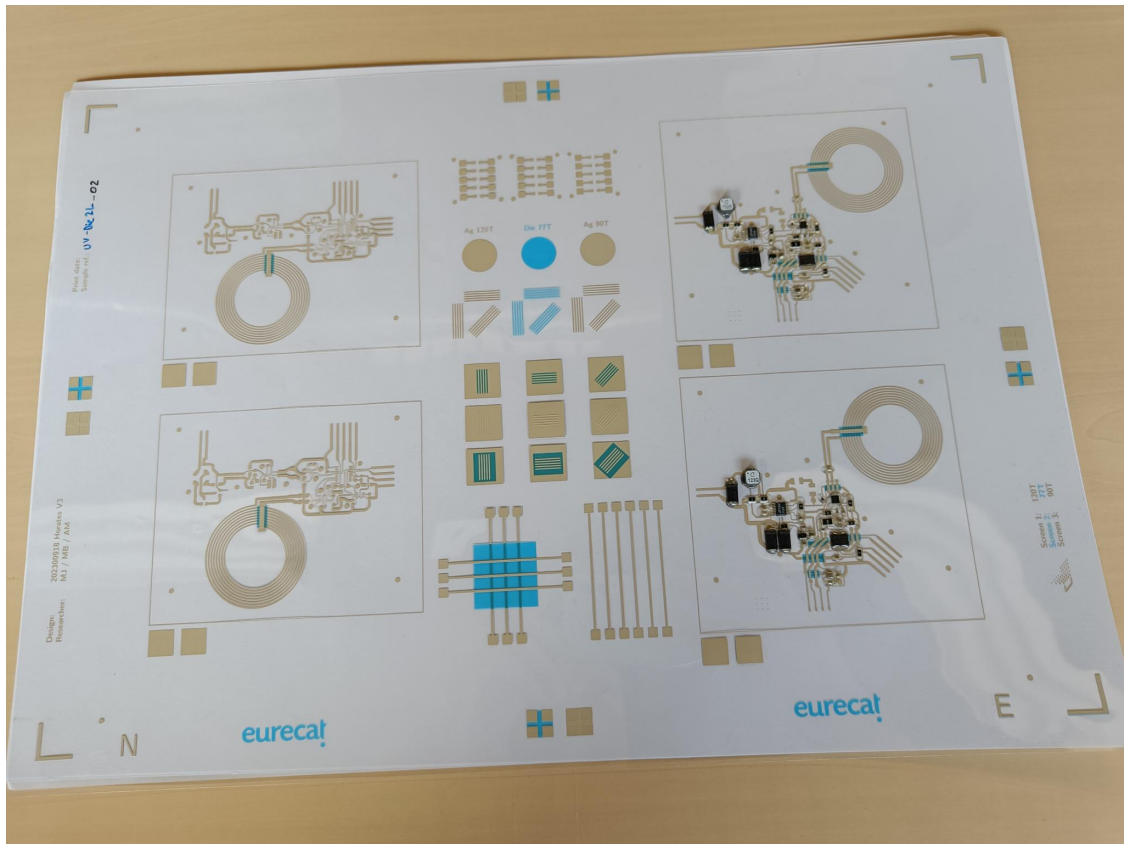


Fig. 2.23: Horates V2.3 screens with characterization patterns.

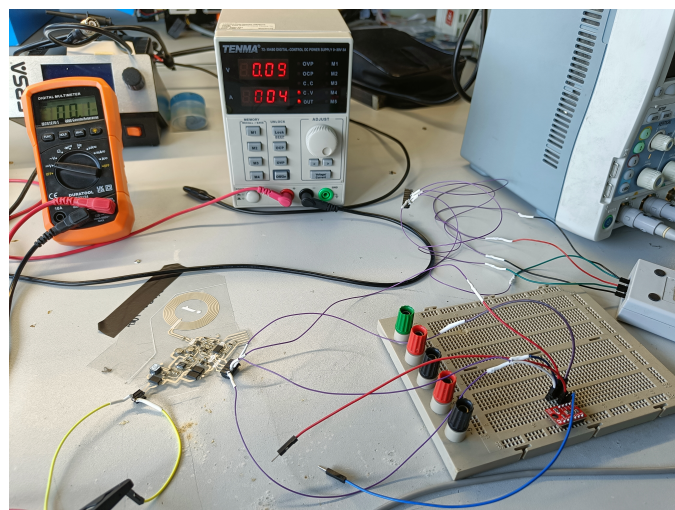


Fig. 2.24: Horates V2.3 setup.

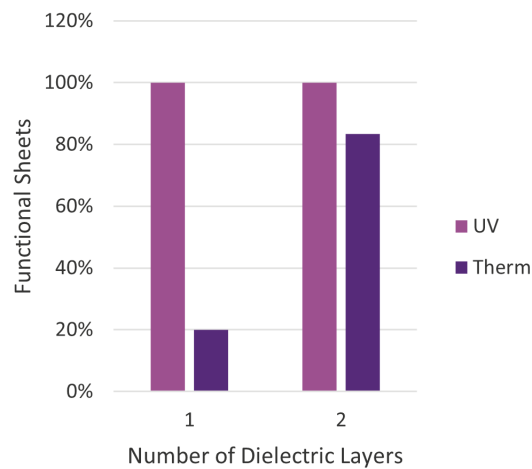


Fig. 2.25: Percentage of functional sheets (from a total of five sheets for each type of ink).

As a conclusion from this figure, when using this combination of inks, for the same process of fabrication (this is, without altering curing times or temperature/UV exposition), the batch of circuits with thermal inks benefits from using two layers of dielectric ink.

2.5 Chapter Conclusions

The feasibility of producing energy harvester circuits (Horates V2.1, Horates V2.2, and Horates V2.3) using flexible hybrid electronics was demonstrated, as a fully-functioning environmental sensing circuit was fabricated, with energy harvesting capabilities from TEGs or NFC. The importance of isolating the output of the boost converter from the rest of the circuit until the output is fully charged, in this case, using the "Power Good" output from the LTC3108, was first stressed in this chapter. In the next section, a new self-powered oscillator topology created in the framework of this thesis is presented. The circuit operation is described theoretically, along with simulations and an implementation of the circuit.

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Chapter 3

Startup Circuits for Low-Voltage DC-DC Converters

3.1 Introduction

As stated in chapter 1, the Commercial Off-the-Shelf (COTS) Direct Current - Direct Current (DC-DC) converters currently on the market can be separated into two groups. The motivation behind the design of a startup circuit for a DC-DC converter is to have the best of both groups. Through the use of an startup circuit, the DC-DC converter starts operating at lower voltages while keeping its high efficiency. In niche or small markets, such as printed thermoelectric energy harvesting, where investing in an Application-Specific Integrated Circuit (ASIC) for each Thermoelectric Generator (TEG) might be prohibitive, and the commercially-available DC-DC converters are not suitable for the application, one solution is to make a custom circuit. This circuit is made with easily available, COTS discrete components, and consists of a startup circuit and a DC-DC converter, controlled by a microcontroller. The startup stage is crucial to reduce the power demands on the generators, for example, allowing the circuit to work with TEGs with smaller areas.

When working with ultra-low-voltage generators, the startup circuit must comply with two requirements: the first, for the startup voltage to be lower than the output voltage of the generator, in the conditions the application is expected to operate. The second requirement

is to have a high conversion ratio, i.e., high voltage-amplifying capabilities, high enough to switch the transistors of the converter. Printed TEGs in low-temperature applications tend to have output voltages lower than 100 mV. As an example, one of the printed TEGs used in an article published in the framework of this thesis is presented in Figure 3.1, along with its output power and voltage plot for different ΔT .

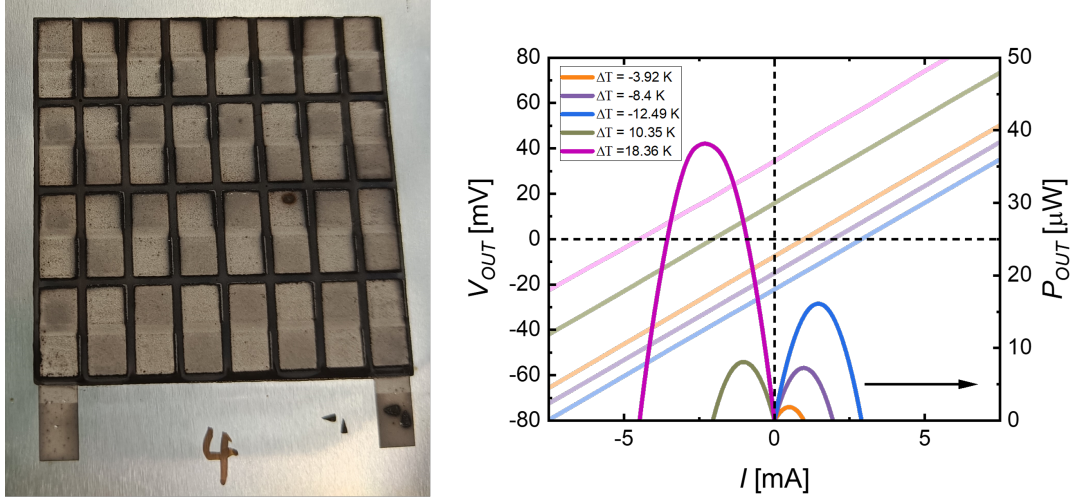


Fig. 3.1: Output voltage of a printed inorganic TEG. Source: [1].

Other desirable, although not crucial requirements, are for the startup circuit to have the capacity to be turned off after the startup stage, to avoid extra power consumption. The other one is to design the startup circuit to match the output impedance of the generator, if it is known beforehand. Meanwhile, the DC-DC converter, as mentioned previously, should be as efficient as possible, count with Maximum Power Point Tracking (MPPT) methods to extract the maximum possible power from the generator, and have output voltage regulation, as well as the possibility of having a battery/super-capacitor for energy storage.

3.1.1 Startup alternatives - State of the Art

There are many alternatives available in the literature to start up a DC-DC converter. Some of these alternatives are described next.

1. Using a precharged battery or super-capacitor, which is not practical, and might stop working if the battery cannot be recharged over a long time.

2. Using switches activated by motion [2], when talking about wearable devices, allows using external energy (movement, in this case) to generate the switching of the DC-DC converter, and consequently extract energy from the TEG.
3. Start the circuit with the aid of external energy sources to generate a high-enough voltage during startup. Transducers such as photovoltaic cells can be used in a thermoelectric energy harvester, or RF sources, among others [3].
4. Startup circuits based in the voltage boosting techniques mentioned in chapter 1, same as the DC-DC converters.

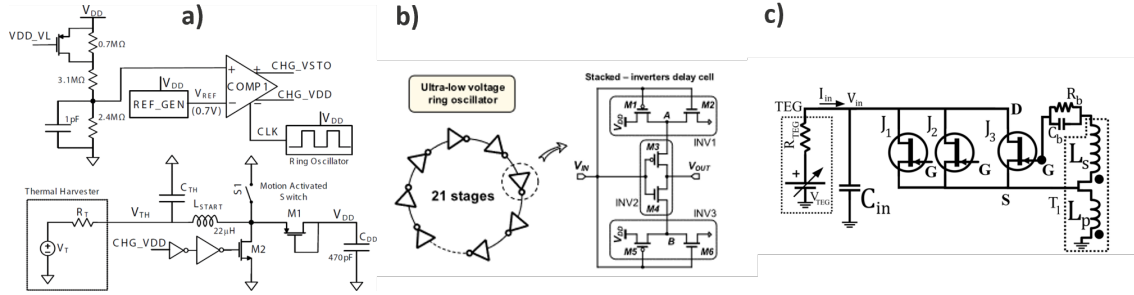


Fig. 3.2: Alternatives to cold-start a circuit. Sources: a) [2] © 2010 IEEE, b) [4] © 2019 IEEE, c) [5] © 2024 IEEE.

In the upcoming sections, an analysis of the state of the art regarding startup circuits is presented. This analysis will emphasize item 4 of the mentioned alternatives and will categorize the circuits into two groups: those made with Very Large Scale of Integration (VLSI) and those made entirely with discrete components, to differentiate advantages and disadvantages provided by both methods.

Startup circuits in VLSI

When working at the VLSI scale, such as in CMOS processes, there is a wider variety of possible startup circuits for multiple reasons, such as:

- The ability to cascade multiple stages of amplification, which is not always possible when using discrete components, and it is impossible in a considerable or useful scale.

- Greater variety of circuits available due to less strict power limitations resulting from the lower power consumption of Integrated Circuits (ICs) compared to discrete circuits.
- Lower voltage requirements for circuits in general to start operating.
- The use of specific analog, digital or mixed-signal circuits is difficult or impossible to implement with discrete components.

One of these available circuits is the ultra-low-voltage ring oscillator, which can be used as a startup clock. Bose et al. present a circuit using an ultra-low voltage ring oscillator, composed of 21 stages (cascaded individual cells). This oscillator acts as the clock of the startup voltage multiplier block of the circuit, consisting of cross-coupled complementary charge pumps. The resulting boost converter starts operating with an input voltage of 57 mV [6].

Coustans et al. (Figure 3.3 a)) also use a charge pump driven by ring oscillators (denominated as self-oscillating charge pump). The accumulated voltage of this charge pump supplies power to a pulse generator, whose control signal is derived from the amplified ring oscillator signal. This arrangement allows a boost converter to start operating with an input voltage of 60mV [7].

Lastly, Liu et al. (Figure 3.3 b)) exhibit a circuit whose startup stage is composed of a boost converter parallel to the main one. The block in charge of switching this low-side transistor is comprised of a low-voltage ring oscillator, a V_{out} detector, and two CLK bootstraps (a bootstrap is a circuit used to exceed the supply voltage [8]). This startup circuit is powered by V_{out} , which at the start is charged directly through the diode, and later is charged by this startup block. This converter starts working with an startup voltage of 260mV [9].

Moreover, transistors in VLSI processes have lower V_{TH} and capacitance, which makes it easier to switch them with low voltages, while also maintaining very low power consumption due to possibilities like driving them in sub-threshold regime [13].

Works such as the one from Teh et al. (Figure 3.3 c)) present a self-started boost converter where the voltage regulation is determined by the I_{DSat} of a MOSFET [10]. This parameter can be defined during design by altering the dimensions of the transistor, and it would not be possible to implement precisely using discrete MOSFETs. For the experiments, different

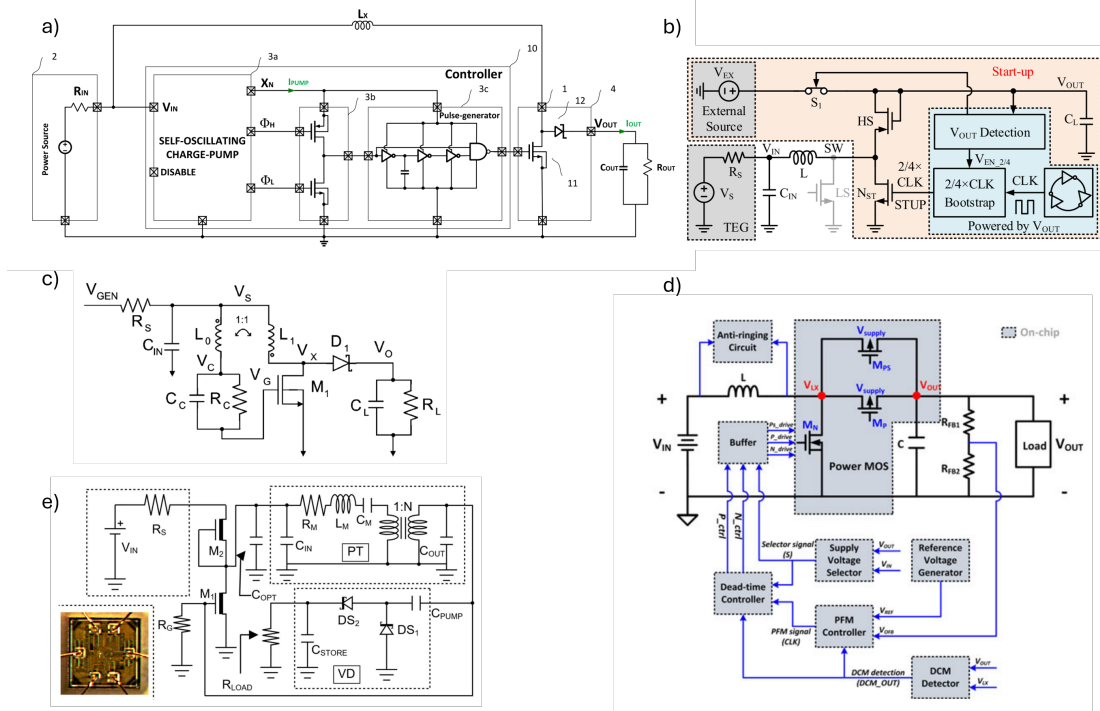


Fig. 3.3: Startup circuits done in CMOS processes: a) [7], b) [9], c) [10], d) [11], e) [12].

transistors were used in this work, with threshold voltages ranging from 0 to 300 mV. The startup process is similar to the one presented by Telles et al. [14], where an LC circuit generates the initial pulses for transistor biasing. The startup voltage for this circuit is 21mV for an input power of $5.8\mu W$.

Another feasible option is to let the input charge the output through the diode (or the parasitic diode of the synchronous rectifier). Two problems that arise from this option is that the output is equal to the input voltage minus the forward voltage drop of the diode, $V_o = V_{in} - V_F$. The other problem is that V_{in} has to be high enough to power the control circuits, which rules out the use of this technique in discrete circuits. An implementation of this method is presented in the work of Wu et al. (Figure 3.3 d)), where the synchronous rectifier is split into two MOSFETs. A large M_P , and a very small M_{PS} , where the large transistor is off during the startup stage, and the small one, which has a higher resistance to avoid inrush currents, is on. Thus, the output is charged through M_{PS} until the control circuits are powered. The circuit starts operating with a voltage of 430mV, which, when compared with other works presented here, supports the idea that this startup method is not practical to reach low startup voltages [11].

Startup circuits with discrete components

When the startup circuit design is translated to circuits made with discrete components, if the use of external energy sources is ruled out, then the best alternative is to use self-powered oscillators. The other techniques depend on on-chip integration to obtain amplification with multiples stages while keeping a reduced size, use specialized techniques only applicable in VLSI, or simply have a too-high startup voltage to be considered techniques applicable to startup circuits with discrete components.

These oscillators can be coupled with some of the techniques previously mentioned in chapter 1, mainly voltage multipliers and magnetic coupling, while starting from very low input voltages [15]. They amplify the input signal generating oscillations, generally through the use of resonant circuits [16]. These oscillations can be rectified and used to power another circuit [16], or used to directly switch a transistor in a DC-DC converter [5]. This usually results in a loss of control of the frequency and duty of the switching signal, but it is a simpler and cheaper solution due to the reduced number of components.

As the input voltage in this kind of circuit is not high enough to switch transistors, normally-on transistors are typically used as switching elements, such as JFETs, depletion MOSFETs [17, 18] or zero/near-zero threshold voltage MOSFETs. When discrete components are used, the variety of depletion or zero-threshold-voltage MOSFETs is quite narrow, so Junction Field Effect Transistors (JFETs) are mainly utilized. Figure 3.4 shows both the transfer and output curve for an N-Channel JFET, where it can be appreciated that for a $V_{GS} = 0V$, the transistor conducts the maximum current I_{DSS} , and it stops conducting when $V_{GS} < V_P$.

Colalongo et al. present a modification of the Royer oscillator [20], where JFETs are used in place of Bipolar Junction Transistors (BJTs) to lower the startup voltage. This circuit has one of the lowest startup voltages for circuits made with discrete components at $V_{in} = 9mV$ [15]. Telles et al. also use the Royer oscillator topology as an ultra-low voltage integrated circuit for energy harvesting [14]. As the BJTs are not normally-on transistors, a starting block is employed to generate a voltage pulse, that in turn is amplified by a transformer and stored in a capacitor to bias the transistors (Figure 3.5). Besides from this starting block, the converter works the same as the original Royer oscillator or the one presented by Colalongo et al. They also have the same disadvantage, and it is the fact that they need hand-wound transformers

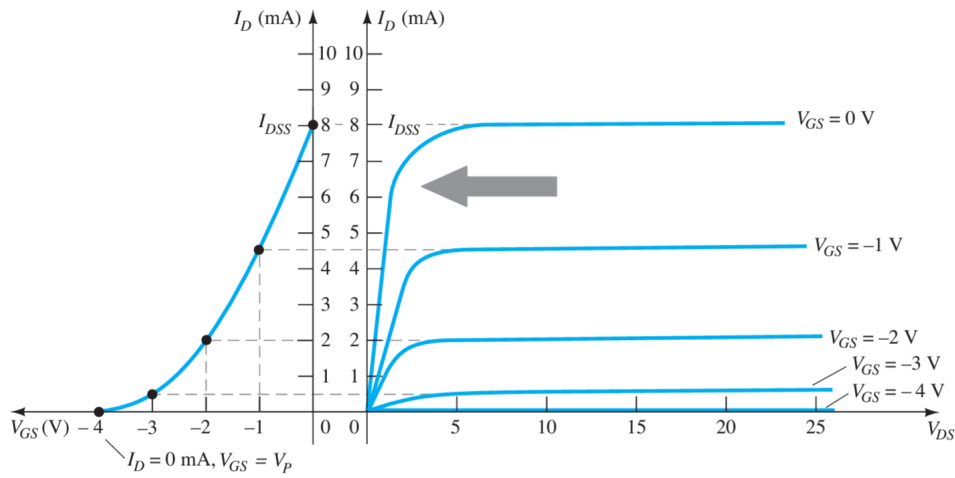


Fig. 3.4: Left: Transfer curve of a JFET. Right: Output curve of a JFET. Source: [19].

to fit the particular configuration needed for this circuit. This circuit, in turn, has a startup voltage of $50mV$.

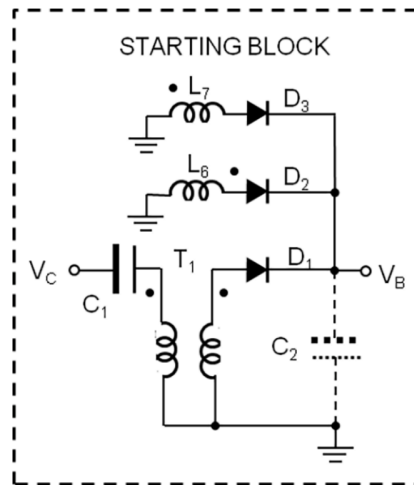


Fig. 3.5: Starting block for BJT's biasing. It works thanks to the transient pulses generated by C_1 and the primary of T_1 . Source: [14].

Park et al. presents a circuit made with COTS components, which acts as both startup and DC-DC converter, with a startup voltage of 440 mV [21]. A BJT is used as the switching element in a flyback converter, while an LC series circuit is used at the base of the transistor to generate the oscillations along with the transformer of the converter.

Many works focus on modifying already established oscillator topologies, mainly focusing in the Armstrong oscillator [22–26] (Figure 3.6 a), b)) and the Hartley oscillator [16] (Figure 3.6 c)). Works focusing in the Colpitts topology are more common in ICs [27–29] (Figure 3.6 d)) or with the use of zero-threshold-voltage MOSFETs [30]. These circuits tend to have ultra-low startup voltages, but a limited Conversion Ratio (CR).

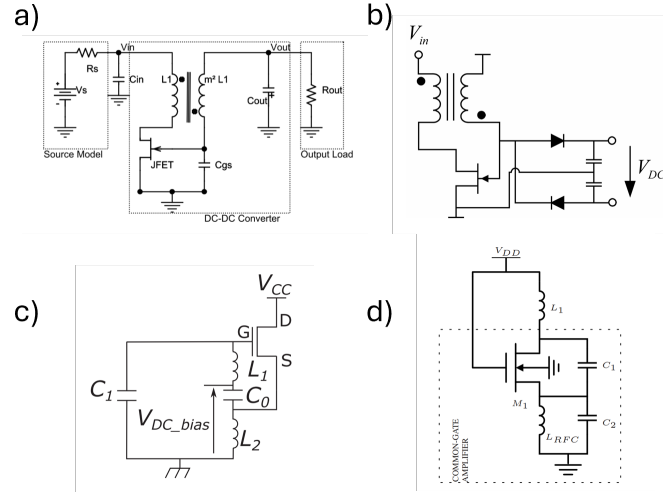


Fig. 3.6: Most common self-powered oscillator topologies. Sources: a) [22], b) [23], c) [16], d) [29].

An overview of the improvements made by some of the circuits presented in Figure 3.6 is presented next:

- a) The work of Adami et al., based on an Armstrong oscillator. There are two main improvements presented in this work: the oscillator transfers energy in the same way as a forward converter, i.e., makes the transfer during the on-state of the transistor. This avoids collapsing the oscillation when charging the output. To understand why, the working mechanisms of the flyback and forward converter are analyzed next (Figure 3.7).

In a flyback converter, energy is stored in the form of a magnetic field in the primary of the coupled inductors during the on-state. When the off-state occurs, the magnetic field collapses and the energy is transferred to the output through the secondary. This means that no external energy is supplied to the output during the on-state. In the context of an oscillator circuit, this could potentially lead to a collapse of the oscillations

Meanwhile, in the forward converter, during the on-state, the energy is transferred through magnetic coupling from primary to secondary, and consequently, to the output. During the off-state, the output inductor, that stored energy during the on-state, starts discharging through the output too. Meanwhile, the tertiary of the transformer resets the flux stored in the transformer core, returning the energy to the input voltage generator. It can be observed then that the forward converter transfers energy to the output during both the on and off state, reducing the chances of oscillation collapse.

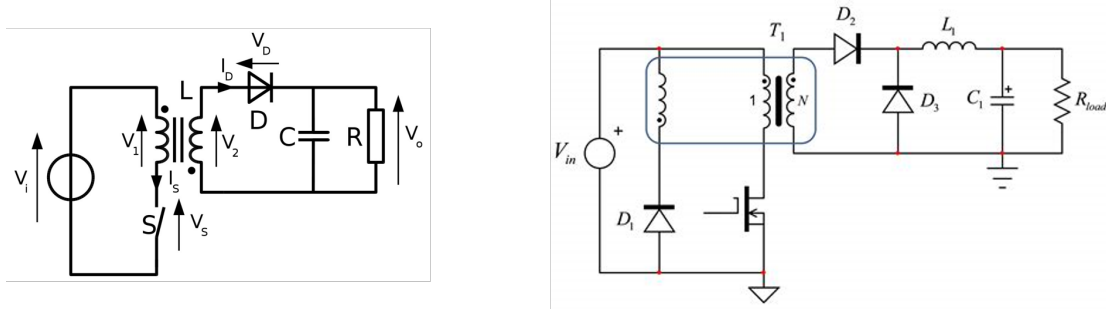


Fig. 3.7: Left: Flyback Converter. Right: Forward Converter.

The second improvement involves the rectifier circuit. The junction formed between the gate and source of the JFET can be represented as a diode between these terminals. Through the oscillation process explained in the article, this configuration allows for the output capacitor to be in series with the gate of the JFET, being charged with negative voltage and altering the bias point of the transistor. As a result, this leads to a larger swing for the oscillating signal and therefore a greater overall current gain. This technique is also used in other works [16, 5], and in the oscillator designed in this thesis. This circuit starts operating with a relatively high input voltage of $100mV$, since its oriented to high-resistance voltage sources. The input power needed for startup is $P_{in} = 3\mu W$.

- b) Grgić et al.'s work is a classic unmodified Armstrong oscillator, although with an N-channel JFET instead of a MOSFET or BJT. The improvement in this work comes from its ultra-low startup voltage and high CR. To obtain these characteristics, seven print transformers (Block VB 0.35/2/6) are cascaded and used in place of the usual transformer of the Armstrong oscillator. Although the characteristics obtained are notable and in-par with the state of the art, the use of these transformers makes the circuit expensive and area-consuming, since each transformer has an area superior to $4cm^2$. Its startup voltage is the lowest obtained for a circuit made with discrete components (at least to the author's knowledge) at $V_{in} = 6mV$.

- c) Lallart et al.'s work consists in a modified Hartley oscillator. The improvement applied is the same as the one mentioned previously in Adami et al.'s work, regarding a capacitor introduced to store energy and alter the bias of the transistor, resulting in higher magnification. This circuit has an startup voltage of $55mV$.

Another way to step-up voltage is to use piezoelectric transformers, which have much higher quality factors than magnetic ones [31], resulting in higher efficiency. Nevertheless, circuits with piezoelectric transformers are not very common due to their price and scarce availability when compared to magnetic transformers. Camarda et al. (Figure 3.3 e)) introduced a converter with a startup circuit, operating from $-8\text{ mV}/+15\text{ mV}$ input voltage, comprised of an inverter in a feedback loop with a piezoelectric transformer. The output is then connected to a voltage doubler for an amplified and rectified voltage output [12].

In this thesis, a new ultra-low voltage self-powered oscillator topology, made entirely with COTS components and based in the Armstrong and Hartley oscillators is presented. In the upcoming sections, the research conducted during this PhD on startup circuits is discussed in detail.

3.2 Armstrong oscillator circuit

As part of the state-of-the-art and oscillator design research phase, a circuit found on literature, presented by Adami et al. [22], was built to be validated.

The circuit is a modified Armstrong oscillator, aimed to work with high-resistance voltage sources (Figure 3.8) [22]. The component values were changed to fit this particular use case, which consisted of a high-resistance printed inorganic TEG.

Another circuit was made, composed of a COTS DC-DC converter, a MAX17220 boost converter. This circuit acts as a second stage and gives the extra amplification needed to reach an output voltage of $2V$, the objective of this experiment. This output voltage level was considered the minimum necessary for the circuit to power IoT or conventional low-power electronic devices. This second circuit also counts with a comparator at the output of the

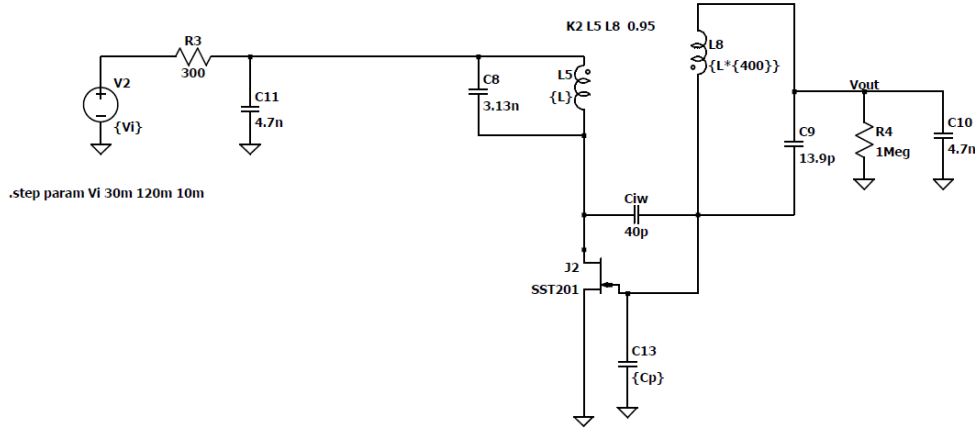


Fig. 3.8: Schematic used for simulation of the modified Armstrong oscillator.

boost converter, acting as a sort of "output enable" to avoid discharging the storage capacitor before time. When the desired voltage is reached, the comparator enables its output, which supplies the load (Figure 3.9). The whole circuit (oscillator with boost converter), along with a printed TEG was published in the journal "Advanced Functional Materials" [32].

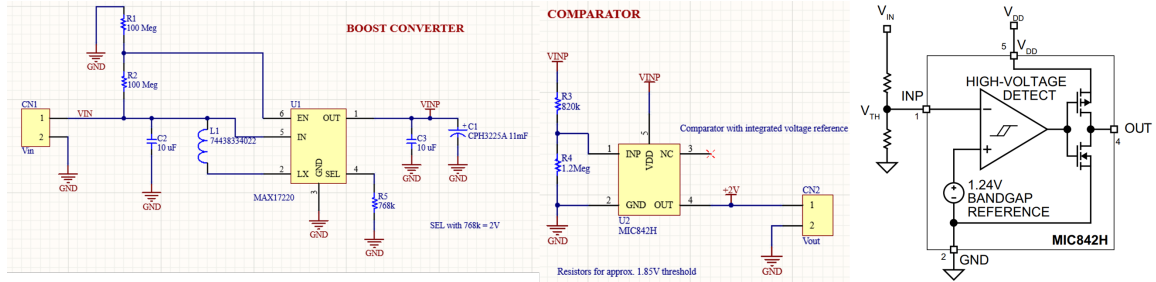


Fig. 3.9: Schematic of the second circuit.

To test the circuit and the TEG in conditions similar to the ones found in real world applications, the TEG was coupled with a heatsink and positioned above a hot plate. The whole measurement setup is shown in Figure 3.10. At the time of measurement, the electrical resistance of the TEG was of approximately 80Ω .

As mentioned previously, the boost converter LTC3108 [33] is commonly employed in literature due to its ability to operate at low voltages (around 20 mV) [34]. Despite the availability of more efficient DC-DC converters, such as those mentioned in [35], their higher startup voltages, often exceeding 600mV, pose challenges. However, the LTC3108 low input resistance ($\approx 2\Omega - 25\Omega$) as specified in its datasheet, is not conducive to maximum power

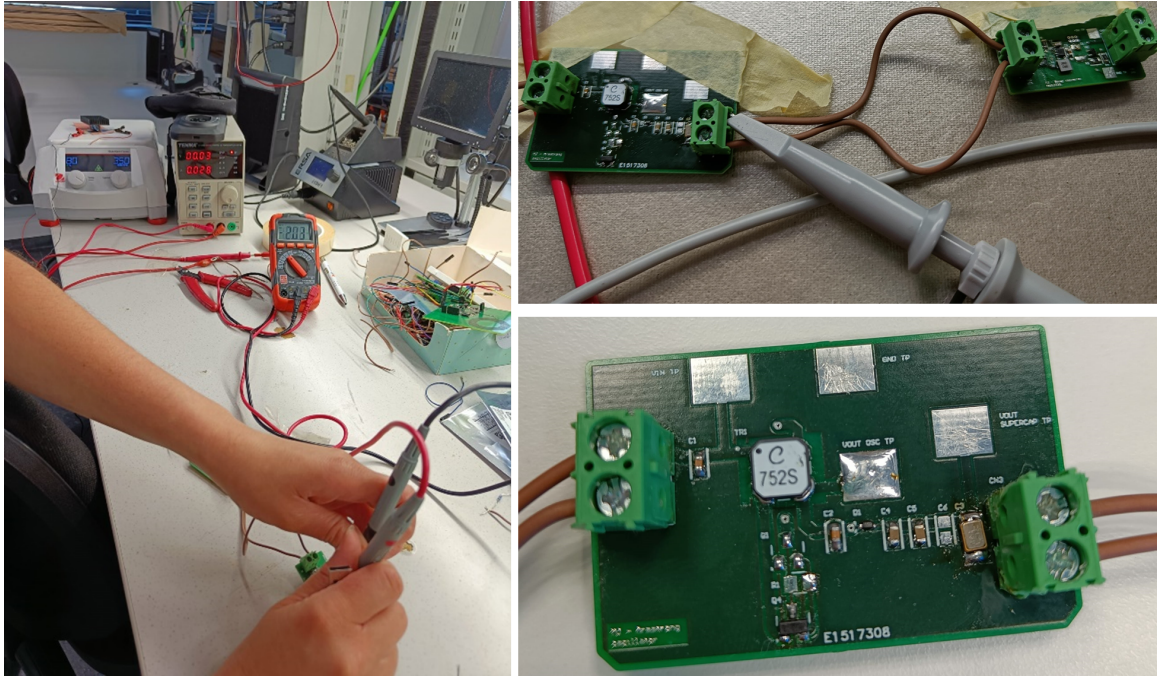


Fig. 3.10: Experiment setup.

transfer in this scenario, where the output resistance of the TEG and the input resistance of the converter are mismatched. Furthermore, the startup voltage is more difficult to reach, as both resistances form a resistive voltage divider. This results in only about 24% of the open-circuit voltage being accessible at the input of the boost converter.

To address these challenges, the system described by Figure 3.11 is proposed, where the TEG is connected to a low-voltage startup stage, providing an initial amplification and operating with lower voltages than conventional converters. The output of this startup stage is connected to a second stage that further amplifies the voltage. The connection between the two boards is shown in Figure 3.10.

The first stage consists of the DC-DC resonant converter mentioned at the start of the section (Figure 3.11 1)), a modification of an Armstrong oscillator adapted from [22]. This oscillator has a low startup voltage thanks to the use of JFETs as the switching element, enabling conduction with zero voltage between their gate and source terminals. It incorporates high-turn ratio transformers to amplify the voltage and complete the feedback loop. Moreover, this circuit is particularly suitable for voltage sources with moderately high output resistance and needs less input power (around $5 \mu W$ for a 1 V output) than the LTC3108 to start working.

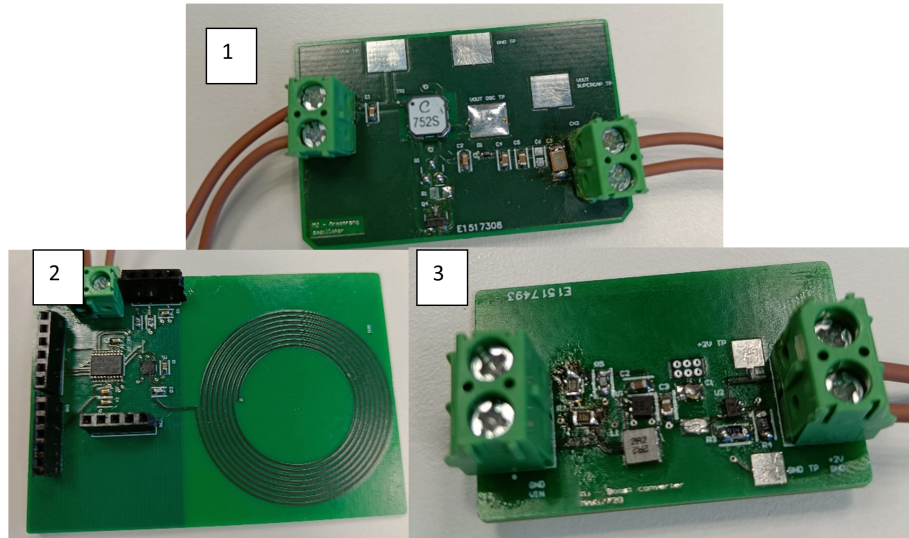


Fig. 3.11: Modules for the Armstrong circuit. 1) Armstrong oscillator based circuit, 2) Application board, 3) Boost converter and comparator board.

As a second stage, a MAX17220 boost converter is employed to further amplify the output voltage from the initial stage to the desired level. It is worth noting that when the input voltage source (TEG) exhibits a resistance exceeding 1Ω , additional input capacitance is required for this converter, to supply the current needed by the boost converter during startup. However, this extra capacitance can load the oscillator, elevating the startup voltage and diminishing the amplification. The extra capacitance only has to sustain the voltage during the startup stage, since the current draw is higher, as well as the voltage needed, than during the main working stage.

3.2.1 Experimental Results

For this experiment, a $C_{in} = 440\mu F$ was used, as it was proven empirically to be the minimum value that allowed a correct startup of the boost converter.

The main components used in the oscillator are the following: the JFET used is a SST201 (SMD equivalent of the J201) due to its low V_P , and a pair of coupled inductors (LPR6235), with a turn ratio of 1:100. For a better matching between resistances, the JFET could be replaced by a 2SK3320-BL, which has a similar V_P but an I_{DSS} almost one order of magnitude higher, reducing the resistance of the transistor. Subsequently, the open circuit values for the

TEG at different hot plate temperatures (when the ambient temperature is $T_a = 24^\circ\text{C}$) are presented.

| Hot plate temperature | Open circuit voltage |
|-----------------------|----------------------|
| 34°C | 22.3 mV |
| 44°C | 37.1 mV |
| 54°C | 56.7 mV |
| 65°C | 74.9 mV |
| 74°C | 81 mV |

Table 3.1: Relationship between hot plate temperature and open circuit voltage.

At 80°C , the boost converter starts working and produces 2V at its output (Figure 3.12). This demonstrates that the output voltage of the TEG can be amplified, and its energy stored in a capacitor for later usage.

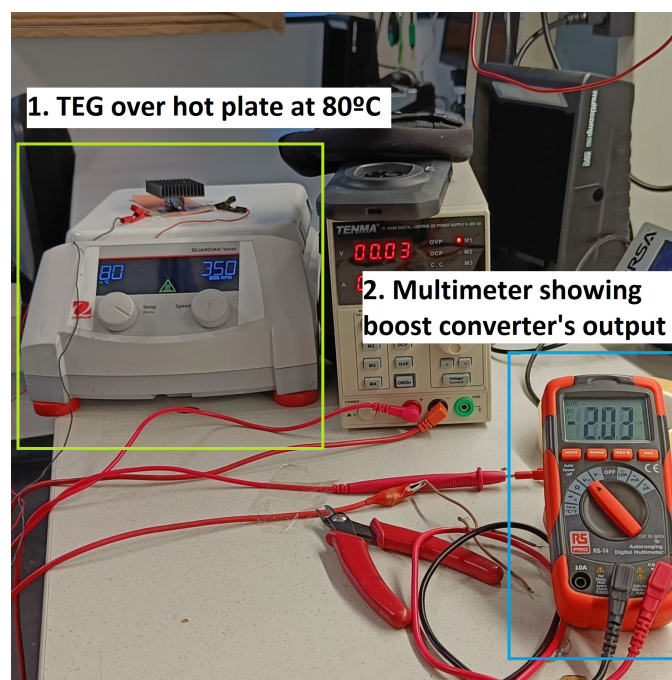


Fig. 3.12: Zoomed setup.

The oscillator was also tested as a standalone amplifier, measuring its startup voltage as well as the input power needed to reach $\approx 1\text{V}$ (Figure 3.13).

In the following section, a new self-powered oscillator topology developed as part of this PhD program is presented.

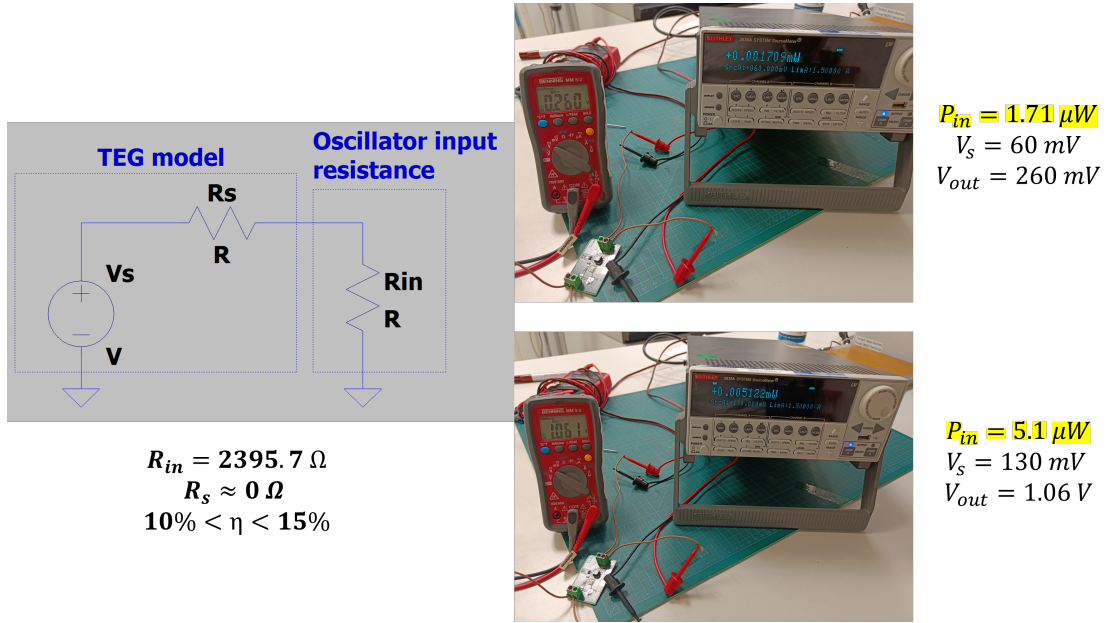


Fig. 3.13: Startup voltage and power (top), input power and voltage for an output of 1V (bottom).

3.3 New self-powered oscillator topology (Horates V3)

3.3.1 Description of the oscillator operation

This section introduces a newly developed self-powered oscillator topology, named Horates V3 following the naming convention from chapter 2. The circuit is based on a Hartley oscillator [36], a topology consisting of a tank circuit conformed by two inductors in series (which might be coupled or not), in parallel with a capacitor, and an amplifier element between the tank and the terminal between both inductors. It is also based in an Armstrong oscillator, due to the use of coupled inductors in the feedback loop. In this case, the amplifier or switching element consists of an N-JFET, since it is a normally on device, a desired characteristic for generating energy build-up when the voltage is small.

When using a JFET as the amplifier element, this topology has an inherent limitation on the output voltage, due to the p-n junction between gate and source that constitutes a diode. This diode conducts during the oscillation positive interval, dampening the oscillations and introducing distortion in the signal. While this behavior might be useful in applications

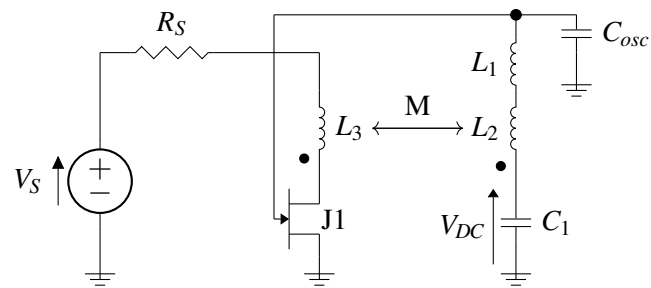


Fig. 3.14: Horates V3 circuit schematic.

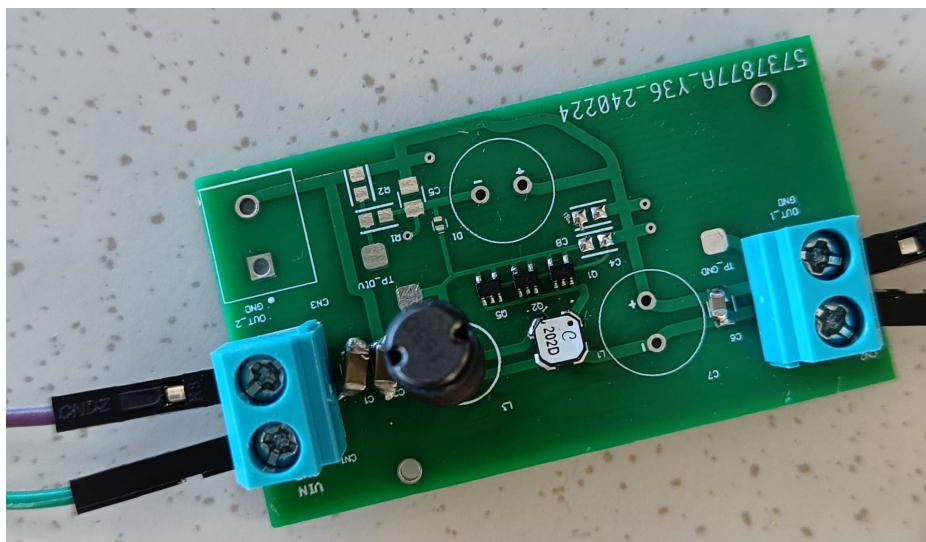


Fig. 3.15: PCB implementation.

where a limited output level is needed, it reduces the maximum amplification achievable when using it as a startup stage for other circuits.

Therefore, one way to overcome this limitation is to add a capacitor (C_1) in series with the inductors. This facilitates the storage of the negative voltage generated by the oscillation during the transistor OFF state and shifts the gate bias voltage of the transistor away from positive values [5]. While this approach does not eliminate entirely the dampening produced by the conducting gate, it notably diminishes it, facilitating larger excursions in the oscillation. This capacitor not only improves the excursion of the oscillation, but because it stores energy, it can be used as a DC negative voltage output. Furthermore, its position does not alter the behaviour of the circuit, so one of its terminals can be connected to ground, to obtain an output referenced to ground and with reduced ripple, since its connected directly to a capacitor. As a result, the circuit is not only enhanced by introducing a bias-altering capacitor, but also obtains a DC output with reduced ripple and the capability to supply loads referenced to the same ground.

The process of voltage amplification in this circuit is divided into two steps: the first amplification comes from two COTS coupled inductors introduced in the circuit design to reduce the startup voltage and amplify the magnitude of the oscillations, as part of the input voltage is amplified by the turn ratio (N) of the coupled inductors. The second amplification comes from the inductors L_1 and L_2 , as L_2 discharges during resonance, with a current $I_{L_2} = V_{L_2}/(j\omega_o L_2)$, where V_{L_2} is the voltage over L_2 and ω_o the circuit resonance frequency, so the voltage over L_1 is equal to $V_{L_1} = V_{L_2} L_1/L_2$, effectively amplifying V_{L_2} by a factor L_1/L_2 . Both amplification sources can be traced back to classical oscillator topologies, as seen in Figure 3.16.

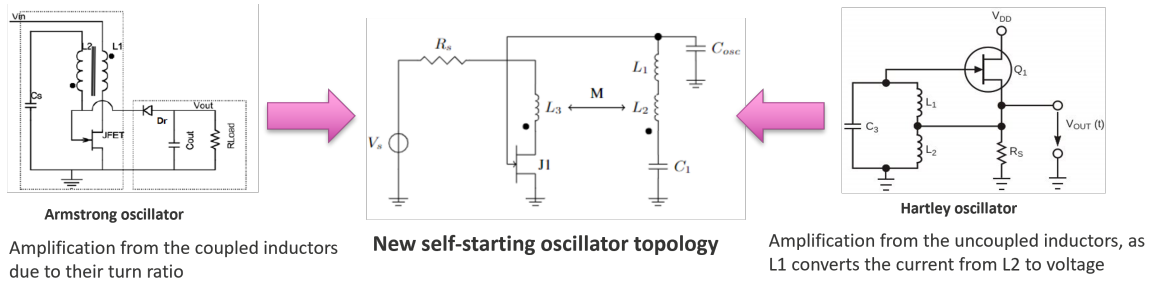


Fig. 3.16: Voltage amplification sources and relationship of the circuit with classical oscillators.

The coupled inductors added to the circuit generate a marginal compromise in design flexibility, although the utilization of commercially available options offsets this concern.

The oscillation process is the same as in a classical Armstrong oscillator with a JFET as the amplifier element, but taking into consideration that the storage capacitor, C_1 , gets charged with a negative voltage V_{DC} during the OFF-state of the transistor, altering the bias voltage of the gate [22].

- At startup, when V_{IN} is connected, the JFET starts conducting and a positive voltage drop is generated over L_3 . In turn, this generates a positive voltage over L_2 , amplified by the turn ratio (N) between L_3 and L_2 . During this stage, the gate-source diode conducts, and the storage capacitor (C_1) is charged with negative voltage.
- When the primary current saturates, the voltage drop in both coupled inductors turns to zero. The negative voltage stored in C_1 is applied over the JFET's gate, pinching the channel.
- The primary current starts decreasing due to the pinched channel, generating a negative voltage over both coupled inductors and pinching the channel even more. Now L_2 starts charging the gate-source capacitor of the JFET with negative voltage.
- Once L_2 is discharged, the cycle begins again, giving way to oscillation.

In order to design this oscillator circuit, different concepts and mechanisms previously explained in literature were integrated to reduce its startup voltage and raise its conversion ratio. To summarize:

- Use of a JFET (normally-on transistor) for conduction with zero voltage.
- A capacitor in series with the gate of the JFET, to accumulate a negative DC voltage that slowly shifts the bias point of the transistor. This, in turn, allows for a bigger excursion of the oscillating signal before the channel is fully pinched-off, elevating the conversion ratio of the circuit.
- Coupled inductors between the input and the resonant branch, to add extra voltage amplification proportional to their turns ratio [23]. Secondly, the secondary of the

coupled inductors has a double function, as it not only allows magnetic coupling, but also acts a current pump in the resonant branch [16].

- An inductor with a much higher inductance value than the secondary of the coupled inductors. This high inductance, when coupled with the current introduced by the secondary inductor, is transformed to a voltage proportional to the ratio between the two inductors, acting in a similar way to an autotransformer.
- Lastly, as the oscillating signal is mounted over a negative DC voltage, and its positive side is clipped by the gate-source diode of the JFET, a negative rectifier circuit can be coupled to the oscillator circuit output, to almost double the amplification level, obtaining a DC voltage. This option allows for a high conversion ratio while keeping a single-ended output, which is ideal when supplying circuit that cannot accept a differential supply voltage.

3.3.2 Oscillator Circuit Architecture

The small-signal model of the Horates V3 circuit (Figure 3.17) is obtained to derive the equations for the voltage required for startup. The following considerations are taken:

- C_1 , the storage capacitor, can be considered a short-circuit at the resonance frequency, since $C_1 \gg C_{osc}$.
- Since $V_{DS} \ll |V_P|$, the JFET works in the ohmic linear region, where it behaves as a voltage-controlled resistor. Its small-signal behavior is represented by a current source $g_m V_{gs}$, with g_m being the transconductance and V_{gs} the dynamic gate-source voltage, while a resistor $R_{DS_{on}}$, equal to the zero-gate-source voltage drain-source resistance, represents the bias condition during startup when the gate-source voltage is near 0.
- The first analysis is performed with ideal passive components and source resistance $R_S = 0$.

Once the small-signal model (Figure 3.17) is obtained following the previously stated criteria, Kirchhoff's laws are applied to it, leading to the following equations describing the circuit

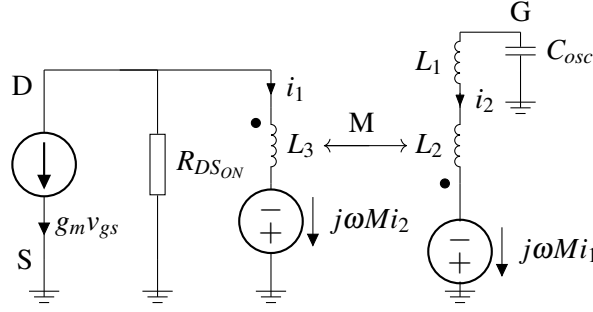


Fig. 3.17: Small-signal model of the Horates V3 circuit during startup.

$$v_{ds} = i_1 R_{DS_{on}} - R_{DS_{on}} g_m \frac{i_2}{sC_{osc}} \quad (3.1)$$

$$i_1 = \frac{sMi_2 - v_{ds}}{sL_3} \quad (3.2)$$

$$v_{gs} = \frac{i_2}{sC_{osc}} \quad (3.3)$$

$$i_2 = \frac{s^2 M C_{osc} i_1}{s^2 L_{eq} C_{osc} + 1} \quad (3.4)$$

where $L_{eq} = L_1 + L_2$.

These equations are then used to produce the signal flow graph in Figure 3.18, from which the characteristic equation (the determinant of the graph) of the circuit is obtained through the use of Mason's gain formula, as described in [37].

The loop gains in the graph are as follows:

$$T_1 = \frac{s^2 M^2 C_{osc}}{L_3 (s^2 L_{eq} C_{osc} + 1)} \quad (3.5)$$

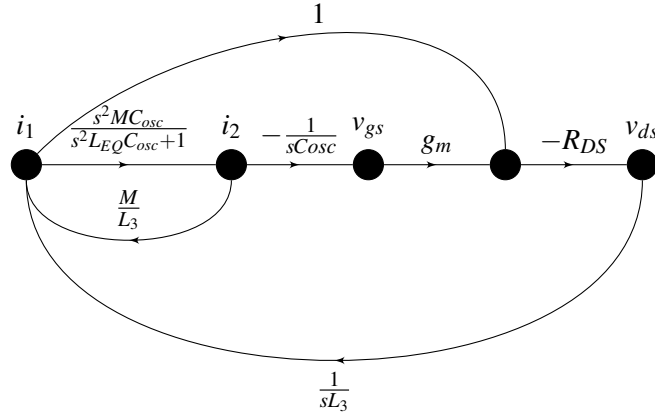


Fig. 3.18: Flowgraph describing the circuit.

$$T_2 = \frac{s^2 MC_{osc} g_m R_{DS_{on}}}{s^2 C_{osc} L_3 (s^2 L_{eq} C_{osc} + 1)} \quad (3.6)$$

$$T_3 = -\frac{R_{DS_{on}}}{sL_3} \quad (3.7)$$

Consequently, the characteristic equation is

$$\Delta = 1 - T_1 - T_2 - T_3 = 0 \quad (3.8)$$

and it is evaluated in the Fourier domain ($s = j\omega$). The oscillation frequency ω_o is obtained equating the real term to 0:

$$\omega_o = \frac{1}{\sqrt{C_{osc} L_{eq}}} \quad (3.9)$$

Meanwhile, the instability condition is determined by the imaginary part of the equation being less than 0, when ω is replaced by the resonance frequency ω_o .

$$g_m R_{DS_{on}} > \frac{M}{L_{eq}} \quad (3.10)$$

To put the equation in terms of the input voltage, we replace g_m and $R_{DS_{on}}$ by their actual values during startup, when $V_{GS} \approx 0$.

$$I_{DS} = \frac{2I_{DSS}}{V_P^2} (V_{GS} - V_P - \frac{V_{DS}}{2}) V_{DS} \quad (3.11)$$

$$R_{DS_{on}} = \frac{V_{DS}}{I_{DS}} = \frac{|V_P|}{2I_{DSS}} \quad (3.12)$$

$$g_m = \frac{d(I_{DS})}{d(V_{GS})} = \frac{2I_{DSS}}{V_P^2} V_{DS} \quad (3.13)$$

Then, as $V_{DS} \simeq V_S$ on startup, and $R_S = 0$:

$$V_S > \frac{k\sqrt{L_3 L_2}}{(L_1 + L_2)} \cdot |V_P| \quad (3.14)$$

Which for a turn ratio of N , assuming $L_3 = L_2/N^2$ turns to

$$V_{IN} > \frac{kL_2}{N(L_1 + L_2)} \cdot |V_P| \quad (3.15)$$

and the startup voltage is N times smaller than it would be while using just an inductor L_2 of the same value without the addition of coupled inductors.

It can also be appreciated that the startup voltage is directly proportional to the coupling factor (k) of the inductors, and it is proved through simulations that diminishing the coupling factor also reduces the startup voltage. Nonetheless, as expected, this only applies to a circuit with ideal components, where both inductors and the voltage source do not have any resistance.

The next step deriving the startup voltage equation is to add resistance to these ideal components. R_S corresponds to the voltage source resistance, while r_1 corresponds to the series resistance of L_1 and L_2 . The resistance of L_3 is counted as part of R_S , and the Equivalent Series Resistance (ESR) of the capacitors is ignored. To simplify the calculations, the coupling between inductors is considered perfect, so $k = 1$ and $M = \sqrt{L_2 L_3}$. To calculate the new ω_o and oscillation condition, the loop gains are calculated with the new parameters, and the previous process is repeated.

$$T_1 = \frac{s^2 M^2 C_{osc}}{L_3 (s^2 L_{eq} C_{osc} + r_1 s C_{osc} + 1)} \quad (3.16)$$

$$T_2 = \frac{M g_m R_{DS_{on}}}{L_3 (s^2 L_{eq} C_{osc} + r_1 s C_{osc} + 1)} \quad (3.17)$$

$$T_3 = -\frac{R_{DS_{on}}}{s L_3 + R_S} \quad (3.18)$$

The oscillation frequency in this case is described by:

$$\omega_o^2 = \frac{L_3 (R_S + R_{DS_{on}}) - M g_m R_{DS_{on}} R_S}{C_{osc} (L_3^2 r_1 + L_{eq} L_3 (R_S + R_{DS_{on}}) - M^2 R_S)} \quad (3.19)$$

Meanwhile, to find the oscillation condition (or the startup voltage), an additional consideration must be made, as the analysis now includes R_S . Just before the start of the oscillations, the behavior of L_3 would be dominated mainly by its resistance, r_3 . As a small inductance, $R_S \gg r_3$ and $R_{DS_{on}} \gg r_3$ its assumed, so the drain-source voltage is

$$V_{DS} = V_S \frac{R_{DS_{on}}}{R_{DS_{on}} + R_S} \quad (3.20)$$

where $b = (R_{DS_{on}} + R_S) / R_{DS_{on}}$.

$$V_S > b \frac{R_{DS_{on}} + r_1(1/N^2 + C_{osc}r_1(R_S + R_{DS_{on}})/L_2 + C_{osc}L_{eq}(R_S + R_{DS_{on}})^2N^2/L_2^2)}{r_1/N + R_{DS_{on}}L_{eq}N/L_2} |V_P| \quad (3.21)$$

Evaluating Eq. 3.21, it can be concluded that there are tradeoffs when trying to reduce the startup voltage, mainly between L_1 and its resistance, r_1 , as well as between L_2 and the turn ratio N .

Looking at the equation, C_{osc} could be reduced all the way (although the minimum would be determined by the gate-source capacitance of the JFETs, C_{gs}), but in reality, that raises the frequency and might affect L_1 and r_1 . Effects such as skin effect or core losses are more appreciable at higher frequencies, leading to an increase in r_1 , while L_1 might be diminished due to limitations related to the self-resonance frequency.

One advantage of this circuit is that by introducing the coupled inductors, the requirements for L_1 are relaxed since its value can be diminished (reducing r_1 and raising the self-resonance frequency) and obtain the same effect as in a circuit without coupled inductors. This is especially important since for a low startup voltage, we want C_{osc} to be as low as possible as stated previously.

Then, overall, when using coupled inductors with low turn ratios the circuit will tend to have a lower resistance in the L_1 branch since the resistance of the secondary is not high enough to offset the advantages previously mentioned. Another effect that stems from a lower L_1 is a higher operating frequency, which has a direct positive impact on both efficiency and DC output level, as it reduces the main source of losses, conduction losses in both the transistor and inductors.

In the next section, simulations done on LTSpice to verify the validity of the startup voltage equation are presented.

3.3.3 Simulations

Before design, the circuit was simulated in different conditions to see how well the startup voltage equation approximates reality, as well as to help make the final decision in component choices and values. To test for the startup voltage (Figure 3.19 and Figure 3.20), the input voltage source is swept from 0 mV to 100 mV in a linear fashion, with 0.1 mV steps. The startup voltage is found when the output of the circuit starts oscillating.

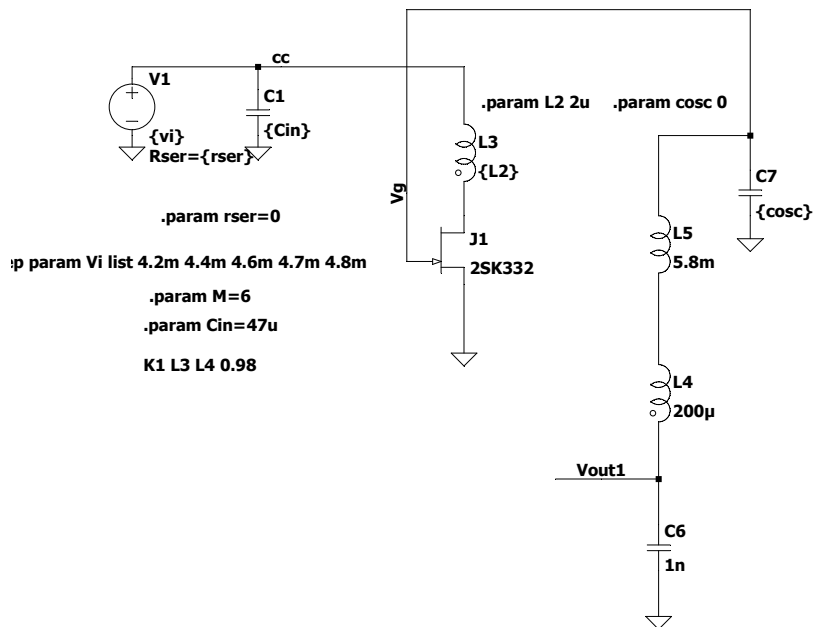


Fig. 3.19: Schematic used for the simulations.

The result from the simulations is a startup voltage of 4.7mV , when the startup voltage of the real circuit is 9.3mV and the provided by the equation is 9.9mV . These differences come mostly from the inductor L_5 in Figure 3.19, since its frequency-dependent behavior was not modeled. Since the oscillation frequency of the circuit is not much lower than the self-resonance frequency of the inductor, as it should be to avoid changes in the impedance of the inductor, its inductance and series resistance suffer changes. One inductor with a nominal 3.3mH value was measured with a HM8118 LCR Bridge, from a frequency of 20 kHz to a

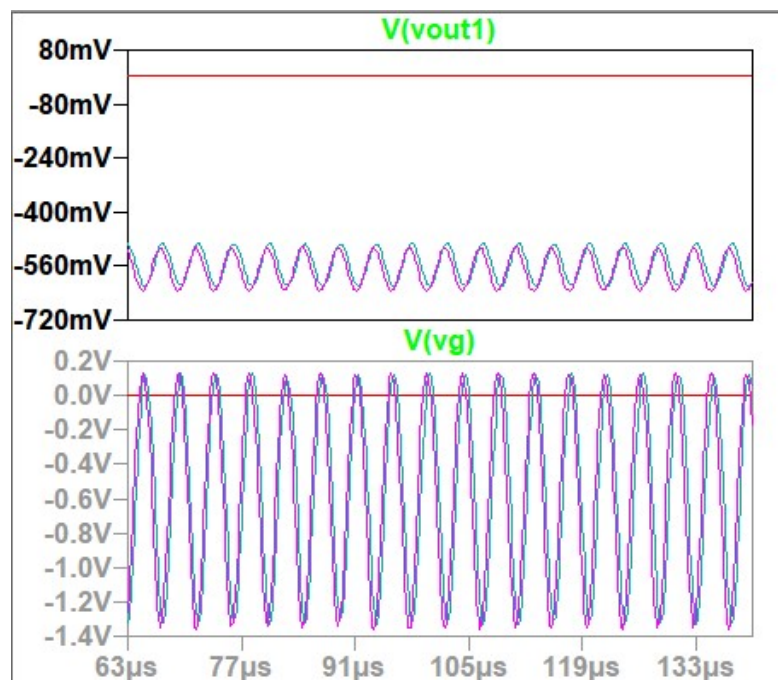


Fig. 3.20: Results of the startup voltage simulation.

frequency of 200 kHz (corresponding to the oscillation frequency when $V_{in} = 40mV$). The results are presented in Table 3.2.

| Frequency | Inductance | Series Resistance |
|-----------|------------|-------------------|
| 20 kHz | 2.92mH | 13.7Ω |
| 50 kHz | 2.91mH | 16.5Ω |
| 75 kHz | 2.91mH | 18.1Ω |
| 100 kHz | 2.9mH | 20.2Ω |
| 150 kHz | 2.9mH | 23.5Ω |
| 200 kHz | 2.9mH | 25.7Ω |

Table 3.2: Inductance and series resistance against frequency.

Additionally, the circuit was simulated with different inductors to optimize startup voltage and CR, but the final decision was made empirically, due to the lack of modeling of the frequency-dependent behavior mentioned previously. On top of that, the circuit was also simulated with another JFET, the SST201, to verify its performance with high-resistance voltage sources (Figure 3.21).

As can be seen in Figure 3.22, the circuit starts operating with an open circuit voltage of 80mV and a generator output resistance of 1kΩ, validating the design adapted for high-resistance

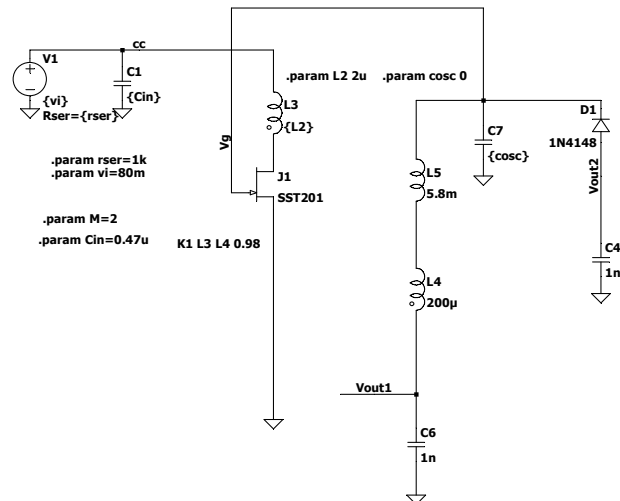


Fig. 3.21: Schematic of the oscillator circuit adapted to a high-resistance generator.

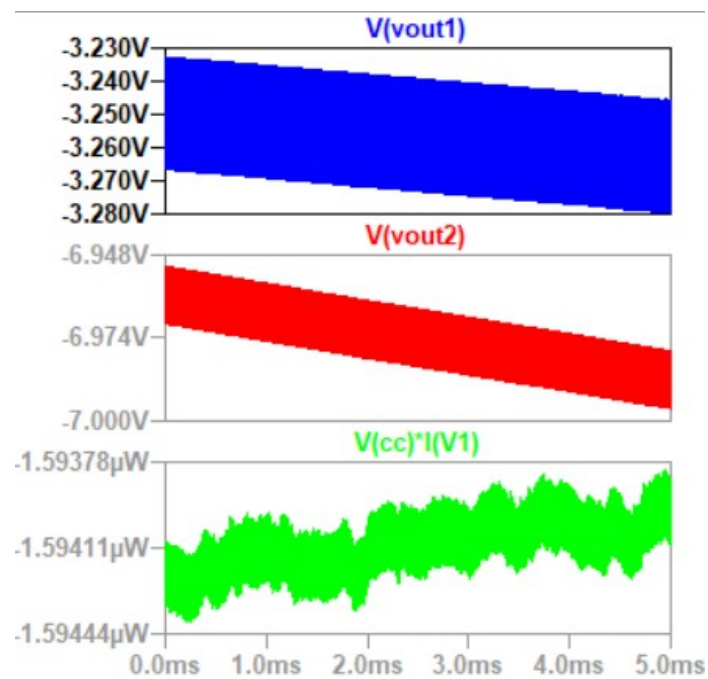


Fig. 3.22: Results of the simulation for the high-resistance adapted circuit.

generators. As a future step for this work, the simulation results should be corroborated by fabricating the oscillator using SST201 JFETs instead of the 2SK3220 ones it currently uses.

3.3.4 Experimental Results

Oscillator Circuit Design

The circuit Horates V3 was built to validate the theoretical development done. The design criterion for this circuit is to have the minimum possible startup voltage, while matching its input resistance during startup to the resistance of a printed TEG with a resistance of around 5Ω . To select the JFET, based on the startup equation (Eq. 3.21), V_P should be as small as possible, as it affects the whole equation. Meanwhile, as the TEG selected has a relatively small resistance $R_{TEG} = 5.5\Omega$, the I_{DSS} of the JFET should be as high as possible. The JFET 2SK3320 was selected, as it fits the criteria, with a V_P between $-0.2V$ and $-1.5V$, and an I_{DSS} between 1.2 mA and 14 mA . As the 2SK3320 is comprised of two N-JFETs in a same package, three of them were used in the circuit, leading to 6 JFETs in parallel in total. This leads to an $R_{DS_{on}} = 5.06\Omega$ using the Eq. 3.12, with $|V_P| = 0.85V$, as the average between minimum and maximum, and $I_{DSS} = 14mA$, equal to the maximum I_{DSS} . It is important to note that selecting a smaller V_P will reduce the efficiency and the output voltage, as it reduces the conduction time of the JFET, and therefore, L_3 stores less energy per oscillation cycle. This constitutes a tradeoff between startup voltage and maximum output voltage.

As the circuit was made with COTS components, the next components chosen were the coupled inductors, as their variety is more limited. Based on Eq. 3.15, it is crucial that the ratio L_2/L_{eq} be as small as possible, since it affects both startup voltage and conversion ratio. Hence, a small L_3 maximizes the benefits, as it allows for a larger N while keeping L_2 small. With this criterion, coupled inductors from the LPR4012 (Coilcraft) series were chosen, with $L_3 = 2\mu H$ and $N = 10$, as it has the highest N of the series, while maintaining L_3 and r_1 small enough.

Considering C_{osc} is equal to the C_{gs} capacitance of the JFETs, the last component which affects the startup voltage to be chosen was the inductor L_1 . For this selection, since all the other components had been chosen, the Eq. 3.21 was used to test different inductors. As

mentioned before, the fact that both inductance and resistance are a function of the oscillation frequency should be taken into account. The inductor chosen had an inductance $L_1 = 3.3mH$ and $r_{1DC} = 7.8\Omega$, but when measured at a frequency of 200 kHz using an HM8118 LCR Bridge (Rohde & Schwarz), $L_{1200kHz} = 2.9mH$ and $r_{1200kHz} = 25.7\Omega$. Two of these inductors were used in series, to achieve a higher inductance while maintaining a higher self-resonance frequency than with just one larger inductor.

Lastly, the storage capacitor was chosen to be $C_1 = 220\mu F$, which is a sufficiently high value to not influence the resonance between L_{eq} and C_{osc} . Table 3.3 presents a summary of the components chosen.

| Designator | Reference |
|------------|-----------------------------|
| J_1 | 2SK3320-BL (Toshiba) x 6 |
| L_1 | 17335C (Murata) x 2 |
| L_2 | LPR4012-202LMR_ (Coilcraft) |
| L_3 | LPR4012-202LMR_ (Coilcraft) |
| C_1 | UKL1A221MPD (Nichicon) |

Table 3.3: List of components used in the oscillator circuit.

Oscillator Circuit Characterization

To characterize the Horates V3 circuit, a 2604B Sourcemeter (Keithley) was used as a voltage source V_S , and the output voltage was measured with a 34410A multimeter (Agilent), which can be characterized as a load resistance $R_L = 10M\Omega$.

The voltage V_S was swept starting from zero. The circuit starts working at $V_S = 9.92mV$. The voltage was then increased up to 100 mV in steps of 10 mV in order to measure the output voltage V_{DC} and the ratio between it and V_S , called conversion ratio.

The onset voltage $V_S = 9.92mV$ is equal to $V_{IN} = 9.3mV$ when accounting for the series resistance of the power source and its connection. Moreover, the conversion ratio for the startup voltage is equal to 30 times, while for $V_S \geq 20mV$, the conversion ratio is larger than 50 times, resulting in a significant amplification of the input voltage.

An extra characterization was done after this one, adding a negative voltage rectifier to the gate of the JFET, to obtain a second output with higher amplification than the original one (Figure 3.23). The resulting circuit schematic can be observed in Fig. S5 in the Supporting Information. The characterization setup is the same as the first one, where the input voltage is increased in steps of 10 mV until reaching 100 mV. In this case, the onset voltage is $V_S = 10.6\text{mV}$, and is equal to a $V_{IN} = 10\text{mV}$.

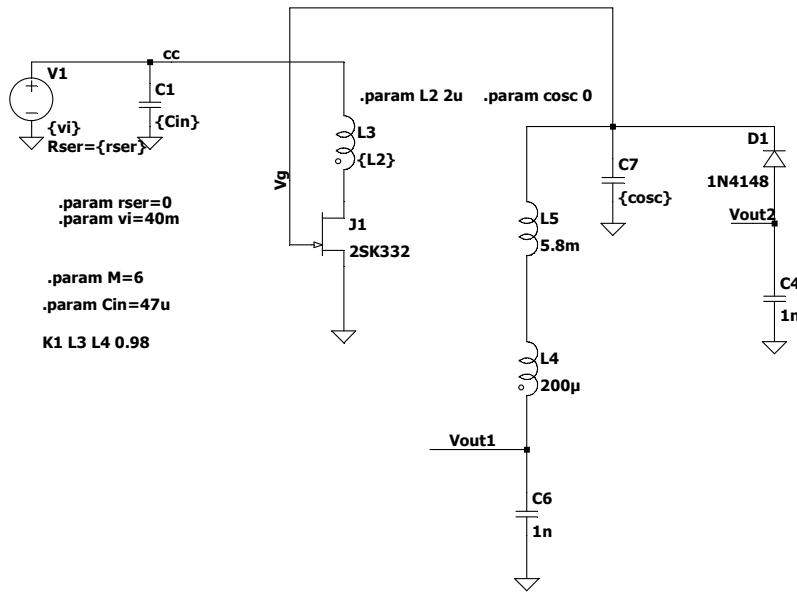


Fig. 3.23: Schematic of the circuit used with the added negative voltage rectifier.

The results of both characterizations are shown Figure 3.24.

Albeit efficiency (η) is not the focus of this circuit, as it is just expected to work as a startup stage for a more efficient circuit, it was measured using a linear potentiometer as a variable load resistance R_L to achieve maximum power transfer. Results are shown in Table 3.4.

The input resistance R_{IN} during startup is equal to $R_{IN} \approx R_{DS_{on}}$. Measurements indicate that $R_{IN} = 11.25\Omega$. This value goes up as the circuit starts working, since the channel of the

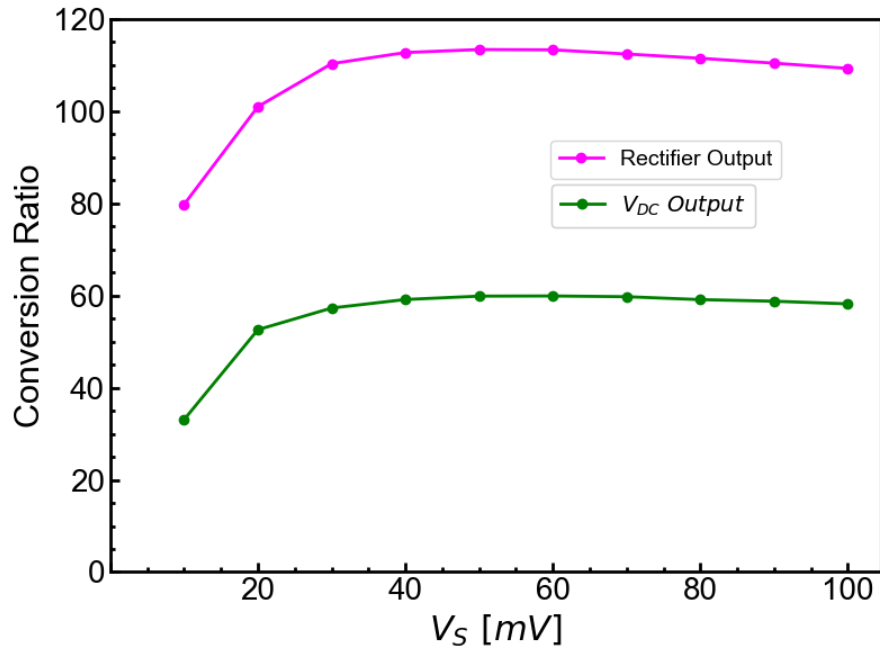


Fig. 3.24: Conversion ratio for the V_{DC} output and for the negative rectifier output.

| V_S | R_L | η |
|--------|-----------------|--------|
| 40 mV | 473.4 $k\Omega$ | 4.46% |
| 70 mV | 423 $k\Omega$ | 5.97% |
| 100 mV | 402.5 $k\Omega$ | 6.17% |

Table 3.4: Efficiency of the oscillator circuit.

JFET starts getting pinched with the voltage of C_1 . This circuit has potential to be adapted to work with generators with high output resistance, by changing the JFET that acts as switching element. Simulations of this use case are presented in subsection 3.3.3. Lastly, in Table 3.5 a comparison is made against the state-of-the-art in startup circuits made with discrete components, comparing normalized startup voltage, startup power, and conversion ratio.

| Ref. | Startup V_{IN} | Startup P_{IN} | Max. Conv. Ratio | Peak η |
|-----------|------------------|------------------|------------------|-------------|
| [23] | 62 mV | 42.2 μW | N/A | 17% |
| [23]* | 6 mV | 0.49 μW | ≈ 280 ** | 12% |
| [16] | 55 mV | 90.5 μW ** | 54 | 1.7% |
| [22] | 100 mV | 3 μW | 10 | 25% |
| [15] | 9 mV | 0.8 μW | 99 | 54.4% |
| [5] | 17 mV | 8.87 μW | N/A | N/A |
| This work | 9.3 mV | 7.7 μW | 60 *** | 6% |

Table 3.5: Parameters comparison with state-of-the-art startup circuits. * [23] with seven cascaded transformers instead of one. ** Parameters estimated based on available data. *** Can be nearly doubled adding a negative rectifier connected to the gate of the JFET.

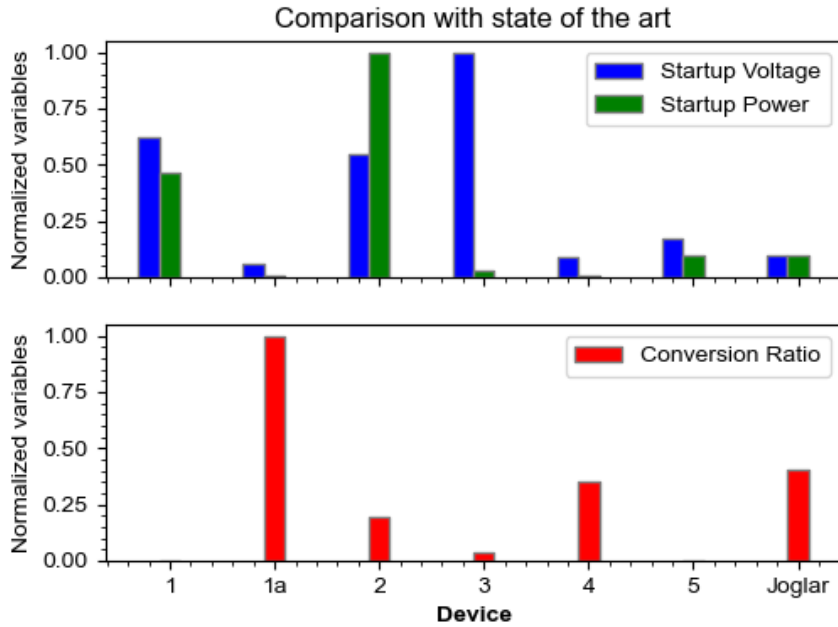


Fig. 3.25: Comparison with state of the art. The Horates V3 circuit is represented as "Joglar".

Impedance matching with the generator

Since the efficiency of the Horates V3 circuit is already pretty low ($\approx 6\%$), it is best to match the impedance of the generator to the input impedance of the startup circuit, for maximum power transfer. In this circuit, since the R_{IN} during startup is approximately equal to $R_{DS_{on}}$, impedance matching can be done while designing the circuit, if the generator to be used is previously known. It is not an exact process, since JFET parameters have a wide variation due to their fabrication process, as seen in Figure 3.26, but it is enough to discriminate between high and low resistances. To prove this, simulations have been done where the JFET is changed depending on the voltage source used.

Electrical Characteristics (Ta = 25°C) (Q1, Q2 common)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|------------------------------|---------------------|---|------|------|------|------|
| Gate cut-off current | I_{GSS} | $V_{GS} = -30\text{ V}, V_{DS} = 0$ | — | — | -1.0 | nA |
| Gate-drain breakdown voltage | $V_{(BR) GDS}$ | $V_{DS} = 0, I_G = -100\text{ }\mu\text{A}$ | -50 | — | — | V |
| Drain current | I_{DSS} (Note) | $V_{DS} = 10\text{ V}, V_{GS} = 0$ | 1.2 | — | 14.0 | mA |
| Gate-source cut-off voltage | $V_{GS (OFF)}$ | $V_{DS} = 10\text{ V}, I_D = 0.1\text{ }\mu\text{A}$ | -0.2 | — | -1.5 | V |
| Forward transfer admittance | $ Y_{fs} $ | $V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ kHz}$ | 4.0 | 15 | — | mS |
| Input capacitance | C_{iss} | $V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$ | — | 13 | — | pF |
| Reverse transfer capacitance | C_{rss} | $V_{DG} = 10\text{ V}, I_D = 0, f = 1\text{ MHz}$ | — | 3 | — | pF |
| Noise figure | NF (1) | $V_{DS} = 10\text{ V}, R_G = 1\text{ k}\Omega, I_D = 0.5\text{ mA}, f = 10\text{ Hz}$ | — | 5 | — | dB |
| | NF (2) | $V_{DS} = 10\text{ V}, R_G = 1\text{ k}\Omega, I_D = 0.5\text{ mA}, f = 1\text{ kHz}$ | — | 1 | — | |

Note 2: I_{DSS} classification Y (Y): 1.2~3.0 mA, GR (G): 2.6~6.5 mA, BL (L): 6.0~14.0 mA

() I_{DSS} rank marking

Fig. 3.26: Spread of JFET parameters. Source: [38].

Startup stage powered by TEG

The Horates V3 circuit was used first as a step-up stage for a printed inorganic TEG, the product of the work of another student in the HORATES project, and part of the work submitted for publishing during this thesis [1], as a way to verify the performance of both devices. The TEG was connected to the startup stage and placed in a custom-built setup to maintain a known and steady ΔT . In the custom-built setup, the temperature of two copper blocks can be adjusted between 273K - 363K, to generate a temperature difference along the TEG. The TEG was introduced between the copper blocks, and subsequently connected to the oscillator circuit. After that, the temperature of the copper blocks was swept, raising

ΔT until the circuit started oscillating. Oscillation was observed for $\Delta T = 7.5K$. This is considered the ΔT needed for startup. Both the startup ΔT and V_{OC} are shown in Figure 3.27, while the whole test setup is shown in Figure 3.28.

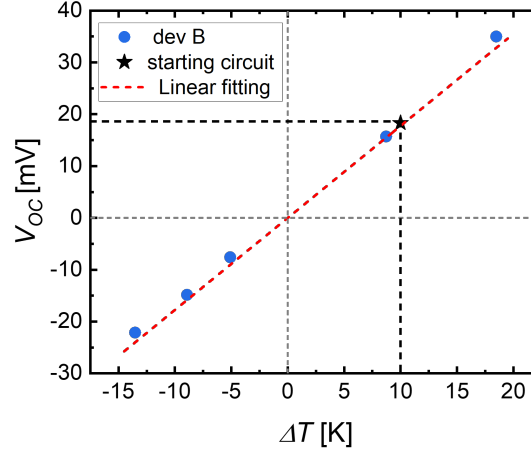


Fig. 3.27: Output voltage against ΔT . The startup voltage for the circuit is marked with a star.

Startup stage powering a DC-DC converter

A basic (without MPPT method nor output voltage regulation) custom-built DC-DC converter was made to verify the performance of the Horates V3 circuit as a startup stage (Figure 3.29). A 2604B Sourcemeter (Keithley) was used as a voltage source for better control and reproducibility.

The output of the startup stage was connected to a relaxation oscillator, i.e., a square wave oscillator, made with a TS881 comparator (ST Microelectronics), due to its low power consumption and minimum supply voltage. This relaxation oscillator was then in charge of driving the gate of the P-MOSFET used in the DC-DC converter as switching element. The converter was not characterized as it was made as a prototype to show the performance of the startup circuit.

The DC-DC converter has two outputs. One with negative voltage (V_{DC}), that was connected through a diode to the output of the startup stage, partially shutting it down due to the

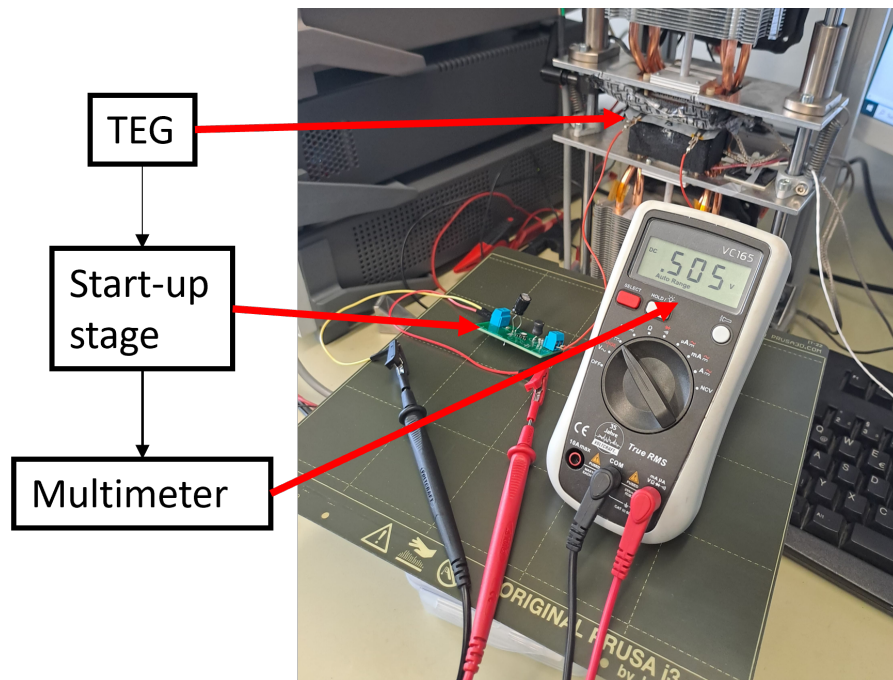


Fig. 3.28: Setup used for the experiment.

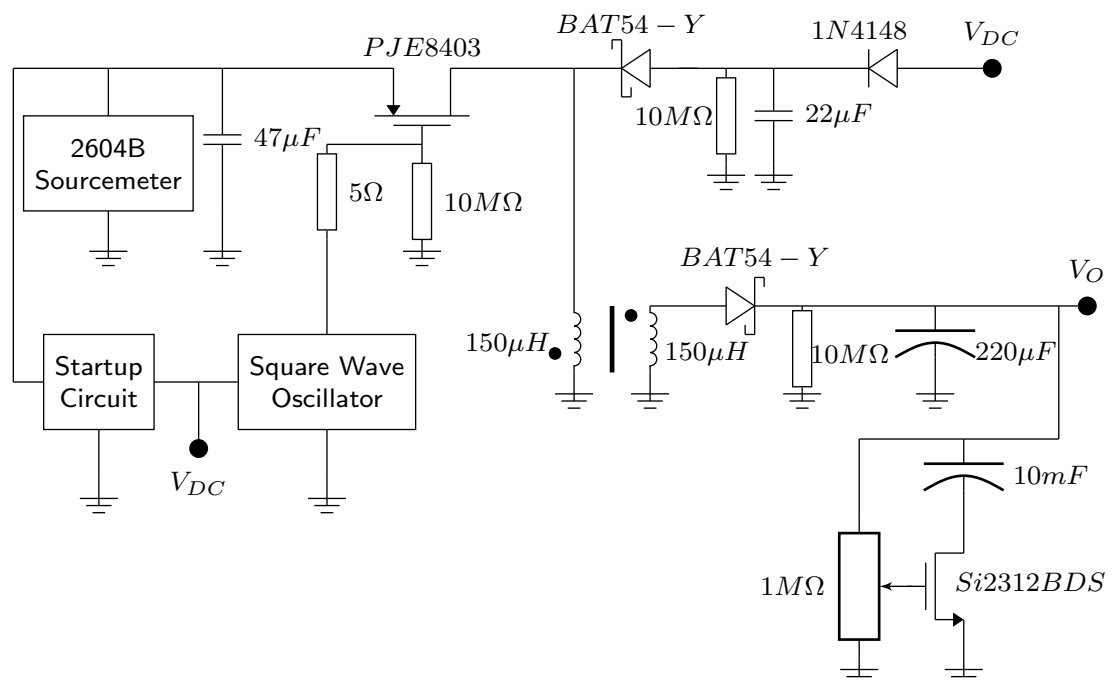


Fig. 3.29: Schematic of the custom-built DC-DC converter.

pinch-off of the JFET channel. This leads to more efficiency in the converter, as the startup stage stops draining current from the voltage source.

The second output (V_O) is a positive voltage output, and it is connected to a supercapacitor with an N-MOSFET to regulate the output voltage, as shown in [5].

To test the performance of the DC-DC converter, efficiency measurements were done. The supercapacitor was removed, and the DC-DC converter was connected to a potentiometer with a resistance $R_L = 98.4k\Omega$. Then, the input voltage source was varied from 40 mV to 100 mV in 10 mV steps. The efficiency results are shown in Figure 3.30, as well as the output voltage corresponding to each data point.

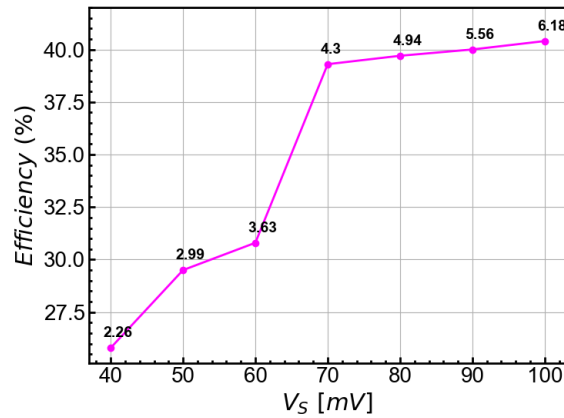


Fig. 3.30: Efficiency of the DC-DC converter with $R_L = 98.4k\Omega$. Output voltage is shown over the data points.

This DC-DC converter has not been optimized for efficiency nor impedance matching with the TEG. If the characteristics of the TEG are known beforehand, the frequency and duty of the square wave oscillator can be altered (changing its tuning capacitor and resistors) to match the impedance of both TEG and DC-DC converter. The experiment setup is shown in Figure 3.31.

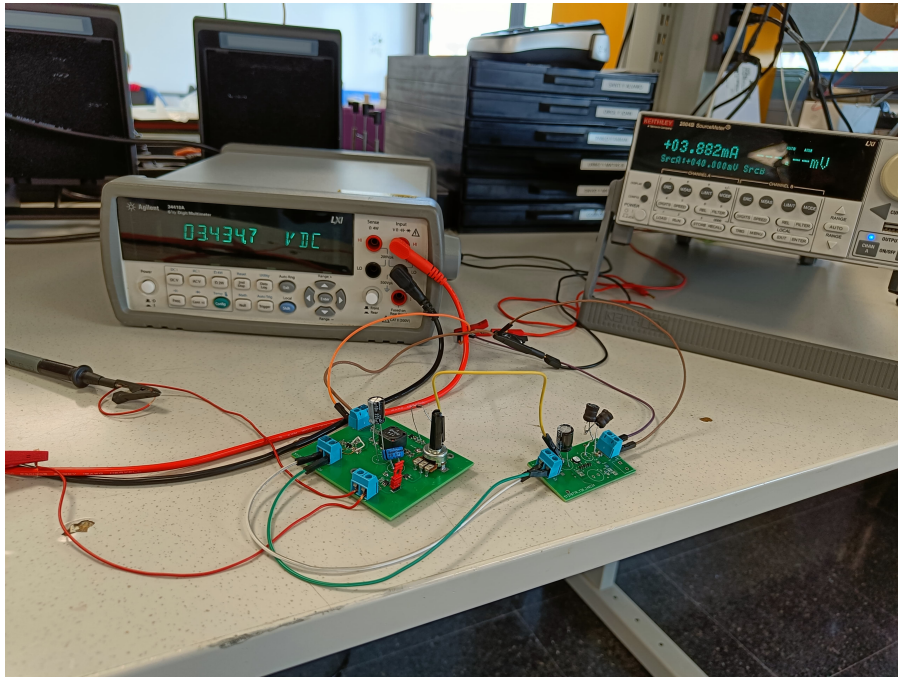


Fig. 3.31: Setup used to measure the output voltage and efficiency of the DC-DC converter.

3.4 Chapter Conclusions

As a conclusion from this chapter, the self-powered oscillator (Horates V3) was proven to be viable as a startup circuit or as a DC-DC converter in applications where efficiency is not as important as a low startup voltage. It feats a startup voltage lower than $10mV$ using only COTS components (not using hand-wound transformers or inductors), among the lower of the state-of-the art for discrete circuits, while boasting a conversion ratio in par with the state-of-the-art. In the following section, a custom DC-DC converter (Horates V4) is presented. While a basic DC-DC converter was presented in the current section, Horates V4 was designed not only to be integrated with the self-powered oscillator, but also to be controlled by a microcontroller, with the addition of an MPPT method.

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Chapter 4

Low-Voltage DC-DC Converter

4.1 Introduction

Direct Current - Direct Current (DC-DC) power converters, or switching regulators, are widely abundant as they are found in laptops, mobile phone chargers, power supplies, and a large array of devices. These converters take an unregulated DC input voltage, denoted as V_s , and transform it into a regulated output voltage, V_o . Depending on the DC-DC converter topology used, V_o can be higher or lower than V_s , and the polarity might be the same or inverted. This voltage boosting capability makes DC-DC converters attractive for low-voltage energy harvesting.

Although there is a great number of DC-DC converter topologies, and there are more still being published in the literature currently, there are a few that can be considered basic topologies, which can be separated as non-isolated topologies and isolated topologies, as shown in Figure 4.1. From the non-isolated topologies, the buck converter steps down the input voltage, so $V_o < V_s$, the boost converter steps it up, $V_o > V_s$, and the buck-boost converter can do both, while also inverting the polarity of the output, so $|V_o| > V_s \vee |V_o| < V_s$. Concerning isolated topologies, both the flyback and the forward converter can increase or decrease the input voltage while providing galvanic isolation. The forward converter is usually more efficient than the flyback converter, and it is used for applications handling higher input power.

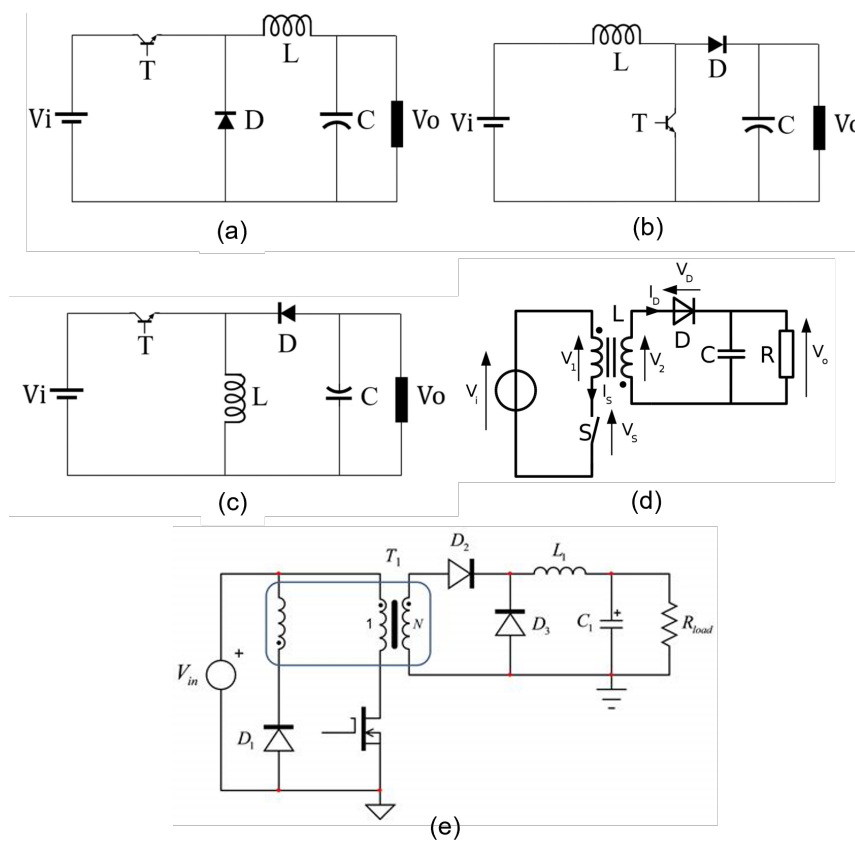


Fig. 4.1: Basic non-isolated DC-DC converter topologies: (a) Buck converter, (b) Boost converter, (c) Buck-Boost converter. Source: [1]

Basic isolated DC-DC converter topologies: (d) Flyback converter, (e) Forward converter. [2].

All of them work through the use of a switching element, like MOSFETs or Bipolar Junction Transistors (BJTs), to charge and discharge an inductor, opposite to linear regulators, where the regulation is based on a voltage drop over a transistor, which makes it less much efficient since the power dissipated, $P = (V_s - V_o) * I_{LOAD}$, is proportional to the difference between V_s and V_o . The use of a switching element forces changes in the current pathways in the circuit. Due to Faraday's Law [3], where $L \frac{dI}{dt} = V$, this change in current intensity generates a voltage opposed to it (Figure 4.2). Exploiting this effect to regulate the voltage is the basis of the way of working of DC-DC converters and allows efficient regulation.

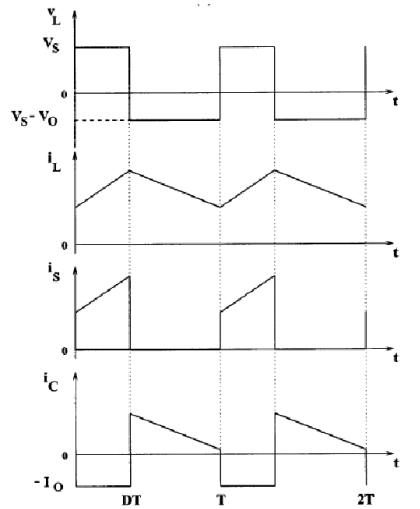


Fig. 4.2: Waveforms of a boost converter. The change in V_L can be observed along with the change in current direction. Source: [2].

These converters can work in two different modes, depending on the relationship between the average current $I_{L,AVG}$ and the peak current $I_{L,PK}$ circulating through their inductor. When this current is allowed to reach zero or change polarity, the converter is working in Discontinuous Conduction Mode (DCM). When compared to Continuous Conduction Mode (CCM), the other working mode, DCM has the following characteristics.

- Higher peak currents to deliver the same power than the other mode.
- Higher peak voltage over the components, resulting in higher stress.
- Higher efficiency at light-load operation.
- Higher undesirable voltage ripple at the output.
- Conversion ratio is a function of the load resistance.

Consequently, CCM tends to be used in applications where the load demands a high current, or when an output voltage independent of the load resistance is needed.

DC-DC converters usually have efficiencies ranging from 70% to 95%, since the process does not involve generating a resistive-like voltage drop. These high efficiencies, along with the capability of stepping up voltages, make DC-DC converters a suitable choice when extracting energy from low-voltage energy harvesting generators such as Thermoelectric Generator (TEG).

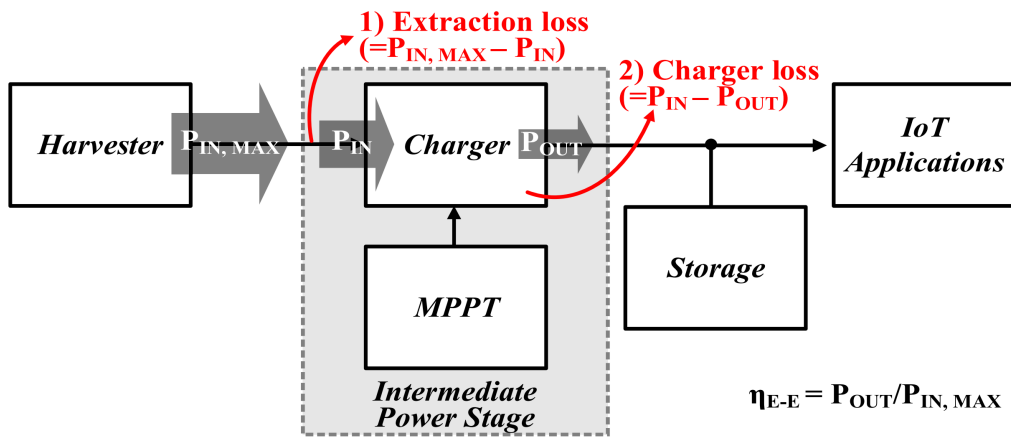


Fig. 4.3: Diagram of the system level efficiency and its components. Source: [4] © 2020 IEEE.

Prior to the discussion and analysis of this DC-DC converter, an introduction to the state of the art is done in the following section to provide the reader with an adequate background.

4.1.1 DC-DC Converters in Energy Harvesting - State of the Art

Thermoelectric generators in compact form factors or low temperatures deliver small output voltages, so DC-DC converters are needed to elevate the voltage to conventional values. In this manner, this energy can be used to power electronic devices. The topology used depends on various factors, like circuit footprint (for example, a switched-capacitor converter is much easier to escalate in a CMOS process than a boost converter, as the latter usually needs to incorporate external components such as inductors), input power, Conversion Ratio (CR), efficiency, and working voltages.

The most commonly used topologies in low-power energy harvesting applications are mainly the boost converter [5–8], and the switched-capacitor converter [9–11]. The former allows for flexible and larger CR, handles greater power, and has high efficiency, except for high CR or low output currents. Meanwhile, the latter has a fixed CR (although there are works that introduce charge pumps with reconfigurable CR [10]), handles lower power, is easier to obtain high conversion ratios due to its scalability, and is more efficient under this condition. Switching control is also easier to implement.

Some works combine both topologies, such as the work of Umaz, which uses a boost converter in parallel with three charge pumps that act as a sort of impedance matching/startup circuit. Putting N charge pumps in parallel widens the range in which the internal TEG resistance is near the input resistance of the circuit, allowing resistance matching without an active MPPT method [12]. However, the matching is far from perfect, and adding more converters is expensive and area-consuming.

Chandrarathna and Lee propose a topology that combines TBC (Transformer-Based Converter) and IBC (Inductor-Based Converter) to take advantage of their efficiencies on different ranges of input voltages, and achieve relatively high efficiency for a wider range than using them separately [13]. It uses a transformer with three coils, which allows it to have a lower turn ratio between primary and secondary during normal operation (leading to fewer losses) and a higher one for the startup. One of these coils is reutilized as an inductor for the IBC (similar to [14], where both converters share an inductor), saving in costs and circuit area.

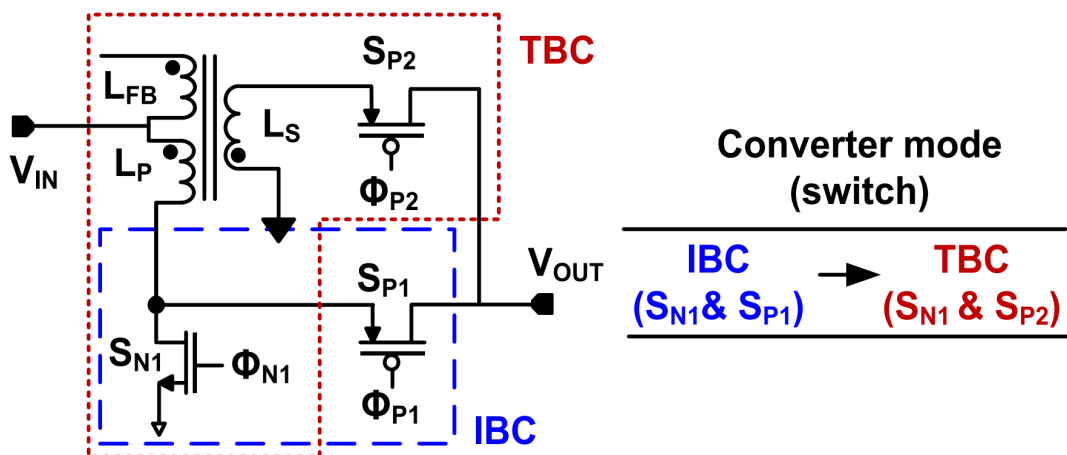


Fig. 4.4: Schematic of Chandrarathna and Lee converter. Source: [13] © 2019 IEEE.

It can be easily seen that this converter shares similarities with the one presented in this work. Although the methodology is not the same, the basis of starting the circuit by means of magnetic coupling and switch during the main phase to an "Inductor-Based Converter" is shared.

Park et al. present another converter based in an isolated topology, specifically a flyback converter. This converter uses positive feedback, enabling operation with lower startup voltages without an extra startup stage. It starts operating from an input voltage of 440 mV, using easily accessible off-the-shelf components [15].

Guan et al. present a system made with discrete components, such as the circuits being presented in this thesis, implementing Fractional Open-Circuit Voltage (FOCV) as Maximum Power Point Tracking (MPPT) and Zero Current Switching (ZCS) to improve efficiency. The novelty is that no current sensors are used to implement the ZCS, hence the power consumption is lower. To accomplish this, the on/off time of the switches is theoretically calculated for both MPPT and ZCS, using a microcontroller and measuring the OCV. The calculation is based on the ideal boost converter equations. Nevertheless, when using a microcontroller for this task, the efficiency is reduced due to its power consumption. The power consumption of the controller is around $200\mu W - 225\mu W$ [5]. The losses of the controller come mostly from the microcontroller, hence, another possible approach is to switch it for a control circuit designed in a mixed-signal Integrated Circuit (IC), reducing significantly the losses [16]. Such an approach is described in subsection 4.2.12.

Many of the converters presented can only regulate the input or the output, because to regulate both is necessary to be able to modify both the duty and the switching frequency, using PWM + PFM control [17], for example, using burst mode switching, or using two cascaded converter stages, where the first is in charge of the MPPT and the second controls the output voltage. So, when designing a converter stage, one of the design parameters is whether to use a single-stage or dual-stage converter. A single-stage converter needs fewer components, is more efficient, and if it works in burst mode, needs less time to charge the input capacitor and can deliver energy to the output for more time. Meanwhile, a dual-stage converter allows regulation of the output voltage without entering burst mode, which might result in a simpler control scheme [12].

Brogan et al. present an asynchronous single-stage converter with output voltage regulation and MPPT, using burst mode as a way to regulate the output voltage, which results in greater efficiency at light loads [18]. The mentioned work seeks to reduce the complexity of the control system, and in turn, reduce power consumption. The converter operates in burst mode, working only when V_o falls below a certain hysteresis level. This way, it avoids unnecessary consumption and regulates V_o . One drawback is that the V_{mpp} voltage is updated only at the start of every conversion cycle, hence, there can be mismatches for long periods of activity.

Lee et al. propose [19] a solution to one of burst mode drawbacks: the diminish of the conversion ratio due to a reduced duty cycle. The implementation is simple, and it consists on connecting two signals to an OR gate. The first signal, called the slam carrier, applies the full-duty during a predetermined time, boosting the conversion ratio. The second signal is the switching carrier, and has a higher frequency than the slam carrier. In this way, the converter still commutates less frequently, as expected of the burst mode, but also maintains a high effective duty, maintaining a high conversion ratio, as it is seen in Figure 4.5. The implementation of the slam method results in the efficiency at light load increasing more than 20%.

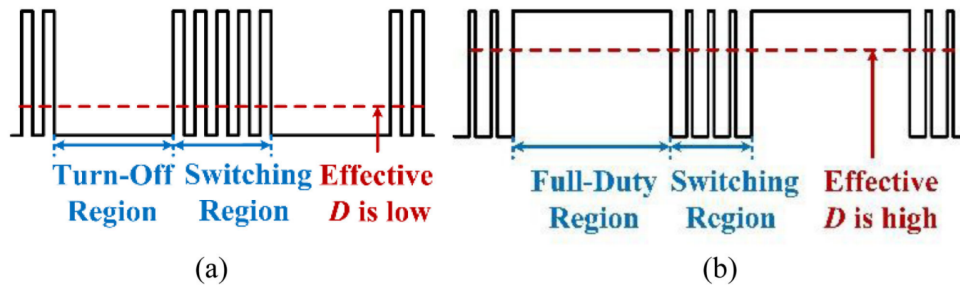


Fig. 4.5: Basis of the Slam Method. Source: [19] © 2022 IEEE.

Here should go more converters, or merge the MPPT section with the converters section.

4.1.2 MPPT methods

When the DC-DC converter is part of an energy harvester device, the system level efficiency, or end-to-end efficiency (η_{EtoE}) is determined by the product of the converter efficiency and the extraction efficiency, $\eta = \eta_{CONV} \eta_{MPPT}$, as seen in Figure 4.3 [4]. The extraction

efficiency ($\eta_{MPPT} = P_{IN,AVR}/P_{IN,MAX}$) is a ratio between the maximum available power of the generator ($P_{IN,MAX}$) and the real average extracted power $P_{IN,AVR}$, while the converter efficiency ($\eta_{CONV} = P_{OUT}/P_{IN,AVR}$) is a ratio between the input power, or average extracted power $P_{IN,AVR}$, and the output power P_{OUT} .

The exploitation of thermal energy with TEGs has some drawbacks such as [20, 21]:

- Low output voltage and power for TEGs with small areas [22].
- Poor conversion efficiency from heat to current.
- Temperature-dependent parameters.
- Organic, printed and thin-film TEGs tend to have bigger resistances than conventional ones.

Consequently, if the power delivered by the TEGs is small, the converter must extract the maximum possible quantity of energy. There are different methods to extract the maximum power available, independently of the temperature, heat, or load of the generator. These are called MPPT algorithms/methods. They are not only applied to TEG, since they are an application of the theorem of maximum power transfer, which says that to extract the maximum possible power from a generator, the input impedance of the "extracting" circuit should be equal to the complex conjugate of the output impedance of the generator, thus, $Z_L = Z_S^*$ [23]. It is worth mentioning that extraction of maximum available energy is not the same as maximum efficiency, as can be appreciated in Figure 4.6.

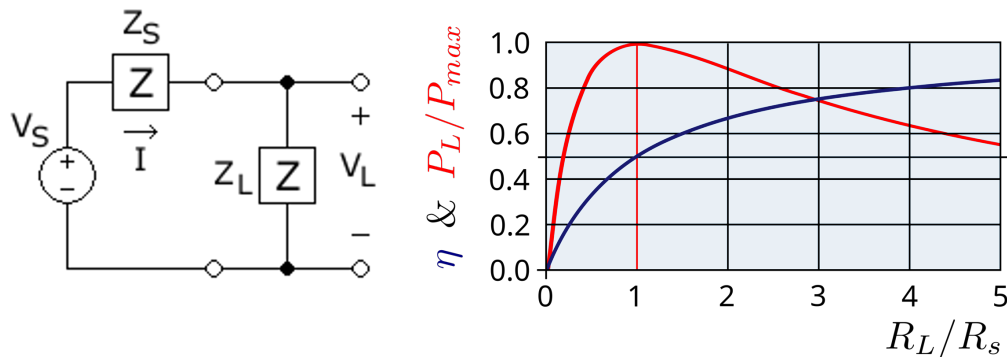


Fig. 4.6: Left: Schematic used for maximum power transfer demonstration, Right: Efficiency and extracted power versus R_S .

TEGs in steady-state can be represented by a voltage source in series with a resistor (R_{TEG}), like a Thevenin equivalent [24]. Hence, following the maximum power transfer theorem, there is a load resistance that allows the extraction of the maximum power, and it is equal to the internal resistance of the TEG. However, if the Peltier effect is considered, then the equation is modified, resulting in $R_{LOAD} = R_{TEG}\sqrt{1 + ZT}$ [25]. However, many works argue against this, stating that dependencies between the heatsink and the TEG thermal resistance that have to be included too [26, 27].

In the bibliography, we find MPPT methods such as Incremental Conductance (INC) [28], Perturbe and Observe (P&O), FOCV [29], or Fractional Short-Circuit Current (FSCC) [30]. These could be inadequate for TEGs under certain circumstances [31], or have drawbacks that must be solved. Many works describe the operation of those methods and the control systems employed to implement them [32–35]. Most of these works are exclusively oriented to Photovoltaic (PV) systems, although the basic concepts are similar if the PV panel is homogeneously illuminated, i.e., the basic case where there is only one maximum power point instead of multiple ones.

As mentioned previously, for a converter to extract the maximum available power from a TEG, its input resistance has to be equal to the output resistance of the latter. Another way to accomplish this is that $V_{in} = V_{TEG}/2$, i.e., the input voltage of the converter has to be half the Open-Circuit Voltage (OCV) of the generator, since they form a resistive divider with two equal resistances.

FOCV consists in measuring the OCV of the TEG, and consequently adapt the switching conditions (frequency and duty) to accomplish the $V_{in} = V_{TEG}/2$ condition. The main problems of this method are the TEG disconnection from the circuit, which leads to an intermittent energy transfer, and slow voltage response due to the use of capacitances, so the measured MPP could not be the same as the actual one during steady-state [31]. Furthermore, the control system can be relatively complex compared to other methods *REF*. Improvements to this method can be found in the works of Bijukumar et al. [36], Dalala et al. [37, 38] and Hou et al. [39], like estimating the open circuit voltage (OCV) without disconnecting the TEG, taking advantage of the linear characteristics of the I-V curve of TEGs. This method works altering the duty cycle to generate two different bias points for the TEG, and in this way, obtaining the slope of the I-V curve. Thereafter, both OCV and Short-Circuit Current (SCC) are calculated using the slope and the bias points (V_1, I_1) and

(V_2, I_2) in Figure 4.7), and with those points, the Maximum Power Point (MPP) is found as the middle point of the curve.

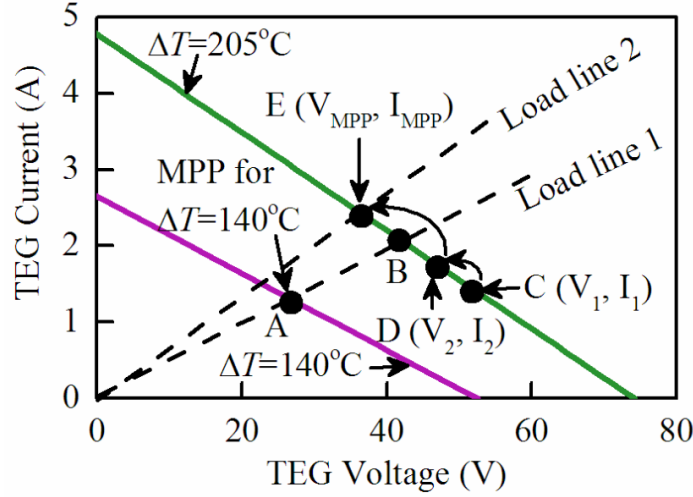


Fig. 4.7: Implementation of estimation of the MPP point through linear estimation. Source: [36] © 2018 IEEE.

Both P&O and INC work in an iterative manner, and both need to measure the input power of the converter. INC consists in measuring the $\frac{dP}{dV}$ derivative, and altering the switching conditions until it is zero, which means the peak of the power-voltage curve has been met. The sign of $\frac{dP}{dV}$ indicates on which side of the power curve the circuit is at the moment (Figure 4.8). This method might have problems in certain systems, such as non-homogeneously illuminated PV panels, since it can get stuck in a local maximum of the curve, instead of reaching the global maximum.

Meanwhile, P&O introduces a perturbation in the generator (altering the switching conditions of the converter), and then measures the input power of the converter in the current cycle $P(i)$. If the power is greater than the one measured before, thus $P(i) - P(i-1) > 0$, then the switching conditions have to be altered in the same way as before. For example, if the frequency was raised, then for the next cycle, it is raised again. This continues until $P(i) - P(i-1) \leq 0$. Once this condition is reached, it can be considered that the MPP has been reached, or the step resolution can be increased to get closer to it. Ideally, the approximation to the MPP ends when $P(i) - P(i-1) = 0$.

The problems for both methods are the same:

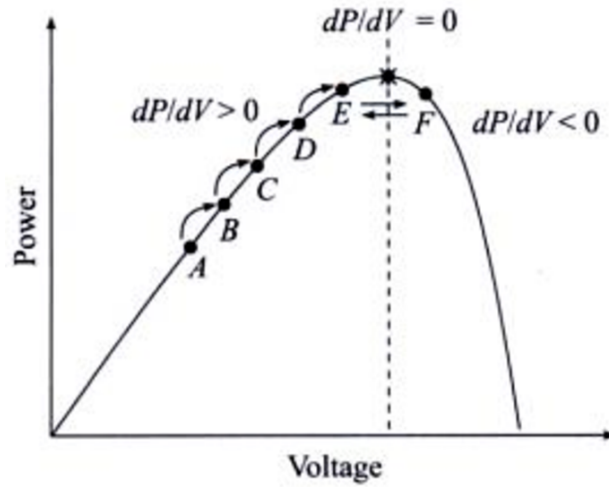


Fig. 4.8: Incremental Conductance Method. Source: [40].

- Extra power consumption due to sensors measuring current and voltage to calculate power.
- Trade-off between tracking speed and tracking resolution based on the step size used.
- Possibility of getting trapped in local maximum power points.

Little steps allow less oscillation around the MPP (although this effect is less pronounced in INC *REF*), but the capacity to follow transient changes diminishes. Meanwhile, big steps provoke more oscillation but allow faster transient tracking. A possible solution is using an algorithm that detects the oscillation and stops the search, or using adaptive steps instead of fixed ones [39, 41].

Some works propose not to use MPPT to improve end-to-end efficiency on systems whose converter efficiency is very variable with the input voltage. In these cases, the system MPP does not usually coincide with the MPP of the TEG, so an MPPT method that does not account for that, will have suboptimal performance [31, 42]. Next, some of the most recent MPPT methods presented in the literature are analyzed.

State of the Art of MPPT methods

Hou and Chen present an MPPT method that works adjusting the duty cycle of a boost converter to match its input resistance R_{LOAD} to R_{TEG} [39]. To accomplish this, it has two working modes. In the first one, R_{TEG} is estimated without disconnecting the TEG like in FOCV. Instead, it uses linear estimation like the previously mentioned work of Bijukumar et al. [36]. Afterward, the microcontroller consults a Look-up Table (LUT) to choose the corresponding duty cycle for the boost converter such as that $R_{LOAD} = R_{TEG}$. The second working mode is used as a fine adjustment, and consists of a modified P&O called Observation and self-optimization (O&SO) (O&SO) where the oscillations near the MPP are eliminated. To this end, the algorithm stops making adjustments when it detects that the coefficient R_{LOAD}/R_{TEG} is lower than a predetermined value. This combination of coarse and fine adjustment allows for transient tracking without oscillations near MPP, giving both tracking speed and precision.

In Miao et al. work, the input power variation can be estimated through t_{mp} (conduction time of the high-side P-type MOSFET). Consequently, P&O is implemented with t_{mp} and V_{out} as control variables instead of the input voltage and current. This type of control is easy to implement, provides an adaptive step for P&O, and allows it to work with a large range of input resistances [16]. It also counts with a ZCS control scheme, based on a mixed-signal circuit. The polarity of the high-side MOSFET voltage allows the controller to know if the commutation was done early or late. This voltage, in turn, controls the direction in which a binary-coded decimal counter counts. Consequently, this counter controls how many current mirrors of an array are connected to a resistor R_2 . The voltage over R_2 thus determines the conduction time of the P-type MOSFET.

Some works in the literature are oriented to reducing the number of sensors used, mainly the ones that measure current due to higher power consumption when compared to voltage sensors. In Bond et al. work [43], P&O is implemented by sensing only voltage. Through the ON-OFF time of the MOSFET, which is measured using a microcontroller timer, the variation in input power is estimated, and P&O is utilized to generate a reference voltage that alters the duty cycle, converging to the MPP.

Liu et al. propose a P&O method that does not utilize current sensors or microcontrollers. Input voltage is converted to current through an operational amplifier and a resistance. After

that, a perturbation is applied to the MOSFET conduction time (t_{on}), and the input voltage is converted the same way as before. Comparing both currents, the system knows whether it has to increase or decrease t_{on} .

When designing an energy harvester, it is important to remember that the focus must be on the end-to-end efficiency, i.e., the system efficiency, not on the extraction efficiency. Thus, the power extracted from the TEG must be considered, but also the controller losses, or the converter efficiency, which is dependent on its input voltage [31, 44].

Jeong et al. work, instead, seeks a balance between extraction efficiency and converter efficiency [4]. The input voltage ripple, inherent to the boost converter topology, generates a temporal mismatching which diminishes extraction efficiency Figure 4.9.

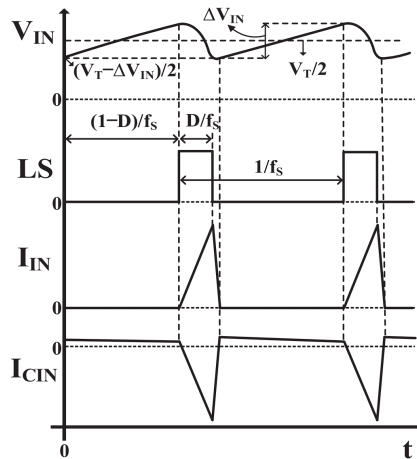


Fig. 4.9: Ripple in V_{in} due to the converter current consumption. Source: [4] © 2020 IEEE.

This ripple is inversely proportional to the switching frequency while switching losses are directly proportional. Therefore, the idea is to reach an optimal frequency, such that the sum of the losses is the minimum possible. [14] proposes a double conversion path architecture, where an asynchronous converter is used to start at lower voltages (during the startup phase), while a synchronous converter is used during normal operation to achieve better efficiency. Both share the inductor, thus allowing a reduced circuit size. The MPPT method used is impedance matching, with two control variables (duty cycle and switching frequency). This allows the circuit to have maximum power transfer at the input and maximum transfer power to the output, as in the circuit mentioned previously. The output voltage cannot be regulated, due to the duty cycle not being fixed, since that would lead to a non-optimal switching

frequency). If output voltage regulation is desirable, burst mode can be implemented [18] or the addition of a regulator cascaded with the converter.

Printed and thin-film TEGs usually have bigger resistances than the conventional ones, ranging from hundreds to thousands of Ohm [45–47]. This is a factor to account for when designing the converter because it can greatly impact both the startup of the converter and its efficiency, needing MPPT methods specifically tailored to high-resistance sources.

Along these lines, Xu et al. present a circuit with MPPT Internal Resistance Adaptive (IRA) [17]. The idea is to use FOCV but add an adaptive delay to the voltage comparison between V_{in} and V_{mpp} (V_{mpp} must be $V_{OC}/2$). The duration of the delay is inversely proportional to the product between the comparison time and the input voltage. This achieves greater efficiency than the traditional comparator, given that it avoids unnecessary switching when the current received by the input capacitor is small, at the cost of more ripple on the input voltage. Another advantage is that it can also work with a greater range of input power and resistances.

Wang et al. develop a converter for high input resistance TEGs, with ZCS and using FOCV as MPPT method. It works in a burst-like manner (i.e., not in a continuous manner), allowing it to be compatible with high-resistance TEGs, and it has a current control scheme that allows it to minimize the losses of the converter stage [48].

Table 4.1 shows a comparison between some of the MPPT method implementations found in literature, as a way to compare the power consumption of the controller circuit in integrated and discrete circuits. The table shows the power consumption of the controller used to implement the method, as well as if the circuit is integrated or discrete.

| Reference | V_{IN} range/ V_{INMIN} | R_{IN} | Control Power Cons. | Integrated |
|-----------|---|------------------------------|---------------------------|------------|
| [5] | 150 mV - 1 V | 10 Ω - 47 Ω | $\approx 200 - 225 \mu W$ | Discrete |
| [49] | 2 V - 7.2 V | 1 k Ω - 30 k Ω | 9 μW | Integrated |
| [4] | 500 mV (cold-start) 200 mV (after startup) | 1.68 k Ω † | 6 μW * | Integrated |
| [9] | 20 mV - 450 mV 38 mV (startup) | N/A | 1.26 μW | Integrated |

Table 4.1: MPPT comparison. † Value used for simulations. *: Minimum Input Power.

4.2 Design of a Custom DC-DC Converter (Horates V5)

The DC-DC converter designed in this work (Figure 4.10), called Horates V5 from now on, constitutes an improvement over the previous iteration shown in section 3.3.4. It is based on the boost and flyback topologies, and it uses two 1:1 coupled inductors to magnetically couple two independent boost converters. Furthermore, it integrates a microcontroller to implement MPPT and control the voltage regulation, as well as the energy storage.

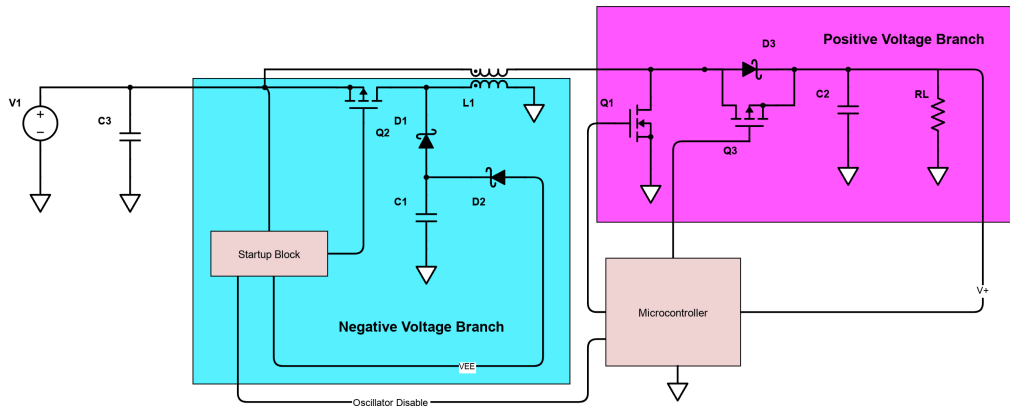


Fig. 4.10: DC-DC converter (Horates V5) designed for this work.

4.2.1 Theoretical Description

During the startup phase, it operates similarly to a flyback converter. The startup block commutates $Q2$, storing energy in the primary of $L1$ during the ON-time. During the OFF-time, the energy is released in two ways. Firstly, the energy is transferred through the secondary due to the magnetic coupling between $L1$ inductors. Since their polarity is reversed, it charges the output capacitor with positive voltage, hence the term “positive voltage branch”. Secondly, the energy from the primary of $L1$ is discharged through $D1$ to charge $C1$ with a negative voltage. The voltage of this “negative voltage branch” is then supplied to the startup block through the diode $D2$.

Once the output of the positive branch reaches around $2V$, the microcontroller starts operating and takes control of the converter, leaving the startup phase. In this “main phase”, the startup block is turned off, and the commutation is now done through $Q1$, and the positive branch

starts operating as a proper boost converter, with the secondary of $L1$ as its main inductor. The primary is still magnetically coupled, but the startup stage is isolated through an N-MOSFET, to avoid further consumption from the negative branch.

The first boost converter, or the negative branch, as it is named in Figure 4.10, is connected to the startup block through a diode (to avoid affecting the startup voltage of the latter). As has been seen in the previous section, the startup block consists of a startup oscillator (Horates V4), a square wave oscillator, and in this new iteration, an extra block called “Output Isolation Block” (refer to section 4.2.5). Since the output voltage of this startup block is negative voltage in respect to GND, a P-Channel MOSFET is used as the switching element, as an N-channel would need a positive voltage to be switched. It is important to note that using a P-channel MOSFET as it is connected in this diagram is only possible thanks to having a low V_{in} , since the source is directly tied to it, but it is not enough to surpass the threshold voltage V_{TH} .

This negative branch has more than one function:

1. Once it starts working, since it is connected to the startup block, it raises the voltage used for switching the P-MOSFET, leading to a lower R_{DSon} , and in turn, more efficiency. This means that the negative branch replaces the startup circuit at this point, for a more efficient conversion.
2. The feedback to the startup block also helps with reducing the current that block consumes, since the gate of its N-JFET get polarized even more negative than before.
3. Since the negative branch is magnetically coupled to the positive branch, its output starts charging with positive voltage too.

In the next subsections, the design criteria for the converter is described along with the description of each block present in Figure 4.10.

4.2.2 Layout considerations

The performance of a DC-DC converter is greatly influenced by its PCB layout, which makes it a crucial part of the design. To create an optimum layout, specific guidelines must be followed. Following these guidelines will help minimize the impact of layout on circuit performance, and reducing Electromagnetic Interference (EMI) and noise coupling. These guidelines are well-established and applicable to all DC-DC converters, although specific details may vary between different topologies due to the pathways taken by high currents.

Since the circuit presented in this thesis can be thought of as two boost converters working in parallel, some of the basic layout rules for boost converters are presented [50]:

1. Minimize loop areas

- Minimize the area of critical loops, since they act as parasitic inductances. In high $\frac{di}{dt}$ nodes, these loops radiate magnetic fields, and generate ringing and voltage spikes. For a boost converter, there are high frequency switching currents along the inductor, transistor and diode. Minimizing this loop area reduces parasitic inductance, which helps in reducing noise and EMI.
- Minimize the length of high-current paths. For the boost converter, for continuous current, this is the input path, since the current at the output is lower.
- Placing components close is a good way to maintain short traces and small loops. Filter capacitors should be as near as possible to the circuits at their outputs.
- Components should be placed as close as possible to the switching node, and connected by short and wide traces.

2. Optimize Ground Plane Layout

- Use a solid, uninterrupted ground plane on one layer of the PCB. This provides a low-impedance return path for switching currents, reducing noise and improving thermal performance.
- Ground connections of the power stage of the converter should be tied together at a single point to avoid ground loops.

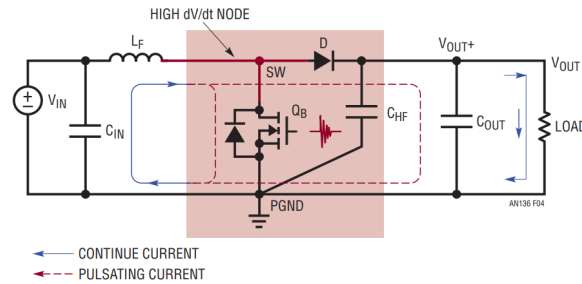


Figure 4. Continuous and Pulsating Current Paths of a Boost Converter

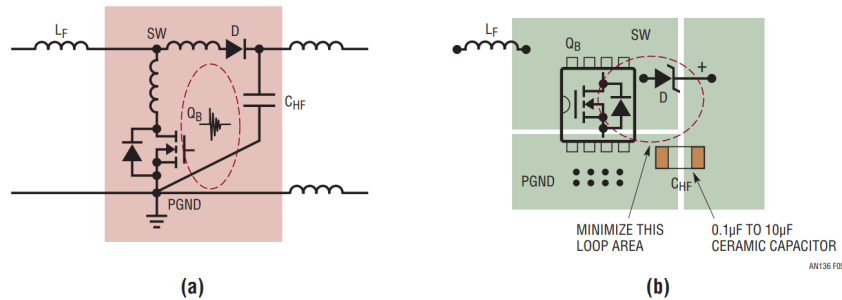


Figure 5. Minimize the High di/dt Loop Area in the Boost Converter.
(a) High di/dt Loop (Hot Loop) and its Parasitic PCB Inductors, (b) Layout Example

Fig. 4.11: Boost critical current paths. Source: [50].

- In the case of this converter, an extra ground plane separates the top face components from the bottom face ones. This ground plane gives extra isolation from the EMI.

3. Thermal Management

- Power-conducting devices, such as MOSFETs and diodes, should be connected to wide traces, pads or copper pours, to dissipate heat effectively. In the case of the converter presented in this work, the thermal management is not as crucial since the power handled is low.
- Use copper pours connected to GND to help dissipate heat from power components.
- For multi-layer boards, use thermal vias under heat-generating components to transfer heat to other layers. This rule does not apply neither.

4. Capacitor Placement

- Use low ESR capacitors for input and output to reduce voltage ripple and switching noise. They should be as close as possible to the components conforming the switching node.

5. Traces Layout

- Ensure that traces carrying high current are wide enough to handle the current without excessive voltage drop or heating.
- Avoid placing any sensitive signals or components near the inductor due to its radiating magnetic field.
- Avoid routing traces directly under the inductor. In the case of this work, traces that inevitably had to pass below the inductors due to area restrictions, were laid out over the bottom layer, to ensure isolation thanks to the two ground planes.
- If possible, isolate the power stage from the control stage of the converter to prevent noise from coupling into sensitive control circuitry.
- If possible, vias should be avoided in critical traces, since they add extra inductance and resistance.

Some of the rules are further elaborated next to better understand their causes and effects. Afterwards, the layout design for the converter, as outlined in this thesis, is presented and compared with these rules.

Ground Planes Isolation

Considering that the converter has a microcontroller in charge of the switching control, an area of the PCB is dedicated exclusively to this component, as well as the control circuits. By separating the ground planes, the goal is to minimize the coupling due to high-frequency signals, such as the signals from the switching node from the converter.

Figure 4.12 shows a guideline for the separation of circuits on a PCB. It is based on the categorization of circuits as digital, analog, or high current. The PCB designed in this thesis incorporates all three types of circuits, and it utilizes three power grounds. However, it is important to note that these power grounds are not strictly separated based on the aforementioned criteria.

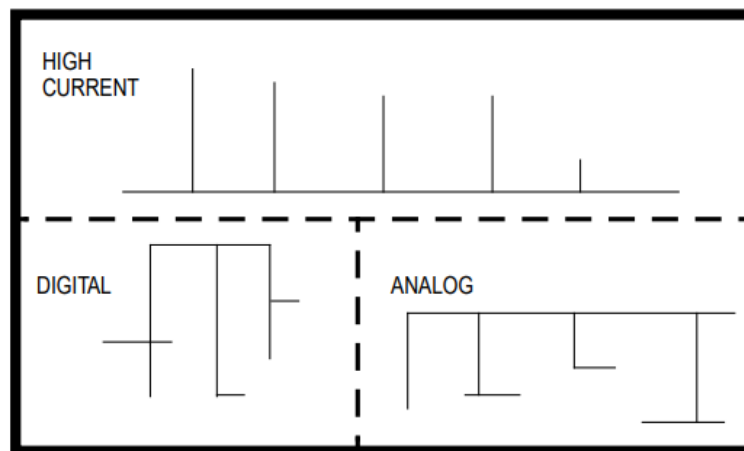


Fig. 4.12: Correct isolation of circuits in a PCB to minimize noise coupling. Source: [51].

Ground Plane Breaks

Interrupting the ground plane creates voltage differences between the opposite points of the break, as well as a longer return path for the current (which implies higher inductance and greater susceptibility to external magnetic fields).

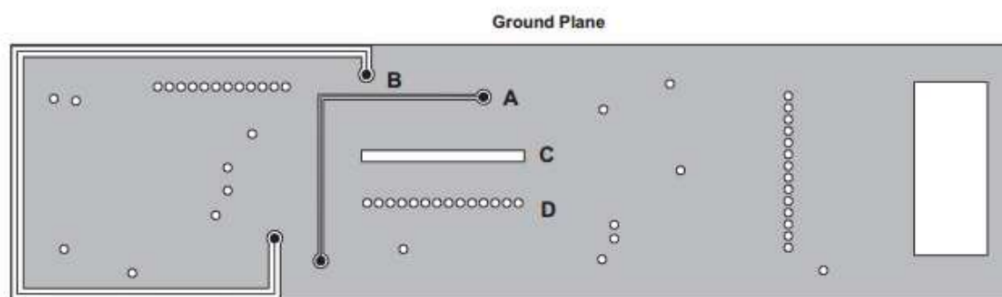


Figure 2. Ground Plane Trace Styles

Fig. 4.13: Different styles of ground plane interruptions. Source: [52].

Figure 4.13 shows four different styles of ground plane interruptions. Curve type C is simply the absence of copper, and is the worst-case scenario among those shown. Curve type D is an improvement over curve type C, leaving small spaces for current conduction from one side to the other. Curve type A is a trace across the ground plane, almost entirely separating its left side from its right side. A more favorable alternative for the design is curve B, which by going around the board practically does not interrupt conduction along the plane.

Current Return Paths

Similar to the previous point, the effect of different current return paths when there is a ground plane is analyzed.

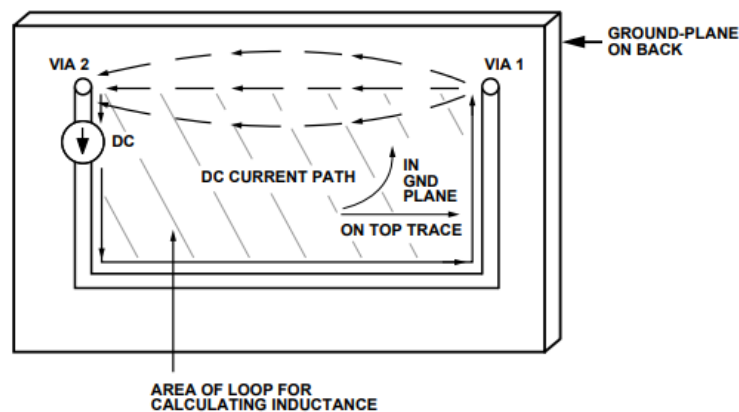


Figure 12.61: DC Current Flow for Figure 12.60

Fig. 4.14: Current return path for DC. Source: [53].

The direct current flows from via 1 to via 2 through the path of least resistance, which coincides with the shortest distance between the two, through the ground plane. In Figure 4.14, the loop area is shown in a shaded pattern.

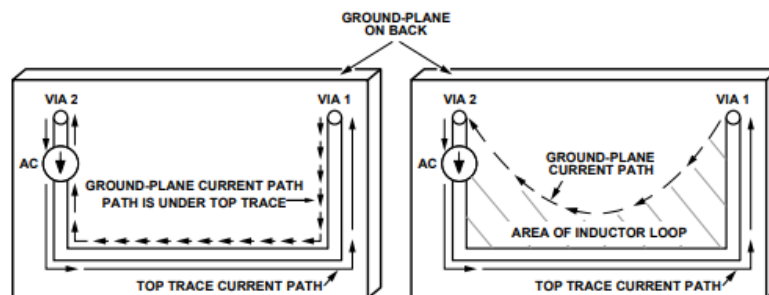


Figure 12.63: AC Current Path Without (left) and with (right) Resistance in the Ground Plane

Fig. 4.15: Current return path for AC. Source: [53].

The alternating current does not flow through the path of least resistance, but through the path of least impedance, which as seen in figure 4.15, corresponds to the path right below the trace of the top layer. This holds true in the case of a perfect and resistance-free ground

plane. However, when considering the effect of resistance, the return path becomes an arc between the two vias. This generates a larger area for the current loop, greatly increasing inductance and making the circuit more susceptible to the influence of external magnetic fields. Therefore, when designing traces, the goal is to minimize the area between the two vias as much as possible, as shown in Figure 4.16.

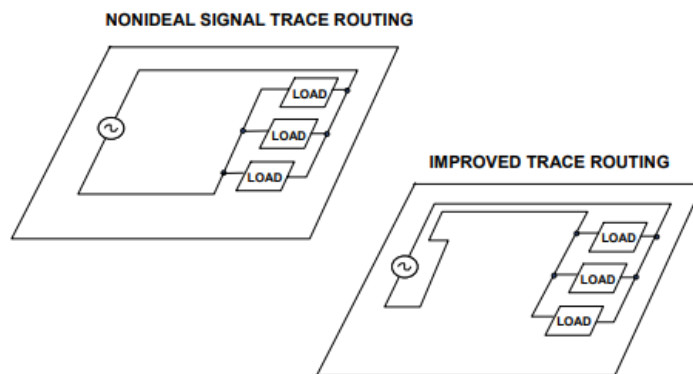


Figure 12.19: Nonideal and Improved Signal Trace Routing

Fig. 4.16: Non-ideal design vs. improved design. Source: [54].

4.2.3 Layout of the designed DC-DC converter

The PCB is designed using a 4-layer process to make the layout less complex and constrained. Using a 4-layer PCB allows one to design the board in a smaller area because components can be placed on both sides of the board.

Some of the main advantages of designing in a 4-layer process are:

1. Components are placed over both faces of the board. This allows fitting the circuit in a reduced area.
2. Control signals from the Microcontroller Unit (MCU) and power signals can be properly isolated.
3. The layout is less convoluted, which leads to wider and shorter traces, reducing both parasitic inductance and resistance.

4. The two middle layers are used for ground planes. This results in reduction of EMI and noise coupling between the top face and the bottom face. It also helps reducing parasitic inductance and resistance in critical traces, since it makes the return path for the current shorter, in cases where the layout is too constrained to fit the traces in the same layer.
5. It allows for clean distribution of power, as the negative voltage can go along the bottom layer, while the positive voltage goes along the top layer.

In Figure 4.17 and Figure 4.18, the layout of the bottom and top layer can be observed. It can also be appreciated that the ground plane is split in three local ground planes, where each connection is made at the lowest impedance point, just after the filter capacitors to avoid introducing extra noise into the other ground planes. The top-left ground plane corresponds to the DC-DC converter, and its function is to provide short and narrow paths back for critical currents. The rightmost ground plane corresponds to the microcontroller and control circuits in general, supplied by positive voltage. Lastly, the left-bottom ground plane mainly corresponds to the start block, which is supplied purely by negative voltage. This arrangement allows for minimal noise coupling between the different circuits, as well as an efficient layout and power distribution.

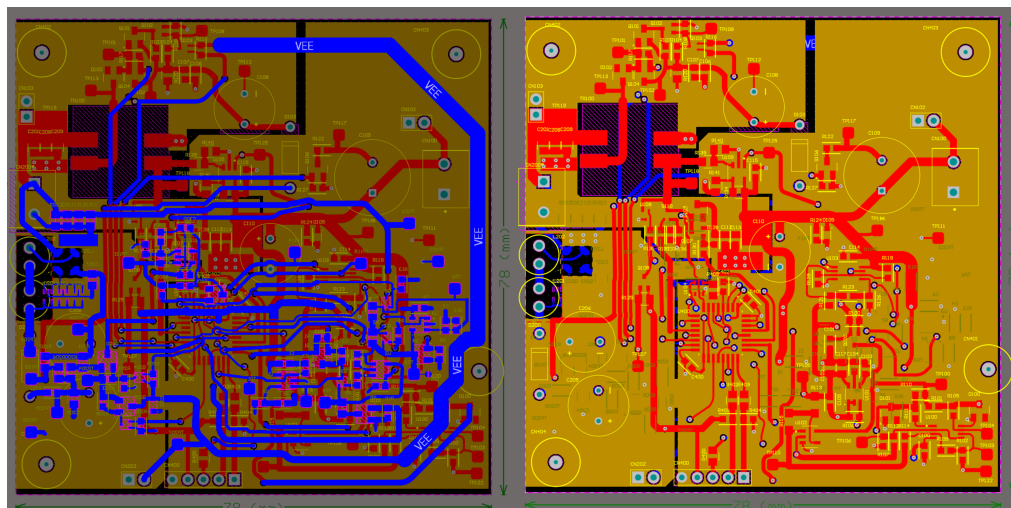


Fig. 4.17: PCB Layout. Left: Bottom layer, Right: Top layer.

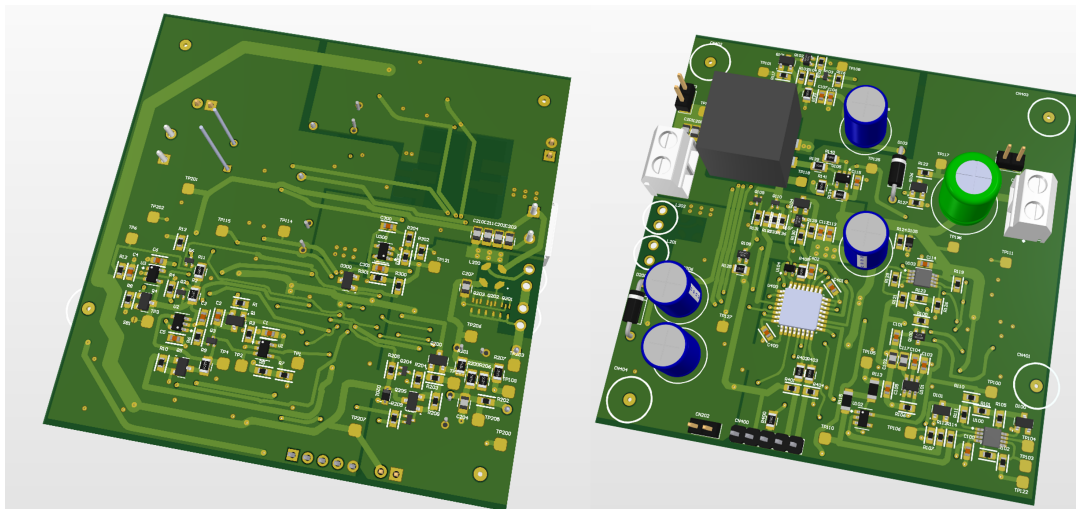


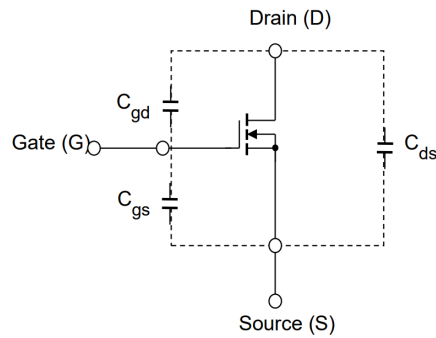
Fig. 4.18: PCB 3D view. Left: Bottom layer, Right: Top layer.

4.2.4 Components selection criteria

MOSFET selection - C_{oss} and $R_{DS(on)}$ criteria

Regarding component selection, while the criteria to choose the MOSFET usually is to choose the one with less $R_{DS(on)}$ to reduce conduction losses, capacitances should also be taken into account (Figure 4.19). While the gate capacitance is usually considered, as its part of the switching losses, the output capacitance started being the focus of study only in recent years with the advent of GaN MOSFETs [55].

For this DC-DC converter, Horates V5, while $R_{DS(on)}$ is still a crucial parameter to determine efficiency, C_{oss} was also taken into account, due to the work of Nikoo et al. [56]. In this work, it is explained that for high conversion ratio DC-DC converters, the parameters R_{ind} , $R_{DS(on)}$, C_{oss} and L , all have an impact on the efficiency, due to the C_{oss} capacitor limiting the maximum conversion ratio of the circuit, and storing energy that should go to the output instead. This energy stored in C_{oss} can be discharged efficiently through resonance with L and ZVS switching, but if certain conditions are not met, then it is discharged through the MOSFET channel, lowering the efficiency of the circuit (Figure 4.20).



Input capacitance (C_{iss}) = $C_{gd} + C_{gs}$

Output capacitance (C_{oss}) = $C_{ds} + C_{gd}$

Reverse transfer capacitance (C_{rss}) = C_{gd}

Fig. 4.19: Capacitances of a MOSFET.

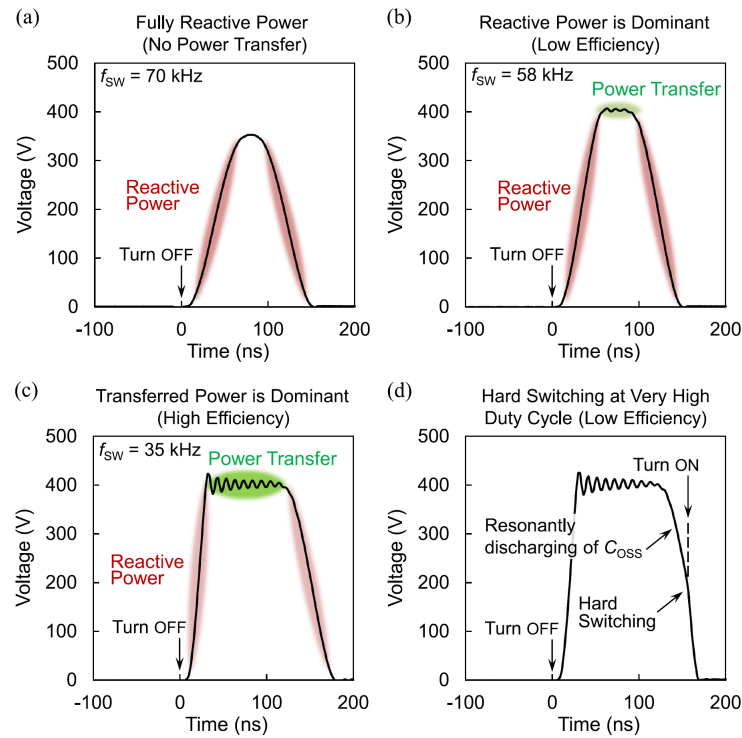


Fig. 4.20: Differences in energy transfer for different conversion ratios. Source: [56] © 2020 IEEE

Inductor

The inductor was picked such as that two conditions were met. The time constant ($\tau = L/R$) should be much greater than the T_{on} used, for efficient charging. The inductor should have an inductance small enough such that it is always working in DCM. Hence, there is a tradeoff between both.

Another factor to take into account is the fact that the inductor will affect the duty cycle of the circuit. As will be introduced in the section describing the MPPT method used, the optimal or "MPP" frequency is:

$$f_{s_{opt}} = \frac{V_{TEG}^2}{2I_{peak}^2 L R_{TEG}} \quad (4.1)$$

$$f_{s_{opt}} = \frac{V_{TEG}^2 L}{2V_{IN}^2 T_{on}^2 R_{TEG}} \quad (4.2)$$

As such, it can be observed that for a fixed T_{on} , a higher L raises the optimum frequency, raising the duty cycle too, since $\delta = T_{on}/T_s$. This is a crucial point, considering the boost converter needs a high conversion ratio to amplify the low input voltage. Although counterintuitive, in this case, the duty cycle is inversely proportional to T_{on} . Additionally, the switching frequency f_s is inversely proportional to T_{on}^2 , so using a higher inductance permits maintaining the duty cycle while raising T_{on} and significantly reducing f_s .

Diode/Synchronous Rectifier

The rectifier diode is chosen to have the lowest possible V_F , to reduce conduction losses. This rises the leakage current, but the losses are not considerable. Meanwhile, the synchronous rectifier is chosen to have the lowest possible $R_{DS,on}$, while maintaining V_{TH} in a range attainable for the microcontroller. Hence, a logic-level transistor is used.

4.2.5 Startup Stage

The startup stage consists of the self-powered oscillator topology (Horates V4) presented in section 3.3, cascaded with an output isolation block and a square wave oscillator, as appreciated in Figure 4.21.

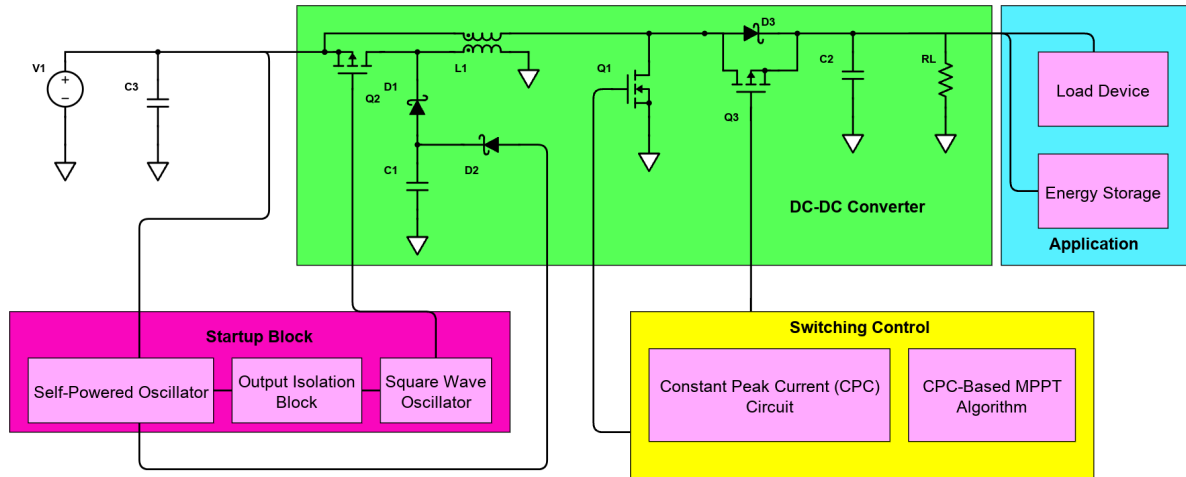


Fig. 4.21: Schematic of the converter.

The startup stage counts with two outputs. In this converter, the output with negative voltage rectifier is used since it has two times the amplification of the other output. The voltage generated by this output is stored in a ceramic capacitor to reduce the loading on the output. For the same reason, to avoid loading the output, since this reduces the maximum available voltage, an output isolation block is implemented, and described next. Lastly, the startup oscillator and output isolator blocks supply power to a square wave oscillator, in charge of switching the P-channel MOSFET Q_2 .

Isolation and Shutdown

As mentioned in section 3.3, for the oscillator to reach the maximum possible output voltage, an extra circuit is used to isolate the output from the load, while the output capacitor is still charging. To this end, load switch ICs were first used in this design, as they count with an enable pin to control when the switch is closed or open, and have a very low power consumption ($\leq 1\mu A$).

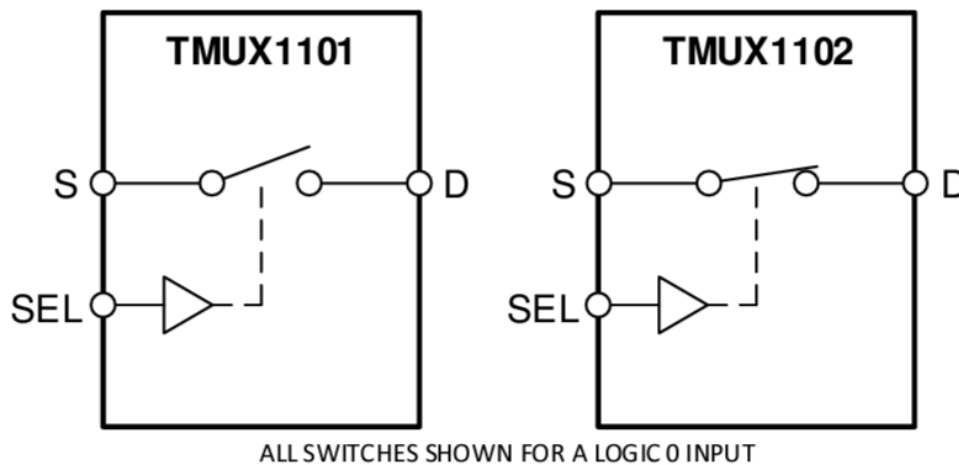


Fig. 4.22: Load switch as one of the alternatives.

Nonetheless, this proved to be an ineffective solution, as the SEL pin (Figure 4.22) expects a digital signal, with fast rise and fall times. But in this case, the output of the oscillator rises slowly, and the SEL input ends in an undetermined state, leading to erratic behavior.

The next iteration of the circuit consisted of an N-type MOSFET, with its gate connected to an RC circuit (Figure 4.23). The circuit works as follows: initially, the capacitor $C2$ is discharged, and acts as a near short-circuit during the transient stage of the circuit. Thus, while the oscillator output is rising, both source and gate are at almost the same voltage. Then, the capacitor starts charging slowly through $R2$, generating a positive V_{GS} voltage, which, when $V_{GS} > V_{TH}$, leads to conduction through $M1$. This connects the startup oscillator to the square wave oscillator avoiding loading the output during the initial stages. As a final consideration, both $C2$ and $R2$ control the isolation time, but $R2$ should be as big as possible, as it is loading the oscillator output during the starting stage, but low enough for a quick startup.

In the Figure 4.24, the simulation shows how the voltage over $R3$ (the square wave oscillator input) does not appear until a determined time passed.

Once the microcontroller is powered, the square wave oscillator should be turned off, as to avoid short-circuits between the two MOSFETs working as switching elements of the DC-DC converter. To this end, an N-channel MOSFET $M2$, controlled by the microcontroller,

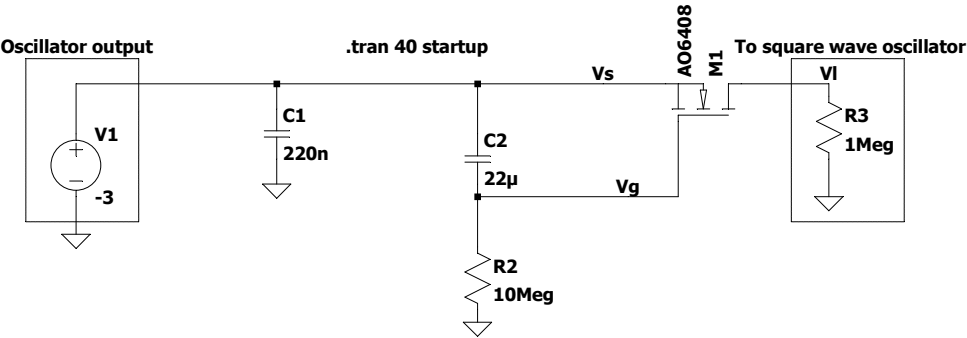


Fig. 4.23: Schematic of the circuit used for isolation of the oscillator circuit output.

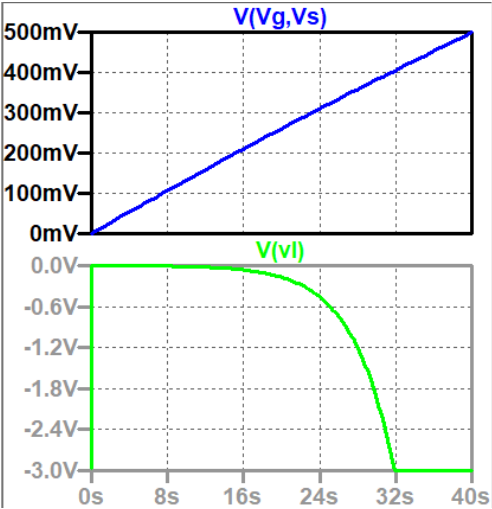


Fig. 4.24: Transient simulation for the previous circuit.

was added to the isolation circuit (Figure 4.25). This transistor pulls the gate of $M1$ to V_{EE} , cutting the power supply to the square wave oscillator.

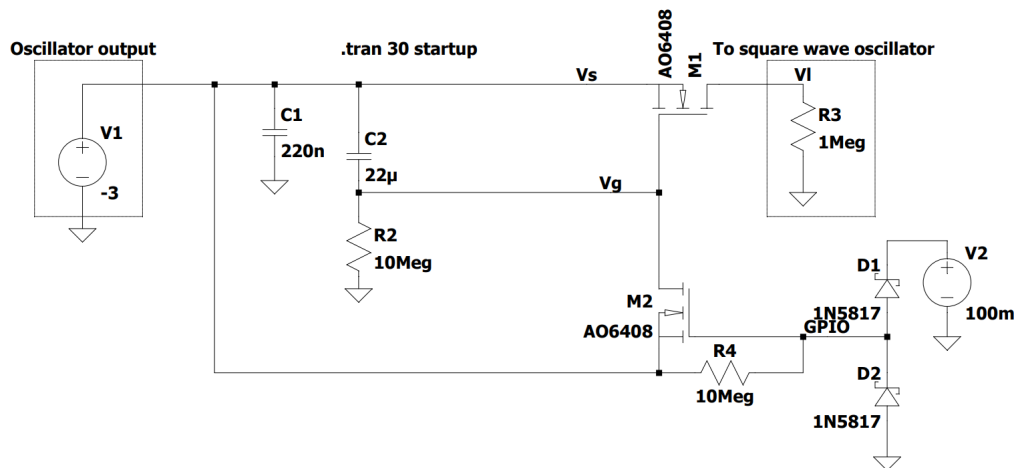


Fig. 4.25: Schematic of the circuit used for isolation of the oscillator circuit output with added N-Channel MOSFET for output disable.

However, the microcontroller power rails are connected to $V+$ and GND , and therefore, the protection diodes of each pin of the MCU are connected to the same rails (Figure 4.26) [57]. This leads to the gate of $M2$ not being pulled down by the resistor $R4$, since the protection diode connected to GND ends in direct mode, and hence, connecting the gate of $M2$ to GND too.

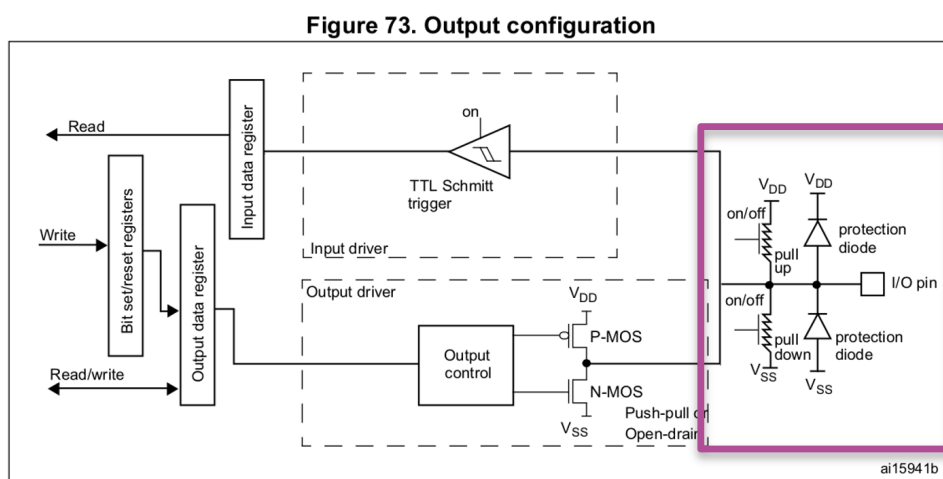


Fig. 4.26: Structure of input stage of an MCU pin.

This leads to the DC-DC converter circuit never leaving the startup stage, since when V_{EE} builds up, $M2$ starts conducting and $M1$ never closes, as can be seen in Figure 4.27.

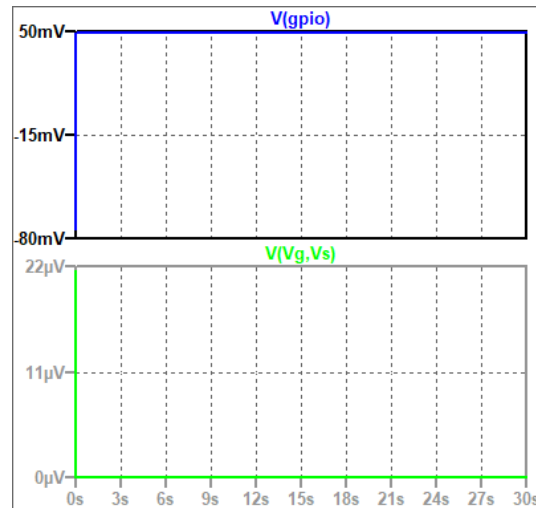


Fig. 4.27: Plot of the circuit used for isolation of the oscillator circuit output with added N-Channel MOSFET for output disable.

To fix this issue, a P-MOSFET is added to the gate of $M2$ as a buffer (Figure 4.28). With this modification, the MCU can put the gate of $M2$ to $V+$ without having issues during startup. When $M2$ has to be turned off, $M3$ is opened, and the gate of $M2$ is discharged through $R4$.

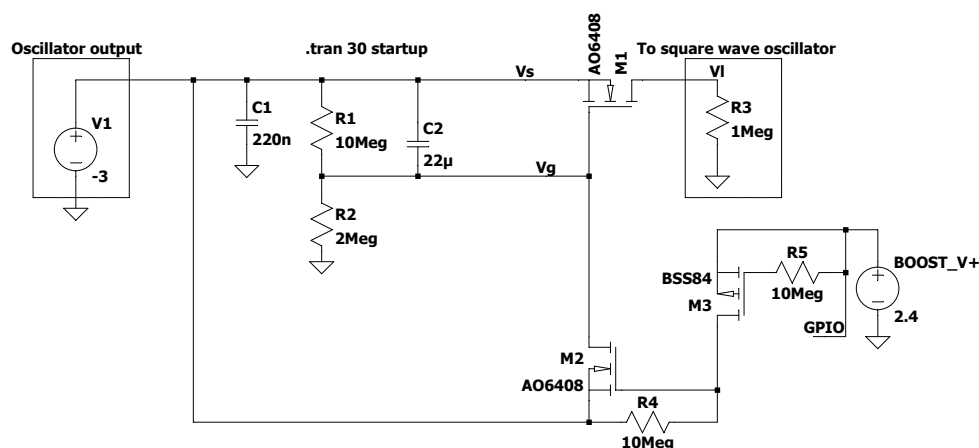


Fig. 4.28: Schematic of the circuit used for isolation of the oscillator circuit output with added P-Channel MOSFET for output disable.

As a final improvement, the delay circuit with the resistive divider and the charging capacitor was replaced with an ultra-low power voltage supervisor (XC6136 [58]). The delay circuit

final design is as presented in Figure 4.29 (transistors M1, M2 and M3 from previous figures are not shown, but are still part of the circuit). The voltage supervisor outputs V_{IN} Figure 4.29 when $V_{IN} > 2V$, and $0V$ when $V_{IN} < 2V$. The schematic of the voltage supervisor, provided in its datasheet, is presented in the next subsection, along with the method used to isolate the DC-DC converter output from the microcontroller.

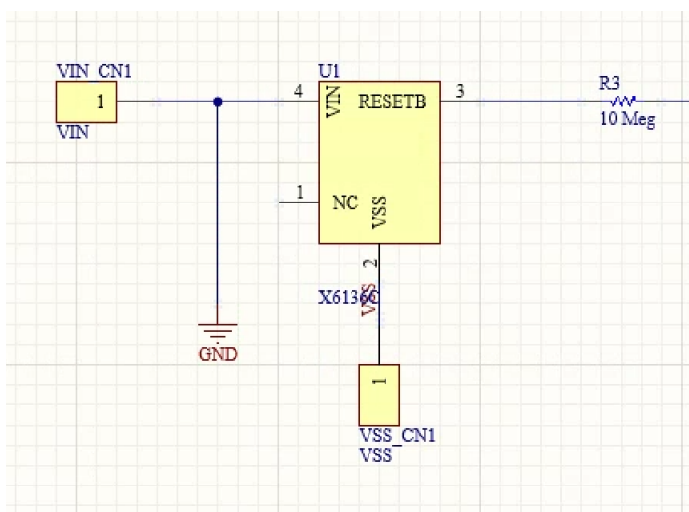


Fig. 4.29: Voltage supervisor replacing the delay circuit.

4.2.6 Isolation of the Microcontroller

As with the startup circuit, the DC-DC converter (Horates V5) also has to be isolated from the rest of the circuit before reaching the desired voltage. This is due mainly to the behavior of the microcontroller when V_{CC} has a low slew rate (it grows slowly). In this case, when V_{CC} is near $V_{CC_{min}}$, where $V_{CC_{min}}$ is the minimum supply voltage of the microcontroller, the microcontroller consumes a much higher current than during normal operation. This, in turn, results in V_{CC} dropping, and then the cycle repeats, with V_{CC} stuck at $V_{CC_{min}}$. This phenomenon can be compared to inrush currents [59], as the effect is the same.

In this work, to achieve this isolation, the circuit shown in Figure 4.30 was used.

The core of the circuit is an XC6136 voltage supervisor [58], and its schematic is shown in Figure 4.31.

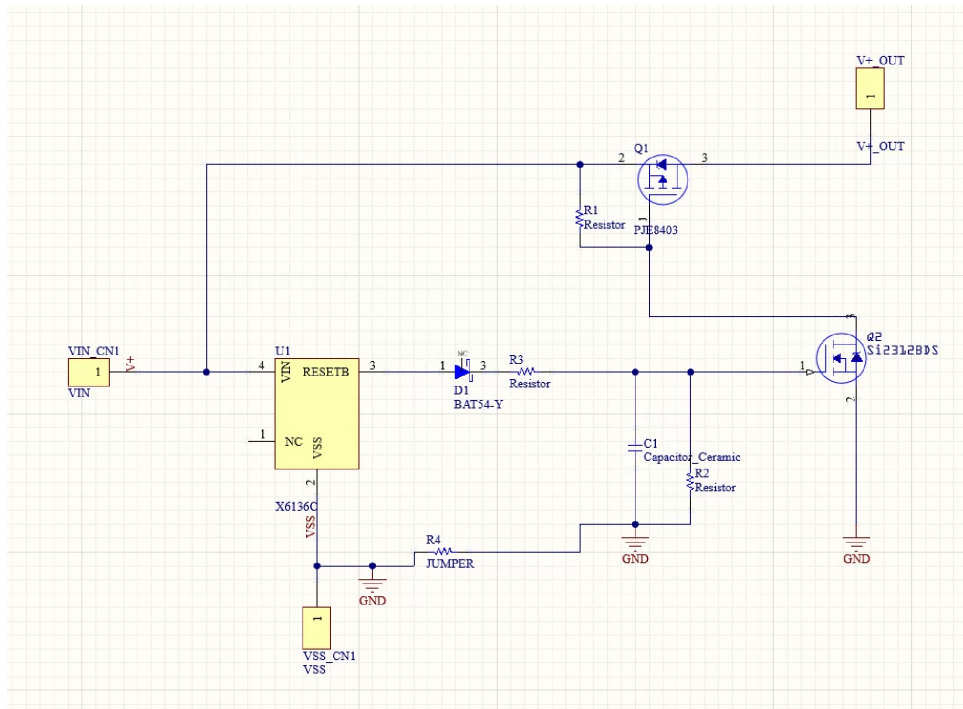


Fig. 4.30: Schematic of the circuit used for boost converter isolation.

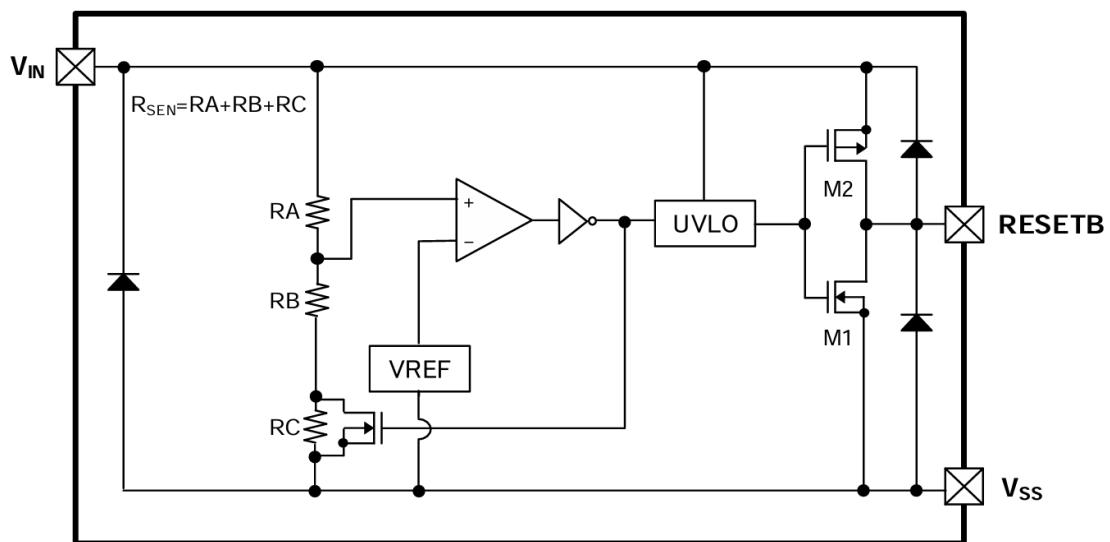


Fig. 4.31: XC6136 schematic. Source: [58].

The output of this voltage supervisor is equal to 0V when V^+ is lower than 2.1V (the detection level is equal to 2V, and the circuit has a hysteresis of 100mV), where V^+ is the output of the boost converter. When V^+ is greater than 2.1V, the output of the voltage supervisor is equal to V^+ . The output is connected to two transistors (Q1 and Q2 in Figure 4.30) acting as a load switch.

While this arrangement achieves the isolation required, using only the voltage supervisor IC has a drawback. When V^+ goes below 1.9V, its output is at 0V again, meaning that the initial current draw of the microcontroller opens the load switch, entering a reset cycle as mentioned previously. To avoid this, a diode is connected from the output to a capacitor. In this way, once V^+ surpasses 2.1V, the load switch closes, connecting the output of the boost converter to the microcontroller. Meanwhile, if V^+ drops below 1.9V, the output cannot open the load switch, since the diode prevents conduction in that direction.

The final result of this circuit can be described as a switch with a voltage threshold of 2.1V, where the control terminal gets latched once the threshold voltage is reached. The load switch only opens after the capacitor is discharged through a bleeder resistor of 10M Ω . An equivalent circuit was designed and simulated in LTSpice to illustrate the operation of the circuit graphically, as shown in Figure 4.32. V_X corresponds to the input voltage and V_o to the output voltage.

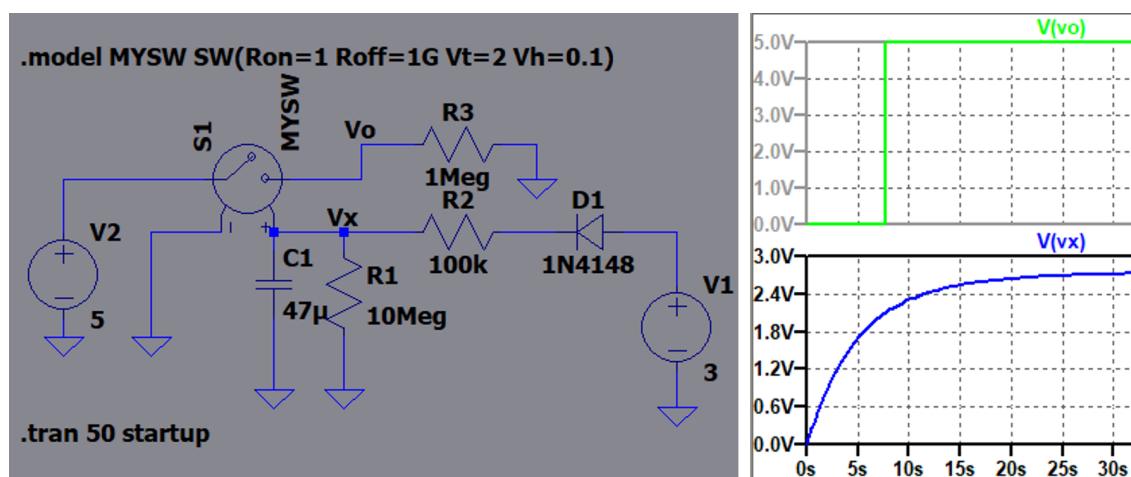


Fig. 4.32: Equivalent circuit of the boost converter isolation circuit along with simulation.

4.2.7 Oscillator implementation

As mentioned previously, the startup circuit has the Horates V4 as part of it. The schematic of the startup oscillator circuit (Horates V4) as implemented in Horates V5 is shown in Figure 4.33. The DC_{BIAS} output is used to power a square wave oscillator, which is then in charge of switching the transistor of the Horates V5 negative branch, as explained in the introduction of this chapter. Furthermore, a circuit has been added to disconnect the negative branch of the DC-DC converter from the startup oscillator circuit (Horates V4) after the microcontroller starts operating, to avoid further power consumption from that branch.

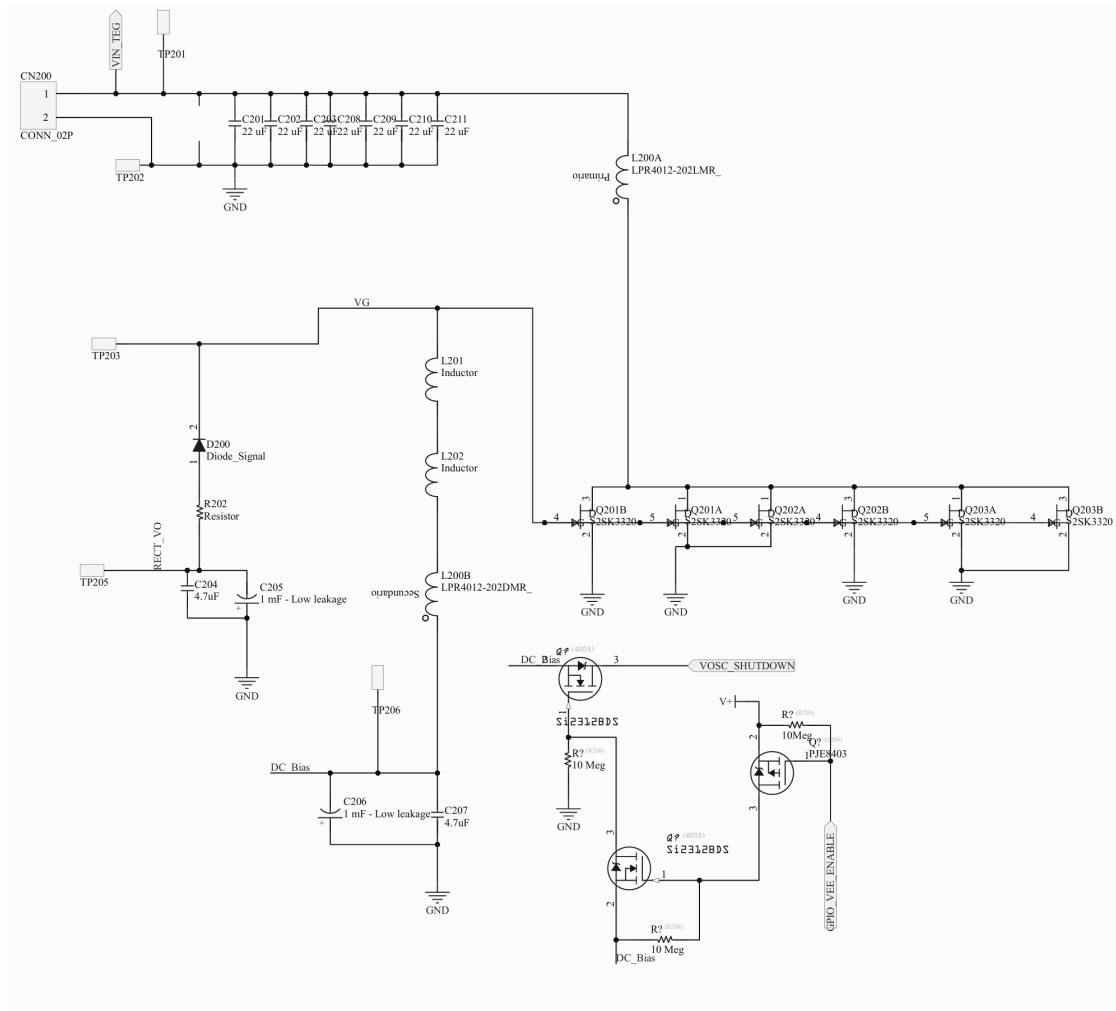


Fig. 4.33: Oscillator schematic.

Meanwhile, the square wave oscillator is shown in Figure 4.34. This is the oscillator in charge of switching the P-MOSFET in the negative branch, and it consists of a classical relaxation oscillator.

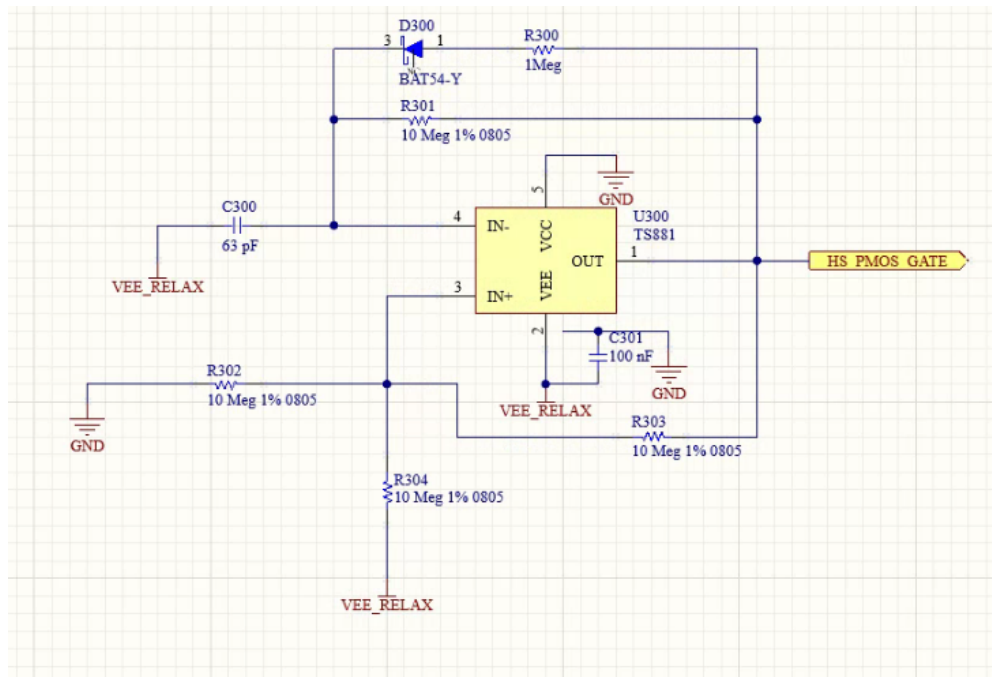


Fig. 4.34: Schematic of the square wave oscillator.

4.2.8 DC-DC Converter

The schematic of the DC-DC converter, the core of the Horates V5 circuit, is shown in Figure 4.35. The negative branch is the one corresponding to transistor Q109, while the positive branch is the one corresponding to transistor Q110. The connection of the negative branch to the startup oscillator can be seen in the port named "VOSC_SHUTDOWN".

4.2.9 Adaptive Ton Block

Adaptive T_{on} is the name of a method to control the switching frequency and duty of the transistors in the DC-DC converter. This method, while not explicitly an MPPT method, can be used in low-power scenarios to reduce system losses. Losses in a DC-DC converter

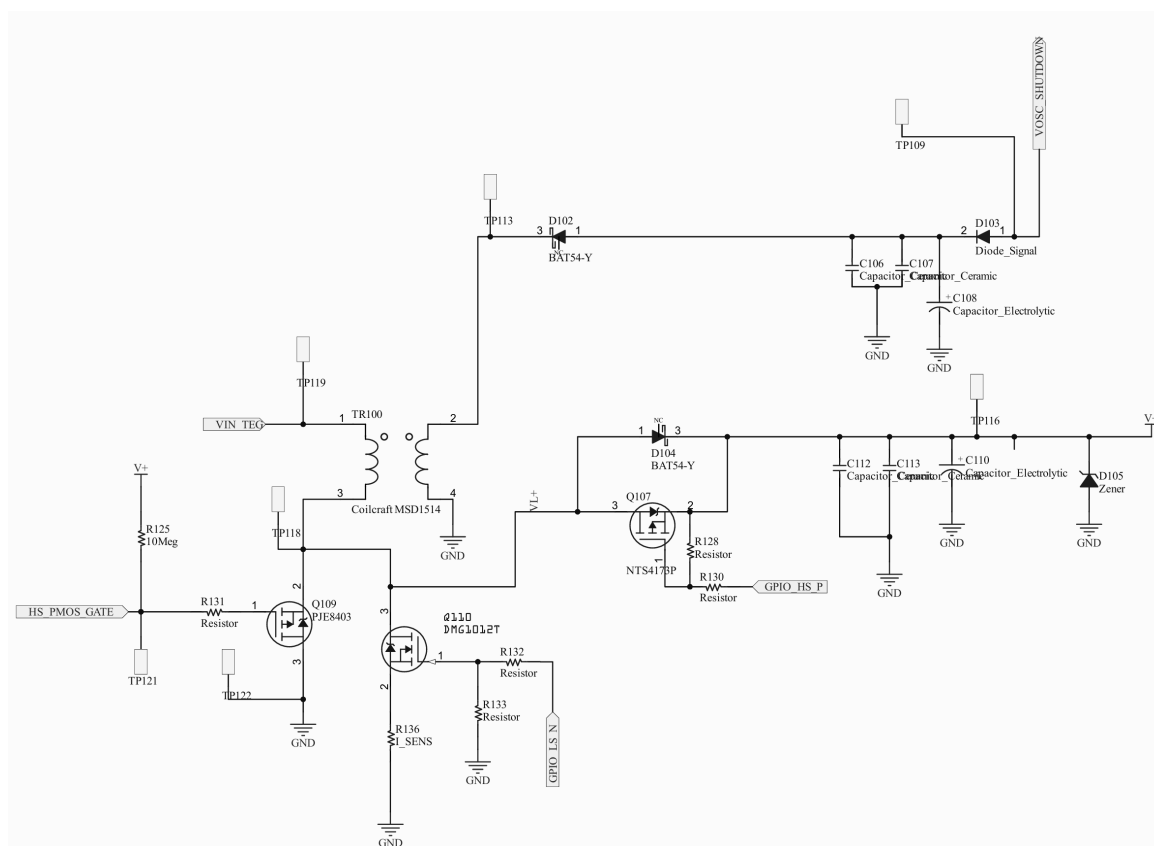


Fig. 4.35: Schematic of the DC-DC converter.

can be mainly separated into switching losses, conduction losses, and control circuit losses. These losses are a function of V_S and I_{LPeak} , among other factors. In CCM, for a determined V_S , conduction losses tend to be smaller than switching losses. Meanwhile, in DCM, for the same V_S , since the I_{LPeak} is much higher than in CCM, the conduction losses are relatively higher when compared to the switching losses.

Hence, DCM is the preferred mode to be used in low input voltage situations. Nonetheless, it is also important to note that, when using a Constant On-Time (COT) control scheme for switching, i.e., maintaining a constant T_{on} while the varying parameter is the frequency, the switching losses are constant, since they are inversely proportional to T_{on} [60]. This switching loss becomes the main loss factor when reducing V_S , considering that the conduction losses go down with V_S , as the peak current is $I_{LPeak} = V_{IN}T_{on}/L$, while the switching losses are constant. In DCM, the switching losses can be expressed as:

$$P_{SW} = \frac{2L(\lambda_{LS}C_{LS} + \lambda_{HS}C_{HS})}{R_S T_{on}^2} V_{OUT}^2 \quad (4.3)$$

In Equation 4.3, the lack of relationship of the switching losses with V_S can be observed, as well as the inverse relationship with T_{on} . One possible solution to this problem is to use an adaptive T_{on} control scheme instead of a COT one. This means that, when V_S goes down, T_{on} increases in the same proportion. This solution has two effects on the circuit:

1. Since $I_{LPeak} = V_{IN}T_{on}/L$, the peak current is constant for any V_S .
2. As P_{SW} is inversely proportional to T_{on} (Equation 4.3), and the maximum available power from the voltage source is $P_{av} = \frac{V_S^2}{4R_S}$ [23], when V_S goes down, the switching losses diminish in the same proportion that the available power at the input.

Consequently, an adaptive on-time control scheme reduces the losses when working with low-input voltages. Another advantage of this control method is that the peak current is independent of V_S (Figure 4.36), a fact that can be exploited to implement MPPT methods [61]. Figure 4.36 shows the peak current and correspondent V_{IN} when simulating a basic boost converter with the adaptive on-time circuit integrated.

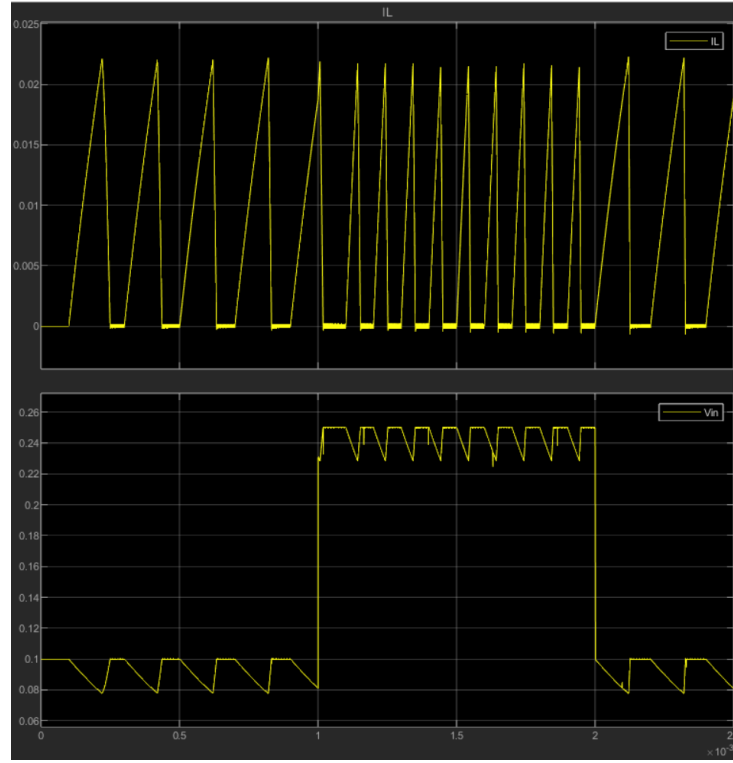


Fig. 4.36: Constant peak current along V_{in} variation plot.

4.2.10 Circuit Implementation

For Horates V5, the adaptive on-time circuit is implemented by means of a voltage-controlled current source, made by an operational amplifier in follower configuration, which copies V_{in} to a resistor connected to GND. This constant current source then discharges a previously charged capacitor linearly, so the discharging time can be used as T_{on} , as it is inversely proportional to V_{in} . The schematic is shown in Figure 4.37.

The capacitor should be as small as possible to reduce dynamic power losses. The resistor can be replaced by an array of parallel resistors in series with transistors to have different T_{on} ranges, since the resistor determines the current intensity.

The diminishing voltage of the comparator V_{CAP} is compared against a reference voltage V_{REFC} , as seen in Figure 4.37. The equation that describes the current of a capacitor is:

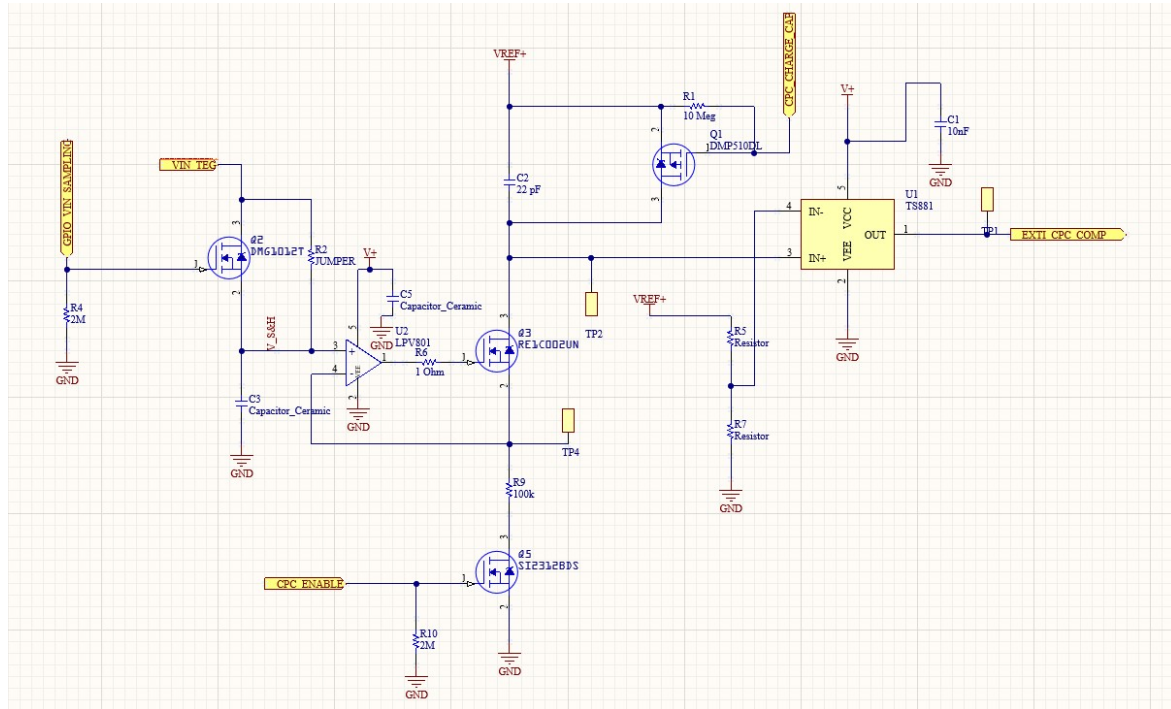


Fig. 4.37: Schematic of the adaptive T_{on} circuit.

$$C \frac{dV}{dt} = I \quad (4.4)$$

Hence, if the current I is constant, the voltage is a linear function of time Figure 4.38.

Since the principle of an adaptive on-time circuit is for $T_{on} = A/V_{IN}$, with A a proportionality constant, then the capacitor discharge can be used to implement it. To this end, the discharge current should be proportional to V_{IN} .

Through the use of an operational amplifier connected in follower configuration, V_{IN} is "copied" to a resistor $R9$ (Figure 4.37), such that $I = V_{IN}/R9$. Finally, from Equation 4.4, $T_{on} = \frac{\Delta V C R9}{V_{IN}}$, with ΔV equal to the difference between V_{CAP} and V_{REFC} .

The voltage reference used for V_{REFC} is provided by a resistive divider connected to a REF35 IC [62] from Texas Instruments, which outputs $1.6V$. For resistors $R5 = 2M\Omega$ and $R7 = 5.1M\Omega$, $V_{REFC} = 1.16V$.

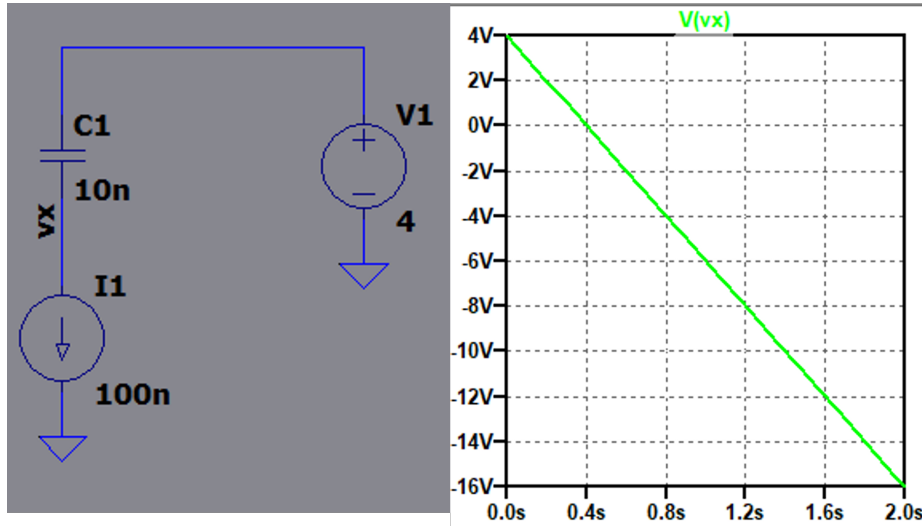


Fig. 4.38: Simulation of capacitor discharging with a fixed current.

The circuit is designed to generate a T_{on} such that the δ (duty cycle) and f_s are adequate for the application. In this case, $T_{on} = 274\mu s$ for a $V_{in} = 40mV$. The minimum T_{on} is limited by the propagation delay ($2\mu s$ typical) and slew rate of the comparator used. The comparators in the microcontroller used, an STM32L412, have multiple operating modes. They can work at higher speeds at the cost of consuming more power, which widens the range of possible on-times. This also allows reducing power consumption in low frequency switching scenarios.

Nonetheless, while the integrated comparator offers flexibility at reduced power consumption ($\approx 10\mu A$ for low-power modes and $\approx 100\mu A$ for the high-speed mode), since this peripheral is part of the APB2 (Advanced Peripheral Bus 2) group, the clock for this peripheral bus must be enabled. This results in an increase of current consumption of $300\mu A$, and it is not useful considering the comparator is the only peripheral from that group being used. As a result, external low-power comparators ICs are used.

In Figure 4.39, a comparison of the on-time for different V_{in} voltages is presented. It was proven empirically that the linearity of this method is sufficient to implement the MPPT method based on adaptive on-time.

The schematic of the adaptive T_{on} circuit of the final design is shown in Figure 4.37.



The Horates V5 circuit uses MPPT method based on a method presented in the literature, implemented with mixed signal circuits in ICs but adapted here to work with a discrete circuit using a microcontroller as the control unit.

The MPPT method, as mentioned in subsection 4.2.9, is based on the use of a CPC control method [61]. This method is used in low-power conditions (determined by the input voltage), since a CPC control scheme reduces the switching losses at low input power when compared to a constant on-time scheme [63].

The basis for this method is that, since each switching period consists of a constant peak current “packet”, then each packet has the same energy as every other one. This means, in turn, that the number of packets sent in a frame of time is directly related to the energy, and that there is a switching frequency that optimizes the quantity of energy extracted from the generator.

The optimum frequency to obtain MPPT in this case is:

$$f_{s_{opt}} = \frac{V_{TEG}^2}{2I_{peak}^2 LR_{TEG}} \quad (4.5)$$

Besides, the average input voltage is equal to:

$$\overline{V_{IN}} = \frac{V_{TEG} \pm \sqrt{V_{TEG}^2 - 4kf_s}}{2} \quad (4.6)$$

where $k = ((I_{peak}^2 LR_{TEG})/2)$.

If the equation for $\overline{V_{IN}}$ is then derived with respect to f_s , the result is:

$$\frac{d\overline{V_{IN}}}{df_s} = \frac{-k}{\sqrt{V_{TEG}^2 - 4kf_s}} \quad (4.7)$$

Lastly, plotting both $\overline{V_{IN}}$ and its derivative in Figure 4.40, it can be appreciated that the derivative has a sharp increase when $\overline{V_{IN}}$ reaches $V_{TEG}/2$, this is, the maximum power point.

Since T_{on} is a function of $\overline{V_{IN}}$, this means that near the MPP there is a sharp increase of T_{on} , which consequently results in a sharp increase of the duty cycle $\delta = T_{on}/T$. Hence, if the circuit can detect sharp changes in δ when varying the frequency, then it can detect when the operating point corresponds to the MPP.

Implementation on microcontroller

Since the Horates V5 circuit uses an STM32L412 microcontroller, the MPPT method is implemented using the Low Power Timer (LPTIM) peripheral, a timer clocked by an internal 32kHz oscillator, and able to work during low-power modes, to take advantage of them for

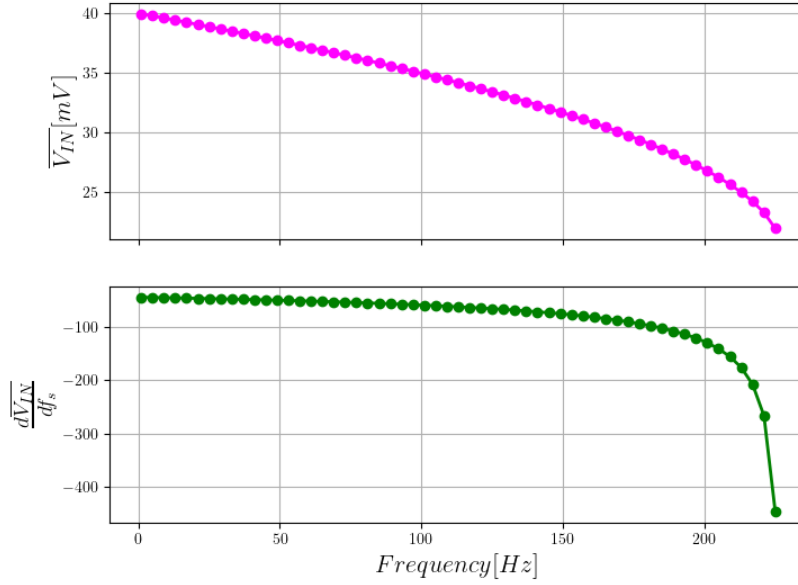
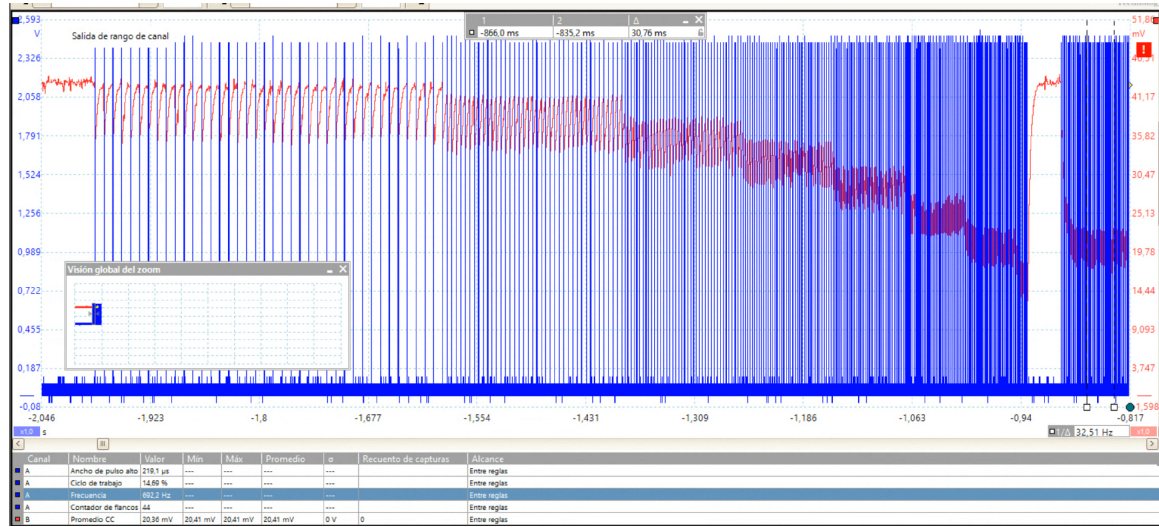


Fig. 4.40: $\overline{V_{IN}}$ and its derivative.

power consumption reduction. Additionally, the method involves the adaptive ton circuit exhibited previously, whose output is connected to a pin of the microcontroller with External Interruption (EXTI) capabilities, to wake up the microcontroller once T_{on} ends.

Figure 4.41 shows how the MPPT method works for a $V_{TEG} = 40mV$.

As it can be seen in the figure, the switching frequency f_s is increased (the blue lines get closer together) while T_{on} varies according to V_{IN} . Meanwhile, the duty cycle δ is measured by the LPTIM, which consists in a simple division operation between the counter of said timer and the auto-reload value (maximum value for the counter). When switching frequencies, with f_c and f_p being the current frequency and the previous frequency respectively, the current δ_c is compared with the δ_p corresponding to the previous f_s . If $\delta_c - \delta_p > \delta_{TH}$, this is, if the current duty cycle is bigger than the previous duty cycle by a predefined value, then the algorithm considers that the MPP has been reached. At that point, the DC-DC converter stops switching until V_{IN} goes back to the value it had when $f_s = f_p$. Lastly, the converter starts switching again with $f_s = f_p = f_{MPP}$ (or the cycle repeats again with smaller frequency steps for a better approximation of the MPP).

Fig. 4.41: Red: V_{IN} , Blue: NMOS gate signal

The implementation of this MPPT method is graphically represented as a finite-state machine [64], presented in the following figures.

Figure 4.42 shows a flow diagram of the main state of the finite-state machine, called CPC_OFF. In this diagram, cD or c_D represent the current duty cycle, D_Ref corresponds to the duty cycle corresponding to the previous f_s , ΔTH is the threshold difference between current and previous duty that needs to be surpassed to consider the MPP reached, and N counts the number of cycles.

Figure 4.44 shows the rest of the states. The retrieve state is entered when the MPP has been reached, to stop the switching and give time to V_{IN} to recover to the value it had before increasing the frequency, as explained by Venugopal et al. work [61]. To this end, a comparator with a sample and hold circuit is used (Figure 4.43), to signal when V_{IN} reaches the desired value.

As for the rest of the states:

- The idle state is entered when there is no switching of the main transistor (such as during output regulation).
- The "no input" state is entered when $V_{IN} \approx 0V$, as to not waste power unnecessarily.

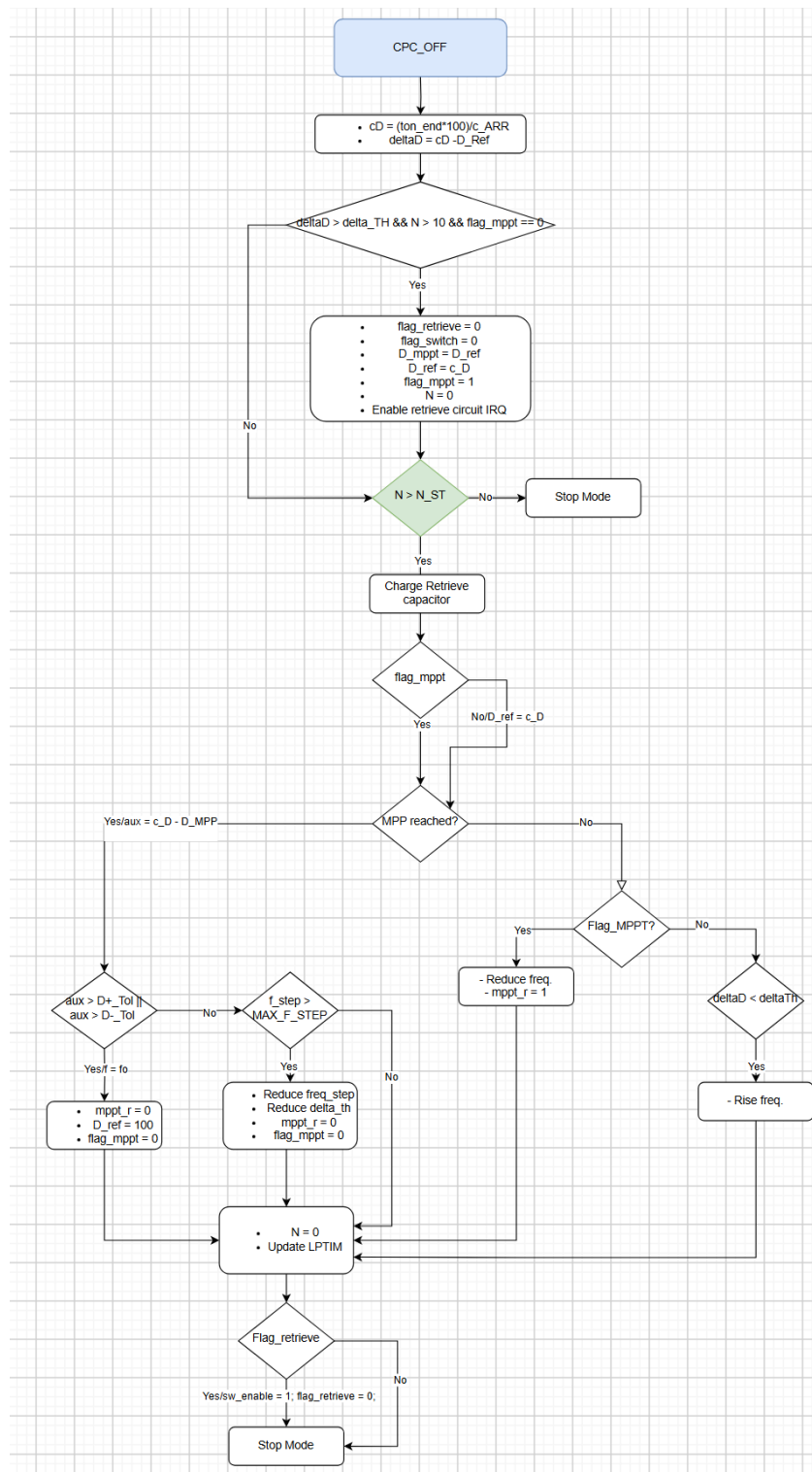


Fig. 4.42: Flow diagram of the main state of the state machine.

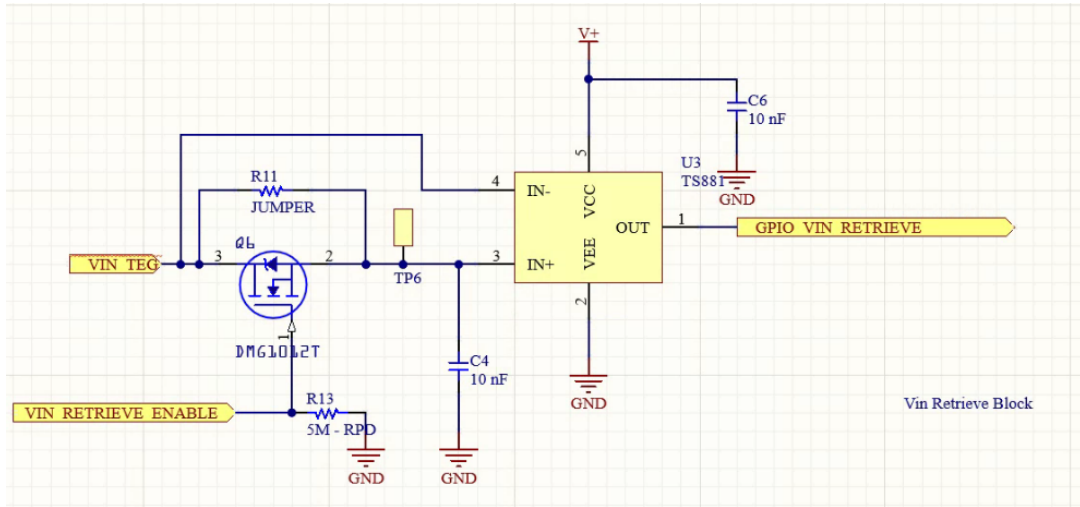


Fig. 4.43: Retrieve state circuit.

- The init state realizes the initialization of the system, and is entered when the circuit first starts, or when it comes out of the "no input" state.

Finally, Figure 4.45 shows diagram flows for each interrupt handler used.

- The CPC_COMP handler is in charge of turning off the main transistor when T_{on} ends. It is the handler connected to the interruption of the adaptive on-time circuit comparator.
- The LPTIM handler is in charge of implementing a time base, detect when there is no input, and manage the frequency of the main transistor switching.
- The Programmable Voltage Detector (PVD) handler is in charge of regulating the output voltage.
- The retrieve handler is in charge of the voltage retrieve process, which gives time to V_{IN} to recover after finding the MPP.

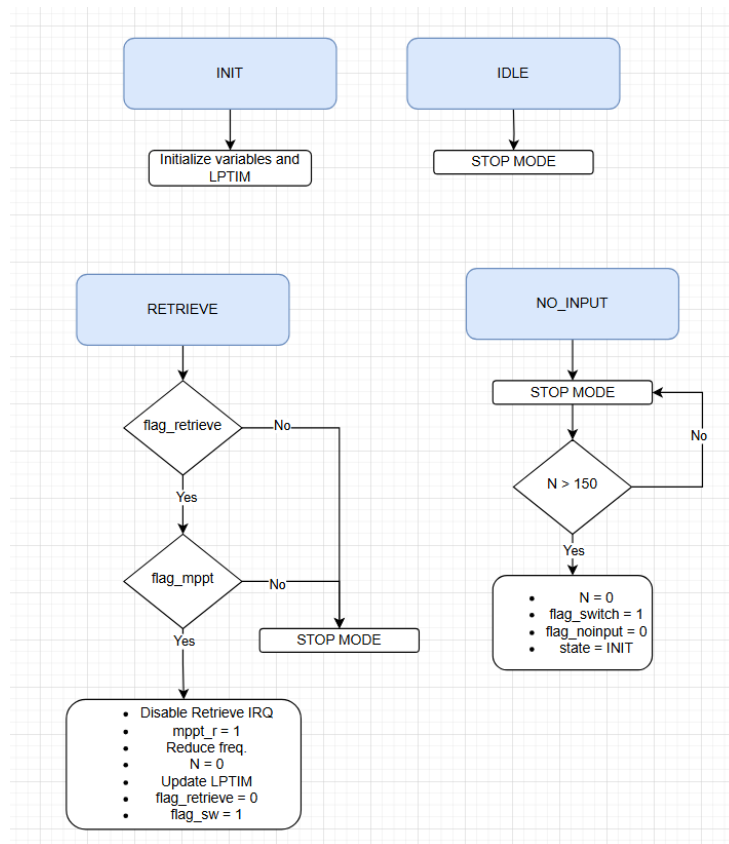


Fig. 4.44: Rest of the states.

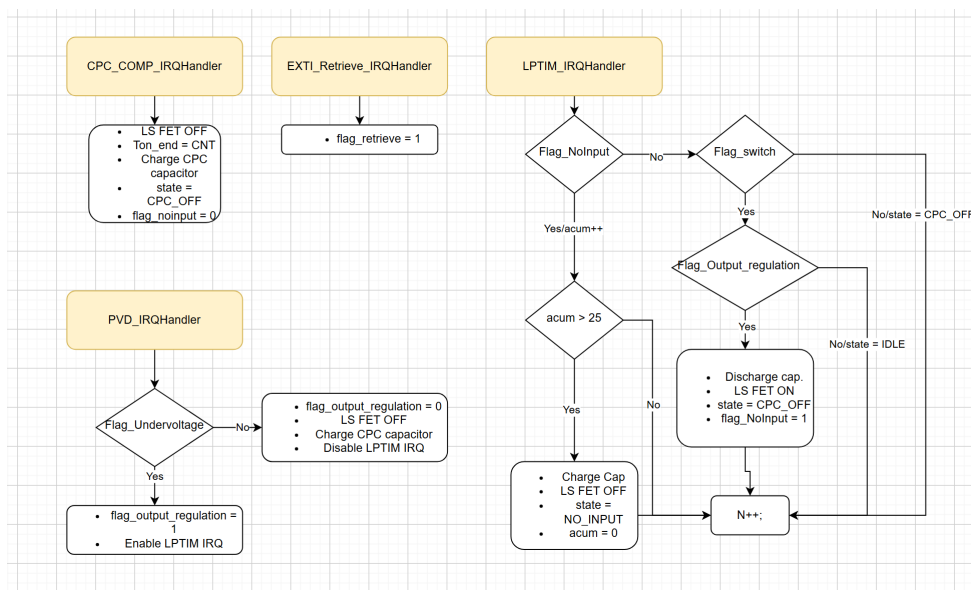


Fig. 4.45: Interruptions.

4.2.12 ZCS implementation

The operation of a boost converter can be divided into two stages, depending on the state of the switching MOSFET, as shown in Figure 4.46. When the switch is closed (ON state), the inductor starts to store energy from the input voltage source. After a charging period, the switch is opened (OFF state), and the inductor discharges its energy to the output through the diode. This explanation, along with the diagrams in Figure 4.46, makes it clear that the diode causes losses since it is in the path of the discharging current. These conduction losses can be expressed as

$$P_D = I_{LAVG} * V_F + I_{LRMS}^2 * R_D \quad (4.8)$$

where I_{LAVG} is the average current through the diode, V_F is its forward voltage drop, I_{LRMS} is the RMS current through the diode, and R_D is the diode dynamic resistance [65].

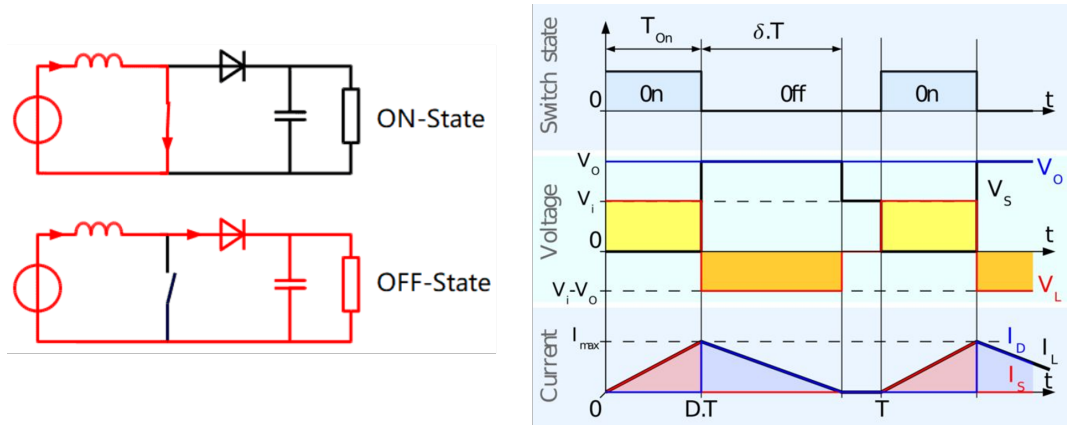


Fig. 4.46: Boost converter with switch in ON and OFF state.

To reduce these losses, the diode can be replaced with a MOSFET, which in this case is called a “synchronous rectifier”. The reason for this name is that this MOSFET is controlled to conduct only in one direction, the same as a diode. The benefits of replacing the diode with a MOSFET are the lack of a minimum required voltage to conduct (the forward voltage drop of the diode) and a much lower resistance, resulting in a higher efficiency in most of the cases (since the switching control of the MOSFET introduces additional losses, so it must be evaluated in a per-case basis). The difference between both cases can be observed in Figure 4.47.

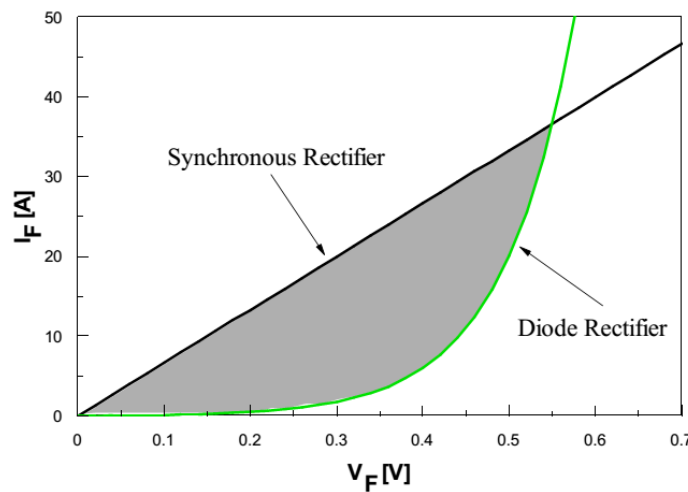


Fig. 4.47: Comparison between synchronous rectifier and diode. The gray area represents the power saved when using a synchronous rectifier. Source: [66]

The MOSFET needs a control circuit to behave like a diode, since in reality when it is closed it conducts in both ways. This leads to instances where, if the control is not perfectly timed, the current can go from output to input (when the MOSFET is opened too late), losing charge from the output, and hence, efficiency of the circuit. The other case is when the MOSFET is opened too early, leading to the inductor not discharging entirely in the output, but instead discharging the rest of the energy through the parasitic diode of the low-side MOSFET, resulting in loss of efficiency too. To avoid these power losses due to the switching timing, a ZCS control scheme is implemented, which corrects the switching timing so that the MOSFET is switched off at the exact point when the current through it is equal to zero.

Implementation

The ZCS control scheme implemented in Horates V5 is based in an established method. When the high-side MOSFET is opened during the discharging phase, an abrupt voltage change is generated in the inductor, due to Faraday's Law: $L \frac{dI}{dt} = V$ (Figure 4.48). The polarity of this voltage indicates whether the MOSFET was opened early or late.

A comparator is used to compare this signal with V_+ , and the result is fed to a timer in the microcontroller, to have an accurate estimate of how early or late the MOSFET was opened (Figure 4.49). Subsequently, through iterations, the optimum on-time for the high-side

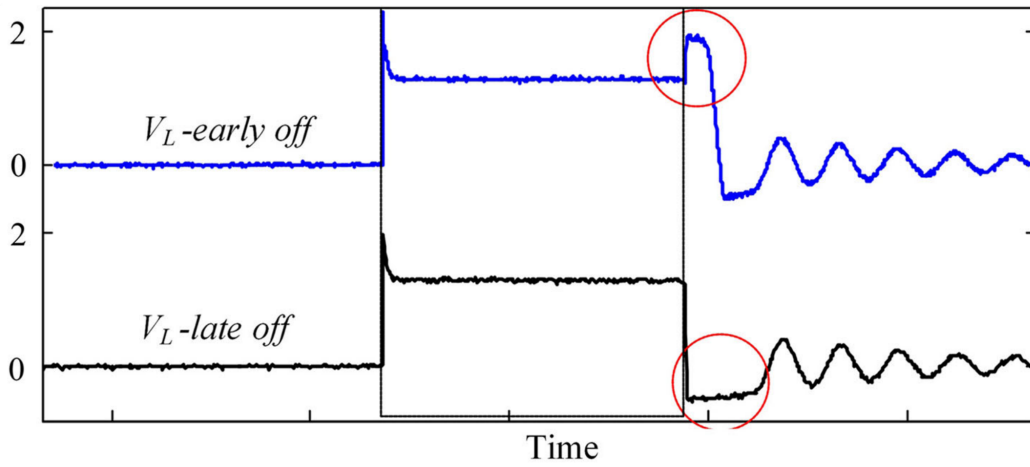


Fig. 4.48: Polarity of V_L indicating an early or late opening. Source: [48]

MOSFET is reached. This method is easy to implement both with a microcontroller or with digital logic in an IC, with a difference in power consumption.

The implementation in the circuit design is shown in Figure 4.49.

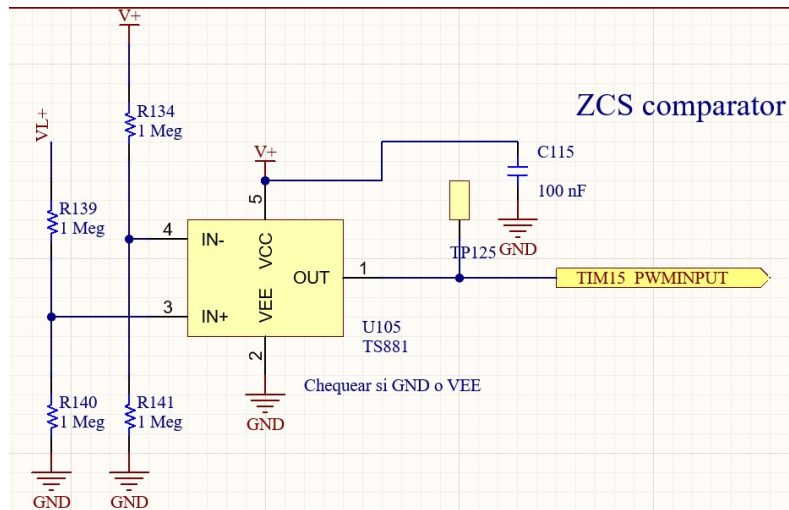


Fig. 4.49: Schematic of the ZCS circuit.

While this circuit was implemented, the final design of the converter does not use ZCS. Due to the T_{on} used, it was unfeasible using only the LPTIM, and using other timers introduces a significant power consumption. This will be delved further upon in the results section.

4.2.13 Output voltage regulation

The output voltage regulation block originally consisted of two low-power comparators in a window configuration Figure 4.50, which compared the output voltage $V+$ against a fraction of V_{REF} , the reference voltage provided by a REF35 IC from Texas Instruments [62]. Both comparators outputs were connected to an EXTI line of the microcontroller, to generate an interruption and wake up the MCU on rising edges.

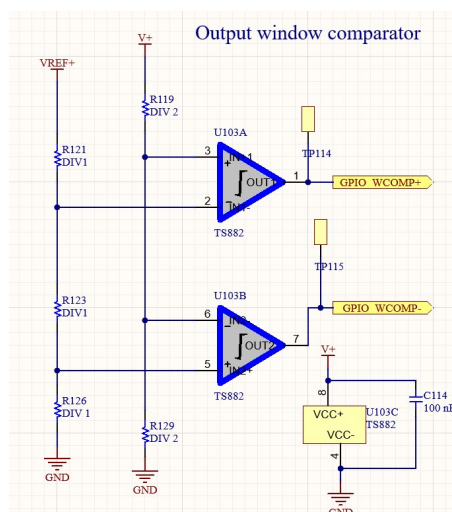


Fig. 4.50: Window comparator schematic

This output window comparator worked as the voltage regulation stage, making the converter work in burst mode, as seen in subsection 4.1.1). Nonetheless, after the design, a better option was found in one of the peripherals of the microcontroller, reducing area and power consumption of the circuit. The PVD generates an interruption when the voltage supply of the microcontroller (the output of the DC-DC converter) is below or above a programmable voltage level. It also counts with a hysteresis of $100mV$, as seen in Figure 4.51.

4.2.14 Energy Storage

The energy storage consists of a supercapacitor connected in series with an N-MOSFET and a current limiting resistor Figure 4.52. The MOSFET is controlled by the microcontroller, and it is closed depending on the output situation (generally when the output voltage reached the maximum voltage and the load is light). When the output voltage diminishes, the super-

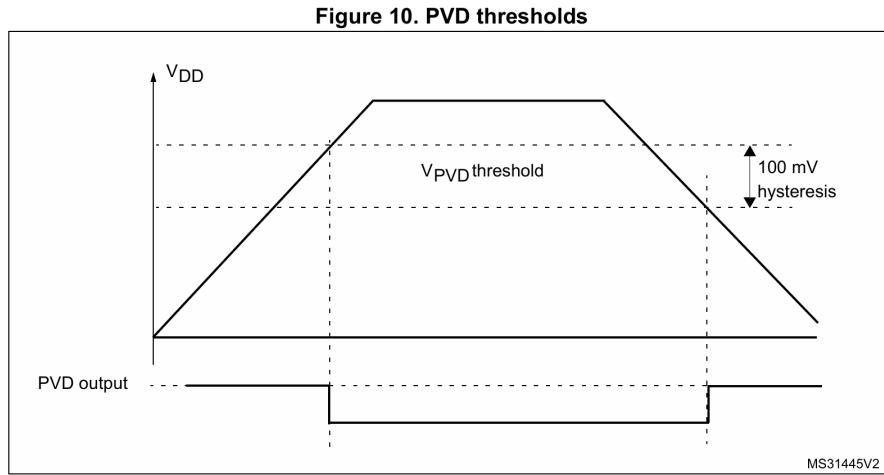


Fig. 4.51: PVD peripheral.

capacitor discharges to the output through the parasitic diode of the N-Channel MOSFET, same as in Patra et al. work [67].

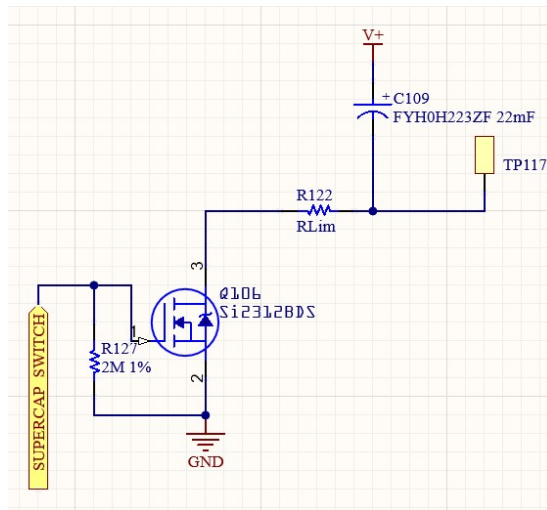


Fig. 4.52: Energy storage.

As all the blocks conforming the DC-DC converter have been presented, the next section presents the results obtained.

4.3 Results

The resulting Printed Circuit Board (PCB) for the Horates V5 circuit is shown in Figure 4.53. As mentioned previously, the board has 4 layers, with two layers connected to GND in the middle. The top layer is mostly destined to the microcontroller and the DC-DC converter, while the bottom layer houses the startup circuit along with the adaptive on-time circuit. The dimensions of the PCB are 7.8 cm x 7.8 cm, although the area was significantly reduced while reworking the design.

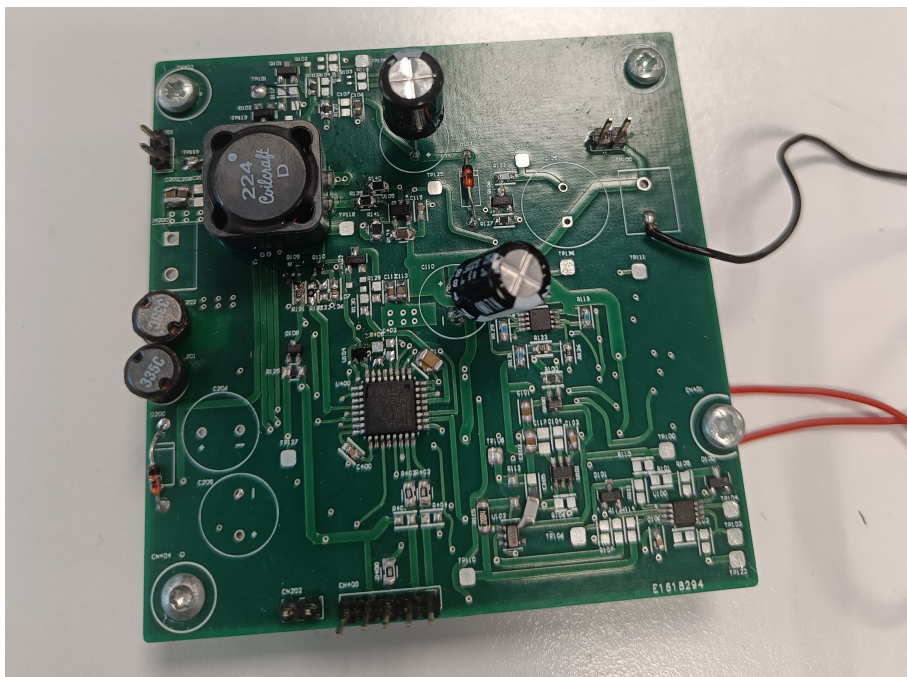


Fig. 4.53: Horates V5 PCB implementation.

The board was designed such as that the output of the DC-DC converter can be isolated from the rest of the circuit. This characteristic allows measuring the current given by the converter without loading, and also allows the use of the STLINK-V3PWR debugger probe and source measurement unit [68]. This, in turn, permits measuring the power consumption of the whole circuit without the influence of the boost converter, so it is effectively the current consumed by the control circuit. The probe is shown in Figure 4.54, along with the rest of the measurement setup. The measurement setup in this case is conformed just by a power source in series with a 4Ω resistor, used for all measurements, a multimeter, and an oscilloscope outside the frame.



Fig. 4.54: Measurement setup and STLINK-V3PWR probe.

The measurements involved testing the output regulation capabilities of the circuit, its startup voltage, the tracking capabilities of the MPPT method, and the current consumption in idle mode and operation mode. It is worth noting that due to changes in the circuit, provoked by a low duty cycle in the original circuit, the switching frequency currently is higher than it should be, affecting various parameters, such as the overall power consumption of the microcontroller, the MPP tracking capabilities (with reduced T_{on} , the LPTIM resolution is reduced too), and the use of ZCS. The ZCS circuit was not used in this case, since it requires a timer with a frequency of around 100 times greater than f_s to have an acceptable resolution. As ongoing work, to reduce significantly f_s and T_{on} , as was previously explained in subsection 4.2.4, the inductance would be changed from $220\mu H$ to $1mH$.

Continuing with the results, the first measurement was the consumption in idle mode (Figure 4.55), which resulted in an average of $21.5\mu A$ for a $V_{CC} = 2V$, resulting in a quiescent power of $43\mu W$. In all measurements, the red graph corresponds to the input voltage while the blue graph corresponds to the signal at the gate of the main MOSFET.

In Figure 4.56, the accuracy of the MPPT method is demonstrated for an input of $V_{oc} = 80mV$ (open circuit voltage). The circuit increases the frequency from the start until it reaches the

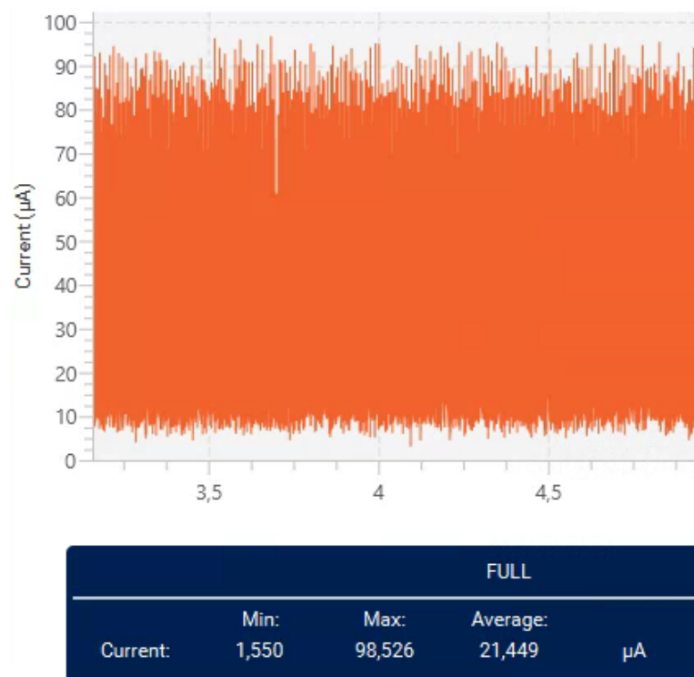


Fig. 4.55: Current consumption in idle mode for $V_{CC} = 2V$.

threshold value preprogrammed, and then it stops switching to give V_{in} time to rise back, as explained in the finite-state machine section of this chapter. The resulting V_{in} is equal to $43.8mV$, and considering that $V_{mpp} = 40mV$, the error is of $(V_{in}/V_{mpp} - 1) * 100 = 9.5\%$. The mentioned change of inductance from $220\mu H$ to $1mH$ should improve the accuracy, since the resolution of the LPTIM would be improved too.

After showing the tracking capabilities of the circuit for a steady input voltage, the next measurement was to verify the tracking capabilities when the input voltage has variations. The results are shown in Figure 4.57, and the values used for the input voltage are $80mV$, $120mV$ and $60mV$, in that order. The measurement shows that the tracking capabilities are sufficient, especially for TEG applications, where the voltage tends to change slowly.

Following the tracking measurements, that were done with the boost converter isolated from the rest of the circuit (this is, powering the circuit from the STLINK-V3PWR), the next measurements are done powering the converter using the startup circuit. The results of this measurement are shown in Figure 4.58 and Figure 4.59, where $V_{oc} = 100mV$ in the first one and $V_{oc} = 120mV$ in the second one. These measurements not only show the capability of the circuit to power itself from the input generator, but also show the output voltage regulation

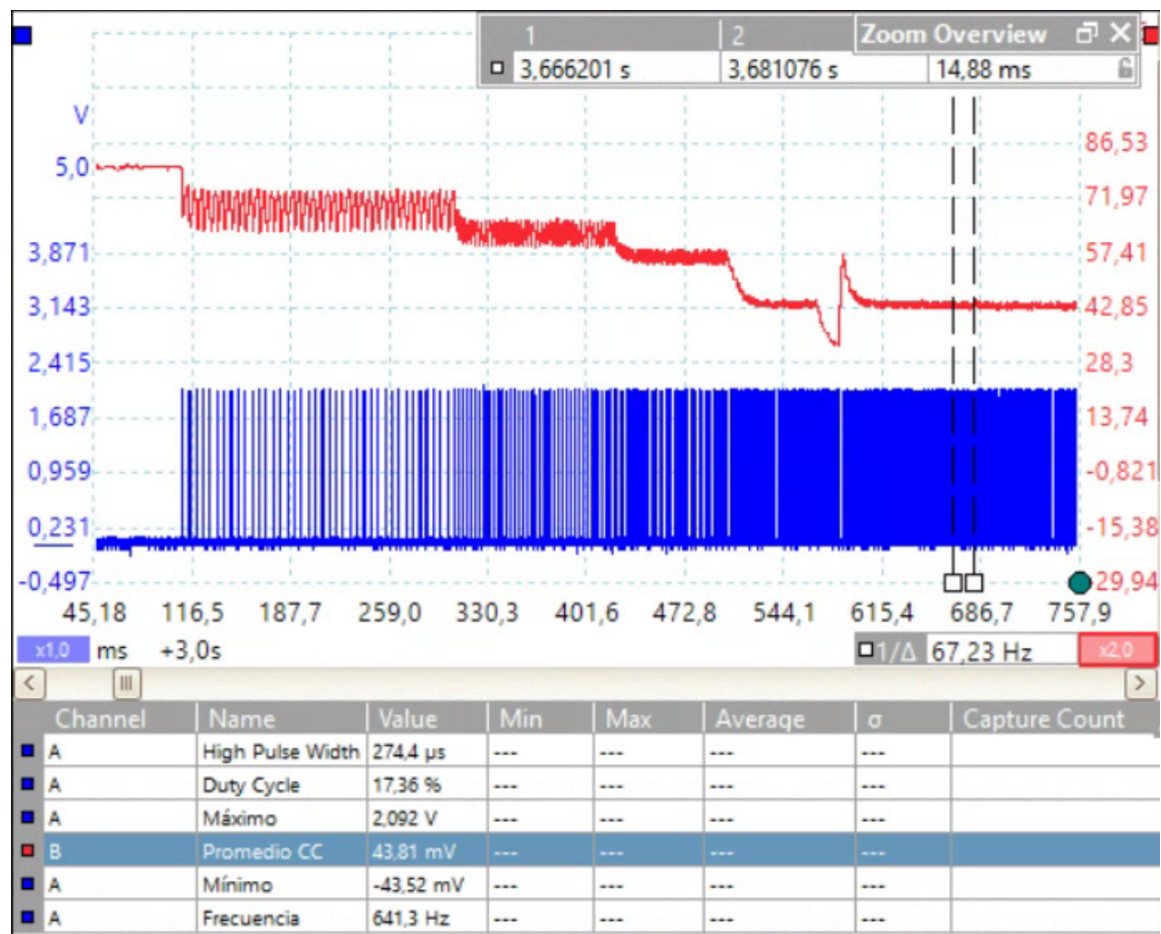


Fig. 4.56: MPP tracking for $V_{oc} = 80mV$.



Fig. 4.57: MPP tracking for a changing voltage signal.

capabilities. When the circuit reaches 2.3V, it stops switching until reaching 2.1V, and then it starts switching again. This can be appreciated in the figures at the points where the blue lines (gate signal of the main MOSFET) go to 0V.

From these two figures, it can be appreciated that the output voltage regulation works independently of V_{in} , and that for a bigger V_{in} , the startup occurs faster. For this circuit, the startup voltage currently is 100mV, and it is mostly determined by the storage capacitance for the microcontroller, since the power consumption from the circuit is lower than a few μA during startup. If the capacitance can be reduced, then the startup voltage can be reduced too. Nonetheless, it is also worth noting that the converter might work below the startup voltage once it is in operating mode. This has not been tested yet, but is one of the measurements to be done as future work.

Finally, as all the capabilities of the converter have been shown, along with its power consumption during idle mode, the last measurements are related to power consumption and extraction during operating mode. Figure 4.60 shows the current consumption for the control circuit operating at $V_{CC} = 2V$ when $V_{oc} = 100mV$. The current consumed amounts to 71.4 μA average.

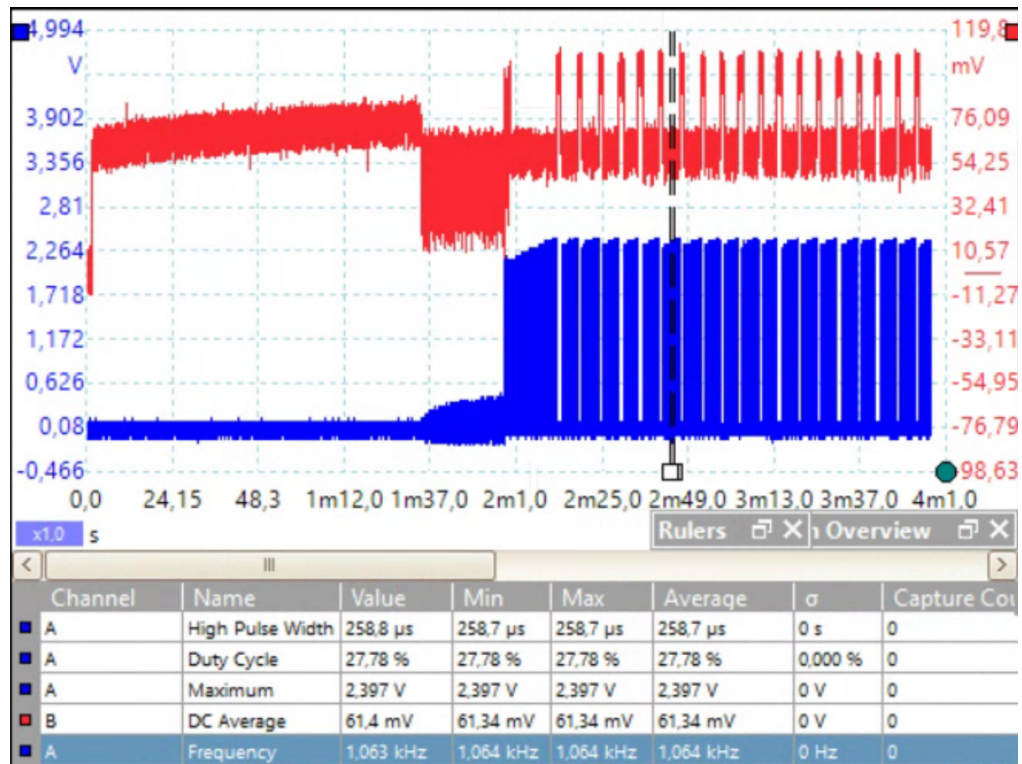


Fig. 4.58: Progress from startup mode to main operating mode for $V_{oc} = 100mV$.

Meanwhile, while measuring current directly from the output capacitor of the converter, the result is $0.5mA$, as can be seen in Figure 4.61. While this does not constitute an efficiency measurement, it can be noted that the current consumption of the control circuit is $(71.4\mu A / 500\mu A) * 100 = 14.3\%$ of the extracted current from the generator (limited by the resolution of the multimeter). As the power consumption increases linearly with frequency, it is expected that once the inductance has been changed, this value drops even more, allowing the circuit to work with lower input voltages.

4.4 Chapter Conclusions

A custom topology of DC-DC converter Horates V4, controlled by a microcontroller, and with a MPPT method implemented, was designed such that it could integrate the Horates V3 circuit as part of a startup circuit. The Horates V3 circuit was proven to work as a startup circuit, resulting in a startup voltage measured (for the entire system) around $V_{oc} = 100mV$ for a generator with a resistance of 4Ω . The capabilities of the DC-DC converter such as



Fig. 4.59: Progress from startup mode to main operating mode for $V_{oc} = 120mV$.



Fig. 4.60: Current consumption of the control circuit working in operating mode for $V_{cc} = 2V$ and $V_{oc} = 100mV$.

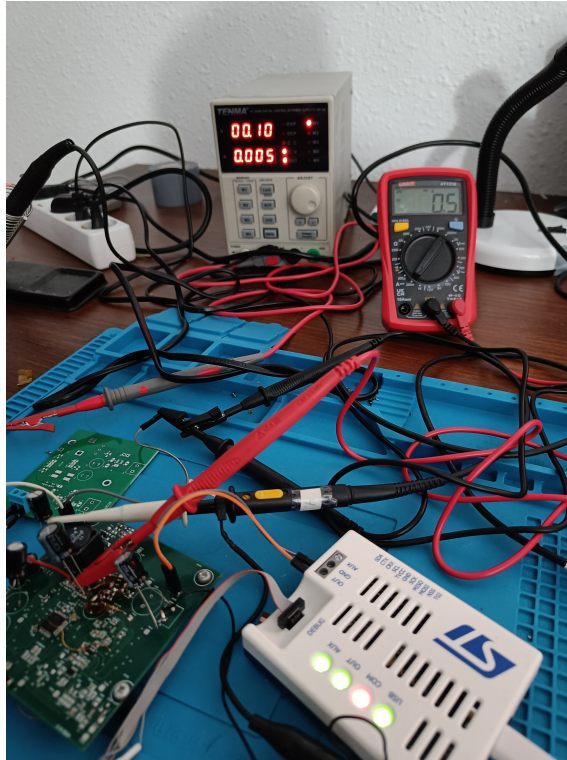


Fig. 4.61: Extracted current from the generator, shown in the multimeter.

MPP tracking, output voltage regulation, and power consumption were presented too and found to be in the expected ranges, although with room for possible improvement. The next section discusses the conclusions and future direction of this work.

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Chapter 5

Conclusions and Future Direction

5.1 Conclusions

During this thesis work, several energy harvesting circuits to be powered by Thermoelectric Generators (TEGs) were developed. These circuits can be applied to several low-power applications, with a focus in Internet of Things (IoT), where devices comprise sensors to gather environmental information, energy generators for self-powering or recharging batteries, a microprocessing unit and a communication module for data exchange.

Figure 5.1 shows a brief summary of the characteristics of each circuit presented in this thesis. Furthermore, the conclusions extracted from this work are presented next, from conclusions originating from chapter 2 to conclusions originating from chapter 4, in that order.

- **Chapter 2:** The feasibility of producing energy harvester circuits (Horates V2.1, Horates V2.2, and Horates V2.3) using flexible hybrid electronics was demonstrated, as a fully-functioning environmental sensing circuit was fabricated, with energy harvesting capabilities from TEGs or Near Field Communication (NFC). The importance of isolating the output of the boost converter from the rest of the circuit until the output is fully charged was first stressed in this chapter.

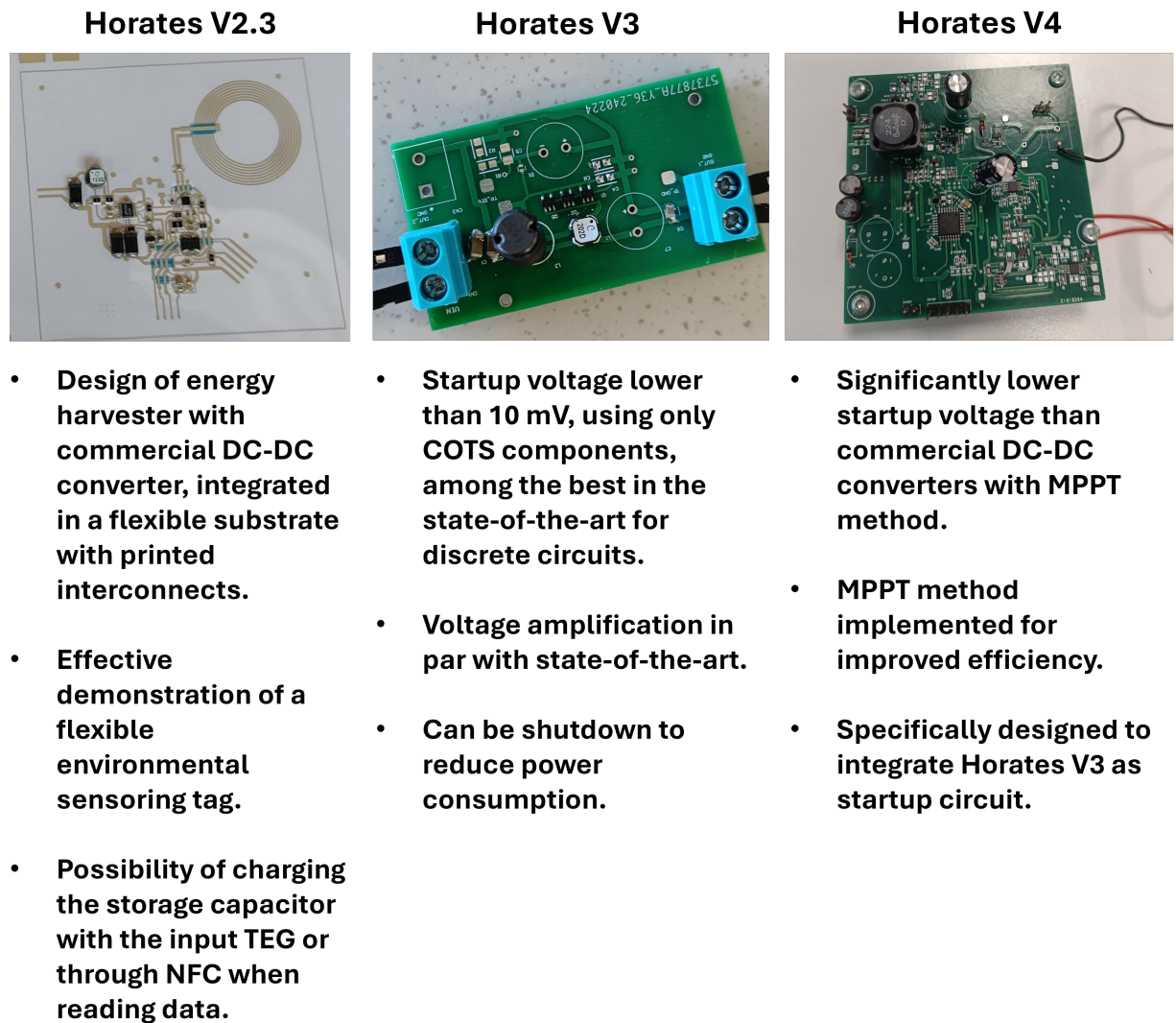


Fig. 5.1: Summary of the characteristics of the three final circuits presented in this thesis work.

- **Chapter 3:** The self-powered oscillator (Horates V3) was proven to be viable as a startup circuit or as a Direct Current - Direct Current (DC-DC) converter in applications where efficiency is not as important as a low startup voltage. It feats a startup voltage lower than $10mV$ using only Commercial Off-the-Shelf (COTS) components (not using hand-wound transformers or inductors), among the lower of the state-of-the-art for discrete circuits, while boasting a conversion ratio in par with the state-of-the-art. Furthermore, it has two crucial advantages when compared with commercial alternatives:
 - The input resistance of the self-powered oscillator can be determined during design, through the choice of different transistors. For example, the transistor 2SK3320 utilized for low input resistance can be swapped with a SST201 to adapt the circuit to higher input resistances ($> 100\Omega$). This allows the circuit to work with generators with a wide range of output resistances. Meanwhile, the input resistance of the commercially available low-voltage converters is fixed.
 - The circuit can be shutdown through the application of a negative voltage bias over the Junction Field Effect Transistor (JFET) gate, reducing considerably the power consumption of the circuit to improve efficiency in circuits where it is used a startup circuit.
- **Chapter 3:** The Horates V3 circuit was coupled to a modified boost converter, without Maximum Power Point Tracking (MPPT) method, to prove its performance as startup circuit. The minimum efficiency of the whole circuit was around 25%.
- **Chapter 4:** A custom topology of DC-DC converter (Horates V4), controlled by a microcontroller, and with a MPPT method implemented, was designed such that it could integrate the Horates V3 circuit as part of a startup circuit. The Horates V3 circuit was proven to work as a startup circuit, resulting in a startup voltage measured (for the entire system) around $V_{oc} = 100mV$ for a generator with a resistance of 4Ω . Hence, the Horates V4 circuit obtained startup voltages lower than the converters of the second group (introduced in chapter 1).

Recalling the problem statement: low-voltage TEGs needed DC-DCs converters who could work with low-voltages while having great efficiency (for example, through the implementation of MPPT methods). The preferred method to achieve this was using discrete circuits instead of Application-Specific Integrated Circuits (ASICs), due to the significant investment and development time needed for the later.

This thesis has provided a completely new self-powered oscillator topology to work with ultra-low voltage sources, as well as a DC-DC converter which can integrate this oscillator as a startup circuit, resulting in a conversion with significantly higher efficiency. This higher efficiency is due to the fact of implementing an MPPT method, as well as the fact that the conversion using a modified boost converter is always higher than the one from the Horates V3 circuit, as was demonstrated at the end of chapter 3. As such, the author feels that this study represents an important initial step towards addressing the problem statement, offering a basis for subsequent advancements and deeper investigation. In the next section, the future direction of this work is discussed.

5.2 Future Perspectives

In this thesis work, novel topological designs for self-powered oscillators and DC-DC converters were accomplished as summarized in section 5.1. In parallel, several insights arise from this thesis work, indicating new perspectives in the different fields explored, such as an insight into the integration of startup circuits and DC-DC converters in discrete low-power applications, since the majority of the literature is focused in the development of one or the other. Furthermore, problems arising from this integration were identified and proposed a solution, such as the inrush current provoked by microcontrollers when reaching their minimum supply voltage, which impedes fully charging the output of low-power DC-DC converters.

The future direction of this work will consist in:

- **Chapter 3:** Fabricate the high-resistance version of Horates V3 mentioned in chapter 4, as it was only simulated, and integrate it with the DC-DC converter, to characterize their performance as a whole.
- **Chapter 3:** Consider changing the main inductor (the one that is not magnetically coupled with the rest) of the Horates V3 circuit for a hand-wound inductor, to greatly reduce the resistance and verify the effect it has in efficiency and startup voltage. This inductor should be fully characterized through an LCR with an appropriate bandwidth

or a Vectorial Network Analyzer (VNA), to verify further more the validity of the startup voltage equation proposed.

- **Chapter 4:** Improvements can be made to the Horates V4 circuit, in particular, to the storage capacitor of the startup circuit, to allow the use of a big capacitance of $\approx 620\mu F$, instead of the current $220\mu F$ being used. This change results in a longer startup time, but will allow the square wave oscillator to commute effectively for more time, consequently reducing the startup voltage, as the output capacitor of the DC-DC converter would have more time to be fully charged. Furthermore, changing the inductance of the converter, as it was mentioned in chapter 4, will significantly reduce the power consumption while improving the resolution of the MPPT method.
- **Chapter2/Chapter 4:** Translate the Horates V4 circuit to a flexible hybrid electronics based design. To this end, redundant circuits can be cut or replaced to reduce the footprint size and layout complexity. Such examples are presented primordially in chapter 4, where changes made to the original schematic are shown. One such change is the replacement of the window comparator, conformed by two resistive dividers and a dual-comparator Integrated Circuit (IC), for the power supervisor peripheral of the microcontroller.

Glossary

***I*²C** Inter-Integrated Circuit. 32, 42

ASIC Application-Specific Integrated Circuit. 7, 8, 51, 164

BJT Bipolar Junction Transistor. xiii, 56, 57, 59, 95

CCM Continuous Conduction Mode. 95, 96, 130

COT Constant On-Time. 130

COTS Commercial Off-the-Shelf. 7, 8, 14, 18, 30, 31, 51, 57, 60, 67, 78, 87, 164

CPC Constant Peak Current. xvii, 134

CR Conversion Ratio. 6, 12, 58, 59, 76, 96, 97

DC-DC Direct Current - Direct Current. xi, xv, 6–8, 11, 12, 14–19, 51, 60, 84, 87, 93–96, 99, 107, 109, 115, 116, 120, 123, 124, 127, 128, 136, 144–146, 151, 164–166

DCM Discontinuous Conduction Mode. 95, 118, 130

ECA Electrically Conductive Adhesive. xi, 16, 30, 43

EEPROM Electrically Erasable Programmable Read-Only Memory. 31, 32, 40

EMI Electromagnetic Interference. 109, 110, 115

EXTI External Interruption. 136, 144

FHE Flexible Hybrid Electronics. 27

- FOCV** Fractional Open-Circuit Voltage. 98, 101, 104, 106
- FR-4** Flame Retardant Laminate 4. 30, 38, 168
- FSCC** Fractional Short-Circuit Current. 101
- Horates V2.1** Horates V2.1 circuit, a flexible environmental sensing tag made over a copper-clad polyimide substrate. 31, 48, 162
- Horates V2.2** Horates V2.2 circuit, a rigid environmental sensing tag made over a rigid Flame Retardant Laminate 4 (FR-4) substrate. xii, 38–40, 48, 162
- Horates V2.3** Horates V2.3 circuit, a flexible environmental sensing tag made over a Polyethylene Terephthalate (PET) substrate. xii, 42, 44, 45, 47, 48, 162
- Horates V3** Horates V3 circuit, a self-powered oscillator. xiii, xiv, 65, 66, 69, 70, 78, 79, 82–84, 87, 151, 164, 165
- Horates V4** Horates V4 circuit, a DC-DC converter circuit that integrates the Horates V3 circuit in its startup circuit stage. 87, 151, 164, 166
- IC** Integrated Circuit. 27, 32, 35, 54, 58, 98, 119, 126, 132–134, 143, 166
- INC** Incremental Conductance. 101–103
- IoT** Internet of Things. iv, 2, 31, 162
- IRA** Internal Resistance Adaptive. 106
- JFET** Junction Field Effect Transistor. 56, 74, 164
- LDO** Low Dropout Output. 37, 38
- LPTIM** Low Power Timer. 135, 136, 139, 143, 147, 148
- LUT** Look-up Table. 104
- MCU** Microcontroller Unit. 114, 144
- MPP** Maximum Power Point. xviii, 102–104, 118, 136, 137, 139, 147, 149, 150, 153
- MPPT** Maximum Power Point Tracking. iv, 11, 18, 52, 84, 87, 98, 100, 101, 103, 104, 106, 107, 118, 128, 130, 133–137, 147, 151, 164–166

NFC Near Field Communication. 32, 35, 38, 40, 48, 162

O&SO Observation and self-optimization (O&SO). 104

OCV Open-Circuit Voltage. 101

OTEG Organic Thermoelectric Generator. 1, 4, 7

P&O Perturbe and Observe. 101, 102, 104

PCB Printed Circuit Board. xi, xviii, 16, 17, 30, 31, 42, 146

PET Polyethylene Terephthalate. 16–18, 30, 42, 43, 168

PV Photovoltaic. 101, 102

PVD Programmable Voltage Detector. 139, 144

RF Radiofrequency. 2

SCC Short-Circuit Current. 101

SPDT Single Pole Double Throw. 15

SWCNT Single-Walled Carbon Nanotubes. 11

TEG Thermoelectric Generator. iv, x, 1–4, 8, 10–12, 15, 17, 31, 34, 40, 48, 51–53, 60–63, 83, 96, 97, 100, 101, 103–105, 148, 162, 164

VLSI Very Large Scale of Integration. 18, 53, 54, 56

VNA Vectorial Network Analyzer. 166

WP Work Package. 4

ZCS Zero Current Switching. 98, 104, 142, 143, 147

Annex A

Publications

1. L. Franke, A. Georg Rösch, M. I. Khan, Q. Zhang, Z. Long, I. Brunetti, **M. N. Joglar**, A. M. Lara, C. D. Simão, H. Geßwein, A. Nefedov, Y. M. Eggeler, U. Lemmer, M. M. Mallick, High Power Density Ag₂Se/Sb_{1.5}Bi_{0.5}Te₃-Based Fully Printed Origami Thermoelectric Module for Low-Grade Thermal Energy Harvesting. Adv. Funct. Mater. 2024, 2403646. <https://doi.org/10.1002/adfm.202403646>
2. **Joglar, Matias** and Brunetti, Irene and Zhang, Qihao and Franke, Leonard and Roesch, Andres Georg and Mallick, Md Mofasser and Moya, Ana and Lemmer, Uli and Delgado Simão, Claudia, Printed Teg Based Energy Harvesting System Driven by Self-Powered Low-Power Oscillator. Available at SSRN: <https://ssrn.com/abstract=4890153> or <http://dx.doi.org/10.2139/ssrn.4890153>. Submitted to Energy Conversion and Management, Manuscript Number: ECM-D-24-07056.

Printed TEG Based Energy Harvesting System Driven by Self-Powered Low-Power Oscillator

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Abstract

Environmental Energy Harvesting (EH) is a sustainable energy source which can be used to power electronic devices, and its implementation is of paramount importance since the emerging of technologies like Wireless Sensor Networks (WSN). EH can be used as the main power source in ultra-low-power applications, or as an auxiliary source, supplementing batteries or supercapacitors. This work introduces an energy-harvesting system comprised of a novel fully screen-printed flexible inorganic Thermoelectric Generator (TEG) and a novel self-powered oscillator. As the output voltage of the TEG at low temperatures is not enough to power conventional electronic devices, the self-powered oscillator boosts its voltage to meet the requirements. The TEG is prepared by a screen-printing process, without the addition of complex extra processing steps, provides a normalized power of $6nWcm^{-2}K^{-2}$. With this normalized power, a screen-printed 5cm x 5cm device was able to initiate the novel self-powered oscillator with a ΔT of only 7.5 K. The self-powered oscillator is based on a Hartley oscillator, has a startup voltage of 9.3mV, a startup input power of 7.7 μ W, a minimum conversion ratio (amplification of the input voltage) of 50 times for input voltages greater than 20mV, and it is made with Commercial Off-the-Shelf (COTS) components for a cost-effective and scalable implementation. The theoretical analysis is validated through characterization of the devices, and the implementation of a custom DC-DC converter powered by the oscillator. The whole system is presented as a potential power source for energy-harvesting applications.

Keywords: Printed TEG, Flexible inorganic materials, Energy Harvesting, DC-DC converter, Energy Harvesting, Oscillator.

1. Introduction

In an era of abundant IoT devices, including wearables and Wireless Sensor Networks (WSNs), the demand for portable and sustainable power sources has become paramount. Therefore, integrating energy harvesting EH presents an attractive alternative for supplementing or replacing batteries, reducing maintenance, and enhancing overall lifetime.

As low-power electronics have advanced considerably in recent years, the energy demands of components have reduced significantly, reaching the μ W range [1]. This development facilitates the utilization of EH that exploits surplus energy that would otherwise be unused. Dissipated heat is a widely available resource that can be converted into electrical energy in a fully sustainable way by thermoelectric generators (TEGs)[2, 3, 4]. Considering that the majority of excess heat remains below 100°C, TEGs must

demonstrate the capacity to generate enough energy from a low-grade heat source to adequately power an electronic circuit [5]. The challenge of producing a small-area low-cost TEG capable of adapting to non-flat surfaces, maximizing the utilization of the waste heat to generate sufficiently large power, remains ongoing [6, 7].

Traditional inorganic TEGs suffer from high costs, complicated manufacturing techniques, and issues with integration and customization [8]. Conversely, solution processable inks suitable for large-area printing methods, including 3D printing, inkjet printing, and screen printing, have significantly lowered production costs and are more environmentally sustainable [9]. Among these techniques, screen printing stands out for its capability to produce a high number of scalable devices in a short time, making the process suitable for industrialization. However, the majority of screen-printed inorganic devices described in literature necessitate costly and time-consuming additional post-processing steps beyond the printing [10, 11, 12], making the industrialization process more complex.

In this work, a fully screen-printed TEG is presented, fabricated without the need for complicated assembly pro-

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cesses. Additionally, when harvesting energy from low-temperature sources, usually the output voltage of TEGs is too low to directly power an electronic device. Hence, there is a need for DC-DC converters, which act as an interface to boost this voltage to the required level.

One of the challenges to overcome involves the minimum voltage required by DC-DC converters to start working. In commercially available converters, this startup voltage tends to be high (usually more than a few hundred of mV) [13], demanding the use of a startup stage, in charge of amplifying the voltage to the point where the DC-DC converter starts working independently. This startup stage is generally much less efficient than the main converter, but also has lower power requirements. While there are converters working with lower voltages, such as the LTC3107/LTC3108 (Analog Devices) [14], which has been often utilized in articles regarding energy harvesting, these kinds of circuits usually have some drawbacks such as lack of Maximum Power Point Tracking (MPPT), good efficiency only in a narrow voltage range, and high current draw at the input, limiting their use with sources of moderately high output resistance.

Accordingly, for the energy-harvesting system to work, the TEG must provide a minimum voltage set by the startup stage. Therefore, this startup stage is crucial to minimize the area of the TEG, proportional to the number of thermocouples n , as well as the ΔT needed. For this reason, the focus is on developing DC-DC converters with ultra-low startup voltages and Maximum Power Point Tracking (MPPT) methods to improve efficiency in these ultra-low power cases [15, 16].

DC-DC converters developed within integrated circuits offer greater flexibility for designs aimed at low-voltage and low-power applications when compared to converters designed using discrete components. This is primarily due to some key advantages: the transistors employed in ICs typically have lower threshold voltages (V_{th}), resulting in inherent lower power consumption; increased availability of depletion MOSFETs (normally-ON devices), as well as an increased availability of low-power control methods [17]. Additionally, DC-DC converter topologies such as charge pumps are easier to escalate, for large voltage amplification, while maintaining good efficiency [18]. Conversely, discrete DC-DC converters for low-voltage applications are predominantly constrained to self-powered oscillator topologies [19, 20], but they are significantly less expensive than integrated circuits for low production volumes [21]. For a more comprehensive analysis of current DC-DC converter topologies, the reader are referred to recent review articles [22, 23, 24].

Interestingly, [25] aims to fill a research gap, where the harvesting system is analyzed holistically, not only analyzing the TEG as an isolated device, but in the context of an energy harvester system combining the TEG and the circuit used for voltage amplification. In this sense, the work reports the material synthesis for the TEG, as well as the design, optimization and fabrication of the module. Fur-

thermore, the TEG is connected to a commercial DC-DC converter with an efficiency of around 21%. Other example is the work reported by [26], that presents novel TEG devices in the context of a portable energy harvesting system through the use of a commercial DC-DC converter. However, the drawback of this approach is that commercial DC-DC converters used with low input voltage generators usually have low efficiency. Lastly, [27] introduces an energy harvesting system where the main amplification chain is composed of a custom-made DC-DC converter, with MPPT method and ZCS (Zero Current Switching) implementation, for a more efficient amplification process. This DC-DC converter is cascaded with a commercial DC-DC converter for extra amplification. The peak efficiency for the whole system is 75.4%.

In this work, a novel discrete self-powered oscillator, with ultra-low working voltage and high conversion ratio is introduced in this article, and it is used as the startup stage of a custom DC-DC converter. This self-powered oscillator, along with the previously presented printed TEG and the custom DC-DC converter, is part of a cost-effective, small-area energy-harvesting system, oriented to applications powered by waste heat.

The paper is structured as follows: the fabrication process of the fully printed TEGs and their characterization (Section 2), are presented, along with the explanation of the working principle of the DC-DC converter circuit, derivation of the equations describing its operation, and relevant experimental verification (Section 3). Lastly, the self-powered oscillator is connected to the custom-designed boost converter, to be used as a startup stage, and the system is used to charge a supercapacitor (Section 4).

2. TEG

2.1. TEG fabrication

A vertical structure is needed to enhance the density of the thermocouples per unit area, thus elevating voltage output and facilitating efficient thermal contact with the heat source and sink. The TEGs were fully screen-printed following using inorganic nanomaterials following the design presented in Ref. [28]. Two layers of carbon paste (Dycotec DM-CAP-4701S) were added, one for the top and one for the bottom contact, to reduce the contact resistance between the silver contact and the inorganic thermoelectric nanomaterials [29]. Each TEG with an area of 5 cm x 5 cm had 32 thermocouples made of n-type and p-type inorganic materials made of n-type and p-type inorganic printed TE materials.

An anodized aluminum foil product by Steinert GmbH (65 μ m) with a high thermal conductivity, was selected as a substrate to increase the effective gradient of temperature along the legs, and maximize the power output.

The TEGs were made with seven screen-printed layers stacked on top of each other. The Fig. 1f-c depict the deposition of the last two layers. At first, a commercially

available silver (LOCTITE ECI 1010 E&C) bottom contact was screen-printed, followed by a layer of commercially available carbon paste using the same screen and layout (Fig. 1a). Subsequently, the insulator layer was screen-printed with square cavities to create a container for the thermoelectric legs (Fig. 1b). The thermoelectric legs p-type and n-type legs were printed with two different layouts to alternatively fill the cavities (Fig. 1c-d). Finally, a layer of a carbon paste and a silver top contact were printed one after the other using the same screen and layout to complete the TEG and reduce once again the contact resistance (Fig. 1e). For the concluding step, the devices were annealed for 5 minutes inside a N_2 -filled glovebox at 400 °C to sinter the inorganic materials. No further fabrication steps were needed.

The geometrical fill factor (FF) of the TEG architecture, which is the ratio of the area covered by the thermoelectric materials to the total device area can be optimized for specific application scenarios and depends on layer thickness limitations and the resolution of the printing method. Here, we use a fill factor of 0.3. Fig. 1h shows a photograph of a fully screen-printed TEG fabricated according to the described method. The entire thickness of the device, excluding the thickness of the substrate, was measured with a digital electronic micrometer and was found to be 175 μm .

The n-type and p-type inorganic pastes were prepared following the same in-home one-pot methods reported in the article [30]. These inorganic thermoelectric inks demonstrated exceptional performance from a thermoelectric perspective. The p-type [31] $Bi_{0.5}Sb_{1.5}Te_3$ -based printable TE material exhibited a power factor (PF) of 24 $\mu W cm^{-1} K^{-2}$, whereas the PF of type n-type Ag_2Se -based printable TE material measured 10.5 $\mu W cm^{-1} K^{-2}$. The PF s were measured at room temperature after the sintering.

2.2. Characterization of the TEG

Two different TEGs (*dev A*, *dev B*) printed following the process previously described, were characterized. The *dev A* and *dev B* were found to have an internal device resistance of $R_{TEG} = 5.5 \Omega$ and $R_{TEG} = 5.3 \Omega$, indicating the reproducibility of the process.

The 32 thermocouple devices containing 32 thermocouples were characterized using a custom-built setup where the temperature of two copper blocks can be adjusted between 273K - 363K. During the measurement, the devices were clamped between the two copper blocks using thermal paste to improve the thermal contact. The devices were characterized by measuring the current-voltage curve using a Keithley 2601B (SMU) after establishing a steady ΔT . Moreover, the power output (P_{OUT}) was evaluated.

Small ΔT under 20 K were selected to simulate real conditions for an IoT application. Fig. 2a-b show the ideal behaviour of the TEG. The open circuit voltage (V_{OC}), i.e. the voltage provided by the TEG without any load, exhibits a linear dependence with respect to ΔT .

Moreover, the P_{OUT} of the fully printed TEG show an ideal behaviour with maximum power output $P_{OUT MAX}$ when the load resistance is matched to the internal resistance following the equation: [32]

$$P_{OUT} = \frac{V_{OC}^2 R_{LOAD}}{(R_{LOAD} + R_{TEG})^2} \quad (1)$$

The $P_{OUT MAX}$ of the *dev A* and *dev B* are reported as a function of the absolute ΔT in Fig. 2c. The P_{OUT} follow the ideal parabolic behaviour showing an outstanding reproducibility of the fully printed TEGs made following this fabrication method.

This printing method produced functional flexible inorganic TEGs showing the possibility of making fully printed devices without time-consuming extra-steps, except from the short annealing.

2.3. Performance of printed devices

In IoT applications, one of the fundamental parameters is the area occupied by the devices [33]. With regard to thermoelectric devices, the objective is to maximize power density per unit area, thereby facilitating high power output for a restricted area. Another critical parameter is the temperature difference required to achieve a given power output. In order to consider these factors and to compare the device with the state of the art, a crucial parameter for TEGs has been computed: the power normalized per device area and the square of the applied temperature difference [34]. Specifically, *dev B* shows a normalized power of $6 nW cm^{-2} K^{-2}$, which is in line with the state-of-the-art for inorganic TEGs [35, 36, 37, 38].

The TEGs further exhibited a noteworthy flexibility, which is essential in applications where conformability and durability are required. The resistance remained constant even when the TEG was rolled into a cylinder with a bending radius of 2.75 cm (see Fig. S1 of the supporting information).

Stability of power output over time is a very important parameters for IoT applications. The characterization of the *dev B* was repeated after one month to verify its stability. The current-voltage curve of the *dev B* measured one month after the first measurement is reported in Figure S2 of the supporting information. The $P_{OUT MAX}$ measured one month later and initial $P_{OUT MAX}$ measured one month earlier are depicted in Fig. 3a. The powers follow the same parabola with a R-square (COD) of 0.99297, showing promising stability over time.

3. Oscillator Circuit Architecture

3.1. Description of the oscillator operation

The circuit (Fig. 4) is based on a Hartley oscillator [39], a topology consisting of a tank circuit conformed by

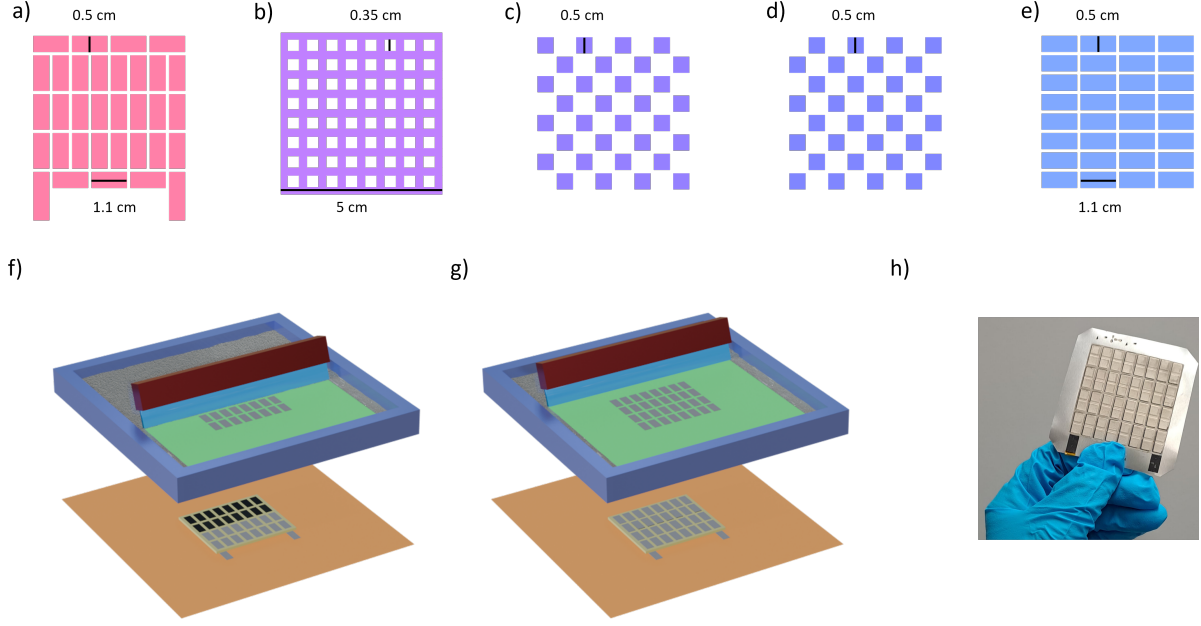


Figure 1: Layouts of the screen printed layers : a) the bottom contact silver and carbon layers, b) the insulator layer, c) the p-type legs layer, d) the n-type legs layer, and e) the top contact silver and carbon layers. Sketch of the last screen-printed layer of the vertical TEGs on the Aluminium oxide foil. The sketch shows two moments of the printing step of the silver top contact: f) in the middle (16 thermocouples) and g) at the end (32 thermocouples). h) Photograph of the screen-printed TEG.

two inductors in series (which might be coupled or not), in parallel with a capacitor, and an amplifier element between the tank and the terminal between both inductors.

When using a JFET as the amplifier element, this topology has an inherent limitation on the output voltage, due to the p-n junction between gate and source that constitutes a diode. This diode conducts during the oscillation positive interval, dampening the oscillations and introducing distortion in the signal. While this behavior might be useful in applications where a limited output level is needed, it reduces the maximum amplification achievable when using it as a startup stage for other circuits.

Therefore, one way to overcome this limitation is to add a capacitor in series with the inductors. This facilitates the storage of the negative voltage generated by the oscillation during the transistor OFF state and shifts the gate bias voltage of the transistor away from positive values [40]. While this approach does not eliminate entirely the dampening produced by the conducting gate, it notably diminishes it, facilitating larger excursions in the oscillation. As a result, the circuit is enhanced by introducing a bias-altering capacitor, referenced to the ground, to obtain a DC output with reduced ripple and a simplified connection for loads referenced to the same ground.

The contribution to voltage amplification in this circuit is twofold. The first amplification comes from two Commercial Off-The-Shelf (COTS) coupled inductors introduced in the circuit design to reduce the startup voltage and amplify the magnitude of the oscillations, as part of the input voltage is amplified by the turn ratio (N) of the

coupled inductors. The second amplification comes from the inductors L_1 and L_2 , as L_2 discharges during resonance, with a current $I_{L_2} = V_{L_2}/(j\omega_o L_2)$, where V_{L_2} is the voltage over L_2 and ω_o the circuit resonance frequency, so the voltage over L_1 is equal to $V_{L_1} = V_{L_2} L_1/L_2$, effectively amplifying V_{L_2} by a factor L_1/L_2 .

The coupled inductors added to the circuit generate a marginal compromise in design flexibility, although the utilization of commercially available options offsets this concern.

The oscillation process is the same as in a classical Armstrong oscillator with a JFET as the amplifier element, but taking into consideration that the storage capacitor, C_1 , gets charged with a negative voltage V_{DC} during the OFF-state of the transistor, altering the bias voltage of the gate [19].

3.2. Theoretical analysis

The small-signal model of the circuit is obtained to derive the equations for the voltage required for startup. To this end, the following considerations are taken:

- C_1 , the storage capacitor, can be considered a short-circuit at the resonance frequency, since $C_1 \gg C_{osc}$.
- Since $V_{DS} \ll |V_P|$, the JFET works in the ohmic linear region, where it behaves as a voltage-controlled resistor. Its small-signal behavior is represented by a current source $g_m V_{gs}$, with g_m being the transconductance and V_{gs} the dynamic gate-source voltage, while a resistor $R_{DS_{on}}$, equal to the zero-gate-source

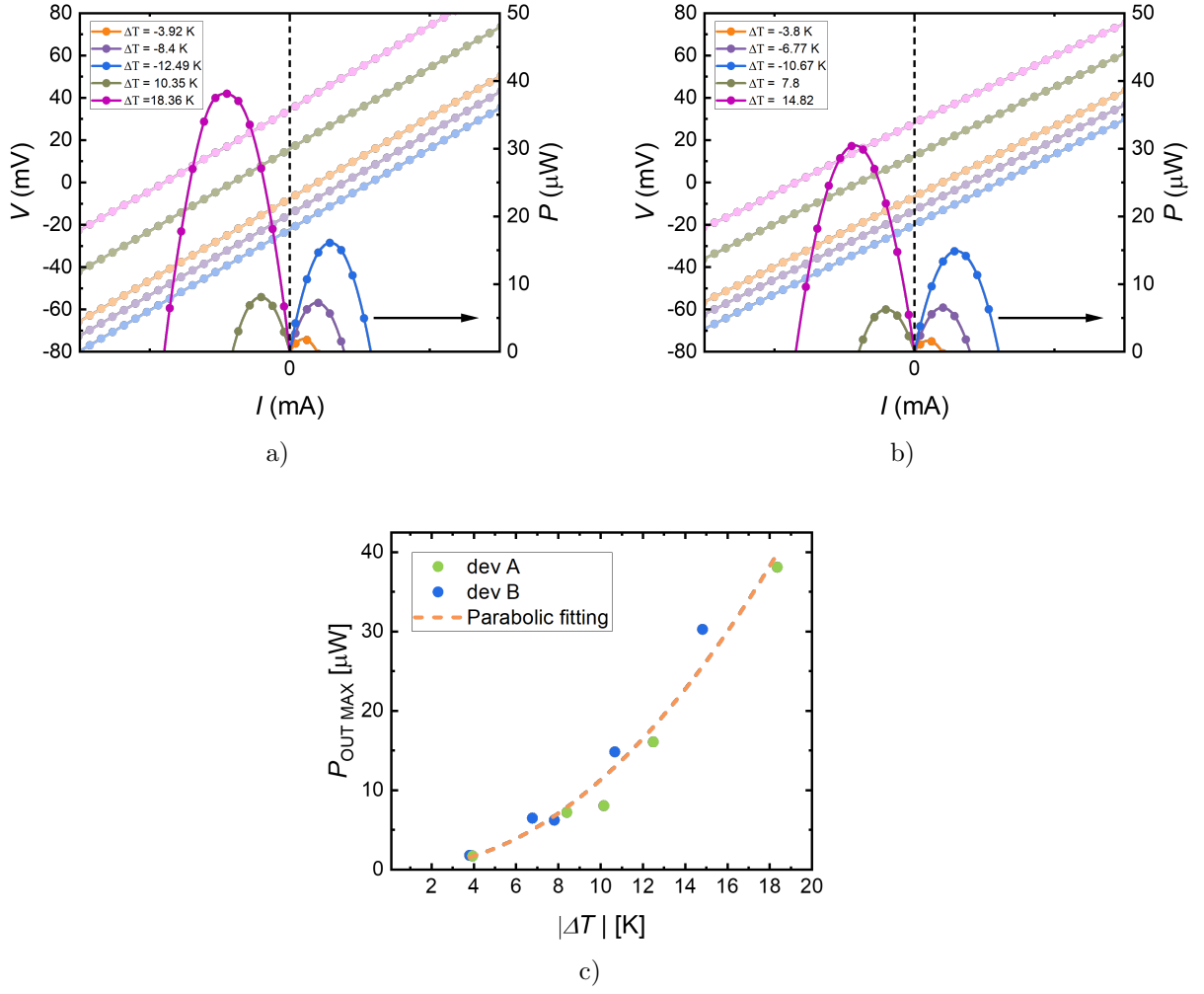


Figure 2: V_{OUT} (left y-axis) and P_{OUT} (right y-axis) as a function of the current applied to the printed TEG for two different devices: a) Device A, b) Device B. c) P_{OUT_MAX} of Device A (green dots) and B (blue dots) as a function of the absolute value of the ΔT , fitted with a parabolic curve.

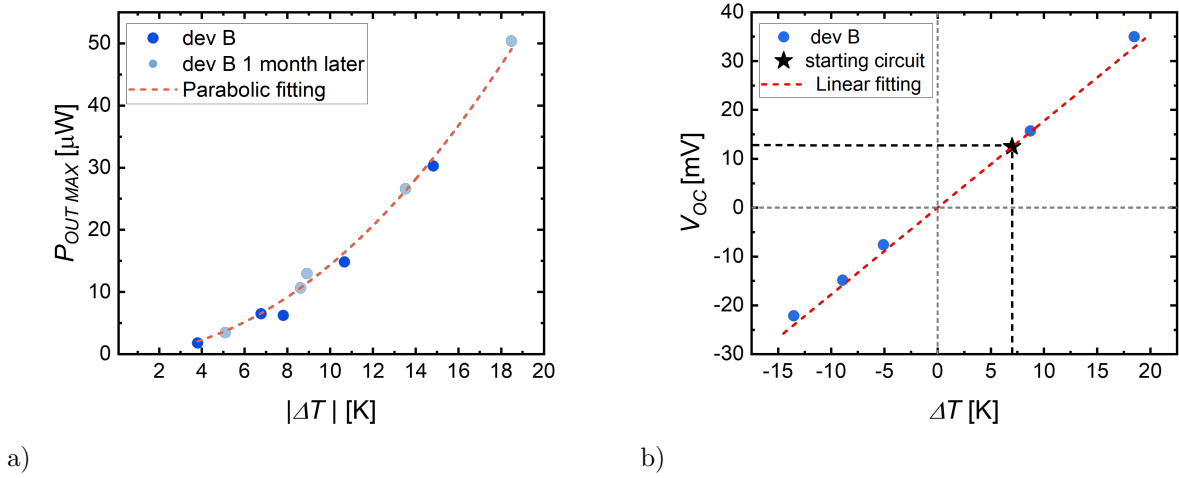


Figure 3: a) P_{OUT_MAX} of device B at day 0 (blue dots) and 1 month later (light blue dots) as a function of absolute value of the ΔT , fitted with a parabolic curve. b) V_{OC} (green dots) of device B as a function of ΔT . The black star shows the V_{OC} necessary to start the circuit proposed in this article.

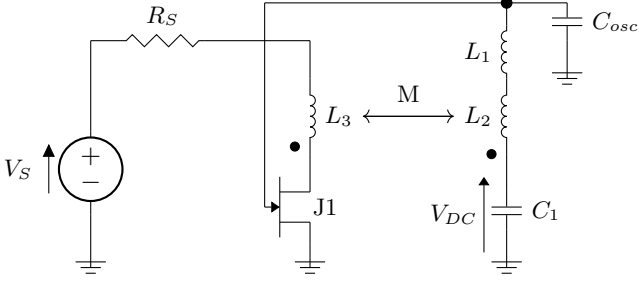


Figure 4: Oscillator circuit schematic

voltage drain-source resistance, represents the bias condition during startup when the gate-source voltage is near 0.

- The first analysis is performed with ideal passive components and source resistance $R_S = 0$.

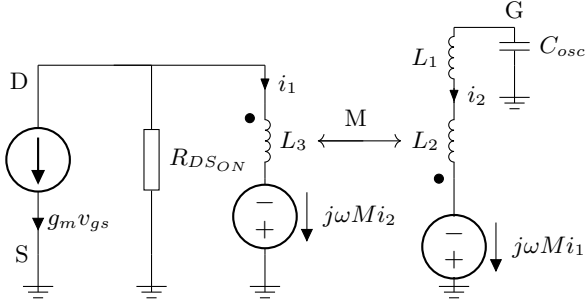


Figure 5: Small-signal model of the oscillator circuit during startup

Once the small-signal model (Fig. 5) is obtained following the previously stated criteria, Kirchhoff's laws are applied to it, leading to the following equations describing the circuit

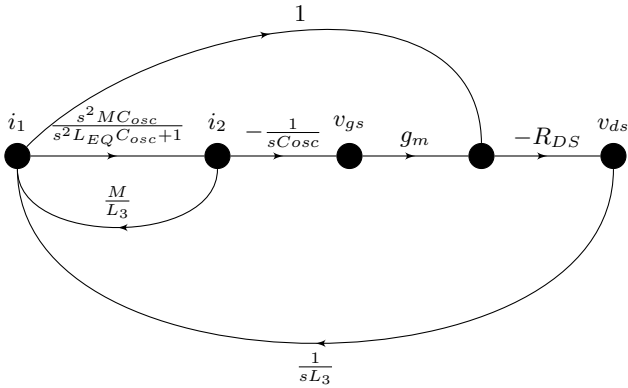


Figure 6: Flowgraph describing the circuit

$$v_{ds} = i_1 R_{DS_{on}} - R_{DS_{on}} g_m \frac{i_2}{s C_{osc}} \quad (2)$$

$$i_1 = \frac{s M i_2 - v_{ds}}{s L_3} \quad (3)$$

$$v_{gs} = \frac{i_2}{s C_{osc}} \quad (4)$$

$$i_2 = \frac{s^2 M C_{osc} i_1}{s^2 L_{eq} C_{osc} + 1} \quad (5)$$

where $L_{eq} = L_1 + L_2$.

These equations are then used to produce the signal flow graph in Fig. 6, from which the characteristic equation (the determinant of the graph) of the circuit is obtained through the use of Mason's gain formula, as described in [41].

The loop gains in the graph are as follows:

$$T_1 = \frac{s^2 M^2 C_{osc}}{L_3 (s^2 L_{eq} C_{osc} + 1)} \quad (6)$$

$$T_2 = \frac{s^2 M C_{osc} g_m R_{DS_{on}}}{s^2 C_{osc} L_3 (s^2 L_{eq} C_{osc} + 1)} \quad (7)$$

$$T_3 = -\frac{R_{DS_{on}}}{s L_3} \quad (8)$$

Consequently, the characteristic equation is

$$\Delta = 1 - T_1 - T_2 - T_3 = 0 \quad (9)$$

and it is evaluated in the Fourier domain ($s = j\omega$). The oscillation frequency ω_o is obtained equating the real term to 0:

$$\omega_o = \frac{1}{\sqrt{C_{osc} L_{eq}}} \quad (10)$$

Meanwhile, the instability condition is determined by the imaginary part of the equation being less than 0, when ω is replaced by the resonance frequency ω_o .

$$g_m R_{DS_{on}} > \frac{M}{L_{eq}} \quad (11)$$

To put the equation in terms of the input voltage, we replace g_m and $R_{DS_{on}}$ by their actual values during startup, when $V_{GS} \approx 0$.

$$I_{DS} = \frac{2 I_{DSS}}{V_P^2} (V_{GS} - V_P - \frac{V_{DS}}{2}) V_{DS} \quad (12)$$

$$R_{DS_{on}} = \frac{V_{DS}}{I_{DS}} = \frac{|V_P|}{2 I_{DSS}} \quad (13)$$

$$g_m = \frac{d(I_{DS})}{d(V_{GS})} = \frac{2 I_{DSS}}{V_P^2} V_{DS} \quad (14)$$

Then, as $V_{DS} \simeq V_S$ on startup, and $R_S = 0$:

$$V_S > \frac{k \sqrt{L_3 L_2}}{(L_1 + L_2)} \cdot |V_P| \quad (15)$$

Which for a turn ratio of N , assuming $L_3 = L_2/N^2$ turns to

$$V_{IN} > \frac{kL_2}{N(L_1 + L_2)} \cdot |V_P| \quad (16)$$

and the startup voltage is N times smaller than it would be while using just an inductor L_2 of the same value without the addition of coupled inductors.

It can also be appreciated that the startup voltage is directly proportional to the coupling factor (k) of the inductors, and it is proved through simulations that diminishing the coupling factor also reduces the startup voltage. Nonetheless, as expected, this only applies to a circuit with ideal components, where both inductors and the voltage source do not have any resistance.

The next step deriving the startup voltage equation is to add resistance to these ideal components. R_S corresponds to the voltage source resistance, while r_1 corresponds to the series resistance of L_1 and L_2 . The resistance of L_3 is counted as part of R_S , and the Equivalent Series Resistance (ESR) of the capacitors is ignored. To simplify the calculations, the coupling between inductors is considered perfect, so $k = 0$ and $M = \sqrt{L_2 L_3}$. To calculate the new ω_o and oscillation condition, the loop gains are calculated with the new parameters, and the previous process is repeated.

$$T_1 = \frac{s^2 M^2 C_{osc}}{L_3(s^2 L_{eq} C_{osc} + r_1 s C_{osc} + 1)} \quad (17)$$

$$T_2 = \frac{M g_m R_{DS_{on}}}{L_3(s^2 L_{eq} C_{osc} + r_1 s C_{osc} + 1)} \quad (18)$$

$$T_3 = -\frac{R_{DS_{on}}}{s L_3 + R_S} \quad (19)$$

The oscillation frequency in this case is described by:

$$\omega_o^2 = \frac{L_3(R_S + R_{DS_{on}}) - M g_m R_{DS_{on}} R_S}{C_{osc}(L_3^2 r_1 + L_{eq} L_3(R_S + R_{DS_{on}}) - M^2 R_S)} \quad (20)$$

Meanwhile, to find the oscillation condition (or the startup voltage), an additional consideration must be made, as the analysis now includes R_S . Just before the start of the oscillations, the behavior of L_3 would be dominated mainly by its resistance, r_3 . As a small inductance, $R_S \gg r_3$ and $R_{DS_{on}} \gg r_3$ its assumed, so the drain-source voltage is

$$V_{DS} = V_S \frac{R_{DS_{on}}}{R_{DS_{on}} + R_S} \quad (21)$$

Evaluating Eq. 22, it can be concluded that there are tradeoffs when trying to reduce the startup voltage, mainly between L_1 and its resistance, r_1 , as well as between L_2 and the turn ratio N . Meanwhile, just looking at the equation, C_{osc} could be reduced all the way, but in reality, that raises the frequency and might affect L_1 and r_1 . Effects

such as skin effect or core losses are more appreciable at higher frequencies, leading to an increase in r_1 , while L_1 might be diminished due to limitations related to the self-resonance frequency.

One advantage of this circuit is that by introducing the coupled inductors, the requirements for L_1 are relaxed since we can diminish its value (reducing r_1 and raising the self-resonance frequency) and obtain the same effect as in a circuit without coupled inductors. This is especially important since for a low startup voltage, we want C_{osc} to be as low as possible as stated previously.

Then, overall, when using coupled inductors with low turn ratios the circuit will tend to have a lower resistance in the L_1 branch since the resistance of the secondary is not high enough to offset the advantages previously mentioned. Another effect that stems from a lower L_1 is a higher operating frequency, which has a direct positive impact on both efficiency and DC output level, as it reduces the main source of losses, conduction losses in both the transistor and inductors.

3.3. Experimental Results

3.3.1. Oscillator Circuit Design

The circuit was built to validate the theoretical development done. The design criterion for this circuit is to have the minimum possible startup voltage, while matching its input resistance during startup to the resistance of the TEG. To select the JFET, based on the startup equation (Eq. 22), V_P should be as small as possible, as it affects the whole equation. Meanwhile, as the TEG selected has a relatively small resistance $R_{TEG} = 5.5\Omega$, the I_{DSS} of the JFET should be as high as possible. The JFET 2SK3320 was selected, as it fits the criteria, with a V_P between $-0.2V$ and $-1.5V$, and an I_{DSS} between 1.2 mA and 14 mA. As the 2SK3320 is comprised of two N-JFETs in a same package, three of them were used in the circuit, leading to 6 JFETs in parallel in total. This leads to an $R_{DS_{on}} = 5.06\Omega$ using the Eq. 13, with $|V_P| = 0.85V$, as the average between minimum and maximum, and $I_{DSS} = 14mA$, equal to the maximum I_{DSS} . It is important to note that, although it has not been delved into in this article, selecting a smaller V_P will reduce the efficiency and the output voltage, as it reduces the conduction time of the JFET, and therefore, L_3 stores less energy per oscillation cycle. This constitutes a tradeoff between startup voltage and maximum output voltage.

As the circuit was made with COTS components, the next components chosen were the coupled inductors, as their variety is more limited. Based on Eq. 16, it is crucial that the ratio L_2/L_{eq} be as small as possible, since it affects both startup voltage and conversion ratio. Hence, a small L_3 maximizes the benefits, as it allows for a larger N while keeping L_2 small. With this criterion, coupled inductors from the LPR4012 (Coilcraft) series were chosen, with $L_3 = 2\mu H$ and $N = 10$, as it has the highest N of the series, while maintaining L_3 and r_1 small enough.

$$V_S > \frac{R_{DS_{on}} + R_S}{R_{DS_{on}}} \frac{R_{DS_{on}} + r_1(1/N^2 + C_{osc}r_1(R_S + R_{DS_{on}})/L_2 + C_{osc}L_{eq}(R_S + R_{DS_{on}})^2N^2/L_2^2)}{r_1/N + R_{DS_{on}}L_{eq}N/L_2} |V_P| \quad (22)$$

Considering C_{osc} is equal to the C_{iss} capacitance of the JFETs, the last component which affects the startup voltage to be chosen was the inductor L_1 . For this selection, since all the other components had been chosen, the Eq. 22 was used to test different inductors. As mentioned before, the fact that both inductance and resistance are a function of the oscillation frequency should be taken into account. The inductor chosen had an inductance $L_1 = 3.3mH$ and $r_{1DC} = 7.8\Omega$, but when measured at a frequency of 200 kHz using an HM8118 LCR Bridge (Rohde & Schwarz), $L_{1200kHz} = 2.9mH$ and $r_{1200kHz} = 25.7\Omega$. Two of these inductors were used in series, to achieve a higher inductance while maintaining a higher self-resonance frequency than with just one larger inductor.

Lastly, the storage capacitor was chosen to be $C_1 = 220\mu F$, which is a sufficiently high value to not influence the resonance between L_{eq} and C_{osc} . Table 1 presents a summary of the components chosen.

Table 1: List of components used in the oscillator circuit

| Designator | Reference |
|------------|---|
| J_1 | 2SK3320-BL (Toshiba) x 6 |
| L_1 | 17335C (Murata) x 2 |
| L_2 | LPR4012-202LMR ₋ (Coilcraft) |
| L_3 | LPR4012-202LMR ₋ (Coilcraft) |
| C_1 | UKL1A221MPD (Nichicon) |

3.3.2. Oscillator Circuit Characterization

To characterize the circuit, a 2604B Sourcemeter (Keithley) was used as a voltage source V_S , and the output voltage was measured with a 34410A multimeter (Agilent), which can be characterized as a load resistance $R_L = 10M\Omega$.

The voltage V_S was swept starting from zero. The circuit starts working at $V_S = 9.92mV$. The voltage was then increased up to 100 mV in steps of 10 mV in order to measure the output voltage V_{DC} and the ratio between it and V_S , called conversion ratio.

The onset voltage $V_S = 9.92mV$ is equal to $V_{IN} = 9.3mV$ when accounting for the series resistance of the power source and its connection. Moreover, the conversion ratio for the startup voltage is equal to 30 times, while for $V_S \geq 20mV$, the conversion ratio is larger than 50 times, resulting in a significant amplification of the input voltage.

An extra characterization was done after this one, adding a negative voltage rectifier to the gate of the JFET, to obtain a second output with higher amplification than the original one. The resulting circuit schematic can be observed in Fig. S5 in the Supporting Information. The characterization setup is the same as the first one, where the

input voltage is increased in steps of 10 mV until reaching 100 mV. In this case, the onset voltage is $V_S = 10.6mV$, and is equal to a $V_{IN} = 10mV$. The results of both characterizations are shown Fig. 7.

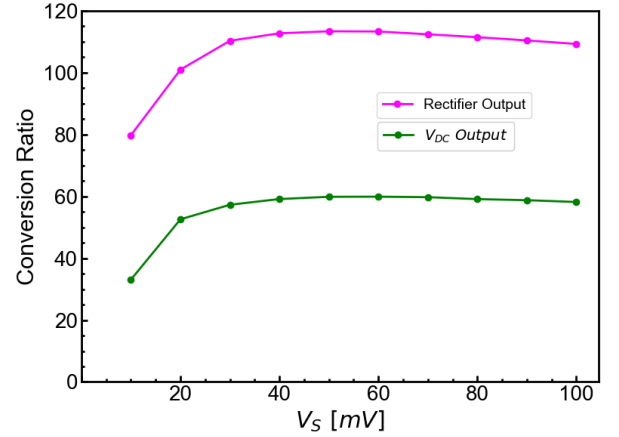


Figure 7: Conversion ratio for the V_{DC} output and for the negative rectifier output

Albeit efficiency (η) is not the focus of this circuit, as it is just expected to work as a startup stage for a more efficient circuit, it was measured using a linear potentiometer as a variable load resistance R_L to achieve maximum power transfer. Results are shown in Table 2.

Table 2: Efficiency of the oscillator circuit

| V_S | R_L | η |
|--------|------------------|--------|
| 40 mV | 473.4 k Ω | 4.46% |
| 70 mV | 423 k Ω | 5.97% |
| 100 mV | 402.5 k Ω | 6.17% |

The input resistance R_{IN} during startup is equal to $R_{IN} \approx R_{DS_{on}}$. Measurements indicate that $R_{IN} = 11.25\Omega$. This value goes up as the circuit starts working, since the channel of the JFET starts getting pinched with the voltage of C_1 . This circuit has potential to be adapted to work with generators with high output resistance, by changing the JFET that acts as switching element. Simulations of this use case are presented in the Supporting Information, in Fig. S5 and Fig. S6. Lastly, in Table 3 a comparison is made against the state-of-the-art in startup circuits made with discrete components.

4. Application

4.1. Startup stage powered by TEG

The oscillator circuit was used first as a step-up stage for the TEG presented in Section 2, as a way to verify

| Ref. | Startup V_{IN} | Startup P_{IN} | Max. Conv. Ratio | Peak η |
|-----------|------------------|------------------|------------------|-------------|
| [42] | 62 mV | 42.2 μW | N/A | 17% |
| [42]* | 6 mV | 0.49 μW | ≈ 280 ** | 12% |
| [21] | 55 mV | 90.5 μW ** | 54 | 1.7% |
| [19] | 100 mV | 3 μW | 10 | 25% |
| [20] | 9 mV | 0.8 μW | 99 | 54.4% |
| [40] | 17 mV | 8.87 μW | N/A | N/A |
| This work | 9.3 mV | 7.7 μW | 60 *** | 6% |

Table 3: Parameters comparison with state-of-the-art startup circuits. * [42] with seven cascaded transformers instead of one. ** Parameters estimated based on available data. *** Can be nearly doubled adding a negative rectifier connected to the gate of the JFET.

the performance of both devices. The TEG was connected to the startup stage and placed in the custom-built setup mentioned in Section 2 to maintain a known and steady ΔT . The ΔT was then increased until the circuit started oscillating. Oscillation was observed for $\Delta T = 7.5 K$. This is considered the ΔT needed for startup. Both the startup ΔT and V_{OC} are shown in Fig. 3b). The custom-built setup, along with this experiment, are presented in Fig. S3 in the supporting information.

4.2. Startup stage powering a DC-DC converter

The second experiment to verify the circuit performance was to use the oscillator circuit as a startup stage for a custom-built DC-DC converter (Fig. 8), using a 2604B Sourcemeter (Keithley) as a voltage source for better control and reproducibility.

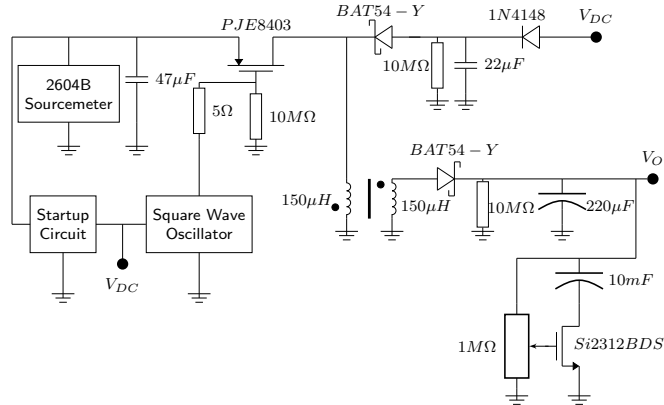


Figure 8: Schematic of the custom-built DC-DC converter

The output of the startup stage was connected to a relaxation oscillator, i.e., a square wave oscillator, made with a TS881 comparator (ST Microelectronics), due to its ultra-low power consumption. This relaxation oscillator was then in charge of driving the gate of the P-MOSFET used in the DC-DC converter as switching element. The converter was not characterized as it was made as a prototype to show the performance of the startup circuit.

The DC-DC converter has two outputs. One with negative voltage (V_{DC}), that was connected through a diode to the output of the startup stage, effectively shutting it down when it was more negative, due to the pinch-off of

the JFET channel. This leads to more efficiency in the converter, as the startup stage stops draining current from the voltage source.

The second output (V_O) is a positive voltage output, and it is connected to a supercapacitor with an N-MOSFET to regulate the output voltage, as shown in [40].

To test the performance of the DC-DC converter, efficiency measurements are done. The supercapacitor is removed, and the DC-DC converter is connected to a potentiometer with a resistance $R_L = 98.4 k\Omega$. Then, the input voltage source is varied from 40 mV to 100 mV in 10 mV steps. The efficiency results are shown in Fig. 9, as well as the output voltage corresponding to each data point. This DC-DC converter has not been optimized for efficiency nor impedance matching with the TEG. If the characteristics of the TEG are known beforehand, the frequency of the square wave oscillator can be altered (changing its tuning capacitor) to match the impedance of both TEG and DC-DC converter. The experiment setup is shown in Fig. S4 in the supporting information.

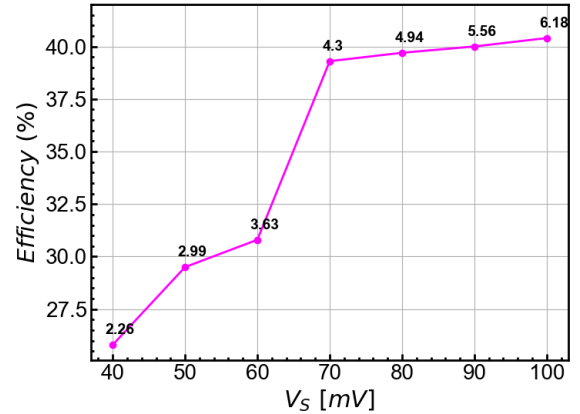


Figure 9: Efficiency of the DC-DC converter with $R_L = 98.4 k\Omega$. Output voltage is expressed over the data points

5. Conclusion

In this work, an environmental energy harvesting unit was prepared in a facile, cost-effective and versatile methodology. The system is composed by a fully-printed flexible

TEG and an ultra-low voltage self-powered oscillator circuit with a high conversion ratio, able to magnify the voltage of low-voltage sources, and made with readily available materials and COTS discrete components. The printed TEG and the high conversion ratio make the whole system a viable alternative as a power source for IoT devices or low-voltage energy-harvesting applications, when paired with a custom-designed DC-DC converter. The TEG and oscillator system starts working at $\Delta T = 7.5$ K, reinforcing its usefulness in low-temperature applications. It has been shown that the oscillator, with a 40 mV input voltage, can power a DC-DC converter while it can also be shut-down after a certain voltage has been reached, improving the efficiency of the whole system. As the next steps, the DC-DC converter design must be optimized, as well as the integration between it and the oscillator to reduce the minimum working voltage of the system.

6. Acknowledgments

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1 Supporting Information

1.1 TEG flexibility and stability

A fully printed TEG was bent to verify its flexibility, crucial feature in application where the portability is needed. The device was bended with a bending radius ranging from 8.5 cm to 2.75 cm. The resistance of the device remained constant with an average error of less than 10%.

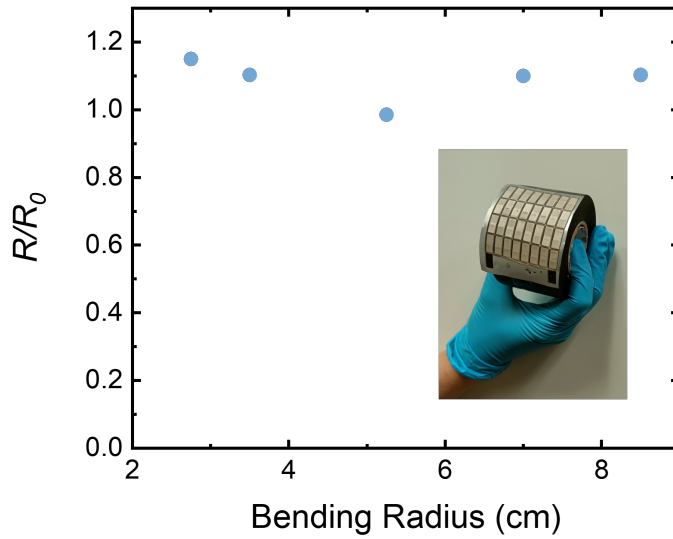


Figure 1: Resistance change ratios of a screen-printed TEG as a function of the bending radius

The *dev B* was measured one month later to verify the stability of the device over the time. Figure 2 shows the current-voltage curve and the P_{OUT} of the *dev B* one month later. The current-voltage measurements of *dev B* were repeated under the same conditions, using the same measurement setup. The device showed stability even after one month.

1.2 Oscillator circuit powered by TEG

A custom-built setup, where the temperature of two copper blocks can be adjusted between 273K - 363K is used to generate a temperature difference along the TEG. The TEG was introduced between the copper blocks, and then was connected to the oscillator circuit. Following that, the temperature of the copper blocks was swept, raising ΔT until the output capacitor of the circuit started

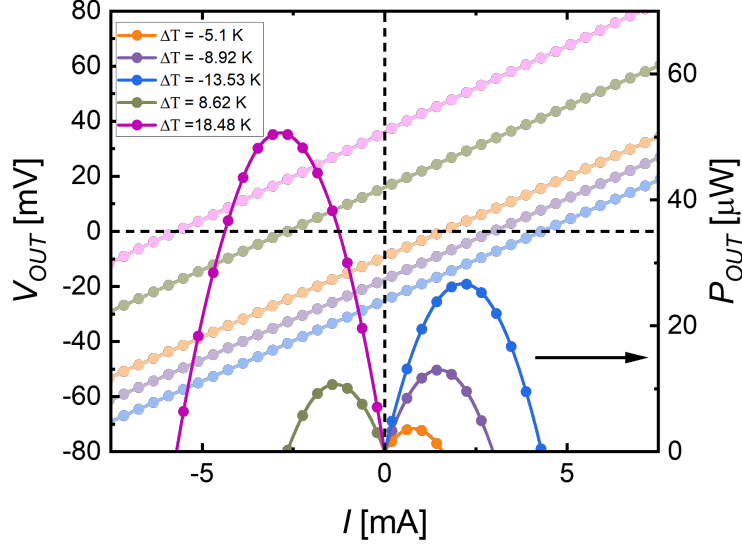


Figure 2: current-voltage curve and the P_{OUT} of the *dev B*

charging. To verify the output voltage level, a multimeter was used. The whole setup is shown in Figure 3.

1.3 Oscillator circuit powering a custom built DC-DC converter

The setup is shown in Figure 4. Refer to video ("DC-DC_ConverterSetup") showing the setup and the output capacitor charging when using a 2604B Sourcemeter (Keithley) as a voltage source.

1.4 Simulation of oscillator operating with high-resistance voltage source

The oscillator circuit was simulated in LTSpice for a voltage source with an output voltage $V_S = 80mV$ and a resistance $R_S = 1k\Omega$. The circuit in the simulation is modified when compared to the one in the main text, as it uses an SST201 JFET instead of a 2SK3320 (Figure 5). The results of the simulations for the steady state of the circuit are shown in Figure 6.

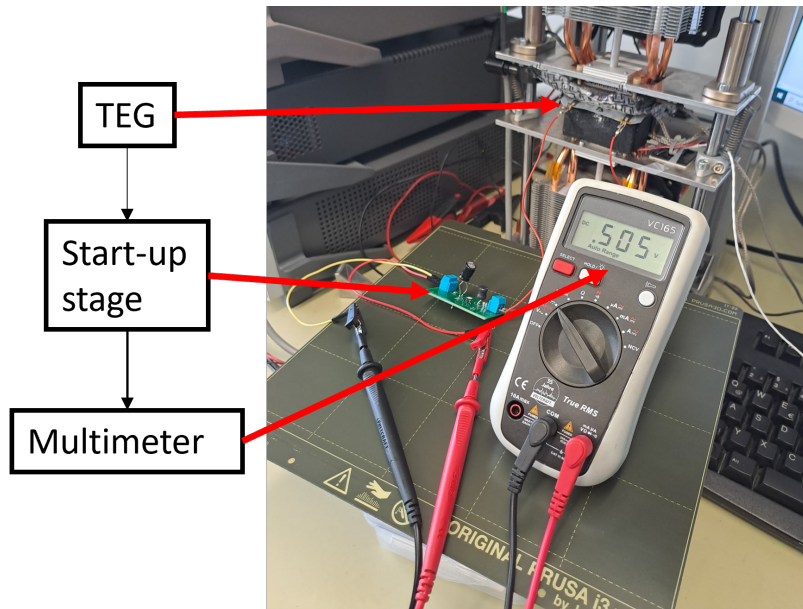


Figure 3: Start-up stage powered by the vertical TEG

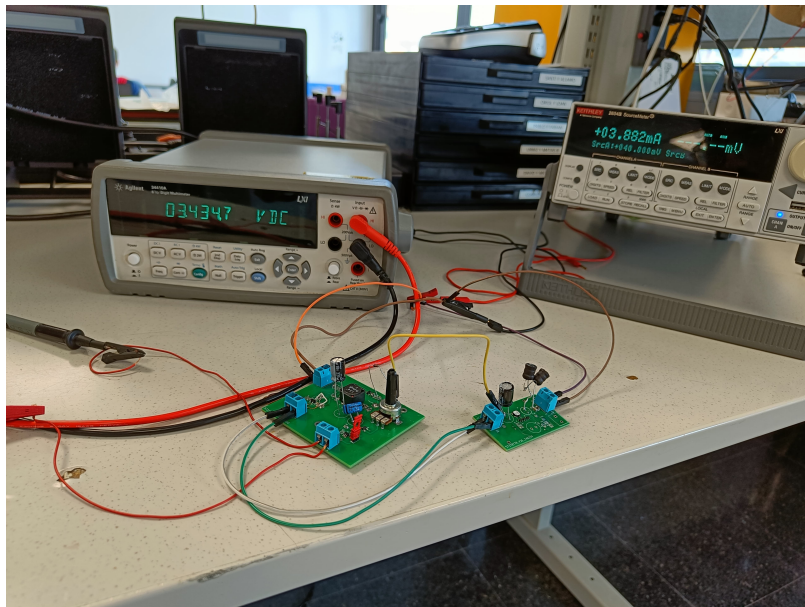


Figure 4: Setup of the DC-DC converter circuit powered by the oscillator

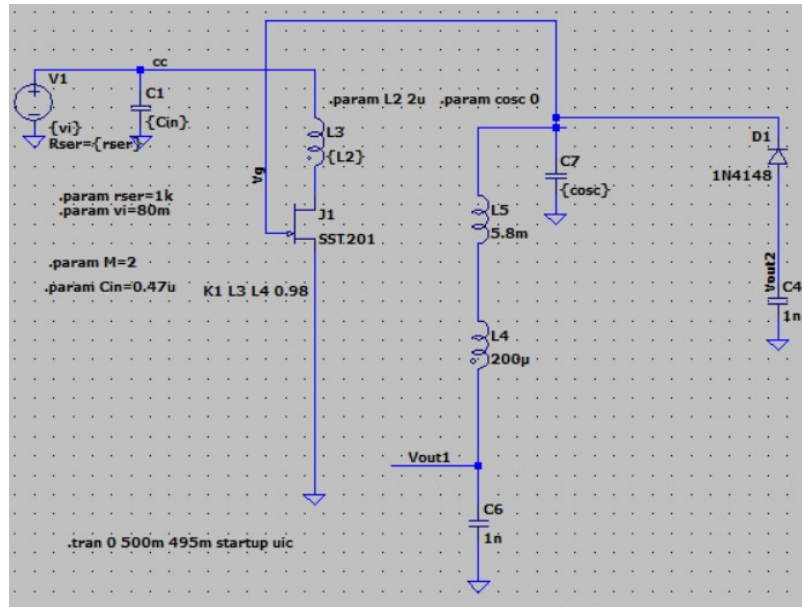


Figure 5: Schematic used for simulation. The original JFET (2SK3320) is changed for a SST201.

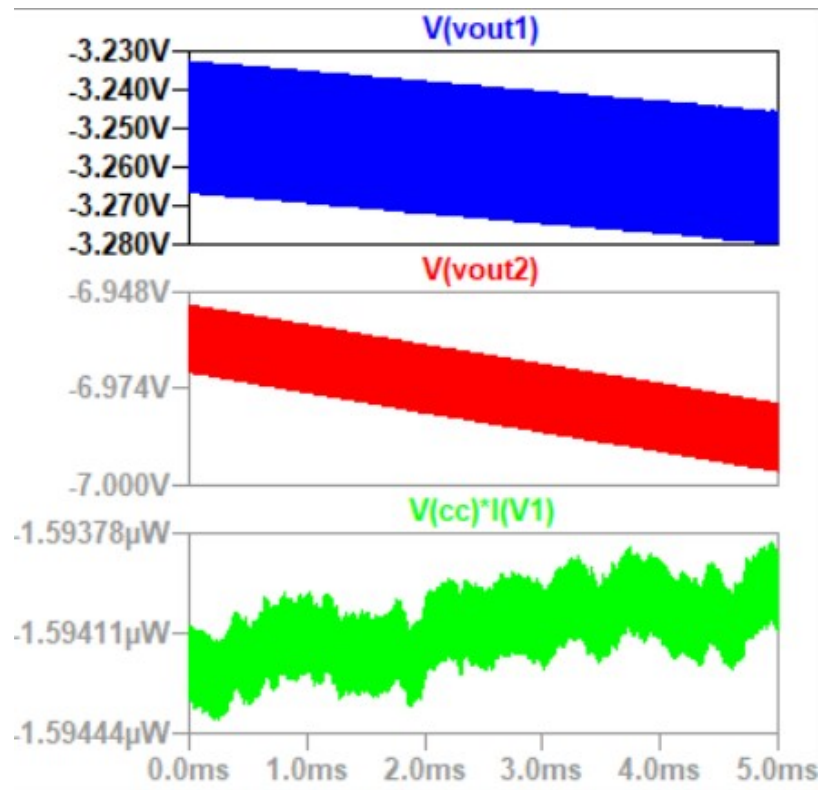


Figure 6: Simulation plot of the steady state of the circuit. From top to bottom: voltage output at capacitor C6, voltage output after the negative voltage rectifier, input power provided by the generator.