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Characterization of degradation induced by BTI, HCI and OFF-State stress, and of the Resistive Switching phenomenon in FD-SOI Ω-Gate NW-FET devices. Analysis of aging relaxation in ring oscillator circuits fabricated in 28nm technology

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Ph.D. Thesis written by

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The undersigned, Prof. Rosana Rodríguez Martínez, Professor of the Electronic Engineering Department (Engineering School) of the *Universitat Autònoma de Barcelona*,

CERTIFY:

That the thesis entitled "*Characterization of degradation induced by BTI, HCI and OFF-State stress, and of the Resistive Switching phenomenon in FD-SOI Ω-Gate NW-FET devices. Analysis of aging relaxation in ring oscillator circuits fabricated in 28nm technology*" has been written by the Ph.D. candidate **Carlos Andrés Valdivieso León** under her supervision, in fulfilment of the requirements of the PhD programme in Electronic and Telecommunication Engineering.

Author:	**Supervisor:**
Carlos Andrés Valdivieso León	Rosana Rodríguez Martínez

Bellaterra (Barcelona), July 2025.

Content

"Aunque nuestro intelecto
siempre quiera claridad y
certeza, a nuestra naturaleza,
normalmente, le parece fascinante
la incertidumbre"

Carl von Clausewitz

Agradecimientos

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Preface

The exponential growth of electronic systems has become essential in recent years. They have enabled significant improvements in many aspects of our lives, such as communication, transportation, and healthcare. Without the invention of the transistor in 1947 by John Bardeen, Walter Brattain and William Shockley, it would not have been possible to understand microelectronics in the 20th and 21st centuries, the miniaturization of electronic devices, and, later, the digitalization of society. Not only has the academic field focused its efforts on these achievements, but also the semiconductor industry, which finances research and seeks profitability for its products by maintaining low prices for consumers. Improvements in fabrication techniques have allowed consumer electronics to evolve. As a result, many different devices have emerged, such as computers, smartphones, and supercomputers.

Nowadays, there is a high demand for highly integrated devices that can storage more information with lower power consumption. The technological roadmap evolves with these new devices. As an example, FinFETs, the gate all around transistors (GAA-FETs) and Ω-gate nanowire FETs fabricated with high dielectric materials (high-k dielectric).

Defects in transistors, such as interface traps and bulk traps, lead to device variations and impact reliability. They become more pronounced with the reduction in technology size. Variations in intrinsic transistor parameters, such as threshold voltage (Vth) or mobility (μ), both after fabrication and over time during circuit operation, are primary causes of performance deviations that can negatively impact integrated circuit (IC) reducing their intended lifetimes. These deviations must be statistically characterized and modelled.

In this context, it is essential to identify the most significant sources of phenomena affecting modern nanometer-scale MOSFETs. Furthermore, methodologies for experimentally characterizing devices to obtain precise transistor parameters due to degradation must be described.

The work presented in this thesis tries to advance in this way. Thus, an experimental characterization of the main failure mechanisms that take place in fully depleted silicon on insulator (FD-SOI) Ω-gate nanowire FETs using high-k dielectric is presented. Aging of these samples due to Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), Off-state stress and dielectric breakdown are studied. The reversibility of the dielectric breakdown also known as resistive switching phenomenon, has also been observed and analyzed in this thesis.

On the other hand, the final goal is to analyze how device degradation affects the circuits performance. In this sense, in this thesis, the degradation of a TSMC array of a high-k ring oscillator is also studied.

In chapter 1, an overview of MOSFETs is provided, discussing their electrical characteristics and reviewing the key milestones in the evolution of electronics in recent years. It will then focus on the topic of variability, with particular attention to the phenomena of time zero variability (TZV) and time dependent variability (TDV), which significantly impact circuit performance and reliability. Then, a detailed explanation of the resistive switching phenomenon is presented.

Chapter 2 will present the samples FD-SOI (Fully Depleted Silicon on Insulator) high-K dielectric transistors used. Then, it will detail the methods used to characterize the aging mechanisms. Besides, the results of the main aging mechanisms will be presented. These mechanisms include BTI degradation, HCI degradation, and Off-state degradation. This chapter will evaluate and compare the degradation mechanisms observed after the stress phases in these samples.

Chapter 3 will address another key topic of this thesis: resistive switching. This phenomenon has been analyzed in the FD-SOI omega gate FETs samples. The chapter will be divided into two parts: first, the recovery of the transistor after the resistive switching phenomenon, and second, the effect of the transistor's back gate on the resistive switching.

Chapter 4 will focus on the research conducted at the Inter-university Microelectronics Center (IMEC). This work outlines the electrical characterization performed at the circuit level. The samples used in these studies consist of TSMC 28nm high-k ring oscillator arrays. In these samples, both static degradation (BTI) and dynamic degradation (BTI-HCI) will be investigated, and the results will be presented.

Next, the conclusions of this thesis will be summarized. Finally, the annexes of this thesis will be appended.

1. Introduction

In this chapter, a brief review of the evolution of micro and nano electronics technology will be presented, with particular emphasis placed on the devices that are used in this thesis. Then, the types of variability will be described including the different failure mechanisms studied in this work. Finally, the resistive switching mechanism will be explained along with its characteristics.

1.1 MOSFET device

In this section, an overview of one of the most significant electronic innovations of the 20th century is presented. Subsequent sections will explore the evolution, composition, and electrical characteristics of MOSFETs in detail.

The MOSFET is composed by a MOS structure (Figure 1.1). The top layer is typically a metal, though it can also consist of highly doped polysilicon. Beneath this lies an insulating layer, commonly silicon dioxide (SiO_2) or a *high-k* dielectric material. The substrate usually consists of silicon and can be doped to create either p-type or n-type devices, depending on the majority carriers present within the substrate.

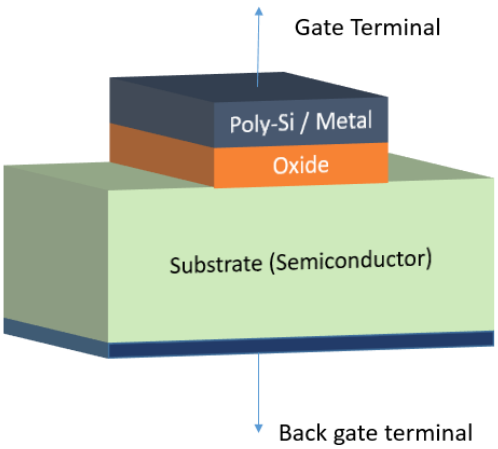


Figure 1.1: Scheme of a MOS structure

The MOS structure is completed to form a MOSFET by introducing two highly doped regions with impurities opposite to those in the substrate, thus, forming the source and drain regions. The device operates by forming a channel between source and drain contacts by inversion, electrons in the case of a p-type substrate (n-channel MOSFET) as shown in Figure 1.2, or holes in the case of an n-type substrate (p-channel MOSFET). The number of charge carriers in the channel are controlled by the gate terminal.

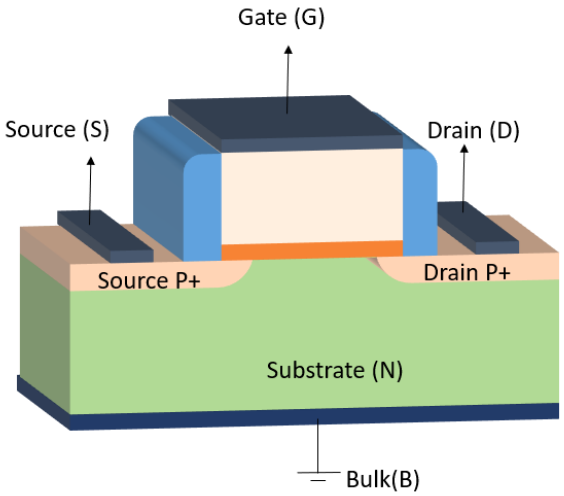


Figure 1.2: Scheme of an n-type substrate MOSFET device

1.1.1 Operation modes of a MOS capacitor

The MOS capacitance has three different modes of operation [1]. They are determined by variations in the gate voltage. These regions are defined based on whether the gate voltage increases or decreases. To explain the different MOS capacitor operation modes, we will consider a device with n-type substrate (Figure 1.2). The first mode of operation is called accumulation. This occurs when a positive voltage is applied to the gate contact (V_G>0), so that the positive voltage attracts the electrons towards the interface between oxide and semiconductor. As a result, the majority carriers, electrons in this case, lead to an accumulation of electrons close to the interface (see Figure 1.3 A).

Depletion is the second mode of operation. It occurs when a small negative voltage is applied to the gate terminal (V_G<0). This negative voltage repels the electrons leaving a depletion region in the substrate region close to the oxide. The total capacitance decreases in comparison to the accumulation region and it leaves a positive charge in the depletion region as depicted in Figure 1.3 B).

The third mode of operation is inversion. This occurs when a voltage much lower than zero (V_G<<0) is applied to the gate terminal. The highly negative charge begins to repel electrons, and eventually, minority carriers accumulate at the surface (see Figure 1.3 C). As for the capacitance, it initially decreases in weak inversion but saturates when strong inversion is reached.

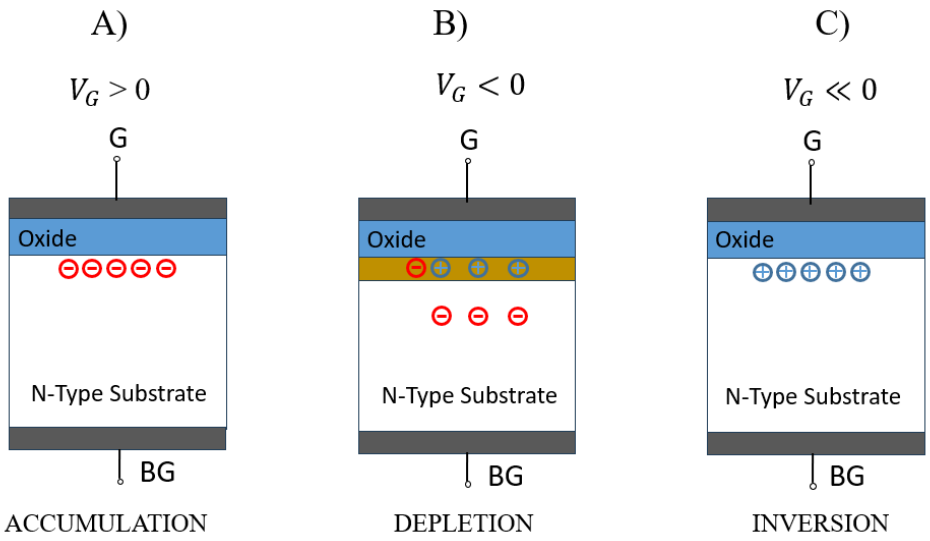


Figure 1.3: Operations modes of a MOS capacitor. A) Accumulation. B) Depletion. C) Inversion.

1.1.2 Technology roadmap

The continuous advancement of microelectronics, along with the growing demand for more compact devices, has driven a sustained reduction in size, in line with Moore's Law. The evolution of MOSFET technology has progressed from simply reducing transistor dimensions to exploring new architectures designed to mitigate the effects associated with miniaturization: The most common problems associated to scaling include short channel effects as, for example, speed saturation, and channel length modulation [2], [3] between others.

This section presents key milestones in the scaling of MOSFETs:

Planar MOSFET and CMOS

Planar MOSFETs and CMOS (Complementary MOS) became industry standards for low power applications [4]. One of its key characteristics was its length, approximately $L = \sim 10\mu m$. This period covers from the 1960s to 1980s [5].

Scaling Era

Moore's Law dominated this period that covers from the 1990s to 2000s, with the number of transistors within an integrated circuit doubling every two years. The achieved dimensions were 0.35 µm of technological node and smaller. In the 1990s the use of technological node started, with the establishment of technology roadmaps such as the National Technology Roadmap for Semiconductors (NTRS), which later evolved into the

International Technology Roadmap for Semiconductors (ITRS)[6] and subsequently the International Roadmap for Devices and Systems (IRDS)[7]. In the 2000s the name of technological node no longer corresponds to the physical channel length, and it became an industry convention.

High-k dielectrics, Strained Silicon

Scaling introduced another problem: the leakage currents through the dielectric. This event consists of electrons that cross the dielectric barrier between gate and substrate most known as *tunnel effect*. This phenomenon can form a current path that accelerates oxide degradation reducing the drain current and increasing the gate current. To mitigate these effects, high permittivity dielectrics or *high-k* dielectrics were introduced. The main characteristic of these materials is their high dielectric constant *K* [8]. The metal gate was introduced as well in this period which allow to reduce leakage currents and helped to continue scaling.

In Figure 1.4 the representation of a MOS structure with silicon oxide dielectric and its equivalent with high-k dielectric is depicted. From this figure, it can be extracted the definition of "Equivalent Oxide Thickness" (EOT) [9]. EOT is defined as the thickness of an ideal silicon dioxide layer that would yield the same capacitance per unit area as the high-k dielectric employed in the MOSFET gate stack. In other words, the dielectric material (high-k) exhibits the same electrical behavior as a much thinner silicon dioxide layer as represented in Figure 1.4.

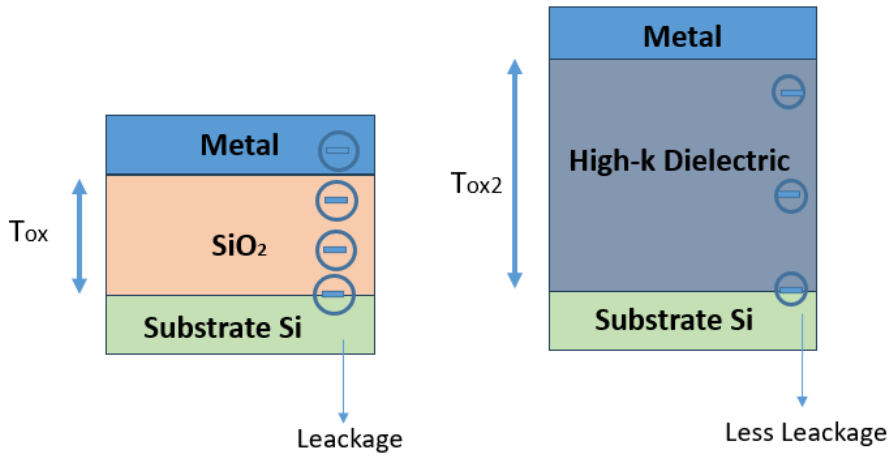


Figure 1.4: LEFT: Schematic representation of a MOS structure with SiO_2 dielectric and RIGHT: its equivalent with high-K dielectric.

FinFETs

Another key moment (that covers between 2010s to 2020s) was the introduction of 3D transistors or FinFETs. In this case, the gate wrapped all the fin-shaped channel, which improves gate control (see Figure 1.5 a). With the introduction of FinFETs at technological node of 22nm low power performance was achieved jointly by the reduction of leakage currents [10].

Gate All Around

As transistors continue to shrink in size, new ways to improve its performance are emerging. Gate-All-Around (GAA) transistors are developed as a technology where the gate fully surrounds a finger structure, which results in enhanced performance and reduced leakage.

The International Roadmap for Devices and Systems (IRDS) [11] identified Gate-All-Around FETs (GAAFETs) as a key successor to FinFETs [12] for advancing future semiconductor nodes. These devices are categorized into vertical and lateral designs. Both lateral and vertical GAAFETs utilize structures such as *nanowires* (NW) and *nanosheets* (NSH) [13] for channel configurations (Figure 1.5 b and c respectively). They demonstrate significant potential for scaling below a technological node of 10 nm due to their enhanced control over short-channel effects and improved performance such as: power consumption (no p-n leakage currents), higher drive currents (I_{ON}) faster switching speeds and low variability.

To optimize area and increase current drive lateral GAAFETs are arranged in stacked nanosheets or nanowires, where multiple sheets and wires are inserted. Lateral GAA structures offer improvements over FinFETs such as: full 360º electrostatic control, reduced short channel effects (DIBL, subthreshold leakage) [14]. In these configurations, the channel is completely wrapped by the gate material, as illustrated in Figure 1.5 b and c.

While lateral GAA transistors have already been adopted in advanced manufacturing nodes, vertical GAA architecture remains largely at the research stage and are currently less prevalent due to their higher fabrication complexity and integration challenge [15].

However, GAA transistors also require more complicated fabrication steps compared to Ω-gate FETs which will be explained in the next sections. This fabrication complexity is due to gate wrapping and nanosheet/nanowire formation. Regarding gate wrapping, the complexity is due to advanced deposition techniques that technology requires, that is to say, the process to create thin films. Concerning nanosheet/nanowire formation, they require many etching - release processes, i.e. remove – isolate layers of material during fabrication process.

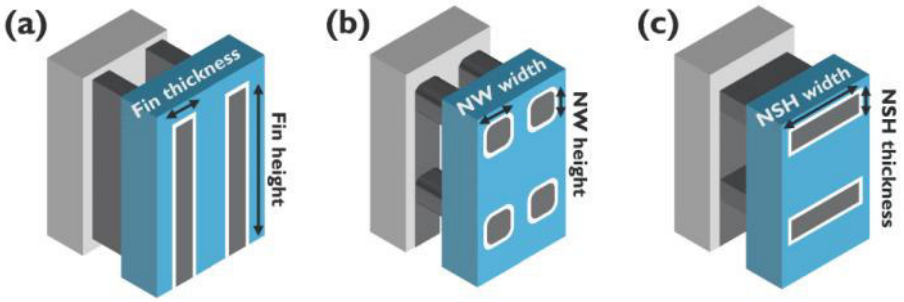


Figure 1.5: 3d schematic view of a lateral a) FinFET, b) NW-FET, c) NSH-FET [15].

On the other hand, cylindrical GAA refers to the vertical nanowire, commonly known as vertical GAA. The cylindrical shape of the channel enhances transistor performance by improving carrier distribution and minimizing corner effects (electric field concentration in sharp corners) [16].

Nanowire transistors - Omega-Gate

Ω-gate FETs are named due to the omega shape of the gate. They are considered as an improvement of the gate-all-around transistors [17]. The Ω-gate FETs are an alternative to reduce the complicated fabrication processes that GAA requires as commented in the last paragraphs. In this kind of transistor, the gate wraps around the channel. Fig 1.6 shows the differences between GAA FETs and Ω-gate FETs.

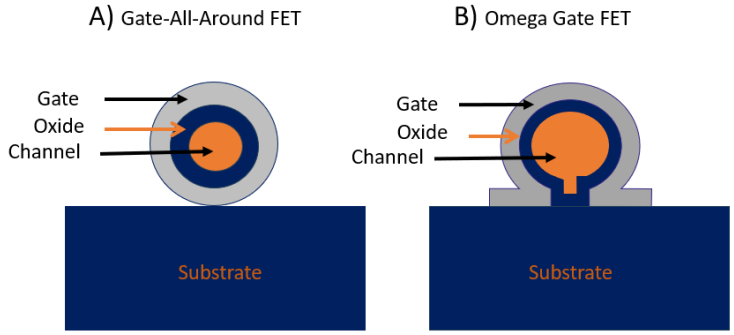


Figure 1.6: Cross section of a gate all around transistor (A) and Ω-gate FET (B).

The Ω-gate FET geometry where the gate wraps three sides of the channel provides better control minimizing short channel effects and reducing leakage currents [18]. Compared to planar transistors and FinFETs, Ω-gate FETs offer enhanced performance and efficiency, particularly in lower 10nm applications like processors and memory devices. They improve scalability and reduce power consumption [19].

1.1.3 Planar FD-SOI transistors

Silicon on Insulator (SOI)

The use of silicon on insulator transistors was an improvement in terms of scaling and channel control. SOI technology has re-emerged as one of the most promising alternatives for continued scaling in semiconductors below 10nm [20]. This technology uses an insulator layer as can be seen in Figure 1.7, called buried oxide or BOX. This layer separates the active silicon region, reducing parasitic capacitances, enhancing energy efficiency and speed compared to traditional bulk silicon semiconductors [20]. In particular, the SOI technology devices eliminate latch-up. Latch-up is an effect that appears between p-n junctions that cause high current flow between them.

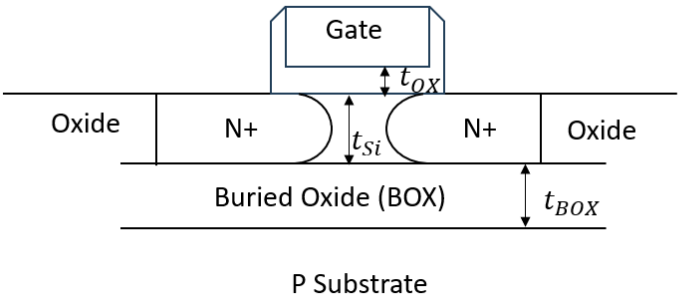


Figure 1.7: Schematic representation of a SOI planar - transistor

SOI technology is classified in two types based on its fabrication:

Partially depleted silicon on insulator (PD-SOI). - A partially depleted device is the technology where the silicon layer, t_{Si} in Figure 1.7, allows the charge accumulation within the channel. This flexibility simplifies the manufacturing process. Contrarily to FD-SOI, body effects are found in this technology.

The body effect refers to the fact that the body region (located between the buried oxide and the dielectric) is electrically floating and capable of accumulating charge. This charge rise can result in an increase in the threshold voltage, with the direction of the shift depending on whether the device is an NMOS or PMOS transistor, respectively. This body effect depends mostly on the biasing conditions of the source, drain, and gate terminals, but not on the substrate, as it is electrically isolated by the buried oxide (BOX) layer.

Fully depleted silicon on insulator (FD-SOI). – In this technology the silicon layer, t_{Si} in the Figure 1.7, is depleted i.e. no charge accumulation occurs within the channel. In a fully depleted device, the influence of the substrate voltage (body) on the threshold voltage V_{TH} (body effect) is eliminated.

1.2 Variability in MOSFETs devices

The variability in transistors refers to the fluctuation in their electrical characteristics. There are two types of variations: Time Zero Variability (TZV) and Time Dependent Variability (TDV), and they will be described in the next paragraphs.

The combined effects of TZV and TDV can critically impact on the functionality of devices and circuits, diminish device and circuit reliability and potentially shortening their operational lifetime. So, their statistical characterization and modeling are necessary.

1.2.1 Time zero variability

The variability phenomenon has always been present in semiconductor fabrication. Time Zero Variability (TZV) refers to those device fluctuations due to the manufacturing imperfections in transistor fabrication that cause variability in transistor parameters as technology scales down. TZV is also known as process variation. This could be stochastic or systematic. The stochastic time zero variability refers to the variability that occurs between devices of the same die. The systematic variation is the variation of the devices parameters between die to die, wafer to wafer, or lot to lot [21].

1.2.2 Time dependent variability

As its name suggests, time-dependent variability (TDV) refers to the variations that devices parameters experience after a period of use under operation conditions. TDV is also known as '*Aging'*. Most important aging mechanisms are Bias Temperature Instabilities (BTI), Hot Carrier Injection (HCI), OFF-State Stress (OSS) and dielectric breakdown. In the next sections, these mechanisms will be developed in depth. It is therefore necessary to characterize aging mechanisms to determine the durability of devices.

1.2.2.1 Bias Temperature Instabilities (BTI)

The Bias Temperature Instabilities, known as BTI, is an aging mechanism that is produced when a device is subjected to elevate temperatures and voltages during a limited time. In p-MOSFETs, it is known as *NBTI.* To characterize NBTI, the gate terminal of the transistor is biased with negative voltage. The electric field that the dielectric endures goes from bulk to gate (red arrows in figure 1.8 LEFT). The transistor's other terminals are grounded. Holes (positive charges) are attracted to the gate insulator interface, which causes continuous degradation in transistors' parameters as: threshold voltage (V_{th}), transconductance (gm), linear current I_{DLIN} and saturation current I_{DSAT} between others [22], [23].

NBTI was observed for the first time in SiO_2 and $SiON$ insulators [24]. Later after the introduction of high-K dielectrics is still an important aging mechanism and reliability

concern. The discovery of this aging mechanism led to the development of models that predict this behavior.

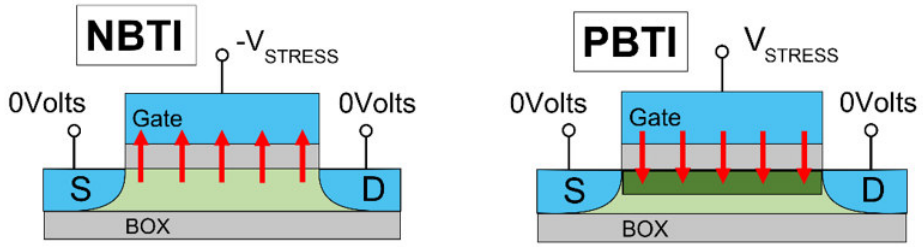


Figure 1.8: Representation of a transistor subjected to NBTI (LEFT) and PBTI (RIGHT). In both cases, the direction of the electric field through the dielectric is represented with red arrows.

In the case of n-MOSFETs, BTI is called *PBTI,* and it is caused when the gate terminal is biased with positive voltages and electrons (negative charges) are attracted to the gate dielectric interface. The electric field is directed towards the bulk (red arrows in figure 1.8 RIGHT). Both NBTI and PBTI illustrate the effects of TDV.

The consequences of P/NBTI are the degradation of transistor's parameters like ΔV_{th}, mobility $\Delta\mu$, drain current I_{DS} and carrier propagation delay τ_{PD}, between others. These changes are not permanent; rather, they have the potential to be reversed after the transistor bias is stopped (relaxation window), allowing it to recover some of its original performance characteristic [20]. According to the reference, even after a long period of relaxation window it is not enough to reach a total recovery i.e. a $\Delta V_{th} = 0$. In [25], a permanent component of relaxation is recognizable after a measurement of 7 decades of relaxation but it is not universal behavior and it will depend on the sample. Defects in materials that cause BTI such as oxygen vacancies and bond breaks in silicon can be activated due to temperature, and voltage. In Figure 1.9 (LEFT) a measurement obtained in [26] shows a voltage dependency of BTI, which means that when stress voltages (from 1.0V to 2.0V) increase, the degradation also increases. In Figure 1.9 (RIGHT) different temperatures tested in a device stressed at the same voltage V = -2V are presented. As observed, for a stress time of 10s, low temperature (50ºC in Figure 1.9 RIGHT) reach a maximum of 60mV of degradation of the observed parameter, while 200ºC (red lines in Figure 1.9) reach ~140mV of degradation. This tendency shows that at higher temperatures higher is the degradation in BTI.

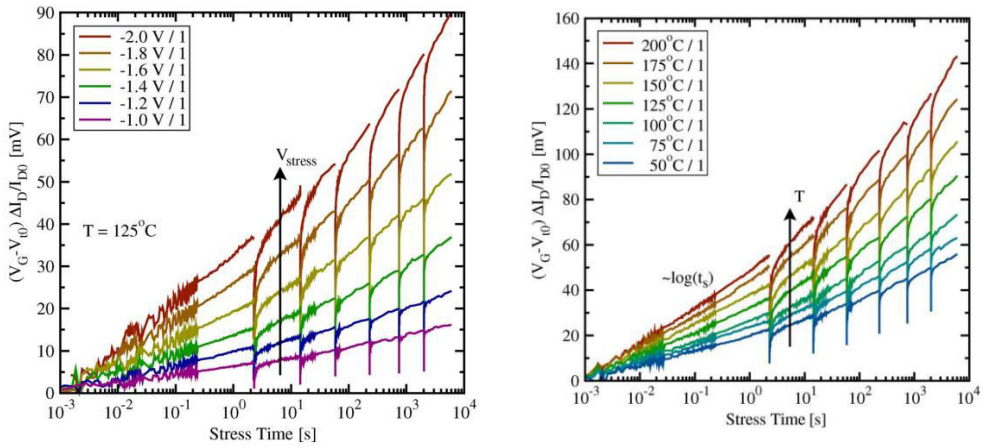


Figure 1.9. BTI degradation LEFT: for different stress voltages at T= 125ºC where degradation depends on stress voltage. RIGHT: for 7 different temperatures at a stress voltage of V= -2V [26].

About the frequency dependency of BTI, many publications show the importance of BTI when the device is subjected to dynamic voltage (AC-BTI) [27], [28], [29]. This aging mechanism is known as the dominant degradation mechanism in computation CMOS logic [30]. Understanding the characteristics of AC-BTI is important, notably its dependence on the duty factor. Specifically, it has been observed that higher duty factors lead to an increased degradation of BTI [30]. Moreover, some publications have shown a strong frequency dependence. For example in [31], the frequency dependence is analyzed using the recently proposed capture/emission time map model. This model explains Bias Temperature Instability (BTI) as a collection of numerous independent reactions reaching good accuracy with experimental data.

1.2.2.2 Hot Carrier Injection (HCI)

Hot Carrier Injection (HCI) is another aging phenomenon that was discovered nearly 50 years ago. From the seventies until the 21st century, research focused on understanding the physics of this principal failure mechanism [32]. This effort converged in the development of models that could predict the behavior [33].

HCI takes place when carriers move in the transistor's channel from source to drain. This mechanism is accelerated by the lateral electric field generated by voltage applied to drain and gate terminals. Some carriers acquire enough energy to penetrate the gate dielectric (impact ionization). These carriers will generate defects that affect the characteristics of the transistor. Figure 1.10 shows the schematics of a transistor under HCI degradation. The blue arrow shows the direction of the lateral electric field and later degradation near the drain side (nonuniform stress).

For long-channel devices ($L > 0.15\mu m$), $V_G = V_D/2$ is the most harmful condition at room temperature. But for short-channel transistors the higher degradation that happens at room temperature is when $V_G = V_D$ [34], [35]. Long and short channel transistors are usually stressed under the most harmful conditions. On the one hand, in long-channel devices stressed at $V_G = V_D/2$ the degradation is less serious due to decreased number and energy of carriers. On the other hand, degradation in short-channel transistors stressed at $V_G = V_D$ increases [36], which means that for short channel devices HCI is substantially harmful.

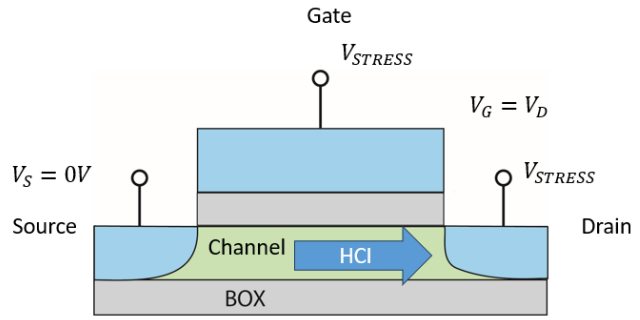


Figure 1.10: Schematics of the effect of HCI in the transistor's channel

As BTI phenomenon, HCI aging is also voltage dependent. It can generate a shift in transistor's threshold voltage V_{TH}, and a reduction of the saturation current [37]. In Figure 1.11, voltage dependency is tested. Several biases tested demonstrate that at higher voltage, threshold voltage degradation ΔV_{TH} increases [38].

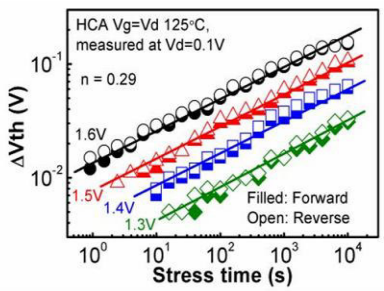


Figure 1.11: Threshold voltage V_{TH} degradation vs stress time after HCI aging. Different biases tested and measured at $V_D = 0.1V$ under 125°C of temperature[38].

HCI is a phenomenon influenced by temperature; higher temperatures result in more severe degradation than lower temperatures under DC stress conditions. HCI depends on frequency, just as BTI aging mechanism, under dynamic conditions (AC-HCI), the degradation at the same temperature is less severe than for samples subjected to DC conditions. As shown in Figure 1.12, some studies show that HCI degradation depends on pulse width. If the signal has a longer pulse width (pulse region where the maximum degradation condition is satisfied $V_G = V_D/2$), more degradation due to the time of exposure that devices endure under HCI. [39].

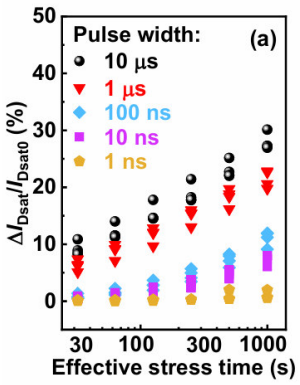


Figure 1.12: AC HCI degradation with different pulse widths at temperature of 85° C [39].

1.2.2.3 Off-state stress degradation (OSS)

Another aging mechanism that has attracted attention recently is the Off-State Stress (OSS) degradation. While HCI and BTI were extensively studied in an 'on-state' of the transistor [40],[41], 'off-state' has not been deeply studied in the last decades [42]. Certainly, this mechanism was not a big reliability concern in SiO_2 $poly$ devices, but the use of high-k dielectrics increased the risk of OSS due to hole trapping inside high-k defects [42].

OSS happens when the transistor is in 'off' mode ($V_G = 0V$) (see Figure 1.13), In this state, the source terminal is grounded ($V_S = 0V$), and also the back gate ($V_{BG} = 0V$), while the drain terminal is biased ($V_D = V_{STRESS}$). This bias creates a lateral electric field that can, over the long term, affect the dielectric material. The damage produced by OSS is located in the oxide close to drain terminal (Figure 1.13). Some researchers have shown that during OSS, the subthreshold slope (SS) increases significantly. It is well known that as the gate dielectric thickness (T_{OX}) continues to thin, controlling the off-state current becomes more complicated [43].

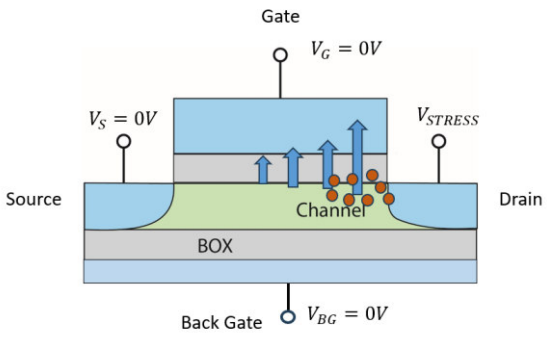


Figure 1.13: Schematics of a transistor under Off-state degradation.

Normally, the devices during their operation are subjected to different failure mechanisms. Transistors frequently switch between on and off states. When in off state, the drain $V_D > 0$ V faces high voltage while the gate remains at zero voltage, which can lead to potential degradation [44]. In the opposite order, in the on state (where $|V_G| > 0$ V and $V_D = 0$ V), BTI becomes a significant factor. During the switching process, when both $|V_G|$ and $|V_D|$ are active, HCI can occur.

In applications such as CMOS inverters or SRAM cells, degradation during the off state plays a substantial role in devices wear-out and needs careful assessment to maintain circuit reliability. In Figure 1.14, the actuation of three aging mechanisms in an inverter is represented. When a low voltage is applied to the input (0V in case A), a negative drop between gate-source and gate-drain is produced. In consequence, pMOSFET suffers NBTI. The nMOSFET is not conducing but an electric field is produced (1V in output), so the nMOSFET suffers OSS. When the input is switched to '1' (case B), the output voltage shifts from '1' to '0' and in this transition both transistors are subjected to HCI aging with $V_D = V_G$. Finally, when a high voltage is applied at the input, the nMOSFET experiences PBTI, while the pMOSFET undergoes OSS. This situation (case C) is the opposite of what occurs in case A.

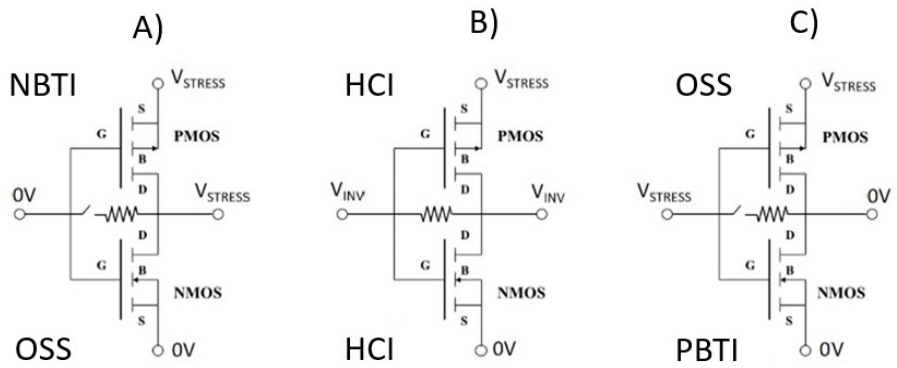


Figure 1.14: In an inverter, the bias switch between the drain and gate makes the device suffer OSS and BTI, alternatively HCI is suffered.

1.2.2.4 Dielectric breakdown

Dielectric breakdown is a consequence of the device dielectric degradation. Degradation leads to a loss of the fundamental characteristics that define these materials. Breakdown signifies either a complete or partial loss of the isolated properties of the device dielectric [45], [46],[47].

Dielectric degradation can be observed when electric stress is applied to the dielectric. In thin insulators, due to the voltage applied, a tunnel conduction is produced through the dielectric. Progressively this conduction will create defects inside the oxide and the interfaces of the oxide with the electrodes. Electrons may either pass directly through the dielectric (Figure 1.15 LEFT) or be assisted by traps present within the oxide (Figure 1.15 RIGHT). There is a moment when the critical density of defects [48] is reached. In this moment dielectric breakdown happens, according to percolative model [49].

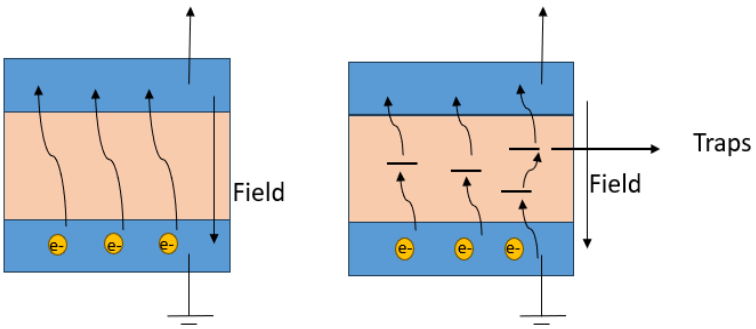


Figure 1.15: LEFT: Schematic representation of the tunnel effect. RIGHT: trapped assisted tunnel effect.

There are different types of dielectric breakdown*: Hard Breakdown* (HBD) occurs when there is an abrupt change in current, resulting in catastrophic damage to the device. *Soft Breakdown* (SBD) involves a rapid increase in current that causes moderate damage to the dielectric, that although not immediately devastating, it can lead to significant issues over time. *Progressive Breakdown* (PBD) manifests as incremental damage, which can silently affect the device's functionality [50].

In Figure 1.16 a), the evolution of the leakage current through the dielectric as degradation increases is illustrated. It begins with the initial stress induced leakage current (SILC). Next, the first soft breakdown (SBD) occurs, followed by a noticeable increase between the first and second SBDs, which can be identified as progressive dielectric breakdown (PDB). Finally, the abrupt change in current at the end is classified as hard breakdown (HBD). This types of breakdown are not a general behavior and depend on the dielectric thickness of the device. In figure 1.16 b) the typical I-V characteristic of the fresh device (black) and after stressed with SBD (red) and HBD (blue).

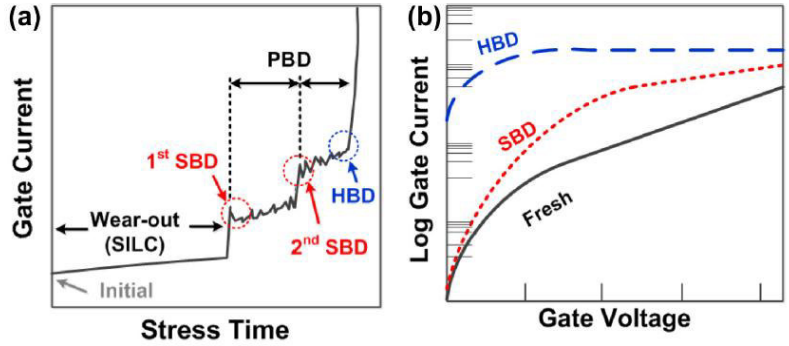


Figure 1.16: Representation of the gate current increment versus time as the dielectric degradation increases: representation of hard breakdown (HBD), soft breakdown (SBD) and progressive breakdown (PBD) (a) and typical I-V curves of a fresh sample and after a after stress (b) [47].

1.3 Reversible dielectric breakdown

As previously mentioned, dielectric breakdown leads to a gradual loss of the device dielectric isolating properties, which can result in permanent damage. However, with the proper current limitation and devices with determinate materials, it is possible for a device to regain some of its dielectric properties after experiencing a drop in resistance when exposed to controlled electrical conditions again. This phenomenon is referred to as reversible dielectric breakdown and it is directly linked to the resistive switching phenomenon, that will be explained in the following sections. In Figure 1.17, the schematic representation of hard breakdown (HBD), also known as irreversible breakdown, and a reversible breakdown, is illustrated. When a fresh device is subjected to electric stress without current limitations, it experiences an irreversible breakdown. In contrast, if the current is limited, the electrical conductance of the device can be restored by applying determinate voltages. This process can be cycled multiple times, depending on the level of current limits.

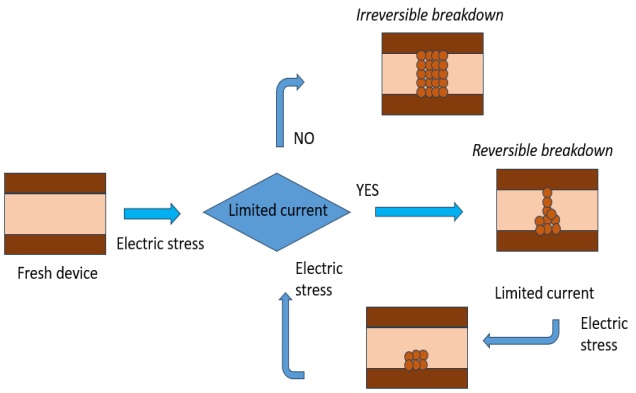


Figure 1.17 Schematic representation of irreversible and reversible breakdown.

1.3.1 Resistive switching phenomenon (RS)

Resistive switching (RS) is a phenomenon in which a device experiences a non-volatil change in its electrical resistance when a determined voltage is applied. Resistive switching phenomenon was discovered in the 1960s [51]. This study was performed in a Metal-Insulator-Metal MIM structure of $Al_2\ O_3$. But the phenomenon started to be deeply studied many years later. After, it was demonstrated that RS could define clearly stable resistive states. Memories based on RS are considered as possible substitutes to *flash* memories [52].

Devices that exhibit resistive switching (RS) behavior are commonly referred to as *memristive devices*. Among them, the most prominent and widely utilized is the *memristor*, a component theoretically introduced by Leon Chua in 1971 as the fourth fundamental two-terminal circuit element, alongside the resistor, capacitor, and inductor [53], [54].

Some works about RS in very scaled devices such as Gate All Around (GAA) transistors are found in literature. In [55], [56] RS is observed in vertical GAA nanopillars integrated with RRAM cells, showing good non-volatile memory properties.

In the next sections, the RS characteristics and the different physical mechanisms responsible for RS, will be explained.

1.3.2 Characteristics of resistive switching

In a device with RS, two different resistance states can be distinguished: low resistance state (LRS) and high resistance state (HRS) (Figure 1.18).

Low Resistance State (LRS) or On-state: It is a high conductivity state.
High Resistance State (HRS) or Off-state: It is a low conductivity state.
When characterizing a resistive switching (RS) device, three distinct mechanisms emerge:

Forming: This is the initial voltage applied to the device or material. This process typically leaves the device in a low-resistance state (LRS) (see Figure 1.18). In some thin oxide materials, performing this step may not be necessary to observe RS.
Set: This mechanism refers to the transition from a high-resistance state (HRS) to a low-resistance state (LRS) (Figure 1.18).
Reset*:* This process involves changing from the LRS back to the HRS (Figure 1.18).

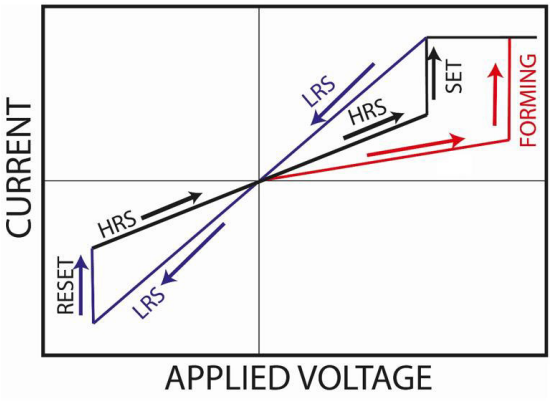


Figure 1.18 Representation of an I-V characteristic of a device with RS in which can be recognized forming, set and reset processes.

Usually, during both *forming* and *set* process, a current limit or compliance is applied to prevent hard breakdown (HBD). In contrast, during the *reset* phase, it is not necessary to limit the current, as the energy used is sufficient to change the conductive state [57].

There are three RS modes that depend on the polarity of the *set* and *reset* and the stability of the states:

Bipolar RS: In bipolar RS, *reset* and *set* processes happen at different polarities. To observe this kind of RS, the applied polarities could be both when $V_{set} > 0$ and $V_{reset} < 0$ or $V_{reset} > 0$ and $V_{set} < 0$. Starting at HRS, a set process can be triggered by $V_{set} > V_{th1}$ which results in LRS as described in Figure 1.19 a.

Unipolar RS: *Reset* and *set* processes happen in the same polarity. It can be distinguished between unipolar positive (V_{set} *and* $V_{reset} > 0$) and unipolar negative (V_{set} *and* $V_{reset} <0$) as represented in figure 1.19 b. Starting at HRS, the set process is triggered at $V_{set} > V_{th1}$. The current compliance is often limiting LRS which is released in RESET process with $V_{reset} > V_{th2}$.

RS threshold: Even though it is fundamentally associated with the resistive switching phenomenon, it cannot be strictly categorized as a standard RS mode due to its distinct behavior regarding voltage polarity and the transient nature of its states. Unlike RS, when the voltage is reverted to zero, the resultant resistance state exhibits a volatile nature, leading to inverse switching at a different threshold voltage, V_{th1} (see Figure 1.19 c). [58].

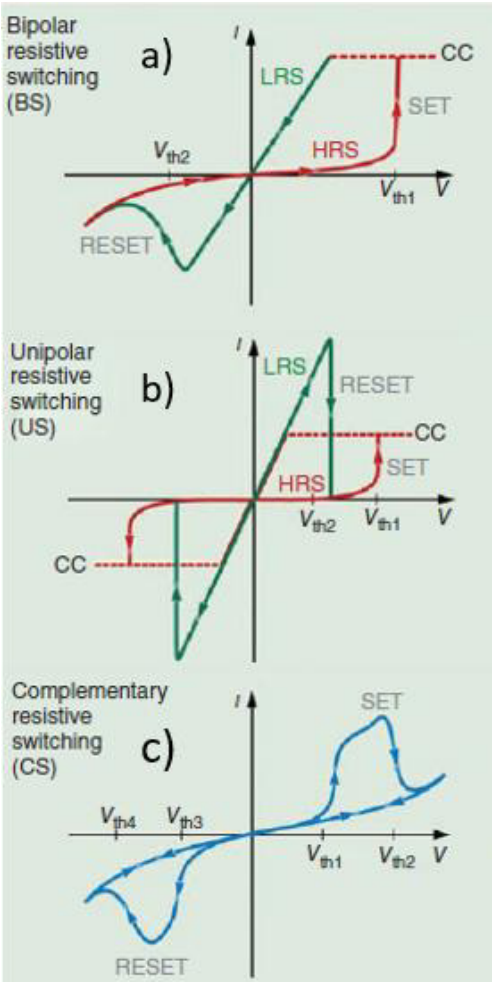


Figure 1.19. Schematic representation of the I-V curve of a device in a) bipolar resistive switching mode. b) unipolar resistive switching. c) complementary resistive switching [51].

1.3.3 Resistive Switching commutation mechanisms

In resistive switching devices, a significant array of processes (Figure 1.20) contributes to the phenomenon of RS. Figure 1.20 illustrates the classification of the different processes that generate the RS phenomenon. They are electrochemical mechanisms (ECM), valence change mechanism (VCM), thermochemical mechanism (TCM), phase changes memories, electrostatics, ferroelectrics, nanomechanics, magneto-resistive and molecular. Among these, we will focus on redox-based mechanisms, which we will see in this thesis.

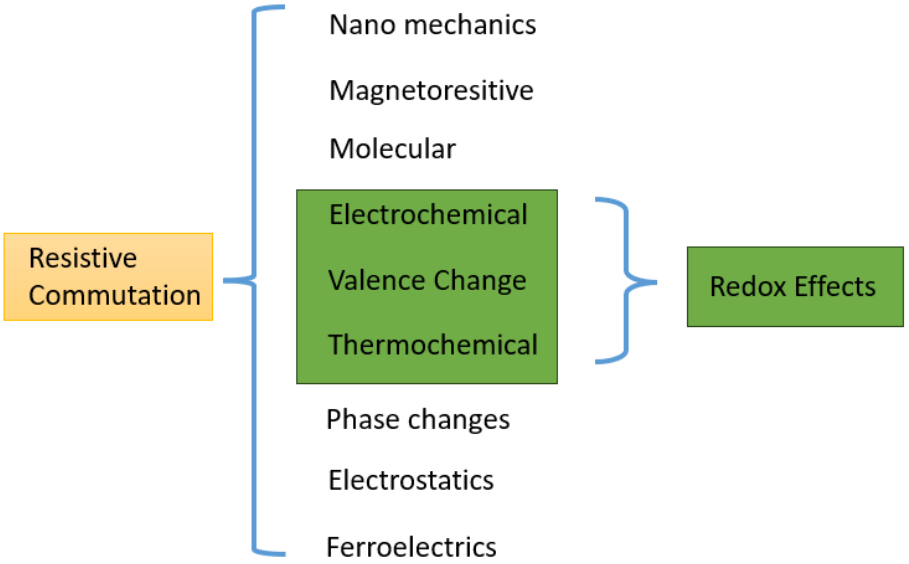


Figure 1.20 Classification of RS commutation physical mechanisms [59].

The generation and destruction of a conductive filament (CF) within the dielectric are key characteristics of reduction-oxidation (RedOx) mechanisms. RedOx mechanisms are chemical processes that involve the transfer of electrons. Oxygen vacancies or metallic cations can migrate within the dielectric, facilitating the formation and destruction of a conductive filament. This process is influenced by the presence and movement of ions within the dielectric material.

The Mechanisms associated with RedOx processes are:

***Electrochemical Mechanism*:** This process is controlled by an electric field and is directly based on the diffusion of a metallic electrode through the oxide, resulting in the formation of a metallic conductive filament (CF).

***Valence Change Mechanism*:** As the name suggests, this mechanism involves the generation of oxygen vacancies within the oxide, which create conductive regions inside the dielectric material.

Thermochemical Mechanism: This process is governed by thermal effects. The resistive switching (RS) phenomenon occurs due to the melting of the conductive filament (CF). Thermal effects also influence the diffusion of atoms and ions.

2. Impact of OFF-State, HCI, and BTI degradation in FD-SOI Ω-Gate NW-FETs

The results of this chapter are reproduced and/or adapted from:

- *C. Valdivieso, A. Crespo-Yepes, R. Miranda, D. Bernal, J. Martin-Martinez, R. Rodriguez, M. Nafria, "Comparison of OFF-State, HCI and BTI degradation in FDSOI Ω-gate NW-FETs", Solid-State Electronics, Volume 194, 2022.*

- *C. Valdivieso, A. Crespo-Yepes, R. Miranda, D. Bernal, J. Martin-Martinez, R. Rodriguez, M. Nafria, "Impact of OFF-State, HCI and BTI degradation in FDSOI Ω-gate NW-FETs", Solid-State Electronics, Volume 203, 2023.*

This chapter is structured into three sections. The first section provides a detailed description of the samples selected from the 'Snow' wafer map and the characterization methods employed. In the second section, experimental results will be presented for HCI, BTI, and OSS. Finally, the conclusions of this chapter will be summarized.

As it was presented in Chapter 1, device degradation caused by BTI or HCI is still relevant in deeply scaled CMOS technologies [60], [61], [62], [63], [64], [65]. The measurement of device degradation by subjecting them to elevated temperatures and voltages accelerates the deterioration of circuits that would otherwise last for years. In recent years, there has been a growing interest on understanding the degradation effects caused by OFF-state stress (OSS), a phenomenon that can arise during the operation of electronic devices within circuits [66], [67], [68], [69], [70], [71]. As highlighted in section 1.2.2.3, OSS plays a critical role in determining the reliability and longevity of these devices. In this chapter, the effects of negative/positive BTI and HCI degradations are also experimentally studied and compared to that of the OFF-state stress in FD-SOI Ω-gate FETs. The dependence on the stress voltage of the ON and OFF drain current shifts induced by OFF-State stresses is also analyzed. Moreover, the variations of the drain, source, back gate and gate currents during and after the stress are compared, to evaluate in more detail the effects on the device electrical properties of each of the aging mechanisms.

2.1 Samples description

The FD-SOI Ω-gate nanowire field-effect transistors (FETs) used in this chapter are illustrated in Figure 2.1. They are a type of Gate-All-Around (GAA) transistor that features an omega-shaped gate that encircles the channel. These devices were fabricated by CEA LETI [72] and utilize a high-k dielectric stack. In Figure 2.1 left, the nanowire (from top) Scanning Electron Microscopy (SEM) image is shown. While, in Figure 2.1 right, the transistor cross-sectional Transmission Electron Microscopy (TEM) image is presented.

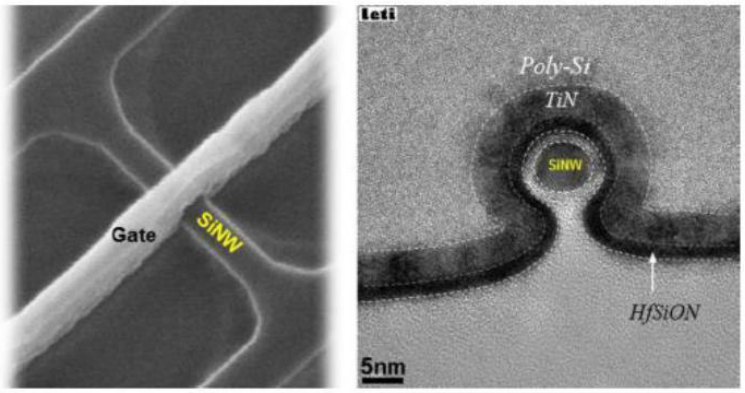


Figure 2.1 (Left) scanning electron microscopy (SEM) and (right) cross-sectional transmission electron microscopy (TEM) images of SOI omega-gate nanowire [72].

2.1.1 The 'SNOW' wafer map

Most of the devices used in this thesis are integrated into a silicon wafer called 'SNOW'. It is organized into a grid of 17 rows and 23 columns, as illustrated in Figure 2.2. This wafer is carefully divided into individual dies. Within each die, lies a specialized block that incorporates advanced FD-SOI (Fully Depleted Silicon-On-Insulator) nanowire technology.

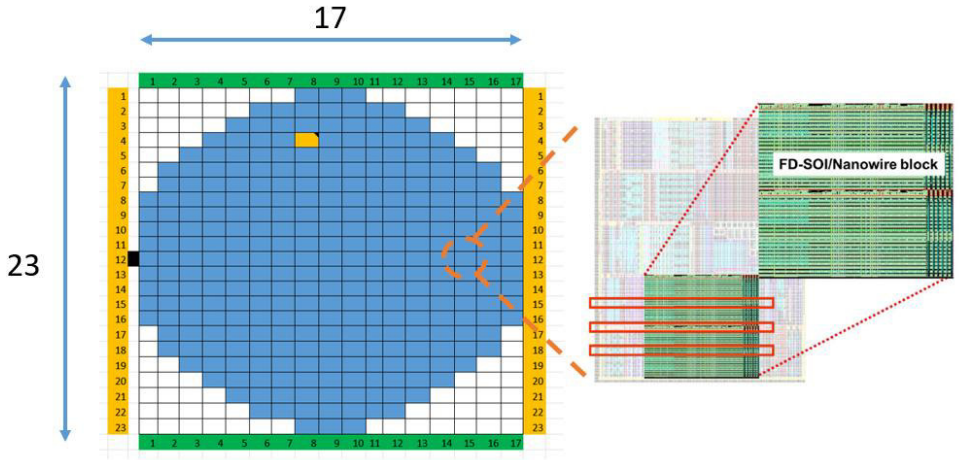


Figure 2.2 'Snow' wafer representation subdivided into individual dies that contains the FD-SOI nanowires transistors.

The structure consists of 22 pads, each of them with an area of $70\ x\ 70\ \mu m^2$. All 22 pads cover a length of $2820\ \mu m$ (see Figure 2.3) and contain 7 devices. The typical arrangement of these pads follows a specific order: beginning with the source terminal (S), followed by the drain terminal (D), then the gate terminal (G), and finally the back gate terminal of the transistors (BG), which is common for seven devices (see Figure 2.3). The devices distribution is shown in Table 2.1.

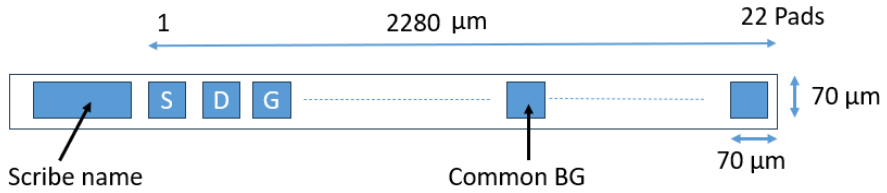


Figure 2.3 Pad distribution of 7 devices in 22 pads with common back gate contact for all 7 devices.

Pad	***Connection***	***Pad***	***Connection***
1	Source of device 1	12	Drain of device 4
2	Drain of device 1	13	Gate of device 4
3	Gate of device 1	14	Source of device 5
4	Source of device 2	15	Drain of device 5
5	Drain of device 2	16	Gate of device 5
6	Gate of device 2	17	Source of device 6
7	Source of device 3	18	Drain of device 6
8	Drain of device 3	19	Gate of device 6
9	Gate of device 3	20	Source of device 7
10	Common substrate contact	21	Drain of device 7
11	Source of device 4	22	Gate of device 7

Table 2.1 Pad distribution of the devices.

2.1.2 Samples structure

In the previous subsection, the 'SNOW' wafer map exhibited a well-organized arrangement of devices in rows. In Table 2.2 the total number of devices used in this chapter is shown, organized by name of scribe, length and width.

Scribe Name	**W(μm)**	**L(μm)**	**Orientation**	**Type (n/p)**	**# of Samp. used**
N14	0.03	0.01	0	N	2

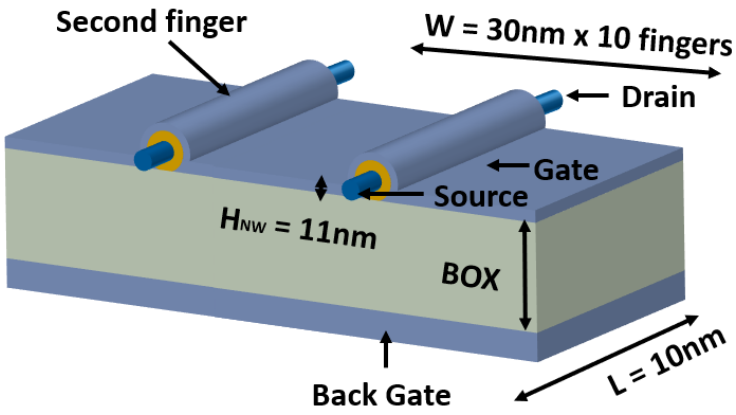
N14	0.03	0.02	0	N	42
N14	0.03	0.03	0	N	3
N14	0.03	0.1	0	N	2

Table 2.2 List of the samples tested in this chapter.

To ensure proper organization of the measurements, each device was marked after the experimentation process. Most of the results used in this chapter are based on one type of device which, after extensive experimentation, was identified as the most suitable for performing the tests conducted. This transistor is designated as its corresponding scribe name, which is **N14**, and it will be described in the next paragraph.

Device N14: The structure of the FD-SOI nanowire transistor [72] is represented in Figure 2.4 up. It has a dielectric, which is a combination of $HfSiON/TiN$ with equivalent oxide thickness of EOT = 1.3nm. The device's dimensions are $W = 300nm\ x\ L = 10{,}20{,}30{,}100\ nm$. The nanowire height is $H_{NW} = 11nm$. The device contains a buried oxide layer (BOX) with a thickness of $145nm$. The gate terminal is comprised entirely of a poly-silicon layer.
It is a multi-finger design, characterized by multiple fingers that extend from a common junction point as represented in Figure 2.4 down. This device is used to test aging mechanisms such as BTI, HCI, and OSS due to its short channel characteristics. The most N14 devices used in this chapter have the follow dimensions:

1) $W = 30nm\ x\ 10\ fingers, L = 10nm$,
2) $W = 30nm\ x\ 10\ fingers, L = 20nm$,
3) $W = 30nm\ x\ 10\ fingers,\ L = 30nm$.



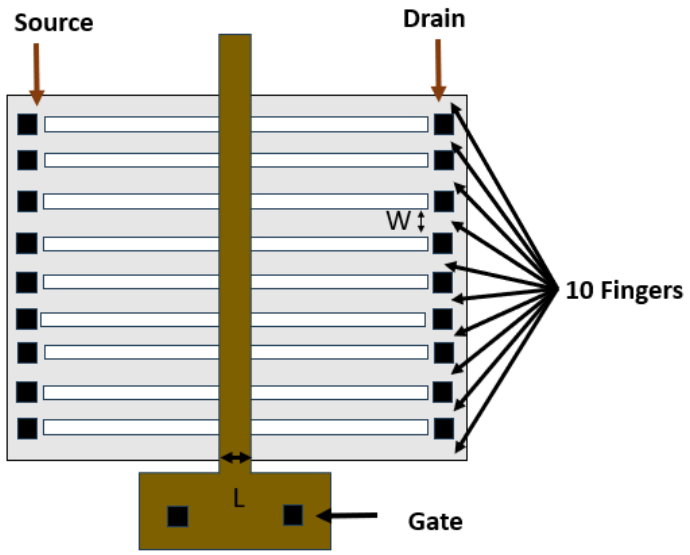


Figure 2.4 Up: Example of two finger representation of a multifinger structure of a Ω-Gate FD-SOI nanowire transistor (N14 device) Down: top view of a multi-finger (10 fingers) structure W= 30nm x 10 fingers.

The FD-SOI Ω-Gate nanowire can be represented as a planar transistor, as illustrated in Figure 2.5, the channel, where electrons flow from the source to the drain, is enclosed by the gate and dielectric.

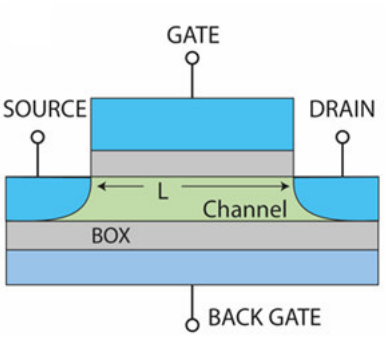


Figure 2.5 Planar representation of the FD-SOI Ω-Gate transistor N14.

The most used sample in the experiments completed in this chapter are the device with the following dimensions $W = 30nm\ x\ 10\ fingers$ and $L = 20nm$. The multi-finger structure is a characteristic of the GAA nanowires that allows an increase in current drive and optimize area [73]. In Table 2.2 the 'Snow' wafer map shows many more devices, but the choice of this sample was with this channel length the results obtained were better. As a result, the observation of the aging phenomenon characteristics was clearer.

2.2 Characterization setup

The basic equipment used is composed by a wafer probe station (WPS) and a semiconductor parameter analyzer (SPA) that will be explained in the next paragraphs.

Wafer probe station

The experimental process began with the placement of the wafer under study in the chuck of the wafer probe station (WPS). Once positioned, the device under test (DUT) is selected using a microscope. Each of the WPS's positioners has a needle that connects the source monitor units (SMUs) of the SPA, to the four terminals of the transistor: source, drain, bulk, and back gate. The WPS used in the experiments of this thesis is enclosed in a Faraday cage that avoids the effect of external electric fields.

Semiconductor parameter analyzer

The WPS is connected to a Semiconductor Parameter Analyzer (SPA) that applies voltage/current and measures current/voltage responses of the device. In this chapter the SPA utilized is the Keithley 4200A-SCS that contains 4 source monitor units (SMUs) capable of applying voltage and measure current and vice versa. The SPA is equipped with the Keithley interactive test environment (KITE) software.

Characterization setup for aging experiments

In this setup, the SMUs of the SPA are connected to the wafer probe station (WPS), which links the positioners to contact the device under test (DUT). The SPA is controlled through commercial software included in the equipment. Figure 2.6 illustrates the block diagram of the first measurement setup used for aging tests.

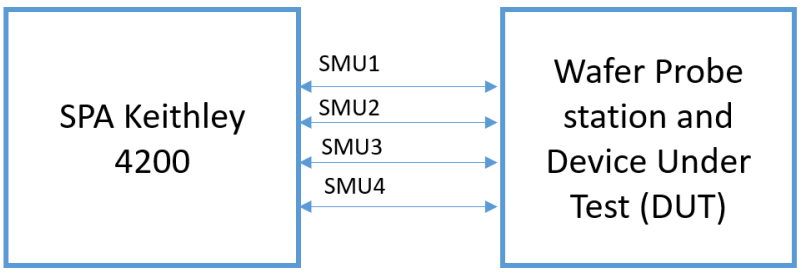


Figure 2.6 Block diagram of the first measurement setup used for the aging experiments. SPA connected in transmission and reception with WPS.

2.2.1 Characterization of transistor parameters

The measurement-stress-measurement (MSM) methodology is the most used for assessing the degradation caused by aging mechanisms in transistor parameters. This technique involves first measuring the characteristics of a device before applying stress, secondly, apply the stress, and finally measure again the device characteristics after the stress has been removed.

To enhance the effects observed during the aging process, during the stress V_G or V_D values are larger than the nominal voltage operation of the technology. This is called accelerated stress conditions. An additional parameter that can be adjusted is the duration of stress, which can be increased exponentially, for instance 1s, 10s, 100s, 1000s based on the requirements of the research. During both the pre-stress and post-stress periods, the characteristics of the transistor are compared to assess the device's degradation.

Following the MSM method, characterization procedure for the aging measurements presented in this chapter involved the following steps:

1) Characterizing the parameters of the transistor in a 'fresh' sample.

2) Performing a stress test to analyze HCI, BTI, or OSS, applying stress voltages of different durations.

3) After each stress test, the transistor's characteristics were assessed to measure the degradation associated with the aging mechanism.

2.3 Measurement procedure

In Figure 2.7 an example of the methodology followed in this thesis is shown. First, a measurement of the transistor characteristics $I_G - V_G$, $I_D - V_G$, $I_D - V_D$ when the transistor is ‘fresh’ that is before stress application. Second, stress voltages are applied to the device. Finally, a post stress characterization of the device characteristics $I_G - V_G, I_D - V_G$, $I_D - V_D$ that measures the effects of degradation. The second and third steps can be repeated successively to analyze the effect of the application of several stress intervals.

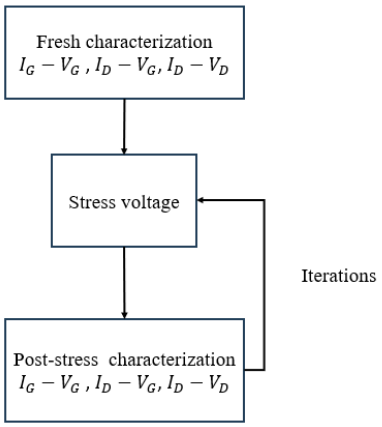


Figure 2.7 Example of the methodology sequence used in most of the experiments performed in this thesis.

Nevertheless, the MSM technique suffers from drawbacks, including the loss of precise data. This loss is particularly evident when stress is released, and some failure mechanisms show recovery during this period.

In the next paragraphs, the different stress voltage configurations will be shown. They will be presented according to the aging mechanism being tested.

Negative/Positive Bias temperature instabilities:

In the characterization of Bias Temperature Instability (BTI), we systematically analyzed both negative and positive biasing conditions. To study PBTI, a stress voltage of 2.4 volts (negative for the case of NBTI) was applied to the gate terminal, while the source, drain, and back gate terminals were maintained at ground potential. This experimental setup is depicted in Figure 2.8, which illustrates the configuration of the terminals during the testing process.

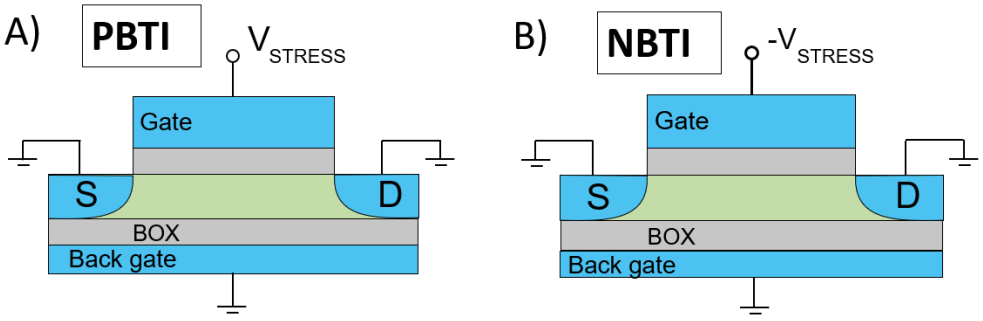


Figure 2.8 Biasing configuration to perform experiments of A) PBTI and B) NBTI.

Hot Carrier Injection HCI:

In the context of Hot Carrier Injection (HCI), we focused on the most detrimental stress scenario for short-channel devices, specifically where the gate voltage V_G equals the drain voltage V_D (i.e. $V_G = V_D$). In this situation, a stress voltage of 2.4V was applied at the same time to both the gate and drain terminals, as depicted in Figure 2.9 left. Meanwhile, the source terminal and the back gate were kept grounded to ensure a controlled environment for the stress testing. This configuration allows for a comprehensive analysis of the device's performance and reliability under more degraded conditions.

Off-state stress (OSS):

During the OFF-state tests, stress voltage was applied specifically to the drain terminal V_D, with all other electrodes maintained at ground potential to ensure accurate measurements, as depicted in Figure 2.9 right. The stress voltage was systematically varied within the range of 1.7 V to 2.5 V to thoroughly investigate how the different voltage levels influenced the degradation occurring in the OFF state. This approach allowed for a comprehensive analysis of voltage dependence on the performance of the device.

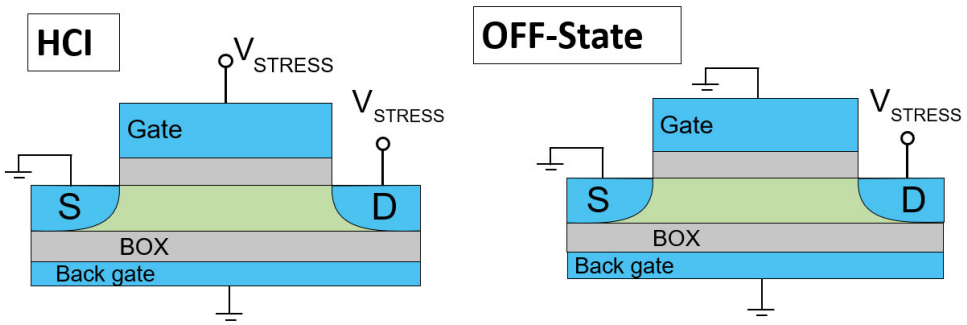


Figure 2.9 Biasing configuration to perform experiments of LEFT) HCI. RIGHT) OFF-state stress.

This setup focused on device-level characterization. The device under test (DUT) features four terminals, thereby requiring the utilization of four Source Measure Units (SMUs) to independently bias and measure each terminal.

Within the MSM technique, one method for assessing the degradation of the subthreshold slope (SS) is to compare the $I_D - V_G$ characteristics at $V_G = 0V$ (I_{D-OFF}) and $V_G = 1.2V$(I_{D-ON}).

The characteristics I_{D-ON} and I_{D-OFF} will be useful to measure degradation caused by aging. They are illustrated in Figure 2.10. I_{D-ON} is the drain current when the gate voltage is 1.2V 'on-state' and I_{D-OFF} is the drain current when the gate voltage is 0V 'off-state' as represented inside the black boxes in Figure 2.10. In this figure, the fresh $I_D - V_G$ of a device is represented in black and the $I_D - V_G$ characteristic of a degraded device in

red. The difference between I_{D-ON} and the I_{D-OFF} of the fresh device and the degraded device, is a measure of degradation.

This method is particularly important in situations where significant distortion in the $I_D - V_G$ characteristics makes the threshold voltage and mobility unreliable parameters for assessing device degradation.

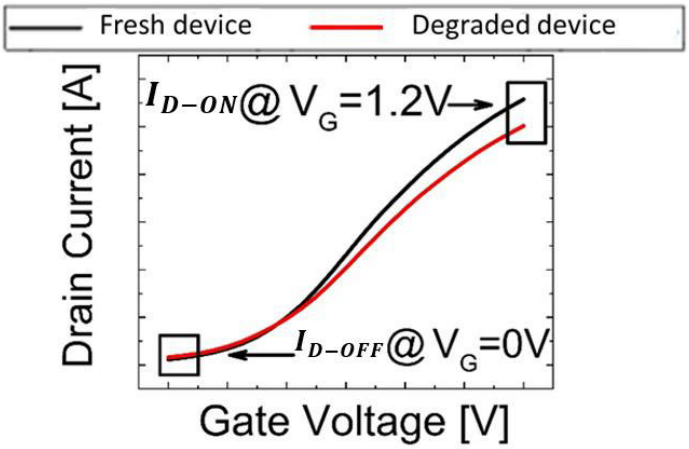


Figure 2.10 Representation of I_{D-ON} and I_{D-OFF} in a $I_D - V_G$ characteristic of the transistor. Black fresh device and red degraded device are represented.

2.4 Experimental Results

This section presents the experimental results derived from the characterization setup depicted in Figure 2.6. First, a comparison of the principal aging mechanisms is presented in Figure 2.11. The $I_D - V_G$ characteristics of the fresh device (before stress) are represented with black line, while the $I_D - V_G$ characteristics after 1500 seconds of stress are represented with red circles.

These characteristics were obtained at $V_{DS} = 50mV$. This figure presents the results of experiments conducted on devices with a width of $W = 300nm$ and a length of $L = 20nm$. Represented from left to right: OFF-state stress (OSS), NBTI, PBTI and HCI stresses at 2.4 V in linear scale (top) and log scale (bottom).

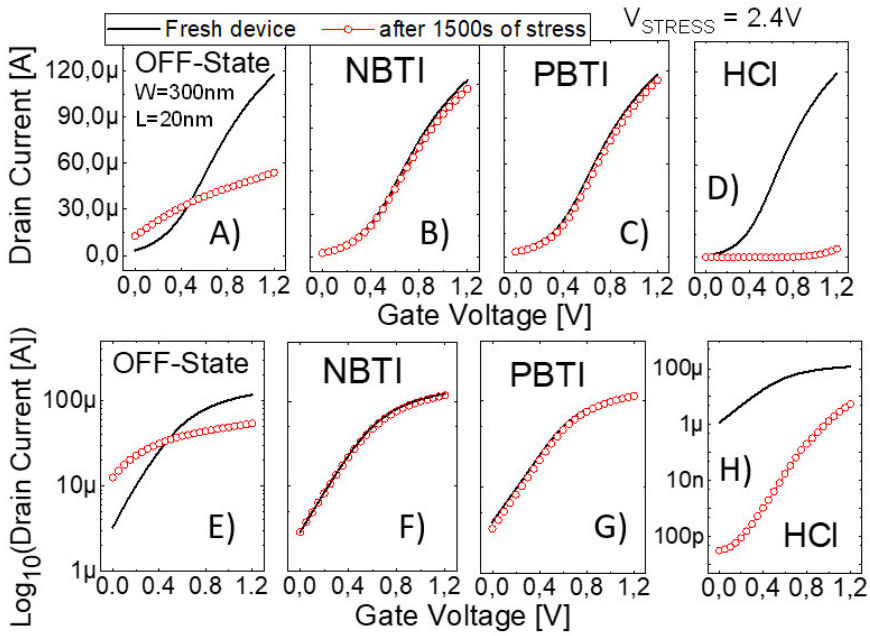


Figure 2.11 $I_D - V_G$ curves (V_{DS} = 50 mV) of the fresh device (black line) and after 1500 s of 2.4 V stress (red circles). Linear (top) and logarithmic (bottom) plots are shown.

For the fresh devices (black line in Figure 2.11), short channel effects (SCE) are evidenced by the large drain current (I_D) in the subthreshold region and the small threshold voltage ($\sim 0.25V$) as depicted in Figure 2.11 A) and E). Regarding the PBTI and NBTI stresses, no significant changes on the $I_D - V_G$ curves can be appreciated after the stress beyond a small reduction of I_{D-ON} (i.e., current at $V_G = 1.2V$).

However, for HCI and OFF-State tests, the consequences of the stress are clearly observed. For HCI stress, there is a large increase of the threshold voltage ($\sim 1\,V$) and the mobility is strongly reduced as depicted in Figure 2.11 D) and H). Therefore, the damage that I_{D-ON} experiences ($\sim 90\%$ reduction) is very detrimental (the largest, when compared to the other stress cases).

For OSS note that, though the $I_D - V_G$ characteristic is largely modified (Figure 2.11 A in red dots), the I_{D-ON} decrease is smaller ($\sim 50\%$). However, in this case the subthreshold current increases significantly and the $I_D - V_G$ characteristic is completely distorted as depicted in Figure 2.11 A) and E), being not possible to clearly identify the subthreshold region. I_D exhibits an almost linear dependence on V_G for large stress voltages, what means a large degradation of the device performance.

In Figure 2.12, a comparison of the $I_G - V_G$ characteristics is presented. These characteristics were obtained immediately after acquiring the $I_D - V_G$ curve. The analysis displays a logarithmic scale for the OFF-state stress (OSS), Negative Bias Temperature

Instability (NBTI), Positive Bias Temperature Instability (PBTI), and Hot Carrier Injection (HCI), arranged from left to right. As shown in Figure 2.12, the fresh devices are represented in black, while the stressed devices are marked with red circles.

As previously mentioned, both the OSS and HCI are particularly damaging to the dielectric's isolation properties (see Figure 2.12 A and D). This is evident from the significant leakage associated with these two mechanisms. In the OFF-state graphic shown in Figure 2.12 A), the leakage current is approximately ~0.1µA at -1V. In contrast, it appears that the dielectric is not significantly affected by NBTI and PBTI, as depicted in Figure 2.12 B) and C).

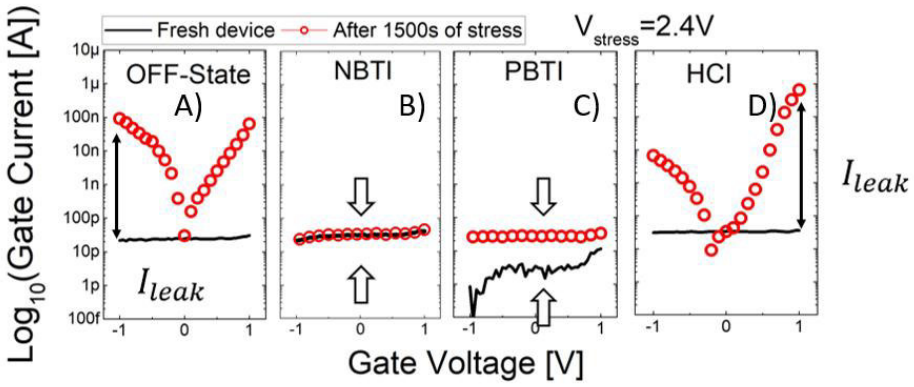


Figure 2.12 $I_G - V_G$ curves of the fresh device (black line) and after 1500 s of 2.4 V stress (red circles). For A) OSS. B) NBTI. C) PBTI. D) HCI

A more detailed comparison of the impact of the different kinds of stresses on the device properties has been made. Figure 2.13 shows the relative I_{D-ON} and I_{D-OFF} reduction suffered after OFF-State (blue triangles), PBTI (black squares), NBTI (red circles) and HCI (pink triangles) stresses as a function of stress time. As observed in Figure 2.13, negative and positive BTI produce the smallest variations on I_{D-ON} (<7% after 2000 s).

On the other hand, HCI provokes the largest reduction of I_{D-ON}, mostly induced within the first 100s of the stress (pink triangles in Figure 2.13 left), indicating that, in this technology, HCI is extremely harmful. Finally, for the OFF-State stress, I_{D-ON} shift suffers a fast increase at the beginning of the stress and then evolves smoothly with the stress time from ~20% (after the first inspection at 80 s) to ~50% after 2500 s (blue triangles in Figure 2.13 left), also exhibiting a saturation effect for larger stress times. Concerning I_{D-OFF}, there is no change for N/PBTI and it largely decreases for the HCI stresses (~100%) in comparison with the I_{D-ON}, but a huge increase is observed for the OFF-State case (~1000%, i.e., 10 times with respect the fresh I_{D-OFF} blue triangles in Figure 2.13 right).

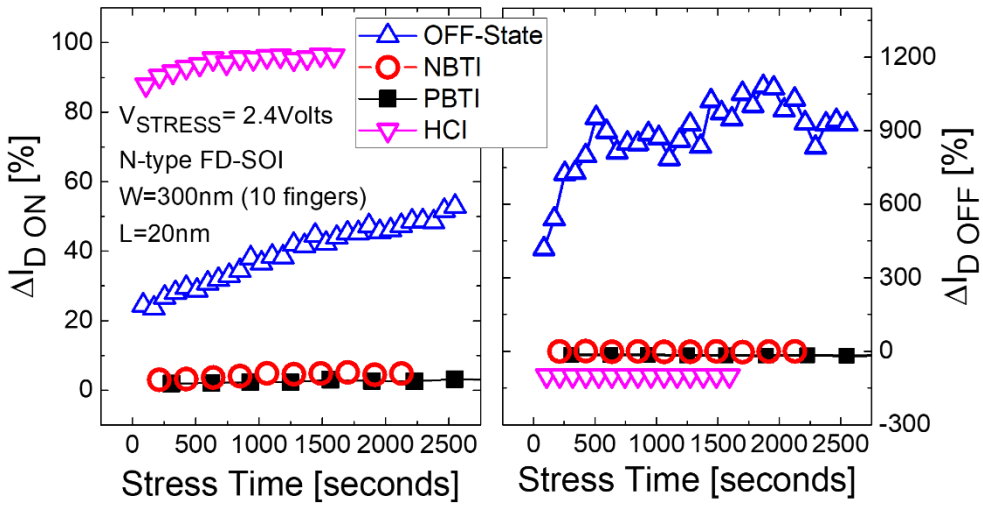


Figure 2.13 Absolute value of the relative I_{D-ON} (left) and I_{D-OFF} (right) variations for an OFF-State (blue triangles), PBTI (black squares), NBTI (red circles) and HCI (pink triangles) stress at 2.4 V, as a function of the stress time.

To get more insight into the OFF-state stress (OSS) aging mechanism, its voltage and time dependences have been evaluated. Figure 2.14 shows some examples of the $I_D - V_G$ curves measured after 2600 s of stress for 1.9V, 2V, 2.1V, 2.3V, 2.4V and 2.5V together with the fresh $I_D - V_G$ curves. Note that, for all the stress voltages, I_{D-ON} decreases with respect to the fresh value, measuring larger reductions for larger stress voltages.

On the other hand, I_{D-OFF} and the subthreshold slope (SS) increases with stress voltage, though the observed I_{D-OFF} degradation is very small for the lowest stress voltages (1.9 V to 2.1 V). These changes are critical for the largest stress voltages (>2.3 V), since the combination of both degradations, I_{D-ON} decrease and I_{D-OFF} increase, extremely distorts the $I_D - V_G$ characteristic, as previously highlighted in Figure 2.14.

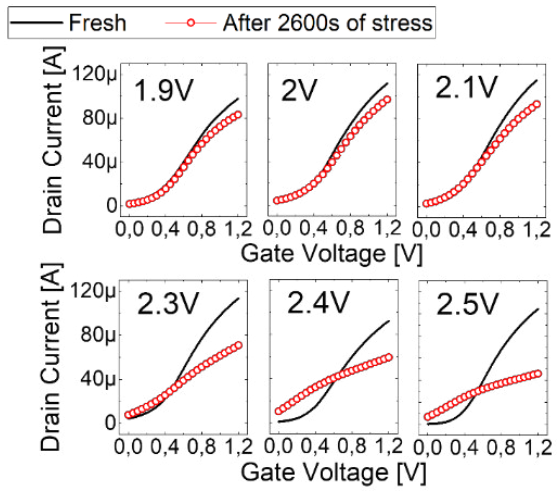


Figure 2.14 $I_D - V_G$ curves (V_{DS}=50mV) value of the fresh device (black line) and after 2600s of OSS (red circles) at 1.9 V, 2 V, 2.1 V, 2.3 V, 2.4 V, 2.5 V.

In Chapter 1, the temporal evolution of degradation resulting from various aging mechanisms affecting transistors was introduced. This degradation is typically characterized by a steady decline in key parameters of the transistor. A power law model is often adhered to, indicating that when these changes are plotted on a double logarithmic graph, a straight line is formed by the data points. This characteristic is illustrated in Figure 2.15, where the predictable nature of degradation over time is demonstrated.

The temporal evolution of I_{D-ON} and I_{D-OFF} variations as parameters to quantify degradation, together with the voltage dependences, for the case of the OSS degradation are analyzed in Figure 2.15. For I_{D-ON} (left), as expected, the larger the stress conditions (voltage and time), the larger the I_{D-ON} degradation, reaching a 60% reduction after 2600 s at 2.5 V.

On the other hand, for I_{D-OFF} (right), only for large enough stress voltages (~2V), an increase of this parameter is observed following the power law. For the lowest stress voltages such as 1,7V, 1,8V and 1,9V I_{D-OFF} decreases with stress time, as can be seen in the subfigure of Figure 2.15 (right), reaching a ~40% reduction for 1.9 V at the end of the test. However, I_{D-OFF} is 30 times the fresh value, for the stress at 2.5 V. All these results indicate that the OFF-state stress modifies the subthreshold and ON operation regions of the device, by increasing the leakage current through the channel and reducing the ON current I_{D-ON}, largely affecting the device performance, as observed in Figure 2.15.

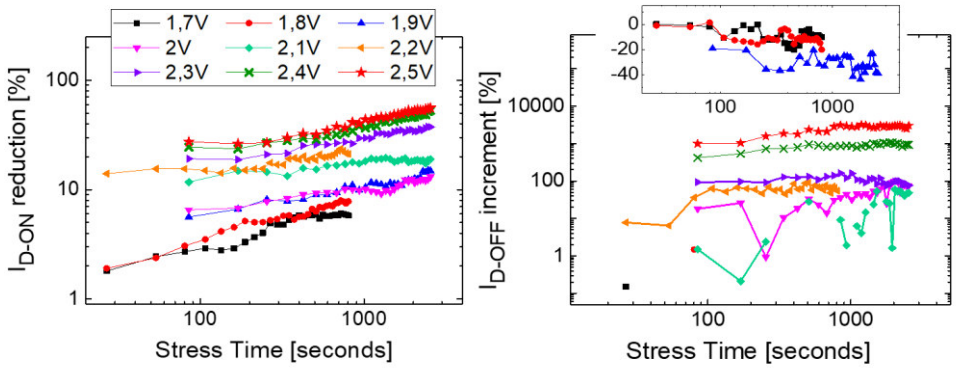


Figure 2.15. Relative I_{D-ON} reduction (left) and I_{D-OFF} increment (right) as a function of the stress time for OFF-State stresses at V_D ranging from 1.7V to 2.5V.

For a better understanding of the effects of each of the aging mechanisms, the currents through the four terminals of the device (gate, drain, source and back gate) during HCI and OSS stresses have been analyzed. Figure 2.16 depicts the I_D(blue), I_G(red), I_S (green) and I_{BG} (black) currents measured during the stress phase of the MSM tests at 2,4V in logarithmic scale for the current and for the time on top of the figure, and linear/logarithmic plot on the bottom.

I_{BG} current shows no relevant change during the test, that means that the buried oxide (BOX) damage can be neglected. For the case of drain terminal current I_D and source terminal current I_S, which have the same magnitude but opposite sign, are larger in the case of the HCI stresses. Moreover, the temporal trend of the currents (see Figure 2.16) for the two stresses is opposite: whereas they smoothly increase in Figure 2.16 A and C (in absolute value) with time for the OFF-state stress, they decrease for the HCI case (Figure 2.16 B and D). Surprisingly, when compared to the fresh device, there is a large increase of the gate current after both kinds of tests. Though at the end of both tests the magnitude of I_G is similar, the temporal evolution differs. For the OSS, I_G remains small until the stress time is large enough (approximately 20 s in the example shown), and then it increases smoothly until a relatively constant value.

In the case of the HCI tests (see Figure 2.16 B and D), however, a large increase is observed at very short stress times and evolves with a similar trend as in the case of the OFF-state until the final value. Despite the different temporal trends, the increase of I_G suggests a significant degradation of the gate dielectric in the two cases.

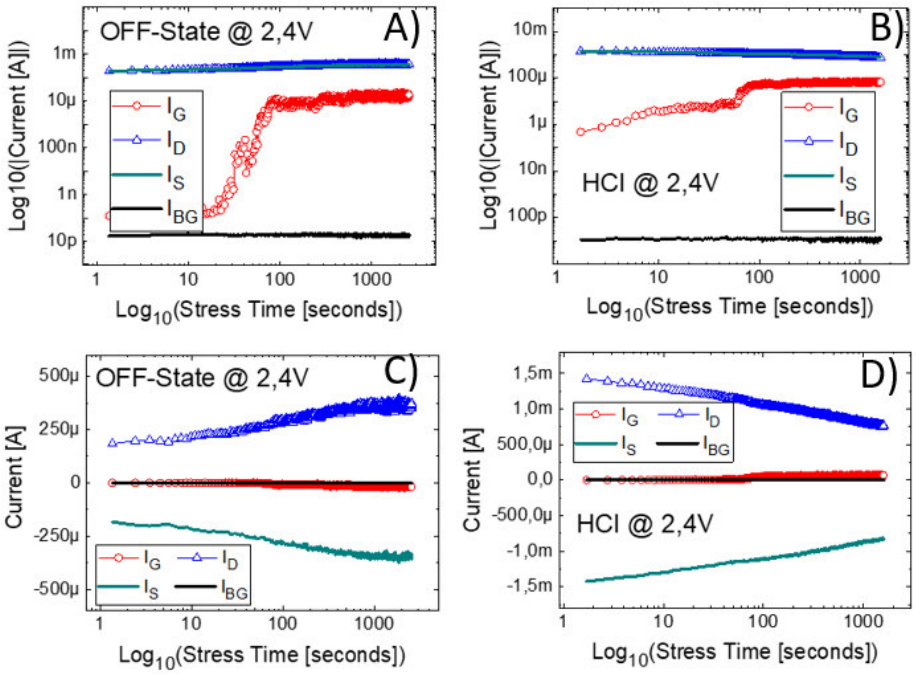


Figure 2.16. I_D (blue), I_G (red), I_S (green) and I_{BG} (black) currents registered during the stress phase of the OFF-State (left A and C) and HCI (right B and D) tests at 2.4 V. Top figures show the absolute value of the currents in a log scale; bottom figures those currents in linear scale (with their sign).

To understand better the electric fields and currents that operate within the transistor, particularly in relation to aging mechanisms during the stress biasing phase, a detailed schematic of these various fields is presented in Figure 2.17. During negative/positive bias temperature instability N/PBTI stress tests, a uniform distribution of the electric field within the device is exhibited along the channel (see Figure 2.17 A and B), indicating a consistent interaction across its length.

In contrast, noticeable asymmetry in the electric field is observed during the OFF-state (OSS) and hot carrier injection (HCI) tests as represented in red arrows in Figure 2.17 C and D). Furthermore, an inversion channel is established during positive bias temperature instability (PBTI) and HCI testing depicted in green in Figure 2.17 B and D, allowing for a distinct current flow that alters the behavior of the device. It is important to note that substantial ON currents can be cross through the channel during HCI stress testing represented in a purple arrow from drain terminal to source terminal.

Although no channel has been created during the OSS stresses, large leakage current between drain and source are measured due to the lateral electric field applied, which is represented with red arrows in Figure 2.17.

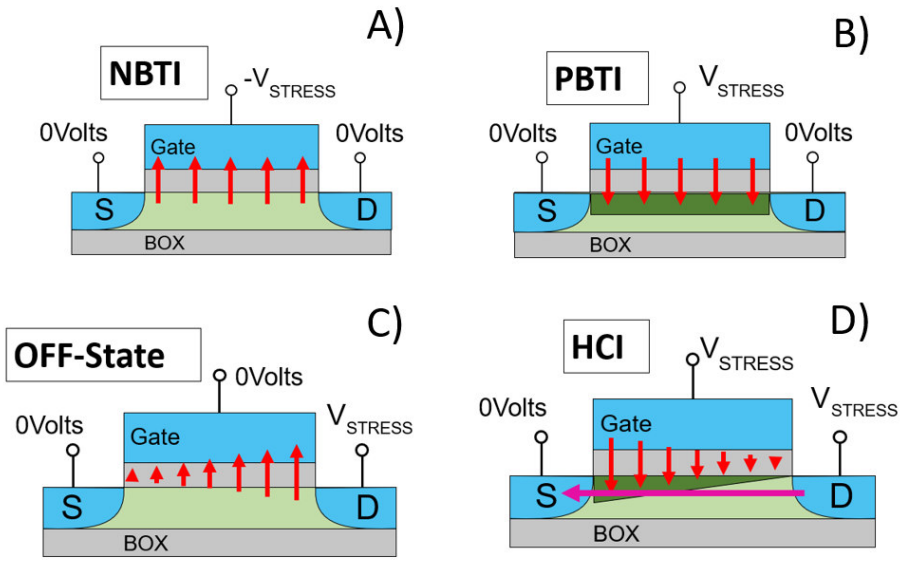


Figure 2.17. Schematic representation of the sign and magnitude of the electric field applied to the dielectric. The inversion channel created during PBTI and HCI tests is depicted in green. The large channel current that can flow during the HCI stresses is represented by the purple arrow from drain to source.

In Figure 2.18, the I_D, I_G, I_S and I_{BG} recorded during a V_G sweep (with $V_{DS} = 0$) when the stress was interrupted after 1500s of stress at 2.4 V, for the 4 considered stresses, together with the fresh currents (coloured lines), are depicted as a function of the gate voltage. Both the ON region (positive voltages) and OFF region (negative voltages) are analysed. The figure shows that, for the BTI tests, the changes in all the currents are very small, independently of the operation region, corroborating that BTI aging (positive or negative) is negligible in these devices.

This is not the case for the OSS and HCI tests, where important changes in all currents are recorded after the stress, in the ON and OFF regimes. For these tests, in addition to the previously shown changes in the ON regime (Figs. 2.11 to 2.15), (i) an important increase of the gate current is measured for both gate voltage polarities and (ii) leakage currents through the drain and source are measured for negative gate voltages. Looking in more detail into the OFF regime (i.e. the negative voltages), one can note that the gate current is almost coincident with the drain current for the OFF-state stress but with the source current for the HCI stress. This result could be interpreted as a larger damage of the bulk dielectric close to the drain for the OFF-State stress (OSS) and close to the source for the HCI stress [74]. The reason of this observation could be the larger vertical fields close to these terminals applied during these stresses (see Figure 2.17).

Since the increase of gate current is not observed during BTI tests (for which there is not current flow through the channel during the stress), the results suggest that currents are also needed (leakage during the OFF-State or ON currents during the HCI stresses) to introduce damage in the bulk of the dielectric (i.e. generate defects), leading to trap-

assisted tunneling through the gate [75]. Note that gate current to appear requires long enough stress time or voltages (see Figures 2.14 and 2.16).

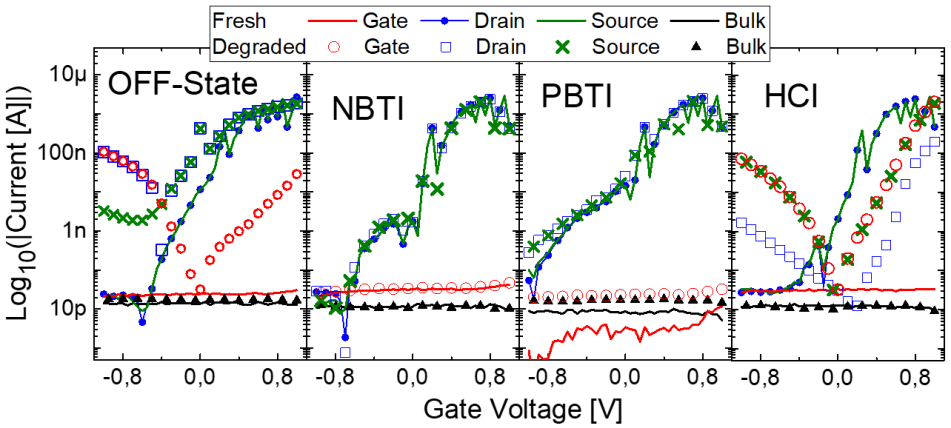


Figure 2.18. I_D (blue), I_G (red), I_S (green) and I_{BG} (Black) currents registered during a V_G sweep (with V_{DS} = 0 V) for the fresh (lines) and stressed (symbols) devices after 1500 seconds and 2.4 V of OFF-State (OSS), NBTI, PBTI and HCI stresses (from left to right).

Regarding the back gate current, it was always close to the noise level, before and after the stresses, indicating that the BOX suffers a negligible damage and is not affected by any of these aging mechanisms.

2.5 Conclusions

In this Chapter, the degradation of N-type FDSOI Ω-gate NW-FETs induced by PBTI, NBTI, HCI and OSS was experimentally analyzed and compared. NBTI/PBTI have the smallest (negligible) effect on the device performance, whereas HCI stress produces the largest I_{D-ON} degradation, linked to a large increase/decrease of V_{TH}/µ, respectively.

However, though the OSS induces a decrease of I_{D-ON} smaller than that measured for HCI, for large enough stress conditions (voltage/time), a large increase of the subthreshold current (I_{D-OFF}) is observed, which can lead to a complete distortion of the $I_D - V_G$ characteristic of the device and, therefore, to the loss of the device functionality. This increase of the subthreshold current has been attributed to the gate current that appears as a consequence of the degradation of the bulk of the gate dielectric during the OSS stresses.

3. First observations of Resistive Switching in FD-SOI Ω-gate transistors

The results of this chapter are reproduced and/or adapted from:

- *C. Valdivieso, R. Rodriguez, A. Crespo-Yepes, J. Martin-Martinez, M. Nafria, "Resistive switching like-behavior in FD-SOI Ω-gate transistors", Solid-State Electronics, Volume 209, 2023.*

- *C. Valdivieso, R. Rodriguez, A. Crespo-Yepes, J. Martin-Martinez, M. Nafria, "Resistive Switching phenomenon in FD-SOI Ω-Gate FETs: Transistor performance recovery and back gate bias influence", Solid-State Electronics, Volume 225, 2025.*

Memristor are resistive switching devices with applications in non-volatile memories, alternative computer architectures and cryptography [76] between others. There are also alternative emerging technologies (e.g. nanowire transistors, nanosheets)[77] that are being studied for this purpose. Although these technologies are still in research, it is necessary to introduce valuable information to suggest possible solutions to potential problems in industry. In this way, in this chapter, an analysis of the resistive switching phenomenon in FD-SOI Ω-gate nanowire transistors is performed.

3.1 Resistive Switching-like behavior in FD-SOI transistors

In this section, the observation of RS in FDSOI N-type Ω-gate NW-FETs is presented. The location of the conductive filament along the transistor's channel and the variation of transistor characteristics during switching are investigated.

3.1.1 Device description

The samples used in this chapter correspond to the 'Snow' wafer described in chapter 2. In Table 3.1 the total number of devices used in this chapter is shown, organized by name of scribe, length and width. They have been registered after measurement.

The process of choosing these samples involved testing various options until we finally selected the Scribe N2 of the wafer, which possessed properties suitable for producing stable RS results. These properties included a quasi-planar structure resembling that of

planar transistors. Additionally, the dimensions of the transistors, measuring 10 µm x 10 µm, suggested a rectangular shape that was ideal for initiating the tests.

Scribe Name	W(μm)	L(μm)	Orientation	Type (n/p)	# of Samp. used
N2	10	10	0	N	112
N3	10	10	45	N	3
N4	10	10	90	N	7
N31N	10	10	0	N	7
N6	0.24	10	0	N	3
N1P	10	10	0	P	3
N1	10	0.01/0.02/0.03/0.05	0	N	4
N1N	10	10	0	N	32
N21N	10	10	0	N	9

Table 3.1 List of the samples used in this chapter. Different dimensions, orientations and types of transistors were tested.

Device N2: It has a dielectric which is a combination of $HfSiON/TiN$ with equivalent oxide thickness of EOT = 1.3nm. The device's dimensions are $W = 10\mu m\ x\ L =$ $10\ \mu m$. The nanowire height is $H_{NW} = 11nm$. The device contains a buried oxide layer (BOX) with a thickness of $145nm$. It is a single finger structure. The gate terminal comprises entirely of a poly-silicon layer. The transistors are type-n and have a [110]-crystal orientation. As the dimensions of the width and the length are much greater in comparison to the nanowire height, these devices can be considered as 'quasi-planar' transistors. The structure of FD-SOI nanowire transistor is represented schematically in Figure 3.1 A.

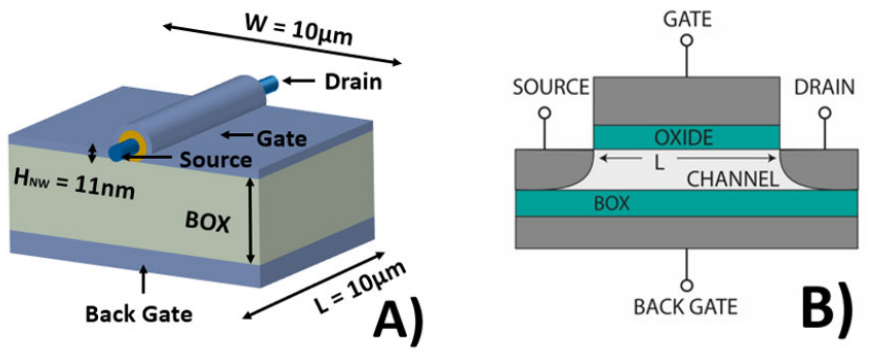


Figure 3.1 3D sketch of the Ω-Gate structure quasi-planar transistor (A) and cross-section (B) of the planar representation of the FD-SOI transistors used in this work.

3.1.2 Setup for Resistive Switching experiments

In the setup to perform the measurements presented in this chapter, the precision semiconductor parameter analyzer SPA Agilent 4156C is utilized. The SPA is equipped with four source monitor units (SMUs), which connect to the wafer probe station (WPS) to apply and measure voltage and current. The Agilent 4156C is connected to the computer via general purpose interface bus (GPIB) protocol to perform more flexible measurements and facilitates data acquisition as depicted in Figure 3.2.

In this thesis, the characterization setup was adapted based on the mechanism being tested. The proposed measurement setup utilizes smart control through General Purpose Interface Bus (GPIB) communication. GPIB or IEEE-488.1 is a standard for communication between electronic instruments (oscilloscopes, function generators) and computers. This protocol facilitates measurement acquisition.

The Agilent 4156C is managed through GPIB communication using MATLAB software, providing enhanced control over the sample characterization process, including the ability to pause and resume stress testing as needed.

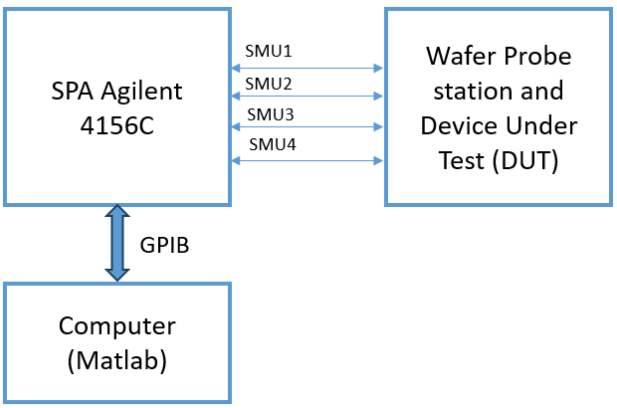


Figure 3.2 Block diagram of the measurement setup: the SPA is connected to the computer via GPIB and electrically connected to the device under test through 4 SMUs.

3.1.3 Measurement procedure

The measurement procedure used for these experiments is represented in Figure 3.3. The measurement sequence was performed as follows:

1) The first step is to characterize the initial electrical behavior of the fresh transistor, measurements such as: $I_G - V_G$, $I_D - V_G$, $I_D - V_D$.
2) A current-controlled forming cycle was conducted using the SPA Agilent 4156C. This process involved applying a voltage ramp from 0V to 4V with compliance of 4mA. Once the voltage reached its maximum value, the ramp was automatically stopped. During this step, a conductive filament was created. The next step is to characterize the transistor's characteristics such as: $I_G - V_G$, $I_D - V_G$, $I_D - V_D$ to measure the change of these characteristics after the creation of a CF.
3) A current-controlled set process is conducted, ramping the voltage from 0V to 5V with a compliance of 5mA using the SPA, as previously described. After completing the set process and confirming that the sample is in low resistance state (LRS), the characteristics of the transistor are measured again as shown in Figure 3.3.
4) Finally, a reset process is conducted, dropping the voltage from 0V to -3.5V with compliance of 10mA. Once the voltage reaches its maximum value, it is gradually reduced to 0V. After this step, the transistor characteristics are measured once more. The set/reset cycles are repeated based on the outcomes of the experiments.

The values of the voltages and currents selected in the previous steps are a consequence of a previous work to find the adequate conditions to observe RS. Several measurements were performed to find the appropriate values to observe a steady RS cycle.

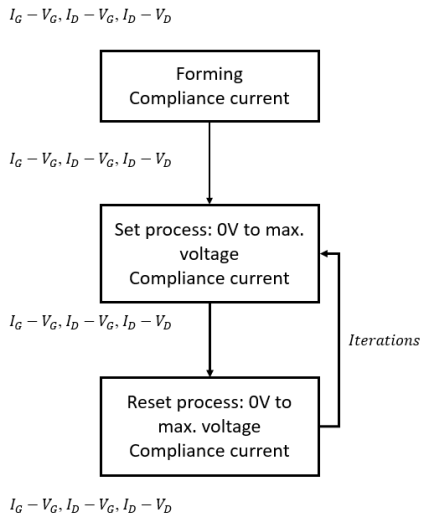


Figure 3.3 Diagram of the measurement sequence used in these experiments.

To perform the RS measurements, all four terminals of the transistor were contacted as shown in Figure 3.4 left. During the whole process (RS cycles) the four currents through

the transistor terminals (I_G, I_D, I_S, I_B) were registered. That is: after forming, set and reset processes.

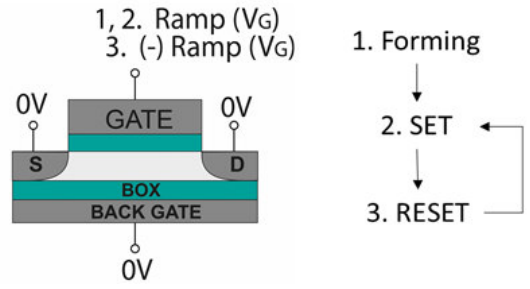


Figure 3.4 LEFT: Biasing configuration of the four device terminals to produce forming, set and reset processes. RIGHT: measurement sequence to perform a complete RS cycle.

3.1.4 Experimental Results

The experimental setup described in the previous section outlines the procedure to achieve a steady RS cycle. Figure 3.5 shows three consecutive experimental gate I-V curves in the same sample, after the forming process. A difference in voltage occurrence (dispersion) of set and reset can be appreciated. In the performed measurements, set/reset voltages vary between 2.5 V and 5V and from -1.3V to -2.5V, respectively (see Figure 3.5).

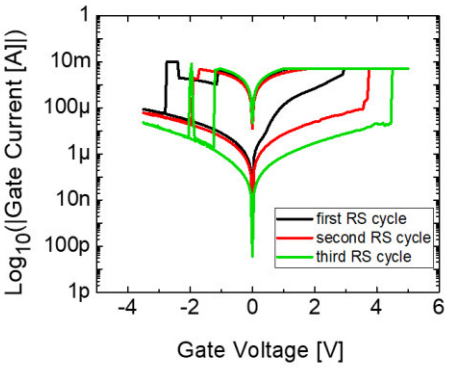


Figure 3.5 I-V characteristics measured in the same sample during three consecutive RS cycles, after a forming process.

The use of transistors allows the analysis of the RS filament location along the channel [78]. Figure 3.6 shows the four terminals transistor currents captured at the same time as measured resistive switching corresponding to the first (Figure 3.6. left) and the second (Figure. 3.6 right) $I_G - V_G$ curves of RS cycle presented in Figure 3.5.

In Figure 3.6 left, for positive voltage range, both in the LRS and HRS, drain and gate currents are also equal which suggests a RS path located close to the drain terminal. In

the negative voltage range, during the LRS the filament is still located close to the drain. However, when reset process is produced, and the device reaches the HRS, a RS path close to the source becomes more relevant. In Figure 3.6 right, the filament close to the source is always predominant in all the RS cycle. Then, the results show the existence of conductive filaments close to the drain and source terminals, and their dominance depends on the RS cycling.

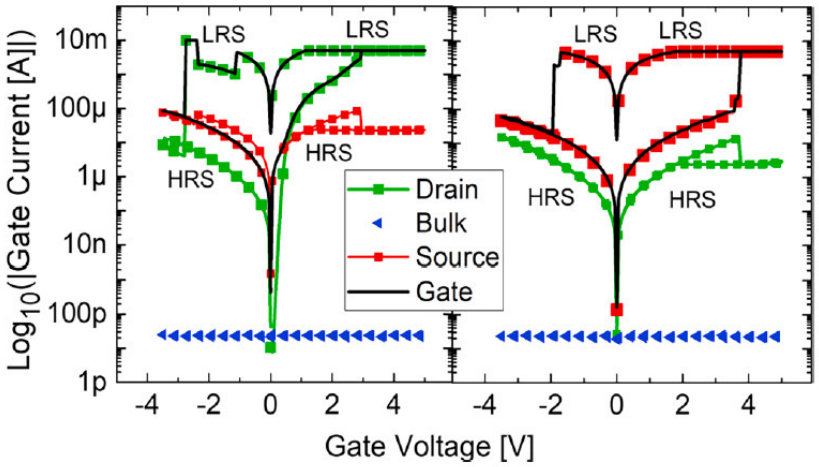


Figure 3.6 I_D (green), I_B (blue), I_S (red), I_G (black) currents registered during first (left) an second (right) RS cycles in Figure 3.5.

In Figure 3.7, the transistor's characteristics $I_D - V_G$ are presented. The $I_D - V_G$ characteristic of a fresh sample is depicted in black, after set process in blue and after reset process is depicted in red. As shown in Figure 3.7, there is a large difference in the current after reset and set processes, the $I_D - V_G$ transistor curves are completely distorted, and the transistor's functionality cannot be recovered after reset.

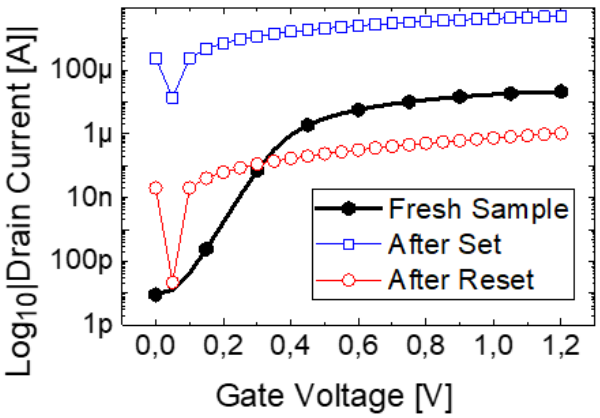


Figure 3.7 $I_D - V_G$ characteristics of the fresh sample (black) and after set (blue) and reset (red) processes.

Figure 3.8 shows the $I_D - V_D$ characteristic of a fresh device (Figure 3.8 A). After forming (Figure 3.8 B), the $I_D - V_D$ curve is still distinguishable but after set (Figure 3.8 C) the functionality of the device is completely lost and cannot be recovered after reset (Figure 3.8 D). The results suggest that the electrical conditions applied to observe RS in these devices produce severe damage in the dielectric, largely affecting the transistor functionality.

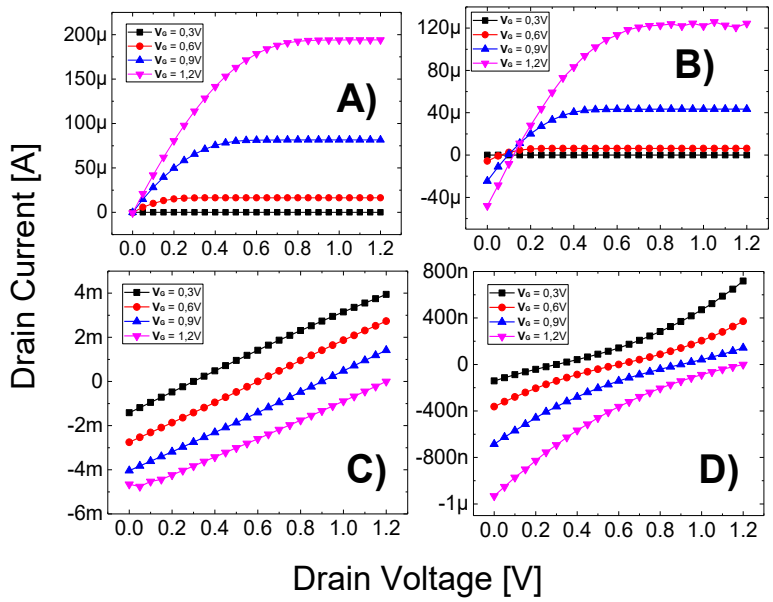


Figure 3.8 $I_D - V_D$ transistor characteristics A) for fresh device. B) After forming. After set C) and reset D) processes.

3.2 Partial recovery of transistor's characteristics during RS

Although RS is usually exploited and researched in two terminal devices, RS was observed in bulk MOSFETs [78] and more recently also in FD-SOI quasi-planar transistors [79], as was presented in the last paragraphs. This opens the possibility of using the device as either a transistor or a memristor, as necessary [78].

In the work presented in SSE2023_1, the electrical conditions used to observe the RS caused significant damage to the transistor's functionality. In contrast to that study, this work analyzes the RS voltage and current conditions required to partially recover the $I_D - V_D$ curves. In this section, samples, setup and measurement procedure are the same as the ones in section 3.1.

3.2.1 Results and discussion

The results presented in this subsection are the outcome of extensive experimental work involving numerous measurements. This extensive effort enabled us to accurately determine the appropriate voltages and current compliance limits required to observe the RS cycle and to recover the transistors' $I_D - V_D$ characteristics.

Figure 3.9 UP shows the $I_G - V_G$ curves measured during the forming process (Figure 3.9 A) and a complete RS cycle, i.e. a reset followed by a set. (Figure 3.9 B). The electrical conditions applied in the electroforming process (Figure 3.9 A) are a continuous voltage sweep ranging from V_G = 0 V to 4 V, with a current compliance limit of 4 mA for the gate current (I_G). The reset process was measured by applying a negative voltage ramp to the gate terminal, ranging from V_G = 0 V to - 2V, with gate current compliance of I_G = 8 mA (Figure 3.9 B Left). The set process was measured by applying positive voltages to the gate terminal, ranging from V_G = 0 V to 4 V with a gate current limit of I_G = 4.5 mA (Figure 3.9 B Right).

The $I_D - V_D$ characteristics were obtained by applying voltage ramps to the drain terminal, with voltages ranging from $V_D = 0V$ to 1.2 V, while setting the gate voltage at V_G = 0.3 V, 0.6 V, 0.9 V and 1.2 V and the back gate voltage at $V_B = 0V$. The $I_D - V_D$ curve of the fresh sample (i.e., before forming) is depicted in Figure 3.9 C. The $I_D - V_D$ characteristics of the transistor measured after the forming process are illustrated in Figure 3.9 D. Note that in a reduced drain voltage range (from 0 to 0.1 V), larger currents than for the fresh case and a negative dependence with voltage is observed, reaching I_D = 0 at V_B = 0.1 V. However, for larger voltages, a similar shape is observed, though with smaller currents, when compared to the fresh case (Figure 3.9 C), indicating that the device can be still operated as a FET.

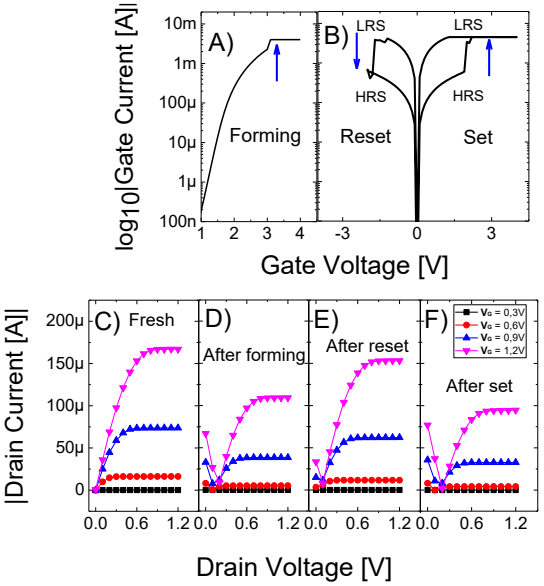


Figure 3.9 UP: Experimental $I_G - V_G$ curves for A) forming, B) reset and set processes. DOWN: $I_D - V_D$ transistors characteristics at different gate voltages for C) a fresh device. D) after forming. E) after reset and F) after set process. In all cases $V_B = 0V$.

The transistor's $I_D - V_D$ curves following reset and set processes are shown in Figure 3.9 E and Figure 3.9 F, respectively. Similar trends than those described for the post-forming curves are observed, i.e. an initial voltage range that shows negative resistance followed by typical MOSFET behavior. However, focusing the attention in the last case, the current levels depend on the dielectric state: when compared to the values measured in the fresh device, smaller currents are observed after set but currents are similar after reset.

Then, the transistor current driving capability is partially recovered after undergoing the reset process (Figure 3.9 E). As an example, I_D after reset process measured at V_G = 1.2 V and V_D = 1.2 V decreases approximately 9% with respect to the corresponding current of the fresh sample (see $I_D - V_D$ characteristic in Figure 3.9 C and Figure 3.9 E), preserving the transistor functionality. This result was validated through several experiments, which revealed that by reducing the current compliance (I_G = 8 mA) and limiting the gate voltage (V_G = - 2V) during the reset process as shown in Table 4.1, the transistor is still operative, though the operating voltage region has slightly changed, as shown in Figure 3.9 E and Figure 3.9 F.

Electrical conditions of RESET process in section 3.1 (Transistor characteristic distorted)	**Electrical conditions of RESET process to recover transistors performance (section 3.2)**
$I_G(limit) = 10mA$	$I_G\ (limit) = 8mA$
max $V_G = -3.5V$	max $V_G = -2V$

Table 3.2 Change, respect to the experiments in section 3.1, in the characteristic of the reset process that reduced severe damage in transistors.

3.3 Impact of the back gate bias on RS

In this section, it will be preliminary analyzed the impact of the back gate bias on the RS phenomenon in FD-SOI Ω-gate FETs (section 3.1 and section 3.2 samples). In these devices, the back gate voltage (V_B) influences transistor's performance [80], [81], [82]. In this section, the effect of V_B on RS is evaluated.

3.3.1 Results and discussion

Figure 3.10 illustrates the measurement procedure for three distinct cases used to compare the influence of the back gate bias voltage in the set and reset processes. In the first case (Figure 3.10A), a positive voltage sweep from 0 to 4 V is applied to the gate terminal (V_G) while a constant negative voltage is simultaneously applied to the back gate terminal (V_B). Voltages of $V_B = 0, -0{,}1V, -0{,}2V, -0{,}3V$ and $-0{,}4V$ are considered. This voltage configuration will be used to analyze the V_B impact on the RS cycle applying these conditions only on set process (V_B = 0 V during the reset process).

In the second case (Figure 3.10 B), a negative voltage sweep from 0 to - 2V is applied to the gate terminal (V_G), with a constant negative voltage of V_B = -0.2V applied simultaneously to the back gate terminal. This voltage configuration will be used to analyze the V_B impact on the RS cycle by applying these conditions only on the reset process (V_B = 0 V during the set process).

In the third case (Figure 3.10 C), a positive voltage sweep (from 0 to 4V) is applied to the gate terminal (V_G), immediately following this, a negative voltage sweep (from 0 to -2V) is applied to the gate terminal. The back gate terminal is biased with a constant negative voltage of $V_B = -0.2\,V$, during both set and reset processes. This voltage configuration will be used to analyze V_B impact on the complete RS cycle applying $V_B \neq 0$.

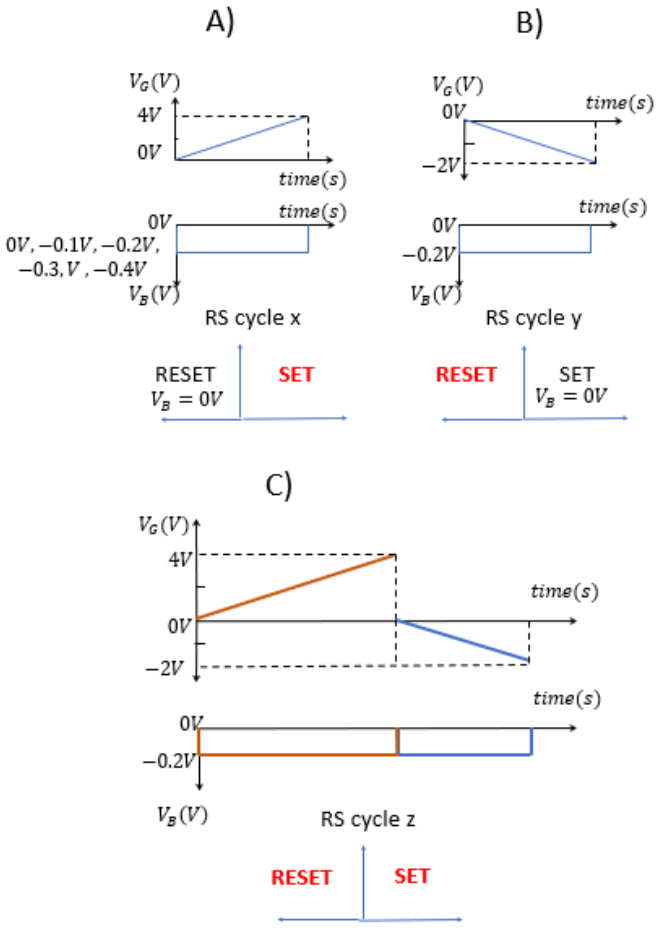


Figure 3.10: Measurement procedure of three approaches used to compare back gate voltage influence in RS set and reset events A) V_B = 0 V, − 0.1 V, − 0.2 V, − 0.3 V, − 0.4 V during set process B) V_B = −0.2 V during reset process C) V_B = − 0.2 V during reset and set processes.

Figure 3.11 shows the average of three RS cycles, when V_B is only applied during the set process (voltage configuration shown in Figure 3.10 A), for the cases of $V_B = 0\ V$ (Figure 3.11 A), $-$ 0.1 V (Figure 3.11 B), $-\ 0{,}2\ V$ (Figure 3.11 C), $-\ 0{,}3\ V$ (Figure 3.11 D) and $-\ 0{,}4\ V$ (Figure 3.11 E). To evaluate the impact of V_B on the device performance, the I_{ON}/I_{OFF} ratio has been used as parameter to describe the device performance. I_{ON} is measured when the sample is in the LRS, and I_{OFF} is measured when the sample is in the HRS. This ratio was measured for $V_G = -1\ V$ and $V_G = +1\ V$ (see Figure 3.11 A and Figure 3.11 D). This mean ratio is calculated over three cycles for each voltage configuration using a single sample.

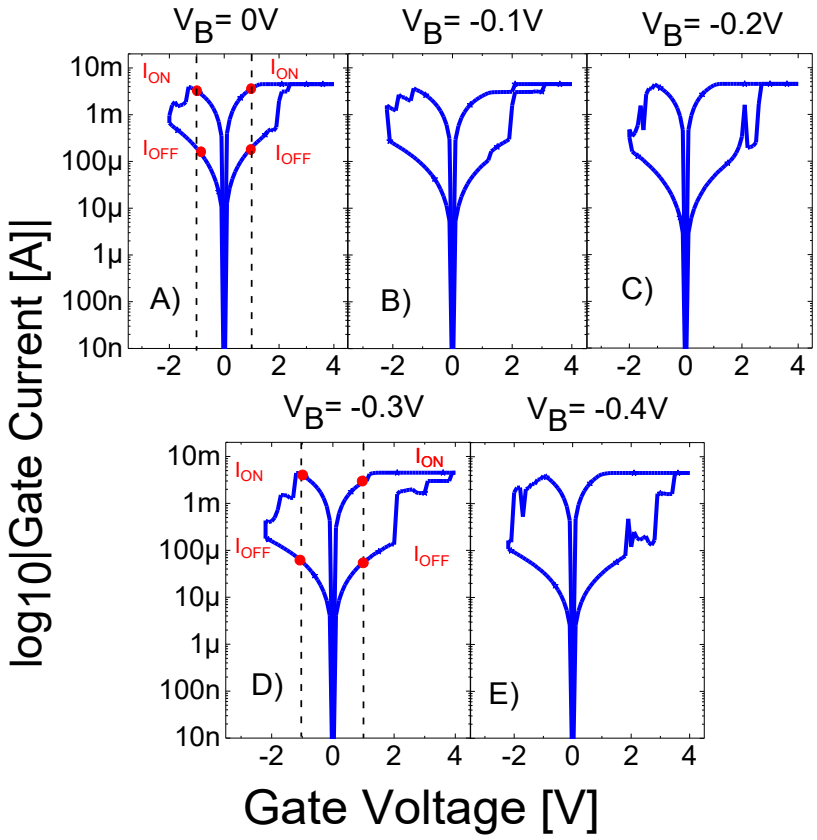


Figure 3.11 RS I-V average curves of several cycles measured on the same sample when A) V_B= 0V, B) V_B= -0.1V, C) V_B= -0.2V, D) V_B= -0.3V, E) V_B= -0.4V during set process. In (A) and (D) the I_{ON} and I_{OFF} currents measured at V_G = -1V and V_G = +1V to obtain the I_{ON}/I_{OFF} ratio is illustrated.

Figure 3.12 shows the I_{ON}/I_{OFF} mean ratio measured at $V_G = -1\ V$ and $V_G = +1\ V$ as a function of V_B. The increasing I_{ON}/I_{OFF} ratio (averaging all the cycles) measured at $V_G = -1\ V$ shows an increase with V_B (see Figure 3.12 blue solid line) and it facilitates the distinction between the memristor conduction states, which is beneficial for memory applications. However, this I_{ON}/I_{OFF} ratio shows no stable increment with V_G when it is measured at V_G = +1V (see Figure 3.12 red dash line). This can be attributed to the transversal electric field effect at negative back gate voltages in these wide-channel

devices (W=10µm) [56], due to the total voltage applied to the structure. This electric field can affect the conductive path structure during RS, especially during the reset process, decreasing the dielectric conduction (see Figure 3.11), and consequently, increasing the I_{ON}/I_{OFF} ratio.

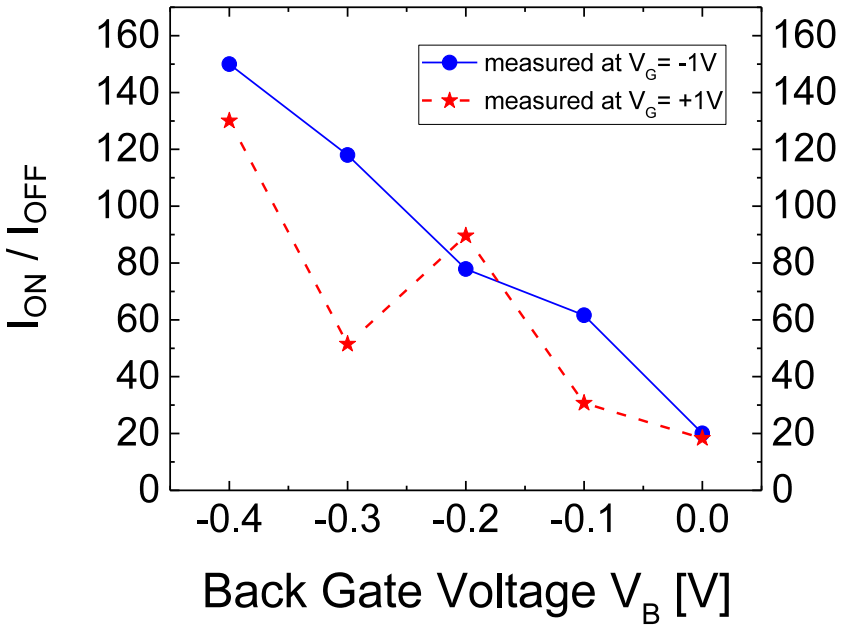


Figure 3.12 I_{ON}/I_{OFF} mean ratio measured at V_G =-1V (blue) and at V_G = +1V (red) as a function of back gate voltage (V_B) for the measurements represented in Figure 3.11.

To provide a clearer understanding of this concept, a graphical analysis was conducted. As depicted in Figure 3.13, the total electric field generated by the negative voltage during the reset phase is measured at -1.8V (red arrow in Figure 3.13, left). This voltage level is inadequate for effectively decreasing the conduction through the dielectric material. In contrast, during set process, the total electric field reaches (red arrow in Figure 3.13, right) 4.2V.

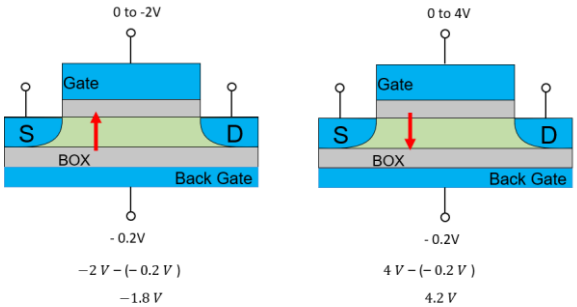


Figure 3.13. Schematic representation of the electric field generated during reset and posterior set processes for the configuration in Figure 3.10C

Continuing with the analysis of the influence of the back gate in RS, in Figure 3.14 A, the average of three RS cycles obtained when $V_B = -0.2\,V$ during the reset process and $V_B = 0\,V$ during the set process (see configuration in Figure 3.10 B) is shown.

In contrast, Figure 3.14 B shows the average of three RS cycles when $V_B = -0.2\,V$ during both reset and set processes (configuration in Figure 3.10 C). The I_{ON}/I_{OFF} mean ratio (averaging all the cycles) for the curves in Figure 3.14 A and 3.14 B respectively are qualitative equal. Note that, when compared to the case in Figure 3.11 C i.e. when $V_B = 0\,V$ during the reset, in both cases, no significant impact of V_B on the I_{ON}/I_{OFF} mean ratio is observed, as far as can be expected in two different samples.

These preliminary results suggest, in contrast to the experiment in Figure 3.11, seems to indicate that there is no significant impact of V_B on RS characteristics when the reset and both set and reset processes are studied i.e. $V_B = -0.2\,V$ only during reset and $V_B = -0.2\,V$during set and reset (see configuration in Figure 3.10 B and 3.10 C)

In the first case, (Figure 3.14 A), the electric field (during the application of $V_B \neq 0\,V$ during the reset process) contributes to larger conduction through the conductive filament.

In the second case, Figure 3.14 B although $V_B \neq 0\,V$ is applied during both set and reset processes consecutively, the electric field generated by the negative voltage (during the reset process) remains insufficient to decrease the conduction through the conductive filament formed during the set process.

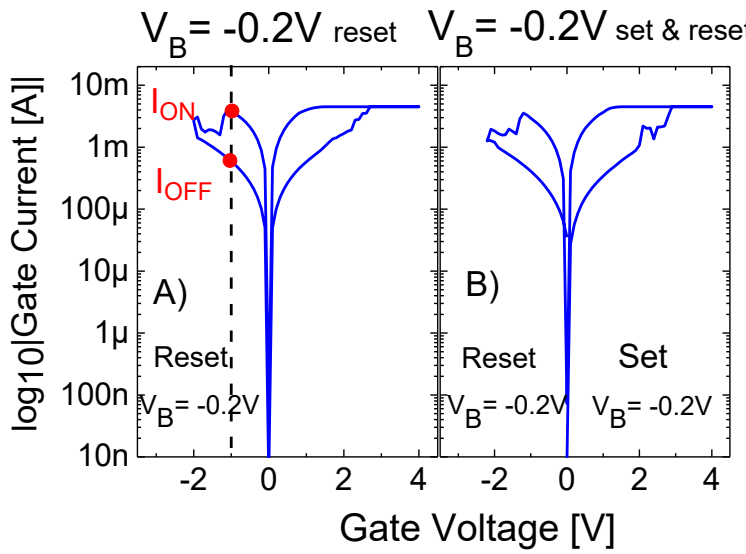


Figure 3.14. RS I_G/V_G average curves measured on the same sample when A) V_B= -0.2V for the reset process only (V_B=0 during the set), B) V_B= -0.2V during set and reset process.

3.4 Conclusions

In the first part of this chapter, RS phenomenon has been experimentally analyzed in N-type FDSOI Ω-gate NW-FETs with high-k dielectric. An initial attempt to know this type of samples and their electrical limitations was shown.

Another study conducted in this section was the conductive filaments located close to drain and source have been observed; one or the other may control the dielectric conductance, depending on the RS cycling. This means that there is no terminal that commands the RS cycles. Although two switchable conductive states can be observed in the MIS gate stack, the electrical conditions used to observe the RS produce severe damage on the transistor functionality.

In the second part of this chapter, the $I_D - V_D$ transistor curves, when the gate dielectric is at the high and low resistance states were presented. The results point out that the transistor performance can be partially recovered after the reset process, by applying appropriate RS voltages and current limit conditions. This demonstrates the feasibility of integrating a memristor and a transistor within a single device also with these FDSOI devices [45].

Finally, the back gate voltage influence on the device has been preliminary studied. When a negative back gate voltage is applied during set process the I_{ON}/I_{OFF} ratio increases, which could be related to the impact of the strong transversal electrical field. However, preliminary results indicate no significant effects of this bias on the I_{ON}/I_{OFF} ratio when it is applied during the reset process with $V_B \neq 0\,V$ or a complete RS cycle with $V_B \neq 0\,V$ in both set and reset processes. These differences need to be further addressed in future research.

4. Aging relaxation after TDV in 28nm TSMC array of ring oscillators

This chapter presents the results of experimental measurements conducted during a research-stage internship within the Device Reliability and Electrical (DRE) characterization group at the Interuniversity Microelectronics Center (IMEC) facilities. The final goal of this thesis is to move beyond device-level characterization and focus on circuit-level characterization and degradation analysis. This transition is important because understanding degradation at the circuit level better reflects the real operating conditions of consumer electronics. While device-level studies provide fundamental insights, only at the circuit level can one capture the cumulative effects of aging mechanisms on system performance and reliability.

In this chapter, first, the array of Ring Oscillators (ROs) employed in the experiments is described. Second, the circuit-level characterization setup used to perform the measurements is explained. Third, the methodology applied for electrical characterization is outlined. Finally, the experimental and simulated results are presented and discussed within the conclusions.

4.1 Samples description

The array of ROs used to perform the experiments presented in this chapter was designed at IMEC [83] and fabricated in Taiwan Semiconductor Manufacturing Company (TSMC). The chip, in its bare die state, is divided into six functional modules as depicted in Figure 4.1A. The experiments were developed with the array of ROs, i.e. the first module (red rectangle in Figure 4.1A). This element includes 24 pads; each individually connected to the RO array for the purposes of signal monitoring and characterization. The total pad dimensions are 140μm x 1035μm.

4.1.1 Array of ring oscillators

The array of ROs is depicted in Figure 4.1B. It is composed of 112 ROs classified in 4 rows and 28 columns (see Figure 4.1B). Each RO consists of 41 inverter stages and includes a NAND gate to control the feedback loop. It is integrated within a dedicated *unit cell* that houses the circuitry required to bias the RO. In addition, every unit cell contains a forward-biased diode functioning as a temperature sensor for on-chip thermal monitoring during testing. The activation of individual unit cells is enabled through a row-and-column selection mechanism. To minimize voltage drops during RO biasing, the array is also equipped with three on-chip Force-and-Sense (F&S) biasing lines. Between the unit cells, vertical strips connected in parallel are used for heating distribution as depicted in Figure 4.1 B [85].

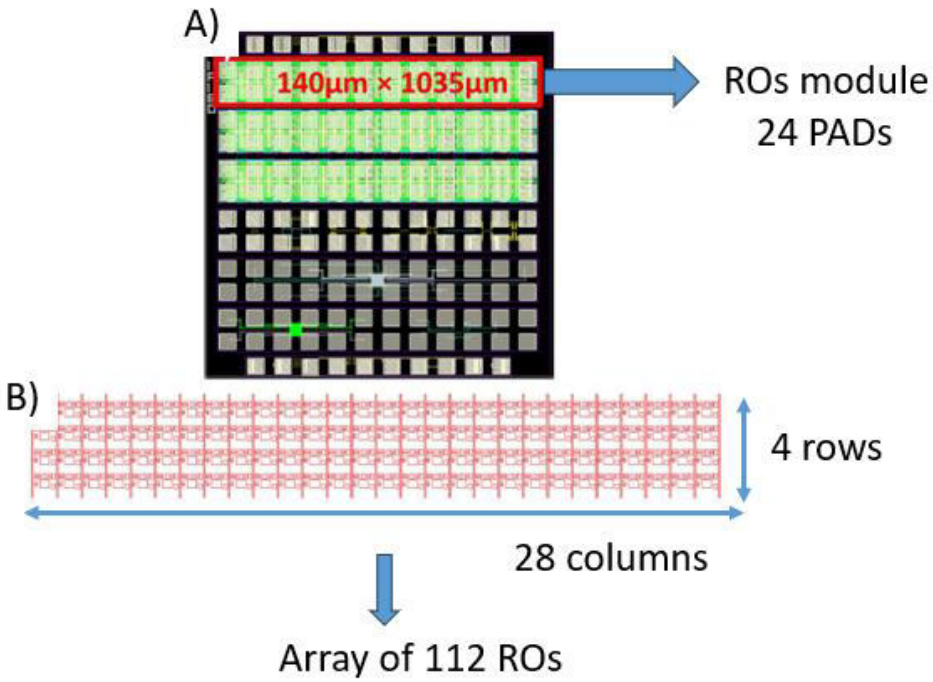


Figure 4.1. (A) Layout of the 24 pad(s) designed array of ROs. (B) Array of 112 ROs distributed in 4 rows and 28 columns [85].

4.2 Characterization setup

Setup for aging experiments at circuit level

The setup includes a probe station to ensure precise alignment and stability during measurements. Two Keithley 2600 SMUs were used to apply and monitor voltages and currents (see Figure 4.2). A debaser was connected to the SMUs to efficiently multiplex

the signals and was controlled via custom GPIB and Python software. A patch panel was incorporated to clearly label and organize signal routing, facilitating identification. This panel was integrated with the probe station to guide the signals toward the Device Under Test (DUT). The next stage of the setup consists of the probe card and the DUT. The probe card interfaces with the 24 multiplexed signals from the debaser and is equipped with 24 needles, each making direct contact with a corresponding pad of the RO module.

Another important component of the measurement setup is data acquisition. For this purpose, a frequency counter connected via GPIB was employed. This instrument captures the output frequency of the ROs through the chip's output pin.

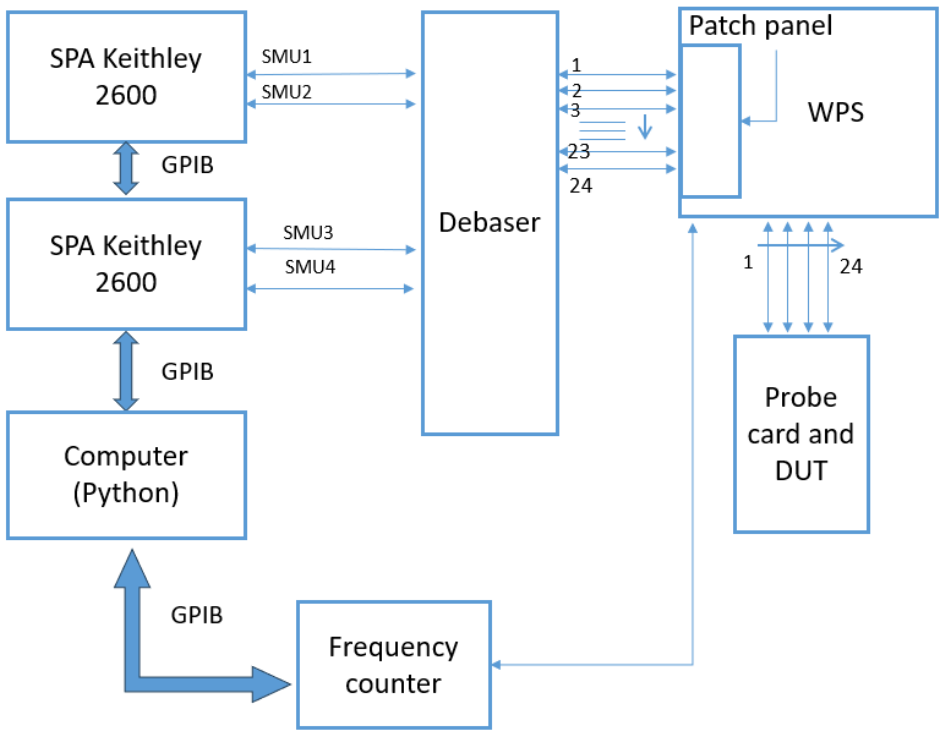


Figure 4.2. Setup used for the experiments at circuit level. This device under test (DUT) is contacted under the 24 needles of the probe card.

Figure 4.3 shows the labeling of each pad corresponding to a signal from the RO unit cell. These signals are electrically routed through the patch panel and subsequently connected to the debaser as represented in Figure 4.3.

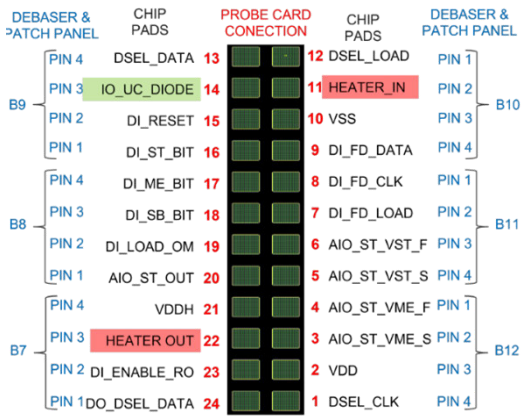


Figure 4.3. Connection from the chip pad(s) to the WPS patch panel and debaser.

Figure 4.4 A illustrates a representation of a probe card, this instrument helps to stablish contact between chip and signals from debaser. It features 24 needles and interfaces with the probe station's patch panel through 24 connections. In Figure 4.4 B, the semiconductor parameter analyzer (SPA), a Keithley 2600 is shown.

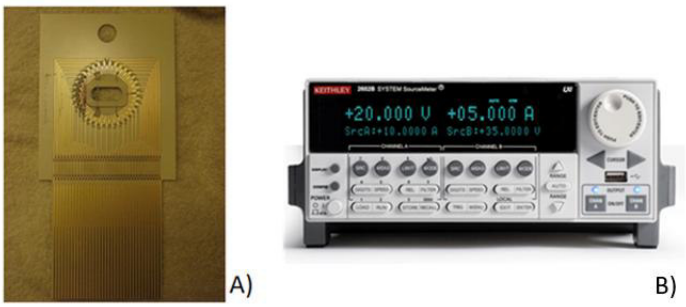


Figure 4.4. A) Schematic representation of the probe card used to establish contact between the module and the probe station. B) SPA Keithley 2600 instrument used during the electrical characterization experiments.

4.3 Measurement procedure

First, we will describe the dynamic and static stresses used in this chapter.

To clarify the concepts of dynamic and static stress, we refer to a ring oscillator loop in Figure 4.5. *Static* stress happens when the ring oscillator experiences only BTI aging in its components. In this scenario, the ring oscillator loop operates in an open mode (as illustrated in Figure 4.5), meaning the voltage across the transistors (V_G) remains

constant. In contrast, *dynamic* stress occurs when the oscillator loop is in closed mode (enable switch in Figure 4.5). During this state, the transistors are subjected to both AC-BTI and AC-HCI sequentially. The combination of these two aging mechanisms leads to additional degradation that components encounter during normal operation.

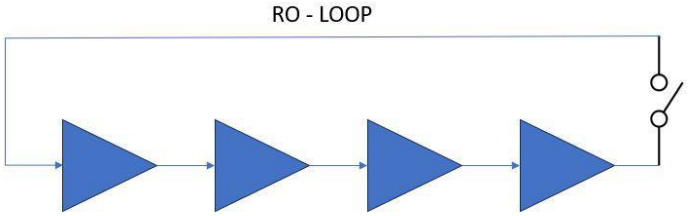


Figure 4.5. Ring oscillator's loop when it is open/close determines static/dynamic stress.

The measurement procedure is illustrated in Figure 4.6. First, the circuit is stressed at nominal voltage operation 0.9V to analyze TZV with the SPA Keithley 2600 (see Figure 4.6), then, the ring oscillator frequency is measured by a frequency counter FCA 3000.

Second, to perform TDV measurements, the device is stressed from 1.1V to 2.4V in dynamic stress (where AC-BTI and AC-HCI) take place and static stress (only BTI). The stress begins with 0.06s of stress time and increases as follows: (0.3s, 0.6s, 1s, 3s, 10s, 30s, 100s, 300s, 1000s, 3000s) and relaxation time $t_r = 100\ s$. After the stress phase, no voltage is applied, allowing the frequency counter to capture the relaxation behavior after aging. This step is important, as the post-stress relaxation of the ring oscillators will be further analyzed. To quantify the degradation experienced by the ring oscillators (ROs), the relative frequency degradation (Δf_r) is used as the metric.

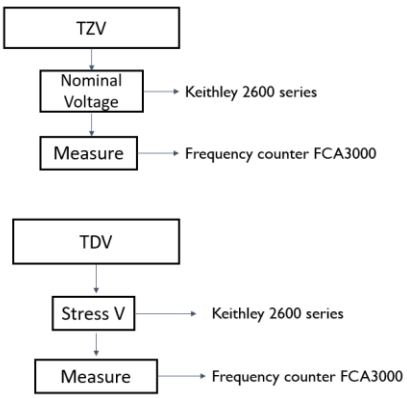


Figure 4.6. Aging and measurement procedure to evaluate TZV and TDV in array of ring oscillators.

4.4 Results and discussion

To obtain the relative variation of the frequency (Δf_r), the degraded frequency is divided into the initial frequency of a fresh sample as illustrated in equation 4.1

$$\Delta f_r = \frac{freq}{initial\ freq} \qquad 4.1$$

The experimental data have been adjusted to the equation 4.2 [84]. t_s/t_r are stress/relaxation times. B and β are given by the equation.

$$\Delta f_r = \frac{R_0(t_s)}{1 + B\left(\frac{t_r}{t_s}\right)^{\beta}} + p\,(t_s) \qquad 4.2$$

Figure 4.7 presents the frequency measurements obtained after applying 1.6 V of dynamic stress (AC-BTI + AC-HCI) over various time intervals. The data points are represented as dots. The stress was applied for durations of 3s, 10s, 30s, 100s, 300s, 1000s, and 3000s. Furthermore, the negative frequency variation ($-\Delta f_r$) as a function of relaxation time is depicted in the same figure.

In this figure, the purple dots, indicating approximately 0.75% initial frequency degradation, correspond to the measurements of the recovery observed after an initial stress duration of 0.3 seconds. In other words, the DUT was subjected to dynamic stress for 0.3 seconds prior to the measurement. The bottom blue continuous line represents the relative frequency variation as a function of relaxation time; it corresponds to the simulation result of the measurement points shown as purple dots. The continuous lines in Figure 4.7 show the fitness of the experimental data (colored dots) to the equation 4.2. The time was extrapolated from $1x10^{-12}$ seconds to $1x10^{12}$ of relaxation time.

The subsequent green dots, showing over 1% initial frequency degradation, reflect the recovery after 0.6 seconds of dynamic stress. The bottom orange continuous line, which is positioned above the 1% degradation mark, corresponds to the relative frequency variation as a function of relaxation time. As we analyze the subsequent stress durations, we notice that at longer stress times, the degradation increases (negatively) as illustrated in Figure 4.7 for a voltage of 1.6V of dynamic degradation.

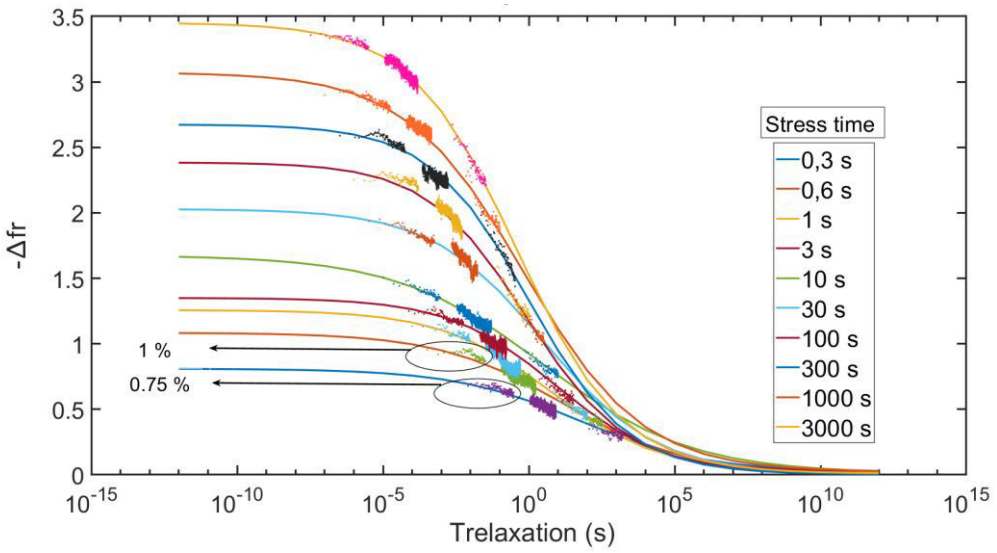


Figure 4.7. Negative frequency variation as a function of relaxation time of experimental data for a stress voltage of 1.6V at different stress times.

Since the frequency counter introduces a 100 µs measurement delay, it cannot record the frequency at zero relaxation time. Therefore, this chapter focuses on analyzing the degradation at that specific point ($t_r = 0$). To obtain the relative frequency variation at the beginning of relaxation time, equation 4.2 is evaluated in time of relaxation zero ($t_r = 0$), so it can be rewritten as:

$$\Delta f_r(t_r = 0) = R_0(t_s) + p\,(t_s) \qquad 4.3$$

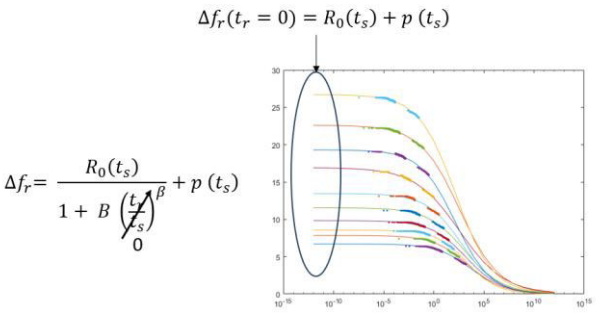


Figure 4.8. Representation of the relative frequency degradation measured at relaxation time zero for 2.4V stress voltage.

As a result, all the initial points of degradation (Figure 4.8), will represent the overall degradation in any stress voltage as depicted in Figure 4.9.

Relative frequency variation as a function of stress time is depicted in Figure 4.9. Each stress voltage tested corresponds to a line in the figure. As an example, 1V of stress (yellow triangles in Figure 4.9) corresponds with a yellow line that shows the smallest variation of the frequency. What can be inferred from Figure 4.9 is that at higher stress voltages (dynamic or static) correspond with higher degradations.

Comparing dynamic stresses with static stresses (Figure 4.9 LEFT and RIGHT), from 1.5V to 2.4V the percentage of degradation (at relaxation time zero) is very similar in the initial times for both stresses. As an example, in case of 2.4V of dynamic stress at 3000 seconds the percentage of degradation is ~22%. Moreover, in case of 2.4V of static stress at 3000 seconds the percentage of degradation ~21%. It means that the ring oscillator suffers from combined degradation of AC-HCI and AC-BTI (dynamic) higher than static degradation for larger times and voltages.

From 1V to 1.4V dynamic and static stress still follows a trend that at higher voltages and times the power law is still accomplished but, the measurements are not stable probable for noise induced data acquired by the equipment.

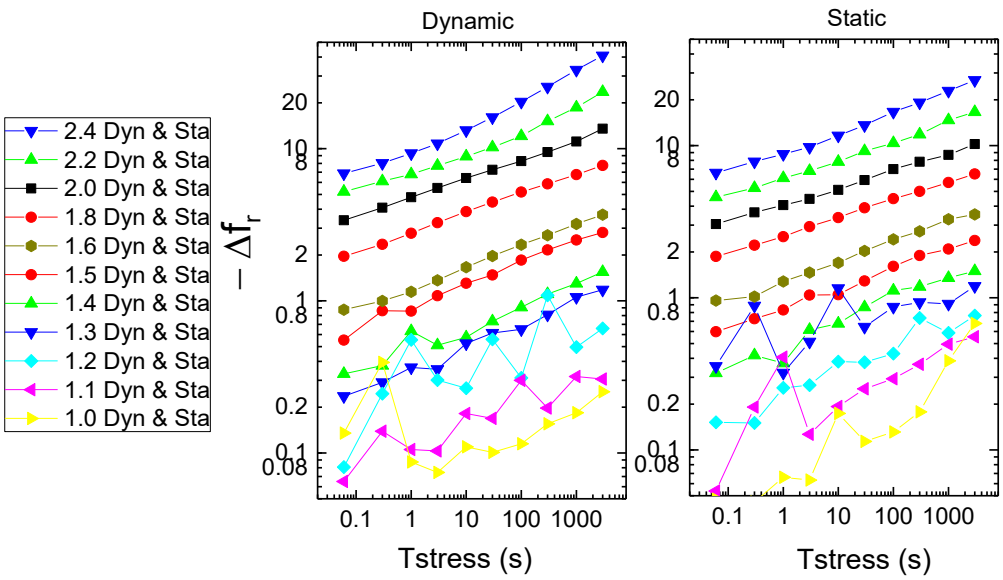


Figure 4.9. Relative frequency variation as a function of total stress time, for relaxation time zero, from 1V to 2.4V of Dynamic (LEFT) and static (RIGHT) stresses.

The tendency in Figure 4.9 will be represented in the next power equation:

$$\Delta f_r(t_r = 0) = a * (t_s)^b \qquad 4.4$$

The fitting parameters *a* and *b* provide insight into the behavior of the degradation model under different stress conditions. In Figure 4.10 (left), the dependence of coefficient *a* on the applied stress voltage is illustrated for both dynamic and static stresses, this comparison explains how this parameter evolves with increasing voltage levels. On the right side of the figure (Figure 4.10, right), coefficient *b* is also examined, allowing for a direct comparison between dynamic and static stress modes as a function of voltage.

In Figure 4.10 left the coefficient *a* remains relatively consistent under both dynamic and static stress conditions. As the voltage increases, the influence of this factor becomes more significant. Turning to Figure 4.10 right, we focus on the coefficient *b*. In this part, there is a clear difference of coefficient *b* between static and dynamic stresses. The coefficient *b* under dynamic stress (black squares in Figure 4.10 right) is greater than its counterpart under static stress (red circles in Figure 4.10, right). Consequently, this behavior may be attributed to the combined effects of HCI and BTI under dynamic stress conditions.

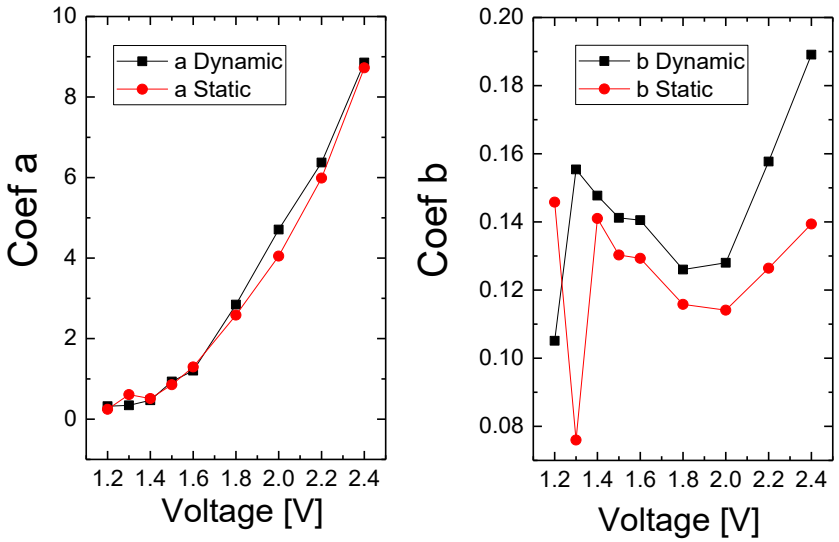


Figure 4.10. LEFT: Coefficient *'a'* in black dynamic stress in red static stress. RIGHT: Coefficient *'b'* in black dynamic stress and static stress from 1.2V to 2.4V.

4.5 Conclusions

In this chapter, the analysis of the degradation and recovery after dynamic and static aging in an array of ring oscillators is shown. This work was part of the activities in the research stage at IMEC facilities. With these results we can conclude:

The negative frequency degradation increases as the dynamic/static stresses time increases, indicating a cumulative effect on the system's degradation. Speaking about recovery trends, a partial frequency recovery is observed after each stress period,

suggesting that the system has some capacity to recover the initial RO operation frequency.

The relative frequency variation is extracted when relaxation time is zero, for both dynamic and static stress conditions, showing a clear dependence on voltage and stress times. The overall degradation follows a power law, meaning that higher voltages and longer stress times lead to greater degradation. This trend is evident in both dynamic and static stress conditions.

When comparing static and dynamic stress at 2.4V with 3000 seconds, dynamic stress results in approximately 22% degradation, while static stress results in around 21%. This indicates that the RO experiences greater degradation under dynamic stress. The coefficient *a* remains relatively stable for both dynamic and static stresses. On the other hand, coefficient *b* shows a clear difference between dynamic and static aging stresses. The contribution of dynamic stresses is greater than static, which may be attributed due to the combined effects of AC-BTI and AC-HCI in dynamic stress

Summary and Conclusions

Electronics has become an important part of our society, consumer electronics and its applications in devices such as tablets, smartphones, electronics for IoT applications and the evolution of the cyber physical systems require always more complex systems. One factor for the evolution of this systems are the miniaturization that allow to build more complex structures, the evolution of new materials and new architectures.

One the other hand, more than Moore devices look promising candidates to continue the scaling and Moore's Law prediction. Reliability studies become increasingly important to understand their possible sources of variability. This thesis is focused on this topic, the evaluation of the Time Zero Variability TZV and Time Dependent Variability TDV in High-k transistors. The core of this thesis is to evaluate the different sources of this variabilities such as Bias Temperature Instabilities, Hot Carrier Injection and Off-state stress, as well as Resistive Switching understood as a Reversible Dielectric Breakdown.

We have developed the setup to perform experiments that test aging mechanisms with their impact in the device and circuit characteristics. In particular, this mechanisms were applied on this FD-SOI omega shaped High-K nanowires and an array of ring oscillators. A model of relaxation in time was also probed, with the goal of find the degradation at zero relaxation times.

In chapter 1, a short introduction of basic notion necessary to understand this thesis are presented.

Variability sources such as: BTI, HCI, and Off-state stress are experimentally analyzed in FD-SOI Ω-gate transistors in Chapter 2. After the experiments with the same electrical conditions these aging mechanisms were compared. For these experiments, to evaluate degradation after aging, I_{D-ON} was used as a parameter for this purpose. In case of NBTI and PBTI, the smallest degradation is shown in comparison to HCI which presents the highest I_{D-ON} diference together with an increase of threshold voltage and decrease of mobility. In the case of the Off-state stress the I_{D-ON} degradation is still higher than N/PBTI. In addition, when subjecting at higher voltage conditions and higher times Off-state degradation shows a significant I_{D-OFF} in subthreshold regions. This results, suggest a large distortion in transistors characteristics that affect device functionality.

The experimental study of resistive switching in N-type FDSOI Ω-gate NW-FETs with high-k dielectric is presented in Chapter 3. On the one hand, as a first approximation, an attempt to understand the electrical limitations of the samples is presented. With the use of transistors currents to observe the change in the drain/source currents after RS, the conductive filament close to this terminals have been observed. Either drain filament or source filament could influence the dielectric conductance, depending on the RS cycling. As an attempt to find a device that could combine transistor and memristor capabilities,

$I_D - V_D$ characteristics were measured during RS. The electrical conditions produce severe damage on transistors functionality at the first part of the study.

However, we investigate the electrical conditions to recover the transistors characteristics during RS. Thus, the transistor's $I_D - V_D$ can be partially recovered by applying appropriate RS voltages and current limits. This demonstrates the possibility to integrate in the same device a transistor and a memristor in this FD-SOI quasi-planar transistors. Additionally, transistor's back gate voltage influence on resistive switching was also studied. The experiments suggested that when negative back gate voltage was applied during set process ($V_B = 0\ V$ during reset process) I_{ON}/I_{OFF} ratio increases. This could be related to strong electric field that dielectric suffers. Nevertheless, preliminary results suggest that there is no important influence of back gate voltage on I_{ON}/I_{OFF} ratio when this bias is applied during reset process ($V_B = 0\ V$ during set process), or neither when it is applied during a complete RS cycle i.e. set and reset.

In Chapter 4, the results obtained during the research stage at IMEC facilities are presented. The analysis focuses on relative variation of frequency degradation during recovery after the stress application, specifically in an array of 112 ring oscillators. A model was applied to predict the transistors' recovery at recovery time zero, as well as, after an extended recovery period. The findings include a comparison between dynamic and static stress conditions. A clear dependency on voltage and time is observed, indicating that higher voltages and longer durations of stresses, lead to an increase of relative frequency degradation (decrease of ring oscillator frequency). The results also suggest, that dynamic stress causes slightly higher degradation than static stress. This could be interpreted as the combined contribution of dynamic stress (AC-HCI+AC-BTI).

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Articles in the Ph.D. thesis

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Comparison of OFF-State, HCI and BTI degradation in FDSOI Ω-gate NW-FETs

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ABSTRACT

In this work, the degradation of N-type FDSOI Ω-gate NW-FETs caused by OFF-State stress under different conditions has been experimentally studied and compared with the effects of positive/negative BTI and HCI aging. The experimental observations show that HCI and OFF-State are the most damaging aging mechanisms in these devices while N/PBTI produce negligible degradation. Moreover, for large enough stress conditions, OFF-State aging largely distorts the I_D-V_G curves of the transistor, leading to an almost linear dependence on V_G.

1. Introduction

Device degradation caused by Bias Temperature Instability (BTI) or Hot Carrier Injection (HCI) is still relevant in deeply scaled CMOS technologies [1–6]. The changes introduced into the dielectric and/or channel properties reduce the device reliability and, therefore, the circuit performance and lifetime [7]. In the last years, the interest in the degradation induced by an OFF-state stress has grown and reported [8–10], showing the importance of accounting for the diverse biasing configurations that FETs may experience when they operate in digital circuits such as CMOS inverters or logic gates [11–13]. In this work, the impact of the OFF-state degradation in short channel FDSOI transistors (Fully-Depleted Silicon On Insulator) N-type FDSOI Ω-gate Nanowire transistors (NW-FETs) [14] under different stress bias conditions is studied. Moreover, the impact of negative/positive BTI and HCI degradations are also experimentally studied and compared to that linked to the OFF-state degradation. Finally, the OFF-state ON and OFF Drain Current degradation dependence on the stress voltage and stress time were analyzed.

2. Device description and measurement procedure

The FDSOI N-type Ω-gate NW-FETs studied in this work were fabricated at CEA-LETI [14] and had a high-K Ω-Gate (HfSiON/TiN) with EOT = 1.3 nm, H_{NW} = 11 nm and a buried oxide thickness of 145 nm (Fig. 1). Devices were fabricated using a multi-finger structure, with W = 300 nm splitted in 10 fingers and had L = 20 nm.

To analyze the impact of the N/PBTI, HCI and the OFF-State degradations, different experiments were carried out. For BTI, both biasing, negative and positive, were analyzed applying the stress voltage (2.4Volts) to the gate terminal while source, drain and back-gate terminals were grounded (as shown in Fig. 2). For HCI, the worst case was considered (i.e., $V_G = V_D$), so that the stress voltage (2.4Volts) was applied to the gate and drain terminals, while source and back gate were grounded. For OFF-State, the stress voltage was applied to the drain terminal, keeping the rest of terminals grounded. In this case, the stress voltage was varied from 1.7 V to 2.5 V. A Measurement-Stress-Measurement sequence was used, so that the stress sequence was interrupted to evaluate the stress impact and its time evolution by measuring the I_D-V_G curves of the stressed devices.

3. Results and discussion

Fig. 3 shows the I_D-V_G curves of fresh devices (black line) and after 1500 s (red circles) of (from left to right) OFF-State, NBTI, PBTI and HCI stress at 2.4Volts in linear scale (top) and log scale (bottom). For the fresh devices short channel effects are evidenced by the large drain current (I_D) in the subthreshold region and the small threshold voltage (~0.25 V). For the PBTI and NBTI stresses, no significant changes on the I_D-V_G curves can be appreciated beyond a small reduction of $I_{D\text{-}ON}$

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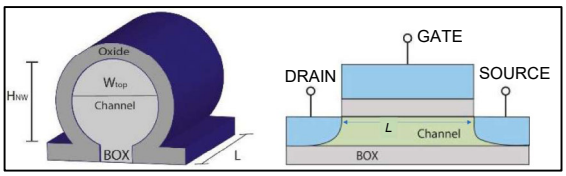

Fig. 1. LEFT: 3D sckecht of the Ω-Gate architecture of the FD-SOI transistors (EOT = 1.3 nm, H_{NW} = 11 nm and Buried Oxide Thickness = 145 nm). RIGHT: Cross-section of the FD-SOI transistors.

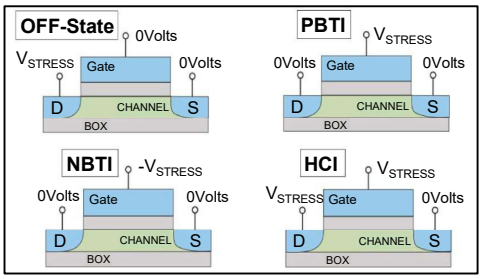

Fig. 2. Biasing configurations for the study of the OFF-State, PBTI, NBTI and HCI degradations. The back-gate was always grounded.

(current at V_G = 1.2 V). However, for HCI and OFF-State the consequences of the stress are clearly observed. For the HCI, there is a large increase of the threshold voltage (~1V) and the mobility is strongly reduced. Therefore, the damage that $I_{D\text{-}ON}$ experiences (~90% reduction) is so detrimental (the largest, when compared to the other stress cases). Note that, though the I_D-V_G characteristic is extremely modified, the subthreshold and linear regions are still distinguishable. In the case of the OFF-State stress, for this stress voltage, the changes in the curves are much dramatic. As in the case of the HCI stress $I_{D\text{-}ON}$ is large reduced, but the decrease is smaller (~50%). However, the subthreshold current increases significantly and the I_D-V_G characteristic is completely distorted being not possible to clearly identify the subthreshold region: I_D exhibits an almost linear dependence on V_G for large stress voltages (see Fig. 5).

Because the large I_D-V_G distortion caused by the OFF-State degradation, threshold voltage and mobility are not useful parameters to quantify the device degradation. Therefore, $I_{D\text{-}OFF}$ (i.e., I_D @ V_G = 0 V) and I_{ON} (i.e I_D @ V_G = 1.2 V) were used as parameters with this purpose. Fig. 4 shows the relative $I_{D\text{-}ON}$ and $I_{D\text{-}OFF}$ reduction suffered after OFF-State (blue triangles), PBTI (black squares), NBTI (red circles) and HCI (pink triangles) stresses. As observed in Fig. 3, Negative and Positive BTI produce the smallest variations on $I_{D\text{-}ON}$ (<7% after 2000 s). On the other hand, HCI provokes the largest reduction of $I_{D\text{-}ON}$, mostly induced within the first 100 s of the stress, indicating that, in this technology, HCI is extremely harmful. Finally, for the OFF-State stress, $I_{D\text{-}ON}$ shift suffers a fast increase at the beginning of the stress and then evolves smoothly with the stress time from ~ 20% (after the first inspection at 80 s) to ~ 50% after 2500 s, also exhibiting a saturation effect for larger stress times. Concerning $I_{D\text{-}OFF}$, there is no change for N/PBTI, a large reduction for the HCI (~100%), but a large increase for the OFF-State case (~1000%, i.e., 10 times with respect the fresh $I_{D\text{-}OFF}$).

The stress voltage dependence of the OFF-State degradation has been also analyzed. Fig. 5 shows some examples of the I_D-V_G curves measured after 2600 s of stress for different stress voltages together with the fresh I_D-V_G. Note that $I_{D\text{-}ON}$ decreases respect of the fresh value being larger with the stress voltage applied during the OFF-State stress. On the other hand, $I_{D\text{-}OFF}$ and the subthreshold slope increases with the stress voltage being critical for the largest stress voltages (>2.3 V). However, the observed $I_{D\text{-}OFF}$ degradation is very small for the lower stress voltages (1.7 V to 2 V). The combination of both degradations, $I_{D\text{-}ON}/I_{D\text{-}OFF}$ increase/decrease, extremely distorts the I_D-V_G characteristic, as

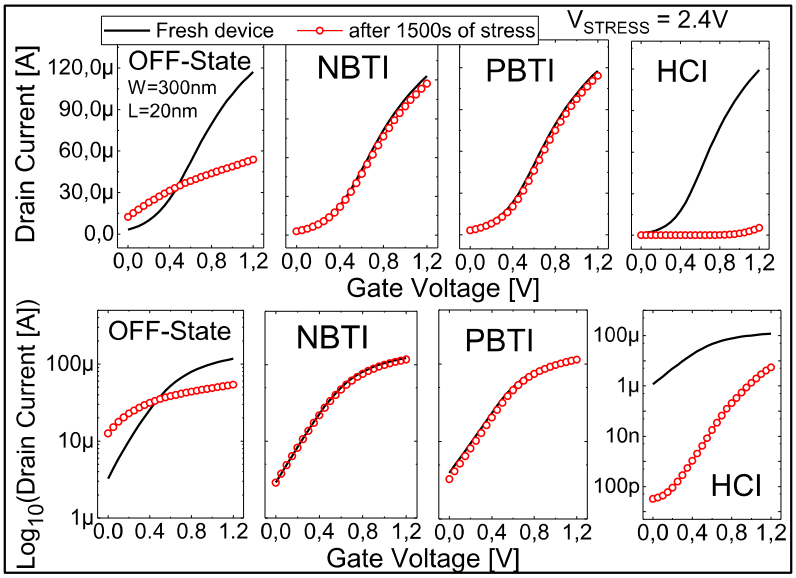

Fig. 3. I_D-V_G curves (V_{DS} = 50 mV) of the fresh device (black line) and after 1500 s of 2.4 V stress (red circles). Linear (top) and logarithmic (bottom) plots are shown.

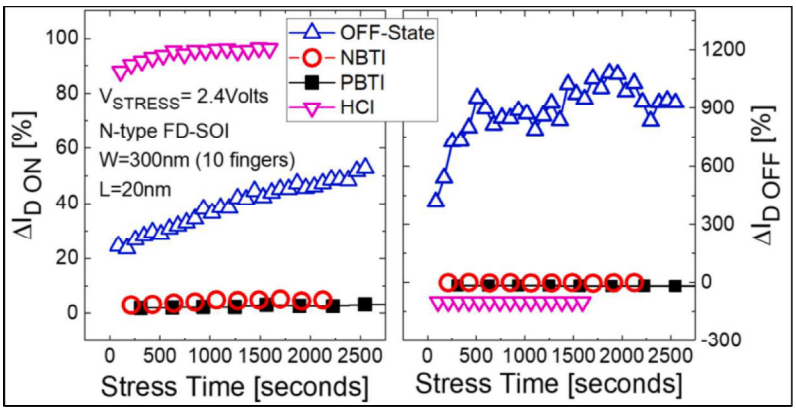

Fig. 4. Relative $I_{D\text{-}ON}$ (left) and $I_{D\text{-}OFF}$ (right) variations for an OFF-State (blue triangles), PBTI (black squares), NBTI (red circles) and HCI (pink triangles) stresses at 2.4 V, as a function of the stress time.

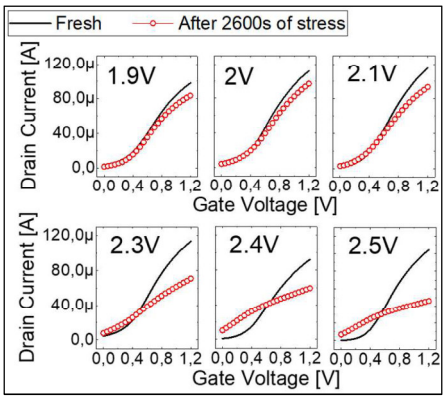

Fig. 5. I_D-V_G curves (V_{DS} = 50 mV) of the fresh device (black line) and after 2600 s of OFF-State stress (red circles) at 1.9 V, 2 V, 2.1 V, 2.3 V, 2.4 V and 2.5 V.

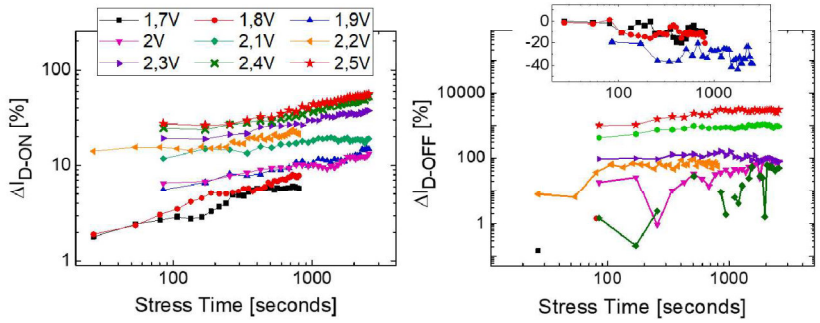

Fig. 6. Relative variations of $I_{D\text{-}ON}$ (top) and $I_{D\text{-}OFF}$ (bottom) as a function of the stress time for OFF-State stresses at V_G ranging from 1.7 V to 2.5 V.

previously highlighted in Fig. 3.

The temporal evolution, together with the voltage dependences, are further analyzed in Fig. 6. For $I_{D\text{-}ON}$, as expected, the larger the stress conditions (voltage and time), the larger the $I_{D\text{-}ON}$ degradation, reaching a 60% reduction after 2600 s at 2.5 V. On the other hand, for $I_{D\text{-}OFF}$, only for large enough stress voltages/times, an increase is observed. However, $I_{D\text{-}OFF}$ is 30 times the fresh value, for the stress at 2.5 V.

4. Conclusions

The degradation of N-type FDSOI Ω-gate NW-FETs induced by PBTI, NBTI, HCI and OFF-State stress was experimentally analyzed and compared. NBTI/PBTI have the smallest effect on the device performance, whereas HCI produces the largest $I_{D\text{-}ON}$ degradation, linked to a large increase/decrease of V_{TH}/μ. However, though the OFF-State stress induces a decrease of $I_{D\text{-}ON}$ smaller than for HCI, for large enough stress

conditions (voltage/time), the large increase of the subthreshold current can lead to a complete distortion of the I_D-V_G characteristics and even to the loss of the device functionality. Furthermore, in both cases (HCI and OFF-State) the gate dielectric experiences a large degradation during the stress leading to large tunneling currents through the high-k based Ω-gate.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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ABSTRACT

In this work, the degradation of N-type FDSOI Ω-gate NW-FETs caused by OFF-State stress under different conditions has been experimentally studied and compared with the effects of positive/negative BTI and HCI aging. The experimental observations show that, in these devices, HCI and OFF-State are the most damaging aging mechanisms while N/PBTI stresses produce negligible degradation. Moreover, for large enough stress conditions, OFF-State aging introduces large leakage currents, largely distorting the I_D-V_G curves of the transistor.

1. Introduction

Device degradation caused by Bias Temperature Instabilities (BTI) or Hot Carrier Injection (HCI) is still relevant in deeply scaled CMOS technologies [1–6]. The changes introduced into the dielectric bulk and/or dielectric/channel interface (detected as an increase of the threshold voltage and/or decrease of carriers' mobility) reduce the device reliability and, therefore, the circuit performance and lifetime [7]. In the last years, the interest in the degradation induced by an OFF-state stress (which may appear during device operation in circuits) has grown [8–10] and the importance of accounting for the diverse biasing configurations that FETs may experience when they operate in digital circuits such as CMOS inverters or logic gates has been demonstrated [11–14]. In this work, the impact of the OFF-state degradation in short channel Fully-Depleted Silicon On Insulator (FDSOI) N-type Ω-gate Nanowire transistors (NW-FETs) [15] under different stress bias conditions is analysed. The dependence on the stress voltage of the ON and OFF Drain Current shifts induced by OFF-State stresses is also analysed. The effects of negative/positive BTI and HCI degradations are also experimentally studied and compared to that of the OFF-state stress. Moreover, the variations of the Drain, Source, BackGate and Gate currents during and after the stress are compared, as a means to evaluate in more detail the effects on the device electrical properties of each of the aging mechanisms.

2. Device description and measurement procedure

The FDSOI N-type Ω-gate NW-FETs studied in this work were fabricated at CEA-LETI [15] and had a high-K Ω-Gate (HfSiON/TiN) with EOT = 1.3 nm, H_{NW} = 11 nm and a buried oxide thickness (BOX) of 145 nm (Fig. 1). Devices were fabricated using a multi-finger structure, with W = 300 nm split in 10 fingers, and L = 20 nm.

To analyse the impact of the N/PBTI, HCI and the OFF-State degradations, different experiments were carried out. For BTI, both negative and positive biasing were analysed when a stress voltage (absolute value of 2.4Volts) to the Gate terminal was applied, while Source, Drain and BackGate terminals were grounded (as shown in Fig. 2). For HCI, the worst stress case for these short channel devices was considered (i.e., $V_G = V_D$), so that the stress voltage (2.4Volts) was applied to the Gate and Drain terminals, while Source and BackGate were grounded. For OFF-State tests, the stress voltage was applied to the Drain terminal, keeping the rest of electrodes grounded. In this case, the stress voltage was varied from 1.7 V to 2.5 V to analyse the voltage dependence of the OFF-state degradation. Note that the biasing during the different stresses lead to different electric fields and currents in the devices, as schematically depicted in Fig. 2. During BTI stresses, the electric field in the device is

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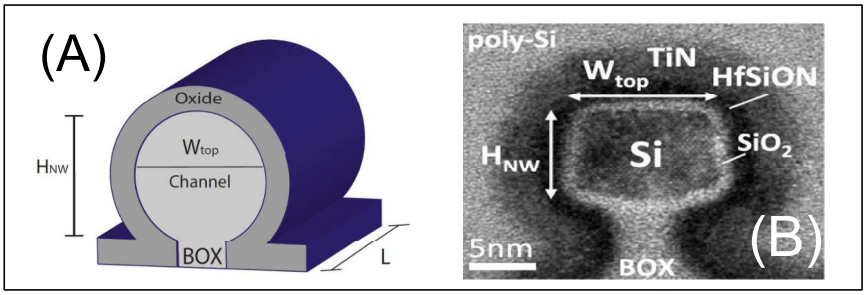

Fig. 1. (A) 3D sketch of the Ω-Gate architecture of the FD-SOI transistors (EOT = 1.3 nm, H_{NW} = 11 nm and Buried Oxide Thickness = 145 nm). (B) SEM image of the Cross-section of the FD-SOI transistors [15].

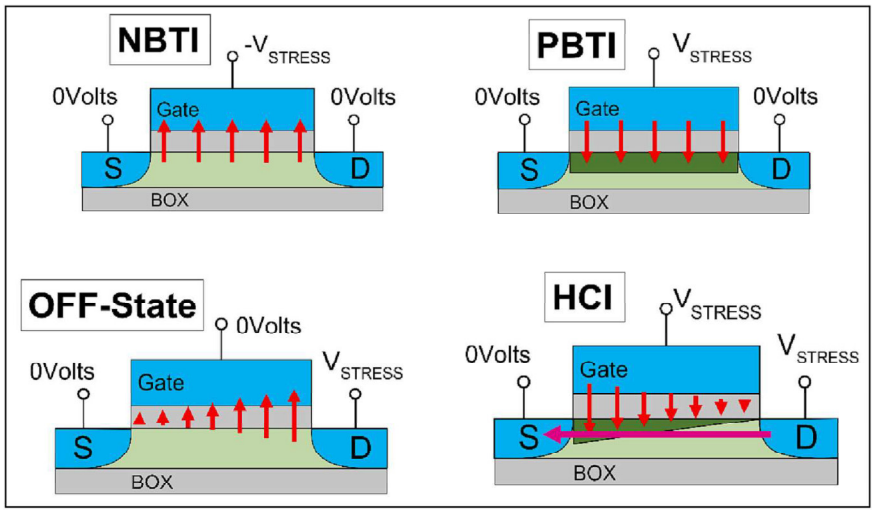

Fig. 2. Biasing configurations for the study of the device aging during OFF-State, PBTI, NBTI and HCI stresses. The BackGate was always grounded. Vertical red arrows schematically indicate the sign and magnitude of the electric field applied to the dielectric. The inversion channel created during PBTI and HCI tests is depicted in green. The large channel current that can flows during the HCI stresses is represented by the purple arrow from Drain to Source. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

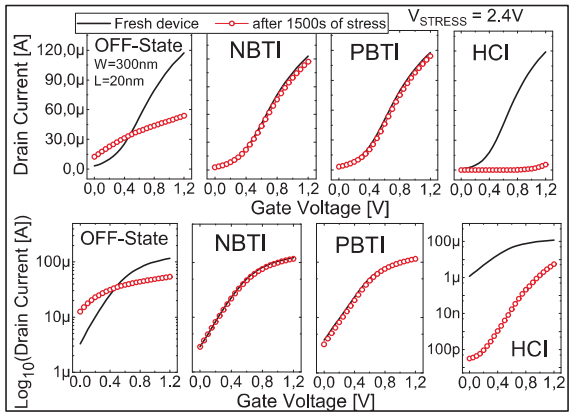

Fig. 3. I_D-V_G curves (V_{DS} = 50 mV) of the fresh device (black line) and after 1500 s of 2.4 V stress (red circles). Linear (top) and logarithmic (bottom) plots are shown. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

uniform along the channel, though a clear asymmetry exists during OFF-state and HCI tests. Moreover, an inversion channel has been created during PBTI and HCI tests. Finally, large ON currents can flow through the channel during the HCI stresses.

A Measurement-Stress-Measurement (MSM) test scheme was used, so that the stress sequence was interrupted periodically to evaluate the stress impact and the time evolution of the degradation. The currents through all the device terminals were measured during the stress and measurements phases.

3. Results and discussion

Fig. 3 shows the I_D-V_G curves (measured at V_{DS} = 50nmV) of the fresh devices (black line) and after 1500 s (red circles) of (from left to right) OFF-State, NBTI, PBTI and HCI stress at 2.4 V in linear scale (top) and log scale (bottom). For the fresh devices, short channel effects are evidenced by the large Drain current (I_D) in the subthreshold region and the small threshold voltage (~0.25 V). Regarding the PBTI and NBTI stresses, no significant changes on the I_D-V_G curves can be appreciated after the stress beyond a small reduction of $I_{D\text{-}ON}$ (i.e., current at V_G = 1.2 V). However, for HCI and OFF-State tests, the consequences of the stress are clearly observed. For HCI stress, there is a large increase of the threshold voltage (~1 V) and the mobility is strongly reduced. Therefore, the damage that $I_{D\text{-}ON}$ experiences (~90% reduction) is very detrimental (the largest, when compared to the other stress cases). Note that, though the I_D-V_G characteristic is largely modified, the

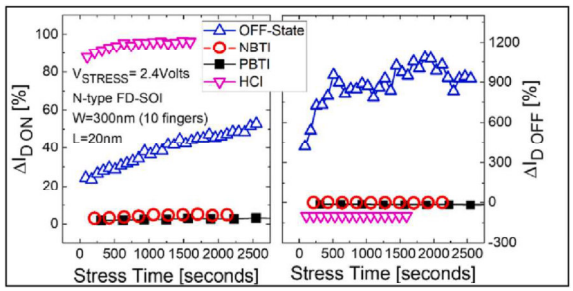

Fig. 4. Absolute value of the relative $I_{D\text{-}ON}$ (left) and $I_{D\text{-}OFF}$ (right) variations for an OFF-State (blue triangles), PBTI (black squares), NBTI (red circles) and HCI (pink triangles) stress at 2.4 V, as a function of the stress time. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

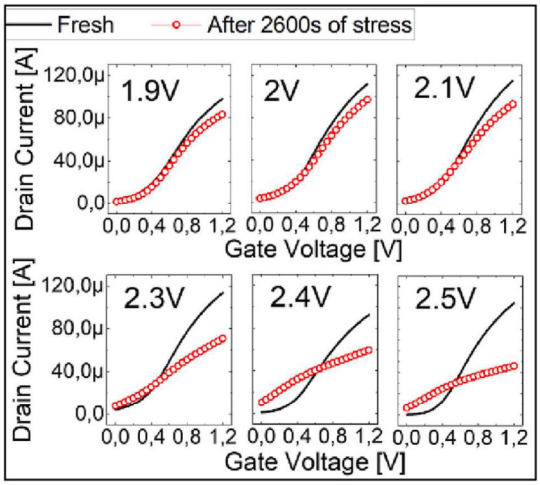

Fig. 5. I_D-V_G curves (V_{DS} = 50 mV) of the fresh device (black line) and after 2600 s of OFF-State stress (red circles) at 1.9 V, 2 V, 2.1 V, 2.3 V, 2.4 V and 2.5 V. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

subthreshold and linear regions are still distinguishable. In the case of the OFF-State stress, for this stress voltage, the changes in the curves are much dramatic. As for the HCI stress, $I_{D\text{-}ON}$ is strongly reduced, though the decrease is smaller (~50%). However, in this case the subthreshold current increases significantly and the I_D-V_G characteristic is completely distorted, being not possible to clearly identify the subthreshold region. I_D exhibits an almost linear dependence on V_G for large stress voltages (see Fig. 5), what means a large degradation of the device performance.

A more detailed comparison of the impact of the different kinds of stresses on the device properties has been done. Because of the large I_D-V_G distortion caused by the OFF-State stress, threshold voltage and mobility are not useful parameters to quantify the device degradation. Therefore, $I_{D\text{-}OFF}$ (i.e., I_D @ V_G = 0 V) and $I_{D\text{-}ON}$ (i.e I_D @ V_G = 1.2 V) were used as parameters with this purpose. Fig. 4 shows the relative $I_{D\text{-}ON}$ and $I_{D\text{-}OFF}$ reduction suffered after OFF-State (blue triangles), PBTI (black squares), NBTI (red circles) and HCI (pink triangles) stresses as a function of the stress time. As observed in Fig. 3, Negative and Positive BTI produce the smallest variations on $I_{D\text{-}ON}$ (<7% after 2000 s). On the other hand, HCI provokes the largest reduction of $I_{D\text{-}ON}$, mostly induced within the first 100 s of the stress, indicating that, in this technology, HCI is extremely harmful. Finally, for the OFF-State stress, $I_{D\text{-}ON}$ shift suffers a fast increase at the beginning of the stress and then evolves smoothly with the stress time from ~20% (after the first inspection at 80 s) to ~50% after 2500 s, also exhibiting a saturation effect for larger stress times. Concerning $I_{D\text{-}OFF}$, there is no change for N/PBTI and it largely decreases for the HCI stresses (~100%), but a huge increase is observed for the OFF-State case (~1000%, i.e., 10 times with respect the fresh $I_{D\text{-}OFF}$).

To get more insight into the OFF-state aging mechanism, its voltage and time dependences have been evaluated. Fig. 5 shows some examples of the I_D-V_G curves measured after 2600 s of stress for different stress voltages together with the fresh I_D-V_G curves. Note that, for all the stress voltages, $I_{D\text{-}ON}$ decreases with respect to the fresh value, measuring larger reductions for larger stress voltages. On the other hand, $I_{D\text{-}OFF}$ and the subthreshold slope increases with the stress voltage, though the observed $I_{D\text{-}OFF}$ degradation is very small for the lowest stress voltages (1.7 V to 2 V). These changes are critical for the largest stress voltages (>2.3 V), since the combination of both degradations, $I_{D\text{-}ON}$ decrease and $I_{D\text{-}OFF}$ increase, extremely distorts the I_D-V_G characteristic, as previously highlighted in Fig. 3.

The temporal evolution of $I_{D\text{-}ON}$ and $I_{D\text{-}OFF}$ variations, together with the voltage dependences, for the case of the OFF-State degradation are analysed in Fig. 6. For $I_{D\text{-}ON}$ (left), as expected, the larger the stress conditions (voltage and time), the larger the $I_{D\text{-}ON}$ degradation, reaching a 60% reduction after 2600 s at 2.5 V. On the other hand, for $I_{D\text{-}OFF}$ (right), only for large enough stress voltages (~2V), an increase of this parameter is observed. For the lowest stress voltages, $I_{D\text{-}OFF}$ decreases with the stress time, as can be seen in the inset of Fig. 6 (right), reaching a ~40% reduction for 1.9 V at the end of the test. However, $I_{D\text{-}OFF}$ is 30 times the fresh value, for the stress at 2.5 V. All these results indicate that the OFF-state stress modifies the subthreshold and ON operation regions

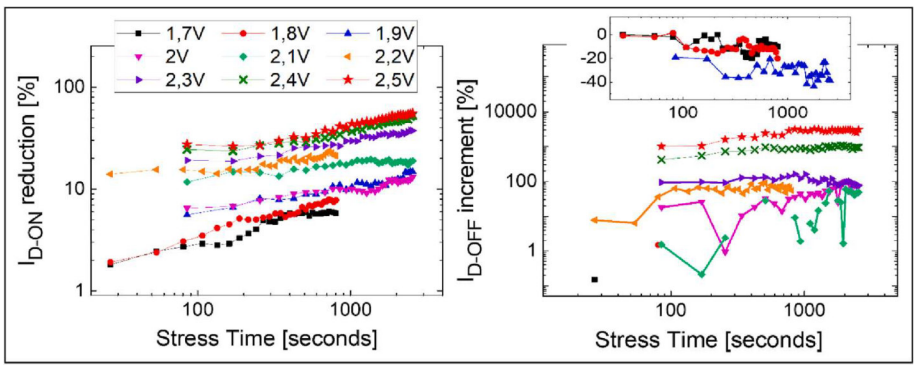

Fig. 6. Relative $I_{D\text{-}ON}$ reduction (left) and $I_{D\text{-}OFF}$ increment (right) as a function of the stress time for OFF-State stresses at V_D ranging from 1.7 V to 2.5 V.

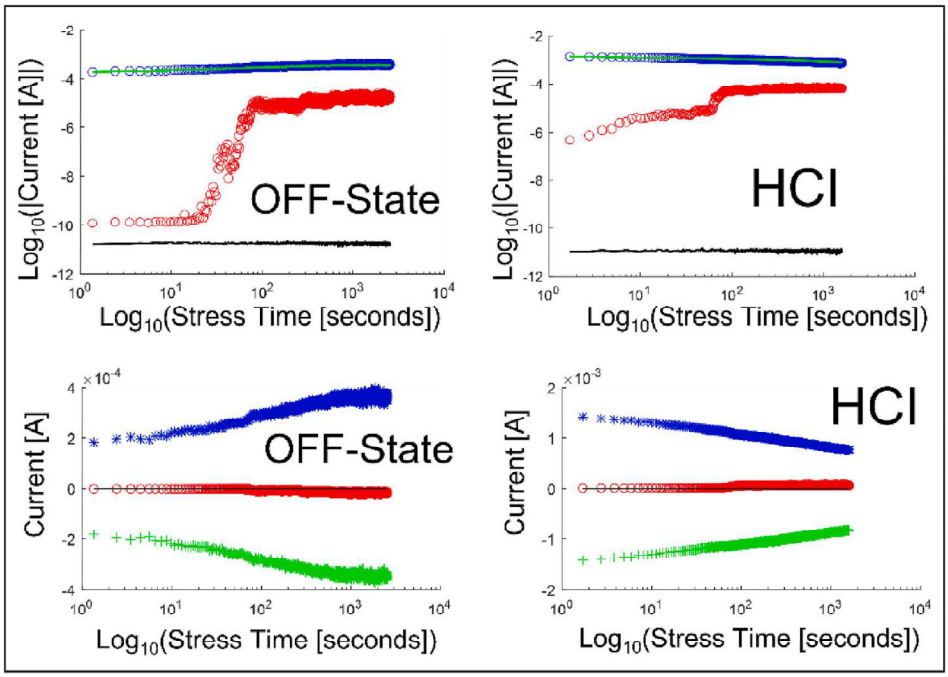

Fig. 7. I_D (blue), I_G (red), I_S (green) and I_{BG} (Black) currents registered during the stress phase of the OFF-State (left) and HCI (right) tests at 2.4 V. Top figures show the absolute value of the currents in a log scale; bottom figures those currents in linear scale (with their sign). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

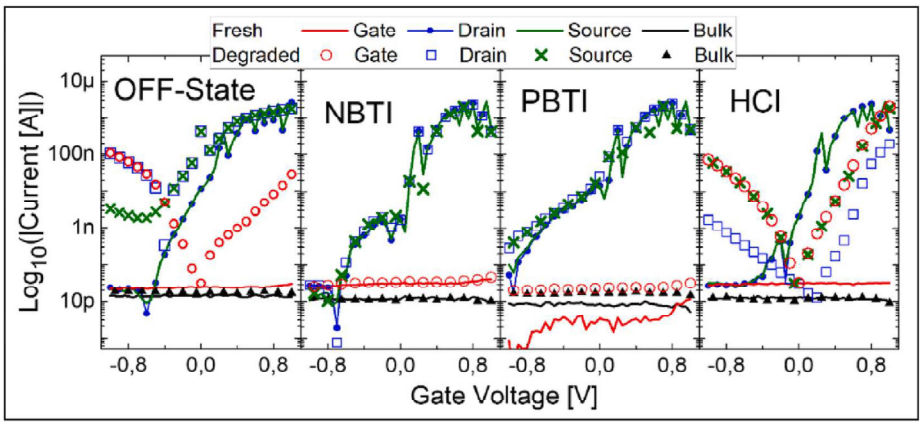

Fig. 8. I_D (blue), I_G (red), I_S (green) and I_{BG} (Black) currents registered during a V_G sweep (with $V_{DS} = 0$ V) for the fresh (lines) and stressed (symbols) devices after 1500 s and 2.4 V OFF-State, NBTI, PBTI and HCI stresses (from left to right). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

of the device, by increasing the leakage current through the channel and reducing the ON current, largely affecting the device performance, as observed in Fig. 5.

For a better understanding of the effects of each of the aging mechanisms, the currents through the four terminals of the device (Gate, Drain, Source and BackGate) during HCI and OFF-state stresses have been analyzed. Fig. 7 depicts the I_D, I_G, I_S and I_{BG} currents measured during the stress phase of the MSM tests at 2,4V. I_{BG} current shows no relevant change during the test, that means that the BOX damage can be neglected. I_D and I_S, which have the same magnitude but opposite sign, are larger in the case of the HCI stresses. Note that, though no channel has been created during the OFF-State stresses, large leakage current between Drain and Source are measured due to the lateral electric field applied. Moreover, their temporal trend of the currents for the two stresses is opposite: whereas they smoothly increase (in absolute value) with time for the OFF-State stress, they decrease for the HCI case. Surprisingly, when compared to the fresh device, there is a large increase of the gate current after both kind of tests. Though at the end of both tests the magnitude of I_G is similar, the temporal evolution differs. For the OFF-State stress, I_G remains small until the stress time is large enough

(approx,. 20 s in the example shown), and then it increases smoothly until a relatively constant value. In the case of the HCI tests, however, a large increase is observed at very short stress times and evolves with a similar trend as in the case of the OFF-State until the final value. Despite the different temporal trends, the increase of I_G suggests a significant degradation of the gate dielectric in the two cases.

In Fig. 8, the I_D, I_G, I_S and I_{BG} recorded during a V_G sweep (with $V_{DS} = 0$) when the stress was interrupted after 1500 s of stress at 2.4 V, for the 4 considered stresses, together with the fresh currents (coloured lines), are depicted as a function of the gate voltage. Both, the ON region (positive voltages) and OFF region (negative voltages) are analysed. The figure shows that, for the BTI tests, the changes in all the currents are very small, independently of the operation region, corroborating that BTI aging (positive or negative) is negligible in these devices. This is not the case for the OFF-Stress and HCI tests, where important changes in all currents are recorded after the stress, in the ON and OFF regimes. For these tests, in addition to the previously shown changes in the ON regime (Figs. 3 to 6), (i) an important increase of the gate current is measured for both gate voltage polarities and (ii) leakage currents through the drain and source are measured for negative gate voltages. Looking in more detail into the OFF regime (i.e. the negative voltages), one can note that the Gate current is almost coincident with the Drain current for the OFF-state stress but with the Source current for the HCI stress. This result could be interpreted as a larger damage of the bulk dielectric close to the drain/source for the OFF-State/HCI stresses [16]. The reason of this observation could be the larger vertical fields close to these terminals applied during these stresses (see Fig. 2). Since the increase of gate current is not observed during BTI tests (for which there is not current flow through the channel during the stress), the results suggest that currents are also needed (leakage during the OFF-State or ON currents during the HCI stresses) to introduce damage in the bulk of the dielectric (i.e. generate defects), leading to trap-assisted tunneling through the gate [17]. Note that gate current to appear requires long enough stress time or voltages (see Figs. 5 and 7).

In a nutshell, these experimental results suggest that in these deeply scaled FDSOI Ω-gate NW-FETs transistors, the simple application of a vertical electric field (BTI stress) provokes a negligible damage to the device (i.e. bulk and dielectric/channel interface degradations). However, when the transistor biasing is such that a channel current flows, either leakage (OFF-State stress) or direct (HCI stress), the device properties are substantially degraded. On the one hand, a large reduction of the drain current is observed in the ON regime, probably related to the degradation of the interface, that leads to an increase of the threshold voltage and to a decrease of the mobility of the carriers in the channel. On the other, for large enough stress conditions (time or voltage), a large increase of the Gate current is produced, which could be related to the degradation of the bulk of the dielectric as a consequence of the large vertical fields applied at one of the channel extremes, combined with the channel currents. This gate current will be measured as leakage current when the device is operated in the subthreshold and OFF-regimes. Regarding the BackGate current, it was always close to the noise level, before and after the stresses, indicating that the BOX suffers a negligible damage and is not affected by any of these aging mechanisms. More work has to be done to corroborate these preliminary interpretation of the results.

4. Conclusions

The degradation of N-type FDSOI Ω-gate NW-FETs induced by PBTI, NBTI, HCI and OFF-State stress was experimentally analysed and compared. NBTI/PBTI have the smallest (negligible) effect on the device performance, whereas HCI stress produces the largest $I_{D\text{-}ON}$ degradation, linked to a large increase/decrease of V_{TH}/μ, respectively. However, though the OFF-State stress induces a decrease of $I_{D\text{-}ON}$ smaller than that measured for HCI, for large enough stress conditions (voltage/time), a large increase of the subthreshold current ($I_{D\text{-}OFF}$) is observed, which can lead to a complete distortion of the I_D-V_G characteristic of the device and, therefore, to the loss of the device functionality. This increase of the subthreshold current has been attributed to the gate current that appears as a consequence of the degradation of the bulk of the gate dielectric during the OFF-State stresses.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

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Resistive switching like-behavior in FD-SOI Ω-gate transistors

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ABSTRACT

In this work, the Resistive switching (RS) phenomenon is experimentally investigated in N-type FDSOI Ω-gate NW-FETs with high-k dielectric. The location along the channel of the conductive filament through the device dielectric during switching is analyzed. Finally, the effects of RS on the characteristic transistor curves are also presented.

1. Introduction

Resistive switching (RS) is a phenomenon that has gained importance in the last years because its potential exploitation in many applications such as non-volatile data storage, alternative computing architectures, cryptography, etc. [1]. RS can be observed in Metal-Insulator-Metal or Semiconductor (MIM/MIS) structures fabricated with specific materials [2]. In these devices, the dielectric resistance shows a non-linear current–voltage characteristic, and the dielectric conductance can be changed when subjected to a proper biasing. When bias is not applied, the device resistance presents a non-volatile behavior. RS phenomenon is usually attributed to the formation of a conductive filament through the device dielectric whose physical structure is directly related to the dielectric resistance [2]. In the case of MIS structures in MOSFETs, the analysis of the currents through the transistor terminals allows to obtain information about the location along the channel of the conductive filament in the gate dielectric [3]. Few works about RS in very scaled devices as Gate All Around (GAA) transistors are found in literature. In [4,5] RS is observed in vertical GAA nanopillars integrated with RRAM cells, showing good non-volatile memory properties. In this work, the study of RS in FDSOI N-type Ω-gate NW-FETs is presented. The location of the conductive filament and the variation of transistor curves during switching are investigated.

2. Device description and measurement procedure

The FDSOI N-type Ω-gate NW-FETs under research were fabricated at CEA-LETI [6] and had a high-K dielectric stack (HfSiON/TiN) with EOT = 1.3 nm, H_{NW} = 11 nm and a buried oxide (BOX) thickness of 145 nm (Fig. 1). The devices were [1 1 0]-oriented. In this work, a single finger structure with gate width of W = 10 μm and gate length of L = 10 μm was used. The electrical measurements were performed with a Keithley 4200 Semiconductor Parameter Analyzer (SPA). To observe RS, firstly, a forming process was performed to create the conductive filament through the dielectric, by applying a voltage ramp from 0 V to 4 V with a 4 mA current limit. The current limit is applied to avoid the irreversible hard breakdown of the dielectric. During RS, dielectric resistance changes between two different states, a Low Resistance State (LRS) and a High Resistance State (HRS). The transition from LRS to HRS is called reset process and the change between the HRS to LRS is named set process (Fig. 2 left). The samples used in this work show bipolar RS, what means that positive/negative voltages are needed to provoke the set/reset processes respectively (Fig. 2 right).

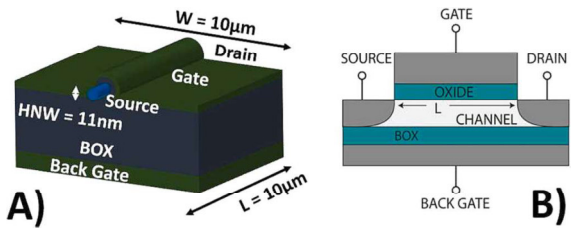

Fig. 1. 3D sketch of the Ω-Gate structure (left) and cross-section (right) of the FD-SOI transistors used in this work.

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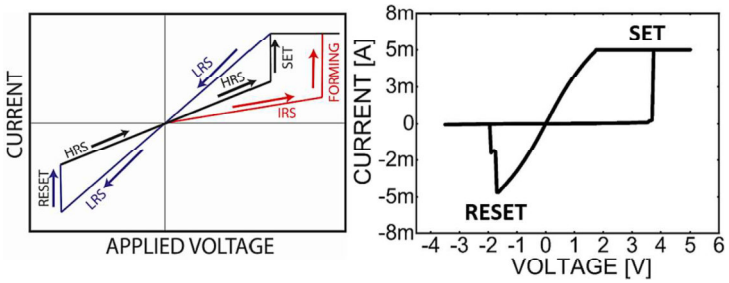

Fig. 2. Schematic (left) and experimental (right) RS I-V curves in bipolar resistive switching.

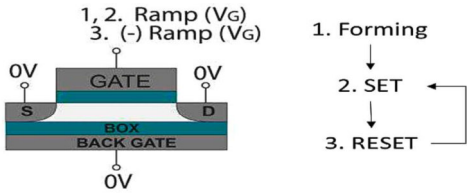

Fig. 3. Biasing configuration of the four device terminals to produce a forming, set and reset processes.

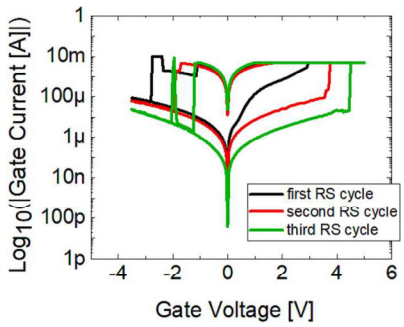

Fig. 4. I-V characteristics measured in the same sample during three consecutive RS cycles, after a forming process.

To perform the RS measurements, all four terminals of the transistor were contacted (Fig. 3). To provoke set processes, a positive ramp voltage from 0 to 5 V with a compliance of 5 mA was applied to the gate with the other three terminals grounded. The reset process was observed by applying a negative ramp voltage from 0 to −3.5 V, with a compliance of 10 mA, to the gate, with the other three terminals grounded. During the voltage sweeps (starting from 0 to 5 V, continuing from 5 V to −3.5 V and finally from −3.5 V to 0 V) that produce the set and reset processes (RS cycle), the currents through the transistor terminals (I_G, I_D, I_S, I_B) were registered.

3. Results and discussion

Fig. 4 shows three consecutive experimental gate I-V curves in the same sample, after the forming process. Cycle-to-cycle dispersion of the set and reset voltages is observed. In the performed measurements, set/reset voltages vary between 2.5 V and 5 V and from −1.3 V to −2.5 V, respectively.

The use of transistors allows the analysis of the RS filament location along the channel [3]. Fig. 5 shows the four terminals transistor currents as a function of V_G measured simultaneously to the first (Fig. 5 left) and the second (Fig. 5 right) I-V curves of Fig. 1. In Fig. 5 left, for positive

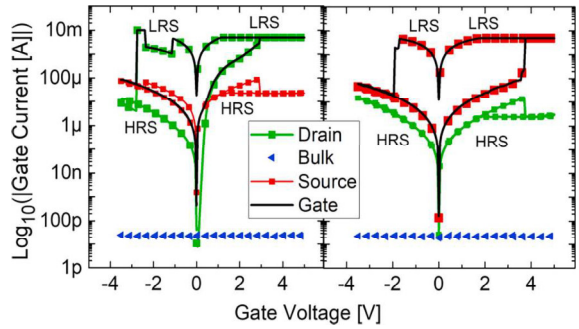

Fig. 5. I_D (green), I_B (blue), I_S (red), I_G (black) currents, registered during the first (left) and second (right) RS cycles in Fig. 1

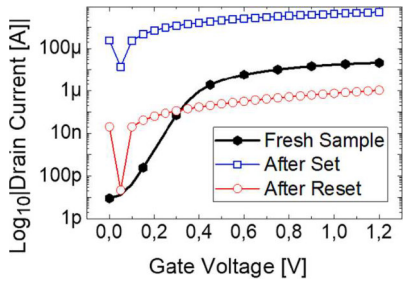

Fig. 6. I_D-V_G characteristics of the fresh sample (black) and after set (blue) and reset (red) processes.

voltage range, both in the LRS and HRS, drain and gate currents are also equal which suggests a RS filament located close to the drain. In the negative voltage range, during the LRS the filament is still located close to the drain. However, when reset process is produced, and the device reaches the HRS, a RS filament close to the source becomes more relevant. In Fig. 5 right, the filament close to the source is always predominant in all the RS cycle. Then, the results show the existence of conductive filaments close to the drain and source and their dominance depends on the RS cycling.

The influence of RS on transistor curves was also studied. Fig. 6 shows that after both set and reset processes, the I_D-V_G transistor curves are completely distorted and the transistor's functionality cannot be recovered after reset. Fig. 7 shows the I_D-V_D characteristic of a fresh device (Fig. 7A). After forming (Fig. 7B), the I_D-V_D curve is still distinguishable but after set (Fig. 7C) the functionality of the device is completely lost and cannot be recovered after reset (Fig. 7D). The results suggest that the electrical conditions applied to observe RS in these devices produce severe damage in the dielectric, largely affecting the transistor functionality.

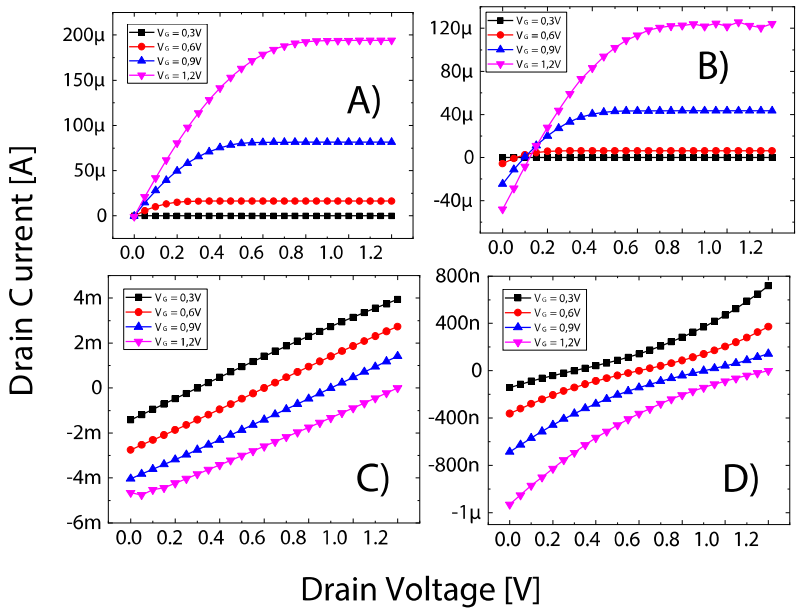

Fig. 7. I_D-V_D transistor characteristics A) for fresh device. B) After forming. After set C) and reset D) processes.

4. Conclusions

RS phenomenon has been experimentally analyzed in N-type FDSOI Ω-gate NW-FETs with high-k dielectric. Conductive filaments located close to drain and source have been observed; one or the other may control the dielectric conductance, depending on the RS cycling. Although two switchable conductive states can be observed in the MIS gate stack, the electrical conditions used to observe the RS produce severe damage on the transistor functionality. In this regard, future works will explore the possibility of recovering the transistor functionality after a reset process using less harmful RS electrical conditions during the set process. This may allow to combine in a single device a memristor and a transistor [3].

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

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Resistive Switching phenomenon in FD-SOI Ω-Gate FETs: Transistor performance recovery and back gate bias influence

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Resistive Switching phenomenon in FD-SOI Ω-Gate FETs: Transistor performance recovery and back gate bias influence☆

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ABSTRACT

Resistive Switching (RS) phenomenon, usually observed in two-terminal memristor devices, refers to the reversible change in resistance of a material under an external electric field. In this work, RS has been observed in N-type Fully Depleted Silicon-On-Insulator (FDSOI) Ω-gate nanowire field-effect transistors (NW-FETs). For the first time, partial recovery of the transistor's I_D-V_D characteristics during the RS cycling is experimentally demonstrated, indicating the potential of the device to be used both as a transistor and a memristor. The effect of increasing the back gate voltage on the RS characteristics was also experimentally investigated. It was found that higher back gate voltages enhance the RS parameters, thereby establishing a direct relationship between back bias and device performance.

1. Introduction

Resistive Switching (RS) phenomenon, as the basis of memristor devices, has acquired significant interest in the scientific community because of its potential in memory, logic, security, neuromorphic applications, etc. [1]. RS is typically observed in two terminal structures that incorporate a dielectric material between their terminals, such as Metal-Insulator-Metal (MIM) or Metal-Insulator-Semiconductor (MIS) devices. RS involves the reversible change of the conductivity of the dielectric material: the larger conductivity corresponds to a Low Resistance State (LRS), while the smaller correspond to a High Resistance State (HRS) [2]. These changes in the dielectric resistance are achieved by applying an appropriate voltage to the device terminals. The resistance states associated to the RS phenomenon are linked to the formation of a conductive path (CP) through the dielectric, which in some devices is generated through an initial electroforming process, referred to as 'forming' (see Fig. 2A). The transition from HRS to LRS is named as 'set' process, while the transition from LRS to HRS is named as 'reset' process (see Fig. 2B).

Though RS is usually exploited in two terminal devices, RS was observed in bulk MOSFETs [4] and more recently also in FD-SOI quasi-planar transistors [3], which opens the possibility of using the device as either a transistor or a memristor, as necessary [4]. In [3], the electrical conditions used to observe the RS caused significant damage to the transistor's functionality. In contrast to that study, this work analyzes the RS voltage and current conditions required to partially recover the I_D-V_D curves. On the other hand, in these devices the back gate voltage (V_B) influences transistor's performance [5–7]. In this work, for the first time, the effect of V_B on RS is evaluated.

2. Device description

The N-type Ω-gate NW-FETs used in this work were fabricated at CEA-LETI with SOI (Silicon on Insulator) technology and have L = 10 μm gate length and W = 10 μm width [7]. Their planar and cross-section representations are shown in Fig. 1A and Fig. 1B, respectively. The device is a single finger structure with a nanowire height (H_{NW}) of 11 nm. The buried oxide layer (BOX) has a thickness of 145 nm (see Fig. 1B). Because the large difference between the gate length and width (L = 10 μm x W = 10 μm) compared to the nanowire height (H_{NW} = 11 nm), the device can be considered as a quasi-planar SOI MOSFET [7] (Fig. 1C).

Electrical measurements were carried out using an Agilent 4156C Precision Semiconductor Parameter Analyzer, to obtain the I_G-V_G and I_D-V_D curves of the devices.

3. Results and discussion

This section experimentally analyses the possibility of recovering the

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transistor's characteristics during a complete RS cycle. Additionally, the impact of the back gate voltage on RS is experimentally evaluated.

3.1. Partial recovery of transistors characteristics during RS

Fig. 2 shows the I_G-V_G curves measured during the forming process (Fig. 2A) and a complete RS cycle, i.e. a reset followed by a set. (Fig. 2B). The electrical conditions applied in the electroforming process (Fig. 2A) are a continuous voltage sweep ranging from $V_G = 0$ V to 4 V, with a current compliance limit of 4 mA for the gate current (I_G).The reset process was measured by applying a negative voltage ramp to the gate terminal, ranging from $V_G = 0$ V to −2V, with gate current compliance of $I_G = 8$ mA (Fig. 2B Left). The set process was measured by applying positive voltages to the gate terminal, ranging from $V_G = 0$ V to 4 V with a gate current limit of $I_G = 4.5$ mA (Fig. 2B Right). The device shows bipolar switching. A reversible dielectric breakdown is a potential mechanism underlying resistive switching (RS). It occurs within a localized area of the insulator, where a CP forms through the dielectric, facilitating the RS phenomenon [8–10].

The I_D-V_D characteristics were obtained by applying voltage ramps to the drain terminal, with voltages ranging from $V_D = 0$ V to 1.2 V, while setting the gate voltage at $V_G = 0.3$ V, 0.6 V, 0.9 V and 1.2 V and the back gate voltage at $V_B = 0$ V. The I_D-V_D curve of the fresh sample (i.e., before forming) is depicted in Fig. 2C. The I_D-V_D characteristics of the transistor measured after the forming process are illustrated in Fig. 2D. Note that in a reduced drain voltage range (from 0 to 0.1 V), larger currents than for the fresh case and a negative dependence with voltage is observed, reaching $I_D = 0$ at $V_B = 0.1$ V. However, for larger voltages, a similar shape is observed, though with smaller currents, when compared to the fresh case (Fig. 2C), indicating that the device can be still operated as a FET.

The transistor's I_D-V_D curves following reset and set processes are shown in Fig. 2E and Fig. 2F, respectively. Similar trends than those described for the post-forming curves are observed, i.e. an initial voltage range that shows negative resistance followed by typical MOSFET behaviour. However, focusing the attention in the last case, the current levels depend on the dielectric state: when compared to the values measured in the fresh device, smaller currents are observed after set but currents are similar after reset. Then, the transistor current driving capability is partially recovered after undergoing the reset process (Fig. 2E). As an example, I_D after reset process measured at $V_G = 1.2$ V and $V_D = 1.2$ V decreases approximately 9 % with respect to the corresponding current of the fresh sample (see I_D-V_D characteristic in Fig. 2C and Fig. 2E), preserving the transistor functionality. This result was validated through several experiments, which revealed that by reducing the current compliance ($I_G = 8$ mA) and limiting the gate voltage ($V_G = -2$V) during the reset process, the transistor is still operative, though the operating voltage region has slightly changed, as shown in Fig. 2E and 2F.

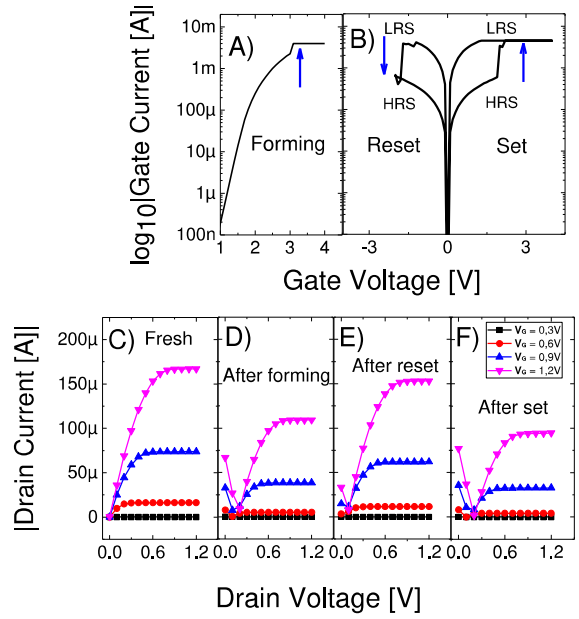

Fig. 2. Experimental I_G-V_G curves for A) forming, B) reset and set processes. I_D-V_D transistor characteristics at different gate voltages for C) a fresh device. D) after forming. E) after reset and F) after set processes. In all cases, $V_B = 0$ V.

3.2. Impact of the back gate bias on RS

In this section, it will be preliminary analyzed the impact of the back gate bias on the RS phenomenon in these devices. Fig. 3 illustrates the measurement procedure for three distinct cases used to compare the influence of the back gate bias voltage in the set and reset processes. In the first case (Fig. 3A), a positive voltage sweep from 0 to 4 V is applied to the gate terminal (V_G) while a constant negative voltage is simultaneously applied to the back gate terminal. Voltages of $V_B = 0$, −0,1V, −0.2 V, −0,3V and −0,4V are considered. This voltage configuration will be used to analyze the V_B impact on the RS cycle applying these conditions only on set process ($V_B = 0$ V during the reset process). In the second case (Fig. 3B), a negative voltage sweep from 0 to −2V is applied to the gate terminal (V_G), with a constant negative voltage of $V_B = -0.2$ V applied simultaneously to the back gate terminal. This voltage configuration will be used to analyze the V_B impact on the RS cycle applying these conditions only on the reset process ($V_B = 0$ V during the set process). In the third case (Fig. 3C), a positive voltage sweep (from 0 to 4 V) is applied to the gate terminal (V_G) Immediately following this, a negative voltage sweep (from 0 to −2V) is applied to the gate terminal. The back gate terminal is biased with a constant negative voltage of $V_B =$

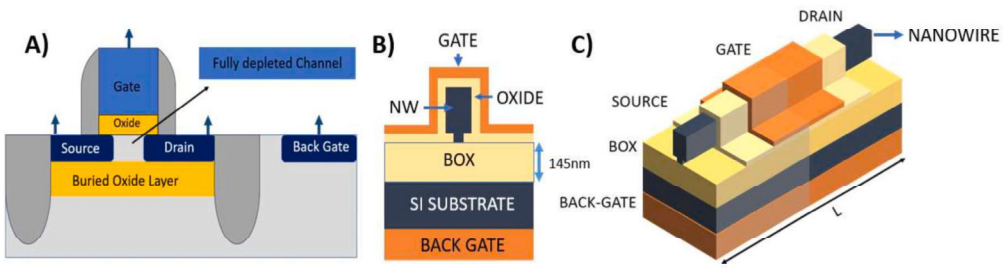

Fig. 1. Planar representation of the FD-SOI FET (A) cross section of the Ω-gate Nanowire (B) 3D sketch (not in scale) of the FD-SOI quasi-planar transistors used in this work (C).

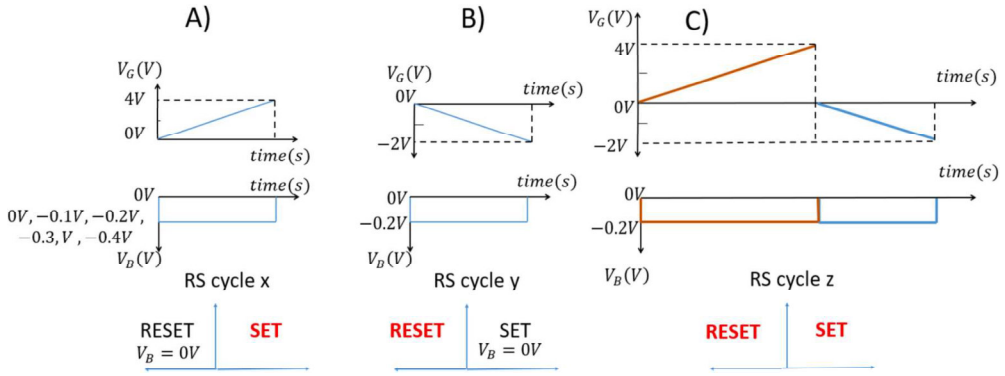

Fig. 3. Measurement procedure of three different approaches used to compare back gate voltage influence in RS set and reset events A) V_B = 0 V, −0.1 V, −0.2 V, −0.3 V, −0.4 V during set process B) V_B = − 0.2 V during reset process C) V_B = − 0.2 V during reset and set processes.

−0.2 V, during both the set and reset processes. This voltage configuration will be used to analyze V_B impact on the complete RS cycle applying $V_B \neq 0$ V.

Fig. 4 shows the average of three RS cycles, when V_B is only applied during the set process (voltage configuration shown in Fig. 3A.), for the cases of $V_B = 0$ V (Fig. 4A), − 0.1 V (Fig. 4B), − 0.2 V (Fig. 4C), − 0.3 V (Fig. 4D) and − 0.4 V (Fig. 4E). To evaluate the impact of V_B on the device performance, the I_{ON}/I_{OFF} ratio has been used as parameter to describe the device performance. I_{ON} is measured when the sample is in the LRS, and I_{OFF} is measured when the sample is in the HRS, at V_G = −1V and V_G = +1V (see Fig. 4A and D). This mean ratio is calculated over three cycles for each voltage configuration using a single sample. Fig. 5 shows the I_{ON}/I_{OFF} mean ratio measured at V_G = −1V and V_G = +1V as a function of V_B. The increasing I_{ON}/I_{OFF} ratio (averaging all the cycles) measured at V_G = -1V shows an increase with V_B (see Fig. 5 blue solid line) and it facilitates the distinction between the memristor

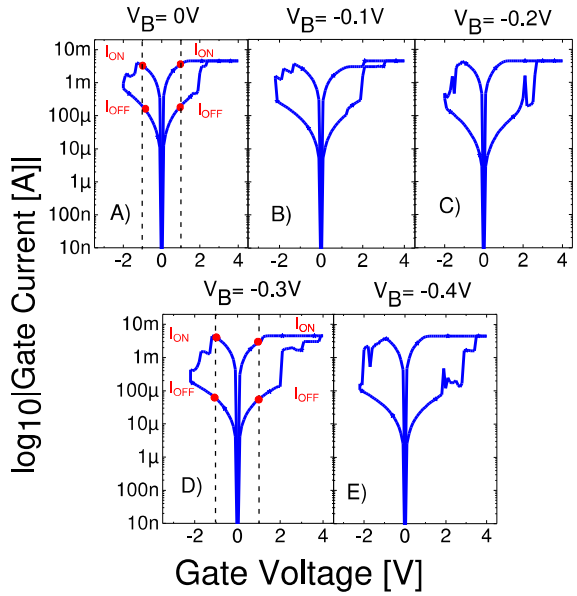

Fig. 4. RS I-V average curves of several cycles measured on the same sample when A) V_B = 0 V, B) V_B = -0.1 V, C) V_B = -0.2 V, D) V_B = -0.3 V, E) V_B = -0.4 V during set process. In (A) and (D) the I_{ON} and I_{OFF} currents measured at V_G = −1V and V_G = +1V to obtain the I_{ON} /I_{OFF} ratio are illustrated.

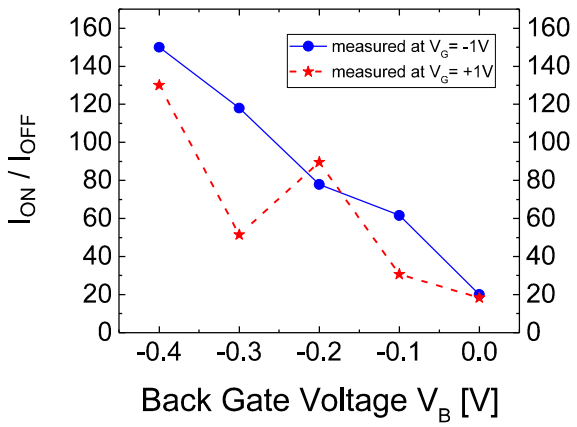

Fig. 5. I_{ON}- I_{OFF} mean ratio measured at V_G = -1V (blue) and at V_G = +1V (red) as a function of back gate voltage (V_B) for the measurements represented in Fig. 4.

conduction states, which is beneficial for memory applications. However, this I_{ON}/I_{OFF} ratio shows no stable increment with V_G when it is measured at V_G = +1V (see Fig. 5 red dash line). This can be attributed to the transversal electric field effect at negative back gate voltages in these wide-channel devices (W = 10 µm) [7], due to the total voltage applied to the structure. This electric field can affect the conductive filament structure during RS, especially during the reset process, decreasing the dielectric conduction (see Fig. 4), and consequently, increasing the I_{ON}/I_{OFF} ratio.

Fig. 6A shows the average of three RS cycles obtained when V_B= − 0.2 V during the reset process and V_B = 0 V during the set process (configuration in Fig. 3B). Fig. 6B shows the average of three RS cycles when V_B= − 0.2 V during both reset and set processes (configuration in Fig. 3C). The I_{ON}/I_{OFF} mean ratio (averaging all the cycles) for the curves in Fig. 6A and 6B, respectively are qualitative equal. Note that, when compared to the case of V_B = 0 V during the reset (Fig. 4C), in both cases, no significant impact of V_B on the I_{ON}/I_{OFF} mean ratio is observed, as far as can be expected in two different samples. These preliminary results suggest, in contrast to the experiment in Fig. 4, seems to indicate that there is no significant impact of V_B on RS characteristics when the reset and both set and reset processes are studied. In the first case, (Fig. 6A), the electric field (during the application of $V_B \neq 0$ V during the reset process) contributes to larger conduction through the conductive filament. In second case, (Fig. 6B) although $V_B \neq 0$ V is applied during both

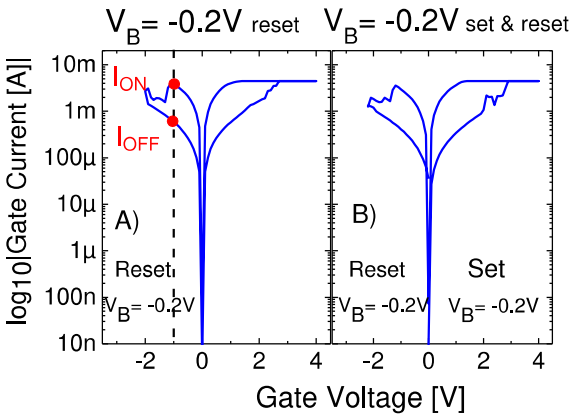

Fig. 6. RS I_G -V_G average curves measured on the same sample when A) V_B = -0.2 V for the reset process only (V_B = 0 during the set), B) V_B = -0.2 V during set and reset process.

set and reset processes consecutively, the electric field generated by the negative voltage (during the reset process) remains insufficient to decrease the conduction through the conductive filament formed during the set process.

4. Conclusions

In summary, this work experimentally studies, on the one hand, the I_D-V_D transistor curves, when the gate dielectric is at the high and low resistance states. The results point out that the transistor performance can be partially recovered after the reset process, by applying appropriate RS voltages and current limit conditions. This demonstrates the feasibility of integrating a memristor and a transistor within a single device also with these FDSOI devices. On the other hand, the back gate voltage influence on the device has been preliminary studied. When a negative back gate voltage is applied during set process the I_{ON}/I_{OFF} ratio increases, which could be related to the impact of the strong transversal electrical field. However, preliminary results indicate no significant effects of this bias on the I_{ON}/I_{OFF} ratio when it is applied during the reset process with $V_B \neq 0$ V or a complete RS cycle with $V_B \neq 0$ V in both set and reset processes. These differences need to be further addressed in future research.

CRediT authorship contribution statement

C. Valdivieso: . **R. Rodriguez:** Writing – original draft, Supervision. **A. Crespo-Yepes:** Resources. **J. Martin-Martinez:** Supervision. **M. Nafria:** Writing – original draft, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

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Data availability

Data will be made available on request.

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