UAB
Universitat Autònoma de Barcelona

Integration of silicon micro- and nano-structures for thermoelectric generators

Alex Rodríguez Iglesias

ADVERTIMENT. L'accés als continguts d'aquesta tesi queda condicionat a l'acceptació de les condicions d'ús establertes per la següent llicència Creative Commons: https://creativecommons.org/licenses/?lang=ca

ADVERTENCIA. El acceso a los contenidos de esta tesis queda condicionado a la aceptación de las condiciones de uso establecidas por la siguiente licencia Creative Commons: https://creativecommons.org/licenses/?lang=es

WARNING. The access to the contents of this doctoral thesis it is limited to the acceptance of the use conditions set by the following Creative Commons license: https://creativecommons.org/licenses/?lang=en

Universitat Autònoma de Barcelona
Department of Microelectronics and Electronic Systems

Integration of silicon micro- and nano-structures for thermoelectric generators

A thesis submitted to obtain the degree of:

Doctor of Philosophy (PhD) in Electronic and Telecommunication Engineering

Alex Rodríguez Iglesias

Supervisors:

Dr. Marc Salleras Freixes

Dr. Iñigo Martín Fernández

Dr. Marta Fernández Regúlez

Tutor:

Dr. Nuria Barniol Beumala

PhD Thesis - 2025

The doctors **Dr. Marc Salleras Freixes**, **Dr. Iñigo Martín Fernández** and **Dr. Marta Fernández Regúlez**, senior researchers at the Institute of Microelectronics of Barcelona, hereby certify that the work presented in the doctoral thesis entitled:

Integration of silicon micro- and nano-structures for thermoelectric generators

has been carried out by **Alex Rodríguez Iglesias** under our direct supervision. We confirm that we have guided and monitored the research activities, and further certify that the work presented constitutes the candidate's own research.

Dr. Marc Salleras Freixes	Dr. Iñigo Martín Fernández	Dr. Marta Fernández Regúlez

Barcelona, November, 2025

Acknowledgments

Esta tesis se ha podido llevar a cabo gracias a la ayuda y compañía de mucha gente: compañeros de equipo (especialmente de los grupos Thermitas y MESSI), de laboratorio, de despacho y de comida; personal de las diferentes áreas de sala blanca y del IMB-CNM; el grupo Nanophononics de la Universidad de Basilea, el grupo de Propiedades Térmicas de Materiales en la Nanoescala (GTNaM) de la UAB, el grupo de Nanoionics and Fuel Cells de IREC y la empresa AEInnova; familia y amigos. Estoy especialmente agradecido a mis tres directores de tesis: Marc Salleras, Íñigo Martín y Marta Fernández, por la ayuda continua y la supervisión durante todos estos años, y a Aida, por haberme acompañado más de cerca en este camino.

Abstract

Harvesting environmental energy sources to meet the growing demand of electronic devices is a key challenge in reducing the environmental footprint of our society. Among the available sources, heat offers a promising future due to its ubiquitous presence as a byproduct in industry, transportation and energy-related processes. In this context, thermoelectric generators stand out as a route to convert heat into electricity, as they are compact and robust devices (i.e. they have no moving parts and therefore require little to no maintenance) and possess excellent scalability (i.e. they can be reduced in size without affecting their efficiency). These properties make thermoelectric generators promising candidates for powering wearable or sensor devices, particularly those operating in harsh environments, such as Internet of Things sensor nodes. Nonetheless, the current use of thermoelectric generators remains significantly limited because most commercial devices are based on expensive and toxic materials, like bismuth telluride. Therefore, alternative materials must be explored. Silicon is a prominent choice due to its abundance, non-toxicity, and excellent integration and miniaturization capabilities. However, the high thermal conductivity of bulk silicon limits its thermoelectric efficiency. Therefore, to make silicon viable in thermoelectric applications, this challenge must be addressed. The objective of this thesis is to investigate the potential of silicon as a thermoelectric material.

Two main approaches were employed for this purpose. The first is nanostructuring silicon in the form of nanowires and nano-patterned thin films. In this case, the thermoelectric properties of silicon are enhanced by the dimensional constraints of the structures. Silicon nanowires were grown by IREC collaborators, whereas the patterned thin films were fully developed within this thesis. The second approach involves using silicon microbeams. Here, the thermoelectric properties of silicon remain equivalent to those of bulk, and the objective is to explore whether enhancing thermal management in a thermoelectric generator can make bulk silicon viable for this application. Various micro-test devices and micro-thermoelectric generators were fabricated in this thesis using silicon technology to investigate the structures described above. Moreover, a reliable procedure to integrate a heat sink onto the micro-thermoelectric generators was developed to maximize their performance. In the case of nanowires and microbeams, fully packed micro-thermoelectric generators with heat sink were fabricated and characterized under conditions that mimic real operational scenarios. Power densities well within the Internet of Things requirements (i.e. above 10 $\mu W/cm^2$) were obtained for temperatures above 175°C, while powers in the microwatt range were achieved under moderate hot temperatures (above 100°C). Thermal, electrical and Seebeck measurements employing micro-test devices were performed to study the thermoelectric properties of the patterned thin films. These measurements demonstrated more than an 8-fold increase in the thermoelectric figure of merit compared to bulk silicon. Voltage generation capabilities were investigated

in micro-thermoelectric generators based on patterned thin films. A 4.4-fold increase in the harvested thermal gradient was observed compared to the best nanowire-based micro-thermoelectric generators. These results demonstrated that nano-patterned films offer a significant improvement both in terms of thermoelectric properties and thermoelectric generation compared to the first generation of silicon structures (i.e. nanowires).

Resumen

Aprovechar las fuentes de energía medioambientales para satisfacer la creciente demanda de los dispositivos electrónicos es un desafío clave para reducir la huella ambiental de nuestra sociedad. Entre las fuentes disponibles, el calor presenta un futuro prometedor debido a su presencia ubicua como subproducto en los procesos relacionados con la energía, la industria y el transporte. En este contexto, los generadores termoeléctricos destacan como una posible ruta para convertir calor en electricidad debido a que son dispositivos compactos y robustos (i.e. no tienen partes móviles y, por lo tanto, necesitan poco o ningún mantenimiento) y poseen una escalabilidad excelente (i.e. se pueden reducir en tamaño sin empeorar su eficiencia). Estas propiedades hacen que los generadores termoeléctricos sean candidatos prometedores para alimentar dispositivos portátiles o sensores, en particular aquellos que operan en entornos adversos, como los nodos de sensores del llamado Internet de las Cosas. Sin embargo, el uso actual de los generadores termoeléctricos sigue siendo limitado debido a que la mayoría de los dispositivos comerciales están basados en materiales costosos y tóxicos, como el telururo de bismuto. Es por ello que se deben explorar materiales alternativos. En este contexto el silicio destaca por su abundancia, no toxicidad y excelentes capacidades de integración y miniaturización. No obstante, la alta conductividad térmica del silicio limita sus capacidades termoeléctricas, por lo que hay que abordar este desafío para hacer al silicio viable en aplicaciones termoeléctricas. El objetivo de esta tesis es por lo tanto investigar el potencial del silicio como material termoeléctrico.

Para ello se han empleado dos estrategias. La primera es nanoestructurar el silicio en forma de nanohilos o de capas finas nanoestructuradas. En este caso se mejoran las propiedades termoeléctricas del silicio gracias a las limitaciones dimensionales de las estructuras. Los nanohilos se han crecido gracias a una colaboración con el IREC, mientras que las capas nanoestructuradas se han desarrollado por completo en el marco de esta tesis. El segundo enfoque consiste en utilizar microestructuras de silicio. Como en este caso no se mejoran las propiedades termoeléctricas del material, el objetivo de esta estrategia es explorar si una mejora considerable en la gestión térmica del generador puede hacer viable al silicio. Para investigar estas tres estructuras se han fabricado varios dispositivos y micro-generadores termoeléctricos usando la tecnología de silicio. Además, se ha desarrollado también una metodología para poder integrar un disipador de calor en los micro-generadores termoeléctricos con el objetivo de maximizar su rendimiento. En el caso de las microestructuras y los nanohilos de silicio, se han fabricado y caracterizado micro-generadores termoeléctricos con disipador de calor bajo condiciones que imitan escenarios operativos reales. Se obtuvieron densidades de potencia dentro de los requerimientos del Internet de las Cosas (i.e. superiores a 10 $\mu W/cm^2$) a temperaturas superiores a 175°C, mientras que se alcanzaron potencias en el rango de los microvatios a temper-

aturas más moderadas (por encima de 100°C). Además, se han medido las propiedades térmicas, eléctricas y el coeficiente de Seebeck de las capas finas nanoestructuradas usando dispositivos de test específicamente diseñados. Estas mediciones demostraron un incremento superior a 8 veces en la figura de mérito termoeléctrica en comparación con el silicio sin estructurar. Las capacidades de generación de voltaje se investigaron en micro-generadores termoeléctricos basados en capas finas nanoestructuradas. Se observó un aumento de 4.4 veces en el gradiente térmico que eran capaces de aprovechar en comparación con los mejores generadores basados en nanohilos. Estos resultados demuestran que las capas finas con nanoestructuras ofrecen una mejora significativa, tanto en las propiedades termoeléctricas como en la generación termoeléctrica, en comparación con la primera generación de nanoestructuras de silicio (i.e. los nanohilos).

Scope of the thesis

The objective of this thesis is the investigation of silicon as a thermoelectric material. This encompasses not only the characterization of the thermal, electrical and Seebeck properties of the structures but also their integration into functional micro-thermoelectric generators. Subsequently, their thermoelectric generation capabilities are also explored. Three silicon structures were investigated in this thesis: silicon nanowires, silicon microbeams and nanostructured silicon thin films.

Previous work in the group successfully fabricated micro-thermoelectric generators with epitaxially grown silicon nanowires and microbeams. Investigation of the nanowire properties was also performed. Therefore, this thesis aims to build upon the group's previous work in this field by optimizing and characterizing different generator layouts to identify the best design, and by continuing the previous efforts to enhance their power generation through the integration of a heat sink. For these reasons, most of the work on material characterization is focused on the nanostructured silicon thin films that were fully developed within the scope of this work, although Seebeck characterization of the nanowires was also carried out. In contrast, the characterization of thermoelectric generation encompasses all three silicon structures. With the exception of thermoelectric generators based on nanowires and microbeams, the remaining devices in this thesis were designed or redesigned ad hoc, and were either fabricated or supervised during their fabrication. In the case of nanowires and microbeams, the contribution was limited to specific steps at the final stages of the fabrication process.

This thesis was developed at the Institute of Microelectronics of Barcelona (IMB-CNM, CSIC), primarily in the cleanroom facilities and the different electrical characterization laboratories. The nanowires studied in this work were grown within a collaboration with the Institute for Energy Research of Catalonia (IREC), while the integration of a 2x2 thermoelectric generator system was done in collaboration with AEInnova, a Spanish company innovating in autonomous sensors that exploit thermoelectric power generation. Thermal characterization of the devices was carried out in collaboration with the Autonomous University of Barcelona (UAB) for the 3ω steady state measurements, and within the framework of an internship at the University of Basel on the laser/bridge and thermoreflectance cases. The thesis is divided in three parts, each including different chapters, and is organized as follows:

- **Part 1: Background and Methods.**

Chapter 1: Introduction. This chapter introduces the main motivation of this thesis, which relates to the possibility of powering Internet of Things nodes with thermoelectricity. This is followed by a thorough overview of the principles of thermoelectricity and a state of the art review of thermoelectric materials, including silicon. Then, thermo-

electric generators are presented, with a specific review dedicated to micro-thermoelectric generators. Finally, this chapter concludes with a brief overview of block copolymers, the materials employed in this thesis to nanostructure silicon thin films.

Chapter 2: Experimental methods. This chapter starts with a brief presentation of the different micro- and nano-fabrication methods used in this thesis to fabricate structures and devices. This includes an explanation of their limitations and operating conditions. The following section describes the structural characterization methods employed to evaluate materials and devices, followed by the methods related to thermoelectric characterization. First, the electrical methods are described, including 4-probe and transmission line, which were used to measure resistivity and contact resistance on thin films. Second, the thermal methods are described, including 3ω steady state, thermoreflectance, bridge/laser and temperature coefficient of resistance. Some considerations of the setups, operational conditions or thermal models are discussed. Finally, the setup used for thermoelectric characterization is presented, followed by the Seebeck and power generation use cases.

- **Part 2: Micro-thermoelectric generators based on silicon nanowires and microbeams.**

Chapter 3: Characterization of micro-thermoelectric generators. This chapter focuses on the results of bare micro-thermoelectric generators based on nanowires and microbeams. To this end, and to better understand the operation of the devices, the chapter begins with a description of the design and fabrication of the micro-thermoelectric generators, with particular emphasis on the steps optimized within this thesis. Afterwards, the results of the characterization of the different devices are shown. This includes the Seebeck and generation capabilities of the different designs before the integration of the heat sink. The final conclusions from this chapter are presented.

Chapter 4: Heat sink integration in micro-thermoelectric generators. This chapter starts by describing the methodology for implementing a heat sink in the micro-thermoelectric generators. Afterwards, simulations predicting the expected improvement in thermal management are presented. This is accompanied by a description of the thermal model used to understand the behavior of the complete micro-thermoelectric device at all stages of heat sink integration. Later, the results of the characterization of these chips with the heat sink are benchmarked. The effect of the heat sink on the nanowires and microbeams devices is discussed, along with a comparison to other silicon micro-thermoelectric generators reported in the literature. Further characterization to evaluate the compatibility of these generators with the Internet of Things needs is described, including long term and transient experiments. Finally, a 2x2 generator is presented. This device integrates four individual micro-thermoelectric generators, demonstrating the scalability of the number of micro-generators within a single device. The final conclusions from this chapter are presented.

- **Part 3: Thermoelectric characterization of silicon thin films nanostructured with block copolymers.**

Chapter 5: Silicon thin films nanostructured with block copolymers. This chapter focuses on the results of nanostructuring silicon thin films. The first sections present the optimization of block copolymer self-assembly, blending, and pattern transfer into silicon films. These show the different routes that were explored to pattern silicon films using block copolymers. The next section presents the doping process optimized using the spin on dopant technique, applied to both thin films and bulk samples on chips and

wafers. Subsequent results of the electrical characterization of bare and nanostructured films are presented, discussing the effect of patterning on their electrical conductivity. The final conclusions from this chapter are presented.

Chapter 6: Thermal characterization of nanostructured silicon thin films. This chapter presents the thermal characterization of nanostructured silicon thin films. It is divided in three sections, each corresponding to a different characterization method. In all cases, the device design and fabrication are first described in detail, with particular emphasis on the challenges that had to be solved to reliably fabricate devices with suspended nanostructured silicon films. Then, the results are presented and discussed, and put into perspective with other holey silicon structures and models reported in the literature. In the thermoreflectance case, the experimental work is still pending at the time of the submission of this thesis. Thus, this part ends after discussing the thermal model that was developed to analyze the results from the characterization. The final conclusions from this chapter are presented.

Chapter 7: Micro-thermoelectric generator based on nanostructured thin films. This chapter focuses on micro-thermoelectric generators based on nanostructured silicon films. It starts with the description of its design and fabrication, followed by the thermoelectric characterization. Due to the high contact resistance of this first generation of devices, the characterization is limited to voltage generation and Seebeck measurements. These last allow the final calculation of the figure of merit of the patterned films. All the results are followed by a discussion and benchmarking against the solutions based on nanowires and microbeams in chapter 3 and other structures in the literature. The last section presents the work done to optimize the resistance of the silicon-titanium contact. The final conclusions from this chapter are presented.

Chapter 8: Conclusions. This chapter discusses the achievements of this thesis and outlines its future perspectives.

Additionally, four appendices are included:

Appendix A: Directed self-assembly of block copolymers. This appendix presents a brief theoretical overview of the directed self-assembly of block copolymers, followed by the results obtained within this thesis. This includes the fabrication of guiding patterns and the directed self-assembly of lamellar block copolymers.

Appendix B: Suspension of membranes using topside KOH etching. This appendix presents an alternative route to suspend ultra-thin Si membranes using topside KOH etching that was explored and successfully developed within this thesis.

Appendix C: Adapter piece redesign. This appendix presents the redesign of the adapter piece aimed at improving the thermal management of micro-thermoelectric generators with heat sink. First, COMSOL simulations demonstrate the enhancement that could be achieved with an improved adapter. Then, the first fabrication trials that were explored with different designs are described.

Appendix D: Ongoing work on nanostructured films. This appendix presents the ongoing work related to nanostructured films. This includes the thermoreflectance characterization of membranes and the fabrication of the second generation of micro-thermoelectric generators with optimized contact resistance.

Nomenclature

List of abbreviations

3ω	3-omega characterization
4X	µTEG with four platforms featuring integrated heaters
e	Electrical
ph	Phonon
µTC	micro-Thermocouple
µTEG	micro-Thermoelectric generator
a-Si	Amorphous silicon
AA	Acetic acid
ALD	Atomic layer deposition
AOT	Dioctyl sulfosuccinate sodium salt
BCP	Block copolymer
BOE	Buffered oxide etchant
BOX	Buried oxide
CMOS	Complementary Metal-Oxide Semiconductor
CPD	Critical point dryer
CVD	Chemical vapor deposition
DC	Direct current
DRIE	Deep Reactive ion etching
DSA	Directed self-assembly
EBL	Electron beam lithography
EDS	Energy Dispersive X-ray Spectroscopy
FCV	Forced convection
FDTR	Frequency-domain thermoreflectance
FEM	Finite element model
FIB	Focused ion beam
GDOES	Glow-discharge optical emission spectroscopy
GP	Guiding pattern

HCl	Hydrochloric acid
HF	Hydrofluoric acid
IC	Integrated circuits
IMB-CNM	Institute of Microelectronics of Barcelona
IoT	Internet of Things
IPA	Isopropanol
IREC	Catalonia Institute for Energy Research
IVP	Voltage-Power versus Current curves
KOH	Potassium hydroxide
LP	Low pressure
MACE	Metal-assisted chemical etching
MEMS	Micro-Electro-Mechanical Systems
NC	Nanocrystal
NL	Neutral/Brush layer
NP	Nanoparticle
NW	Nanowire
PC	Polycrystal
PCB	Printed circuits board
PE	Plasma enhanced
PEEK	Polyether ether ketone
PGMEA	Propylene glycol methyl ether acetate
PID	Proportional-Integral-Derivative controller
PMMA	Poly(methyl Methacrylate)
PS	Polystyrene
PSA	Pressure sensitive adhesive
RF	Radio Frequency
RIE	Reactive ion etching
RT	Room temperature
RTA	Rapid thermal annealing
RTG	Radioisotope thermoelectric generator
SC	Single crystal
SEM	Scanning electron microscopy
SL	Superlattice
SoD	Spin on Dopant
SOI	Silicon on Insulator
STEM	Scanning transmission electron microscopy
TDTR	Time-domain thermoreflectance

TE	Thermoelectric	
TEG	Thermoelectric generator	
TEM	Transmission electron microscopy	
TEOS	Tetraethoxysilane	
TER	Thermoelectric refrigerators	
TF	Thin film	
TLM	Transmission line method	
UAB	Autonomous University of Barcelona	
UV	Ultra violet light	
VLS	Vapor-liquid-solid method	
YSZ	Yttria-Stabilized Zirconia	

List of symbols

α_{BCP}	Ratio of molecular weight	
α	Thermal diffusivity	m^2/s
χ	Flory-Huggins parameter	
ϵ	Lattice strain	
η	Efficiency	
γ	Grüneisen parameter	
ι	Interaction energy	J
κ_B	Boltzmann constant	J/K
κ	Thermal conductivity	$W/m \cdot K$
λ	Mean free path	m
μ	Charge carrier mobility	$m^2/V \cdot s$
ω	Angular frequency	rad/s
Φ	Porosity	
ϕ	Heat flow in Laplace space	W
Π	Peltier coefficient	V
ρ_C	Contact resistivity	$\Omega \cdot m^2$
ρ	Electrical resistivity	$\Omega \cdot m$
σ	Electrical conductivity	S/m
τ	Relaxation time	s
θ	Temperature in Laplace space	K
$\varphi_{Harvesting}$	Specific harvesting power generation capacity	$W/m^2 \cdot K^2$
φ	Specific power generation capacity	$W/m^2 \cdot K^2$
A	Area	m^2
C_v	Specific heat capacity at constant volume	$J/kg \cdot K$
C_p	Specific heat capacity at constant pressure	$J/kg \cdot K$

COP	Coefficient of performance	
C	Thermal capacitance	J/K
D	Probe distance in 4-probe measurements	m
d	Diameter	m
E	Energy	J
e	Electron charge	C
F_{BCP}	Electron scattering factor	
F_G	Geometrical factor	
F_{ph}	Phonon scattering factor	
f_{th}	Thermal gradient fraction	
f	Relative volume fraction	
G	Thermal conductance	W/K
h_P	Planck constant	J · s
h	Heat transfer coefficient	W/m^2·K
I_{SC}	Short circuit current	A
I	Current	A
K	Thomson coefficient	V/K
L_T	Transfer length	m
L	Length	m
l	Period	m
m^*	Effective mass	kg
M	Molecular weight	kg
N	Degree of polymerization	
n	Electron carrier concentration	1/m^3
P_{max}	Maximum power	W
P	Power/Heat flow	W
p	Hole carrier concentration	1/m^3
Q	Heat flow	W
R_C	Contact resistance	Ω
R_{int}	Internal resistance	Ω
R_{load}	Load resistance	Ω
R_S	Sheet resistance	Ω
R	Electrical resistance	Ω
S	Seebeck coefficient	V/K
s	Laplace variable	1/s
TCR	Temperature coefficient of resistance	1/K
T	Temperature	K

t	Thickness	m
V_{OC}	Open circuit voltage	V
V	Voltage	V
W	Width	m
zT	TE figure of merit	
Z	Dimensional figure of merit	1/K

List of Figures

1.1 Waste heat in global economy and temperature distribution of the waste heat. . . . 6
1.2 Scheme of the thermocouple. . . . 7
1.3 Heat-to-power and power-to-heat module schemes. . . . 9
1.4 Thermoelectric properties versus carrier concentration. . . . 13
1.5 Figure of merit of n- and p-type materials reported in the literature. . . . 15
1.6 Abundance in Earth's crust of the n- and p-type TE materials reported in the literature. . . . 17
1.7 Examples of different silicon nanostructuring strategies to reduce κ_{ph} . . . 18
1.8 Schemes of the typical vertical π-type and planar TEGs. . . . 22
1.9 Efficiency of TEGs and conventional engines versus power. . . . 24
1.10 Examples of µTEGs extracted from the literature. . . . 25
1.11 Theoretical plot of the different phases of a diblock copolymer . . . 26
1.12 Experimental plot of the miscible and immiscible regions in blends of diblock copolymers. . . . 29

2.1 Schemes of the two photolithography techniques used in this work. . . . 32
2.2 Schemes of the etching profiles obtained through dry and wet mechanisms. 34
2.3 Schemes of the lift-off and patterning processes. . . . 36
2.4 Scheme of the galvanic displacement with surfactant and organic liquid addition on the area of reaction. . . . 37
2.5 Scheme of the CVD-VLS process. . . . 38
2.6 Scheme of the thermally driven diffusion process of a lamellar BCP. . . . 40
2.7 Scheme of the nanostructuration of a Si thin film using block copolymers. 41
2.8 Scheme of the 4 probe method. . . . 44
2.9 Scheme of the transmission line method (TLM) characterization. . . . 46
2.10 Scheme of the typical device used for 3ω characterization. . . . 47
2.11 Scheme of the Frequency-domain thermoreflectance (FDTR) technique. . 49
2.12 Scheme of the bridge device. . . . 51
2.13 Image of a bridge device with a membrane and the corresponding thermal circuit of the system. . . . 54
2.14 Example plots of the two thermal states needed to calculate T_{Laser} with the bridge/laser method. . . . 55
2.15 Images of the TCR characterization setup. . . . 56
2.16 Images of the thermoelectric power characterization setup. . . . 57

3.1 Schemes of the 4X type µTEG for Si NWs. . . . 64
3.2 Optical images of the 4X and Parallel types of µTEGs. . . . 65

3.3 Scheme of the fabrication process for the 4X and Parallel devices for Si NWs. 66
3.4 Microscope images of the KOH etching process optimization of the device Si under the membranes. 68
3.5 SEM images of NWs chip after etching the supporting beams with FIB. . 69
3.6 Plots of the TCR measurement process. 69
3.7 Plots of V_{OC} and Seebeck as a function of the temperature gradient and hotplate temperature. 70
3.8 Comparison of the Seebeck coefficient of this work for NWs with examples of NWs from the literature. 71
3.9 Optical images of the four different platforms of a 4X device with NWs. . 72
3.10 Voltage and power vs current measured in a 4X chip on each of the four platforms. 72
3.11 Open circuit voltage, internal resistance and maximum power for the different platform designs as a function of the hotplate temperature. 73
3.12 Voltage and power versus current in a Parallel µTEG as a function of temperature and the number of platforms connected in series. 74
3.13 V_{OC}, P_{max}, R_{int} and ΔT of the Parallel µTEG at different temperatures as a function of the number of platforms in series. 75
3.14 V_{OC}, P_{max}, R_{int} and ΔT of the Parallel µTEG at different temperatures under forced convection (1.3 m/s). 76
3.15 Optical images of the platforms with microbeams and results of the conductance characterization. 78
3.16 Plots of the thermoelectric generation in harvesting mode of three platforms with different number of microbeams. 79
3.17 Comparison of the thermoelectric generation of three platforms with different number of microbeams at 250°C. 79

4.1 Scheme of the complete integration process of the heat sink into the µTEG. 82
4.2 Image of the pick and place setup used for heat sink integration. 83
4.3 Images of the optimized adapter integration with both thermal pastes. . . 84
4.4 COMSOL simulations results for the µTEG with and without heat sink. . 86
4.5 Schemes of the heat flow in the Bare chip, Chip with Si adapter and Chip with Si adapter and heat sink, with the equivalent thermal circuits. 87
4.6 $f_{th}^{HS}/f_{th}^{Bare}$ versus $R_{\mu TC}$ and R_h^{HS} and for different R_h^{Bare}/R_h^{HS} ratios. . . . 89
4.7 Increase factors obtained in different chips after adapter and heat sink integration for both thermal pastes. 91
4.8 Voltage and power vs current of a Parallel µTEG across the three stages of the heat sink integration. 92
4.9 Voltage and power vs current in a parallel chip under free and forced convection. 92
4.10 V_{OC} versus air flow velocity at different hotplate temperatures. 93
4.11 V_{OC}, P_{max}, P_{max}/A and ΔT versus hotplate temperature during all the stages of the heat sink integration under free and forced convection. . . . 94
4.12 P_{max} versus ΔT in the µTEG during all the heat sink integration stages. 95
4.13 V_{OC}, P_{max} and ΔT versus hotplate temperature across the different stages of the heat sink integration (microbeams). 96
4.14 Improvement of V_{OC} of µTEGs with 3 and 5 microbeams throughout the integration of the heat sink. 97

4.15 Comparison of R_{int}, V_{OC} and P_{max} of two Parallel µTEGs with NWs and microbeams versus number of platforms connected in series before (left) and after (right) heat sink integration. 98
4.16 Comparison of P_{max}/A versus ΔT of this work µTEGs (NWs and microbeams) with the current state-of-the-art of µTEGs based on Si. 99
4.17 P_{max} and ambient temperature of a NWs-based Parallel-type µTEG measured continuously during 168 h at hotplate temperatures of 150 and 250°C. 101
4.18 P_{max} and V_{OC} of a NWs-based Parallel-type µTEG during 1000 h of continuous operation at different hotplate temperatures. 102
4.19 $P_{max}/\Delta T^2$ and R_{int} of a NWs-based TEG during 1000 h of continuous operation at different hotplate temperatures. 102
4.20 STEM and EDS measurements of an as grown Si NW and a NW exposed during 168 h to 250°C. 103
4.21 Thickness of the oxides in the as-grown Si NW and in the degraded NW. 104
4.22 $P_{max}/\Delta T^2$ and R_{int} of a microbeams-based TEG for 120 h of continuous operation at 250°C. 105
4.23 V_{OC} transients and hotplate temperature of a µTEG. 106
4.24 Detailed view of V_{OC} peaks after heating and cooling in transient cycles on a Parallel NWs-based µTEG. 107
4.25 P_{max} transients of a µTEG. 107
4.26 Comparison of V_{OC} transients at 200°C versus voltage ranges needed by DC-DC boosters. 108
4.27 Layout of the 2x2 array of Parallel chips hosting microbeams-based µTEGs. 109
4.28 Scheme of the 2x2 integration design. 110
4.29 Scheme of the multi stack structure used to ensure good thermal contact between the Si adapters and the heat sink. 110
4.30 Pictures of the 2x2 array of µTEGs on the PCB before and after the integration of the 4 adapters and welding of the Pt100. 111
4.31 Setup used for the characterization of the 2x2 integrated TEG with heat sink. 112
4.32 P_{max} and V_{OC} at different heat sink integration stages versus hotplate temperature (2x2 TEG). 113
4.33 Voltage and power versus current measured on the 2x2 TEG based on Parallel µTEGs with microbeams under free and forced convection. 113

5.1 Example SEM images of lamellar and cylindrical BCPs self-assembled in free surface. 118
5.2 Thickness of the deposited BCP versus spinning velocity. 120
5.3 SEM images of self-assembled BCP from Arkema and intermediate blends. 121
5.4 SEM images of two different PS-C35 homopolymer-BCP blends. 122
5.5 SEM images of three different C80-C35 BCP-BCP blends. 123
5.6 Tilted cross-section SEM images of the Ar/O_2 RIE of L37 BCP samples. . 125
5.7 Plots of the measured remaining PMMA, PS and brush thickness versus attack time with the Ar/O_2 RIE. 126
5.8 SEM images of the Ar/O_2 RIE of C35 BCP. 127
5.9 SEM images of the PMMA wet etching route of C35 BCPs 128
5.10 Optimization of the mixed Bosch process RIE to obtain a completely anisotropic attack. 130
5.11 SEM images of SOI samples with lamellar BCPs etched with the mixed Bosch process. 131

5.12 Plots of the etched Si, remaining PS and Si neck size versus RIE time with the mixed Bosch RIE in L37 BCPs. 132
5.13 SEM images of the pattern transfer of cylindrical BCPs into Si. 133
5.14 Plots of the etched Si and hole diameter versus RIE time with the mixed Bosch RIE in cylindrical C35(50%)-C80(50%) BCPs. 133
5.15 SEM images of the pattern transfer of the optimal BCPs in the final 50 nm thick SOI samples. 134
5.16 Pictures of 1x1 cm^2 chips throughout the SoD cleaning process to dope 50 nm thick Si films. 135
5.17 Resistivity and doping concentration obtained with SoD versus annealing temperatures. 136
5.18 Comparison of doping densities of 50 nm thick Si films in different batches of chips doped with SoD at 900°C and 850°C. 137
5.19 In-depth doping in SOI thin films obtained by GDOES. 138
5.20 Wafer-scale doping in SOI thin films obtained with SoD. 138
5.21 Carrier density and resistivity of an intrinsic N-type bulk Si wafer doped by SoD at 1100°C. 139
5.22 SEM images of a non-doped and a doped 50 nm thick Si film with the same cylindrical nanostructuration with a period of $\sim$ 57 nm. 140
5.23 Examples of the transfer of nanostructured patterns into a COMSOL model. 140
5.24 Resistance increase and geometrical factors of cylindrical C35(50%)-C80(50%) BCPs versus etched depth. 141

6.1 COMSOL simulations of the 3ω device design. 146
6.2 Scheme of the main fabrication steps of the 3ω chip. 147
6.3 Optical and SEM images of the 3ω device after wafer-scale fabrication. . . 148
6.4 SEM images of the 3ω chip after wet etching of the PMMA cylinders and subsequent pattern transfer into Si using the PS mask. 149
6.5 Schemes of the three main routes used to control the KOH droplet and perform the etching at temperatures > RT. 150
6.6 Optical images of three suspended membranes with different PECVD Si_3N_4 stress compensation. 151
6.7 Optical images of a suspended membrane with Si_3N_4 support and nanostructured Si. 152
6.8 Pt heater resistance versus hotplate temperature in the 3ω steady state measurements. 153
6.9 Thermal conductance and conductivity of the nanostructured films versus temperature. 154
6.10 Thermal conductivity at RT of the Si film as a function of the etched depth. 154
6.11 SEM and optical images of membrane release in SOI samples with the BOE approach. 156
6.12 Scheme of the fabrication process of the thermoreflectance device. 157
6.13 SEM images of the final 15 µm long membranes with gold transducer and frame and different etched depths. 158
6.14 Scheme of the boundary conditions applied to the thermoreflectance device in the COMSOL model. 159
6.15 COMSOL simulations showing the transducer temperature with time. . . 160
6.16 Phase shift versus frequency obtained with COMSOL simulations and the subsequent curves using the thermal model. 161

6.17 Optical images of two bridge devices with nanostructured Si membranes deposited on top. . . . 163
6.18 Images of the setup used for membrane transfer. . . . 163
6.19 Representative plots of heater resistance versus temperature in bridge devices, together with the dR_0/dT calculations. . . . 165
6.20 Plots of the calculated beam and sample conductance values. . . . 165
6.21 COMSOL simulation results of the temperature profile of a membrane with different rotations. . . . 166
6.22 Thermal conductivity measured with the bridge method versus temperature for bare 50 nm thick films to fully etched samples with the 57 nm cylindrical pattern by the bridge method. . . . 166
6.23 Sequence of optical images showing the laser heating at different positions along a 50 nm-thick Si membrane. . . . 167
6.24 $\Delta T^{Side}_{Laser-S}$ versus laser power observed on both platforms at different measurement positions. . . . 168
6.25 Example plots of $\Delta T^{Side}_{Laser-S}/P_{Side}$ versus laser beam position on the membrane. . . . 169
6.26 Thermal conductivity versus temperature for 50 nm thick films with different etching depths. All films are nanostructured with 57 nm pitch cylindrical patterns. Thermal conductivity measurements do not include the thermal contact resistances. . . . 170
6.27 Example STEM images of two films. . . . 171
6.28 κ and F_{ph} versus the t_H/t thickness ratio, thickness without holes and etched depth. . . . 172

7.1 Example layouts of µTEGs with nanostructured films. . . . 176
7.2 Scheme of the wafer-level fabrication steps for µTEGs based on nanostructured Si thin films. . . . 177
7.3 SEM images of the Si nanostructuring within the µTEGs. . . . 178
7.4 Optical images of a fully fabricated µTEG with nanostructured TE regions and suspended platforms. . . . 179
7.5 V_{OC} versus time and hotplate temperature on a µTEG with bare 50 nm thick Si under different convection regimes. . . . 180
7.6 Average V_{OC} generation versus hotplate temperature of a µTEG with fully etched holey Si film under free and forced convection. . . . 181
7.7 V_{OC} as a function of hotplate temperature and the nano-patterning of the thin Si film compared with the NW-based µTEGs presented in this thesis. 182
7.8 Seebeck characterization of the fully etched holey Si films with a period of 57 nm. . . . 183
7.9 Seebeck coefficient measurement repeatability for fully etched holey Si films with a period of 57 nm. . . . 184
7.10 Comparison of Seebeck coefficient versus temperature for the nanostructured TE films and the Si NWs in this thesis against literature values. . . 184
7.11 Figure of merit for the 57 nm pitch patterned Si thin films as a function of the etched depth. . . . 186
7.12 SEM images of the as-grown Si-Ti interface, after RTA at 700°C and after annealing at 450°C. . . . 187
7.13 Scheme of the TLM chip and I-V and R vs distance curves. . . . 187
7.14 Si-Ti contact resistivity and Si sheet resistance for different thermal treatments. . . . 188

7.15 Comparison of Si-Ti contact resistivity of this work with the literature. . 189

A.1 Schemes of the typical DSA by chemo- and grapho-epitaxy. 199
A.2 SEM images of the optimization of the guiding pattern fabrication for BCP alignment. 201
A.3 SEM images of a guiding patter with degraded BCP. 203
A.4 SEM images of a 600-650 nm wide GP with aligned BCPs (L28 and L37). 203
A.5 SEM images of a 400-450 nm wide GP with aligned BCPs (L28 and L37). 204
A.6 SEM images of a $\sim$ 200 nm wide defective GP with aligned L37 BCP. . . 205

B.1 SEM and optical images on membrane suspension in SOI samples with KOH using Si_3N_4 and HfO_2 as protection layers. 208

C.1 Temperature and voltage COMSOL simulations with different adapter pillar materials. 209
C.2 Schemes and images of the initial YSZ adapter piece designs. 210
C.3 Schemes and images of the second YSZ adapter piece design. 211
C.4 Schemes of the Pyrex adapter piece designs. 212

D.1 Initial FDTR results on a bare Si film membrane. 216
D.2 Thinning of 88nm-thick SOI wafers. 216

List of Tables

1.1 Summary of the main application fields of the IoT. 4
1.2 Summary of the main environmental energy sources, with examples of harvesters and their corresponding power generation ranges. 5
1.3 Comprehensive summary of the different types of Si and Si-based structures reported in the literature. 20

2.1 Optimized parameters for the growth of Si NWs [124]. 39

4.1 Performance of a µTEG at the different stages of heat sink integration at 250ºC under different convection regimes. 93
4.2 Comparison of the specific power generation capacity and the specific *harvesting* power generation capacity of different µTEGs reported in the literature and this work µTEGs with heat sink. 100

5.1 Properties of the brush layers and block copolymers used in this thesis. . 118
5.2 Theoretical and experimental periods and diameters of several lamellar and cylindrical BCPs used in this thesis. 121
5.3 Optimized parameters for the PMMA etching in an ICP type RIE machine 125
5.4 Optimized parameters for Si etching in an ICP type RIE (Alcatel AMS-110 DE). 130
5.5 Increment of resistance, geometric factor and scattering factor of Si thin film decorated with lamellar patterns. 142

7.1 Different μTEG designs compared in Figure 7.7. 182

Contents

Acknowledgments i

Abstract iv

Resumen vi

Scope of the thesis ix

Nomenclature xv

List of Figures xxii

List of Tables xxiii

Background and Methods 1

1 Introduction 3
- 1.1 Motivation . . . 3
  - 1.1.1 Internet of Things . . . 3
  - 1.1.2 Harvesting environmental sources . . . 4
- 1.2 Thermoelectric effect . . . 7
  - 1.2.1 Thermoelectric efficiency . . . 8
- 1.3 Thermoelectric materials . . . 11
  - 1.3.1 State of the art of thermoelectric materials . . . 14
  - 1.3.2 Si based thermoelectric materials . . . 17
- 1.4 Thermoelectric devices . . . 21
  - 1.4.1 Thermoelectric generators . . . 21
    - 1.4.1.1 µ-Thermoelectric generators . . . 23
- 1.5 Block copolymers . . . 26
  - 1.5.1 Blends . . . 28

2 Experimental methods 31
- 2.1 Micro- and Nano-fabrication . . . 31
  - 2.1.1 Photolithography . . . 31
  - 2.1.2 Thin film deposition . . . 32
  - 2.1.3 Metallization . . . 33
  - 2.1.4 Etching . . . 34

2.1.5 Thermal processing . . . 35
2.1.6 Doping . . . 35
2.1.7 Lift-off and patterning . . . 36
2.1.8 Nanowire growth . . . 37
2.1.8.1 Galvanic displacement . . . 37
2.1.8.2 CVD-VLS growth . . . 38
2.1.9 PS-b-PMMA . . . 39
2.1.10 Thin film nanostructuring . . . 41
2.1.11 Encapsulation and wire-bonding . . . 42
2.2 Structural characterization methods . . . 42
2.2.1 Scanning electron microscopy . . . 42
2.2.2 Focused ion beam . . . 42
2.2.3 Transmission electron microscopy . . . 42
2.2.4 Ellipsometry . . . 43
2.2.5 Spectroscopic reflectometry . . . 43
2.2.6 Confocal microscope . . . 43
2.2.7 Glow-discharge optical emission spectroscopy . . . 43
2.3 Electrical characterization . . . 44
2.3.1 4-probe method . . . 44
2.3.2 Transmission line method . . . 45
2.4 Thermal characterization . . . 46
2.4.1 3ω steady state . . . 46
2.4.2 Thermoreflectance . . . 48
2.4.3 Bridge method . . . 51
2.4.3.1 Bridge method with laser heating . . . 53
2.4.4 Temperature coefficient of resistance . . . 56
2.5 Thermoelectric characterization . . . 57
2.5.1 Seebeck coefficient . . . 58
2.5.2 Thermoelectric power . . . 58

Micro-thermoelectric generators based on silicon nanowires and microbeams 61

3 Characterization of micro-thermoelectric generators 63
3.1 Micro-thermoelectric generators design . . . 63
3.1.1 Device fabrication . . . 65
3.2 Thermoelectric characterization . . . 69
3.2.1 Nanowires . . . 69
3.2.1.1 Test mode . . . 69
3.2.1.2 Harvesting mode . . . 71
3.2.2 Microbeams . . . 77
3.3 Chapter conclusions . . . 80

4 Heat sink integration in micro-thermoelectric generators 81
4.1 Heat sink integration . . . 81
4.1.1 Integration procedure . . . 81
4.1.2 Simulations and thermal model . . . 85
4.2 Thermoelectric characterization with heat sink . . . 90
4.2.1 Nanowires . . . 90

4.2.2 Microbeams . . . 95
4.3 Long term characterization . . . 100
4.3.1 Nanowires . . . 101
4.3.1.1 Degradation study . . . 103
4.3.2 Microbeams . . . 104
4.4 Transient measurements . . . 105
4.4.1 Nanowires . . . 106
4.5 2x2 Thermoelectric generator . . . 109
4.5.1 Device design . . . 109
4.5.2 Integration process . . . 111
4.5.3 Thermoelectric characterization . . . 112
4.6 Chapter conclusions . . . 114

Thermoelectric characterization of silicon thin films nanostructured with block copolymers 115

5 Silicon thin films nanostructured with block copolymers 117
5.1 Block copolymer self-assembly . . . 117
5.1.1 Block copolymer blends . . . 120
5.2 Pattern transfer on Silicon . . . 124
5.2.1 PMMA etching . . . 124
5.2.2 Silicon etching . . . 129
5.3 Doping of silicon thin films with Spin on dopant . . . 135
5.3.1 Electrical characterization of nanostructured silicon thin films . . . 139
5.4 Chapter conclusions . . . 142

6 Thermal characterization of nanostructured silicon thin films 145
6.1 3ω steady state . . . 145
6.1.1 3ω device design . . . 145
6.1.2 3ω device fabrication . . . 146
6.1.3 3ω steady state characterization . . . 152
6.2 Thermoreflectance . . . 155
6.2.1 Membrane release . . . 155
6.2.2 Thermoreflectance device fabrication . . . 157
6.2.3 Simulations and thermal model . . . 159
6.3 Bridge method . . . 162
6.3.1 Bridge method devices and membrane transfer . . . 162
6.3.2 Bridge method characterization . . . 164
6.3.3 Bridge method with laser heating characterization . . . 167
6.4 Chapter conclusions . . . 173

7 Micro-thermoelectric generator based on nanostructured thin films 175
7.1 Device design . . . 175
7.1.1 Device fabrication . . . 176
7.2 Open circuit voltage characterization . . . 180
7.3 Seebeck coefficient characterization . . . 183
7.4 Figure of merit . . . 185
7.5 Ti-Si contact resistance . . . 186
7.6 Chapter conclusions . . . 189

8 Conclusions **191**

Scientific contribution **198**

A Directed self-assembly of block copolymers **199**
A.1 Guiding pattern fabrication 200
A.1.1 DSA of lamellar block copolymers 202

B Release of membranes using topside KOH etching **207**

C Adapter piece redesign **209**
C.1 Simulations 210
C.2 Fabrication trials 210

D Ongoing work on nanostructured films **215**
D.1 FDTR characterization 215
D.2 Thermoelectric generator with optimized Ti-Si contact 217

Part I

Background and Methods

Chapter 1

Introduction

1.1 Motivation

Over the past three centuries, the use of energy and electronic devices has grown exponentially. The Industrial Revolution sparked energy consumption through steam and coal-powered machinery, while the 20th century saw electricity become widespread. In recent decades, the proliferation of electronic devices has driven unprecedented energy demand, with global electricity consumption rising sharply to power data centers, smart grids, and connected devices, shaping a highly digital and energy-intensive world. In this context, the Internet of Things stands out as one of the most important emerging technologies, encompassing a large number of electronic devices and significant energy consumption, raising concerns about their power supply.

1.1.1 Internet of Things

The concept of the Internet of Things (IoT) alludes to a collective network composed of embedded sensors that have the ability to communicate between themselves or with the cloud through an internet connection. These networks have become essential in our day-to-day lives due to their joint ability of monitoring the environment and sending the data in real-time, with the consequent enhancement of decision-making processes and the optimization of autonomous systems. Today, the range of applications of the IoT spans through several fields, covering the Machine-to-Person, the Autonomous Systems and the Smart Environment families. Table 1.1 shows different examples of the main areas of application, among which, according to *Transforma Insights* [1], the fields of Transportation & Storage, Retail & Wholesale, Electricity, Gas and Steam and government-related demands were the main ones in terms of recurring revenue in the period 2022-2023, each individually exceeding the 10,000 million USD threshold.

The number of deployed IoT systems highlights their increasing importance in modern society. In 2023, the number of interconnected devices added up to 15.9 billion, and current trends project this figure to exceed 39 billion by the 2030s [2]. The rapid expansion is largely driven by continuous advancements in the fabrication and miniaturization of Micro-Electro-Mechanical Systems (MEMS), as well as reductions in the power requirements of sensors. These developments have enabled the mass production and deployment of IoT nodes. However, this optimistic trend could decline if the issue of power supply

Table 1.1: Summary of the main application fields of the IoT, with specific examples for each case. Adapted from [1], [2], [3].

	Application	Examples
	Healthcare	Remote patient monitoring with wearable sensors and smart medical devices. Hospital asset management with enhanced medical equipment tracking.
	Food & Agriculture	Precision farming with soil moisture, nutrient level and temperature sensors. Food supply chain tracking to monitor the conditions of the food.
	Transport	Fleet management with vehicle and fuel usage tracking. Smart traffic systems to provide real-time congestion data.
	Cities	Environmental monitoring to assess air quality, noise levels or pollution. Smart city lighting systems based on pedestrian or vehicle presence.
	Industry	Predictive maintenance with incorporated sensors. Supply chain optimization with inventory tracking. Enhanced safety for the workers thanks to improved risk tracking in the facilities.
	Wearables	Fitness monitoring with sweat, calories, heart-rate sensors. Smart watches.
	Retail & Wholesale	Real-time inventory management. Personalized marketing. Smart shelves with real-time monitoring of stock in the shops.
	Domotics	Smart temperature and light control in homes based on occupancy of rooms. Enhanced security systems with real-time monitoring and alerts.

is not adequately addressed. Batteries remain the primary power source for IoT devices, but their frequent recharging and disposal pose significant cost and environmental challenges. This concern is particularly critical in some of the most promising IoT application areas (namely Industry, Energy and Transportation [3], [4]) where sensor networks are often installed in remote and harsh environments, making regular maintenance impractical. Thus, alternative energy sources must be explored in order to supply power more efficiently.

1.1.2 Harvesting environmental sources

Environmental sources offer an alternative that can fulfill both the sustainability and long-term autonomy requirements of the IoT that batteries fail to address. The constant miniaturization of sensor and communication systems is shifting the current needs of commercial devices (> 1 mW) towards lower sub-miliwatt ranges, with minimum powers of about tens of µW [5], [6]. The range between 10 and 100 µW/cm^2 could then be

Table 1.2: Summary of the main environmental energy sources, with examples of harvesters and their corresponding power generation ranges. Adapted from [4], [7], [8].

	Source	Harvester	Power range
	Thermal	Thermoelectric generator	$<100\,\mu W/cm^2$ @ $<5\,°C$
	Solar	Photovoltaic cell	$<100\,\mu W/cm^2$ @ indoor $<100\,mW/cm^2$ @ outdoor
	Wind	Micro-turbine	$<35\,\mu W/cm^2$ @ $<1\,m/s$ $<3.5\,mW/cm^2$ @ $<8.4\,m/s$
	Mechanical vibration	Piezoelectric generator	$<4\,\mu W/cm^3$ @ human-Hz $<800\,\mu W/cm^3$ @ machine-kHz
	Ambient radiofrequency	RF Antenna	$<1\,\mu W/cm^2$

considered a suitable objective for the power supply of low-power sensors. In this context, MEMS technology offers the possibility of fabricating energy harvesters that are better suited in size for IoT sensors, while also requiring less maintenance. This reduces long-term costs and extends device lifespan. When combined with an abundant environmental source, we have a major candidate to bring the IoT forecasts into reality. Table 1.2 summarizes the main energy sources available and provides some examples of harvesters and their power ranges.

Among the showcased environmental sources, heat is one of the most prevalent due to its ubiquitous presence as a byproduct in industrial, transportation and energy-related processes. *A. Firth et al.* [9] pointed out that approximately 72% of global energy is lost during conversion processes, with heat losses accounting for 52% of the total input energy consumed worldwide. Specific values of waste heat compared to input energy in different economic areas can be seen in Figure 1.1a, together with the potential minimum percentage of losses to which we should aim from a theoretical perspective [9], [10]. Therefore, it is clear that the major contributor to environmental contamination resulting from energy losses is waste heat. Thus, recovering part of it is mandatory to reduce its environmental footprint [11].

Heat loss can be classified into three categories depending on its temperature (T): high temperature ($>300°C$), medium temperature (100-300°C) and low temperature ($<100°C$). As seen in Figure 1.1b, medium and low temperature waste heat accounts for about 94.8% of heat lost worldwide. In these ranges, possible recovery mechanisms include heat pumps, condensing water heaters, and Thermoelectric generation for low T; and organic Rankine cycle, Kalina cycle, phase change materials, and Thermoelectric generation for medium T [12], [13].

Considering all of the above, several economic sectors (particularly Transportation, Industry, Buildings, and Power generation) are experiencing rapid IoT expansion due to its strong potential for process optimization and cost reduction. At the same time, these sectors suffer significant energy losses in the form of waste heat, much of it at temperatures below 300 °C. Hence, thermoelectric generators (TEG) stand out as a promising solution to recover a significant amount of lost heat and convert it to electricity, which could be

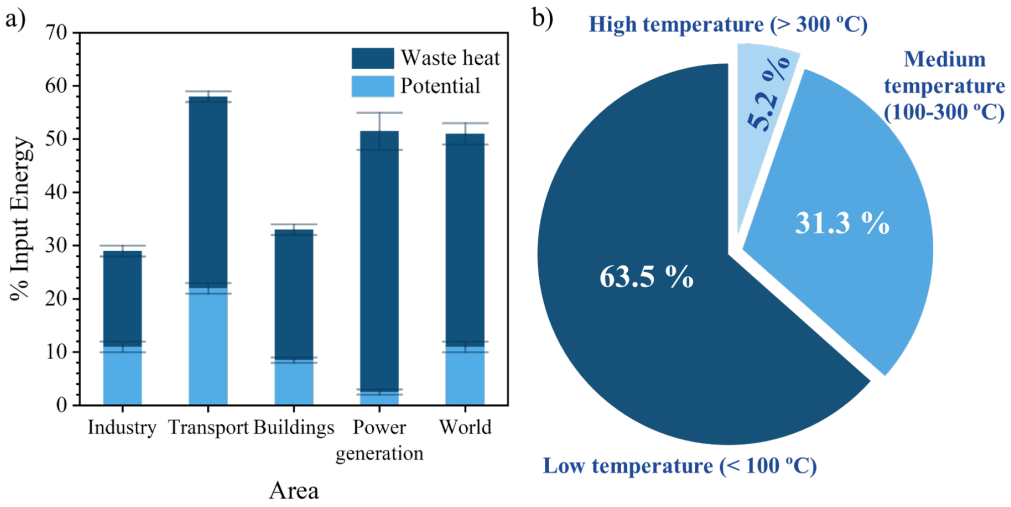


Figure 1.1: a) Comparison of waste heat relative to input energy across different economic sectors and in the global economy. Light blue areas indicate the theoretical minimum energy losses achievable in each sector. b) Distribution of waste heat across different temperature ranges in 2014 [9]. Adapted from [9], [10]

used to power future IoT nodes in these industries [14], [15].

However, commercial thermoelectric generators are still scarce in these areas. The most common thermoelectric modules to date are based on Bismuth Telluride (Bi_2Te_3) pellets, which have great thermoelectric properties but fall behind when it comes to IoT compatibility. Both Bi and Te are scarce and toxic materials that cannot be mass-produced to keep up with the growing pace of IoT node deployment [16]. Therefore, alternative materials should be explored to fabricate thermoelectric generators that could generate enough power to fulfill the IoT needs and, at the same time, be sustainable and compatible with mass-production in CMOS-like processes [17]. In this way, the economic and environmental costs will be reduced and, even, single platforms with integrated sensor-TEG devices could potentially be fabricated.

Since *A. I. Boukai et al.* and *A. I. Hochbaum et al.* showed in 2008 that nanostructuring silicon can effectively tailor its thermoelectric properties, a new interesting field has opened for study [18], [19]. Silicon is a low-cost, nontoxic and abundant material that is highly compatible with industrial processes and large-volume production, while also excelling in miniaturization and integration capabilities. Therefore, if Si can be nanostructured in such a way that the patterning process is compatible with large-scale fabrication, it could become a promising solution to power the IoT nodes.

This thesis studies the potential of silicon as a thermoelectric material, thereby encompassing the nanostructuration and thermoelectric properties of Si, the exploration of technologies to integrate these structures into thermoelectric generators, and the study of their generation capabilities. The introduction chapter provides a detailed overview of thermoelectric theory, state-of-the art in thermoelectric materials and devices, and the use of block copolymers for nanostructuring silicon.

1.2 Thermoelectric effect

Thermoelectricity is a term that refers to the conversion of temperature differences into electric potentials or vice versa, encompassing the three main effects in this field: Seebeck, Peltier and Thomson effects.

The origin of thermoelectricity dates back to the year 1821, when Thomas Seebeck discovered that a magnetic compass needle suffered deflection when placed near a junction of two materials exposed to different temperatures. However, it was not until 1823 when Hans Christian Ørsted correctly associated the needle deflection as a secondary effect of a current flowing through the materials. He found that the temperature difference generates an electrical current, which in turn produces a magnetic field that moves the needle. Thus, what was initially referred to as thermomagnetic effect was later more precisely defined as thermoelectric effect. Figure 1.2 shows a basic thermocouple device. Here, p- and n-type metal or semiconducting materials are electrically connected in series, while being thermally in parallel. The open circuit voltage generated is related to the temperature gradient by means of the Seebeck coefficient of both materials, leading to Equation 1.1:

$$\Delta V = (S_B - S_A)\,\Delta T \tag{1.1}$$

In this formula, the sign of the Seebeck coefficient of each material depends on the charge carriers that dominate its electric transport. Thus, n-type materials have a negative Seebeck coefficient while p-type have a positive one. In cases where a single thermoelectric material is placed between two temperatures, the equation is simplified to $\Delta V = -S\Delta T$, with the S sign following the same principle.

From an atomic point of view, the physical phenomenon that explains the movement of charge carriers from the hot side to the cold side is diffusion, driven by differences in kinetic energy. Carriers exposed to higher temperatures possess greater kinetic energy and move faster than those in colder ones, resulting in a net diffusive movement toward the cold end. Consequently, a voltage is induced in the material, which drives an electric current when the material is connected to a load.

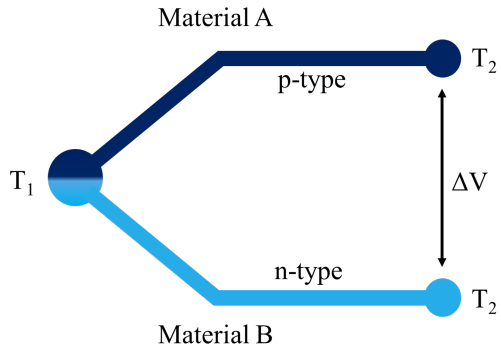


Figure 1.2: Scheme of the thermocouple. The electrical junction between material A and B, n- and p-type respectively, is exposed to a different temperature than the one on the ends of both materials. As a result, an electric potential proportional to the temperature gradient is generated across the terminals.

Later, in 1834, Jean Charles Athanase Peltier discovered the complementary of the Seebeck effect. He observed that heat could be generated or removed at the junction of the two materials depending on the direction of the current flowing through them. Equation 1.2 governs this effect, relating the amount of heat, Q, with the current flow by means of the Peltier coefficient, Π:

$$Q = (\Pi_A - \Pi_B)\, I \tag{1.2}$$

Lastly, in 1851, William Thomson (Lord Kelvin) predicted and later observed that reversible heat generation or absorption occurs when an electric current flows through a single material with a temperature gradient. This means that when charge carriers move from the hot to the cold side, heat is released. This is known as the positive Thomson effect. Conversely, when carriers flow from the cold to the hot side, heat is absorbed. As a result, Thomson effect is present in thermoelectric generators, but it is typically neglected in practical calculations. This effect follows Equation 1.3, where generated or absorbed heat is proportional to the electric current, I, the temperature gradient, ΔT, and the Thomson coefficient, K:

$$Q = KI\Delta T \tag{1.3}$$

Finally, the three thermoelectric effects are interrelated through the Thomson relations. The first Thomson relation connects the Thomson coefficient to the temperature dependence of the Seebeck coefficient. The second relates the Peltier and Seebeck coefficients, establishing a fundamental link between heat and charge transport in thermoelectric materials:

$$K = T\frac{dS}{dT} \tag{1.4}$$

$$\Pi = TS \tag{1.5}$$

1.2.1 Thermoelectric efficiency

To properly evaluate thermoelectric materials and devices, it is important to consider the efficiency of both heat-to-power and power-to-heat conversion mechanisms. Figure 1.3 shows the basic schemes of these mechanisms in two basic modules.

First, we need to define the heat transfer occurring on the hot side of the heat-to-power module. Neglecting the Thomson effect, as it is several orders of magnitude lower than the rest [20], we can divide the heat transfer into three components: the Peltier effect (from Equation 1.2, using the second Thomson relation to relate it to the Seebeck coefficient), half of the irreversible Joule heating (Equation 1.7), as only 1/2 of it goes towards the heat source, and the heat transfer through thermal conductivity (Equation 1.8).

$$Q_1 = \Pi_{TE} I = S_{TE} T_H I \tag{1.6}$$

$$Q_2 = -\frac{1}{2} R_{int} I^2 \tag{1.7}$$

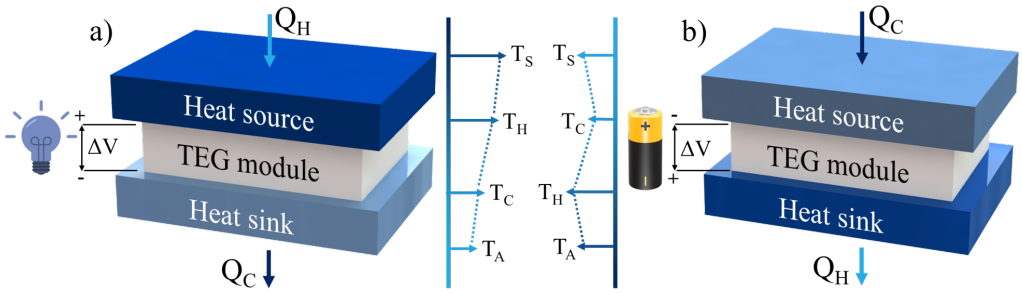


Figure 1.3: a) Basic scheme of a heat-to-power module, together with the temperature distribution along the device. b) Basic scheme of a power-to-heat module, together with the temperature distribution along the device. In both cases, S, H, C and A letters stand for source, hot, cold and ambient. An n-type material is considered to assign the signs of the voltage.

$$Q_3 = G_{TE}\Delta T_{TE} = k_{TE}\frac{A}{L}\Delta T_{TE} \tag{1.8}$$

In these equations, S_{TE}, R_{int}, k_{TE}, A, L and ΔT_{TE} are the Seebeck coefficient, the internal resistance, the thermal conductivity, the area and length of the module, and the temperature difference across the TE, which corresponds to $T_H - T_C$.

The power generated by this module is given by:

$$P_{TE} = I^2 R_{load} \tag{1.9}$$

We can define the efficiency of the heat-to-power conversion as the amount of power generated divided by the amount of heat transferred on the hot side:

$$\eta = \frac{P_{TE}}{Q_1 + Q_2 + Q_3} = \frac{P_{TE}}{Q_H} \tag{1.10}$$

The power can also be considered from a circuit theory point of view. The TE module is supposed to be connected to a load, and the optimal transferred power is found to be when $R_{load} = R_{int}$. At this point, the power is related to half of the open circuit voltage, which, at the same time, can be rewritten as a function of the Seebeck coefficient and the temperature gradient:

$$P_{TEmax} = \frac{V_{OC}^2}{4R_{int}} = \frac{S_{TE}^2 \Delta T_{TE}^2}{4R_{int}} \tag{1.11}$$

This leads to the recalculation of the efficiency using the maximum power and the aforementioned heat transfer equations:

$$\eta = \frac{S_{TE}^2 \Delta T_{TE}^2}{4R_{int}\left(S_{TE}T_H I - \frac{1}{2}R_{int}I^2 + k\frac{A}{L}\Delta T_{TE}\right)} \tag{1.12}$$

However, this analysis of the TEG efficiency assumes that the optimal conditions correspond to electrical load matching since, under these conditions, the transferred power is maximized. This assumption is valid only if the external thermal resistances are considered negligible. Otherwise, it becomes inaccurate because the load resistance value also affects the thermal management of the TEG through the Peltier and Joule effects, which can limit the temperature gradient (i.e. the contribution of the load resistance is not restricted to electrical behavior alone) [21]. When the heat source and sink temperatures are fixed and the external thermal resistances cannot be neglected, the maximum efficiency is obtained when [22]:

$$R_{Load} = R_{int}\sqrt{1 + ZT_m} \tag{1.13}$$

as long as ΔT is below a certain threshold [21]. Under these conditions, the maximum efficiency corresponds to:

$$\eta = \left(1 - \frac{T_C}{T_H}\right) \frac{\sqrt{1 + ZT_m} - 1}{\sqrt{1 + ZT_m} + \frac{T_C}{T_H}} = \eta_C \eta_{TE} \tag{1.14}$$

Here, we see that the overall efficiency depends on $\eta_C = (1 - T_C/T_H)$, the Carnot efficiency, which is the ideal maximum for any thermodynamic device in the conversion of heat into power, and η_{TE}, which reflects the influence of irreversible losses in thermoelectric conversion. In η_{TE}, T_m corresponds to the average temperature, $(T_H + T_C)/2$, while the Z factor is composed of the Seebeck coefficient, S, the electrical resistance, R, and the thermal conductance, G, of the module:

$$Z = \frac{S^2}{RG} \tag{1.15}$$

It is clear that this Z factor is of the utmost importance in the design of thermoelectric generators due to its role in heat-to-power conversion efficiency. Nevertheless, in this thesis, the simpler load-matching condition is considered the optimal operating state. In our case, given the ZT_m values of our structures, this assumption introduces errors below 6% compared to the load conditions of Equation 1.13.

Regarding the reverse mechanism, power-to-heat conversion, the efficiency can be calculated as the amount of heat ejected from the heat source divided by the total power used in the process of cooling. This factor is known as the Coefficient of performance (COP):

$$COP = \frac{Q_C}{P_{TE}} \tag{1.16}$$

The heat flux on the cold side of the module is composed of the same components as in heat-to-power conversion but with a negative sign on Equation 1.8, as in this configuration the heat transfer through thermal conduction goes towards the heat source:

$$Q_C = S_{TE} T_C I - \frac{1}{2} R_{int} I^2 - k \frac{A}{L} \Delta T_{TE} \tag{1.17}$$

In terms of energy balance, the amount of power used is:

$$P_{TE} = Q_H - Q_C = S_{TE}\Delta T I + R_{int} I^2 \tag{1.18}$$

Therefore, dividing the aforementioned Q_C by the power used, and after some manipulations, the maximum Coefficient of performance is:

$$COP = \left(\frac{T_C}{T_H - T_C}\right) \frac{\sqrt{1 + ZT_m} - \frac{T_H}{T_C}}{\sqrt{1 + ZT_m} + 1} \tag{1.19}$$

Again, we see that the Z parameter stands out as the main contributor to the efficiency of the thermoelectric module. Thus, strategies aimed at enhancing this parameter must be explored to enable more efficient thermoelectric energy conversion in practical devices. First, it should be noted that Equation 1.15 depends on three parameters: the Seebeck coefficient, which is intrinsic to the material itself, and the thermal and electrical resistances, which depend on both the material and the device geometry. On the device side, contact and internal resistances need to be optimized, minimizing associated loss mechanisms by ensuring optimum thermal and electrical interconnections. Once loss mechanisms are not considered, the Z factor can be reduced to:

$$z = \frac{S^2\sigma}{k} \tag{1.20}$$

This formula, known as the figure of merit of a thermoelectric material, is more commonly written as zT, becoming a dimensionless factor to evaluate the thermoelectric material performance at different temperatures.

1.3 Thermoelectric materials

The assessment of a material's suitability for thermoelectric applications is fundamentally based on the dimensionless figure of merit, zT. Observing Equation 1.20, it is evident that both Seebeck coefficient and electrical conductivity should be enhanced as much as possible, while the thermal conductivity should be reduced. The term $S^2\sigma$, referred to as the thermoelectric power factor, quantifies a material's capacity to convert a temperature gradient into electrical energy. It captures the combined influence of the Seebeck coefficient and electrical conductivity, where a high power factor indicates efficient voltage generation with minimal resistive losses. Furthermore, reducing the thermal conductivity results in a larger thermal gradient across the material, thereby increasing the potential for energy conversion. Consequently, a comprehensive analysis of S, σ and κ is essential to understand their interdependence and to maximize the figure of merit zT.

The electrical conductivity is a material property that quantifies its ability to conduct electric current. It can be expressed as the charge carrier density multiplied by their mobility as:

$$\sigma = e\left(n\mu_e + p\mu_h\right) \tag{1.21}$$

where e is the electron charge, n and p are the charge carrier concentrations for electrons and holes, and μ_e and μ_h stand for their respective electrical mobilities. In

semiconductors, the values of n and p are primarily determined by the amount and type of dopant atoms introduced into the material. Typically, charge transport is dominated by one of the carriers, simplifying the formula to only one carrier type. Carrier mobility, on the other hand, is related to how easily charge carriers (holes or electrons) move through a material when an electric field is applied. This property depends on scattering mechanisms, carrier concentration, and temperature.

The thermal conductivity is analogous to the electrical one, but its behavior is more complicated, as now two different contributions arise. The first relates to the propagation of lattice vibrations, which are described as phonons (quasi-particles representing the quantized normal modes of atomic vibrations within a crystalline lattice). These phonons are the primary heat carriers in ordered crystals. The phononic thermal conductivity, denoted as κ_{ph}, can be related to the phonon relaxation time, which represents the average time interval between successive scattering events within the lattice. A shorter relaxation time corresponds to a higher scattering rate, which in turn leads to reduced thermal conductivity. Relaxation time can be expressed as [23]:

$$\tau_{ph}^{-1} = \gamma^2 \epsilon^2 + \left(\frac{1}{\overline{M}} \right)^2 \Delta M^2 \tag{1.22}$$

where γ is the Grüneisen parameter that measures the strength of anharmonicity, ϵ is the lattice strain, and $\overline{M}$ and ΔM are the average atomic mass and the mass difference, respectively. Thus, both different types of lattice strains and point defects or interstitial atoms, which are associated to mass differences, will shorten the relaxation time, decreasing κ_{ph}. A simplified formula for κ_{ph} can also be obtained by considering a thin layer [24]:

$$\kappa_{ph} = \frac{1}{3} C_v v \lambda \tag{1.23}$$

where C_v is the specific heat capacity per unit volume, v is the sound velocity in the material and λ is the phonons mean free path. Again, we see that κ_{ph} does not depend on electrical properties and is mainly affected by the phonon scattering mechanisms in the lattice (by means of λ), opening different ways to enhance it.

The second contribution to the thermal conductivity, κ_e, is specifically related to electrical transport, as both holes and electrons can transfer heat. In this case, κ_e is directly related to the electrical conductivity of the material via the Wiedemann–Franz law:

$$\kappa_e = \frac{\pi^2}{3} \left(\frac{k_B}{e} \right)^2 \sigma T \tag{1.24}$$

In metals, Equation 1.24 dominates as they have quasi-free charge-carrying particles, whereas in the case of semiconductors the contribution of κ_e is around 1/3 of the total thermal conductivity when either the material is at high temperatures or it has high doping densities [25], [26]. In any case, κ_e is important as it is directly proportional to the carrier concentration of the material, imposing an upper limit on the amount of useful doping to optimize the correlation between electrical and thermal conductivity.

Lastly, the Seebeck coefficient is also composed of two different contributions associated with electrical, S_e, and phonon transport, S_{ph}. The electrical one is related to charge

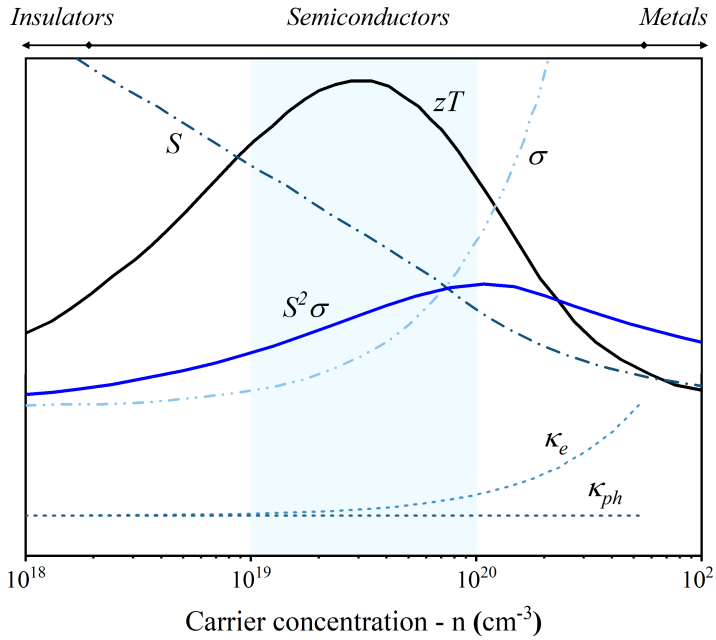


Figure 1.4: Relation between the main thermoelectric properties behavior with the carrier concentration on the material. In doted lines, electronic (κ_e) and phonon (κ_{ph}) thermal conductivities; in doted-dashed lines, electrical conductivity (σ), and Seebeck coefficient (S); in continuous lines, thermoelectric figure of merit (zT), and power factor ($S^2\sigma$). The optimal range in terms of zT is highlighted in light blue. Data taken from [29], [30]

carrier diffusion from the hot to the cold side due to the difference in kinetic energy on both sides. The second is a consequence of the phonon-carrier interactions and is known as the phonon-drag effect. In this case, the mechanical vibrations of the lattice, which travel from the hot to the cold side of the material, interact with the charge carriers and transfer their momentum to them. This effect is dominant at very low temperatures ($<$ 30 K), while it is negligible at higher temperatures [27]. As thermoelectric systems tend to work in environments above room temperature, the phonon-drag component of the Seebeck coefficient is usually discarded and only the electrical one is considered. This component of the coefficient is, for the case of metals or semiconductors with electronic parabolic bands [28]:

$$S_e = \frac{8\pi^2 k_B^2}{3eh_P{}^2} m^* T \left(\frac{\pi}{3n}\right)^{\frac{2}{3}} (1+R) \tag{1.25}$$

where $R = (\delta ln\lambda_s/\delta lnE)_{E_f}$, being λ_s the mean free path of the electrons, which is the average distance between two successive scatterings. If the scattering mechanisms are assumed to be independent of the energy, the term $(1+R) = 1$ in Equation 1.25. Therefore, S_e is proportional to m^*, the effective mass of the carriers, and inversely proportional to $n^{2/3}$, the carrier concentration.

Taking into account the aforementioned equations for the thermal and electrical conductivities and the Seebeck coefficient, a compromise in terms of the carrier concentration appears (see Figure 1.4). An increase in carrier concentration enhances electrical conduc-

tivity but, at the same time, worsens the Seebeck coefficient and increases κ_e. On the other hand, low carrier concentrations lead to higher Seebeck values and lower thermal conductivities, but at the cost of increasing electrical resistance, resulting in lower power generation. Thus, the TE figure-of-merit shows an optimal carrier density range between 10^{19} and 10^{20} cm^{-3}. The power factor, instead, has a small shift towards higher carrier concentrations, having a peak above 10^{20} cm^{-3}, as the thermal contribution is not considered here. These results show that semiconductors are the optimal materials for thermoelectric applications.

Regarding the temperature dependence of these properties, several effects can be observed. At higher temperatures, the electronic contribution to the Seebeck coefficient increases, while the phonon-drag component decreases due to the dominance of phonon-phonon interactions over phonon-carrier interactions. These phonon-phonon interactions also reduce the lattice thermal conductivity by increasing the phonon scattering rate. In general, increasing the temperature enhances the TE performance by increasing both electrical conductivity (due to a greater number of charge carriers in the semiconductor) and the Seebeck coefficient, while decreasing the lattice thermal conductivity, which remains the dominant contribution for $n < 10^{21}$ cm^{-3}. However, there are also limitations at high temperatures. When the charge carrier concentration becomes too high, carrier scattering begins to dominate, reducing mobility. Additionally, the electronic contribution to thermal conductivity increases, counteracting the benefits of reduced lattice thermal conductivity. As a result, each material exhibits an optimal temperature range for maximizing thermoelectric performance.

1.3.1 State of the art of thermoelectric materials

From the discussion in the previous sections, it is evident that zT serves as the primary metric for evaluating thermoelectric materials. Traditionally, efforts to improve zT have driven the search for new materials and the optimization of existing ones. However, beyond achieving a high zT, a good thermoelectric material must also be robust enough to operate under varying environmental and temperature conditions without degradation. Back in 1947, a first thermoelectric generator made of PbS and ZnSb was successfully fabricated, with a conversion efficiency of 5% under a ΔT of 400 K [31]. Later, in 1954, a cooling device based on Bi_2Te_3 was also demonstrated [32]. From that point onward, the exploration of thermoelectric materials accelerated, leading to the discovery of compounds with $zT > 1$ across various temperature ranges. As shown in Figure 1.5, a variety of materials are now being explored, categorized in different categories depending on their base composition and structure.

Inorganic thermoelectric materials are the most abundant group and are usually divided into seven subgroups. Six of them will be briefly presented in this section, while those based on silicon will be shown in depth in the following section.

Chalcogenides: Chalcogenides are based on the combination of chalcogen elements (Te, Se, S) with various metals. The most common material among this type is Bi_2Te_3, which possesses intrinsically low thermal conductivity due to its layered crystalline structure that leads to highly anisotropic properties. In addition, its electrical conductivity can be easily tailored with Sb and Se to obtain enhanced p- and n-type materials, respectively [35]. Commercial modules based on Bi_2Te_3 are still the most standard, as they can have values of zT above 1 for temperatures around RT. Other notable chalcogenide compounds include lead-based materials such as PbTe [36], $AgPb_mSbTe_{2+m}$ [37], $PbTe_{2\%}Na_{8\%}Sr$ [38]

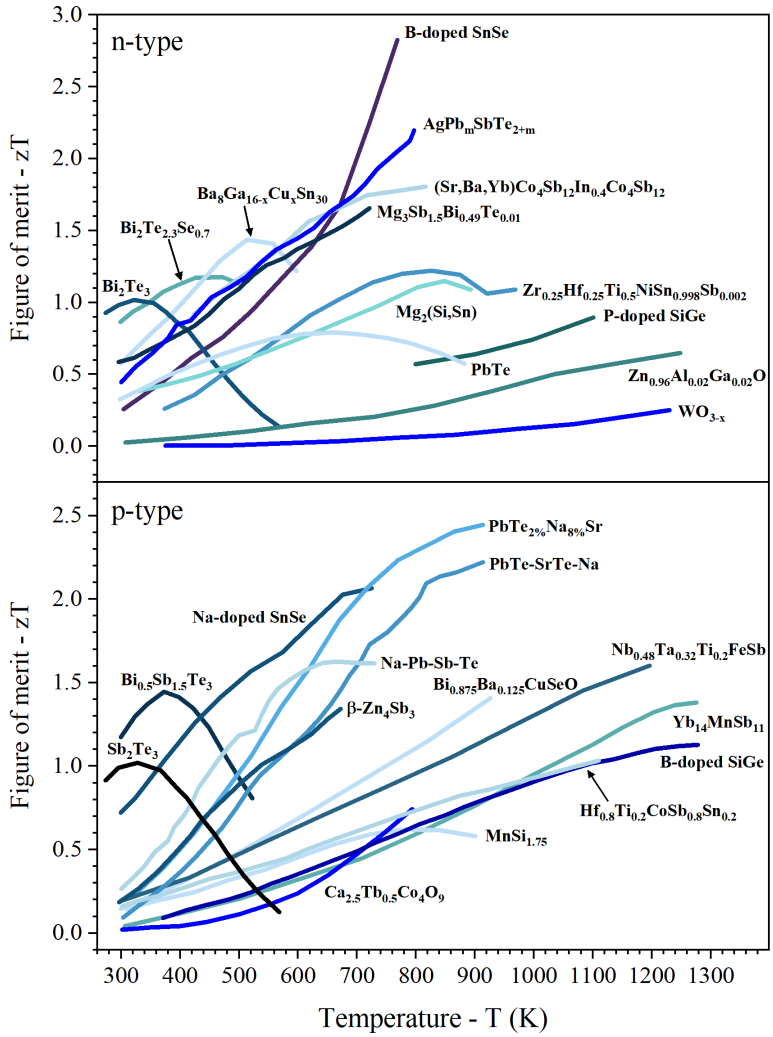


Figure 1.5: Figure of merit (zT) of several n- and p-type thermoelectric materials as a function of temperature. Representative compounds from most common types of thermoelectrics are shown, including chalcogenides, silicides, skutterudites, Zintl phases, clathrates, oxides and Heusler alloys. Data extracted from [29], [33], [34]

and NaPbSbTe [39], all of which have large zT values for temperatures between 600 and 900 K. Additionally, Sb_2Te_3 represents a prominent antimony-based chalcogenide. Tin selenides, particularly Br- and Na-doped SnSe, have also gained attention for their n- and p-type thermoelectric behavior, respectively [40], [41]. Among them, Br-doped SnSe stands out as the highest-performing n-type thermoelectric material, achieving a remarkable zT value > 2.6 at T > 700 K.

Skutterudites: Skutterudites are materials based on the TPn_3 structure, where T stands for a transition metal (i.e. Co, Rh and Ir) and Pn for a pnictogen (elements from group 15 of the periodic table). This kind of material forms cubic structures with some empty cubes that can be filled with ions for electrical and thermal tuning. The most

common type of skutterudites are based on Sb, thanks to their high carrier mobility, electrical conductivity and Seebeck coefficient. Some high zT n-type skutterudites include (Sr,Ba,Yb)$Co_4Sb_{12}In_{0.4}Co_4Sb_{12}$ [42] and β-Zn_4Sb_3 [43], with $Nb_{0.48}Ta_{0.32}Ti_{0.2}FeSb$ [44] as an efficient p-type. For these materials, the most attractive working temperature ranges are between 500 and 850 K, where they are among the materials with the best zT values.

Zintl phases: The term Zintl phases refers to a class of materials composed of polyanionic frameworks covalently bonded to electropositive cations. These materials form salt-like crystalline structures and are differentiated from other related compounds by the presence of electropositive cations that fully transfer their valence electrons to the polyanionic framework (an essential criterion for classification as Zintl phases). Examples of Zintl phases that show high zT values include those that have intrinsically low thermal conductivity and tunable carrier concentration, such as $Mg_3Sb_{1.5}Bi_{0.49}Te_{0.01}$ [45] for n-type TE, and $Yb_{14}MnSb_{11}$ [46] for p-type. The latter is one of the most promising p-type materials for very high temperatures (> 1200 K), as it shows a zT value above 1 and an exceptional absence of degradation in long-term operation under these conditions [47].

Clathrates: Clathrates are composite materials characterized by a distinct structure in which atomic or molecular guest species are encapsulated within a rigid host framework. The host typically forms covalently bonded coordination networks that create cage-like structures, which are subsequently occupied by the guest atoms. This wide range of structures results in anomalous thermal transport properties and a wide range of electrical behaviors, both of which can be tuned by modifying the guest-host compositions. High performance clathrates include variations of tin clathrates ($Ba_8Ga_{16}Sn_{30}$ [48]), like $Ba_8Ga_{16-x}Cu_xSn_{30}$ [49], an n-type thermoelectric (TE) with $zT > 1$ at medium temperature ranges (500-600 K).

Heusler compounds: Heusler compounds and their more interesting variant (the Half-Heusler compounds) are composites that follow the X_2YZ and XYZ proportions, respectively. These systems offer a wide range of strategies to enhance thermoelectric performance through elemental substitution within the crystal structure. This approach enables effective tuning of both thermal and electrical properties, paving the way for compounds with $zT > 1$ at high temperatures. Furthermore, these compounds also have excellent mechanical and thermal stability. Representative examples of n- and p-type Half-Heuslers are $Zr_{0.25}Hf_{0.25}Ti_{0.5}NiSn_{0.998}Sb_{0.002}$ [50] and $Hf_{0.8}Ti_{0.2}CoSb_{0.8}Sn_{0.2}$ [51] respectively.

Metal oxides: From a thermoelectric perspective, these materials usually exhibit low performance due to the high effective mass of their charge carriers and their inherently high thermal conductivity, which combined result in low zT values. However, metal oxides offer exceptional thermal and chemical stability, allowing them to operate at very high temperatures without degradation of structure or performance. They are also easy to fabricate and are generally composed of abundant, low-cost metals. For these reasons, research into metal oxides aims to develop cost-effective thermoelectric materials suitable for high-temperature applications. Notable examples of metal oxides with high zT values include $Zn_{0.96}Al_{0.02}Ga_{0.02}O$ [52] and WO_{3-x} [53] for n-type TE, and $Bi_{0.875}Ba_{0.125}CuSeO$ [54] and $Ca_{2.5}Tb_{0.5}Co_4O_9$ [55] for p-type TE. As shown in Figure 1.5, these metal oxides can achieve zT values exceeding 1 at temperatures above 800-900 K.

Besides inorganic TE, which comprise the vast majority, TE based on organic materials are also being explored and are especially applied in flexible devices due to their inherent soft characteristics [56]. Polymers are usually mixed with other materials like inorganic structures, graphene or carbon nanotubes. Examples of these subgroups are

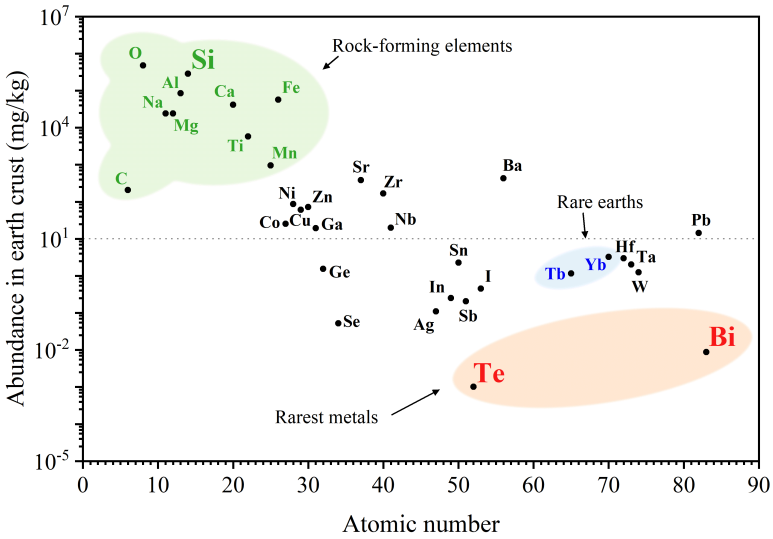


Figure 1.6: Elemental abundance in Earth's crust (in ppm) for the materials shown in Figure 1.5. The dotted line indicates the 10 ppm threshold. Both Bi and Te are among the scarcest elements, whereas only certain silicide-based thermoelectrics incorporate elements with abundances exceeding 10 ppm. Data taken from [33]

PEDOT:PSS with Na_2TeO_3 nanowires [57], which has a $zT = 0.1$ at RT, PEDOT:PSS with fullerenes [58], yielding zT values of 0.067 at RT, and p- and n-type single-walled carbon nanotubes [59], with a zT around 0.12 at RT.

However, if we take a look at Figure 1.6, which shows elemental abundance, all the materials used have concentrations below 10 ppm in the Earth's crust. This is particularly critical given the high reliance on TE materials based on Sb, Se and Sn; and even more so for the most common and still commercially dominant Bi and Te, which are among the rarest metals on earth. Consequently, the production of a large number of thermoelectric devices based on these materials seems difficult due to their cost and scarcity, along with the toxicity and environmental footprint of some of them. Furthermore, the most common materials and fabrication processes used for their manufacturing are hardly compatible with standard CMOS mass production of chips, which makes their integration into MEMS-like structures a difficult task. Considering the significant challenges in miniaturizing devices based on these materials (an imperative requirement in the IoT domain), we reach the same conclusion: alternative materials are essential to enable IoT deployment at the forecasted scale.

1.3.2 Si based thermoelectric materials

Thermoelectrically, silicon performs poorly in its bulk form due to its high thermal conductivity, which averages around 150 W/m·K. On the other hand, it exhibits an excellent thermoelectric power factor, as both Seebeck coefficient and electrical conductivity become significantly high after doping. Furthermore, silicon fulfills all the IoT constraints already mentioned in previous sections: it is abundant (see Figure 1.6), inexpensive and non-toxic; it offers outstanding miniaturization and integration capabilities; and it is inherently compatible with the MEMS and CMOS fabrication processes. Consequently,

silicon is a material with great potential in this field, but strategies to reduce its thermal conductivity are essential to achieve sufficiently high zT values. Since an optimal carrier concentration has already been established (see Figure 1.4), the most promising approach to decrease κ_{ph} is to enhance phonon scattering. To accomplish this, structuring silicon emerges as the most appealing strategy, provided that the critical dimensions remain above the electrons mean free path. In this way, phonon dispersion will occur even for high-frequency phonons, while electrical transport will experience minimal scattering.

An early example of the reduction of κ_{ph} in silicon through structuring dates back to 1997 [68], while complete thermoelectric characterizations validating this approach were reported by *A. I. Boukai et al.* and *A. I. Hochbaum et al.* in 2008 [18], [19]. Both studies demonstrated that silicon nanostructures achieve competitive zT values at room temperature. Since then, extensive research has been conducted, with representative examples shown in Figure 1.7. All these strategies rely, in one way or another, on introducing nano-

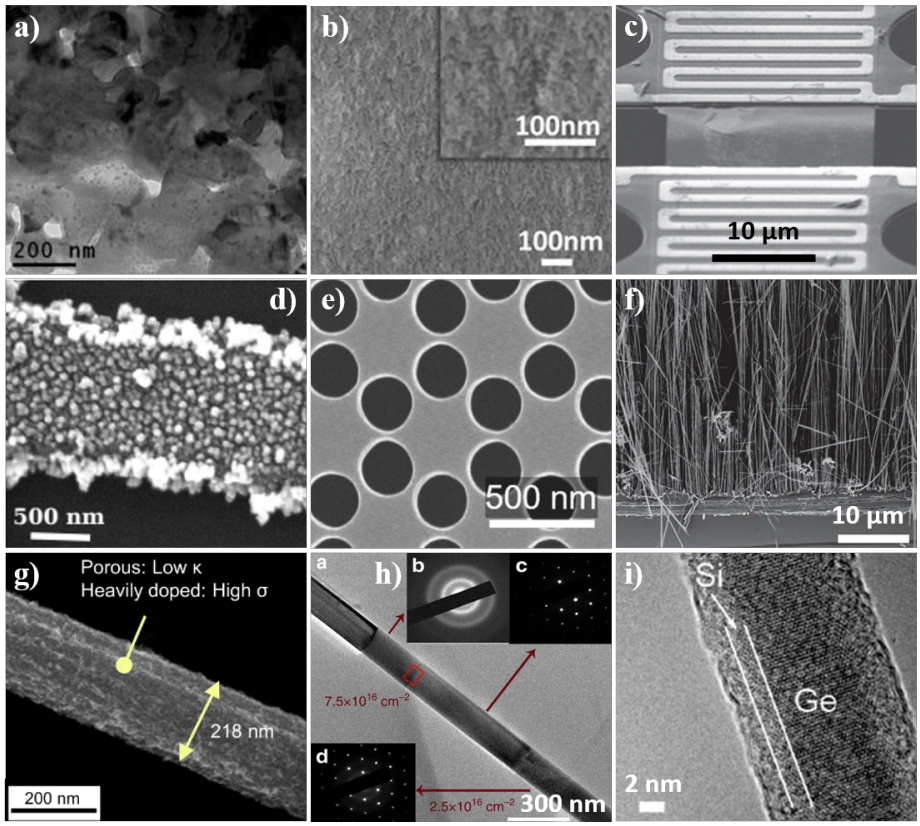


Figure 1.7: Examples of different nanostructuring strategies to reduce κ_{ph}: a) Nanocrystal bulk Si with grain sizes $<$ 200 nm [60], b) Nanoporous bulk Si with pore size $<$ 100 nm [61], c) $<$ 50 nm Si thin film [62], d) 240 nm Si thin film with surface roughness [63], e) Nanopatterned 300 nm poly-Si film [64], f) Rough surface Si nanowires with 20-300 nm of diameter [19], g) Porous Si nanowires with Si crystal sizes around 4 nm [65], h) Superlatticed Si nanowires with diameters of 160 nm [66], i) Core-shell SiGe nanowires with diameters between 11 and 23 nm [67].

metric dimensions into the material to efficiently scatter phonons, as boundary scattering dominates at these scales and increases proportionally with the surface-to-volume ratio. A comprehensive review of state-of-the-art Si and Si-based thermoelectric materials is presented in Table 1.3, including their thermoelectric properties and the corresponding structuring approaches. In the following, we discuss the advantages and limitations of these different nanostructuring strategies.

The first category of potential structures includes micro-/nano-polycrystalline silicon, nano-porous silicon, and dislocated or superlatticed bulk silicon. In these configurations, phonon scattering is enhanced by grain boundaries, dislocations, or pore walls. However, a major drawback of polycrystalline or dislocated structures is that these same features also scatter charge carriers, reducing the material's power factor. This introduces a trade-off in grain size optimization to balance the reduction of κ_{ph} against the preservation of electrical conductivity σ.

The second approach involves the fabrication of silicon nanowires (NWs), where the two-dimensional confinement significantly enhances phonon scattering due to the inherently high surface-to-volume ratio of these structures. However, single-crystal Si NWs still exhibit relatively high κ_{ph} ($> 10\,\mathrm{W/m{\cdot}K}$) unless their diameter is reduced below 30 nm [86]. Achieving high zT values in single crystal Si NWs therefore requires extremely small diameters, which pose substantial fabrication challenges, particularly when producing large, uniform arrays. Although arrays of Si NWs with larger diameters can be fabricated using the vapor-liquid-solid (VLS) method, this process typically employs gold as a catalyst, rendering it incompatible with CMOS technology. Further reductions in thermal conductivity (approaching or even below the amorphous limit) have been explored by using compounds of Si with other materials or by introducing structural heterogeneity. Some examples of compounds include SiGe [76], SiC [77] and $CrSi_2$ [78], with SiGe being the most extensively studied due to its significant reduction in κ_{ph} (which can reach values below $2\,\mathrm{W/m{\cdot}K}$) and its ease of fabrication using the VLS technique with GeH_4 as a precursor. Nonetheless, Ge possesses some environmental concerns, as it is both toxic and relatively scarce. Moreover, SiGe generally exhibits lower Seebeck coefficient values compared to Si (see Table 1.3). Regarding structural modifications, these include tailoring porosity [74] or NWs crystalline lattices [66], in order to minimize their thermal conductivity. However, such modifications typically involve the use of electron beam lithography (EBL) or focused ion beam (FIB) to individually pattern the NWs, or are based on vertical-like growth techniques (such as metal-assisted chemical etching -MACE- [73]). Limitations in integrating these materials at wafer-scale in planar-based TEGs, as well as the low capability of fabricating large arrays of NWs, arise when using these techniques. Furthermore, some approaches rely on roughening the NWs surface [19], which introduces challenges in achieving sufficient reproducibility across large arrays.

The third approach involves thin film fabrication, where phonon scattering is less pronounced than in NWs due to confinement occurring only in one dimension. Consequently, unstructured Si thin films can achieve κ_{ph} values near $20\,\mathrm{W/m{\cdot}K}$ only when their thickness is reduced to 17-20 nm [62], [87]. To further reduce κ_{ph}, strategies similar to those used for NWs have been explored, including alloying Si with other materials and introducing structural modifications. Common compounds for Si thin films include SiGe alloys [83], and silicides such as Mg_2Si [85] and $CrSi_2$ [84]. Except for SiGe alloys, silicides still show zT values ~ 0.01 in thin film form. Efforts to reduce κ_{ph} in Si aim to approach the amorphous limit while preserving σ. *D. Banerjee et al.* [79] reported κ_{ph} values around $1\,\mathrm{W/m{\cdot}K}$ in amorphous Si (a-Si), which also exhibits an exceptionally high

Table 1.3: Comprehensive summary of the different types of Si and Si-based structures reported in the literature. The color of the row indicates the materials used in each: white for Si and light-blue for compounds of Si with other materials. NC: nanocrystal, SC: single crystal, NP: nanoparticle, SL: superlattice, PC: polycrystal, TF: thin film, NW: nanowire, MACE: metal-assisted chemical etching, VLS: vapor–liquid–solid, d: diameter, t: thickness, p = period. The last column specifies the reference of each structure.

Structure	Size	κ (W/m·K)	σ (S/cm)	S (µV/K)	zT	Ref.
NC bulk Si	d_{NP} = 100 nm	10.5	550	120	0.11	[60]
Dislocated bulk Si	-	45	180	600	0.045	[69]
50 % Porous bulk Si	d_{NP} = 5 nm	-	-	1000	-	[61]
Porous bulk Si	t = 80 µm	7.6	700	250	0.25	[70]
NP bulk $(CrSi_2)_{0.9}$ with $(SiGe)_{0.1}$ inclusions	d_{NP} = 2 µm	2.1	925	1.5	0.12	[71]
PC bulk $MnSi_{1.74}$	d_{NP} = 500 nm	2.65	445	135	0.1	[72]
Rough SC Si NWs	d = 52 nm	1.66	590	240	0.6	[19]
Porous MACE Si NWs	d = 20-200 nm	1.68	131.6	382	0.34	[73]
46 % Porous Si NWs	d = 218 nm	2	500	200	0.31	[74]
MACE SC Si NWs	d = 150 nm	1.75	2.65	747.8	0.3	[75]
$Si_{0.9}Ge_{0.1}$ SC NWs	d = 65 nm	0.8	850	-110	0.2	[76]
VLS β-SiC SC NWs	d = 60-100 nm	86.5	225	-1210	0.12	[77]
$CrSi_2$ NWs	d = 150 nm	11	1000	150	0.06	[78]
Ar-doped a-Si TF	t = 100 nm	1.5	15.56	-1450	0.64	[79]
Holey Si TF	t = 100 nm p = 55 nm	1.73	333	250	0.4	[80]
Holey Si TF	t = 300 nm p = 200 nm	11	700	-107	0.02	[64]
PC Si TF with a-SiO_2 interfaces	d_{NP} = 20 nm	0.78	190	220	0.3	[81]
Porous Si TF	t = 3.2 µm d_{NC} = 15 nm	1	55.6	-248	0.1	[82]
PC $Si_{0.7}Ge_{0.3}$ TF	t = 137 nm	1.68	600	-160	0.27	[83]
PC $CrSi_2$ TF	t = 260 nm	2	1250	32	0.015	[84]
PC Mg_2Si TF	t = 650 nm	1.6	10	199	0.01	[85]

Seebeck coefficient of $-1.45\,\mathrm{mV/K}$. However, *Nakamura et al.* [81] and *Ziouche et al.* [82] demonstrated that values near or even below the amorphous limit can be achieved while maintaining a reasonably high σ by fabricating sub-15 nm porous Si or by incorporating sub-5 nm SiO_2 layers at the interfaces of thin films of polycrystalline Si. However, in both cases, the Seebeck coefficient is far from that of a-Si, while σ remains below 200 S/cm. Other structural modifications include further patterning of the thin films to obtain holey Si [80], [88]. The first case, which is the most interesting in terms of zT and CMOS compatibility, leads to a high zT of 0.4 at RT due to a significant thermal conductivity reduction obtained with the holey pattern, which is achieved by means of block copolymer driven nanostructuration. However, a more recent publication of a block copolymer-based holey Si reports a more modest zT of 0.05 due to the decreased electrical conductivity in the structure [89]. As for other holey films, EBL is generally used to pattern holes in the structure, which imposes limitations on wafer-scale fabrication or scalability [88], [90]. Both references report modest values of zT, namely 0.02 and 0.09 at RT.

Throughout this thesis, three different structuring strategies have been studied: Si microbeams, single-crystal Si nanowires (NWs), and block copolymer driven nanostructured Si thin films. The first does not significantly enhance the intrinsic thermoelectric properties of Si. Instead, Si microbeams aim to improve device-level heat management, thereby optimizing the overall power generation to investigate whether this could enable the use of bulk Si in thermoelectricity. The last two correspond to structures with physical confinement (two-dimensional on the NWs and one-dimensional confinement with further patterning on the films). Therefore, these two aim to improve the thermoelectric properties of Si.

1.4 Thermoelectric devices

As previously shown in Figure 1.3, thermoelectric devices have two basic operating modes: power generation, where they are referred to as thermoelectric generators (TEG), and refrigeration, where they are referred to as thermoelectric refrigerators (TER). The device efficiency in both operating modes has been shown in Section 1.2.1, where it is evident that ZT is the most important parameter for maximizing the efficiency of the device. In this section, some considerations on the optimization of ZT from the device point of view will be presented, as its material-based contribution (i.e. the zT) has been extensively explained in the previous sections. In the following, only TEGs will be considered, as the objective of this work is to fabricate TEGs based on different Si structures.

1.4.1 Thermoelectric generators

A TEG is a solid-state device that converts a temperature gradient into electrical power. Since the maximum conversion efficiency of a TEG is influenced by its ZT value, and currently these are within the 0.01 - 2 range, the typical η of a TEG tends to be lower than that of other energy conversion cycles [4]. However, TEGs possess several advantages from a device point of view because they are compact, robust, have no moving parts, and can be applied in a wide range of temperatures. These properties make TEGs especially interesting in waste heat recovery [91] and remote power generation, since the high autonomy of a TEG favors its application in harsh environments.

In terms of device architecture, a TEG is typically composed of three parts: the

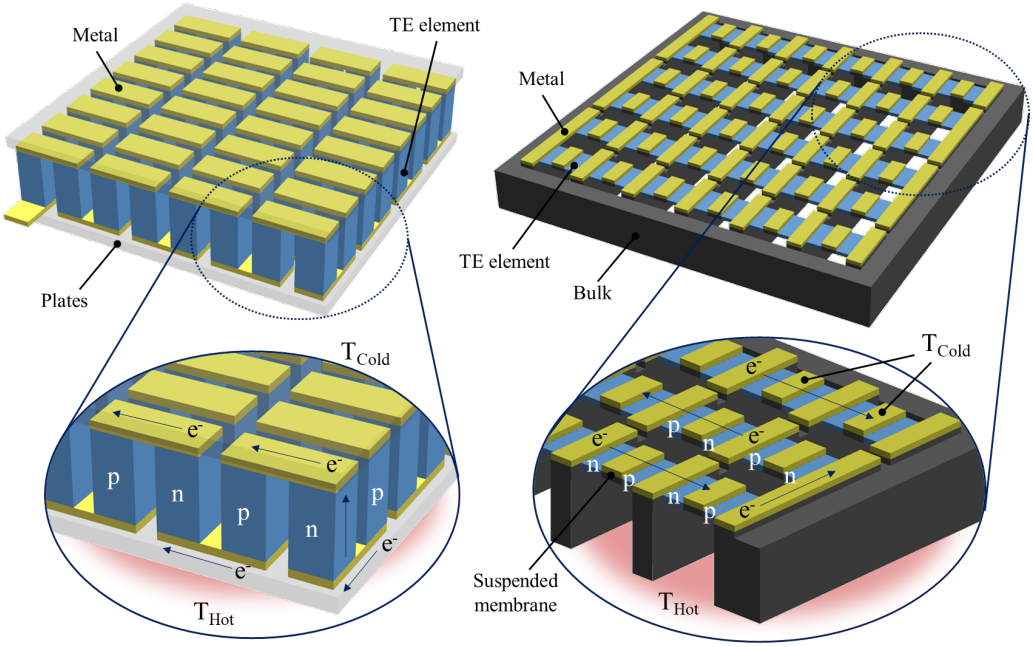


Figure 1.8: Schemes of the typical vertical π-type and planar TEGs. In both cases the n and p-type TE legs are connected electrically in series and thermally in parallel. In the planar design the heat flow is engineered to obtain a lateral temperature gradient thanks to the use of a suspended platform.

TE material (usually in the form of p- and n-type legs), the hot and cold surfaces and the electrical and thermal contacts. Figure 1.8 shows the two basic configurations of a TEG. In the most standard π-type vertical architecture, the p- and n-type legs of the TE material are connected electrically in series and thermally in parallel between two ceramic plates. These serve as the hot and cold surfaces of the TEG. In order to have good electrical and thermal contacts, interface materials are integrated between the TE legs and the conducting layer (in gold in Figure 1.8) to achieve effective soldering and minimize the contribution of the contact resistances, which significantly affect the ZT of the device. Due to the dissimilar thermal and electrical properties of the p- and n-type legs (because they are made of different semiconductor materials), this architecture should be optimized to maximize the conversion efficiency, following the next relationship [92]:

$$\frac{A_p/L_p}{A_n/L_n} = \frac{\sigma_n \kappa_n}{\sigma_p \kappa_p} \tag{1.26}$$

where A and L are the cross-sections and the lengths of the p- and n-type TE legs. Generally, this relationship is not fulfilled due to the greater difficulties of fabricating and integrating the two legs of different sizes. Nonetheless, this geometry is well optimized in terms of thermal losses, as it directly contacts the hot surface and is easily encapsulated with a heat exchanger on the top. Also, there are no parasitic heat losses between the hot and cold sides, which are always separated by the TE legs. In the case where only one type of semiconducting TE leg is present (i.e. a single-leg TEG with either p- or n-type TE legs), it is easier to optimize the geometry of the TE element. However, this

is at the cost of having heat losses between the hot and cold sides, since the conducting layer (i.e. the metallic leg) should connect the top side of one TE leg with the lower side of the following leg, thereby introducing a parasitic heat path along the way. As for MEMS-based TEGs with a vertical configuration, their performance is generally limited by the maximum height of the TE element that can be fabricated and by the challenges of integrating vertical structures within a planar-type wafer-level process flow.

The second configuration corresponds to the planar architecture, where the TE legs are integrated horizontally in the TEG. In this geometry, the heat flow is engineered to convert the vertical external temperature gradient into a lateral one in the device. Generally, this is achieved thanks to the use of suspended areas that serve as the cold end of the TEG. Thus, the TE legs are integrated between these and the bulk regions, harvesting the lateral gradient that is created. Some cavity-free examples are also reported in the literature due to the ease of their fabrication, but this architecture shows limited thermal management, leading to very low temperature gradients in the TE legs. These types of planar TEGs are usually seen in Si-based µTEGs that are fabricated using MEMS technology, as they take advantage of the excellent fabrication and integration capabilities of Si technology, which is planar in nature. In this work, this architecture was chosen as the base geometry for all of our designs.

Regardless of the type of architecture used for the fabrication of the TEG, there are some considerations regarding the final power output of the device. The power generation depends on both the temperature gradient across the TE legs and the total electrical resistance of the TEG. The first is maximized by increasing the length and decreasing the cross-sectional area of the TE legs, while the second is maximized when the TE legs are wider and shorter. Moreover, the legs can be connected electrically in parallel or in series, maximizing either the current or voltage generation of the device depending on the output needs. Thus, besides optimizing the thermal and electrical contacts between the TE legs and the rest of the device, a proper evaluation of the output requirements should be done in order to precisely design the electrical connections and TE leg sizes in each device.

Some examples of bulk TEGs and their use cases include: radioisotope thermoelectric generators (RTGs) that use plutonium-238 as their radioactive source and TE materials such as SiGe and PbTe [93], which have been extensively used for space exploration missions; Bi_2Te_3-based TEGs for waste heat recovery in automotive applications in companies like BMW, General Motors, FIAT and Chrysler [94]; Bi_2Te_3–PbTe hybrid TEGs for waste heat recovery in the Portland cement industry [95]; a Seiko wristwatch completely powered by a TEG unit [96]; and many more.

1.4.1.1 µ-Thermoelectric generators

As mentioned in the previous section, one of the main limitations of the TEGs applicability is the low conversion efficiency of their modules in comparison with other energy conversion cycles. This, however, is only true for power generation above a given threshold, as shown in Figure 1.9. Below these power levels, the efficiency of the current TE modules starts to become competitive, especially below the Watt range. Thus, one of the most promising fields for TEG applications is low-power devices with power requirements that span from nW/cm^2 to mW/cm^2, which are particularly relevant in the context of the IoT.

In terms of the fabrication of TEGs with such power density generation, reducing their size becomes essential to maximize their efficiency and cost, for which MEMS tech-

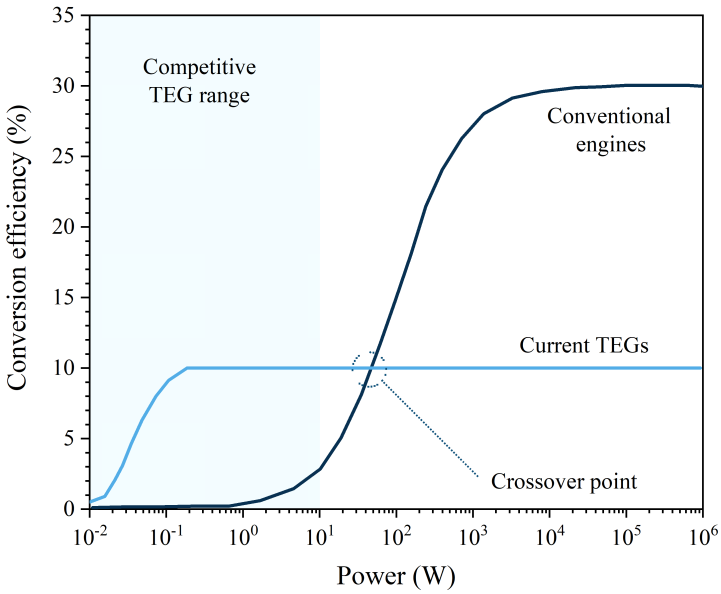


Figure 1.9: Comparison between the conversion efficiency of current TEGs and conventional energy conversion engines as a function of the power level. The values of efficiency and power are qualitative, and serve just to visualize the general trend observed with these kind of devices. Data adapted from [97].

nology stands out as the most promising route to fabricate micro-TEGs (µTEGs). This includes not only using Si or Si-based TE materials (such as Si alloys or silicides) in the µTEGs, but also the possibility of integrating a wide range of other TE materials in MEMS devices, each with different deposition techniques depending on their properties. Furthermore, the excellent integration capabilities of Si technology enable an increased number of TE legs per unit area and allow the mass production of µTEGs at the wafer scale, eliminating the manually assembled typical π-type modules. All this justifies the growing interest in the fabrication of µTEGs [105]. However, a more traditional π-type architectural approach is still being explored for the fabrication of µTEGs thanks to the use of additive manufacturing and other deposition techniques, such as electro-deposition [102], [104]. These generally involve the use of more standard TE materials, like Bi_2Te_3 or Sb_2Te_3, which raise subsequent sustainability concerns, but they are able to generate large power densities in the range of even hundreds of $\mu W/cm^2$. Examples of µTEGs with different geometries and TE base materials are shown in Figure 1.10. Among them, four µTEGs stand out due to their high power density generation: a MEMS-type µTEG with integrated SiGe NWs [98], generating a total of 45.2 $\mu W/cm^2$ when exposed to a hot temperature of 395 K; a π-type vertical µTEG based on electro-deposited BiTe/CuTe legs [102], generating a total of 562.5 $\mu W/cm^2$; a planar-type µTEG based on 70-µm thick BiTe films deposited by means of sputtering [99], generating a total of 755.5 $\mu W/cm^2$ when a $\Delta T = 51.2$ K is present; and a MEMS-type planar µTEG with an integrated holey film fabricated with EBL [106], generating a total of > 100 $\mu W/cm^2$. However, the first three present clear concerns regarding the sustainability of the device due to the use of Ge, Bi, and Te, while the last faces limitations when scaling up fabrication to mass production, owing to the use of EBL for patterning the Si thin films. Therefore, a fully

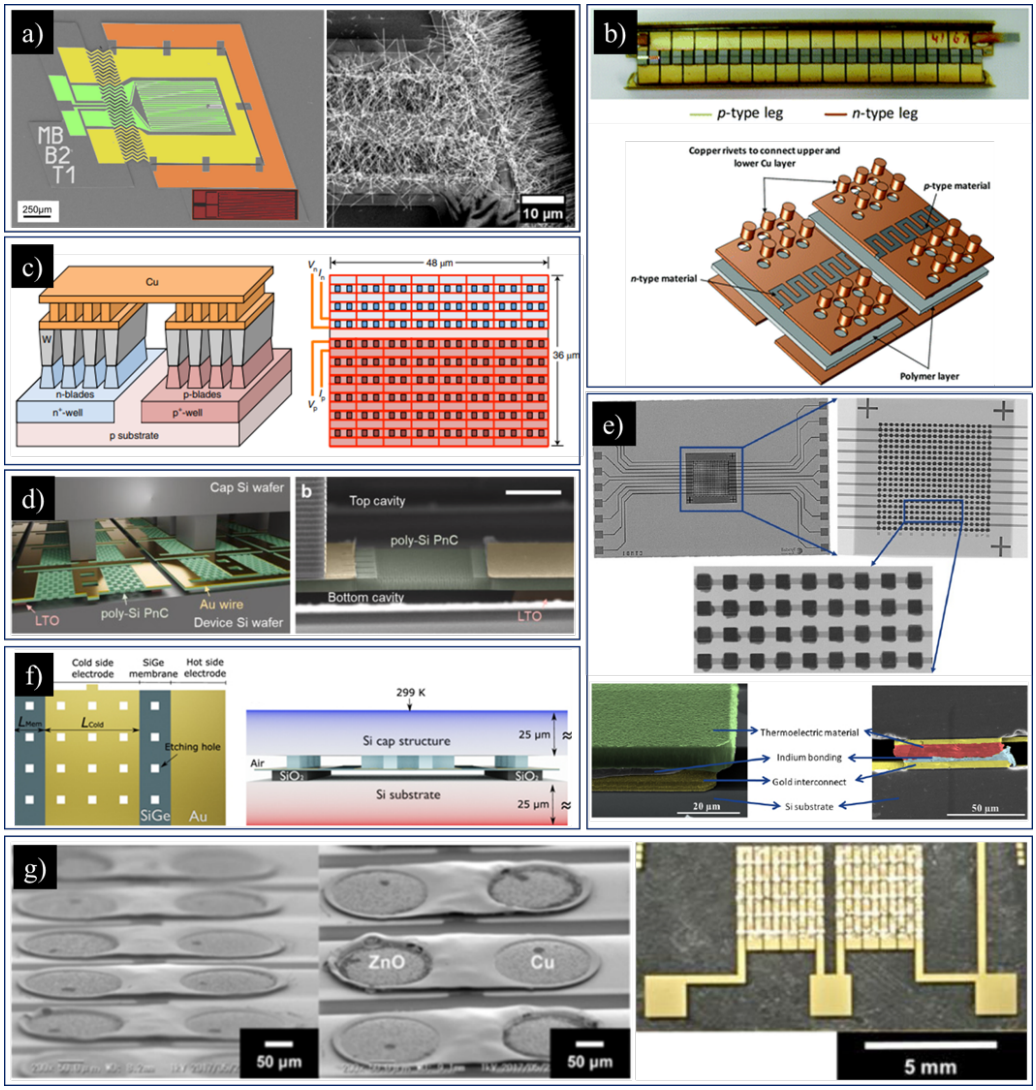


Figure 1.10: Examples of µTEGs extracted from the literature. a) MEMS-type µTEG with integrated SiGe NWs [98], b) planar-type µTEG based on 70-µm thick BiTe films deposited by means of sputtering [99], c) cavity-free π-type Si-beams based µTEG [100], d) MEMS-type planar µTEG with an integrated holey film fabricated with EBL [101], e) π-type vertical µTEG based on electro-deposited BiTe/CuTe legs [102], f) planar MEMS-type µTEG with integrated SiGe thin films [103] and g) π-type vertical µTEG based on electro-deposited ZnO legs [104].

sustainable, wafer-compatible and scalable μTEG with enough power density generation remains to be developed.

1.5 Block copolymers

The following sections provide a brief theoretical overview of block copolymers (BCPs) and their assembly possibilities, as this material was extensively used in this thesis to achieve the nanostructuring of thin Si films.

Block copolymers are composed of two, or more, different polymer blocks covalently bonded together that suffer a certain thermodynamic incompatibility between them (which is quantified by the Flory-Huggins parameter). Because the blocks cannot fully segregate due to the covalent bond, the BCPs are forced to self-assemble into periodic micro- or nano-domains in order to minimize their free energy. In such a way, different types of patterns (such as lamellas, cylinders or spheres) are formed after the BCPs are given sufficient chain mobility, typically above their glass transition temperature, while the system is below the order disorder transition temperature, where they show a thermally-driven micro-phase separation [108].

In the cases where the block copolymer is composed of only two linear polymer units (diblock copolymers), the theoretical phase diagram that represents the possible organization domains is shown in Figure 1.11. The three parameters that affect phase formation are the degree of polymerization, N (which corresponds to the total number of monomers in the BCP), the Flory-Huggins parameter, χ, and the relative volume fraction

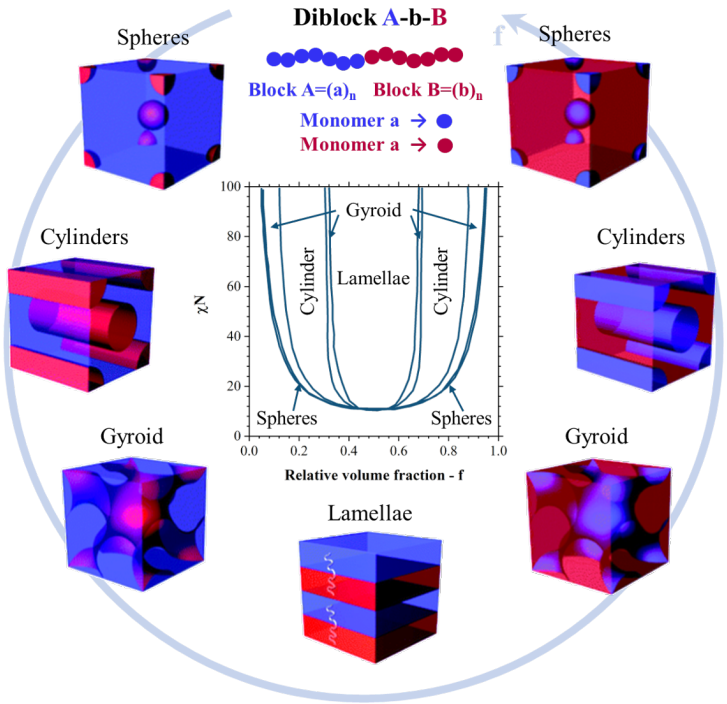


Figure 1.11: Theoretical plot of the different phases that can be created by a diblock copolymer as a function of χ, N and f. Adapted from [107].

between both components, f. The Flory-Huggins parameter is an intrinsic property of the chemical structure of the monomers in each block, and gives a measure of the thermodynamic incompatibility between them. Assuming the energy of interaction per monomer is:

$$\alpha\rho_A\rho_B = kT\chi\rho_A\rho_B \tag{1.27}$$

with ρ_A and ρ_B being the reduced densities of monomers A and B, which correspond to the ratio of the local density of each monomer at a point x averaged across the entire sample, and α being the effective interaction parameter [109]. This interaction parameter can then be expressed as the sum of all the individual monomer-monomer interactions (A-A, B-B and A-B):

$$\alpha = \iota_{AB} - \frac{1}{2}\left(\iota_{AA} + \iota_{BB}\right) \tag{1.28}$$

When the Flory-Huggins parameter (χ) of a diblock copolymer is greater than zero, it indicates that the A-B interaction energy (ι_{AB}) dominates over the combined A-A and B-B interactions, resulting in an effective repulsion between the two blocks. However, reducing A-B contacts simultaneously decreases the system's entropy, which also increases the free energy. Therefore, a trade-off arises between these two contributions. When χ is small, the entropy term dominates, leading to a disordered state in which the chains of both blocks tend to mix. In terms of ρ_A and ρ_B, this corresponds to $\rho_A = f$ and $\rho_B = 1 - f$ at any point in the system, where f is the relative volume fraction of the two components. For higher χ values, or when the product χN exceeds a critical threshold, the enthalpic contribution (the Equation 1.27 term) becomes dominant, and different ordered morphologies can form depending on f and χN (see Figure 1.11). The theoretical value that marks the frontier between disordered and ordered states is $\chi N = 10.5$. If the χN product is sufficiently high, the distribution of monomers A and B (ρ_A and ρ_B) will no longer follow their relative volume fractions, leading to phases where only one monomer is present. However, semi-ordered states with some monomer mixing will occur if χN is near the value of 10.5. Thus, to ensure that strong phase formation appears, block copolymers with high χN values are required. This can be obtained by selecting BCPs with intrinsically high values of χ or by increasing the degree of polymerization N. The drawback of the second case is, obviously, that it limits the minimum size of the formed patterns. It is also important to note that the value of χ is inversely proportional to the temperature [110], which can affect phase formation when the BCPs are exposed to a temperature above their glass transition temperature. Whether this effect is important or not will ultimately depend on the variation of χ with temperature, which is characteristic of each BCP, and on the minimum temperature required to enable chain mobility, which is inversely proportional to the degree of polymerization, or total molecular weight of the BCP.

The field of applications of BCPs is vast and includes topics as wide as thermoplastic elastomers [111], pharmaceutical applications such as drug delivery and release and mimicking of biomembranes [112], the fabrication of mesoporous materials [113] and, specifically related to the scope of this thesis, the use of BCPs for nanometric lithographic applications in electronics [114]. This later application usually involves the elimination of one of the blocks to obtain a mask that is used for either etching the layer underneath or filling the holes by depositing a material [115]. The first approach is the strategy used in this thesis to nanostructure Si thin films (see Section 2.1.10).

An alternative to free-surface self-assembly of BCPs is directed self-assembly (DSA). This technique involves guiding the BCP pattern at a given orientation using either physical or chemical templates. In this thesis, DSA was investigated to obtain aligned lamellar patterns. However, since these structures have not yet been integrated into a device for thermoelectric characterization, a brief overview of this topic, along with the results of the work, is presented in Appendix A.

1.5.1 Blends

One of the possibilities that BCPs can offer for adjusting the periods of the patterns are blends. A blend is a mixture, typically of two BCPs or of a BCP and a homo-polymer, that can form an intermediate phase or that can tailor more precisely the size of one of the blocks in the domain. When mixing two BCPs of the same type, two outcomes are possible: miscibility and immiscibility, forming either a new individual phase or an alternation of two separated phases of the two BCPs. The miscibility of a blend generally depends on two parameters: the ratio between the molecular weights of both BCPs, $\alpha_{BCP} = M_1/M_2$, and the weight fraction of the BCP with a larger monomer chain, f_1, being always $f_1 + f_2 = 1$. When α is below a certain threshold, complete miscibility occurs between the BCPs for $0 < f_1 < 1$, meaning that BCPs with relatively similar size can easily mix to create intermediate patterns. Typically, these α_{BCP} (i.e. the critical values) differ depending on the type of phases that are formed [116], [117]. Above these values, miscible domains are formed only for limited ranges of f_1: $f_{1,CS} > f_1$ and $f_1 > f_{1,CL}$, being $f_{1,CS}$ and $f_{1,CL}$ the critical small and large values, respectively. Another characteristic of blends is that $f_{1,CS} << 1 - f_{1,CL}$ for both lamellar and cylindrical phases, even reaching $f_{1,CS} = 0$ for high values of α_{BCP} (see Figure 1.12) [118]. This suggests that larger BCPs can more easily incorporate shorter ones, whereas shorter BCPs have greater difficulty in solubilizing larger ones. In some cases, even shorter BCPs can be completely incorporated into a micro-domain of block A or B, moving away from the interface [119].

In the case of Polystyrene-Block-Poly(methyl Methacrylate) (PS-b-PMMA, the BCP used in this thesis), blending two BCPs offers several advantages. The most obvious is obtaining intermediate domain periods by blending BCPs with different natural periods. In some cases, these blended systems can exhibit slightly fewer defects compared to individual BCPs with similar domain sizes. The calculation of the domain period obtained after blending is straightforward. It considers only the individual periods of the two BCPs, l_0^1 and l_0^2, and their respective weight fractions, f_1 and f_2:

$$l_0^{blend} = f_1 l_0^1 + f_2 l_0^2 = f_1 l_0^1 + (1 - f_1)\, l_0^2 \tag{1.29}$$

Individual BCPs also present limitations regarding the film thickness that can be deposited on a substrate while still forming well-ordered phases. As the molecular weight increases, the maximum film thickness compatible with the formation of well-ordered domains that are oriented perpendicular to the substrate tends to decrease. However, patterns with larger thicknesses (while maintaining the same period) can be obtained by blending two BCPs with different natural periods, one shorter and one longer [120]. Furthermore, the temperature needed to induce the thermal diffusion of these types of blends is lower due to the higher mobility of the shorter BCPs, while the individual BCPs of high molecular weight demand higher temperatures to form the domains. In the specific application addressed in this thesis, the blending of two compatible cylindrical BCPs

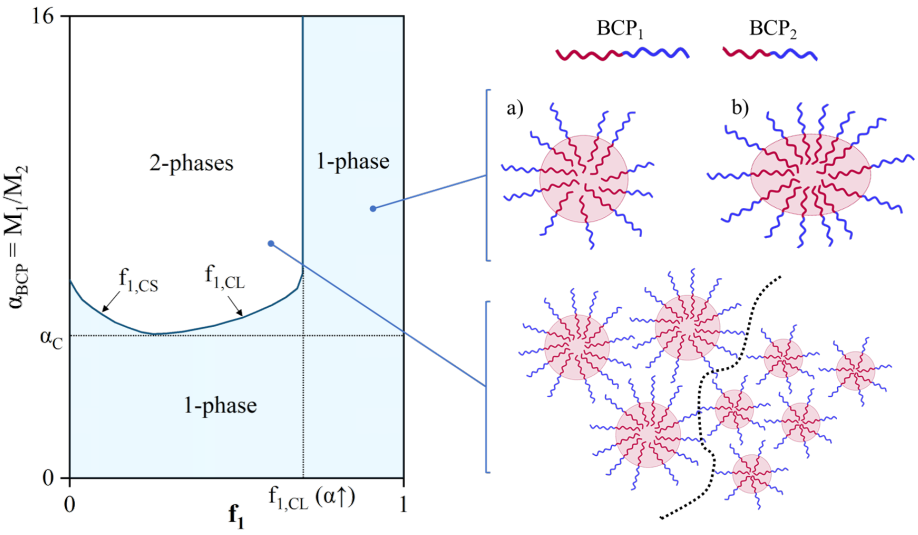


Figure 1.12: Experimental plot of the miscible and immiscible regions in blends of diblock copolymers as a function of α_{BCP} and f_1. For $\alpha_{BCP} < \alpha_C$ a single phase is always present regardless of the value of f_1. When $\alpha_{BCP} > \alpha_C$, the formation of two immiscible phases depends on the values of $f_{1,CS}$, $f_{1,CL}$ and α_{BCP}. If α_{BCP} is sufficiently high, a single phase can only form when $f_1 > f_{1,CL}$. In cases where a single phase is formed, schemes a) and b) show the possible patterns that may emerge within cylindrical domains, depending on the type of reorganization between BCP$_1$ and BCP$_2$. Adapted from [119].

with significantly different chain lengths can be very useful. After the nanostructure is transferred to Si, the formation of different sizes and shapes in the cylindrical phases of the BCP (Figure 1.12 a and b as examples) can help improve its thermoelectric properties. As both long range order and neck size will not be regular, scattering of a wider range of phonons will take place, further hindering thermal conduction through the film. Furthermore, the highest BCP film thickness that can be deposited with blends facilitates the subsequent pattern transfer into the Si layer, while also diminishing the temperature needed to achieve proper self-assembly.

Blends of PS-b-PMMA with either PS or PMMA homo-polymers can also be helpful in adjusting period spacing and pattern formation. Typically, the spacing between micro-domains tends to shrink after thermal treatment, which induces diffusion and reorganization of the BCPs. Adding a small percentage of homo-polymer in the BCP can help maintain a constant domain period at different temperatures [121]. In addition, the introduction of homo-polymers can be used to tailor the diameter of the PMMA cylinders without increasing the PS neck size between them. In some cases, even a small percentage of homo-polymer can help correct mismatched BCP blends, promoting the formation of fully ordered phases [122].

Chapter 2

Experimental methods

In this chapter, the main processes involved in the fabrication of our µTEGs and characterization devices are described. This is followed by an explanation of the structural characterization methods used to evaluate both the devices and the materials. Finally, the last section presents the techniques employed to assess the electric, thermal and thermoelectric properties of the Si-based structures studied in this thesis.

2.1 Micro- and Nano-fabrication

The main strategy behind the fabrication of all devices throughout this work is a combination of bottom-up (such as NWs growth and deposition of materials on top of Si wafers) and top-down (such as micro-machining strategies to selectively remove a material) techniques in order to obtain planar-type devices using standard Si technology fabrication processes. The technological processes used are compatible with scalable fabrication, even if part of the fabrication in this thesis was completed at chip level to maximize the experimental outcome.

2.1.1 Photolithography

Photolithography is the foundation of Si micro-fabrication technologies, as defining multiple layers with different layouts (on both the front and back sides of a wafer) involves going through several photolithographic processes. Photolithography is based on defining a given pattern on a photoresist (a photosensitive resist) by means of a mask with the desired design or a scanning laser. The first is more optimal in terms of time cost, especially when done at a wafer scale, as it exposes the whole wafer simultaneously. The second is more suitable at chip level, for few samples. In the laser lithography case, two resolutions are available at IMB-CNM clean room facilities: 1 and 10 µm, depending on the laser used (KLOÉ Dilase 650 i-line). First, the photoresist is spin coated and then it is exposed to light only in the desired areas (i.e. those where the mask is transparent or where the laser scans the sample). After exposure to light, the samples are developed in a solvent bath to remove either the exposed or unexposed regions of the resist, depending on whether the photoresist is positive or negative. In the positive case, resist bonds are broken by means of a chemical reaction triggered by light, while in the negative case, light causes cross-linking of the bonds in the exposed areas. Thus, during the development step,

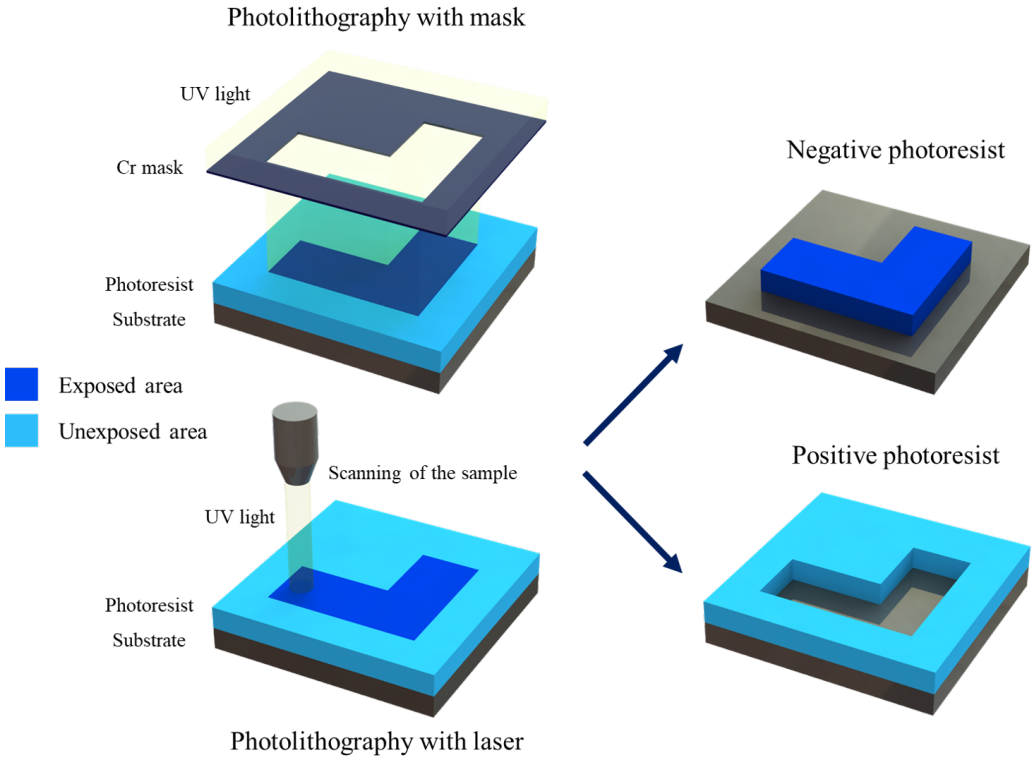


Figure 2.1: Schemes of the two photolithography techniques used in this work (i.e. using a chromium mask and using laser scanning). In the first method, the entire sample is irradiated simultaneously. In contrast, the laser scanning sequentially scans the pattern making it inherently slower. After developing the samples, the features on the patterned photoresist depend on its type (positive or negative) as illustrated in the images.

the areas with broken or non cross-linked bonds are etched away by the solvent. The rest of the photoresist can be used as a mask. This pattern is typically transferred to the substrate using etching or deposition processes, followed by the removal of the remaining photoresist. A basic scheme of the overall process for both approaches described can be seen in Figure 2.1. By iterating this photolithography process, the device can be defined with different layouts in different layers. Mask-based photolithography was used in this work for all the photolithography steps made at a wafer scale, while laser was employed for processes at a chip level scale, especially for the fabrication of thermoreflectance structures.

2.1.2 Thin film deposition

Throughout this thesis, several thin film deposition techniques were used to fabricate the different devices. These include chemical vapor deposition (CVD) techniques, like plasma enhanced (PE) and low pressure (LP) CVD, atomic layer deposition (ALD), and thermal oxidation. The last needs an oxidizing agent in the processing furnace that reacts with Si to form SiO_2. Dry oxidation (i.e. with O_2 gas) shows lower oxide growth rate, high film density and low stress. For these reasons, it was selected in this work to fabricate

guiding patterns used in the DSA of BCPs.

CVD refers to different types of deposition techniques where a chemical reaction occurs between the precursor gases, leading to the formation of a thin layer of material on top of a substrate inside the reaction chamber. The PECVD technique is based on creating a plasma that ionizes the precursor species, thereby lowering the minimum temperature at which the chemical reaction can occur. This can be useful as it makes the CVD process more compatible with materials with lower tolerance to higher processing temperatures, like metals, as the depositions may be achieved in the 200-400°C range. In addition, it has a high growth rate and results in good coverage of the substrate even if a complex structure is underneath. The main disadvantage of PECVD is the high contamination introduced in the grown film, originated by the presence of impurities generated by the plasma. LPCVD, on the other hand, demands higher temperatures (> 400-500°C) but is conducted at subatmospheric pressures. This results in high purity and uniform thin films, but at slow growth rates. Moreover, the higher process temperature makes it incompatible with substrates with metals. Within the framework of this thesis, PECVD was used to deposit SiO_2 films both at wafer and chip scale, Si_3N_4 films at wafer scale only in cases where a metal was already present in the sample and at chip scale regardless of the materials on the sample due to the absence of available LPCVD machines that were compatible with chip processing. LPCVD was used for the deposition of lower-stress Si_3N_4 films at a wafer scale before depositing metal layers.

The last CVD technique that was used is ALD. This relies on the sequential introduction of precursor species into the reaction chamber. A self-limiting mechanism restricts the maximum thickness deposited per cycle, which is determined by the initial precursor-substrate interaction. By adjusting the number of cycles, the final film thickness can be precisely controlled. In this work, ALD was used to deposit thin, conformal HfO_2 films for KOH masking investigations.

2.1.3 Metallization

Metallization refers to the deposition of metallic layers on a substrate. The two main techniques in this field are sputtering and thermal evaporation. Both are based on physically driven processes. In sputtering, a target composed of the desired material is placed inside the reaction chamber and bombarded with argon ions. This bombardment ejects atoms from the target, which then deposit onto the substrate, forming a thin metallic layer. The directionality of the deposition is highly dependent on the chamber conditions, as at higher pressures scattering processes take place (i.e. is less suitable for lift-off processes). This technique is compatible with metals with high melting points. Thermal evaporation relies on a heating source to evaporate material from a target. The vaporized material then condenses and solidifies on a substrate that is maintained at a temperature below the melting point of the evaporated material. The entire process takes place in a vacuum chamber, which minimizes scattering and enables directional and uniform thin films on the substrate. This technique is particularly compatible with lift-off processes. In the context of this thesis, sputtering was used to deposit Ti/W and Cr/Au films, while thermal evaporation was employed for the deposition of Cr/Pt and Cr/Au films.

2.1.4 Etching

In addition to lift-off, which is typically used with metals, etching is the main process involved in film patterning using photolithographic resist masks. There are two main categories of etching processes: dry and wet etching. The first involves using a gas to remove material from the sample, while the second uses liquid-phase substances. A second parameter commonly used to characterize the type of process is the isotropy or anisotropy of the etching. Isotropic etching removes the same amount of material in all directions, whereas anisotropic etching has a preferential direction in which the etch rate is higher than in others. A schematic of this can be seen in Figure 2.2.

Generally, wet etching processes tend to be isotropic due to the nature of their etching mechanism, since they rely solely on chemical reactions. Isotropic wet etching processes used in this work include hydrofluoric acid (HF), which attacks SiO_2 with great selectivity toward Si; buffered oxide etchant (BOE), a solution composed of HF and a buffering agent to make the etch rate of SiO_2 more controlled, stable, and selective with respect to photoresist; and phosphoric acid at high temperature, which attacks Si_3N_4 with good selectivity towards SiO_2. The wet etching mechanism of potassium hydroxide (KOH) is also chemically driven but, when applied to silicon, it shows strong anisotropy due to the varying reaction rates across different crystallographic planes. In this case, the Si atoms of the different crystal planes have different activation energies at which the reaction mechanism is triggered. More specifically, the (100) and (110) planes have a very high etching rate compared to the (111) planes, leading to inverted pyramid-like shapes that appear on wafers with (100) surface orientations (see Figure 2.2). This mechanism was used in this thesis to etch Si with different configurations.

Dry etching processes tend to exhibit greater anisotropy because they are typically based on the bombardment of the sample surface with ionized atoms. These processes

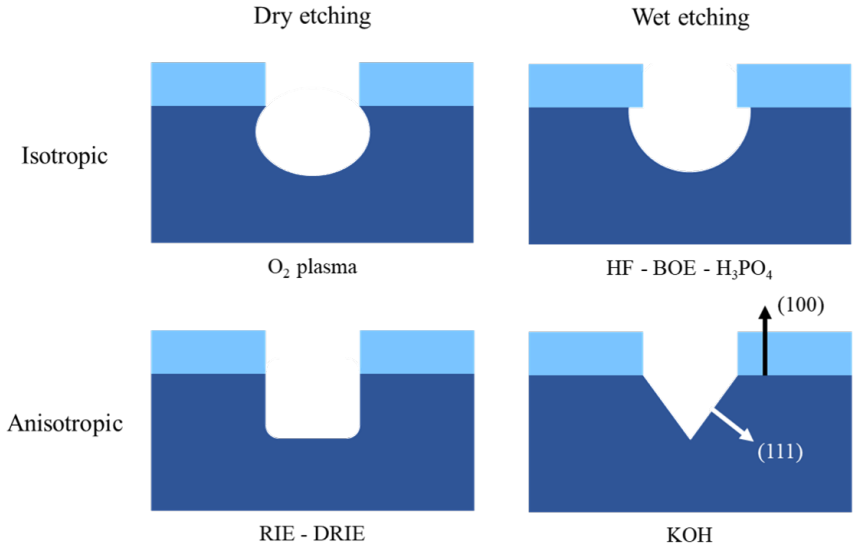


Figure 2.2: Schemes of the different type of etching profiles obtained through dry and wet mechanisms, depending on the isotropy of the process. Some example etching processes used in this work are listed below each profile.

are collectively referred to as reactive ion etching (RIE), even in cases where the ionized species do not chemically react with the substrate. In such instances, the etching is purely by physical sputtering (typically involving inert gases like argon). However, the anisotropy of these processes must be individually tailored by adjusting the gas flow and the directionality of the bombardment or by introducing passivating agents into the chamber, as otherwise the chemically driven reactions could lead to isotropic processes. A variation of RIE is Deep RIE (DRIE), which is based on the same principle but allows for very deep etching given the higher power and gas flows used. Both RIE and DRIE processes were extensively used in this thesis to etch Si, SiO_2, HfO_2 and Si_3N_4 with different chemistries. More in-depth explanations of these can be found in Section 5.2 and Section A.1. Lastly, a second block of dry etching also involves the use of a plasma, but this time without coupling it with directional bombardment. In this case, the etching is governed purely by chemical reactions (i.e. isotropic). The most widely used plasma etching in this work was O_2 plasma, which is especially suitable for photoresist stripping and for cleaning organic residues on samples.

2.1.5 Thermal processing

Thermal processing encompasses any thermal treatment applied to a sample to induce structural changes or phase transitions in a material. This includes treatments at constant temperature to force diffusive processes that are activated by temperature, such as BCP assembly or dopant diffusion; to enhance the quality and homogeneity of a given film, such as the improvement of SiO_2 density and purity (i.e. evaporation of organic contamination) after PECVD deposition; or to perform soft and hard baking of photoresists. Further explanations of these procedures and the reasons why they were necessary will be provided in their corresponding sections. In addition to these, rapid thermal annealing (RTA) involves exposing the sample to very rapid heating (in the range of seconds). These processes are typically used for dopant activation, to densify deposited films or to change the film-to-film interface properties. In this work, RTA processing was optimized to achieve an ohmic contact in metal-Si interfaces.

2.1.6 Doping

The doping process is essential in Si technologies to tailor the electrical conductivity of Si. In thermoelectric applications, achieving an optimal carrier concentration in Si is mandatory to ensure efficient thermoelectric generation. Doping is achieved by introducing impurities into an intrinsic semiconductor material. In the case of silicon, boron and phosphorus are commonly used to obtain p- and n-type doping, respectively. There are different strategies to achieve the desired doping level: ion implantation, in situ co-deposition and doping furnaces being the most common ones. The second involves the addition of dopants in the structure during the growth process. This method was used to dope the NWs, as explained in Section 2.1.8. The other two strategies are post-growth doping processes based on ion bombardment or thermal diffusion using dopant sources. However, the former is incompatible with nanostructured samples, as it causes severe film damage that requires post-annealing processes. The latter presents challenges related to cost-effectiveness and the use of hazardous precursors. An alternative is spin on dopant (SoD), which combines thin film deposition by means of spinning with a thermal diffusion process. This approach enables dopant incorporation without damaging the target film, while also being low-cost, simple, and avoiding the use of hazardous gas sources. This doping process begins by spin coating the SoD solution onto the sample, followed by ther-

mal baking to remove the solvent. A subsequent furnace-based diffusion process activates the dopant movement towards the underlying sample. The SoD typically consists of a polymeric matrix containing dopant precursors and SiO_2. Upon drying, a doped SiO_2 layer forms at the interface between the SoD and the silicon film, serving as the dopant source during the diffusion step. In the frame of this work, in-situ co-deposition was chosen to dope NWs, SoD to dope $\leq$ 50 nm thick device layers on SOI wafers, and ion implantation to dope the 15 µm thick device layer of SOI wafers (i.e. silicon microbeams).

2.1.7 Lift-off and patterning

The combination of the processes described above enables device fabrication, as it allows the definition of desired layouts across the various layers. The design definition can be divided into two basic blocks: lift-off and patterning. The first step involves the deposition of photoresist and the definition of the layout by photolithography, followed by the deposition of the material of interest. Therefore, the material is deposited on the substrate only in those areas where no photoresist is present. Finally, the remaining photoresist is dissolved so that the material is left only on the substrate with the desired layout. The second method is based on the reverse process. First, the film is deposited on the substrate, followed by the photolithography patterning of the photoresist. Then, an etching process is used to eliminate the film from those areas where the photoresist is exposing the film. With the subsequent elimination of the photoresist, the film is left

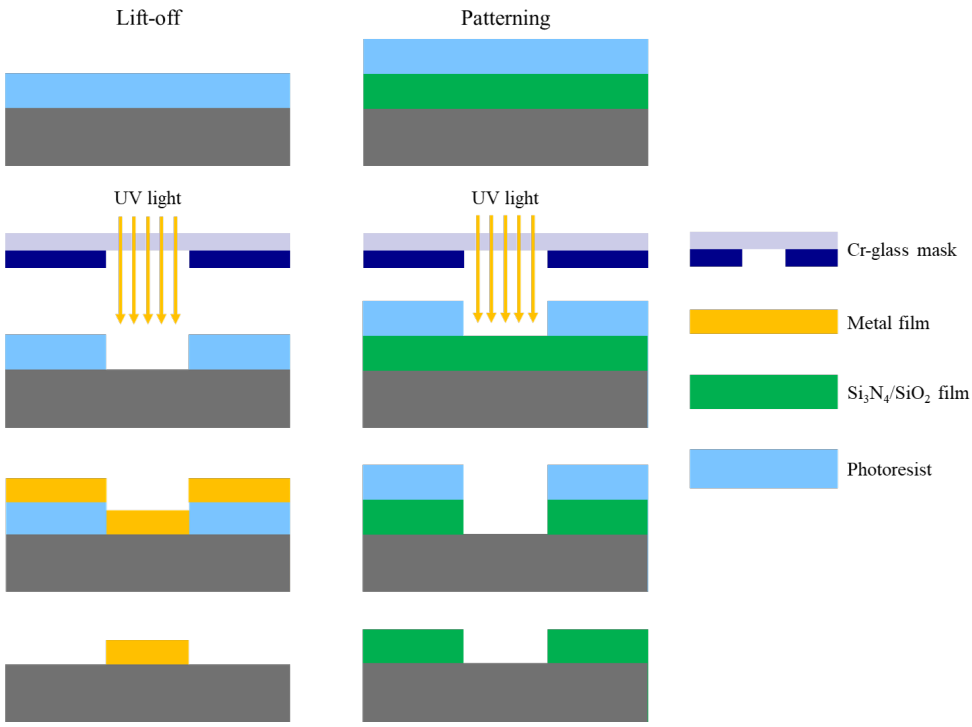


Figure 2.3: Schemes of the lift-off and patterning processes that are the basis for defining the layout of the different layers. Note that, despite using the same type of photoresist (positive in this example case), both processes define inverted patterns.

with the desired layout on the sample. Schemes of these two basic methods are shown in Figure 2.3. Iterating these two processes with some additional intermediate steps (i.e. thermal treatments or doping) a complete device can be fabricated. In this work, the lift-off process was used to define the metal designs, while patterning was applied in the definition of the Si, SiO_2, HfO_2 and Si_3N_4 layers.

2.1.8 Nanowire growth

The basis of the growth of Si NWs is the so-called vapor-liquid-solid mechanism (VLS) using CVD. This technique is based on a 1D bottom-up growth method that is assisted by a metal catalyst (gold in this work), which is deposited locally by galvanic displacement. This section will briefly explain the procedure of these two blocks: deposition of gold catalyst, and growth and integration of the NWs into the devices. Detailed information on the NWs growth and characterization can be found at [123]. The growth of the NWs used in this thesis was carried out by IREC at their facilities.

2.1.8.1 Galvanic displacement

The first step of the NWs growth consists of the deposition of the metal catalyst on the Si walls of the device. Gold is used as the catalyst metal due to several reasons [123]: it can be selectively placed on desired areas of the TEG, which is critical in our case as the NWs should only grow in specific regions of the device; it allows Si NWs to grow at moderate temperatures due to the low Au-Si eutectic point (363°C); Si NWs growth rate is fast due to the high solubility of Si in the Au-Si alloy; gold is stable under ambient conditions.

The technique employed for gold seeding is galvanic displacement, which is an electroless metal deposition procedure (i.e. does not need an external current source to be activated) done in an aqueous environment. This method is based on a spontaneous redox type reaction that takes place between the Si substrate and the liquid solution, which is composed of HF, sodium tetrachloroaurate(III) dihydrate ($NaAuCl_4$) and deionized water

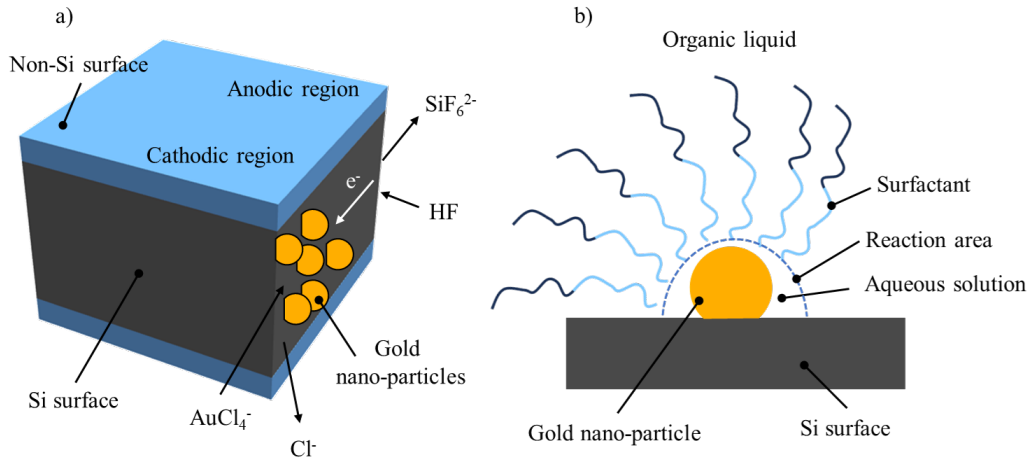


Figure 2.4: Schemes of: a) galvanic displacement reaction when a Si surface is present, b) effect of the surfactant and organic liquid addition on the area of reaction.

(see Figure 2.4). Thus, the overall process is selective to the substrate, and the metal will only be deposited in the zones where Si is exposed. During the reaction, solid Si is etched by HF, forming Si hexafluoride ions (SiF_6^{2-}) as follows:

$$Si_{(s)} + 6\ HF_{(aq)} \rightarrow SiF_6^{2-}{}_{(aq)} + 6\ H^+_{(aq)} + 4\ e^-$$

being (s) and (aq) solid and aqueous states, respectively. The other part of the reaction takes place between the electrons generated in the first reaction and the $AuCl_4^-$ ions in the solution:

$$AuCl_4^-{}_{(aq)} + 4\ e^- \rightarrow Au_{(s)} + 4\ Cl^-{}_{(aq)}$$

In this way, an Au film is deposited on the Si surface. However, for the growth of the NWs, nano-particles of Au are needed to work as catalyst seeds. To achieve this, a surfactant is added to the solution with an organic liquid (dioctyl sulfosuccinate sodium salt (AOT) and N-heptane in this work, respectively), creating a microemulsion that mixes both phases. This organic part doesn't interfere with the aforementioned reactions but forms micelles with a size related to the AOT/H_2O ratio. This size is then related to the diameters of the gold nano-particles that are deposited on the Si surface. The reason for this is that the organic liquid fraction in the emulsion is higher than that of the aqueous phase, which leads to micelles that encapsulate the aqueous solution. As a result, the reaction only occurs within micelles of a defined diameter.

2.1.8.2 CVD-VLS growth

As it has been mentioned, the NWs growth was done using the VLS method. In this process, the precursor gases (silane (SiH_4) and diborane (B_2H_6) in our case) are introduced in the CVD chamber, where the Si substrate decorated with Au nano-particles is placed. Precursor molecules are adsorbed and decomposed on the Au surface (i.e. SiH_4 is decomposed to form solid Si and H_2 gas, which is then desorbed), forming an eutectic alloy with the Au droplets. Once the eutectic alloy becomes supersaturated, the

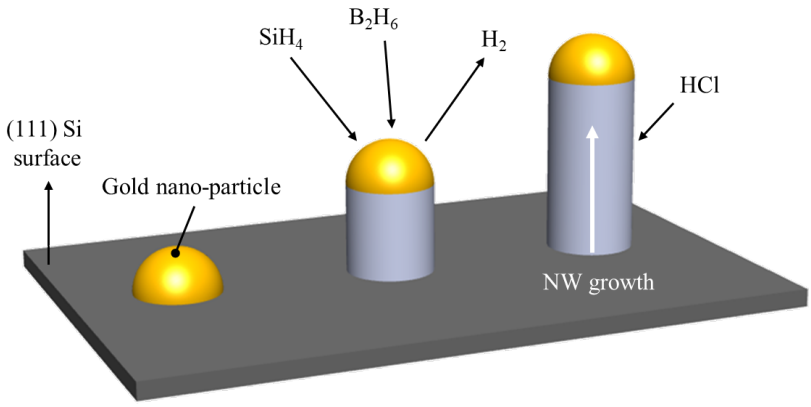


Figure 2.5: Scheme of the CVD-VLS process where the NW grows using the gold nano-droplet as a catalyst. The cylindrical geometry of the NWs in the scheme is used only for illustrative purposes. The NWs used in this work are hexagonal.

Table 2.1: Optimized parameters for the growth of Si NWs [124].

	Parameter	Value
Conditions	Temperature	630 ºC
	Total pressure	330 Pa
	Growth time	95 min
	Total gas flow	1250 sccm
Partial pressures	H_2	318 Pa
	SiH_4	3.35 Pa
	HCl	7.5 Pa
	B_2H_6	5.2 - 20.2 mPa
Gas ratios	SiH_4:HCl	1.5
	SiH_4:B_2H_6	1100 - 200

excess Si begins to precipitate, initiating the growth of the NW. The B_2H_6 contributes to the in-situ doping of the Si NW by adding B atoms in its crystal lattice. During this process, H_2 and HCl gases are also introduced in the chamber acting as carrier gas and to control Au migration and NW morphology, respectively. A scheme of the overall growth process can be seen in Figure 2.5. As the quality, distribution, morphology and size of the NWs are greatly affected by the CVD conditions during growth, these must be properly optimized. The NW growth optimization was done by IREC (the optimal parameters are listed in Table 2.1). It is important to note that NWs have a preferential growth perpendicular to the (111) surface. Thus, in order to correctly integrate these horizontally in our devices, the surface orientation of the used SOI wafers was chosen to be (110). In this way, the vertical walls of the trenches have (111) surface orientation. Lastly, an additional consideration regarding the NWs must be addressed. Although the growth direction is expected to follow the most energetically favorable crystallographic orientation, misorientations can occur, particularly when the Si surface is contaminated or covered by a native oxide layer. To mitigate this, an HF cleaning step was performed immediately before the CVD growth process. This minimizes misalignments due to the incorporation of oxide impurities in Si NWs. The thermoelectric properties of the NWs used during this thesis were measured in prior works [123], [125].

2.1.9 PS-b-PMMA

Several BCPs have been applied for lithographic uses throughout the years, such as Polystyrene-block-Polyisoprene (PS-b-PI), Polystyrene-block-Polybutadiene (PS-b-PB), Polystyrene-block-Poly (methyl methacrylate) (PS-b-PMMA) and Polystyrene-block-poly (ethylene oxide) (PS-b-PEO) [110], [126], [127], [128]. The first three have relatively low χ values, while the last is a high χ material, especially interesting for the fabrication of very small features. Anyhow, as explained in Section 1.3, the objective of this structure in the thesis is to enhance the zT value of Si. This involves nanostructuring Si to the extent where phonon scattering increases but not to the point where the electrical conductivity

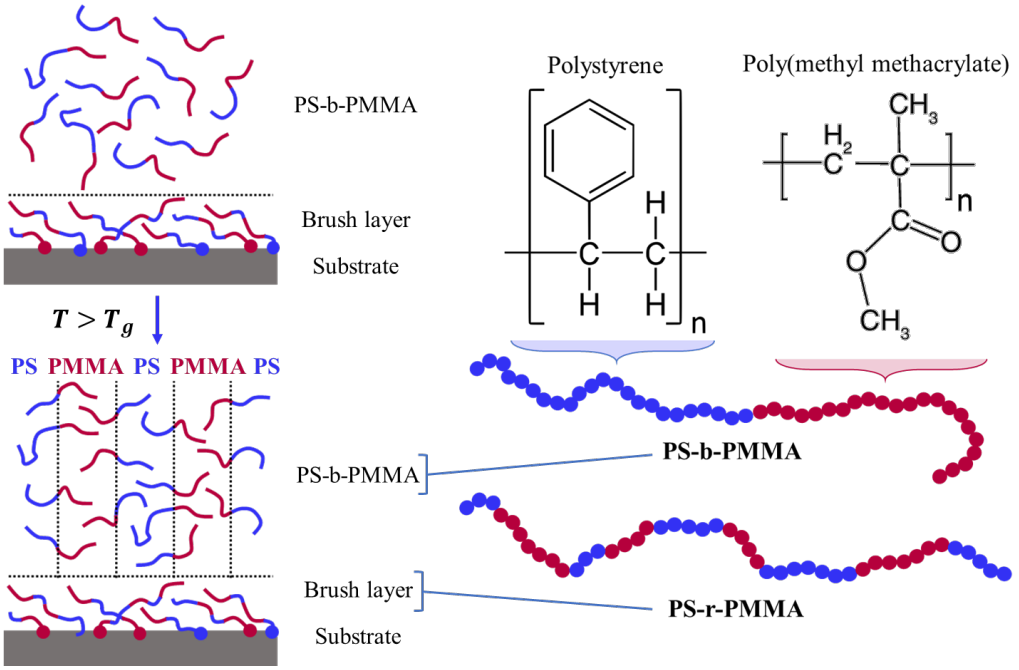


Figure 2.6: Scheme of the thermally driven diffusion process of a lamellar BCP. Distinct PS and PMMA domains are formed and the orientation of these phases is controlled with the help of a grafted monolayer of a random copolymer called brush layer.

is affected, meaning that the periods of the BCPs patterns should exceed, at least, 20-30 nm to be valid for thermoelectricity. These considerations discard the high χ BCPs and suggest the use of materials with lower χ values. Among them, PS-b-PMMA was selected for the following reasons. PS-b-PMMA is commercially available with precise molecular weight distributions and is especially interesting because both blocks have similar surface energy and affinity towards air. This facilitates their perpendicular orientation to the underlying surface, as none of them show preferential facing towards the air. Also, thanks to the use of a grafted random copolymer (PS-r-PMMA) monolayer between the surface and the PS-b-PMMA, there is great control of the domain orientation [129] (see Figure 2.6). The annealing temperatures needed to induce phase separation are low ($<$ 250°C), and the value of χ is relatively constant near these values as it only decreases from 0.043 to 0.038 when going from room temperature to 180°C [130], [131]. The periods compatible with ordered phases can reach a lower limit of 22 nm in both lamellar and cylindrical phases, and above this value BCPs form highly ordered domains. Regarding its compatibility with etching processes, PMMA can be easily removed and PS cross-linked without using destructive processes [132], [133], while also exhibiting great selectivity towards dry and wet etching processes with Ar and CHF_3 [134], [135], [136] and acetic acid [137]. Moreover, PS-b-PMMA is compatible with standard CMOS processes, and its deposition, annealing, and etching mechanisms can be introduced at a wafer scale in a CMOS fabrication process flow. This compatibility meets the requirements imposed by IoT applications for low cost, high-volume production of miniaturized devices.

2.1.10 Thin film nanostructuring

The nanostructuration process used in this work is based on transferring the nanoscale pattern formed by the BCPs into thin Si films. This approach requires the initial deposition and self-assembly of BCP films onto Si substrates with a controlled pattern orientation that enables the subsequent pattern transfer into the underlying Si layer. For this to be possible, the pattern must be oriented perpendicular to the substrate, as only this configuration results in a useful BCP mask for subsequent processing. As has been mentioned in Section 2.1.9, this is achieved by means of a brush layer to control the surface affinity of both BCP components towards Si. In both processes, the films are spin coated using a solution of random copolymers (i.e. brush) or BCPs. This allows good control of the film thicknesses, which is also essential to achieve the desired pattern orientation. Moreover, an annealing process under an inert atmosphere is used to trigger the grafting of the brush and the self-assembly of the BCP. In depth explanations of the optimization of all these steps are shown in Section 5.1.

The next step corresponds to the pattern transfer into the Si film. This process is divided in two etching steps. First, the PMMA component of the BCP matrix is eliminated, which was accomplished through both dry and wet etching mechanisms in this work. This leads to the definition of a PS mask with a given thickness, which can then be used to etch the underlying Si substrate. This second process was carried out using RIE. However, precise optimization of the RIE process is needed to ensure complete anisotropy in the etching. Without such control, the small lateral spacing between the holes in the PS mask can lead to mask detachment, compromising pattern fidelity. Thus, the error margin in the etching isotropy that is compatible with the direct pattern transfer

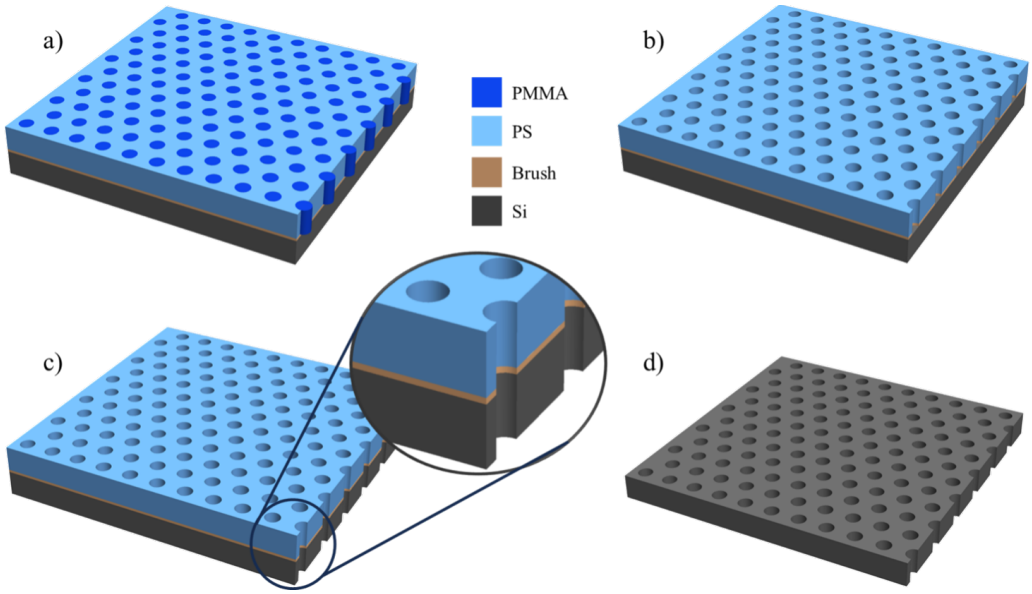


Figure 2.7: Scheme of the nanostructuration of a Si thin film. a) Deposition of the brush and BCP films on top of the Si substrate. Pattern formation with an annealing process. b) Etching of the PMMA (inner cylinders in our BCPs) and the brush under these areas. c) Pattern transfer of the BCP pattern using the PS as a masks with a RIE. d) Elimination of the remaining PS and brush films with oxygen plasma.

using BCPs is low and must be correctly assessed. Further explanations of this, as well as the optimization of the transfer procedure, are shown in Section 5.2. Finally, the remaining PS and brush films are eliminated from the sample using oxygen plasma. A scheme of this process can be seen in Figure 2.7.

2.1.11 Encapsulation and wire-bonding

In order to characterize the fabricated devices, electrical access to their metallic layers is generally needed. Although contacting via metallic probes is also a possibility and was used circumstantially during this thesis, the large number of pads that the devices have made encapsulation and wire-bonding more optimal. The encapsulation of the chips was done using different custom PCBs and conductive pastes depending on the chip design and the set-up at which the characterization was to be carried out. In some cases, the PCBs included custom jumpers to bypass broken platforms on the devices during full-chip characterization. Both highly conductive silver paste and H70 resin (electrically insulating and thermally conductive) were used for the encapsulation of the chips in the PCBs. Additionally, a graphite film was placed between the PCB and the chip to improve the thermal contact in the chips that were encapsulated using the H70 resin. For the wire-bonding, 25 µm thick aluminum wires were used in all the devices. Encapsulation and wire-bonding are critical in this thesis to achieve automatic characterization of the different devices. This includes thermal, electrical and thermoelectric characterization, and implies using different PCBs for each specific case.

2.2 Structural characterization methods

2.2.1 Scanning electron microscopy

Scanning electron microscopy (SEM) is based on imaging the electrons emitted from a sample when it is scanned by a focused electron beam. The interaction of the electron beam with the sample can lead to backscattered electrons (BSE), emission of secondary electrons (SE) and x-ray emission. BSE and SE are typically used for image reconstruction, as they provide information about the atomic number of the material and the surface topography of the sample, respectively. In this work, SEM was extensively used for the evaluation of the different samples during their optimization and fabrication steps.

2.2.2 Focused ion beam

Focused Ion Beam (FIB) combines a focused beam of ions with a scanning electron microscope (SEM), enabling precise milling, imaging, and modification of materials at the micro- and nanoscale. When the ion beam interacts with the sample, it can either sputter atoms from the surface or induce material deposition from a precursor gas. In this work, FIB was used to fabricate TEM lamellas and to etch selected regions of chips.

2.2.3 Transmission electron microscopy

Transmission electron microscopy (TEM) is based on imaging the transmission of an electron beam through the sample. It provides information about the crystallinity, lattice structure and parameters of the material. Since there is a maximum film thickness that is compatible with TEM imaging, this means that thin lamellas of the sample of interest

may need to be fabricated. TEM was used in this thesis to analyze the degradation of the Si NWs after several weeks of working under optimal power generation conditions, and to obtain precise images of the nanostructuration depth achieved with the pattern transfer process in different samples.

2.2.4 Ellipsometry

Ellipsometry is an optical technique that provides information on the thickness of a thin-film sample by analyzing the change in polarization of a light source after reflection from the film. A model based on Fresnel equations is used to fit the measured data. Since this model accounts for the optical parameters and thicknesses of the layers present in the sample, it allows for the calculation of each layer's thickness if its optical properties are known. Ellipsometry was employed in this thesis to characterize the BCP and brush thicknesses obtained with the different spinning conditions used.

2.2.5 Spectroscopic reflectometry

Spectroscopic reflectometry is a technique that provides information of the thickness of transparent and semi-transparent thin films based on the type of interference that a light source experiences after undergoing reflection and transmission on the film. By fitting the intensity versus wavelength data, the film thickness can be obtained. However, as the number of layers increases in the sample, so does the difficulty of resolving the multilayer. In this work, spectroscopic reflectometry was extensively used to characterize film thicknesses during device fabrication and to study the etch rates of RIE and wet etching on different materials.

2.2.6 Confocal microscope

Confocal microscopy is an optical imaging technique that constructs a 3D image of a sample by collecting sharp optical sections at different depths using optical sectioning and point-by-point scanning. However, since this technique is very sensitive in the depth direction, there are imaging limitations when the sample of interest has very rough surfaces. Confocal microscopy was used in this thesis to evaluate the depth and etch rates during the fabrication of samples, and to characterize the adapter pieces made with 3D printing and micro-machining techniques.

2.2.7 Glow-discharge optical emission spectroscopy

Glow-discharge optical emission spectroscopy (GDOES) provides an in-depth study of the presence of atoms in a sample and their relative concentrations by combining surface ablation using a plasma (i.e. by sputtering) with atomic emission spectrometry [138]. In this way, the atoms on the surface of the material are studied by bombarding it with an Ar plasma and then analyzing the emitted spectral lines of the sputtered material. As these lines are characteristic of each material and their intensities correspond to their abundance in the sample, this method allows for a qualitative in-depth analysis of the presence of each material by sequentially ablating the surface with glow-discharge plasma bombardment. GDOES was used in this thesis to measure the in-depth profile obtained after doping SOI samples with SoD.

2.3 Electrical characterization

This thesis includes different electrical characterization studies that were used to evaluate the doping processes and the resistivity of the thin Si films. Precise electrical conductivity characterization of Si NWs has already been performed in previous works [123], [125]. Si microbeams, on the other hand, are equivalent to bulk Si in terms of electrical conductivity. Besides this, a study of the doping of bulk Si using SoD was also conducted.

2.3.1 4-probe method

The most widely used characterization technique to obtain the electrical conductivity of thin films is the 4-probe method, as it does not require further fabrication steps to define a metallic layout. A schematic of the set-up used for this characterization is shown in Figure 2.8. A current is forced between the outer probes, while the inner probes are employed to measure the voltage drop. Considering only the contribution of an individual probe with a given current, the current density (J) at a given point, r, can be written as:

$$J = \frac{I}{A} = \frac{I}{2\pi r t} \tag{2.1}$$

being t the film thickness. Here, the area is considered to be the side of a cylinder, since the current is assumed to flow only laterally. Applying Ohm's law (E = ρJ, knowing E = -dV/dr), we can integrate the equation to obtain:

$$V - V' = \frac{\rho I}{2\pi t}[ln(r') - ln(r)] \tag{2.2}$$

Since the voltage is being measured between V_2 and V_3, and there are two current

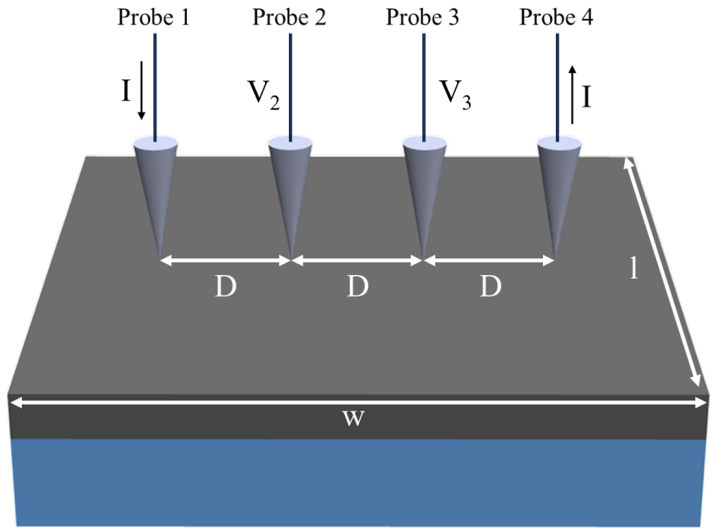


Figure 2.8: Scheme of the 4 probe method. The outer probes are used to force the current while the inner ones serve to measure the voltage.

contributions in the system (i.e.: +I in probe 1 and -I in probe 4), ΔV_{2-3} can be calculated as the sum of both contributions, each with their corresponding r and r$'$ distances to probes 1 and 4, using Equation 2.3:

$$\Delta V_{2-3} = \frac{\rho I}{2\pi t}[(2ln(2D) - 2ln(D)] = \frac{\rho I}{\pi t} ln2 \tag{2.3}$$

Therefore, the resistivity of the film is calculated with:

$$\rho = \frac{\pi}{ln2}\frac{\Delta V}{I} t = 4.53236 \frac{\Delta V}{I} t \tag{2.4}$$

However, this is only valid if the film is assumed to be semi-infinite (i.e. width and length of the chip, w and l, >> D). As this is not the case in reality because the samples are measured at chip level, a correction factor has to be introduced in Equation 2.4, as was shown by *L. B. Valdes* [139]. In our case, the resistivity was measured in square chips of 1x1 cm^2 or 0.8x0.8 cm^2 (w/l = 1) with a separation distance between probes of 1 or 0.8 mm respectively (w/D = 10). Therefore, a correction factor of 0.9313 was used. It is also important to note that the measurements of SOI Si films were done on bulk chips because the electrical conductivity of the underlying BOX layer is negligible compared to that of doped Si. Thus, suspending the films is not necessary.

2.3.2 Transmission line method

In addition to the electrical conductivity of the thermoelectric element, the overall electrical resistance of the generator is also affected by the contribution of the contact between the Si films and the metallic layers. The importance of reducing the overall resistance of the TEG was already shown in Section 1.4.1. Therefore, this contribution should be minimized. A standard technique extensively used to measure the resistivity of a metal-semiconductor contact is the so-called transmission line method (TLM).

This method is based on measuring the electrical resistance between consecutive metal pads separated by different distances (see Figure 2.9). In each measurement, the total resistance is the sum of the resistance of the film itself, which is proportional to its length, plus two film-metal contact resistances: $R_T(L) = R_{Film}(L) + 2R_C$. This can be rewritten as:

$$R_T = 2R_C + R_S \frac{L}{W} \tag{2.5}$$

being R_S the sheet resistance of the film and W its width. Thus, by plotting the different resistances measured as a function of their lengths, a linear fit is obtained, which can be used to extrapolate the case $L = 0$. In that case, the total resistance is the sum of the two contact resistances. However, the value of contact resistance cannot be transferred to a pad with a different geometry and, thus, its resistivity must be calculated. Due to the current crowding effect, this calculation is not straight-forward, as the current through the contact does not flow homogeneously across the entire pad surface, but tends to accumulate at its edge. This leads to an effective contact length that is smaller than the total pad length, which is known as the transfer length, L_T:

$$L_T = \sqrt{\frac{\rho_C}{R_S}} \tag{2.6}$$

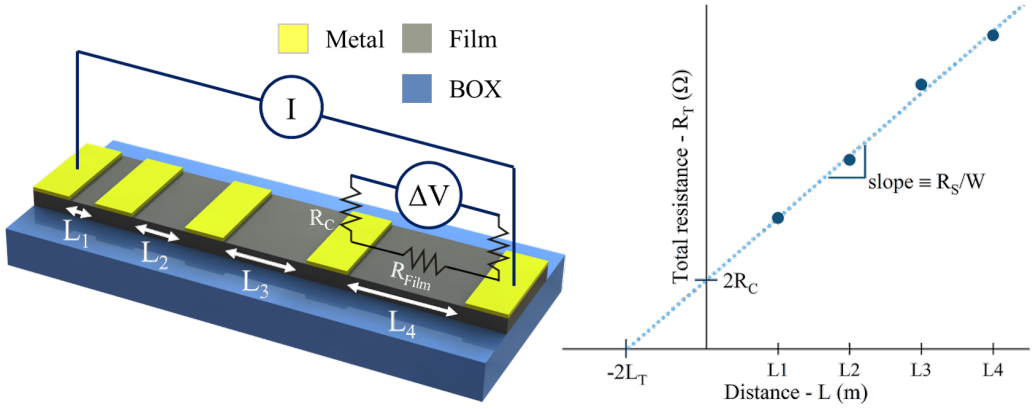


Figure 2.9: Scheme of the transmission line method (TLM) characterization with the correspondent electrical circuit. The right plot shows a typical result obtained with this method, where the slope of the linear fit is proportional to the sheet resistance and the intercept corresponds to twice the contact resistance.

where ρ_C is the contact resistivity. Thus, the contact resistance can be calculated as the ratio between the contact resistivity and the contact area (i.e. W·L_T). Finally, the contact resistance equals:

$$R_C = \frac{\rho_C}{L_T W} = \frac{R_S L_T}{W} \tag{2.7}$$

Using this equation, we can obtain L_T with the measured R_S, R_C and W, and later use L_T to calculate ρ_C of the contact.

2.4 Thermal characterization

Thermal characterization is fundamental for the evaluation of thermoelectric materials, and it is even more important in the case of silicon to evaluate the effect of nanostructuring. This thesis has used 3 methods to evaluate the thermal conductivity of Si thin films ($\leq$ 50 nm thick): 3ω steady state, frequency-domain thermoreflectance and bridge/laser method. Precise thermal conductivity characterization of Si NWs has already been conducted in previous works [123], [125]. Si microbeams, on the other hand, are equivalent to bulk Si in terms of thermal conductivity. In some of them, it was necessary to develop the methodology for the characterization of the materials and devices, while in all cases, specific test structures were fabricated. Among other challenges, this required suspending silicon-only structures, which made the process more costly and difficult. 3ω steady state was carried out with the collaboration of the Autonomous University of Barcelona, while frequency-domain thermoreflectance and bridge/laser method were performed during a PhD internship in the University of Basel.

2.4.1 3ω steady state

The devices fabricated for these measurements were initially designed for 3ω characterization. However, this was ultimately not feasible due to limitations of the 3ω setup.

Despite this, the same devices were used for the thermal characterization of films using a steady state method, which will be referred to as 3ω steady state from this point on. Figure 2.10 presents a scheme of the device. It consists of a suspended membrane with a metallic stripe deposited on top and an insulating film between the two layers. In this configuration, the two voltage probes are placed at a specific distance from the edge of the membrane to ensure that the heat flow remains perpendicular to the heater in this region. The heat flow lines curve beyond the voltage probes due to the presence of bulk Si. For clarity, this bulk region is not shown in the image; however, the membrane is surrounded by bulk Si on all four sides.

The characterization is based on forcing heat dissipation by means of an electrical current that flows through the heater/sensor line. Heat is dissipated through Joule heating, with power proportional to the square of the current. The chip is placed on a hotplate, and different current sweeps are applied to the heater while monitoring the resistance change through the voltage probes (of the same metal stripe). In this configuration, the conductance of the membrane equals:

$$G_{membrane} = \frac{P}{T_{Heater} - T_{Hotplate}} \tag{2.8}$$

where P is the Joule heat dissipated on the metal stripe. This model assumes that the edge of the membrane in contact with the bulk is at the hotplate temperature. In the measurement, a linear fit of the resistance versus squared current plot allows the extrapolation of R_0 (i.e. the resistance of the heater at a given $T_{Hotplate}$ when no current is applied to the heater - Equation 2.9), which is then used to calculate the TCR of the heater (Equation 2.10). By using these two equations:

$$R = R_0 + m \cdot I^2 \tag{2.9}$$

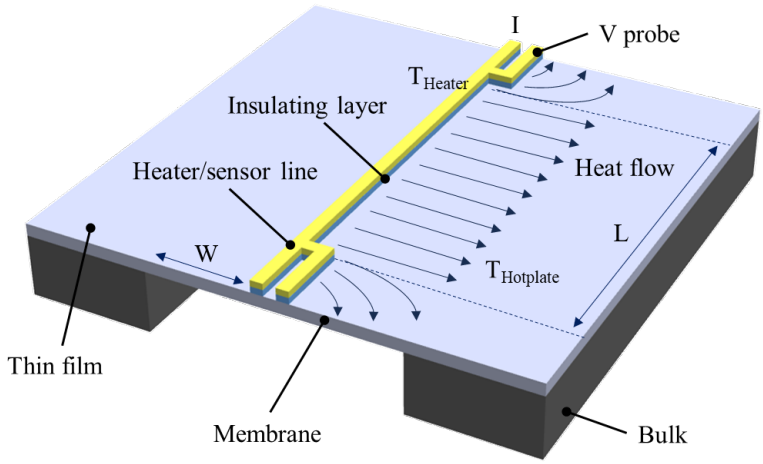


Figure 2.10: Scheme of the typical device used for 3ω characterization. A central metal heater in the middle of the membrane imposes a heat flux that is strictly perpendicular only in the central region of the membrane. The voltage probes, that are used to measure the change in resistance of the metal line, are placed in this area where heat is being conducted in a rectangular film with L and w dimensions.

$$R = R_0 \cdot [1 + TCR \cdot (T_{Heater} - T_{Hotplate})] \tag{2.10}$$

we can now write Equation 2.8 as follows:

$$G_{membrane} = \frac{R \cdot R_0 \cdot TCR}{m} \tag{2.11}$$

where m is the slope of the R vs I^2 curve. This is the formula used in this work to calculate the conductance of the film with the 3ω steady state method. Later, κ is calculated using the dimensions ($L \cdot W$) of the membrane.

2.4.2 Thermoreflectance

A different approach for measuring the thermal properties of thin films involves using photothermal phenomena. It is based on the change in the optical properties (i.e. the reflectivity in this case) of a material as a consequence of its temperature change. A pump and probe laser setup can be used to heat a sample and subsequently measure its temperature change by monitoring the variation in the intensity of the reflected probe beam. The pump laser heats the sample, typically using a transducer material to absorb the laser light and dissipate the heat on the film of interest, causing a subsequent thermal expansion of the transducer that is proportional to its temperature. This thermal expansion, by means of the piezo-optic effect, causes a variation in the reflectance properties of the transducer, leading to a change in the intensity of the reflected probe. As the transducer temperature depends on the thermal properties of the overall sample (i.e. the transducer layer and the film or films of interest, together with its geometry), the thermal conductivity can be obtained by measuring the reflectivity change.

Thermoreflectance characterization can be divided in two main groups: Time-domain thermoreflectance (TDTR) and Frequency-domain thermoreflectance (FDTR). TDTR is based on heating a sample with a pulsing pump laser, and then using a probe laser to measure the change in transducer reflectance over time. This implies having a delay between both lasers to characterize the device. FDTR, on the other hand, is based on heating the sample with a given modulation frequency, leading to a modulated change in the transducer's reflectivity that is measured while the pump laser is heating the sample (see Figure 2.11). Thus, the heating and characterization steps are simultaneous in FDTR. In addition, FDTR avoids the use of a pulsed laser system, which is highly expensive and complex. Since an oscillating heat is imposed on the system, a modulation of the transducer temperature is consequently observed. However, the important point here is that the temperature oscillations in the transducer suffer a phase delay with respect to the modulated heat caused by the diffusivity of the material (i.e. the time needed to increase its temperature). Thus, a phase lag is observed between both signals (i.e. the pump laser and the oscillating reflected probe), which depends on the frequency used and the thermal and geometrical properties of the sample. In this thesis, FDTR was the method selected for the characterization of thin Si films.

Up to this point, the working principle of FDTR has been explained, but a thermal model is still needed to relate the measured phase shift to the thermal properties of the system. The most common thermal model used for FDTR fitting is the quadrupole method. Parting from the heat equation, and after a Laplace transform, one obtains the following equation:

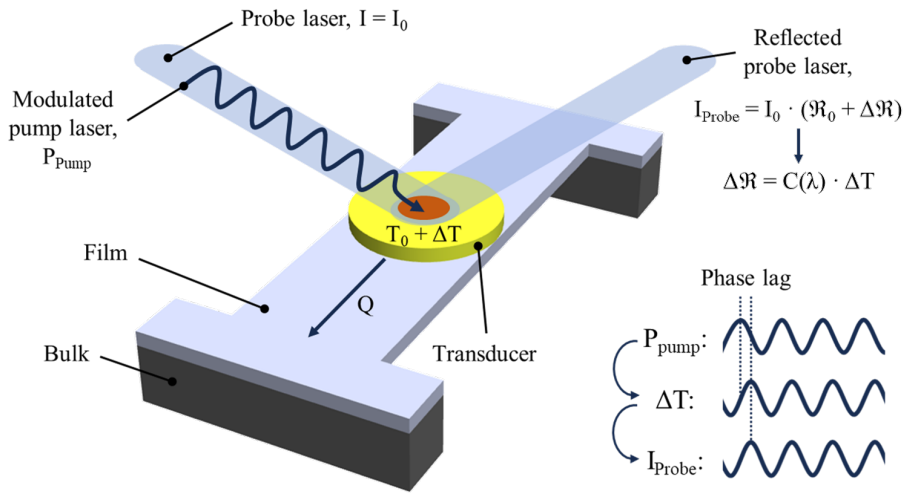


Figure 2.11: Scheme of the Frequency-domain thermoreflectance (FDTR) technique. A modulated pump laser heats up the sample. Simultaneously, a probe laser (not modulated), is reflected at the transducer. As the pump imposes an oscillating heat flux, temperature oscillations are caused in the sample with a given phase lag that is dependent on the thermal properties of the material. These lead to a sinusoidal change in the reflectivity of the transducer (proportional to the coefficient of thermoreflectivity, C(λ)), with the subsequent modulation of the intensity of the reflected laser, that has the same phase lag with respect to the pump laser. $\Re_0$ and $\Delta\Re$ correspond to the reflectance and change of reflectance on the transducer.

$$\frac{d^2\theta}{dx^2} - \frac{s}{\alpha}\theta = 0 \tag{2.12}$$

where s is the Laplace variable (s = i · ω; the real part of s is not considered, as it would represent exponential growth or decay over time, whereas this system focuses on the steady-state frequency response), α is the thermal diffusivity ($\alpha = \kappa/\rho \cdot C_p$), θ is the temperature in the Laplace space and x is the direction of the heat flux. By solving this equation and calculating heat flow in the Laplace domain (ϕ - using Fourier's law) we obtain the general solutions for θ and ϕ:

$$\theta = C_1 \cdot cosh(Kx) + C_2 \cdot sinh(Kx) \tag{2.13}$$

$$\phi = -\kappa AK \cdot (C_1 \cdot sinh(Kx) + C_2 \cdot cosh(Kx)) \tag{2.14}$$

where C_1 and C_2 are integration constants, $K = \sqrt{s/\alpha}$ and A is the cross-section of the film. By using the boundary conditions of θ(x=0) = θ_0 and ϕ(x=0) = ϕ_0, we can find the values of the integration constants: $C_1 = \theta_0$ and $C_2 = -\phi_0/\kappa AK$. Substituting now the input and output boundary conditions (θ_0 and ϕ_0, and θ_{out} and ϕ_{out}, respectively), the relation between them can be written as follows:

$$\begin{bmatrix} \theta_0 \\ \phi_0 \end{bmatrix} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \cdot \begin{bmatrix} \theta_{out} \\ \phi_{out} \end{bmatrix} \tag{2.15}$$

where M_{11}, M_{12}, M_{21} and M_{22} correspond to:

$$\begin{aligned} M_{11} &= M_{22} = cosh(Kz) \\ M_{12} &= \frac{1}{\kappa AK} \cdot sinh(Kz) \\ M_{21} &= \kappa AK \cdot sinh(Kz) \end{aligned} \tag{2.16}$$

Therefore, this matrix characterizes the thermal properties of a material with diffusive behavior, as it relates the temperature and heat flows on both sides (i.e. input and output) of the film. However, the complete thermal system that is being measured by the FDTR is also composed by the transducer (assumed to be thermalized at a uniform temperature but absorbing heat) and the different thermal contact resistances that may be present. Thus, it is necessary to define the matrices corresponding to these two cases (i.e. a purely capacitive mass and a purely resistive barrier, respectively), which can be written as follows [140]:

$$Capacitive \equiv \begin{bmatrix} 1 & 0 \\ C \cdot p & 1 \end{bmatrix}, Resistive \equiv \begin{bmatrix} 1 & R \\ 0 & 1 \end{bmatrix} \tag{2.17}$$

With all these matrices, the complete thermal system can be modeled simply by considering that a multilayer structure is mathematically equivalent to the multiplication of the matrices of each layer. For example, a system composed by a transducer on top of a film can be represented as the multiplication of a capacitive, a resistive (i.e. the thermal contact between the transducer and the film), and a diffusive matrix. This final matrix represents the overall system and relates the temperature and heat flows on both sides of the system. Lastly, it has to be considered that the parameter being measured with FDTR is the phase lag between the pump (i.e. ϕ_0, the imposed modulated flow) and the probe (i.e. θ_0, the temperature oscillations), which are both measured or imposed on the transducer. Thus, some assumptions must be made in Equation 2.15 in order to solve the system of equations and obtain a solution that relates ϕ_0 and θ_0 without the intervention of ϕ_{out} and θ_{out}. One possible assumption used in this work is to consider that $\theta_{out} = 0$, since θ is mathematically equivalent to $\Delta\theta$ and it is assumed that the end of the suspended film sees no change in temperature. See Section 6.2.3 for further details on the simulations that justify this assumption. With this approximation, and using Equation 2.15, we obtain the following relation:

$$\frac{\theta_0}{\phi_0} = \frac{M_{12}}{M_{22}} \tag{2.18}$$

where M_{12} and M_{22} are the corresponding elements of the matrix of the overall thermal system that is being measured. This ratio can be used to fit the measured data as a function of the imposed frequency to obtain the value of κ.

2.4.3 Bridge method

The bridge method involves evaluating the thermal properties of a material by suspending it between two thermally isolated platforms, which can be heated in a controlled manner (see Figure 2.12). Heating is achieved with two metallic heaters deposited on top of each platform, creating a thermal gradient across the sample. In this configuration, the platform is assumed to be thermalized and, thus, the temperatures at each heater and at the sample-platform contact points are considered to be the same. To measure each platform's temperature, the electrical characterization of the heaters has to be performed using the four point probe technique. However, when using a heater to increase the temperature of a platform, the metal traces on the supporting beams also contribute to the power dissipated on the platform and must be taken into account. In fact, half of the dissipated power in the metal traces on the beams flows towards the platform. Therefore, the total power dissipated in the platform is:

$$P_{Total} = P_{Meander} + \frac{1}{2} P_B \tag{2.19}$$

where *Meander* corresponds to the metallic serpentine on the platform and B to the beams (i.e. their metallic lines). P_{Total} can then either be written as P_H (heater) or P_S (sensor) depending on the use of each platform. The total dissipated power will flow through two different routes towards the bulk (which acts as a heat sink): through the heater beams or through the sample and the sensor beams (as this second route goes first through the sample and then through the sensor beams). Considering all this, the following equation can be written:

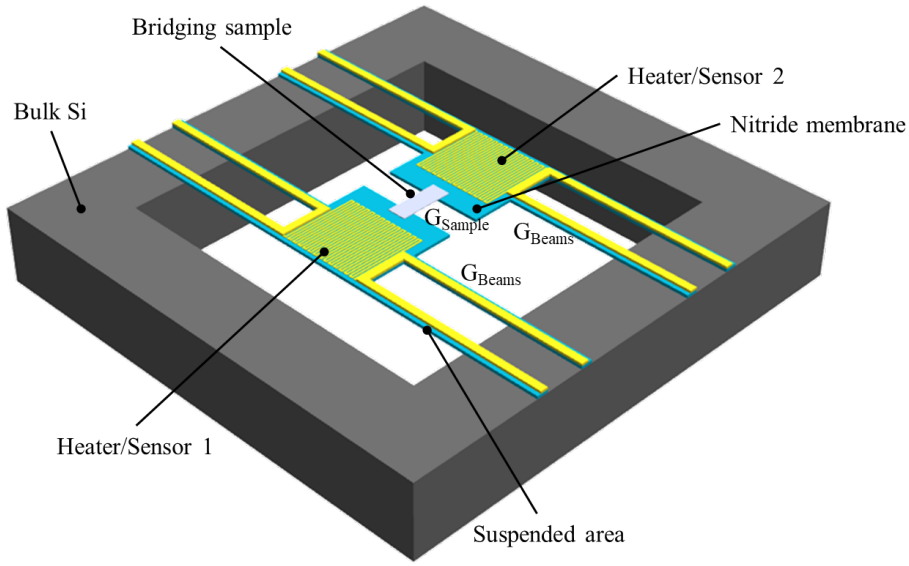


Figure 2.12: Scheme of the bridge device. A membrane of the material of interest bridges two suspended nitride platforms that are supported by elongated beams. On top of each platform, a heater is placed to generate a heat flow that propagates toward the other platform and the bulk through the membrane and the beams, respectively.

$$P_H + P_S = G_{B,H}\Delta T_H + G_{B,S}\Delta T_S \tag{2.20}$$

where *B,H* and *B,S* mean the beams of the heater and sensor platforms, respectively. This leads to the calculation of the beam conductance as follows (assuming the same conductance in both beams):

$$G_{B,S} = \frac{P_H + P_S}{\frac{G_{B,H}}{G_{B,S}}\Delta T_H + \Delta T_S} \rightarrow G_B = \frac{P_H + P_S}{\Delta T_H + \Delta T_S} \tag{2.21}$$

Finally, the heat balance also provides the conductance of the sample:

$$G_{B,S}\Delta T_S = G_{Sample}(\Delta T_H - \Delta T_S) \rightarrow G_{Sample} = G_{B,S}\frac{\Delta T_S}{\Delta T_H - \Delta T_S} \tag{2.22}$$

When using this method, the heater current is swept over a range of values, meaning that $\Delta \mathrm{T}_X/(\mathrm{P}_H{+}\mathrm{P}_S)$ can be rewritten as $\mathrm{d}\Delta \mathrm{T}_X/\mathrm{dP}$, with P denoting the total power ($\mathrm{P}_H{+}\mathrm{P}_S$) and X referring to either the heater or the sensor. With this new relationship, we can obtain the conductance values through the derivatives:

$$G_B = \left(\frac{d\Delta T_S}{dP} + \frac{d\Delta T_H}{dP}\right)^{-1} \tag{2.23}$$

$$G_{Sample} = G_B\frac{d\Delta T_S}{dP}\left(\frac{d\Delta T_H}{dP} - \frac{d\Delta T_S}{dP}\right)^{-1} \tag{2.24}$$

However, assuming that both beams in the device have the same conductance cannot always be true and may lead to errors in the calculation of the conductance of the sample. To correctly measure the beams conductance, the sample has to be considered completely symmetric. Then, the explained measurement is conducted in both directions, using first one platform as the heater and the other as the sensor, and then repeating the procedure but changing the heater and sensor platforms. In these conditions, and assuming G_{Sample} is equal in both directions:

$$\begin{aligned} G_{Sample} = G^*_{Sample} \rightarrow \frac{(P_H + P_S)}{\left(\frac{G_{B-1}}{G_{B-2}}\Delta T_H + \Delta T_S\right)} \cdot \frac{\Delta T_S}{\Delta T_H - \Delta T_S} = \\ = \frac{(P^*_H + P^*_S)}{\left(\frac{G_{B-1}}{G_{B-2}}\Delta T^*_H + \Delta T^*_S\right)} \cdot \frac{\Delta T^*_S}{\Delta T^*_H - \Delta T^*_S} \end{aligned} \tag{2.25}$$

where G^*_{Sample} is measured with heat flowing in the opposite direction to that in the G_{Sample} case. The solution to this equation using derivatives is:

$$\frac{G_{B-1}}{G_{B-2}} = \frac{-ABD{+}B^2D{+}BCD{-}BD^2{+}\sqrt{BD[4AC(A{-}B)(C{-}D){+}BD(A{-}B{-}C{+}D)^2]}}{2AD(A{-}B)} \tag{2.26}$$

with $A = dT_{Heater}/dP$, $B = dT_{Sensor}/dP$, $C = dT^*_{Heater}/dP^*$ and $D = dT^*_{Sensor}/dP^*$. Once this ratio is precisely calculated, it can be introduced in Equation 2.21 to obtain the conductance of the sensor-side beams. Later, this is used to calculate the conductance of the sample using Equation 2.24. The drawback of this type of measurement is that the conductance of the sample is not only the conductance of the material of interest, as this value also includes the thermal contact resistances with the platforms. This means that the obtained R_{Sample} corresponds to:

$$R_{Sample} = R_{Contact-1} + R_{Film} + R_{Contact-2} \tag{2.27}$$

Since the thermal contact resistances are unknown, the resistance of the film cannot be directly obtained using this procedure. Thus, a new type of characterization procedure is needed to obtain a precise measurement of R_{Film}.

2.4.3.1 Bridge method with laser heating

Coupling the bridge method structure with laser heating can overcome the problem of the contacts. This procedure is based on heating the sample that bridges the platforms with a laser and measuring the temperature increase in both platforms. However, in order to measure R_{Film}, this laser heating must be done in different positions on the membrane along its length (i.e. x direction). When the laser is pointed at a given x (with $x > 0$), part of the absorbed heat in the membrane flows towards the left platform and the other part towards the right one, leading to the following thermal balance (see Figure 2.13 for the equivalent thermal circuit of the system):

$$\frac{\Delta T^{Left}_{Laser-S}}{P_{Left}} = R_C^{Left} + R_{Film}\frac{x}{L} \tag{2.28}$$

$$\frac{\Delta T^{Right}_{Laser-S}}{P_{Right}} = R_C^{Right} + R_{Film}\frac{L-x}{L} \tag{2.29}$$

where $\Delta T^{Side}_{Laser-S}$ is the T gradient between the laser spot and the side sensor, R_C^{Side} is the contact resistance on each side, R_{film} is the resistance of the film and P_{Side} is the power dissipated by the laser on each side.

Therefore, by moving the laser in the x direction and measuring $\Delta T^{Side}_{Laser-S}/P_{Side}$ on both sides of the sample, the slope of the previous equations is obtained, which is proportional only to R_{Film}/L. Thus, the resistance of the film can be measured without the contribution of the contacts, which can be obtained through the intercept value. However, some properties of the device should be known before the experiment (i.e. the conductance of the beams and the TCR of the sensors). The conductance of the beams is needed to calculate P_{Right} and P_{Left} ($P_{Side} = \Delta T_S^{Side} \cdot G_B^{Side}$), while TCR is needed to obtain ΔT on both platforms. These parameters are previously obtained using the bridge method explained above. The last undetermined parameter is $\Delta T^{Side}_{Laser-S}$. To measure it, the temperature of the sample at the exact spot where the laser is focused is required. Raman thermometry could be used for this purpose, but very high powers are needed to resolve the Raman shift with sufficient precision. Interestingly, *Po-Ye Huang et al.* [141] have shown that there is another possibility to obtain the value of the temperature at the laser spot that does not require Raman thermometry, involving only electrical characterization. It consists of first heating the sample with the laser at a given

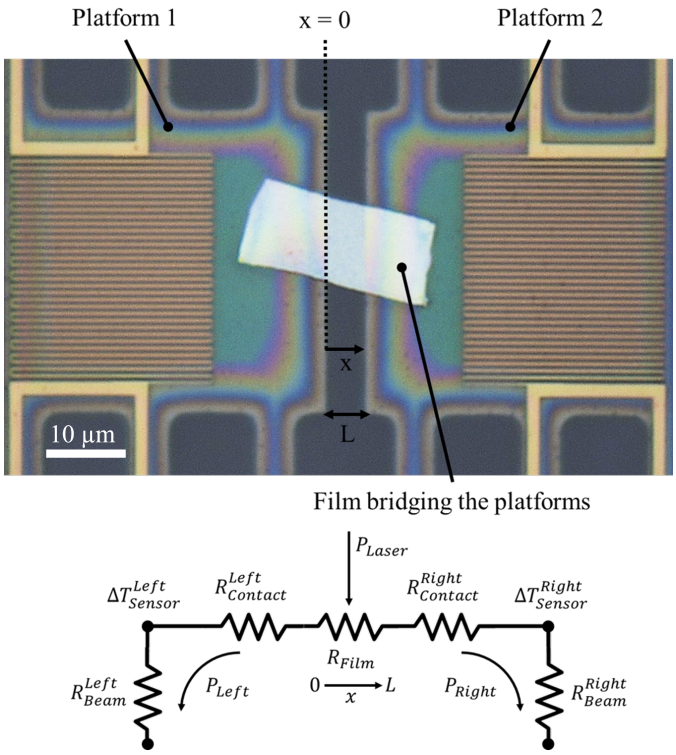


Figure 2.13: Image of one of the devices measured in this work with a membrane bridging the platforms. The laser is focused on the surface of the sample and swept from 0 to L, being L the gap between platforms. The corresponding thermal circuit of the system is shown below.

x position and then measuring ΔT_S on each side. Using these values, P_{Right} and P_{Left} can be calculated since the only contribution to their ΔT comes from the heat induced by the laser. The temperature profile as a function of the membrane position in this state is shown in Figure 2.14a. Then, a current is forced in one of the sides, left for example, to compensate for the laser power that is arriving at this side (P_{Left} in this example case). After achieving this, the system reaches a second state (see Figure 2.14b), where $\Delta T_S^{Left*} = T_{Laser}^*$, since there is no heat flow between these positions due to the heat compensation provided by the power dissipated in the left heater. Also, the power now reaching the right sensor is P_{Laser}, since it includes both the contribution from P_{Right} of the laser and the power dissipated by the left heater, which equals P_{Left} due to flow compensation. Obviously, in both states, the thermal resistance between the laser spot and the right sensor is the same, leading to the following equality:

$$\frac{T_{Laser} - \Delta T_S^{Right}}{P_{Right}} = \frac{T_{Laser}^* - \Delta T_S^{Right*}}{P_{Laser}} \tag{2.30}$$

This equation can be used to obtain the value of T_{Laser} in the initial state since the rest of variables are measured (as $T_{Laser}^* = \Delta T_S^{Left*}$). By doing this at different x positions along the membrane length, T_{Laser} is obtained, and $\Delta T_{Laser-S}^{Side}$ can be calculated

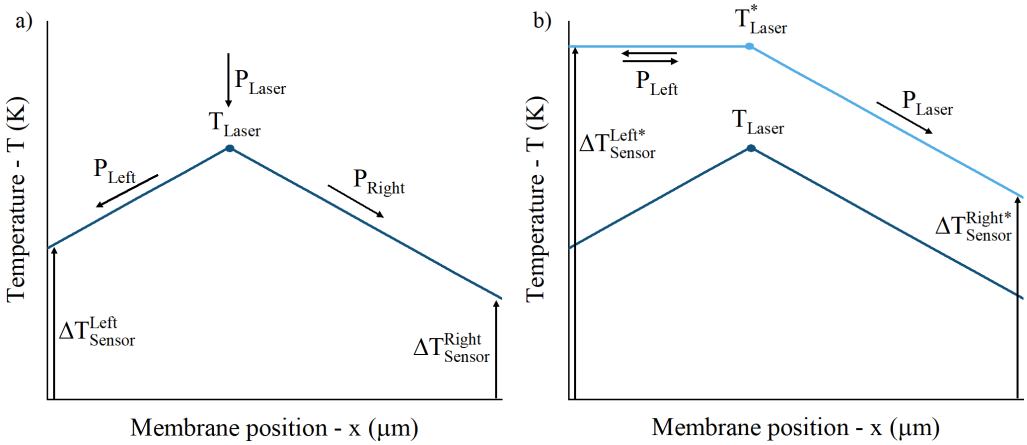


Figure 2.14: Example plots of the two states needed to calculate T_{Laser} with only electrical characterization. a) The sample is heated in a given x position with the laser and two ΔT are measured in both sides. b) P_{Left} is compensated by adding power with the left heater. In this second state P_{Laser} flows towards the right sensor and $\Delta T_S^{Left*} = T^*_{Laser}$.

for all x. However, it is important to note that the total power dissipated in the heater is not just P_{Left}. In order to reach the second thermal state (Figure 2.14b), the power dissipated towards the right platform (i.e. through the sample) must be P_{Left}. However, part of the heat dissipated in the left heater also flows toward the bulk through its beams. Therefore, the power that should be dissipated in the left heater must be calculated. Since the right sensor will detect an increase of P_{Left} in the second state, and this same P_{Left} caused a ΔT_S^{Left} that was measured in the first state, we have the following equality:

$$(\Delta T_S^{Right*} - \Delta T_S^{Right}) \cdot G_B^{Right} = \Delta T_S^{Left} \cdot G_B^{Left} \rightarrow$$

$$\rightarrow \Delta T_S^{Right*} - \Delta T_S^{Right} = \Delta T_S^{Left} \cdot \frac{G_B^{Left}}{G_B^{Right}} \tag{2.31}$$

Therefore, the amount of ΔT caused by the added P_{Left} on the right sensor in the second state will be ΔT_S^{Left} if both platforms beams have the same conductance. Otherwise, the ratio between them will give the ΔT that should be added to the right sensor to obtain the second state. Once this ΔT is known, the amount of power that should be dissipated by the left heater can be calculated using the following equation:

$$P_H^{Left} = (\Delta T_S^{Right*} - \Delta T_S^{Right}) \cdot \left(\frac{d\Delta T_S^{Right}}{dP^{Left}} \right)^{-1} \tag{2.32}$$

For this calculation, the value of $d\Delta T_{Sensor}/dP$ obtained previously with the bridge method is used. Finally, by plotting $\Delta T^{Side}_{Laser-S}/P_{Side}$ versus the position, R_{Film} is obtained. Thus, this method allows for a precise measurement of the R_{Film} regardless of the membrane-platform contact. However, a prior bridge characterization of the sample is required to obtain the parameters needed for the calculations.

2.4.4 Temperature coefficient of resistance

The Temperature Coefficient of Resistance (TCR) is a parameter that quantifies how the electrical resistance of a material changes with temperature. In thermal and thermoelectric measurements, it is necessary to know the TCR of the heaters and thermometers of the devices in order to properly assess the temperature in the different regions. In principle, their TCR values should be the same if they are made from the same metal, but the characterization results have shown that they can have small differences that should be taken into account to obtain an accurate evaluation of the temperature. Therefore, TCR characterization was carried out for each heater and thermometer individually in this thesis. The TCR relates the change in temperature of a material to the consequent change in its electrical resistance, and can be written as follows:

$$R = R_0 \cdot [1 + TCR \cdot (T - T_0)] \tag{2.33}$$

where R is the resistance value at a given temperature T, and R_0 is the resistance at a reference temperature T_0. The TCR is positive in metals and heavily doped semiconductors, while it shows a negative value in intrinsic semiconductors. Therefore, metals show an increase in electrical resistance when their temperature increases.

TCR evaluation of heaters and thermometers on the devices is completed after mounting and wire-bonding the µTEGs onto specifically designed PCBs. The PCBs are compat-

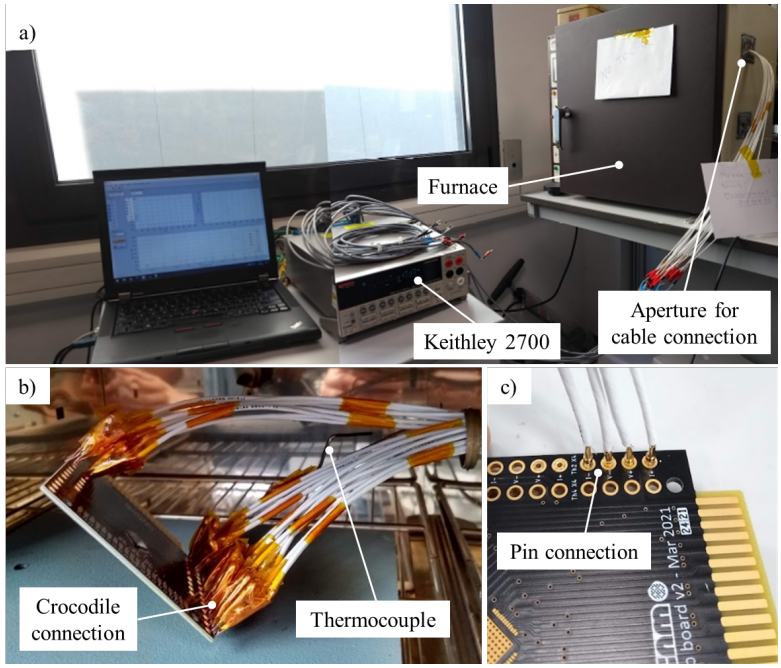


Figure 2.15: Images of the TCR characterization setup. a) General image of the setup with the cables introduced inside the furnace where the TCR studies were carried out. b) Chip mounted on a PCB with external connections using crocodiles. A thermocouple is placed near the PCB. c) Detail of the PCB connection when using pins. Both types of connections were used in this thesis.

ible with the required temperature conditions (up to 250°C) and include plated through-holes along the sides, allowing electrical connection to the µTEG pads using cables with pins or crocodile clips, thus avoiding the need for soldering (see Figure 2.15). The PCBs are introduced into a furnace to ensure that they are exposed to a homogeneous temperature throughout the characterization. The oven temperature is monitored with a type-K thermocouple placed near the PCB. A Keithley® 2700 Multimeter with a 7700 multiplexer expansion card is used during the resistance measurement for each of the heaters/thermometers using a 4-wire configuration. A custom LabVIEW program is used for the simultaneous TCR characterization of all the heaters and thermometers of a chip.

2.5 Thermoelectric characterization

The setup used in this thesis is specifically designed to automate the thermoelectric characterization of the µTEGs. This includes both the characterization of their Seebeck coefficient and their performance under different environmental conditions. A general view of the characterization setup can be seen in Figure 2.16.

The PCB with the µTEG is mounted on top of a hotplate with the help of screws and a Thorlabs® piece with micro-metric control in the z axis to ensure good thermal contact. The temperature control of the hotplate is achieved through a PID controller (OMRON E5DC), which is connected to the PC and governed by a central LabVIEW program. The setup allows three main convection configurations: insulation cage (the device is exposed to natural convection conditions only through the top opening of the cage, which makes the air temperature above the chip more stable), standard natural convection (fully exposed to the ambient, without cage), and forced convection (a variable

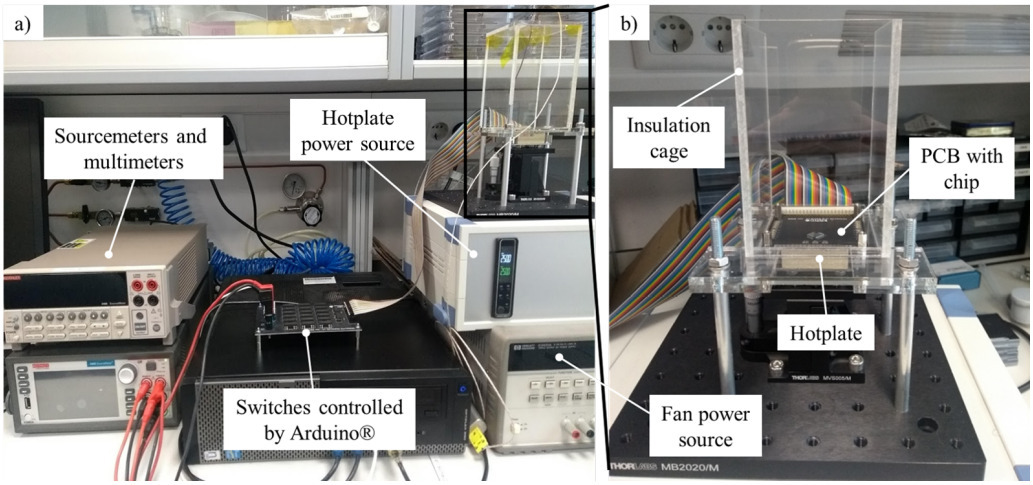


Figure 2.16: Images of the thermoelectric power characterization setup. a) General view of the setup with the sourcemeters connected to the PCB by means of miniature reed relays controlled by an Arduino® board. A 40-pin connector with a ribbon cable is used to interconnect the relays with the PCB to route the desired platform. The hotplate and fan power sources are located underneath the PCB. b) Picture of the PCB with the chip on top of the hotplate. A PMMA cage is used to ensure a stable ambient temperature on the chip.

speed fan forces a horizontal airflow close to the chip). The characterization of the µTEG is performed with two sourcemeters (Keithley 2400 and Keithley 2450) and a multimeter (Keithley® 2700). This allows for simultaneous monitoring of internal and external collectors, heaters, and thermometers of the µTEG. The connection between the PCB and the sourcemeters/multimeter is established through a 40-pin connector, a ribbon cable, and a custom board equipped with several miniature reed relays. These relays are controlled with an Arduino® board via USB commands sent by the central LabVIEW characterization program. This allows for the sequential selection of the pins of each platform in a device in order to perform measurements on all platforms within a single characterization process.

The setup has two operating modes: "test" mode, in which the temperature on both sides of the TE material is controlled through the hotplate and the heater integrated in the µTEG, and "harvesting" mode, in which power generation is evaluated by applying heat only through the hotplate.

2.5.1 Seebeck coefficient

The test mode is used to evaluate the Seebeck coefficient, which describes the relationship between the generated voltage (i.e. the V_{OC}) and the temperature gradient:

$$S = -\frac{V_{OC}}{\Delta T} \tag{2.34}$$

In this case, the devices under test have suspended platforms with integrated heaters and a thermometer on the silicon bulk. By controlling the chip temperature through the hotplate (monitored by the integrated thermometer) and imposing a higher temperature on the platforms through the heaters, the V_{OC} between the collectors can be measured. As the thermal gradient across the thermoelectric element is controlled, the Seebeck coefficient, S, can be calculated. The procedure requires that the TCR of the heaters and thermometers is estimated beforehand (see Section 2.4.4). Different hotplate temperatures are forced to obtain S as a function of the temperature.

2.5.2 Thermoelectric power

Proper characterization of µTEG's power generation capabilities requires exposing it to conditions equivalent to real operating scenarios. This is done through the mentioned harvesting mode, where heat is applied only through the hotplate. In these conditions, the bulk part of the µTEG absorbs heat from the hotplate and achieves a given temperature gradient on its thermoelectric element. This gradient is achieved thanks to the heat exchange between a suspended platform (the cold end of the µTEG) and the environment. In these measurements, both short circuit current (I_{SC}) and open circuit voltage (V_{OC}) are monitored using the Keithley® 2450 sourcemeter. These values correspond to ideal states where the load resistance is infinite (V_{OC}) or zero (I_{SC}). Since the most relevant operating point lies between these states (i.e. in load matching conditions, see Section 1.2.1), after measuring V_{OC} and I_{SC}, a linear regression is performed using LabVIEW to obtain the power curves of the devices. This is possible because our TE behaves approximately as a purely resistive element, and each measurement is performed under stationary conditions (i.e. ΔT and average T remain approximately constant throughout the measurement). As a consequence, R_{int}, S and κ can be considered constant during characterization, resulting in a linear relationship between current and voltage. Moreover,

Joule and Peltier contributions (which could introduce non-linearities) are negligible due to the low currents employed. In this thesis, both natural and forced convection configurations were used to measure the thermoelectric power of the μTEGs. The latter allows for the study of their harvesting capabilities under enhanced heat exchange conditions with the environment.

Part II

Micro-thermoelectric generators based on silicon nanowires and microbeams

Chapter 3

Characterization of micro-thermoelectric generators

This chapter summarizes the work on the characterization of µTEGs based on Si structured in two different forms: arrays of Si microbeams and arrays of Si NWs. Si NWs, which are 1D nanostructures, show reduced thermal conductivity and higher electrical resistance compared to bulk Si (as shown in Section 1.3.2). In contrast, Si microbeams, which are defined by optical lithography and etching of bulk Si, share the electrical and thermoelectric properties of bulk Si. Therefore, µTEGs where the TE material is based on Si NWs may benefit from a higher thermal gradient for enhanced thermoelectric power, while µTEGs where the TE material is based on Si microbeams may show a higher power output resulting from their lower electrical resistance.

3.1 Micro-thermoelectric generators design

The basic operating principle of a planar TEG is the conversion of a vertical external temperature gradient into a lateral one. In our µTEGs, this is achieved by suspending platforms and integrating TE elements that laterally bridge the gap between these platforms and the surrounding silicon bulk (see Figure 3.1). The work presented in this chapter uses two types of chips: 4X and Parallel (see Figure 3.2). The first is designed for TE characterization purposes and enables a more detailed study of the device performance thanks to the heaters integrated into its platforms. The second is designed to maximize the generated power per unit area and is particularly suitable for harvesting studies under real operating conditions.

Figure 3.1a shows an illustration of the 4X chip for the case of Si NWs, in which four individual platforms are fabricated with an integrated heater. In the magnified image of the platform area (see Figure 3.1b), the main parts of the device are shown. The suspended platform, which is supported by a thin metal/nitride membrane on the internal collector side, and by Si trenches filled with arrays of NWs on the external collector side. The four platforms of the device have a different number of trenches connected in series (1 to 4) bridging the gap between the platforms and the surrounding

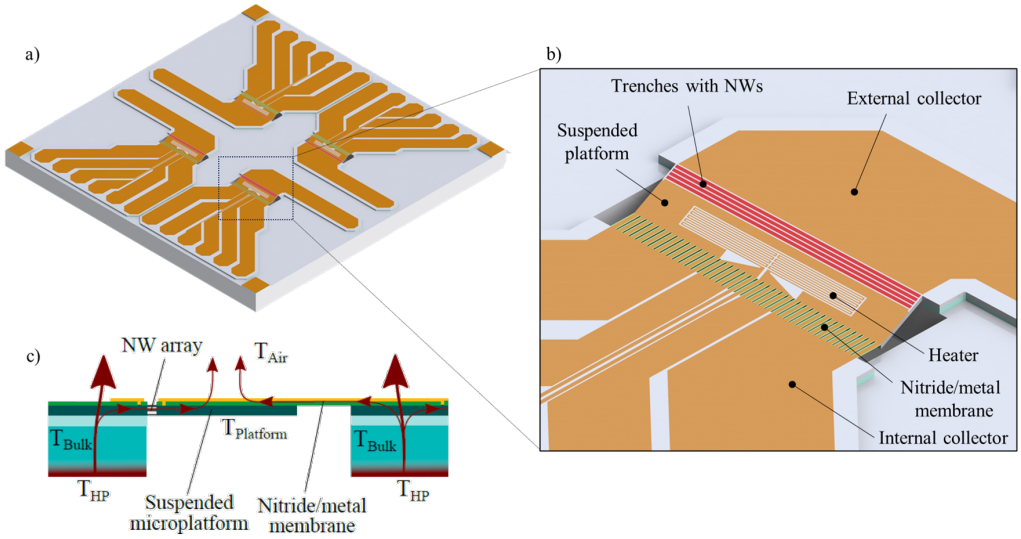


Figure 3.1: a) 3D illustration of the 4X type µTEG for Si NWs. It consists of four suspended platforms with integrated heaters. b) Amplified image of the platform area of the device. A suspended micro-platform is supported by a metal/nitride membrane (internal collector). Arrays of NWs fill the Si trenches that bridge the platform with the surrounding bulk (external collector). c) Cross-section of the device showing its working principle in harvesting conditions, where the bulk part of the chip contacts the hot surface. A lateral heat flow is created in the NWs and a temperature gradient is present between the bulk and the suspended platform. In the case of microbeams, the trenches are filled with arrays of them.

bulk silicon. This allows for the study of the optimal TE length, since there is a trade off in terms of thermal vs electrical resistance when varying the length of the TE element. The length and depth of these trenches is 15 µm, meaning that the total length of the TE leg varies between 15 (platform 1, T1) and 60 µm (platform 4, T4). Regarding the microbeams based TEGs, the general layout is the same, but the trench configuration is different. In this case, a different number of microbeams is integrated between the suspended platform and the external collector for each platform of the 4X chip. Despite that, the length of the trench is fixed at 15 µm. The number of microbeams (5 µm wide) are 3, 5, 9 and 17 depending on the platform (T1 to T4, respectively). This variation in the number of microbeams allows to study the occupancy rate influence (filled width over the total platform width) on device performance to determine the optimal point that best balances thermal and electrical resistance. The heat management in this kind of devices is shown in Figure 3.1c. Under harvesting conditions (when the chip is placed on a hot surface and the temperature gradient is established solely through the heat management of the chip) the bulk part of the device is heated, while the suspended platform is colder due to its contact with the cooler environment. Thus, a heat flow from the bulk converges into the platform and creates a lateral temperature gradient in the TE element integrated between the bulk silicon and the platform. This temperature gradient is converted into electricity by the TE material and collected by the internal and external collectors (platform and bulk metal layers, respectively) by means of an inter-level metal-Si contact through the insulating Si_3N_4 film. When the chips are evaluated

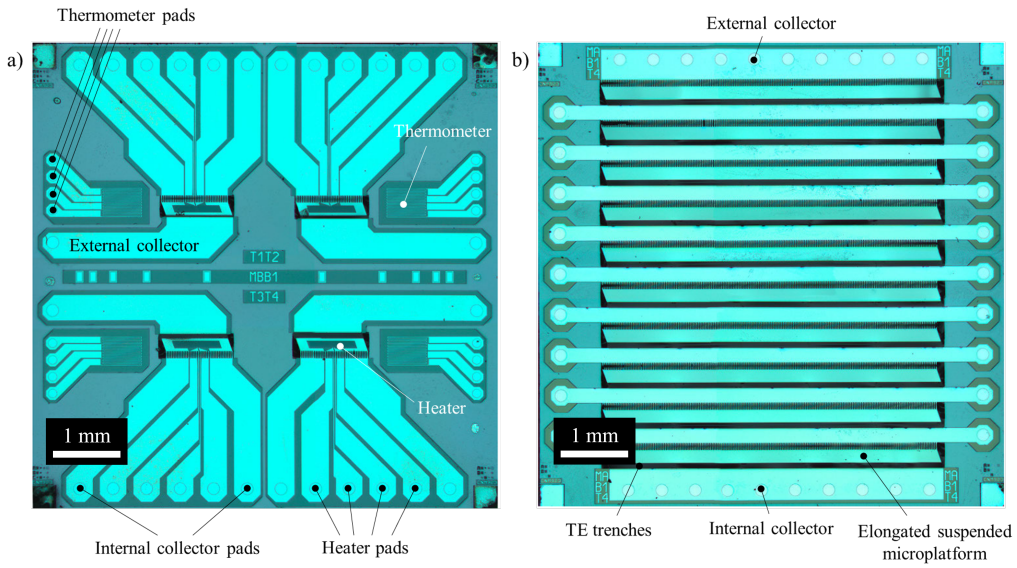


Figure 3.2: Optical images of the: a) 4X and b) Parallel chips used in this work. The Parallel chips includes 50 of the platforms of the 4X chip in parallel/series electrical connection.

in test mode, the temperature gradient is imposed by contacting the chip with a heat source while simultaneously applying a controlled temperature to the platform through the integrated heater. In this way, different temperature gradients can be obtained at each hot temperature. To precisely measure the temperature gradient, four thermometers are also implemented in the silicon bulk near each of the four platforms (see Figure 3.2).

The Parallel chip integrates several devices with the same design as those in the 4X chip, arranged to maximize power generation per unit area. The chip is 7x7 mm^2 and its active area is 0.6 mm^2 (i.e. total area with TE material). Five individual suspended platforms are connected in parallel to form an elongated one (i.e. the length of a 4X chip platform is 1 mm, whereas that of the Parallel chip is 5 mm, see Figure 3.2) and ten of these elongated platforms are connected in series, resulting in 50 individual platforms integrated in this device. To enable the characterization of individual elongated platforms, lateral pads are included on the chip.

3.1.1 Device fabrication

The fabrication of these chips uses a specific type of Silicon-on-Insulator (SOI) wafer with (110) orientation on the top Si layer. The reason for this orientation is the anisotropic behavior of Si etching with potassium hydroxide (KOH), which is essential for one of the fabrication steps, as will be explained later. A SOI wafer consists of a stack of three layers: a device or top Si layer, an insulating layer (the buried oxide, BOX, in this case), and a bulk Si substrate. The thicknesses of the SOI layers are 15 µm, 1.5 µm and 500 µm for the top Si, buried oxide and bulk Si, respectively. The resistivity of the device layer is 0.003 - 0.005 Ω·cm. A scheme of the fabrication steps is shown in Figure 3.3.

The process starts with a cleaning step in a piranha solution bath (H_2SO_4:H_2O_2 =

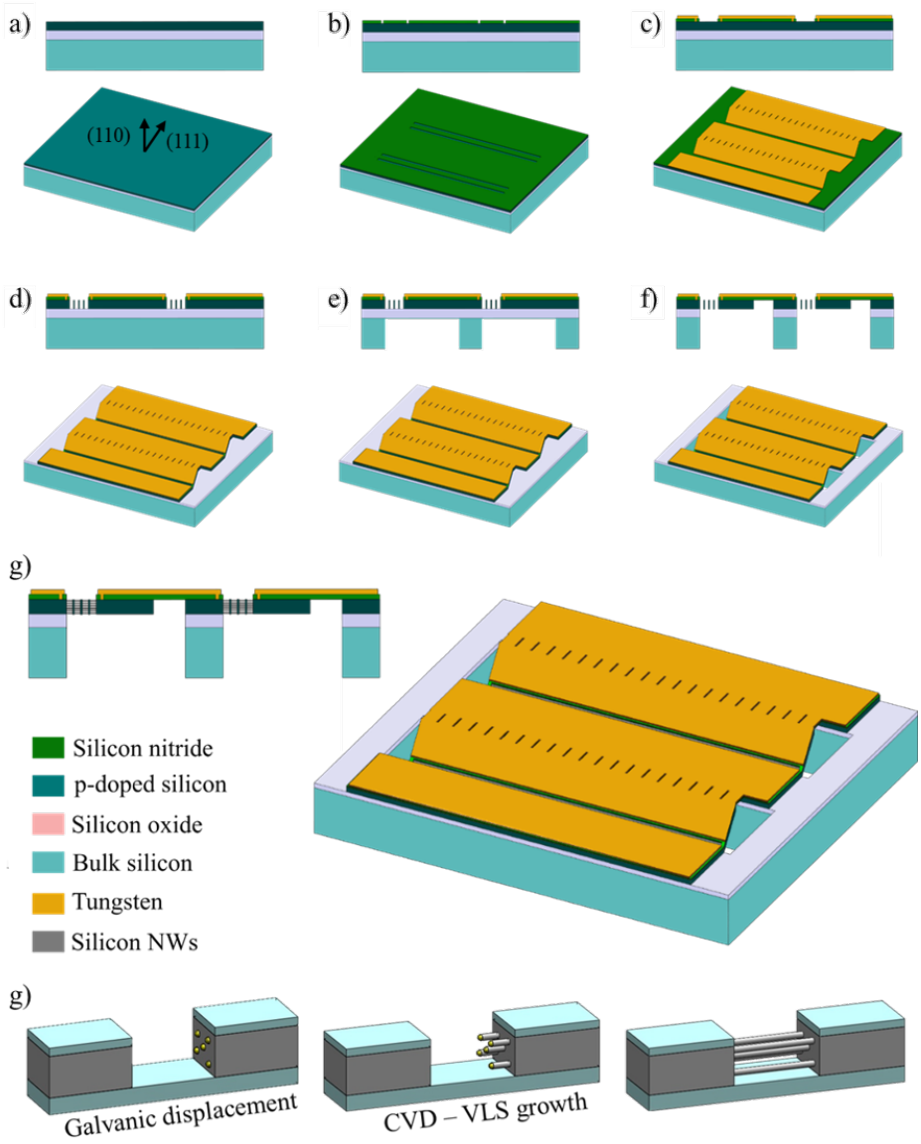


Figure 3.3: Scheme of the fabrication process for the 4X and parallel devices for Si NWs. a) SOI wafer with (110) surface orientation, b) Deposition of 300 nm thick Si_3N_4 by LPCVD and opening of the metal-Si inter-level contacts with RIE. Later, the Si_3N_4 is used as a mask for doping Si by ion implantation, c) Deposition of the metal (Ti/W, 30/200 nm) and patterning with a lift-off. RTA process (700°C during 30s) to achieve metal-Si ohmic contact, d) Definition of the platforms and the membranes with sequential Si_3N_4 and device Si RIE, e) Deposition of a 3.5 µm thick SiO_2 hard mask and opening of a window to etch bulk Si with deep RIE, f) Wafer dicing and KOH process to eliminate Si under metal/nitride membranes, g) Galvanic displacement to deposit gold droplets on the Si walls of the platforms and subsequent CVD growth of the Si NWs by VLS.

3:1) for 10 minutes to eliminate organic residues, followed by a 10 seconds dip in 5% HF to etch native SiO_2, with 10 min water rinses in between. After, a 300 nm thick Si_3N_4 film is deposited by means of LPCVD on both sides of the wafer. This nitride film serves three purposes in our devices. The first is to act as an electrical insulation layer between Si device layer and metal film. The second is to provide mechanical support to the suspended platform. And the third is to thermally insulate the platform to maximize the temperature gradient through the TE element. This nitride film is then patterned with photolithography and RIE to etch parallel rectangles with a width of 5 µm. These serve as vias for the inter-level connections between the underlying device Si layer and the subsequent metal layer (see Figure 3.3 b and c). In order to minimize the electrical resistance of the device, the exposed silicon is doped using the Si_3N_4 layer as a mask. The doping process is done with ion implantation using Boron at a dose of $5{\cdot}10^{15}$ at/cm^2 and an energy of 50 KeV. Afterwards, the metal is patterned by photolithography followed by sputtering of titanium (Ti) and tungsten (W) layers. Their thicknesses are 30 and 200 nm, respectively. Ti is used as an adhesion layer. A subsequent lift-off process patterns the metal. Then, a rapid thermal annealing (RTA) at 700°C for 30 s under nitrogen atmosphere (N_2) is used to obtain an ohmic contact between the metal-Si interface.

The next step involves device passivation depositing a 1 µm thick SiO_2 film by PECVD (this step is done between Figure 3.3c and d, but not specifically shown in the scheme). Later, this oxide film is patterned with two different masks using photolithography and etching processes. The first photolithography etches half of the oxide film in the areas of the device's pads with hydrofluoric acid (HF) wet etching. The purpose of this partial etching is to allow the remaining oxide on the pads to be removed later with HF without fully etching the rest of the passivation oxide on the chip. The second etching step is used to define the layout of the platforms and trenches. For this, 1 µm SiO_2 is etched on two lateral sides of the platforms with RIE. Here, as can be seen in Figure 3.3g (amplified scheme), the platforms are not rectangles, but parallelograms. This is done to have (111) surface orientation in the lateral walls of the Si platform, which later prevents the platforms from being etched by KOH. On the other two sides, this etching step defines the (111) trenches where the NWs will be grown, and the notches on the metal/nitride membrane that supports the platform. In the microbeams device case, they are defined in this step. The reasons of carving parallel notches in the metal/nitride membrane are two: 1) reduce the membrane cross-section to diminish its conductance and 2) give access for the KOH to etch the device Si below this membrane. After this, two sequential RIE processes etch the Si_3N_4 and the device Si (15 µm etching made with deep RIE) where the 1 µm thick SiO_2 film is opened. Finally, a 3.5 µm thick SiO_2 film is deposited by PECVD in the backside of the wafer and patterned with photolithography and RIE. This layer is used as a hard mask to etch the bulk Si below the platforms and the membranes with a deep RIE. At this stage, while the chips are still mechanically robust because the platforms remain anchored to the bulk, the wafers are diced in 7x7 mm^2 chips.

Then, KOH etching is performed at chip-scale to release the platforms. Here, we benefit from the specific orientation of the vertical lateral walls on all sides of the platforms to stop KOH etching, which only occurs through the previously etched notches in the membranes. To reliably perform this etching, several parameters were optimized. Initially, the chips were placed inside a custom nylon holder that clamped them, prior to a KOH bath immersion. However, issues related to the accumulation of air bubbles led to alternative approaches. This is illustrated in Figure 3.4a. Perforated teflon holders were then used to avoid bubble accumulation in the chips. In these holders, the chips are placed inside the holder without any clamping structure. The optimal KOH etching

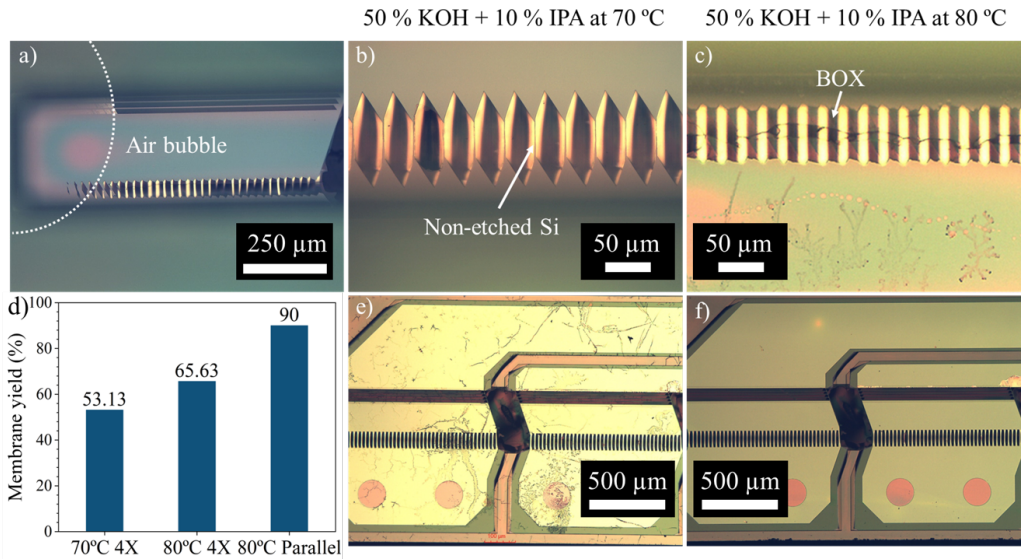


Figure 3.4: Microscope images of the KOH etching process optimization of the device Si under the membranes. a) Bottom view of the device showing etching problems related to air bubble formation due to the nylon holder, b) Bottom view results after etching at 70°C causes sometimes the breaking of the membranes before etching the Si, c) Bottom view with optimal etching conditions to completely eliminate the device Si but maintaining some buried oxide still present (the translucid film that can be seen over the membranes), d) Membranes yield depending on the KOH conditions and type of µTEG, e) Top view of an etched device without HCl cleaning, f) Same device after the HCl cleaning.

conditions to minimize bubble formation were found to be 50 % of KOH in water with 10 % of IPA (which helps reduce bubbling during the KOH) at 80°C. Figure 3.4b and c show two examples of etching under these conditions at different temperatures. In the 70°C case, some Si still remains when the nitride/metal membranes are already broken. In Figure 3.4c all membranes are alive and Si is completely eliminated. With these conditions, the percentage of membranes alive after KOH is $\sim$ 66% in 4X devices and $\sim$ 90 % in Parallel ones (see Figure 3.4d). The larger length of the Parallel platforms can withstand some cracks in different zones of the membrane without collapsing. A 50-60 min etching time window was found to be optimal to avoid damage in other areas of the device. After KOH, the chips are cleaned with hydrochloric acid (HCl) for 10 min. This serves to eliminate the potassium salts deposited on the device after the KOH (see Figure 3.4e and f). At this stage, microbeams-based µTEGs are completed.

For the NWs case, galvanic displacement is then used to deposit gold droplets in the vertical side walls of the trenches and platforms (the rest of the device is still passivated with SiO_2). Afterwards, the NWs are grown by VLS as explained in Section 2.1.8. During all these processes, the Si trenches have been supported by lateral Si beams that prevent the platforms from collapsing. At the end, these supports are eliminated with focused ion beam (FIB) etching (see Figure 3.5) to avoid parasitic heat flow paths through these beams. Etching them at this point is possible because the trenches and the platform are held together by the NW arrays.

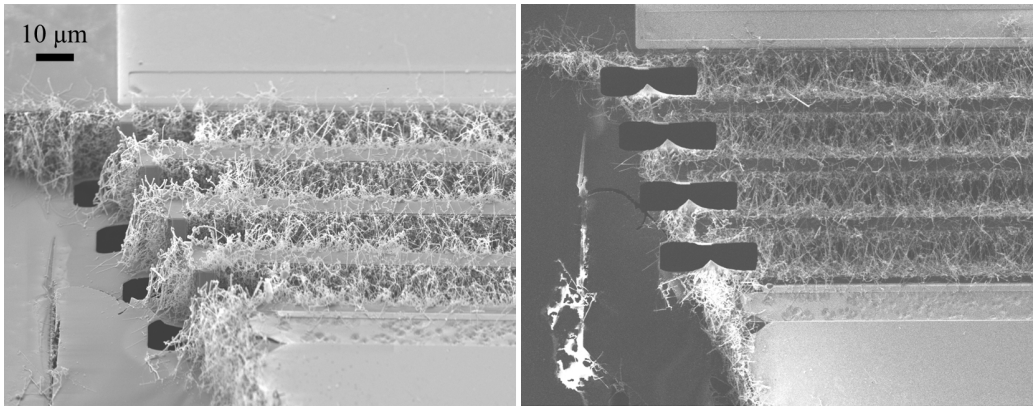


Figure 3.5: Tilted and top-view SEM images of a four-trench NWs chip after etching the supporting beams with FIB. The scale bar is for both images.

3.2 Thermoelectric characterization

This section discusses the thermoelectric characterization and harvesting performance of bare µTEGs with Si NWs and microbeams.

3.2.1 Nanowires

3.2.1.1 Test mode

In test mode, the bulk silicon temperature is controlled by placing the chip on a hotplate, while the platform heater is used to adjust the temperature gradient across the TE material. Therefore, the Seebeck coefficient can be calculated by fitting V_{OC} versus temperature gradient at different hotplate temperatures.

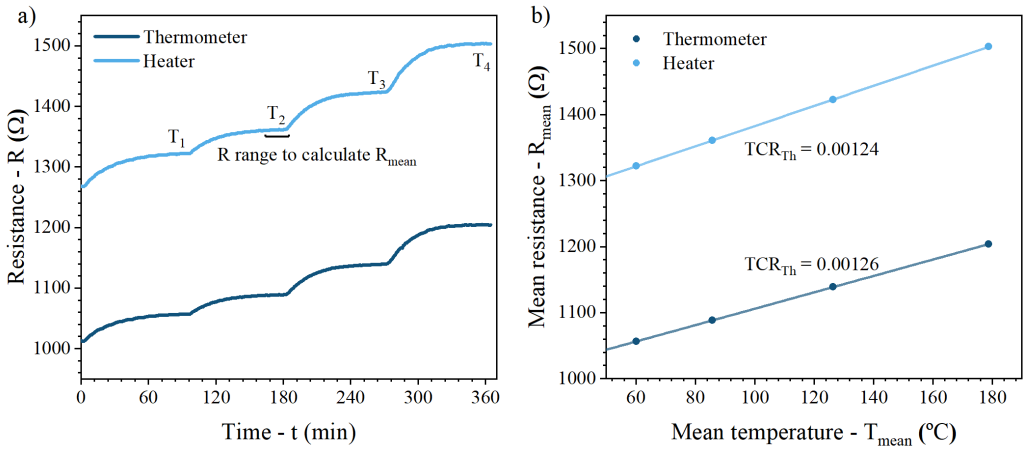


Figure 3.6: a) Heater and thermometer resistance of a platform versus time exposed to different oven temperatures, b) mean resistance calculated with the stable resistance values at each oven temperature.

Since both, the heater and thermometer, need to be calibrated, the first step is the characterization of their TCR (see Section 2.4.4). Figure 3.6a shows a heater and thermometer resistance change of a 4X chip inside an oven at four different oven temperatures. Once the temperature has reached a steady state at at given oven temperature, we calculate the mean resistance (see Figure 3.6b, where the values of mean resistance versus mean oven temperature of these devices are shown). The different resistances for each component is evident, and a consequence of their different designs. These measurements resulted in TCR values of 0.00124 and 0.00126 C^{-1} for the heater and thermometer, respectively.

The Seebeck characterization results can be seen in Figure 3.7b, where a Seebeck coefficient increase is observed from $\sim$ 224 μV/K at 50°C to $\sim$ 238 μV/K at 140°C. These values are in good agreement with previous measurements of the same type of NWs [125] considering their error bars. However, this discrepancy is also attributed to the Si NW growth process, which results in NWs with variable diameter and trench occupancy from chip to chip. Therefore, a good agreement should not be expected.

Figure 3.8 benchmarks the obtained Seebeck coefficient values against literature values. *d* indicates the diameter of the NWs. However, no significant change of Seebeck is expected for d > 20-30 nm [19]. Taking into account the average doping of our NWs, $\sim 3{\cdot}10^{19}$ cm^{-3}, they are in good agreement with the data plotted. The Seebeck coefficient values are similar to those measured by Boukai [18], whose doping is equal, and are in good agreement with those of Sadhu with a doping of $5{\cdot}10^{19}$ cm^{-3} [143]. The NWs with higher doping concentration have lower Seebeck coefficient, which is expected since the Seebeck coefficient is inversely proportional to the doping level. The only NWs with lower doping are those of Sadhu at $2{\cdot}10^{19}$ cm^{-3} [143], which also have a larger Seebeck coefficient. Regarding the Seebeck coefficient increase with temperature, it is equivalent to those observed by Boukai and Sadhu ($2{\cdot}10^{19}$ cm^{-3}), while Sadhu ($5{\cdot}10^{19}$ cm^{-3}) shows a steeper increase with temperature. This can be associated with the fact that the phonon-drag effect is more suppressed in highly doped NWs [145], which, at the same time, leads to

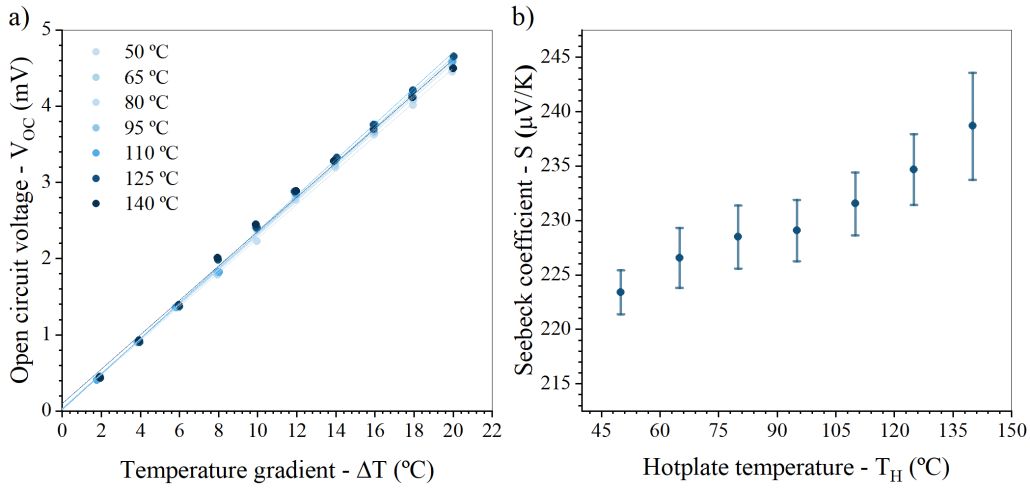


Figure 3.7: a) Open circuit voltage (V_{OC}) versus temperature gradient at the NWs for different hotplate temperatures (50 to 140°C), b) Seebeck coefficient calculated with the data from a) as a function of the hotplate temperature.

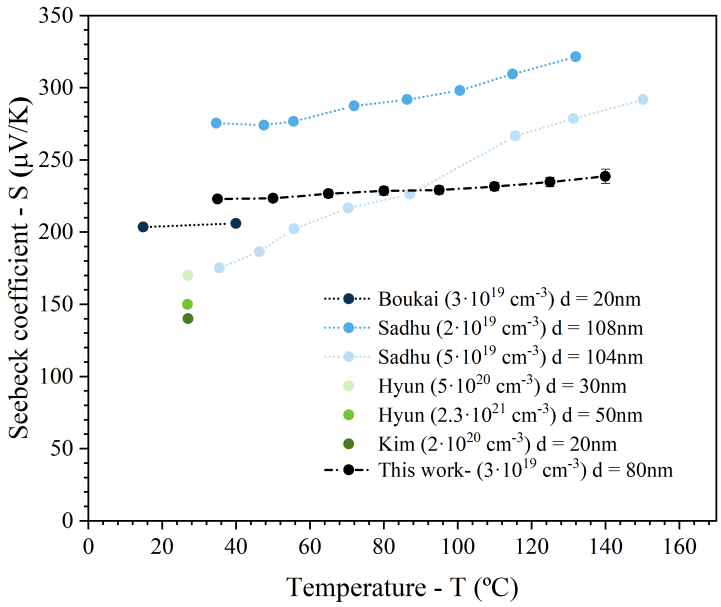


Figure 3.8: Comparison of the Seebeck coefficient of this work for NWs with examples of NWs from the literature [18], [142], [143], [144].

a steeper increase in the overall Seebeck value with temperature (the phonon-drag effect generally compensates the increase of carrier component (S_p) of the Seebeck coefficient).

3.2.1.2 Harvesting mode

As explained in Section 3.1, the harvesting mode is equivalent to real working conditions of a TEG. Therefore, these measurements show the reliability of the µTEGs developed in this thesis to work in a real scenario.

The first set of studies evaluated the influence of the TE element length on device performance. The objective is to determine the optimal length, considering the trade-off between thermal and electrical resistance in terms of power generation. Figure 3.9 shows optical images of the different devices on the 4X chip, illustrating that each platform has a different number of trenches (all of the same length), which results in different TE total lengths on each platform.

The thermoelectric characterization results can be seen in Figure 3.10 for each platform and temperature. The measured voltage and current show a proportional increase with the hotplate temperature. In the measured power, this relation is quadratic as it involves the increase in both voltage and current. This is expected because higher hotplate temperatures lead to higher temperature gradients in the TE elements, thus increasing the voltage generation. Moreover, the Seebeck coefficient increase with temperature, further enhances the voltage generation. By increasing the number of trenches, the amount of voltage generated always increases.

This can be better seen in Figure 3.11, where the open circuit voltage (V_{OC}), internal resistance (R_{int}) and maximum power (P_{max}), are plotted as a function of hotplate temperature for the four platform designs. The behavior of the voltage is expected because longer TE elements imply a higher thermal resistance, and thus a higher temperature

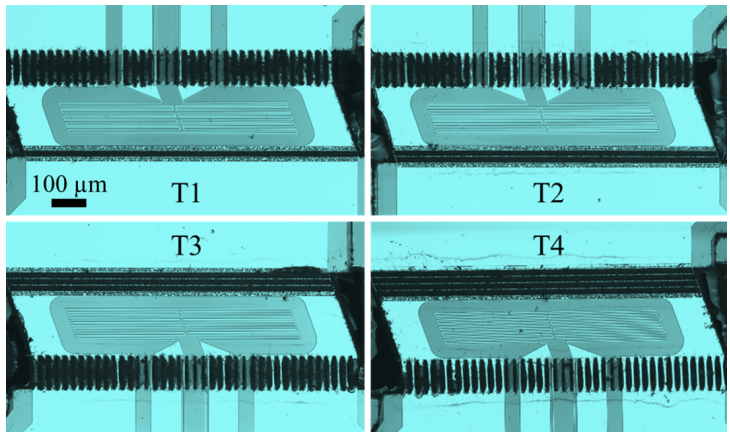


Figure 3.9: Optical images of the four different platforms of the 4X device (T1 to T4), where the number of trenches increases from one to four, resulting in a total TE length of 15 μm to 60 μm (4x15 μm) from T1 to T4, respectively. The scale bar is the same in all images.

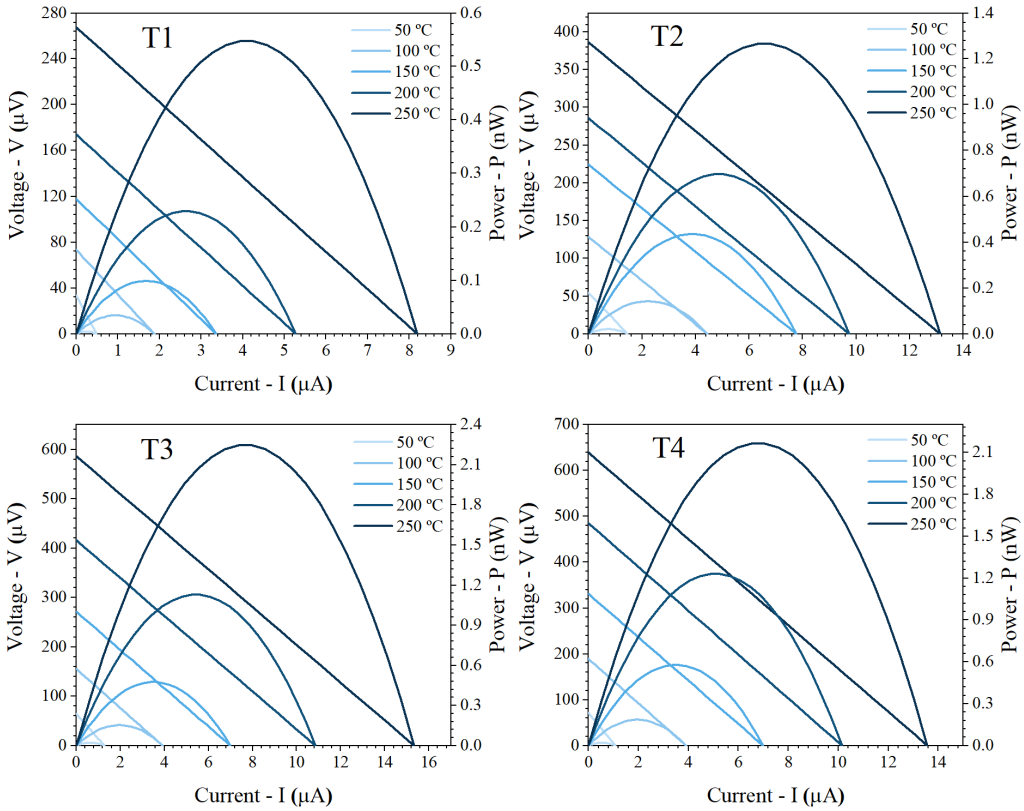


Figure 3.10: Voltage and power vs current measured in a 4X chip on each of the four platforms for different hotplate temperatures. The voltage shows a uniform increase with the number of trenches, but the current has a maximum value for the three trenches platform.

gradient. However, the internal resistance of the device is also affected by the TE length, leading to a maximum short circuit current (I_{SC}) at a given length. This is clearly observable in Figure 3.10, where I_{SC} increases from one to three trenches but then decreases in the fourth platform. In terms of maximum power, the same compromise arises as P_{max}, which is attained when $R_{int} = R_{load}$ (and thus depends on R_{int}), shows a similar trend. This is seen in Figure 3.11c where the three- and four-trench platforms exhibit similar (and maximum) P_{max} generation through the entire temperature range. Based on these results, Parallel-type devices with four trenches were selected for the remainder of the characterization. It is also worth noting that the increase in V_{OC} with the number of trenches suggests that the heat flow through the NW array is not negligible. A saturation in voltage would be expected once the temperature gradient becomes dominated by heat conduction through the nitride/metal membrane. In such a case, further increasing the TE length would not significantly enhance the temperature gradient. This indicates that thermal leakage through the membrane side is not the dominant heat loss mechanism. Thus, the uni-leg type µTEG does not degrade the device's heat management to the

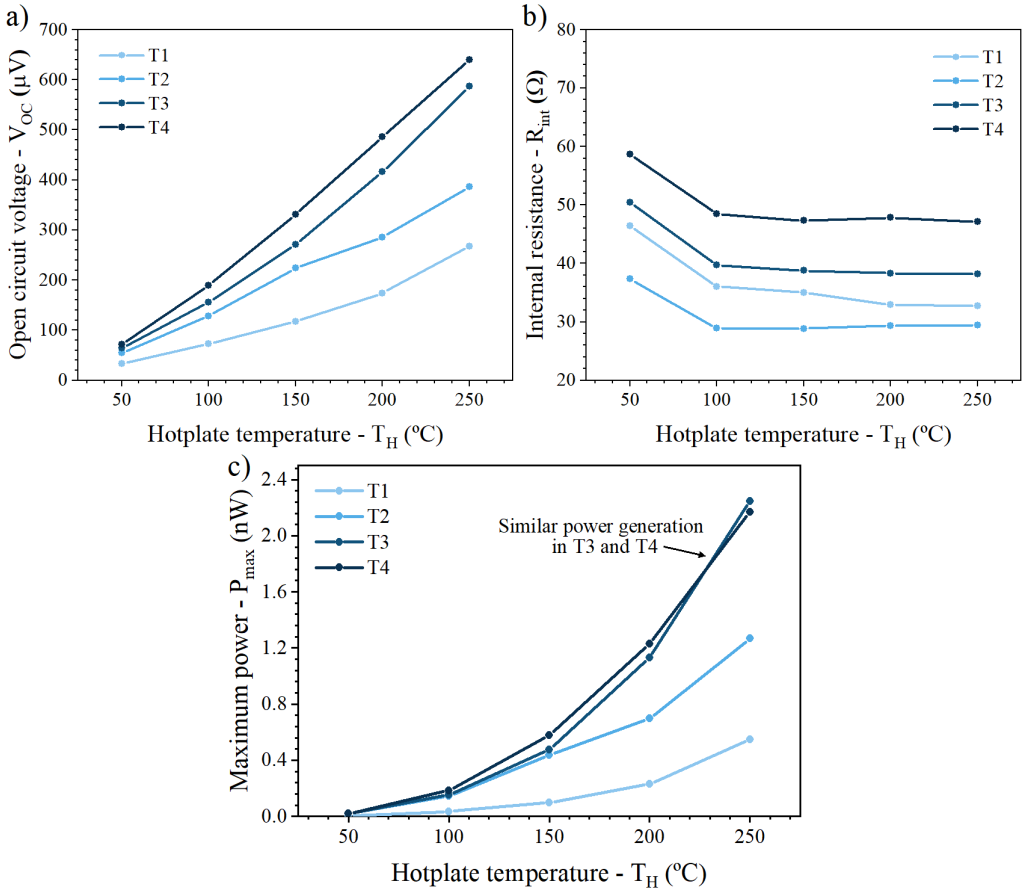


Figure 3.11: Representative plots of the: a) open circuit voltage, b) internal resistance and c) maximum power for the different platform designs as a function of the hotplate temperature. The trends in the open circuit voltage and maximum power are clearly visible, with equivalent power generation for the three and four trench platforms.

extent that the TE element contribution is negligible.

In Parallel chips the power is expected to increase compared to the 4X devices, reaching an enhancement in voltage and current of $\sim$ 10 and $\sim$ 5 times, respectively (Parallel µTEGs have 5 4X platforms in parallel, and 10 of these connected in series). However, since the survival rate of the membranes is low after the KOH fabrication step, the number of membranes that can be connected in series is usually lower than ten. Nonetheless, as it has been explained in Section 2.1.11, the use of jumpers to bypass broken or too resistive platforms is used to connect the maximum number of properly performing platforms. Figure 3.12a shows the thermoelectric characterization of a parallel chip with four trenches. This device has seven working platforms. The values show an increase factor of $\sim$ 7.5 and $\sim$ 6.5 compared to the 4X device in V_{OC} and I_{SC}, respectively. Given the variability in the average NWs diameter and in the NW trench occupancy across different growths, the obtained values are considered to be close to the expected values of 7 and 5. In terms of power generation, the increase is $\sim$ 45 times, with a maximum power of $\sim$ 100 nW when exposed to a hotplate temperature of 250°C.

Figure 3.12b presents a comparison of the maximum power generation of this same device as a function of how many platforms are connected in series. In this case: one single platform (1x µTCs), 4 platforms (4x µTCs) and 7 platforms (7x µTCs). As expected, I_{SC} remains approximately constant no matter how many platforms are measured, while V_{OC} increases. Thus, the increase in maximum power generation is linearly proportional to the number of platforms connected in series. A more comprehensive comparison of V_{OC}, P_{max} and R_{int} for this device as a function of the number of platforms can be seen in Figure 3.13, together with a plot of the sustained temperature gradient in the TE element at different hotplate temperatures. The linear fittings shown for V_{OC} and P_{max} confirm the expected scalability of these parameters with the number of platforms connected in series. In the R_{int} case, a similar trend is observed although the change with temperature is less pronounced (every individual platforms shows a slight increase of R_{int} with temperature). In any case, the fact that the overall R_{int} of the device increases with the temperature is in agreement with the properties of the NWs [125],

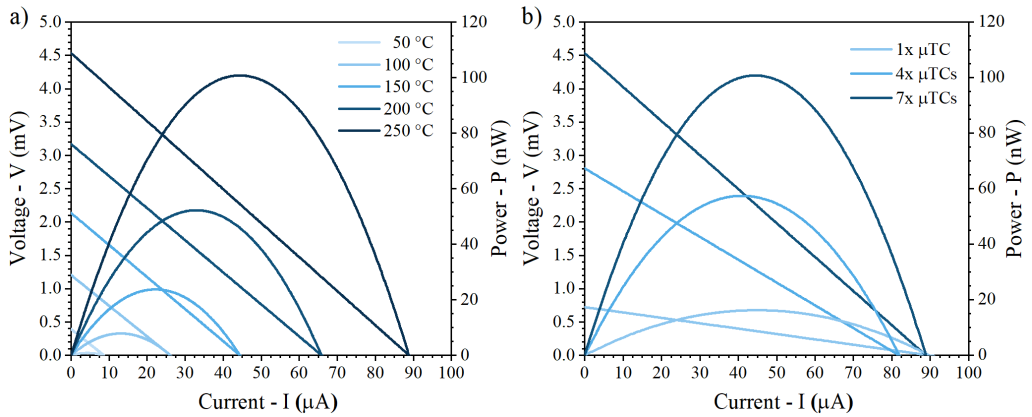


Figure 3.12: a) Voltage and power versus current in a Parallel device with seven platforms connected in series at different hotplate temperatures. b) Comparison of voltage and power of a Parallel device depending on the number of platforms connected in series at 250°C.

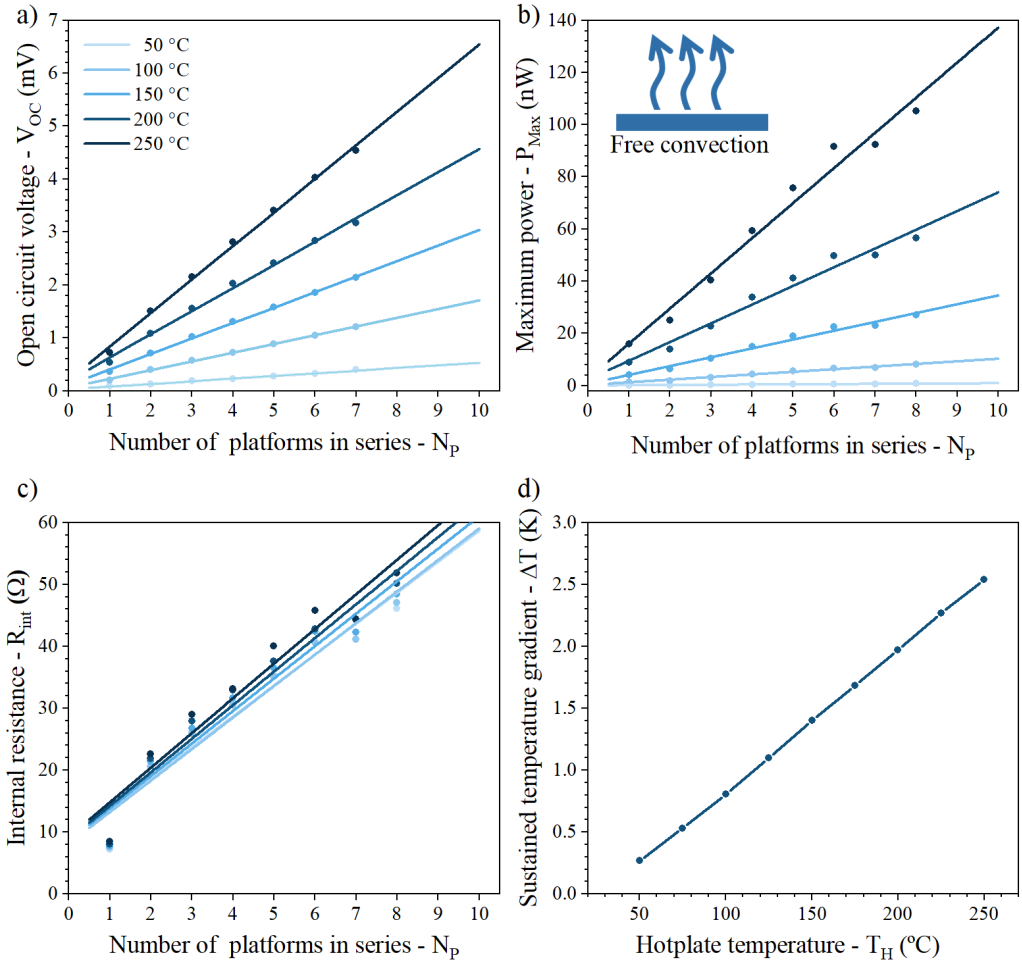


Figure 3.13: Comparison of a) open circuit voltage, b) maximum power and c) internal resistance of the Parallel device at different hotplate temperatures as a function of the number of platforms in series. d) Plot of the sustained temperature gradient in the TE element at different hotplate temperatures (calculated using the Seebeck coefficient and V_{OC}).

since their electrical conductivity decreases when increasing the temperature. A suitable method to evaluate the thermal management of a TEG is to visualize the ratio between the temperature gradient sustained at the TEG and the external temperature gradient, which can be defined as thermal gradient fraction, f_{th}:

$$f_{th} = \frac{\Delta T_{TE}}{\Delta T_{ext}} \tag{3.1}$$

being ΔT_{TE} and ΔT_{ext} the thermal gradient in TE element and available externally (between hotplate temperature and ambient temperature), respectively. Observing the results shown in Figure 3.13d, an average ΔT_{TE} of $\sim 2.6°C$ is sustained in each NW array when exposed to 250°C, meaning that $f_{th} = 0.012$ considering an ambient temperature

of 30°C (note that this ΔT_{TE} is calculated from the Seebeck coefficient and V_{OC} at each temperature, and thus is not a direct measurement). Evidently, a thermal gradient fraction of $\sim 1\%$ is low for a TEG to be applied in a real scenario, as the maximum power does not meet the low-power IoT devices requirements. However, this ratio is expected for a bare chip due to the small footprint of the suspended platforms. Since these are cooled by natural convection, and the thermal resistance to air is proportional to the platform size, a smaller footprint hinders effective cooling of the platforms. To evaluate the harvesting performance under a higher cooling condition, measurements were performed using a CPU fan to force a lateral air flow of 1.3 m/s on the top of the chip. This way, the heat exchange with the environment is enhanced due to the forced convection (FCV) condition.

The results of this study can be seen in Figure 3.14. As before, a linear proportionality

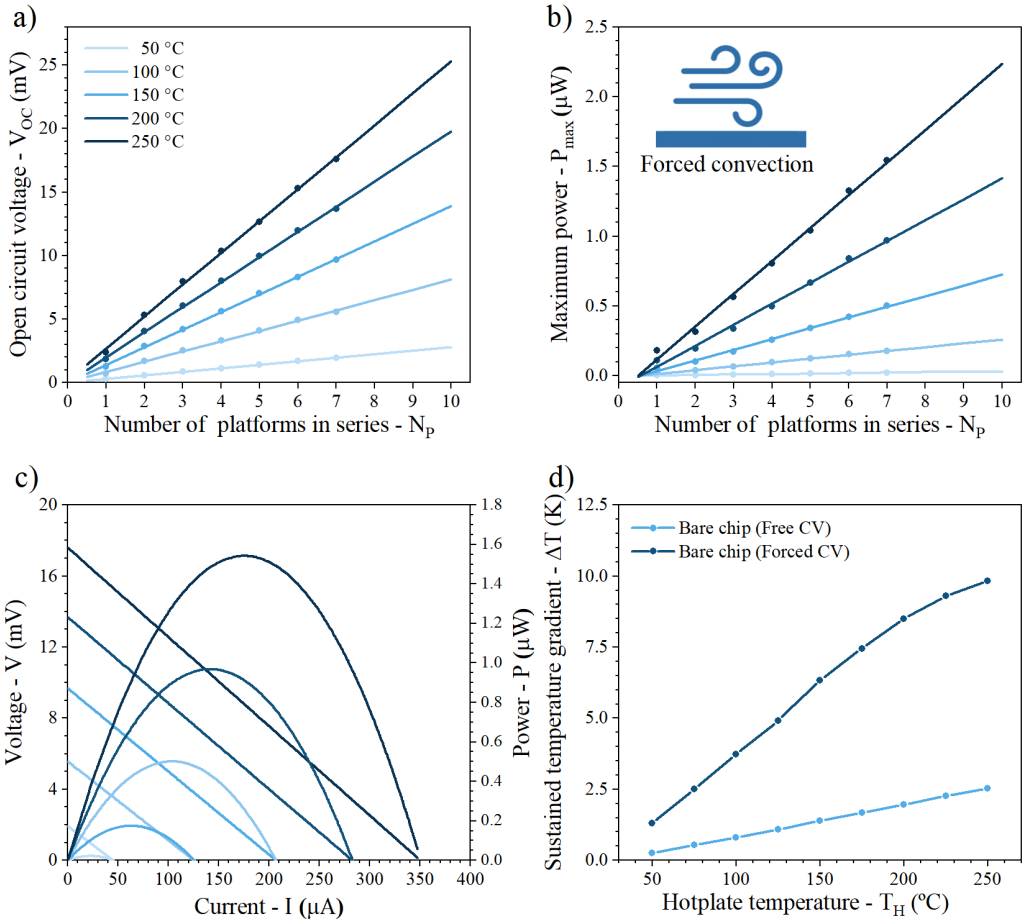


Figure 3.14: Comparisons of: a) open circuit voltage and b) maximum power of the Parallel device at different temperatures as a function of the number of platforms in series with a forced convection of 1.3 m/s, c) Thermoelectric characterization of the device with all the platforms connected in series, d) Sustained temperature gradient in the TE element at different hotplate temperatures compared to natural convection.

can be observed in both plots. In terms of voltage, we observe a ~ 4 times increase compared to the V_{OC} generation in free convection and an outstanding ~ 15 times increase in P_{max}. These results are a consequence of the enhanced heat exchange between the platforms and the environment, which translates into an increase in the temperature gradient attained at the TE element at each hotplate temperature. By comparing this result with the free convection case (see Figure 3.14d), we observe a ~ 4 times increase in terms of thermal gradient, which perfectly matches the increase observed in V_{OC}. This means that, under these conditions, the device shows a f_{th} of 0.045 when exposed to 250°C (assuming an external ambient temperature of 30°C). Furthermore, P_{max} at 250°C is now ~ 1.6 µW, which corresponds to a maximum power density of ~ 7.5 µm/cm^2. The area used to calculate the power density does not consider the outer pads regions, as they were designed only for characterization purposes (i.e. an area of 5.5x5.5 mm^2 is considered). This result is already close to the range of power density needs of IoT devices at the micro-energy range, and indicates that the optimization of the heat exchange with the environment is the strategy to make these TEGs viable for IoT. The clearest route to do this is to integrate a heat sink in contact with the platforms to maximize heat dissipation to the environment.

3.2.2 Microbeams

In the same working conditions and without further improvement of the heat exchange, the devices with microbeams are expected to show lower power generation because their thermal conductivity is higher than that of the Si NWs. Therefore, they will have smaller thermal gradients than NWs under the same conditions. As concluded from the experiment reported in Figure 3.11, the temperature gradient seen by the TE element largely depends on its conductance (NWs in that case), as heat flowing through the metal/nitride membrane is not dominant, since increasing the number of trenches always results in an increase of open circuit voltage. In this case, the TE element is even more conductive and, thus, it will have a major contribution to heat flow in the device. This was confirmed when evaluating the thermal conductance of the devices (see Figure 3.15). The results show a linear relationship between the temperature gradient and the power dissipated in the heater for the four platforms. Platforms with a higher number of microbeams consistently show lower temperature gradients. This is expected since the higher the number of microbeams, the higher the total conductance of the TE element. A linear fitting of the conductance values measured in the four platforms was performed (see Figure 3.15c) to determine the conductance of a single beam (slope of the curve) and the overall conductance of the metal/nitride membrane (extrapolated value at zero microbeams). The values obtained from this study were 92.36 and 295.7 µW/K for each beam and for the membrane conductance, respectively. This indicates that platforms with five or more microbeams exhibit higher thermal conductance on the TE side and are therefore more influenced by it in achieving the temperature gradient.

All these considerations point towards reducing the number of microbeams to optimize the power generation of these devices. The results of the thermoelectric characterization in harvesting mode of a 4X chip with microbeams can be seen in Figure 3.16. It is clear that an increasing number of microbeams in the platform affects negatively on both voltage and current generation, and therefore P_{max}. At the same time, a higher number of microbeams decreases the internal resistance of the device, but this is not enough to compensate for the large thermal conductance which implies small thermal gradients across the microbeams. Another comparison of the power generation of plat-

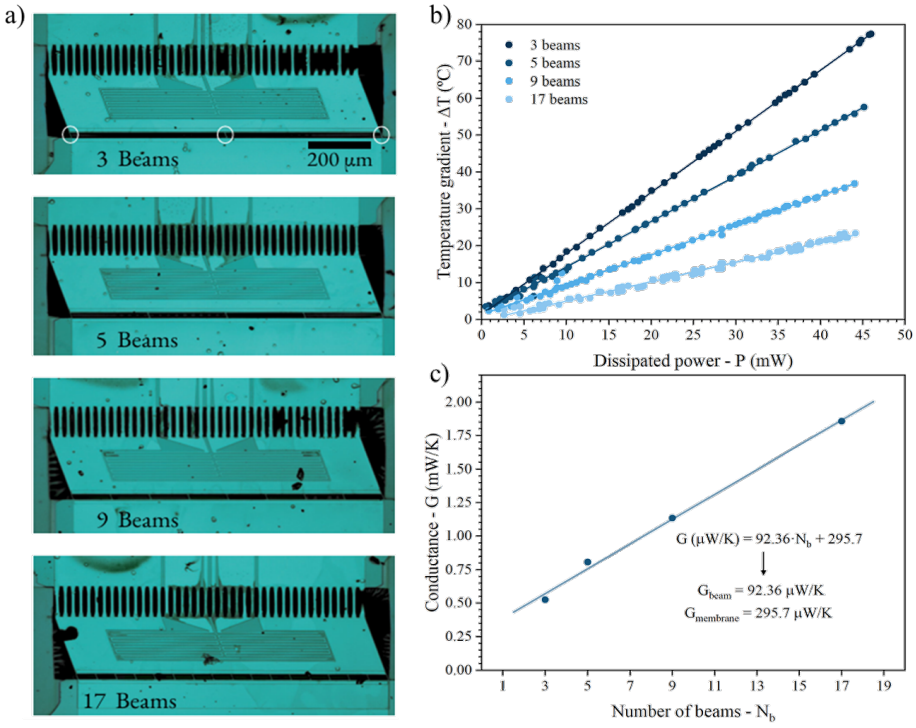


Figure 3.15: a) Optical images of the platforms with microbeams (white circles). The scale bar is the same in all images. b) Thermal gradient measured between the platform and the bulk as a function of the power dissipated by the heater. c) Conductance vs number of microbeams to obtain the conductance of the membrane and the individual beam.

forms with microbeams is shown in Figure 3.17. As already mentioned, the design with fewer microbeams is the best performing as an energy harvester in these conditions (i.e. bare µTEG in harvesting mode under natural convection). However, when comparing these results with those obtained with NWs, different observations can be highlighted. Comparing V_{OC} and P_{max} of the best µTEGs based on Si NWs and Si microbeams ($\sim$ 650 µV and $\sim$ 2.2 nW with NWs, $\sim$ 260 µV and $\sim$ 1 nW with microbeams) shows that the main advantage of devices with microbeams is their low internal electrical resistance. The µTEG with three microbeams harvests a temperature gradient $\sim$ 2.5 times smaller than that of the NWs, while its maximum power is $\sim$ 2.2 lower (i.e. 12% lower than the thermal gradient ratio).

However, it is important to note that this smaller power ratio is heavily impacted by the design of the TE elements being compared. As seen above, in a device with 3 microbeams, the TE element and the membrane have similar thermal conductances. In contrast, in NWs-based µTEGs the overall heat management is more influenced by the membrane, as its conductance is higher than that of the NW arrays. Therefore, in a TEG with a bi-leg type of design (i.e. with n- and p-type TE material on both sides of the platform), a bigger difference in performance should be observed because of their large difference in thermal conductivity. In any case, it was demonstrated that

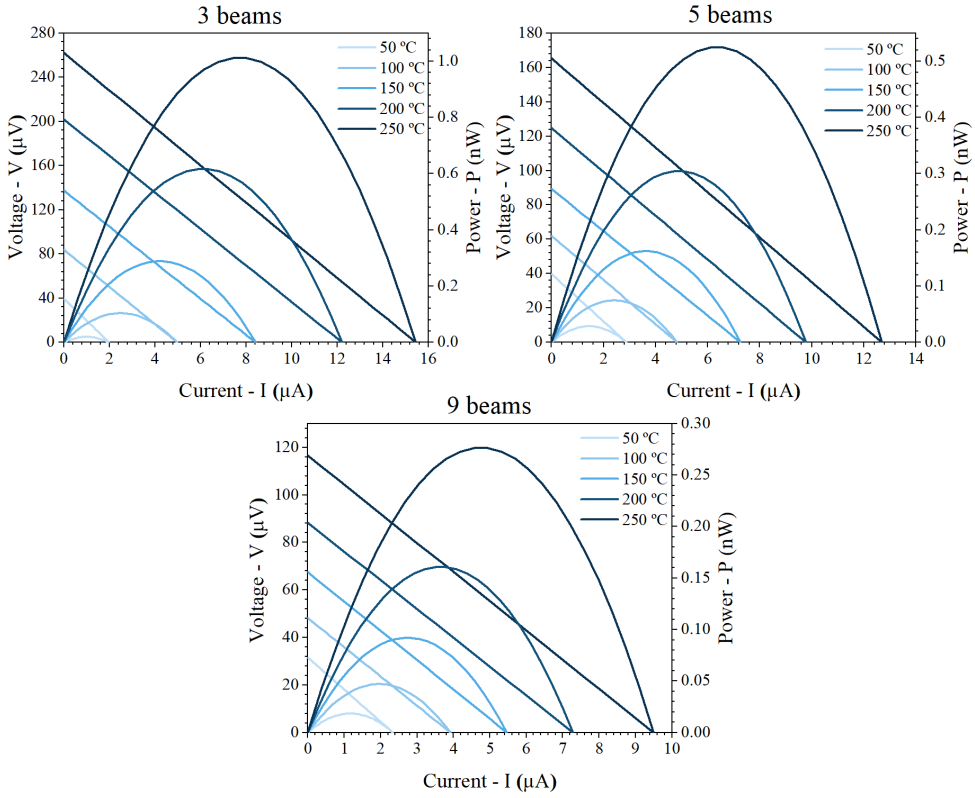


Figure 3.16: Plots of the thermoelectric generation in harvesting mode of three platforms with different number of microbeams. The higher value of open circuit voltage and short circuit current obtained in the 3 microbeams platform proves that reducing the number of microbeams generates more power.

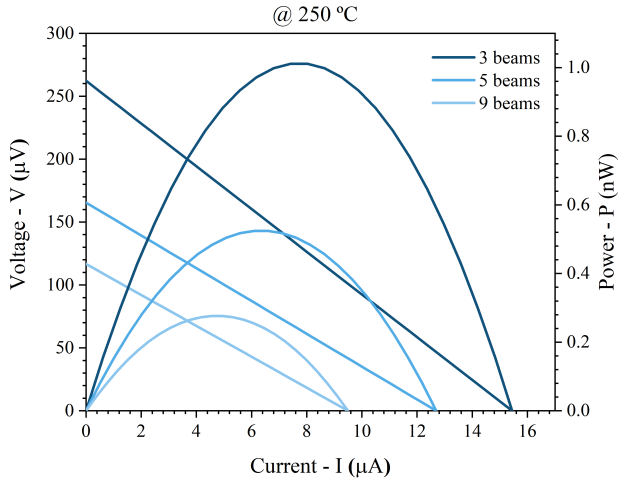


Figure 3.17: Comparison of the thermoelectric generation of three platforms with different number of microbeams at 250°C. An optimal occupancy is found at 1.5 % (3 microbeams), where the maximum power is clearly higher.

enhancing heat exchange between the platforms and the environment is essential to make Si-based µTEGs viable for IoT applications, as their high thermal resistance towards the environment limits performance regardless of the Si structure type.

3.3 Chapter conclusions

This chapter presented the work related to Si NWs and microbeams based µTEGs. On the NWs side, the optimal TE length for power generation was found to be 60 µm and a Seebeck coefficient of 223 µV/K was obtained at RT. In the microbeams case, the optimal geometry was found to be with a limited number of microbeams (1.5% occupancy rate in the trench). Among the explored µTEG designs, the high integration density of the Parallel µTEG, along with the consequent increase in power generation, highlight the strong potential of Si technology to maximize the performance of µTEGs. Nonetheless, the limitations of such µTEGs (i.e. their low thermal gradient fractions and power densities) make them incompatible with IoT applications unless heat exchange between platforms and the environment is properly optimized.

Chapter 4

Heat sink integration in micro-thermoelectric generators

This chapter presents the development of a methodology to integrate a heat sink onto the micro-structured silicon devices described in the previous chapter, aimed at maximizing the thermal gradient across the TE material and improving the performance of the µTEGs. Afterwards, the characterization and benchmarking of µTEGs with an integrated heat sink is shown. Finally, the process of integrating a 2×2 array of µTEGs into a single TEG is also presented, along with its power generation results.

4.1 Heat sink integration

The results in the previous chapter showed the limitations of Si µTEGs to create significant thermal gradients across the TE element, and also showed that the thermal gradient would improve if the thermal resistance of the platform to the environment decreases. The first part of this section discusses the method to integrate a heat sink that contacts the µTEGs at the suspended platforms, enhancing the contact area between the platforms and the environment. The second part is devoted to COMSOL simulations investigating the effect of this integration and considerations regarding its thermal model.

4.1.1 Integration procedure

The µTEGs have a planar design, which means that the suspended platforms and the bulk regions of the upper face have the same height. Also, the platforms are suspended and, thus, fragile. Therefore, the solution should be able to contact the platforms locally while minimizing the contact with the rest of the chip in order to minimize parasitic heat flow paths. For this reason and due to the fragility of the suspended platforms, the heat sink cannot be directly placed on top of the µTEGs, as is usually done with vertical π-type TEGs.

To overcome this challenge, a Si adapter was microfabricated to serve as an intermediate piece in the integration process (see Figure 4.1 for a scheme of the integration

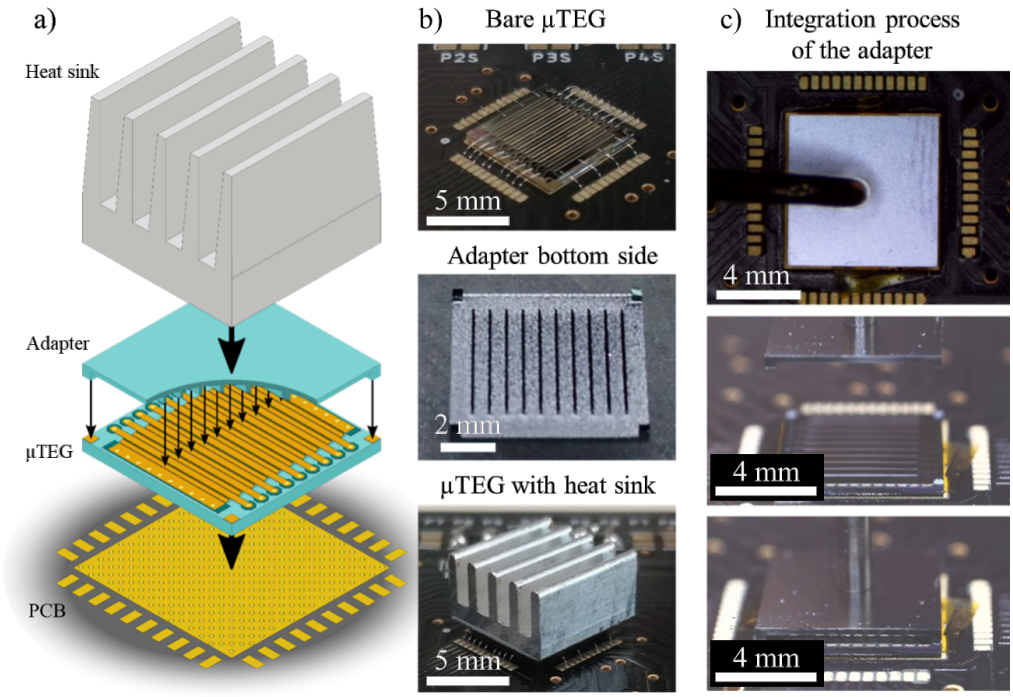


Figure 4.1: a) Scheme of the complete integration process of the heat sink into the µTEG. b) Images of the bare µTEG wire-bonded in the PCB, the bottom side of the Si adapter with the ten central and four corner pillars, and the final µTEG with the integrated heat sink on top. c) Images of the adapter placement process taken by the lateral camera and the top microscope. If the alignment is correct the corner pillars of the adapter coincide precisely with the corners of the µTEG.

process). The purpose of this piece is to distribute the weight of the heat sink more homogeneously in the µTEG by taking advantage of its four corner pillars, which are supported on the silicon bulk of the device. Also, since the platforms and the corners of the chip are at the same height, the platforms should never bend or break if the adapter does not bend under the pressure of the heat sink, which is not expected since the area of the heat sink is bigger than that of the adapter. Thus, a uniform weight distribution should take place on the adapter, preventing it from bending. At the same time, the area of the corner pillars is minimized to minimize parasitic heat flow paths. These Si adapters are fabricated by micro-machining using Si wafers with a thickness of 500 µm. First, a 3.5 µm thick SiO_2 is deposited by PECVD on the backside of the wafer. Then, a photolithography process followed by a RIE defines the layout of the adapter. In the case of the adapter for the Parallel µTEG, the layout consists of ten 0.1×5 mm^2 rectangles in the central area of the chip, corresponding to the ten suspended platforms of the µTEGs, and four 0.4×0.4 mm^2 squares at the corners (the corner pillars of the adapter). During this step, SiO_2 is only left over the rectangles and the squares. After, a deep RIE is performed to etch $\sim$ 300 µm of the bulk Si using the previously defined SiO_2 layout as a hard mask. Lastly, the wafer is diced to obtain the final 7x7 mm^2 Si adapters.

The alignment of the adapter with the µTEG and its gentle placement on top of the

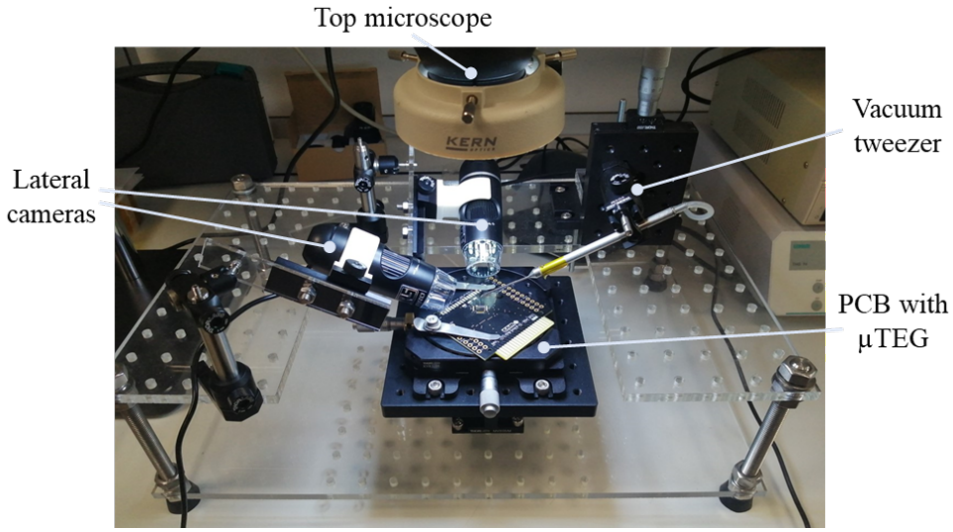


Figure 4.2: Image of the pick and place setup used for heat sink integration. The lateral cameras and the microscope serve to monitor the chip-adapter alignment. The placement of the adapter is controlled by a vacuum tweezer. Micro-metric control of the positioning is available in all axis.

platforms are critical for the proper integration of the heat dissipator. To facilitate this, we developed a custom pick and place setup (see Figure 4.2). Once encapsulated on its PCB, the chip is placed on a Thorlabs piece with XYZ movement and rotation control in the XY plane. The main structure of the setup is made of two PMMA plates with through holes, where the Thorlabs piece is screwed in. The upper PMMA plate has a 19x17 cm^2 square hole to fit it. The Thorlabs piece can be adjusted to match or stay below the upper PMMA plate. A second Thorlabs component (screwed to the upper PMMA plate) holds a vacuum tweezer that positions the adapter during the integration process. This component allows the z-axis control of the silicon adapter. Using a top microscope and two side cameras (screwed to the upper PMMA plate), a complete three-axis view of the chip is obtained, allowing visualization of the rotation and position of the µTEG and the adapter. All the micro-manipulators are compatible with micro-metric control and the cameras and the microscope are simultaneously monitored by means of a LabVIEW program.

In order to ensure good thermal contact between the platforms and the adapter, a thermal paste is used in the process. The thermal paste also provides mechanical robustness to the stack and prevents any displacement of the adapter throughout the experimental work. The integration process of the Si adapter consists of two phases: thermal paste application and adapter placement on the µTEG. Since the paste should only be applied to the pillars of the adapter (i.e. both at the central and corner pillars), a thin layer of paste is first spread on a PMMA surface. The desired thickness of the paste is achieved using a Proceq ZUA 2000 Universal Applicator. The adapter is then stamped into the paste and slowly lifted. The adapter is handled at the pick and place setup with the vacuum tweezer to control the procedure. Two thermal pastes were evaluated: a RS PRO Silicone Thermal Grease (RS stock number 707-4733 -*Thermal paste 1*-), with a thermal conductivity of 1.8 W/m·K, and a second RS PRO Silicone Thermal Grease (RS

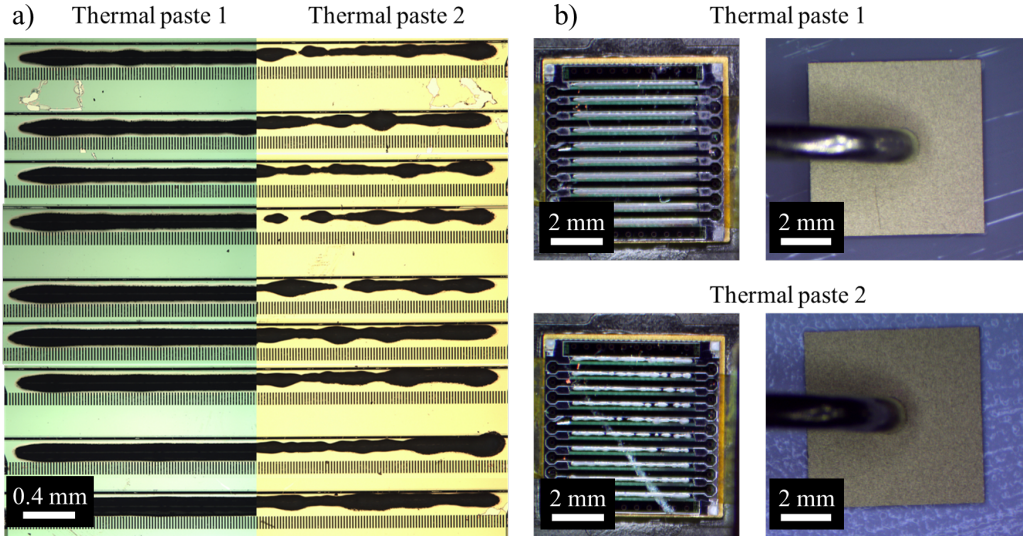


Figure 4.3: Images of the optimized adapter integration with both thermal pastes. a) Footprint of the different thermal pastes on the chip after the stamping and removal of the adapter. *Thermal paste 1* shows a more homogeneous and continuous shape on all the platforms, while *Thermal paste 2* has inhomogeneity issues forming big bubbles and discontinuities. b) (left) Images of the footprint on the complete chip after the integration and (right) the thermal paste texture image taken with the top microscope. The higher texture roughness of *Thermal paste 2* makes the integration more difficult.

stock number 193-8247 -*Thermal paste 2*-), with a thermal conductivity of 2 W/m·K. In both cases, a study of the optimal paste thickness and stamping conditions was conducted. Both pastes have different optimal application parameters due to their distinct texture and viscosity. Figure 4.3 shows a collage of optical images of the platforms after integrating the adapter and later removing it to evaluate the thermal paste footprint, together with images of the adapter being stamped in both pastes. In the *Thermal paste 1* case, its lower viscosity and texture roughness result in a more homogeneous distribution in the adapter and the chip, where the footprint is uniform along the platforms (see Figure 4.3a). For a successful integration to be optimal, the thermal paste was maintained at a thickness of 40 µm and the stamping process was carried out with minimal pressure, and pulling up the piece after seeing that all pillars had contacted the thermal paste. Other approaches, like thicker paste films or applying slightly higher stamping pressures, resulted in excessive amounts of thermal paste transfer causing it to spread beyond the boundaries of the platforms. This would obviously decrease the efficiency of the µTEG due to the presence of paste in the TE trenches, diminishing the maximum temperature gradient. During the optimization, it was also observed that a thicker volume of thermal paste was transferred onto the corner pillars than onto the central ones. However, due to the low viscosity of the thermal paste, the adapter was finally simply placed on the chip with the vacuum tweezer without applying any pressure. In this way, gravity helped the adapter to naturally adjust the pressure on the corner pillars, allowing the paste to spread there and ensure proper contact with the central platforms.

Optimizing the integration with *Thermal paste 2* was more challenging due to its

higher viscosity and rough texture. Since a uniform paste transfer to the adapter was more difficult, the thermal paste thickness was increased to 80 µm and a minimal pressure was applied during the stamping until all the pillars would be partially covered. Using thinner films or applying lower pressures led to very small footprints of paste on the chips. In the final integration on the chip, the weight of the adapter alone was insufficient to compensate the height difference between the thermal paste on the corner pillars and the central ones. Therefore, a controlled pressure was applied with the z-axis control of the vacuum tweezer to force a good contact with the platforms. Reaching a proper contact with the platforms was found to be strongly dependent on the viscosity and texture roughness (i.e. on the size of the filler particle). After a certain pressure, the paste would no longer compress and overflow at the edges of the corner pillars, leading to a misalignment between the adapter and the µTEG chip. Despite a proper contact of the adapter with all platforms can be achieved using this second paste, it is at the expense of a reduced yield across different chips. At this stage, the thermoelectric characterization of the µTEG also serves to cure the paste and ensure complete adhesion between the chip and the adapter.

The final integration step is the placement of the heat sink on top of the adapter. 9x9x4 mm^3 aluminum heat sinks were used in the experiments with individual µTEGs (see Figure 4.1b). To ensure proper adhesion to the adapter, the heat sink is stamped onto a 40 µm thick thermal paste before placing it on top of the adapter. In this case, the procedure is carried out manually. The internal resistance of the µTEG is monitored during the placement of the heat sink to detect any potential damage to the device. Again, thermoelectric characterization of the chip serves to cure the adapter-heat sink paste.

4.1.2 Simulations and thermal model

Simulations of µTEGs were done using a finite element model (FEM) analysis in COMSOL, the results of which are shown in Figure 4.4. The boundary conditions applied set the temperature at the bottom of the chip (equivalent to the hotplate temperature in our setup) to be 500 K. In the cases where the adapter and heat sink were integrated with the µTEG, contact resistances between 15 and 60 $kW/m^2 \cdot K$ were considered between the µTEGs and the adapter columns, and between the adapter and the heat sink. A convective regime with a heat exchange coefficient $h = 10\ W/m^2 \cdot K$ was imposed on the upper surface (the µTEG top surface in the bare case and the heat sink surfaces in the integrated case) to mimic a free convection regime under ambient conditions [146].

These simulations result in a V_{OC} of 4.8 and 37 mV for the bare µTEG and the integrated device, respectively. This implies that the TE elements hold a sustained gradient of 1.6 and 12.3°C (which correspond to f_{th} 0.8 and 6.15 %). Even though simulation results do not match experimental data, a reasonably similar value of 1.2 % Section 3.2.1.2 is obtained for the bare µTEG. The most interesting result from these simulations though, is the f_{th} improvement by a factor of ~ 7.7 in harvest mode after the heat sink integration, which is in good agreement with the result obtained experimentally, as it will be shown in the following section. Therefore, this thermal model helps us understand and improve heat management in our devices. A simplified equivalent thermal circuit of the device across the different integration steps helps us visualize the heat flow in our devices. Figure 4.5 provides both a scheme and an equivalent thermal circuit of the µTEG during the different integration steps.

The thermal model assumes a constant temperature profile in the bulk regions of

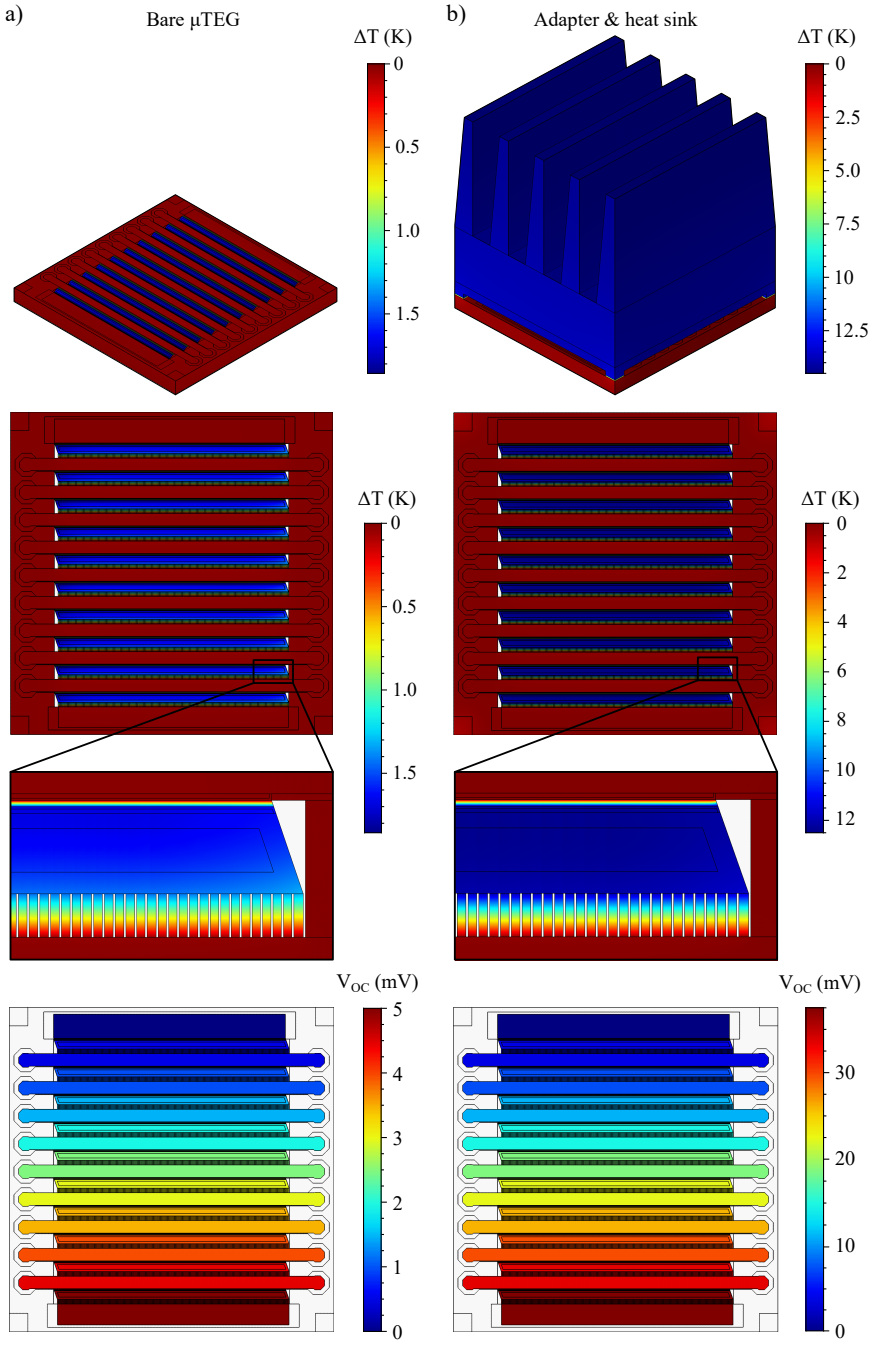


Figure 4.4: COMSOL simulations results for the μTEG without (left) and with (right) heat sink. Temperature maps and open circuit voltage are shown to compare the power generation capabilities of both configurations. The thermal gradient increases by a factor of ~ 7.7 with a heat sink

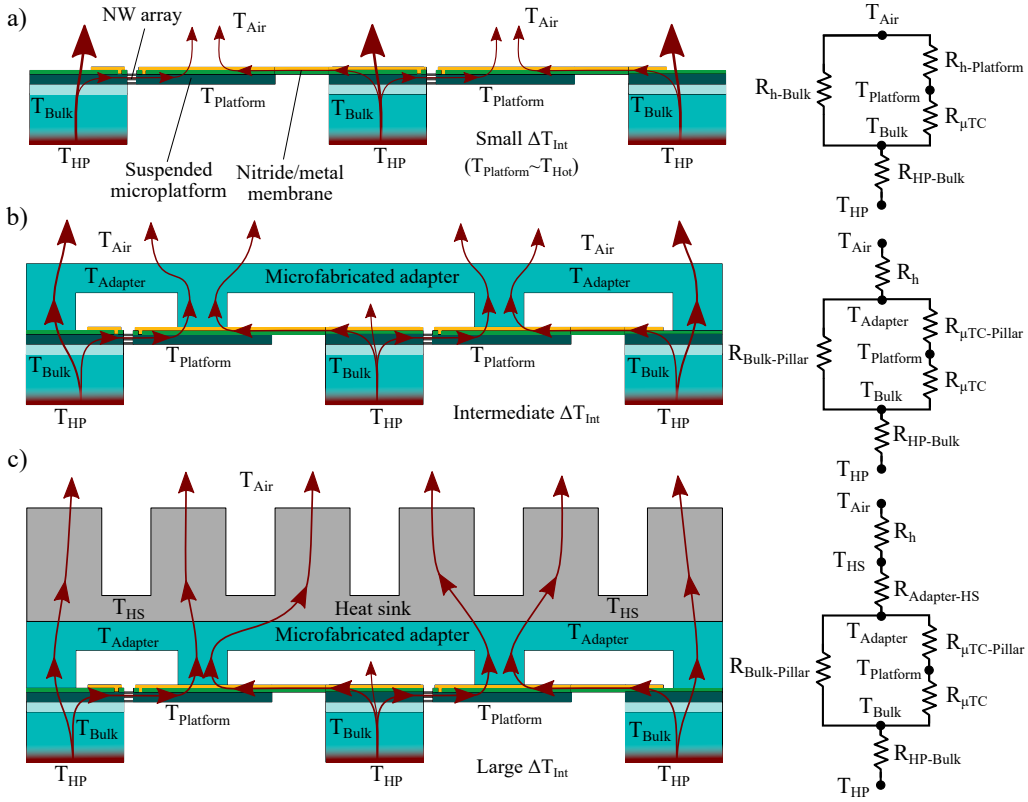


Figure 4.5: Schemes of the heat flow in the: a) Bare chip, b) Chip with Si adapter and c) Chip with Si adapter and heat sink. The equivalent thermal circuits (right) of the devices in the different integration steps.

the device, both in the Si bulk part of the chip and in the aluminum heat sink, because their thermal conductivity is significantly higher than the thermal contacts between the different interfaces. In the bare µTEG there are four different resistances: the thermal resistance between hotplate and bulk Si, $R_{HP-Bulk}$, the thermal resistances associated with the heat exchange between the upper side of the bulk and the platforms with the environment under free convection conditions, R_{h-Bulk} and $R_{h-Platform}$, and the thermal resistance of the platform (i.e. $R_{\mu TC}$, which corresponds to the parallel resistance of the TE element and the membrane).

After integrating the adapter, the resistances between the chip and the ambient are replaced by the contacts between these parts and the pillars of the adapter ($R_{Bulk-Pillar}$ and $R_{\mu TC-Pillar}$). Note that the contribution from the corner pillars is parasitic, since it is creating a new path to heat up the platform. Finally, the exchange with the environment takes place only through the adapter surface ($R_h^{Adapter}$). The contribution from convective heat taking place between the chip and the adapter is assumed to be low due to the large gap between both surfaces (350 µm) and the small temperature difference between them. Furthermore, this contribution was not considered during the COMSOL simulations in good agreement with experimental data.

Lastly, adding the heat sink in the model implies the addition of a new contact re-

sistance between the adapter and the heat sink ($R_{Adapter-HS}$).Moreover, the resistance associated with heat exchange with the environment (R_h^{HS}) decreases with the incorporation of the heat sink, due to the larger contact area with the environment. Taking all of this into account, the temperature gradient at the TE material (T_{Bulk} - $T_{Platform}$) as compared to the maximum available temperature difference (T_{HP} - T_{Air}) can be written as:

$$f_{th} = \frac{T_{Bulk} - T_{Platform}}{T_{HP} - T_{Air}} = \frac{R_{\mu TC} \cdot Q_{\mu TC}}{R_{TOT} \cdot Q_{TOT}} \tag{4.1}$$

For the case with heat sink, this can be rewritten after some manipulation as:

$$f_{th}^{HS} = \frac{R_{||}}{R_{||} + R_{HP-Bulk} + R_{Adapter-HS} + R_h^{HS}} \cdot \frac{R_{\mu TC}}{R_{\mu TC} + R_{\mu TC-Pillar}} \tag{4.2}$$

where $R_{||}$ is the equivalent resistance of the parallel part of the thermal circuit shown in Figure 4.5. This term thus accounts for both the cooling of the platforms by means of the heat flowing through the adapter pillars and also the parasitic heating that is coming from the bulk through the corner pillars:

$$R_{||} = \frac{1}{\frac{1}{R_{Bulk-Pillar}} + \frac{1}{R_{\mu TC-Pillar} + R_{\mu TC}}} \tag{4.3}$$

With this model, we can now interpret the results obtained in the previous simulations. If we assume that the parasitic heat contribution is negligible (high resistance between the bulk and the pillar), $R_{||}$ becomes a series resistance of the platforms and the platform-pillar contact contributions. In this configuration the model can be simplified to:

$$f_{th}^{HS} = \frac{R_{\mu TC}}{R_{\mu TC} + R_{\mu TC-Pillar} + R_{HP-Bulk} + R_{Adapter-HS} + R_h^{HS}} \tag{4.4}$$

Here, by integrating the heat sink the R_h^{HS} component is significantly reduced due to the large increase in contact area with the environment but, at the same time, two series resistances are added in the process associated to the adapter and the heat sink contacts. Thus, this integration only improves the heat management of the device if the decrease in R_h^{HS} is higher than the additional resistances introduced with $R_{\mu TC-Pillar}$ and $R_{Adapter-HS}$.

In the opposite case, if the contribution of the parasitic heat is considered to be high ($R_{Bulk-Pillar} \rightarrow 0$), the platforms temperature is similar to the bulk temperature, f_{th} tends to 0, and the μTEG performance is completely degraded. Interestingly, COMSOL simulations show that the voltage generation of the device is degraded after integration of the heat sink when no contact resistance between the adapter and the chip is considered, which is in good agreement with the thermal model.

The real device performance is somewhere between these two ideal configurations, with some parasitic contribution that also provides heating to the platforms. Nonetheless, as it will be shown in the following section, both simulations and measurements show an

increase in the voltage generation. Therefore, there is a non-negligible contact resistance between the bulk and the corner pillars, which implies that the fully integrated device performs better than the bare case. Moreover, the decrease in R_h^{HS} obtained with the heat sink integration compensates the added contributions of $R_{\mu TC-Pillar}$ and $R_{Adapter-HS}$.

Besides considering f_{th}^{HS} after the heat sink integration, the improvement in f_{th} relative to the initial value (i.e. $f_{th}^{HS}/f_{th}^{Bare}$, as defined in Equation 4.4) should also be evaluated:

$$\frac{f_{th}^{HS}}{f_{th}^{Bare}} = \frac{R_{\mu TC} + R_{HP-Bulk} + R_h^{Bare}}{R_{\mu TC} + R_{\mu TC-Pillar} + R_{HP-Bulk} + R_{Adapter-HS} + R_h^{HS}} \tag{4.5}$$

To simplify, we can consider external contact resistances ($R_{\mu TC-Pillar}$, $R_{HP-Bulk}$ and $R_{Adapter-HS}$) << $R_{\mu TC}$ and R_h, so this equation can be written as:

$$\frac{f_{th}^{HS}}{f_{th}^{Bare}} = \frac{R_{\mu TC} + R_h^{Bare}}{R_{\mu TC} + R_h^{HS}} \tag{4.6}$$

From this equation it is clear that a device with higher $R_{\mu TC}$, which is the parallel sum of the contributions of R_{TE} and $R_{Membrane}$, will have a lower $f_{th}^{HS}/f_{th}^{Bare}$. Considering the extreme case where $R_{\mu TC} \to 0$, then $f_{th}^{HS}/f_{th}^{Bare}$ tends to R_h^{Bare}/R_h^{HS}. On the other hand, if $R_{\mu TC} >> R_h^{HS}$, $f_{th}^{HS}/f_{th}^{Bare}$ tends to 1. Obviously, the real system is between these extreme cases. Figure 4.6a shows $f_{th}^{HS}/f_{th}^{Bare}$ versus $R_{\mu TC}$ and R_h^{HS} for a fixed R_h^{Bare}, while the $f_{th}^{HS}/f_{th}^{Bare}$ versus $R_{\mu TC}$ curves for different R_h^{Bare}/R_h^{HS} ratios are shown in Figure 4.6b. This reveals that the µTEGs with lower $R_{\mu TC}$ are more sensitive to any reduction in R_h^{HS} (i.e. an increase in R_h^{Bare}/R_h^{HS}). Therefore, µTEGs based on microbeams are expected to exhibit a greater f_{th} enhancement as a result of the heat sink integration.

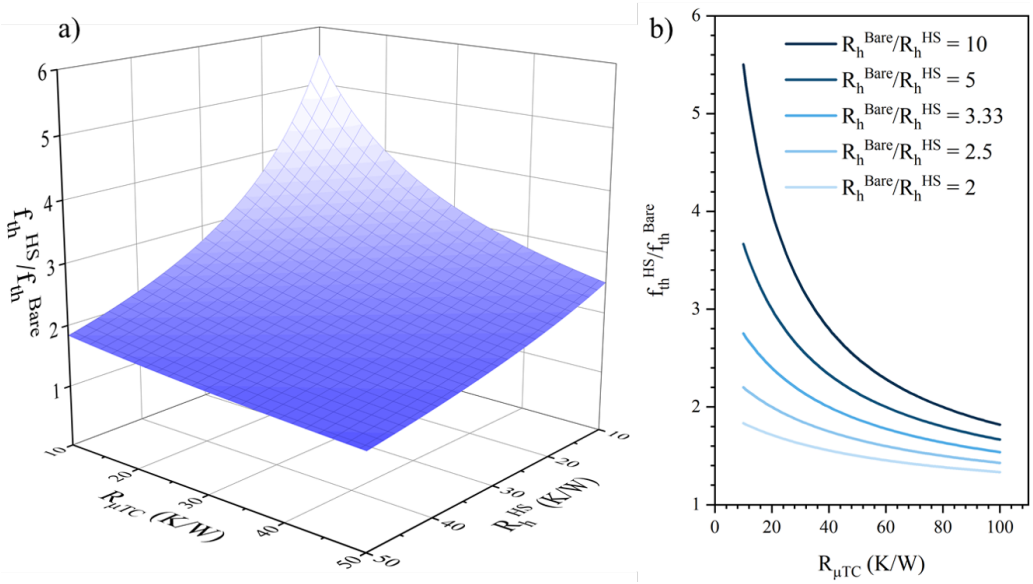


Figure 4.6: a) $f_{th}^{HS}/f_{th}^{Bare}$ versus $R_{\mu TC}$ and R_h^{HS}, as defined in Equation 4.6. b) $f_{th}^{HS}/f_{th}^{Bare}$ versus $R_{\mu TC}$ curves for different R_h^{Bare}/R_h^{HS} ratios.

Moreover, further enhancement of the heat exchange with the environment can be achieved under forced convection conditions. The thermal resistance towards the ambient of a surface under forced convention can be described as:

$$R_h^{Forced} = \frac{1}{A \cdot h_{Forced}} \tag{4.7}$$

where A is the area of the surface exchanging heat with the environment and h_{Forced} is the heat transfer coefficient under forced convection conditions. Since $h_{Forced} > h_{Free}$, a reduction of R_h is obtained. As a consequence, the denominator in Equation 4.4 decreases, thereby improving f_{th}. However, a saturation is expected in both cases (i.e. decrease of R_h with a heat sink or with forced convection) if the values of R_h become negligible compared to the rest of thermal resistances. This effect is expected to be more pronounced when both contributions are considered together. Furthermore, reducing R_h through forced convection on the heat sink case is expected to have a smaller effect on f_{th} because the contribution of R_h in the denominator in Equation 4.4 is smaller (i.e. due to the added $R_{\mu TC-Pillar}$ and $R_{Adapter-HS}$ on this configuration). On the contrary, the effect of R_h reduction on f_{th} in the bare case is more significant, since the denominator includes only $R_{\mu TC}$ and $R_{HP-Bulk}$ in addition to R_h.

4.2 Thermoelectric characterization with heat sink

This section summarizes the thermoelectric characterization of µTEGs with NWs and microbeams for Parallel-type chips after integrating the adapter and heat sink. Since test mode configuration of the chips is not particularly relevant for devices with a heat sink, all the results shown hereafter correspond to harvesting mode, in which the µTEGs performance is evaluated under real working conditions.

4.2.1 Nanowires

Since complete µTEGs thermoelectric characterization was done in all stages of the heat sink integration, a comparison of the performance improvement can be shown. The first interesting result is the performance improvement with the two thermal pastes. V_{OC} of several chips where the heat sink was optimally integrated are shown in Figure 4.7. The average increase factors in V_{OC} are 8.96 ± 2.97 and 13.53 ± 3.51 for *Thermal paste 1* and *2*, respectively. These results indicate that *Thermal paste 2* further improves the thermal gradient of the µTEGs. Since thermal conductivities of both thermal pastes are similar (1.8 vs 2 W/m·K), this behavior could be explained taking into account the paste texture. *Thermal paste 2* exhibits very high roughness, with large filler particles in the paste (i.e. resulting in a low overall contact area with the opposing surface). This is expected to increase the thermal contact resistance between the bulk and platforms of the µTEG and the adapter pillars (i.e. $R_{\mu TC-Pillar}$ and $R_{Bulk-Pillar}$). However, since a higher thermal gradient is achieved in the µTEG, the trade-off is favorable, and the decrease in $R_{Bulk-Pillar}$ becomes more relevant for reducing the parasitic heating of the platforms. In the case of *Thermal paste 1*, all heat sink integrations were successful, whereas *Thermal paste 2* showed more inconsistency in the adapter-platform contact. In some instances, this resulted in very small paste footprints on the platforms, leading to higher contact resistances and a reduced thermal gradient. Therefore, although the potential increase in V_{OC} is higher with *Thermal paste 2*, its lower consistency in the integration of the heat sink makes it unsuitable. From this point onward, the characterization results will

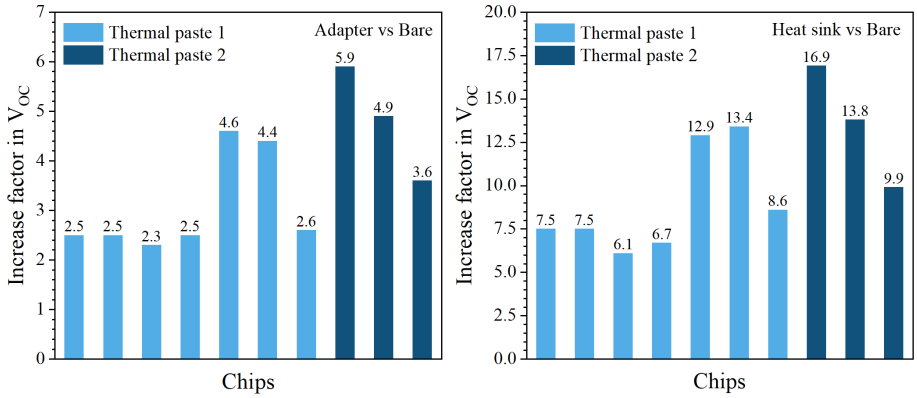


Figure 4.7: Voltage increase factors obtained in different chips after adapter and heat sink integration for both thermal pastes. In average, *Thermal paste 2* leads to a higher increase. However, due to the inconsistency of the integrations with this paste, *Thermal paste 1* was designated as the optimal to ensure a reliable and reproducible integration.

correspond to chips with integrated heat sinks using the more reliable and reproducible *Thermal paste 1*.

Figure 4.8 shows the measurements of voltage and power versus current curves for the bare chip, the chip with adapter and the chip with heat sink, together with a comparison of these at 250°C in Figure 4.8d. It can be seen that at 250°C the initial V_{OC} of 4.5 mV of the bare chip is increased to 11.2 mV after the placement of the adapter. Further improvement is obtained once the heat sink is integrated, reaching a value of 34 mV. Thus, the increase factors in this chip are $\sim$ 2.5 and $\sim$ 7.5 for the adapter and heat sink, respectively. This last value is in great agreement with the factor obtained in the simulations ($\sim$ 7.7). The generated power increases from 100 nW to 5.5 µW and no change is observed in the internal resistance of the device after the integration. Again, the considerable improvement in the generation of the µTEGs after the heat sink integration, demonstrates that the effect of the increased area compensates the added contact resistances with the adapter and the heat sink.

Similarly to the bare µTEGs case, imposing a forced convection (v = 1.3 m/s) horizontally on top of the devices (i.e. parallel to the top surface of the device) increases the heat exchange with the environment. As a consequence, the open circuit voltage also shows a significant improvement. A chip with integrated heat sink under free and forced convection is compared in Figure 4.9. In this case, V_{OC} under forced convection reaches 108 mV when exposed to 250°C, which leads to P_{max} = 58 µW. Interestingly, in this configuration, the µTEG generates more than 10 µW at temperatures as low as 150°C.

In the case where there is forced convection, h_{Forced} increases depending on the velocity of the air and R_h^{Forced} is subsequently decreased. As a consequence, f_{th} is enhanced and so is V_{OC}. The impact depends on whether or not a heat sink is integrated (see Table 4.1). In the bare chip case, V_{OC} shows a $\sim$ 3.9 increase, while this value is $\sim$ 3.1 in the µTEG with heat sink. The effect of R_h on the denominator of Equation 4.4 differs between the bare chip and heat sink cases. In the latter, two additional resistances (i.e. $R_{\mu TC-Pillar}$ and $R_{Adapter-HS}$) further limit the contribution of the decrease in R_h, as predicted in Section 4.1.2. Therefore, these results are in good agreement with the

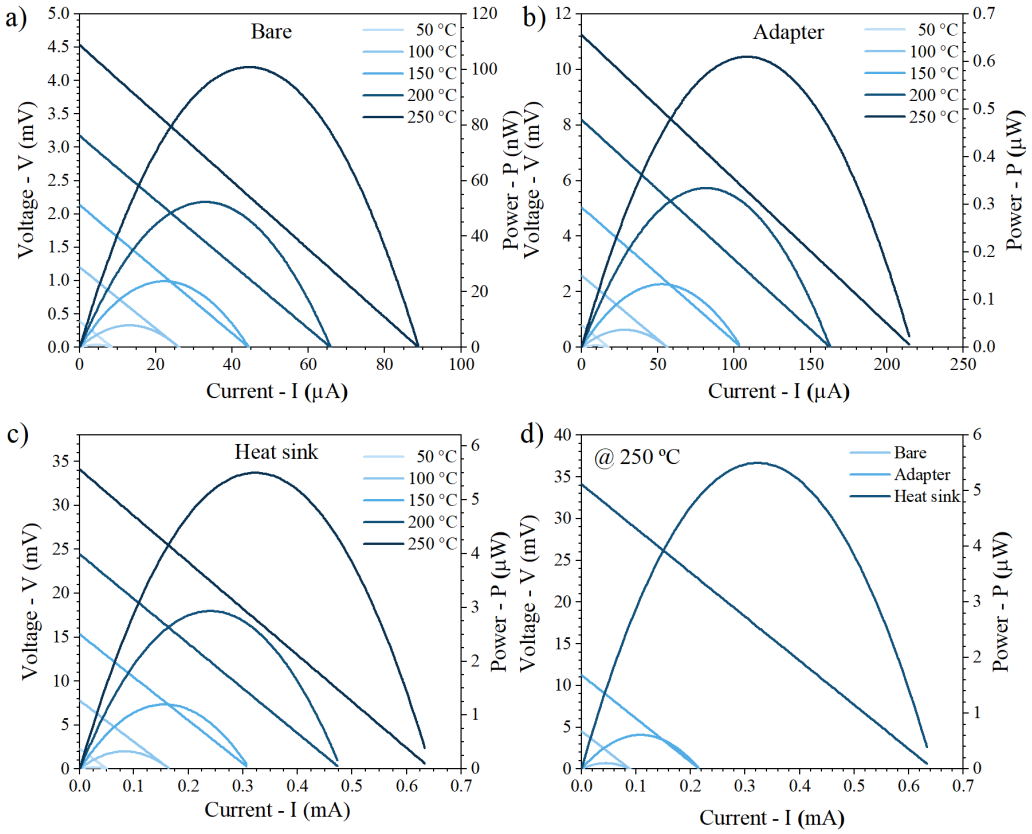


Figure 4.8: Voltage and power vs current of a Parallel μTEG across the three stages of the heat sink integration (a, b and c). d) Comparisons on the voltage and power for the three stages at 250°C. The power shows a $\sim$ 55 times increase with the integrated heat sink.

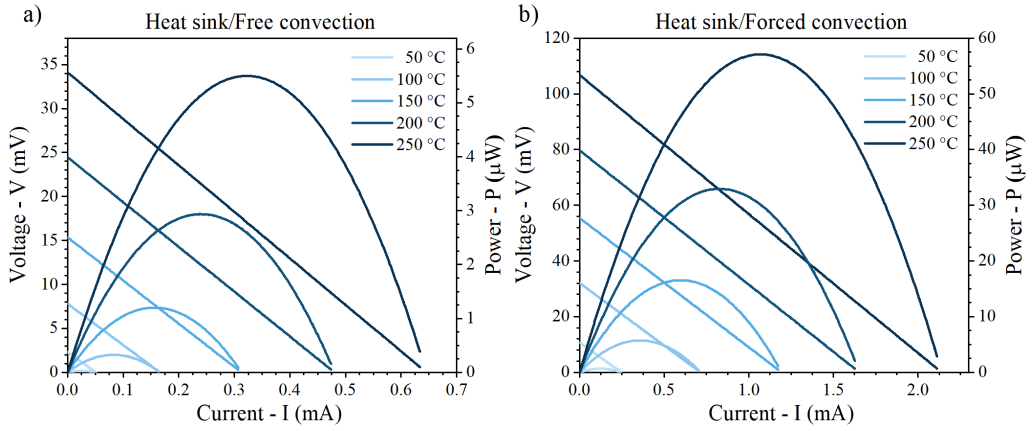


Figure 4.9: Voltage and power vs current in a parallel chip under free and forced convection. Comparing both cases, an increase of $\sim$ 3.1 and $\sim$ 10.5 is observed in open circuit voltage and maximum power, respectively, leading to a maximum power of 58 μW.

Table 4.1: Performance of a µTEG at the different stages of heat sink integration at 250ºC. Free convection means under still air conditions inside a cage with walls. In forced convection conditions a fan was used to impose an air flow of 1.3 m/s above the chip.

Integration step	Convection	ΔT (C)	V_{OC} (mV)	Increase	P_{max} (µW)	Increase
Bare chip	Free	2.5	4.5	-	0.1	-
Bare chip	Forced	9.8	17.6	3.9	1.54	15.4
Adapter	Free	6.3	11.3	2.5	0.61	6.1
Heat sink	Free	19.1	34.1	7.6	5.48	54.8
Heat sink	Forced	59.8	106.5	23.7	57.7	577

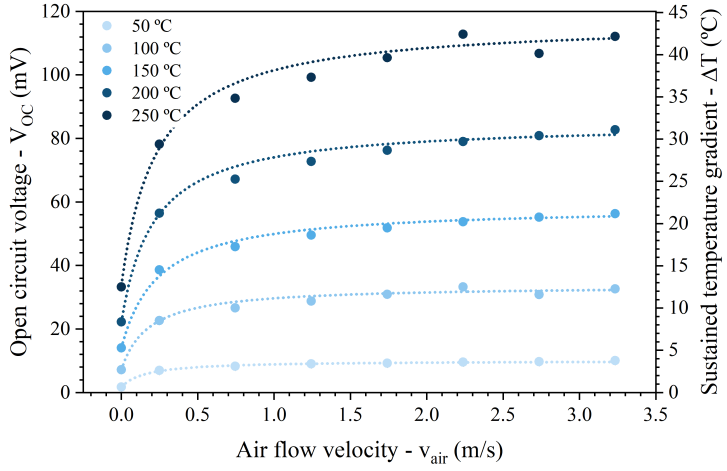


Figure 4.10: V_{OC} versus air flow velocity at different hotplate temperatures. Saturation is observed at every temperature even if the air flow is increased, indicating that limiting contact resistances come into place once the R_h^{Mixed} contribution starts to become negligible.

thermal model.

A second convection study was performed to evaluate the effect of air flow velocity on the open circuit voltage of a device with heat sink, the results of which are plotted in Figure 4.10. A rapid increase of V_{OC} is observed initially, followed by a saturation when air velocity becomes higher than 1 m/s. Since no saturation is expected in the heat transfer coefficient (h_{Forced}) at these air velocities [146], [147], the observed saturation must be associated to the µTEG–heat sink assembly. As explained in Section 4.1.2, this type of saturation is expected when the contributions of the heat sink and forced convection occur simultaneously. In that case, R_h^{Forced} becomes negligible in the denominator of f_{th} compared to the other contact resistances in the system ($R_h^{Forced} << R_{||} + R_{HP-Bulk} + R_{Adapter-HS}$ - see Equation 4.2). In this situation, further improvement of the heat transfer does not translate into a noticeable change in the temperature drop in the TE

element. Thus, to improve device performance under these conditions, the remaining contact resistances must be evaluated, with particular attention to the parasitic heating contribution of the adapter's corner pillars, which could be the dominant resistance in this configuration.

A comprehensive comparison of V_{OC}, sustained temperature gradient and P_{max} on a μTEG across the different heat sink integration stages, under both convection regimes at different hotplate temperatures is shown in Figure 4.11. Interestingly, V_{OC} of the μTEG with heat sink under natural convection is higher than that of the bare μTEG under forced convection (1.3 m/s). This indicates that the integration of the heat sink provides better thermal cooling than an increased air flow parallel to the chip surface. In this case, the resulting f_{th} is 8.7% at 250°C (considering ambient temperature at 30°C), which is a significant improvement over the cases without heat sink. In terms of power generation, it is worth mentioning that power densities in the range of IoT needs (> 10 μW/cm^2) are fulfilled in the fully integrated device for temperatures above 75°C under

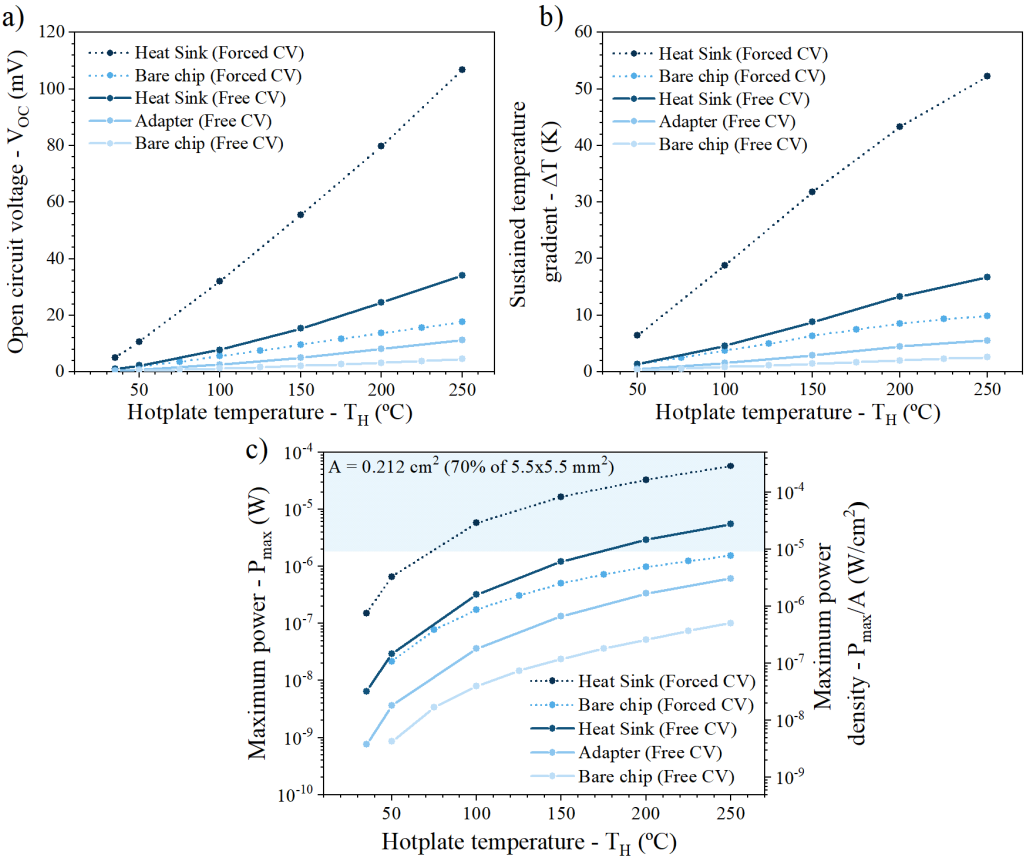


Figure 4.11: Comparisons of: a) open circuit voltage, b) sustained temperature gradient and c) maximum power and maximum power density as a function of the hotplate temperature across the different heat sink integration stages under free and forced convection conditions. The area dyed in blue in c) indicates the power density region in which the low-power IoT devices can operate in.

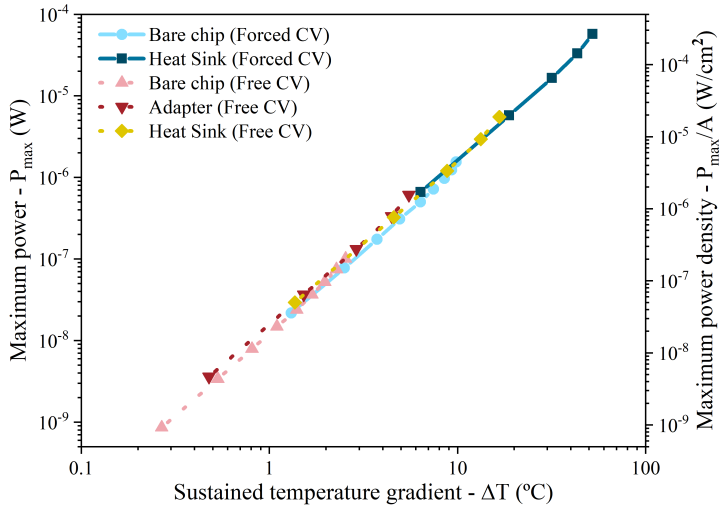


Figure 4.12: Maximum power versus sustained temperature gradient in the µTEG during all the heat sink integration stages and under free and forced convection conditions.

forced convection conditions and, most importantly, for temperatures above 175°C under free convection conditions.

Last, it is worth mentioning that the procedure used to integrate the heat sink on the µTEGs is robust and reliable as it does not compromise the intrinsic properties of the devices. This can be inferred from Figure 4.12, where P_{max} of the µTEG at the three different heat sink integration stages under both free and forced convection conditions is plotted against the corresponding sustained temperature gradient. As P_{max} is expressed as:

$$P_{max} = \frac{S^2 \Delta T^2}{4R_{int}} \tag{4.8}$$

the overlapping of the different stages and convection conditions indicate that neither Seebeck coefficient nor internal electrical resistance of the µTEG are affected. Since the heat sink integration could potentially damage the suspended platforms (through bending or breaking), the internal resistance might increase if such damage occurs. These results confirm the reliability of the integration process.

4.2.2 Microbeams

In microbeams case, full thermoelectric characterization was also completed for the different stages of the heat sink integration. The comparison of V_{OC}, P_{max} and sustained temperature gradient of two platforms with different number of microbeams (3 and 5) versus hotplate temperature are shown in Figure 4.13. Key observations can be extracted from these results. First, the platform with 3 microbeams achieves better performance in terms of V_{OC} and P_{max} before and after heat sink integration. However, V_{OC} of bare platforms with 3 microbeams is 1.85 times higher than that of the 5 microbeams platform, whereas this value is reduced to 1.16 after the heat sink integration. In terms of power, this reduction is higher as the ratio changes from 2.97 to only 1.12 with the heat

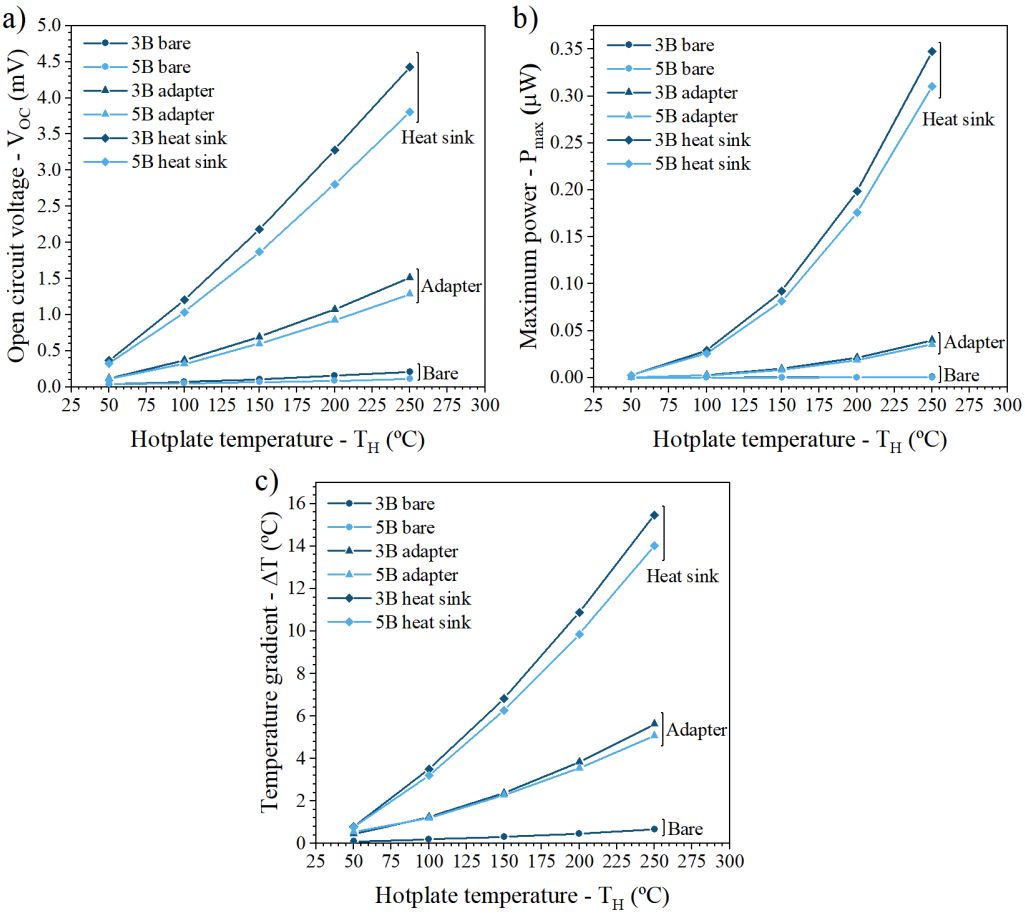


Figure 4.13: Comparisons of: a) open circuit voltage, b) maximum power and c) sustained temperature gradient versus hotplate temperature across the different stages of the heat sink integration.

sink. All these observations are consistent with the predictions of the thermal model in Section 4.1.2 (see Figure 4.6b). Since R_{TE} for the 3 microbeams platform is 1.66 times higher than the 5 microbeams one, the improvement obtained after the integration of the heat sink in this platform is expected to be lower.

The V_{OC} increase for microbeam devices with adapter and heat sink with respect to the bare configuration are shown in Figure 4.14. Improvements of 6.17 ± 1.76 and 17.39 ± 3.90 are obtained for the adapter and the heat sink cases, respectively. *Thermal Paste 1* was used on all these chips. The same behavior (i.e. a larger increase in the devices with lower thermal resistance on the TE element) is observed when comparing microbeam devices with NW devices presented in Section 4.2.1 (i.e. 8.96 ± 2.97 after the heat sink integration). This means that the V_{OC} increase for microbeam devices is ∼ 1.94 times higher than that of the NWs.

Taking all of this into account, we can compare the thermoelectric generation of the best parallel devices with NWs and microbeams before and after heat sink integration.

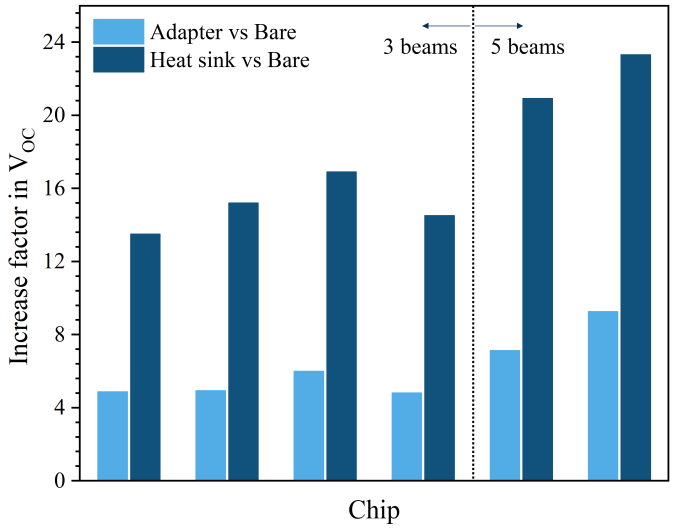


Figure 4.14: Improvement of V_{OC} of µTEG with 3 and 5 microbeams throughout the integration of the heat sink: (left/light blue) upon the integration of the adapter on the platforms, (right/dark blue) upon the integration of the heat sink on the adapter.

These measurements are shown in Figure 4.15. As shown in Figure 4.12, there is no effect on the internal resistance due to heat sink integration, which is also seen here in both NWs and microbeams, showing the microbeams a much lower R_{int}. As for V_{OC}, the NWs generate ~ 3.66 times the V_{OC} of the microbeams in the bare µTEG, but this is reduced to ~ 2.11 times once the heat sink is integrated. Finally, the plots of P_{max} show higher power generation in the microbeams µTEG, which is ~ 1.08 times that of the NWs. Here, a change of trend is observed as a consequence of the higher enhancement of V_{OC} on the microbeams, together with their quantitatively lower internal resistance, leading to a more optimal power generation.

Several conclusions are extracted from these results. First, it is evident that the device with the highest V_{OC} generation will correspond to the material with the lowest thermal conductivity regardless of the device's thermal management. Only in the ideal case where contact resistances are neglected and parasitic heat contributions are absent, will the sustained temperature gradient remain unaffected by the thermal conductivity of the TE material. Second, devices based on TE materials with higher thermal conductivity show a greater enhancement in terms of temperature drop across the TE element (i.e. in f_{th}, as predicted in Section 4.1.2). Lastly, the power factor has a more direct and significant impact on P_{max} than zT if an optimized thermal management is assured within the device. This implies that the strategy for making high power TE devices based on Si should point at developing robust micro-structures with high power factors and small internal resistances, while also maximizing the power output density by increasing the TE active area per chip. However, this holds true only where a heat sink integration or any other type of thermal management solution allows operation without relying entirely on the zT properties of the TE material (i.e. on its thermal conductivity). When thermal management is not possible, nanostructuring Si to enhance zT remains the main path to increase its thermoelectric capabilities. In summary, both structures, NWs and microbeams, have niche applications and the selection of one or the other will ultimately

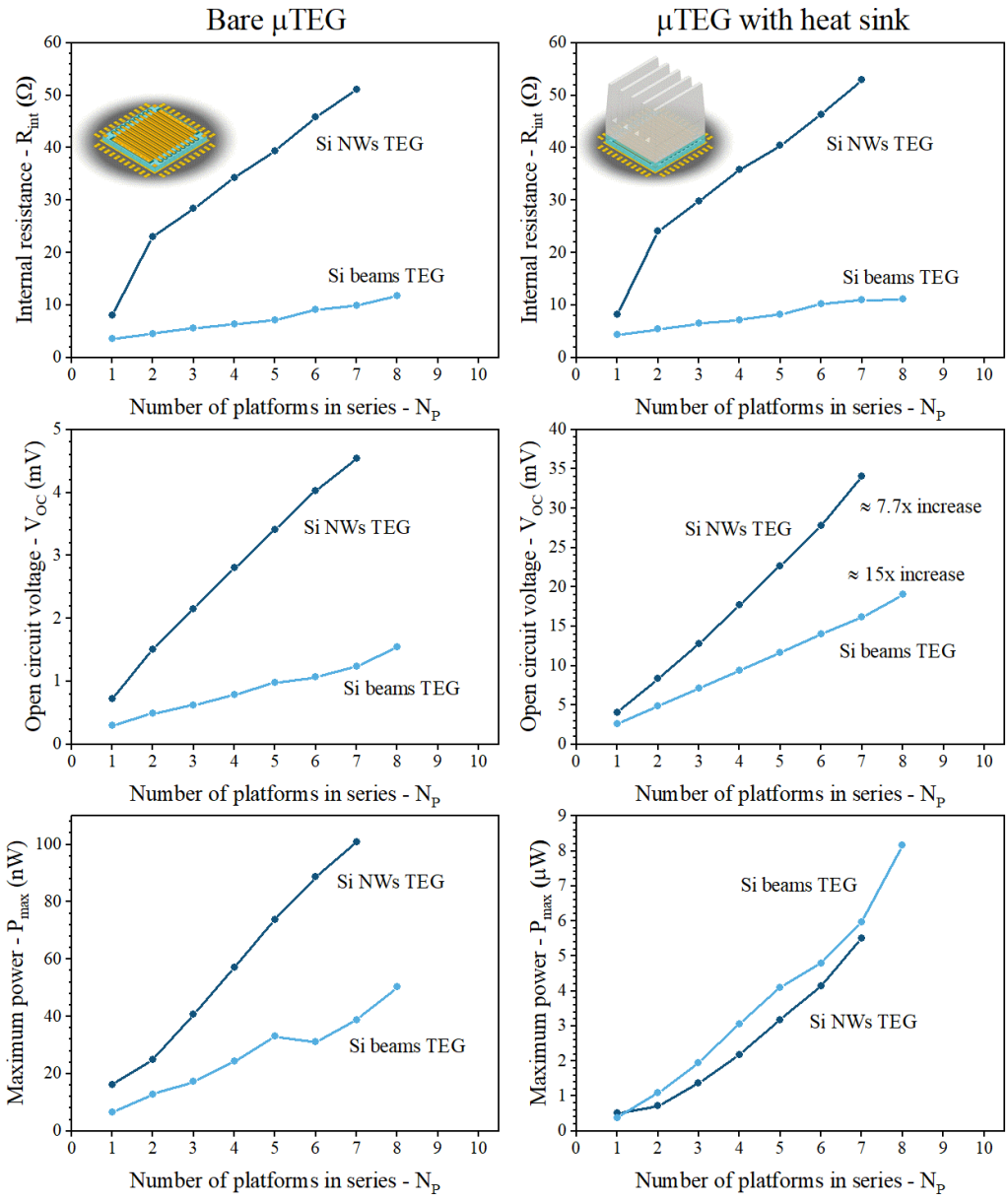


Figure 4.15: Comparisons of R_{int}, V_{OC} and P_{max} of two Parallel μTEGs with NWs and microbeams versus number of platforms connected in series before (left) and after (right) heat sink integration. Since internal resistance is not changing after heat sink integration, the lower difference observed in V_{OC} leads to a higher P_{max} in the microbeams device.

depend on the specific operating conditions and the device design possibilities that are available in each context.

Finally, some comparisons with TEGs based on Si structures reported in the literature can be done to assess the capabilities and challenges of the devices. Figure 4.16 shows the maximum power density vs sustained temperature gradient of this work devices compared to others extracted from the literature. Since the measurements in this plot are basically related to Equation 4.8, a higher power at a given temperature gradient indicates either lower electrical resistance in the device, higher Seebeck coefficient in the TE element, or both. This is the reason why the microbeams based µTEG has higher maximum power density compared to the NWs one. The rest of µTEGs, namely *Yanisawa* [106] and *Hu* [100], show even higher P_{max}/A due to their higher cross-section area of the TE Si. The figure used to compare µTEGs performance is the specific power generation capacity:

$$\varphi = \frac{P_{max}}{A \cdot \Delta T^2} \tag{4.9}$$

However, this is an ideal case, where the temperature gradient in the TE material is set externally to evaluate the performance of µTEGs, which is similar to the test mode explained earlier. As already explained, this does not evaluate performance under real application scenarios. To properly evaluate a µTEG in a real scenario f_{th} must be included, defining the specific *harvesting* power generation:

$$\varphi_{Harvest} = \frac{P_{max}}{A \cdot \Delta T_{TE}^2} f_{th}^2 = \frac{P_{max}}{A \cdot \Delta T_{Ext}^2} \tag{4.10}$$

With this equation, the µTEG real performance is evaluated, as it takes into account

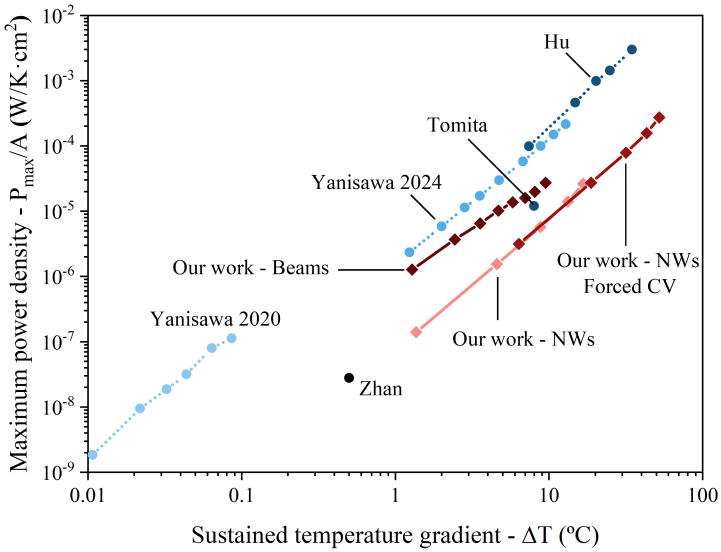


Figure 4.16: Comparison of P_{max}/A versus ΔT of this work µTEGs (NWs and microbeams) with the current state-of-the-art of µTEGs based on Si [100], [101], [106], [148], [149]. For a given temperature gradient, an increase in power output reflects either lower internal resistance, higher Seebeck coefficient, or both.

Table 4.2: Comparison of the specific power generation capacity and the specific *harvesting* power generation capacity of different μTEGs reported in the literature and this work μTEGs with heat sink. * Indicates that $\varphi_{Harvest}$ was calculated assuming a generous f_{th} = 1%, which is a rather optimistic assumption on cavity-free μTEGs. † Indicates that f_{th} was reported as $\Delta T_{TE}/\Delta T_{Hotplate-HS}$, and not calculated using ΔT_{Ext} (i.e. f_{th} is being overestimated).

	Zhan [148]	Tomita [149]	Hu [100]	Yanisawa [106]	Our work NWs	Our work beams
φ ($\mu W/cm^2K^2$)	0.11	0.19	29	1.31	0.09	0.39
$\varphi_{Harvest}$ (nW/cm^2K^2)	0.01*	0.02*	2.9*	133.75†	0.73	2.01

the μTEG capability to capture the available external temperature gradient. The values of both figures are given in Table 4.2. In terms of φ, the μTEG of *Hu et al.* [100] is the best due to the high density of Si microbeams integrated in the device, which significantly decreases its overall electrical resistance. However, these devices, similarly to those of *Tomita et al.* [149] and *Zhan et al.* [148], are fabricated without cavities, meaning that they exhibit significant thermal leakage and parasitic heat flow paths. The authors (Hu and Tomita) mention that the maximum f_{th} reached is 2 and 10% in test mode conditions, i.e. when forcing the temperature gradient in the cold and hot side of the μTEG. Thus, their performance in harvesting conditions will be limited. $\varphi_{Harvest}$ of these devices was calculated assuming a generous f_{th} = 1%, which is a rather optimistic assumption. *Yanisawa et al.* [106] provide enough data in the corresponding research article to extract f_{th}. Their μTEG excels with a value of 133.75 nW/cm^2K^2. However, it is important to note that the f_{th} measured by *Yanisawa et al.* does not account for the total external temperature gradient (ΔT_{Ext}), but rather for the gradient between the hot source and the heat sink (i.e. $\Delta T_{Hotplate-HS}$), thus overestimating f_{th}. This work μTEGs based on microbeams and NWs (under natural convection) are the second best devices among those tested under real working conditions. The high capacity of Yanisawa's μTEGs is a consequence of their large f_{th} under natural convection, which is achieved because their devices allow the integration of large heat dissipation elements (i.e. heat sinks) and a high density of TE elements per chip. Considering these results, the most suitable approach to further optimize the power generation capacity of the μTEGs developed in this thesis is the redesign of the adapter that interfaces the device and the heat sink to minimize parasitic heat flow paths. In this improved configuration, microbeam-based μTEGs with higher integration density would be significantly more competitive and could be comparable to the current state of the art.

4.3 Long term characterization

The significance of the long-term autonomy of the power supply in IoT was explained in the introductory chapter. Therefore, for a TEG to be considered as an energy source of an IoT system, a meaningful operational time should be fulfilled.

4.3.1 Nanowires

To study the long-time operation of generators for periods of 1000 hours, measurements were performed on NWs-based µTEG. As the objective of this study was to test the TEG in optimal working conditions (i.e. in maximum power generation) on harvesting mode, a dedicated LabVIEW program was built. The software measured V_{OC} and I_{SC} every minute and calculated the load matching conditions to be applied until the next measurement. This implies sinking a current equal to $I_{SC}/2$, which is equivalent to having a load resistance equal to the internal device resistance ($R_{internal} = R_{load}$). In this way, the µTEG is always set at maximum power output, which is the expected working condition of a TEG if used as an IoT power supply. The ambient temperature was also monitored throughout the experiment with the same LabVIEW program by means of a thermocouple placed just above the device.

Figure 4.17 shows the P_{max} generation of a NWs-based µTEG during one week at 150 and another week at 250°C. It is evident that the TEG is sensitive to the ambient conditions as P_{max} shows oscillations that correspond ambient temperature changes in day and night cycles. When ambient is colder, a larger temperature gradient is reached in the µTEG and a higher power output is measured.

The power generation throughout the 1000 h test (see Figure 4.18a) shows a stable power output for hotplate temperatures below 150°C, while slight increase or decrease is observed at temperatures above 200°C. Figure 4.18b shows V_{OC} measurements for the same period of time. Its trend matches that of the generated power for each hotplate temperature below or equal 200°C. In the 250°C case, instead, the voltage shows a constant increase, while the power has a slight decrease. In order to evaluate the level of degradation of the device, the power is normalized dividing by the temperature gradient squared. Since there were no dedicated thermometers on the platforms to measure the temperatures, the temperature gradient was calculated from the open circuit voltages shown in Figure 4.18b and the Seebeck coefficient values previously measured on these NWs (see Figure 3.7).

Figure 4.19 plots the normalized P_{max} and the internal resistance of the TEG

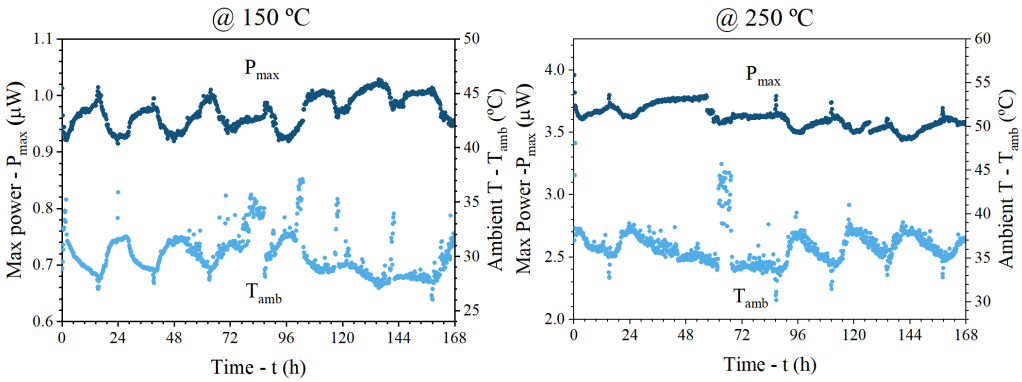


Figure 4.17: Maximum power and ambient temperature of a NWs-based Parallel-type µTEG measured continuously during 168 h at hotplate temperatures of 150 and 250°C. P_{max} shows oscillations that correspond ambient temperature changes in day and night cycles.

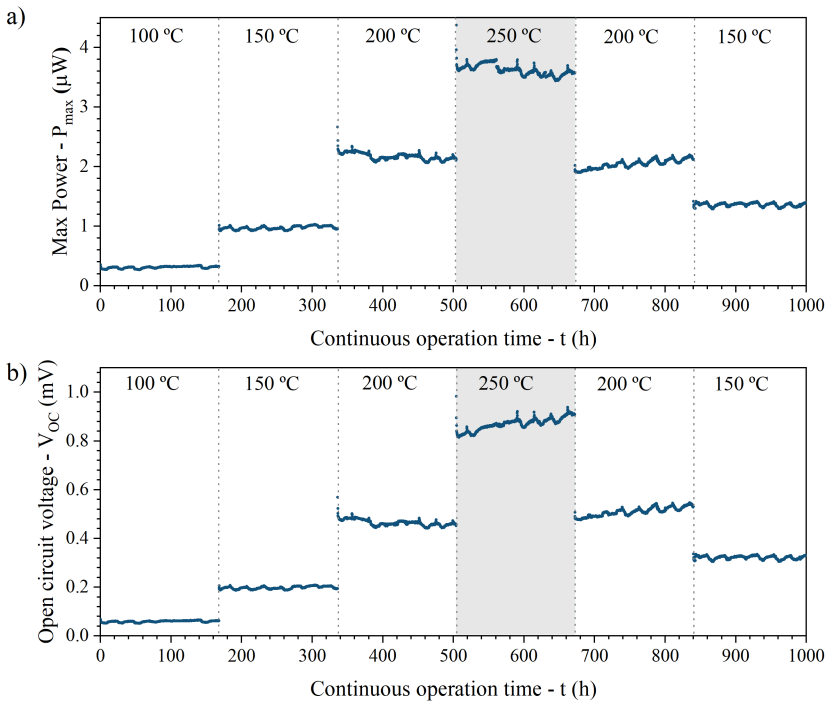


Figure 4.18: a) Maximum power of a NWs-based Parallel-type µTEG during 1000 h of continuous operation at different hotplate temperatures. A stable power output is observed at each temperature. b) Open circuit voltage of a NWs-based TEG during 1000 h of continuous operation at different temperatures.

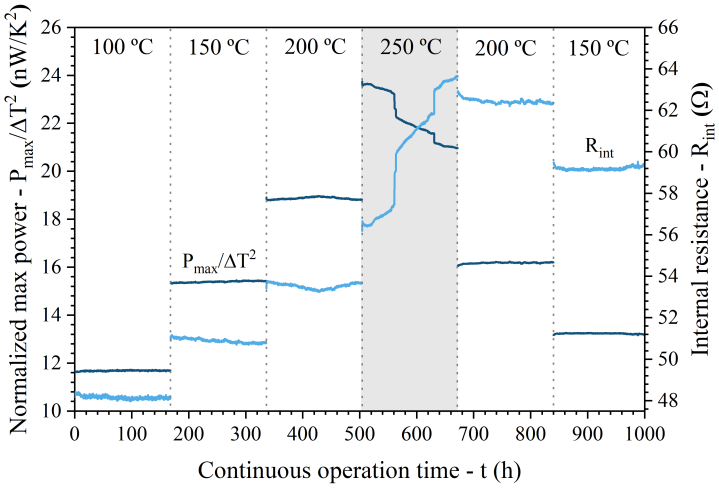


Figure 4.19: Normalized maximum power ($P_{max}/\Delta T^2$) and internal resistance measured in a NWs-based TEG during 1000 h of continuous operation at different hotplate temperatures. A clear degradation of the normalized maximum power at 250°C is observed as a consequence of an 18% increase in the internal resistance. At lower temperatures, the power stays constant with time. The degradation at 250°C is permanent and irreversible but stops once the TEG is brought back to lower temperatures.

throughout the 1000 h measurement. When the hotplate temperature reaches 250°C, the resistance of the device suffers an 18 % increase which is a clear indication of degradation. At hotplate temperatures below 250°C, the power remains constant during all the period. Interestingly, the degradation observed at 250°C is permanent and irreversible but the degradation mechanism stops once the device is brought back to a lower temperature. Then, the TEG was still performing with uniform but lower power generation at each hotplate temperature. In this sense, the normalized power measured at the same temperatures (150 and 200°C) before and after the degradation of the device have a gap of 2.2 and 2.8 µnW/K^2, respectively, which correspond to the degradation in normalized power measured at 250°C (2.7 µnW/K^2). The hotplate temperature dependence of the normalized power can be attributed to the electrical resistance and Seebeck coefficient change of the Si NWs with temperature, which explain the normalized power increase.

Taking into account these results and the previously shown voltage generation (Figure 4.18b), it can be concluded that a degradation of the internal resistance and an increase of the voltage generation take place when the hotplate reaches 250°C. This increase partially compensates for the resistance degradation and results in a near constant maximum power generation with time at 250°C.

4.3.1.1 Degradation study

To further study the reason behind the device degradation at this temperature, the heat sink and the adapter were removed from the µTEG. This resulted in the platforms breaking, as they were adhered to the adapter. This also demonstrated that there is no degradation of the platform-adapter attachment after 1000 h of operation. Once the NWs were exposed, a lamella of the cross-section of a degraded NW was fabricated. Another

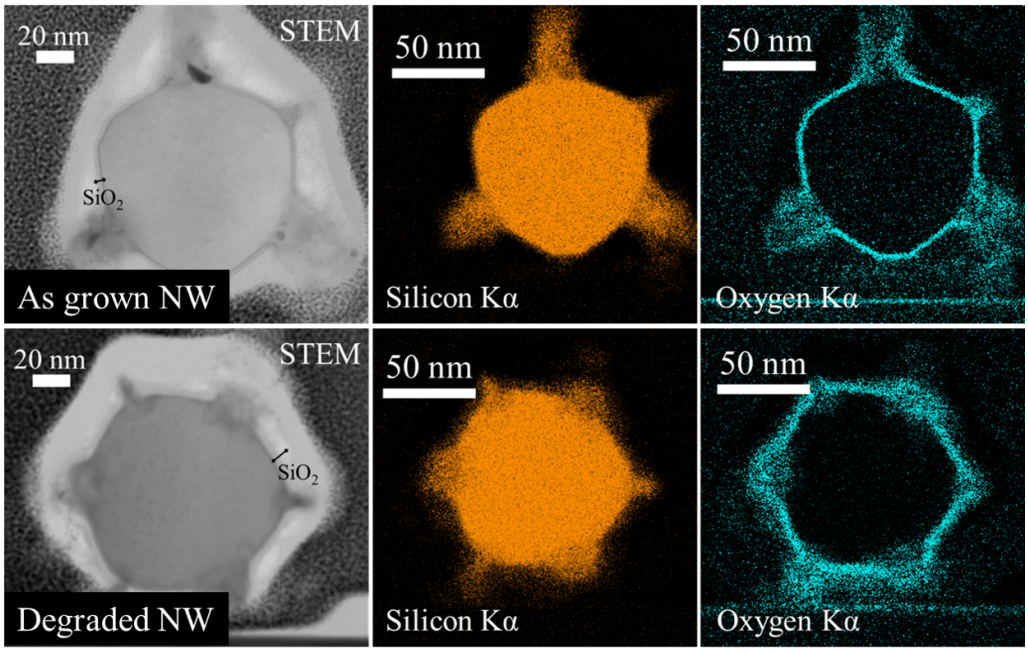


Figure 4.20: STEM images and Si and O distribution of the cross-section for (top) as grown Si NW and (bottom) a NW exposed during 168 h to 250°C.

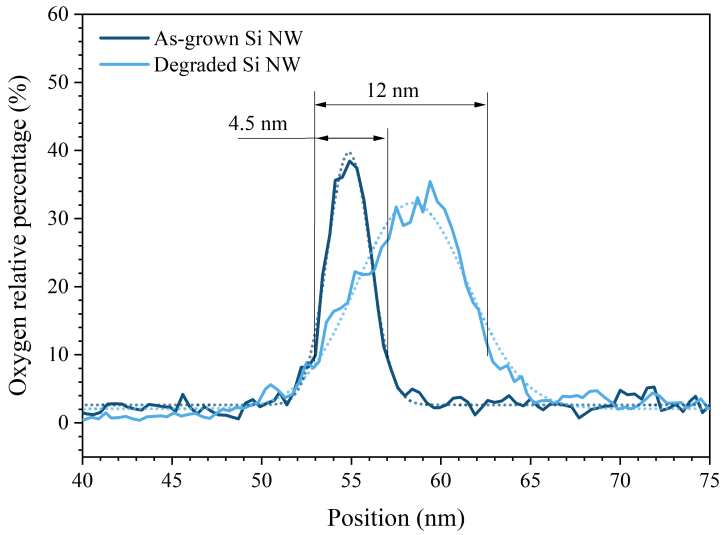


Figure 4.21: Thickness of the oxides in the as-grown Si NW and in the degraded NW. In dotted lines are plotted the Gaussian curves that fit the thickness measurements.

lamella of the section of a non-degraded NW was fabricated for comparison purposes. Figure 4.20 confronts STEM images for both NWs, together with EDS elemental abundance characterization. The STEM images show hexagonal NWs with a diameter around 135-140 nm with a thin layer of oxide. In the degraded NW, a thickening of this oxide is visible but difficult to measure due to the image low contrast. However, the EDS results show the presence of oxide clearly defined on the NWs surface, where both oxygen and silicon overlap. Line scans across the surface of the NWs were collected to evaluate their thicknesses (see Figure 4.21). Even considering an error of 2-3 nm because the EDS signal sees additional excitations of the secondary electrons in the interaction volume [150], the measured thickness of both layers obtained is $\sim$ 4.5 and $\sim$ 12 nm for the as-grown and the degraded NW, respectively. This leads to a $\sim$ 7-8 nm increase of the oxide. The reduction of cross-sectional conductive area can be approximated considering an hexagon with an initial diameter of 135-140 nm (the size of the degraded NW). This resulting value is $\sim$ 23-24 %, which is in great correspondence with the 18 % increase of the TEG internal resistance measured after the long-term studies. These results are also in agreement with the findings of *A. Pap et al.* [151], who observed an acceleration of the oxidation of Si at temperatures above 200°C when exposed for more than 5-10 h.

4.3.2 Microbeams

Regarding the TEGs based on microbeams, no noticeable degradation is expected even for temperatures above 200°C due to their large cross-sectional area. An enhanced native oxidation of the surface will have a negligible contribution to the total cross-sectional area of the beam ($\sim$ 8 nm of oxide vs the 5x15 μm^2 of the microbeams). A $\sim$ 5% lateral degradation of the microbeams would imply $\sim$ 63 years of continuous operation at 250°C. The Deal-Grove parabolic law at large times (i.e. $x(t)^2 = k_p \cdot t$, being x the oxide thickness, t the time and k_p the parabolic constant) was used for this calculation [152]. k_p was approximated considering that at 168 h the oxide thickness was 12 nm. To further

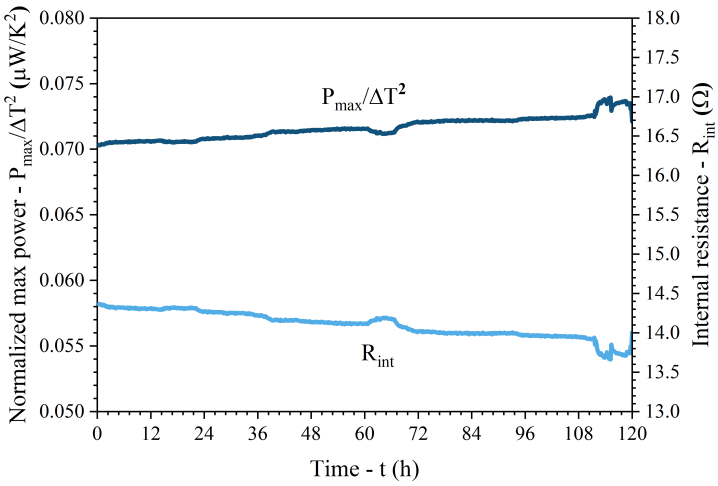


Figure 4.22: Normalized maximum power ($P_{max}/\Delta T^2$) and internal resistance measured in a microbeams-based TEG for 120 h of continuous operation at 250°C.

demonstrate that the degradation observed is a consequence of the NWs oxidation and not with the device degradation, a microbeams-based TEG was exposed to 250°C for 120 h. The results can be seen in Figure 4.22. It is clear that no degradation is taking place in this case, where even a $\sim$ 2 % decrease in the internal resistance is observed.

These results prove that Si NWs-based µTEGs are capable of generating power densities higher than 10 µW/cm^2 in long-term operation conditions with operation temperatures at or below 200°C. Therefore, they meet the requirements to serve as power sources for low-power IoT sensors. When operated at higher temperatures (i.e. at 250°C), their performance degrades due to native oxide growth on the NWs surface. Microbeams-based µTEGs can be operated at 250°C because native oxide growth has a negligible effect. As mentioned above, the oxidation rate on the microbeams would lead to $\sim$ 5% degradation of their internal resistance after 63 years of continuous operation at 250°C. This reflects that microbeams-based devices are most suited as power sources in the IoT domain when operated at temperatures above 200°C, as they will exhibit both higher power generation and long term stability.

4.4 Transient measurements

Most studies on µTEGs performance are in stationary conditions, assuming the device is thermalized. However, when the µTEG contacts a hot surface, there is a transient where the temperature gradient seen by the thermoelectric component of the µTEG is higher than the stationary one. This transient power generation peak ultimately depends on the overall thermal mass and heat flow paths of the device and is especially suitable for powering electronic devices that require a cold start voltage to operate. In this way, this type of devices can be turned on thanks to the transient and then operated by means of standard power generation in stationary conditions. To perform these studies, voltage, current, and power generation were monitored while hotplate temperature cycles were applied to observe the device thermalization.

4.4.1 Nanowires

Figure 4.23 shows three consecutive V_{OC} transients in response to hotplate cycles between 200 and 30°C, with great reproducibility. When heating the device, the voltage peaks to 94 mV which is ∼ 3.6 times higher than the steady state. Assuming an average Seebeck value of 250 μV/K (corresponding to an average temperature of 100°C in the NWs), the estimated temperature gradient is 62°C at the peak. This gradient then decreases to reach the thermalization value, which is around 11°C. A lower voltage peak appears when the hotplate is cooled down. In this case, a negative voltage is observed, indicating that the cooling rate of the bulk part of the device is higher than that of the platforms (caused by the higher thermal mass of the heat sink and the high $R_{\mu TC}$). A detailed view of the heating and cooling peaks can be seen in Figure 4.24. In the heating case, the TEG is generating ∼ 2.3 times the stationary voltage for more than a minute and reaches the steady state 6 min later. In the cooling case, the thermalization takes longer because there is no active cooling and the TEG is operating in reverse mode (i.e. $V < 0$, the temperature is colder in the bulk than in the platform) for more than 5 min.

The maximum power generation observed is equivalent to that of the V_{OC} but with an even higher increase factor. Three consecutive cycles are shown in Figure 4.25. Here, the maximum power peak is ∼ 37 μW (P_{max}/A ∼ 176 μW/cm^2), which is ∼ 13 times higher than the steady state value. Two main approaches can be considered to harvest the transient response in μTEGs: either the heat source exhibits variations over time, which could occur in a real working scenario, or the μTEG is coupled to an oscillating mechanism that intermittently contacts the heat source at a defined frequency. In both cases, an average power above the stationary would be generated in the μTEG. In the second case, however, the oscillation frequency must be accurately determined considering the peak duration, while ensuring an appropriate trade-off between P_{max} enhancement and the power required to activate the intermittent contact mechanism. As for the thermalization of the TE element, P_{max} measured in long term experiments is attained around 6 min

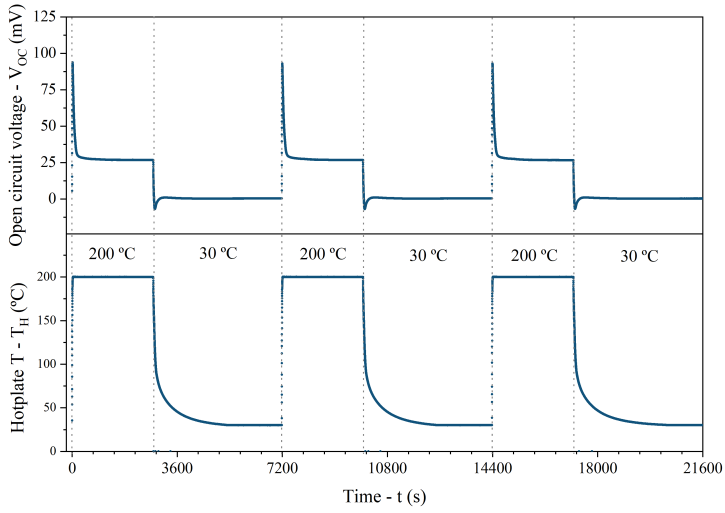


Figure 4.23: V_{OC} transients for three cycles measured during the heating and cooling at 200 and 30°C. The voltage peaks at 3.6 times the steady state output and reaches > 90 mV. The bottom plot shows the hotplate temperature during the cycles.

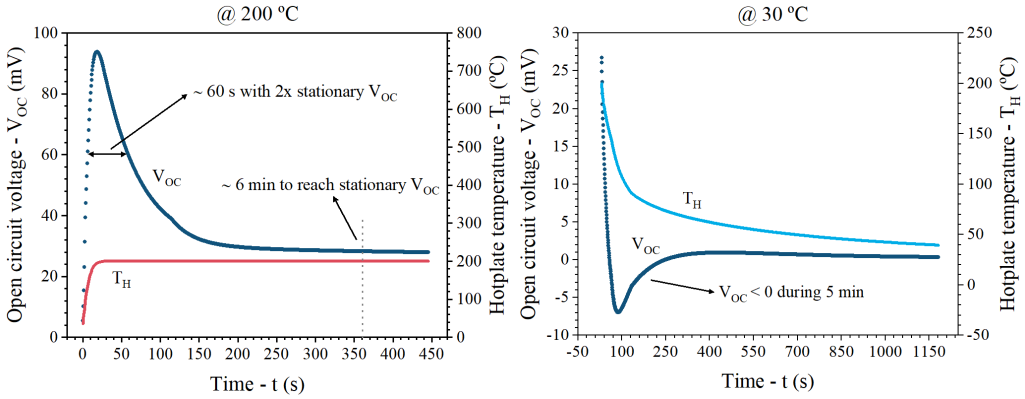


Figure 4.24: Detailed view of open circuit voltage peaks after heating and cooling. During the heating, the voltage is above 60 mV for $\sim$ 60 s. At the peak, the voltage reaches 94 mV. During cooling, the output voltage becomes negative due to the lower cooling rate of the platforms.

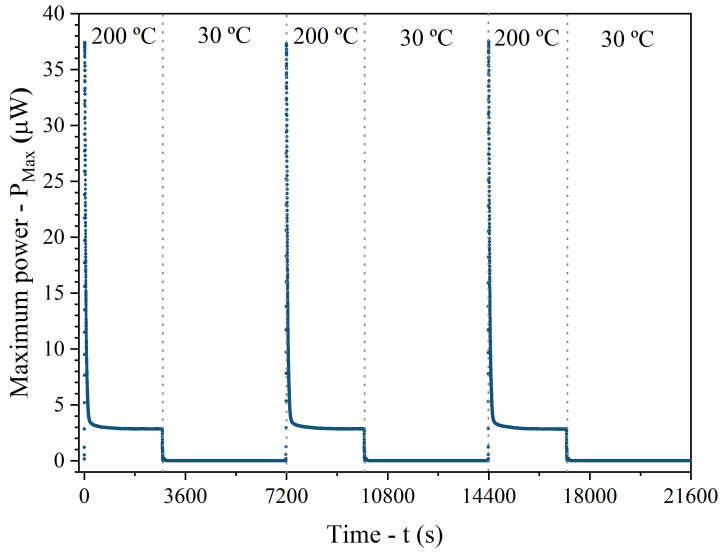


Figure 4.25: Example of three maximum power transients while heating and cooling the TEG at 200 and 30°C. The maximum power peak is > 37 µW which is 13 times higher than in the steady state ($\sim$ 2.8 µW).

after the hotplate reaches its target temperature in the transient measurements (i.e. the μTEG reaches a steady state after ∼ 6 min).

The most straightforward and easier application for the transient behavior of μTEGs is turning on power management devices that have a cold-start voltage, as mentioned above. A comparison between V_{OC} of a NWs-based μTEG at 200°C and the requirements of some state-of-the-art DC-DC boosters (Lim, Ramadass and Bose [153], [154], [155]) is discussed in Figure 4.26. The comparison shows that the transient voltage of the μTEG complies with the requirements of all three DC-DC boosters considered. μTEGs based on microbeams may also be compatible with boosters operating them at 250°C. At this temperature, a 20 mV steady state voltage can be obtained. The transient characteristics in free and forced convection (see Figure 4.26) show similar thermal dynamics duration but different peak behavior. On the one hand, the voltage peak in free convection is ∼ 3.44 times higher than the steady state value, while in forced convection is only ∼ 1.17 times higher. During the transient, the bulk part of the μTEG is rapidly heated up, but the heat sink needs a longer time to reach its steady state (∼ 6 min). Under free convection, the platform reaches a higher steady-state temperature, causing a larger temperature change during thermalization and a marked voltage drop after the peak (during thermalization the cold-side temperature increases). Under forced convection, the platform exhibits a smaller temperature variation. Consequently, the voltage drop following the peak is less pronounced.

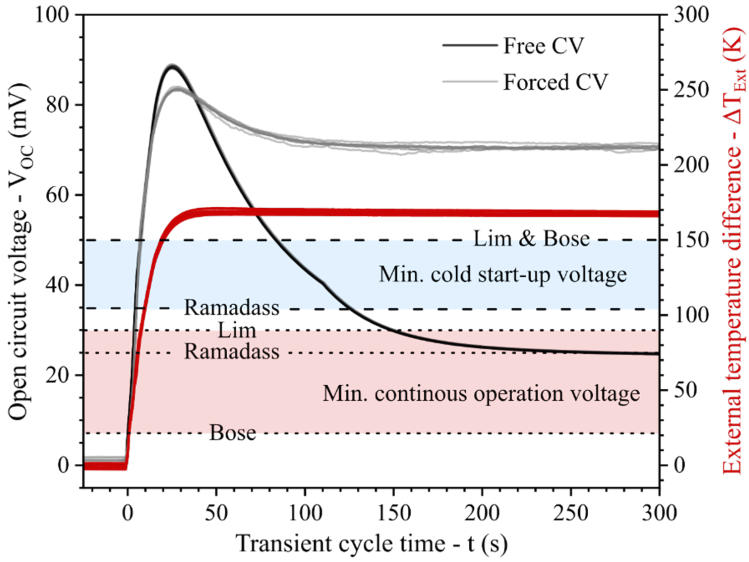


Figure 4.26: Comparison of ten V_{OC} transients overlapped at 200°C versus voltage ranges needed by state of the art DC-DC boosters with cold-start voltage. Measurements shown correspond to natural convection (black) and forced convection (gray). The red shaded region corresponds to the minimum voltage needed by three DC-DC boosters found in the literature: Lim, Bose and Ramadass [153], [154], [155]; the blue shaded area represents the cold-start voltage range needed to turn them on. The right axis indicates the external temperature gradient (i.e. difference between hotplate and ambient). The red curve shows the evolution of ΔT_{Ext} during the transients.

4.5 2x2 Thermoelectric generator

Scaling up the number of µTEGs per device can lead to two potential improvements. The most obvious one is the higher voltage (or current) obtained by simply adding µTEGs in series (or in parallel) to reach the power demands of a given application. The second, and most interesting, is the possibility of enhancing the thermal management of the device by integrating a larger heat sink to potentially increase the power generation of each one of the individual µTEGs. This section introduces and addresses the challenges towards such integration.

4.5.1 Device design

The device fabricated for this scaled-up proof-of-concept is composed of four individual µTEGs. Microbeams-based µTEGs were selected for their superior power generation capabilities, their potential for enhanced performance through improved thermal management, and their mechanical robustness. A PCB was specifically designed to allocate four µTEGs in a 2x2 array layout (see Figure 4.27). Wire bonding was performed such that the final device is equivalent to a chip with 20 platforms connected in series, each having double the width of individual µTEGs. The PCB also has dedicated solder jumpers on the sides to bypass any broken or malfunctioning platform (each jumper would bypass 4 µTC, as indicated in Figure 4.27). Regarding the internal and external collectors of the chips, ones are bonded directly to the PCB while the others are wire bonded connecting the chips.

The encapsulation of the PCB with four µTEGs is designed as shown in Figure 4.28. The PCB is mounted and screwed onto an aluminum base that is later placed on the heat source. This metallic piece is used to minimize the thermal resistance between the PCB and the heat source. Since the heat sink can not be supported by the adapters without compromising the integrity of the platforms, a spacer was used to provide mechanical

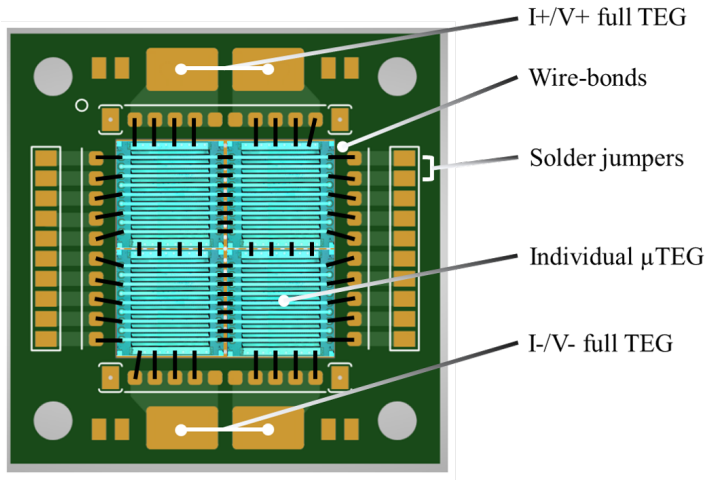


Figure 4.27: Layout of the 2x2 array of Parallel chips hosting microbeams-based µTEGs in the PCB. The final device is equivalent to a chip with 20 platforms connected in series that have double the width compared to individual µTEGs.

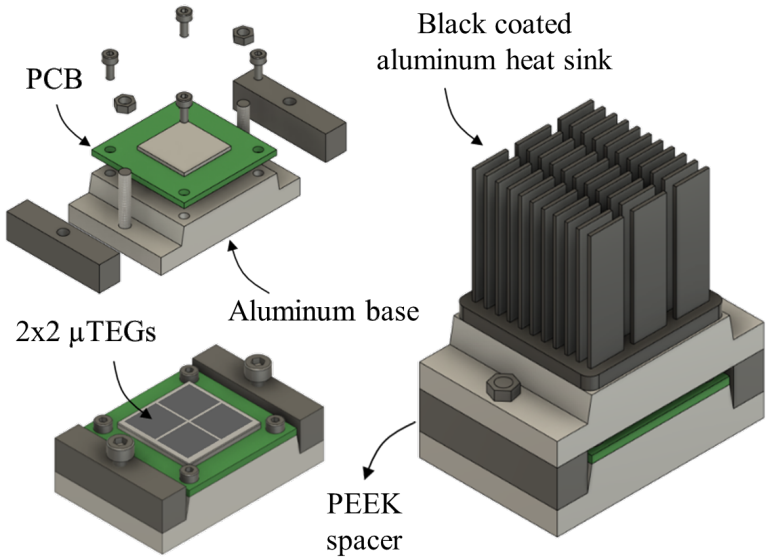


Figure 4.28: Scheme of the 2x2 integration design. The PCB is mounted on an aluminum base and two PEEK spacers serve to support the aluminum heat sink. The height of the spacers is designed to allow the heat sink to be screwed in place without exerting pressure on the Si adapters integrated into the four μTEGs.

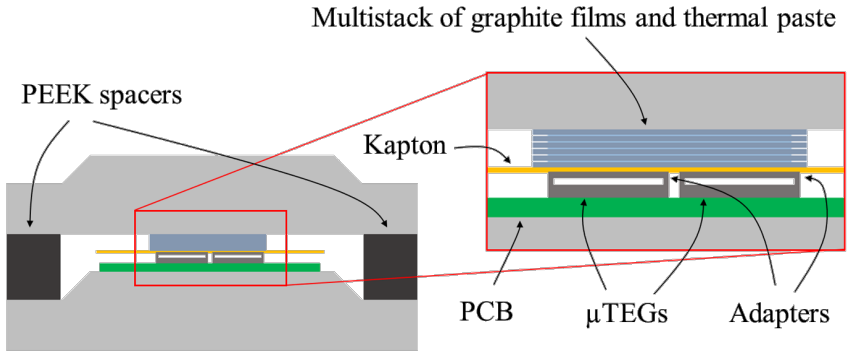


Figure 4.29: Scheme of the multi stack structure that has been used to ensure a good thermal contact between the Si adapters and the heat sink. Kapton tape is used to avoid thermal paste spreading onto the μTEGs.

support. This component provides mechanical rigidity, thermal isolation, and stability during the heat sink integration, similar to the role of the corner pillars in the Si adapter. Polyether ether ketone (PEEK), a polymeric material with low thermal conductivity (0.25 W/m·K) that can withstand temperatures up to 340°C, was chosen as the spacer material. Finally, a black coated aluminum heat sink with an aluminum base is mounted on top of the PEEK spacers and screwed to ensure good thermal contact.

The most critical step of the integration process is the contact between the heat sink

and the Si adapters on the µTEGs. The PEEK spacers were fabricated with sufficient height to leave a safety gap between the adapters and the heat sink, which has to be filled with some material to achieve a good thermal contact. The main challenge is that the four µTEGs are pasted and bonded to the same PCB and may result in uneven height and tilting of the adapters. This imposes the use of some material with flexibility to conform to these differences. As thermal paste alone on the adapters could overflow and short circuit the wire bonds, it was decided to include a Kapton film between the adapter and the heat sink to ensure electrical isolation and protection of the wire-bonds. A multilayer stack consisting of alternating layers of thermal paste and graphite foils was assembled (see Figure 4.29). The graphite foils provide high in-plane thermal conductivity and mechanical flexibility, while the thermal paste ensures conformal contact between layers, reducing interfacial thermal resistance. This layered configuration improves overall heat spreading and accommodates surface irregularities during assembly.

4.5.2 Integration process

Figure 4.30 shows the µTEGs wire bonded to the PCB and with the adapters. The picture on the left shows that part of the platforms on the µTEGs were already broken at this stage. The integration of the Si adapters was completed as described in Section 4.1.1. The picture on the right suggests that the height of the four adapters is uneven. This is a consequence of the chips packaging on the PCB which results in an uncontrolled final height. Besides, a Pt100 is also welded to the PCB to measure the PCB temperature next to the µTEGs.

During the heat sink integration, V_{OC} was constantly monitored (with a hotplate temperature of 100°C) to detect when a thermal contact was established between the adapters and the heat sink. At this point, a first thermoelectric characterization was carried out. Afterwards, the heat sink was screwed to the aluminum base to ensure better contact and mechanical stability of the ensemble. This integration process validated the scaling of the number of µTEGs and the integration of larger heat sinks on the µTEGs fragile platforms. No significant change in the µTEGs internal resistance was detected throughout the integration steps, indicating that the TE elements were not damaged during the process.

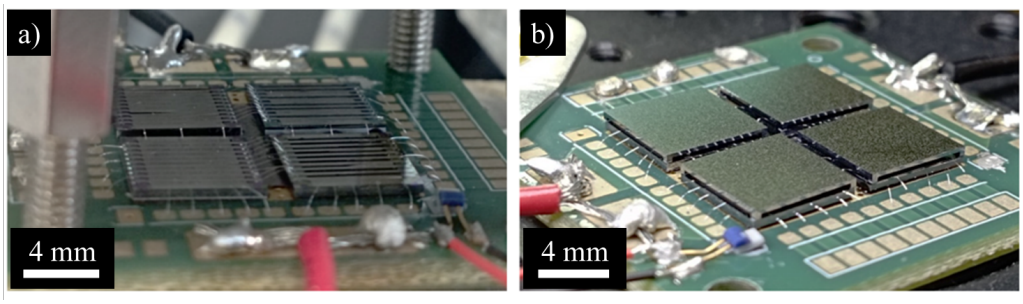


Figure 4.30: Pictures of the 2x2 array of µTEGs after the wire bonding in the PCB (a), and after the integration of the adapters and welding of the Pt100 (b).

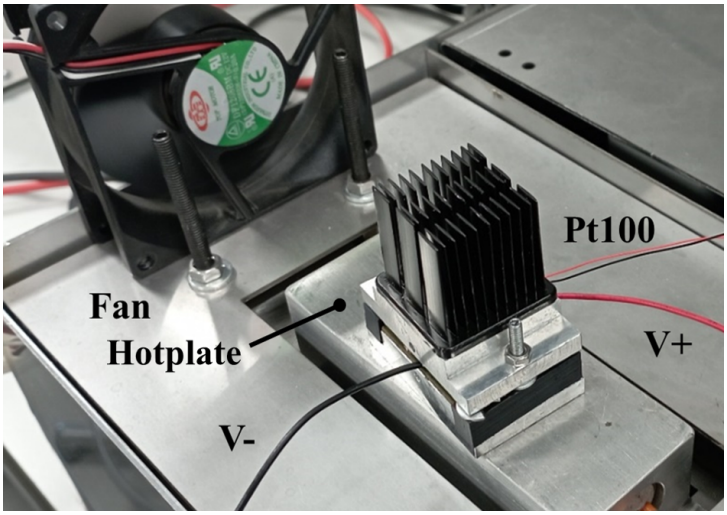


Figure 4.31: Picture of the setup used to characterize the integrated device with the heat sink. The device is placed on top of a hotplate and a fan next to it with the air flow direction parallel to the heat sink fins.

4.5.3 Thermoelectric characterization

The setup used to characterize this 2x2 µTEGs device can be seen in Figure 4.31. The device is placed above a custom-made hotplate while voltage, current and power are monitored. A fan is positioned with the air flow direction parallel to the fins of the heat sink to evaluate the performance under both free and forced convection conditions. A comparison of the device P_{max} and V_{OC} at different heat sink integration stages as a function of the hotplate temperature is shown in Figure 4.32. These include the bare µTEGs, the µTEGs with Si adapters and the final integrated device before and after screwing the heat sink (the final stage -screwed heat sink- is indicated with the + sign).

The increase factor observed in V_{OC} due to the heat sink integration is ~ 20.5 (i.e. $V_{OC}^{HS+}/V_{OC}^{Bare}$), which is ~ 1.2 times higher than the average increase factor of the microbeams-based µTEGs with the individual heat sink (see Figure 4.14 with 3 microbeams). This is due to the reduction (i.e. decrease) of the thermal resistance of the heat sink to ambient, R_h^{HS} in Equation 4.7, which results in a thermal gradient increase at the TE elements. The importance of the thermal contact between the adapters and the heat sink can be seen by comparing V_{OC} and P_{max} before and after screwing the heat sink (Figure 4.32 with or without + sign). Interestingly, the same performance in terms of V_{OC} and P_{max} is observed for screwed heat sink under free convection and the unscrewed one under forced convection. This implies that the heat sink-adapter thermal contact enhancement is equivalent to forcing an air flow (1.3 m/s). This result highlights the importance of having good thermal contacts between the different components of the device.

The measurements reported so far correspond to different hotplate temperatures. The thermal contact between the hotplate and the bottom aluminum block was done without any thermal paste, therefore a high thermal resistance was expected. This implies that the PCB temperature differs from the hotplate temperature, specially in forced convection conditions and high hotplate temperatures. A deviation of up to 30°C was

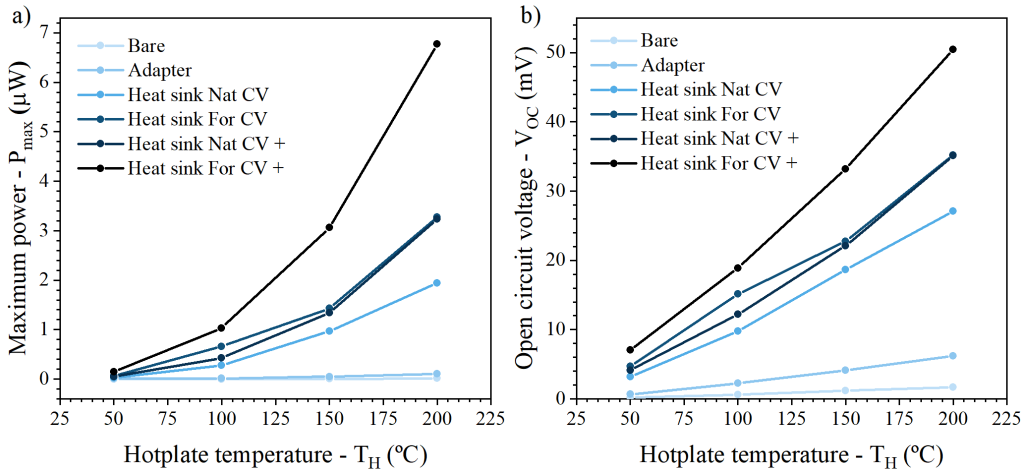


Figure 4.32: Comparisons of a) the maximum power and b) the open circuit voltage of the device at different heat sink integration stages as a function of the hotplate temperature and convection conditions (Nat and For correspond to natural and forced convection, respectively). The + sign in the legend indicates that the heat sink was screwed, while no + sign means the heat sink is only placed on top of the TEG.

measured at a hotplate temperature of 200°C under natural convection. An additional performance characterization using the Pt100 temperature is shown in Figure 4.33. Note that the forced convection case, does not have a 200°C curve because that would imply setting the hotplate temperature above 250°C which could damage the PCB. When comparing V_{OC} for both cases (free and forced convection) we see an increase of ~ 1.7 at 150°C, which is lower than the ~ 3.1 value obtained for the individual µTEGs (see Table 4.1). The decrease is caused by the saturation effect shown in Section 4.1.2. Be-

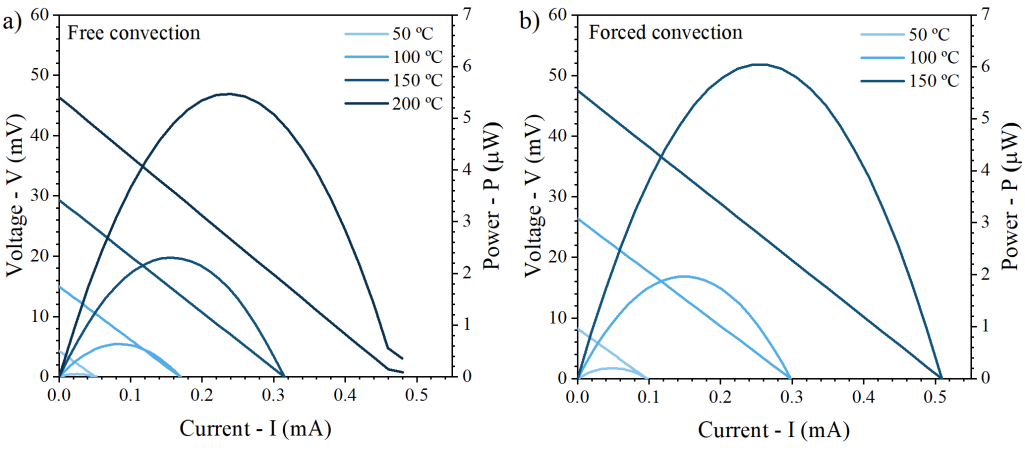


Figure 4.33: Voltage and power versus current measured on the 2x2 TEG based on Parallel µTEGs with microbeams under free and forced convection. An increase of ~ 1.7 is observed in the open circuit voltage, leading to a maximum power of 6.2 µW at 150°C.

yond a given value of R_h^{Forced} its contribution on f_{th} becomes negligible compared to the other limiting contact resistances. As it was mentioned before for this device, the parasitic heating and the heat sink-adapter thermal contacts are worse than those of the individual µTEGs, justifying a lower increase of V_{OC} under forced convection.

Overall, the results of this section demonstrate that it is possible to scale up the number of µTEGs per device and to use a larger heat sink, thereby further enhancing the power generation of each individual µTEG. The main challenge relies on reliably integrating and contacting a large heat sink with a chip that features fragile suspended platforms. Further investigation is needed to develop a more effective contacting method. Nevertheless, the use of a multi-layer stack composed of thermal paste and graphite films proved sufficient to fabricate a functional device, which exhibited a greater increase in the temperature gradient compared to the device with a single heat sink.

4.6 Chapter conclusions

The limitations of bare Si-based µTEGs led to developing a reliable integration procedure with a custom pick and place system that uses a Si adapter piece as an intermediate step. This implementation led to 9 and 17-fold improvement in the thermal gradient for NWs and microbeams-based µTEGs, respectively.

The characterization of the µTEGs demonstrated that the microbeams-based µTEGs have a higher increase in power generation after heat sink integration, finally surpassing the values of NWs-based µTEGs. Thus, it was proven that, as long as the heat management is properly optimized on the overall µTEG, the TE material with lower electrical resistance shows higher power generation. This implies that, given an appropriate µTEG design, the most suitable TE material is the one with the highest power factor, rather than the one with the best zT. Lastly, power density values above 10 $\mu W/cm^2$ were achieved on the Parallel devices with heat sink for hot temperatures above 175°C under natural convection and above 75°C when a forced convection equivalent to a natural breeze (i.e. 1.3 m/s) is present. These values are within the range of low-power IoT sensor requirements. Further characterization of the long term stability of the NWs and microbeams-based µTEGs demonstrated that there is no degradation in the NWs for temperatures up to 200°C under continuous operation for more than a month. In the microbeams case, no degradation is observed in the temperature range studied (i.e. from 50 to 250°C). STEM studies proved that the NWs degradation was caused by an enhanced oxidation at temperatures beyond 200°C. The results of the transient measurements on the µTEGs showed that possible applications of these generators could be expanded to power devices with high cold-start voltages.

Finally, a TEG integrating 4 µTEGs on the same device with a large heat sink was shown. This required a new approach for the integration of the heat sink to accommodate the uneven heights of the different components. These results demonstrate the possibility of scaling up the number of µTEGs per device. The integration also enables an increase in the efficiency of each individual µTEG by implementing larger heat sinks for improved thermal management.

Part III

Thermoelectric characterization of silicon thin films nanostructured with block copolymers

Chapter 5

Silicon thin films nanostructured with block copolymers

This chapter summarizes the results related to the topic of nanostructuring Si thin films using block copolymers. The first section is devoted to describe in detail the procedures for depositing and controlling the morphology of the BCP. The second section describes the process of transferring BCP patterns into silicon thin films. Finally, the use of spin on dopant for doping Si films is presented, followed by the electrical characterization of the doped and nanostructured thin films.

5.1 Block copolymer self-assembly

Self-assembly of block copolymers on free surface (without the use of guiding patterns to orient the BCPs) was conducted using silicon as a substrate. In this configuration, the orientation of the patterns is controlled with a random copolymer, called the brush layer, used to ensure that the surface affinity of both blocks of the BCP towards the substrate is similar. If this is properly done, a vertical orientation takes place. All block copolymers used in this thesis were supplied by a French company called Arkema S.A. whose trade name is Nanostrength®EO. Some of the BCPs were already supplied dissolved in Propylene glycol methyl ether acetate (PGMEA), while others were in powder form. These were later dissolved with different weight concentrations to deposit thin films of BCPs by means of spin-coating. The properties of these random and block copolymers are shown in Table 5.1.

Before spinning the random copolymer, the chips were cleaned in acetone and IPA and later introduced in a PVA TePla machine to perform an oxygen plasma treatment that both eliminates organic residues and activates the Si surface. Afterwards, the random copolymer was spin-coated on the samples at 2000 rpm during 30s. During this thesis, three different brush layers were used: NL1, or R70, with a weight fraction of both components of 69.2% PS - $\sim$ 30.8% PMMA; NL2, or R60, with a weight fraction of both components of 58.8% PS - $\sim$ 41.2% PMMA; and NL18, or R75, with a weight fraction of both components of 74% PS - $\sim$ 26% PMMA. All three were dissolved in PGMEA

Table 5.1: Properties of the brush layers and block copolymers used in this thesis.

Type	Period (nm)	Molecular weight (kg/mol)	PS weight (%)	PMMA weight (%)
Brush NL1	-	9.9	69.2	30.8
Brush NL2	-	7.9	58.8	41.2
Brush NL18	-	8.4	74	26
Lamellar	22	42.3	42.8	57.2
Lamellar	24	44.4	40.3	59.7
Lamellar	31	68.8	43.6	56.4
Lamellar	37	79	50	50
Cylindrical	35	60.8	69.08	30.92
Cylindrical	80	219.6	70.4	29.6

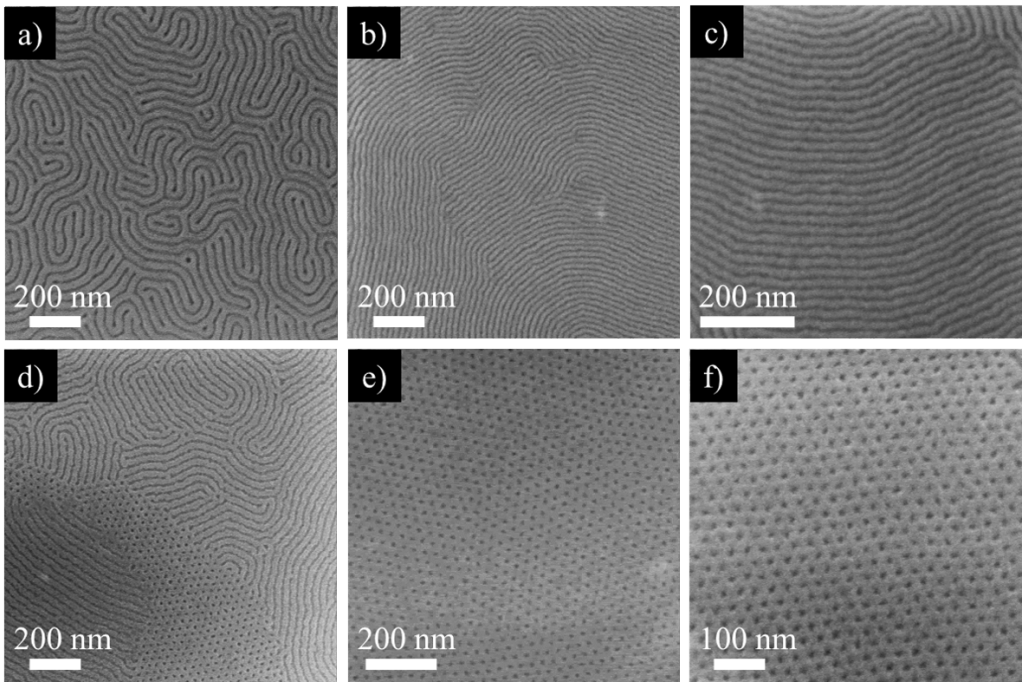


Figure 5.1: Example SEM images of BCPs self-assembled in free surface: a) Lamellar BCP with period = 37 nm (L37), b) L24, c) L22, d) miss-oriented cylindrical BCP with period = 35 nm (C35), e) C35 and f) amplified C35. d) and e) show the different orientations that are obtained depending on the thickness of the BCP film (50 and 30 nm, respectively). A C35 BCP with a thickness > 40 nm has mixed vertical and horizontal cylinder orientation while for thicknesses below 35 nm the alignment is always vertical.

with a weight fraction of 1.5%. The first two were used for BCPs with small periods and the later was used for blends of cylindrical BCPs with larger periods (see Section 5.1.1). NL1 was used to orient the PMMA cylinders vertically, and NL2 was used to form the lamellar patterns perpendicularly to the substrate. After spinning the random copolymer, the samples were introduced in a tube furnace with nitrogen ambient and annealed during 5 min at 230°C. Thanks to this annealing and the previous activation of the Si surface, a very thin ($\approx$ 8 nm) film of the random copolymer is grafted to the substrate, forming the brush layer. To eliminate the remaining non-grafted random copolymer, the chips were cleaned in a PGMEA bath with ultrasounds for 1 min. Later, the BCP was spin-coated above the brush. Finally, a second annealing was performed in the furnace at 230°C during 10 min. As this temperature is above the glass transition temperature of both blocks (PMMA $\approx$ 108°C [156], PS $\approx$ 100°C [157]), thermally-driven diffusion is activated and the BCP pattern is formed.

The results of the free surface self-assembly are shown in Figure 5.1. As the objective of this work is the nanostructuration of Si using the BCP pattern as a mask, the thickness of the film is of utmost importance and should be as large as possible. The deposited thickness as a function of the spinning velocity is shown in Figure 5.2. To obtain these values, a first sample was prepared with only the brush layer grafted onto Si and was used as the reference in the ellipsometry measurements performed with a Horiba Jobin Ivon/AutoSE Ellipsometer. Later, eight samples with four different spinning velocities and a weight fraction of 2% wt in PGMEA were measured. The relationship between BCP thickness (t_{BCP}) and spinning velocity (ω_s) should be: $t_{BCP} = k{\cdot}\omega_s^{-b}$, where k is a given constant that depends on the material properties and b is a value between 0.5 and 0.66, depending on the evaporation rate of the solvent [158], [159]. As can be seen, the data fits the curve perfectly with $b = 0.5$, meaning that the evaporation rate of these samples is $\propto \omega_s^{-1/2}$. For dissolutions with lower weight fraction, the thickness was calculated using the above data and assuming a linear relationship between the BCP weight fraction in PGMEA and the film thickness (this is only true if the weight fraction is $< 2\%$ [158], which is the case in this work).

In the case of the lamellar BCPs, a thickness > 50 nm is compatible with perfectly perpendicular patterns regardless of the periods. Therefore, the optimal spinning conditions were found to be 2000 rpm during 30s using a 2% wt dissolution of BCP in PGMEA. The cylinders, however, have orientation problems when the film is too thick. Figure 5.1 shows three SEM images of cylindrical patterns. Figure 5.1d has a BCP thickness of 50 nm and Figure 5.1e has one of 30 nm. It is clear that the left has a high misorientation of the cylinders in some areas, where the lying down cylinders resemble the fingerprint-like pattern of the lamellas. With the brush used in this work (R70) the functional thickness range to have perpendicular cylinders was found to be < 35 nm. The optimal conditions used for the self-assembly of these BCPs were 1500 rpm during 30s using a 1% wt dissolution of BCP in PGMEA. If a thicker film is required, replacing this brush with another that has a higher PS content could help widen the functional thickness window [160]. However, a thickness of 35 nm was later found to be suitable for patterning 50 nm-thick films. Regarding the C80 BCP, even using the R75 brush layer it is difficult to obtain a correctly aligned pattern due to its high molecular weight. Also, this period is not interesting enough for thermoelectric purposes due to the large neck size between holes ($\approx$ 40 nm), which is almost equivalent to the thickness of the Si films used in this work. For these reasons, this BCP was only used in blends to obtain intermediate cylindrical periods.

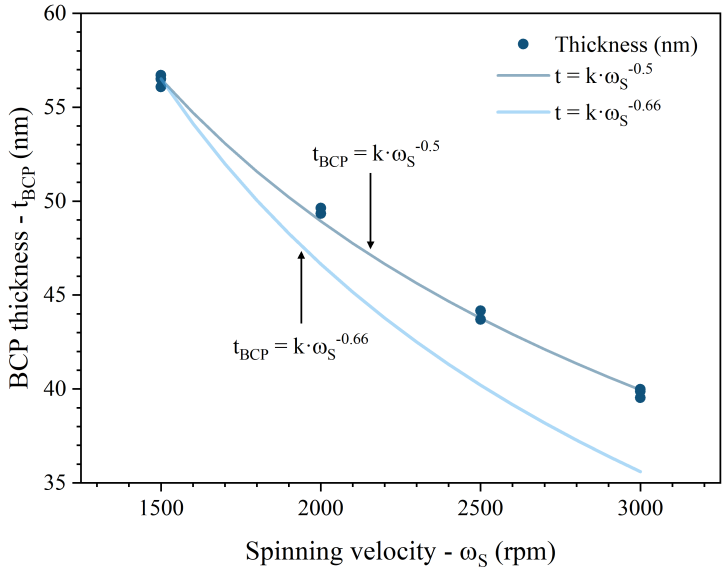


Figure 5.2: Thickness of the deposited BCP versus spinning velocity. The values of thickness of the 2% wt BCPs dissolved in PGMEA were measured in a Horiba Jobin Ivon/AutoSE Ellipsometer. The two curves correspond to $t_{BCP} = k{\cdot}\omega_s^{-b}$ with b = 0.5 and 0.66.

5.1.1 Block copolymer blends

The strategy of blending BCPs was used in this work to obtain patterns with more optimal sizes in terms of zT enhancement. Decreasing the period of the pattern leads to a higher scattering rate of phonons but also to a possible increase in the scattering of electrons. Therefore, the Si neck (width of Si between holes) should be maintained to be larger than the mean free path of electrons ($\simeq$ 13.5 nm for hot electrons in a Boron doped Si [161]). This is not especially important in the case of free surface lamellar patterns as they don't have continuity from side to side and complete pattern transfer onto the Si layer cannot be done. In the cylindrical ones, instead, the PS matrix is continuous and complete etching of the Si layer can be achieved. This means that patterning Si using BCPs with periods $<$ 40 nm (neck sizes $<$ 20 nm) could highly degrade the electrical conductivity of the Si film. For these reasons, lamellar patterns with periods between 22 and 37 nm were assembled, while blends of cylindrical BCPs were explored to obtain periods above 40 nm.

The results of the blending of lamellar BCPs can be seen in Figure 5.3. For these BCPs the blending procedure is simple and only involves mixing solutions of different BCPs following Equation 1.29. The exact fraction of each BCP used for the blends, together with the expected and measured periods are indicated in Table 5.2. In all cases, the experimental period agrees with the calculated one when the standard deviation is taken into account. The measurements of the periods were done with a custom Python program that used 2D Fourier transforms to analyze the SEM images of the different BCPs. The great homogeneity observed in the SEM images and the absence of miscibility problems are expected in these blends due to their similar periods ($\alpha_{BCP} < 1.68$). Also, the same brush layer (NL2 - R60) was used in all cases.

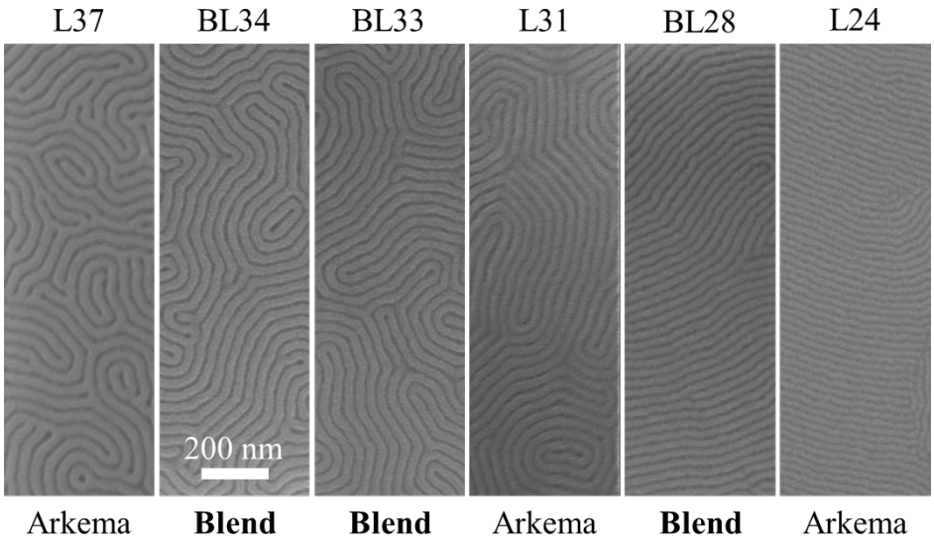


Figure 5.3: SEM images of self-assembled BCP from Arkema and intermediate blends (denoted as BL).

Table 5.2: Theoretical and experimental periods and diameters of several lamellar and cylindrical BCPs used in this thesis.

Block copolymer	Theor. period (nm)	Exp. period (nm)	Exp. diameter (nm)
L37	37	36.51 ± 1.91	-
L31 (50%) - L37 (50%)	34	33.19 ± 1.91	-
L24 (31%) - L37 (69%)	32.97	31.57 ± 1.66	-
L31	31	31.31 ± 2.19	-
L22 (60%) - L37 (40%)	28	27.78 ± 1.86	-
L24	24	22.82 ± 0.78	-
L22	22	22.14 ± 1.43	-
C35	35	34.64 ± 1.28	14.26 ± 1.29
PS (10%) - C35 (90%)	-	37.48 ± 1.62	16.44 ± 2.18
PS (15%) - C35 (85%)	-	40.28 ± 1.39	16.55 ± 1.12
C35 (90%) - C80 (10%)	39.5	40.75 ± 1.93	18.71 ± 1.55
C35 (75%) - C80 (25%)	46.25	45.98 ± 1.46	21.22 ± 1.46
C35 (50%) - C80 (50%)	57.5	58.02 ± 4.71	25.36 ± 3.49

On the other hand, the blends of cylindrical BCPs are more problematic because they involve higher α_{BCP} (~ 2.3) or BCP-homopolymer mixtures. The first set of blends studied were BCP-homopolymer mixtures. The purpose of these blends is to mix the PS homopolymer with the cylindrical BCP in order to enlarge the neck size between the PMMA cylinders without altering their diameters. This should subsequently translate into a larger neck size in Si, which is essential for the C35 BCP, as its neck size is below 20 nm after self-assembly. However, some problems arise when introducing more quantity of one of the polymers in the blends, as the original ~ 7 to 3 proportion between PS and PMMA is altered. As explained in Section 1.5, BCP pattern formation depends on the volume fraction of both polymers. In these types of BCP-homopolymer blends the volume fraction is shifted to the right in Figure 1.11, which could lead the system to be in the frontier between cylindrical and spherical phases. This idea is used in some contexts to improve the pattern formation in under-optimized BCPs, but adding PS in an already optimized BCP like C35 could introduce more drawbacks than advantages. The results of two blends with different amounts of PS (10 and 15 % in weight fraction) and C35 BCP can be seen in Figure 5.4.

In the case of 10% PS, a pattern with a predominant cylindrical phase is observed. However, some areas (dark gray in Figure 5.4) show no holes in the surface of the BCP film. This could either indicate the formation of a spherical phase or orientation issues in the cylinders. Also, the cylindrical domains show misalignment, thus not looking completely vertical as in the pristine C35 BCP. Regarding the period, an increase of $\sim$ 3 nm was measured in these samples, while the diameter is ~ 2 nm bigger than that of

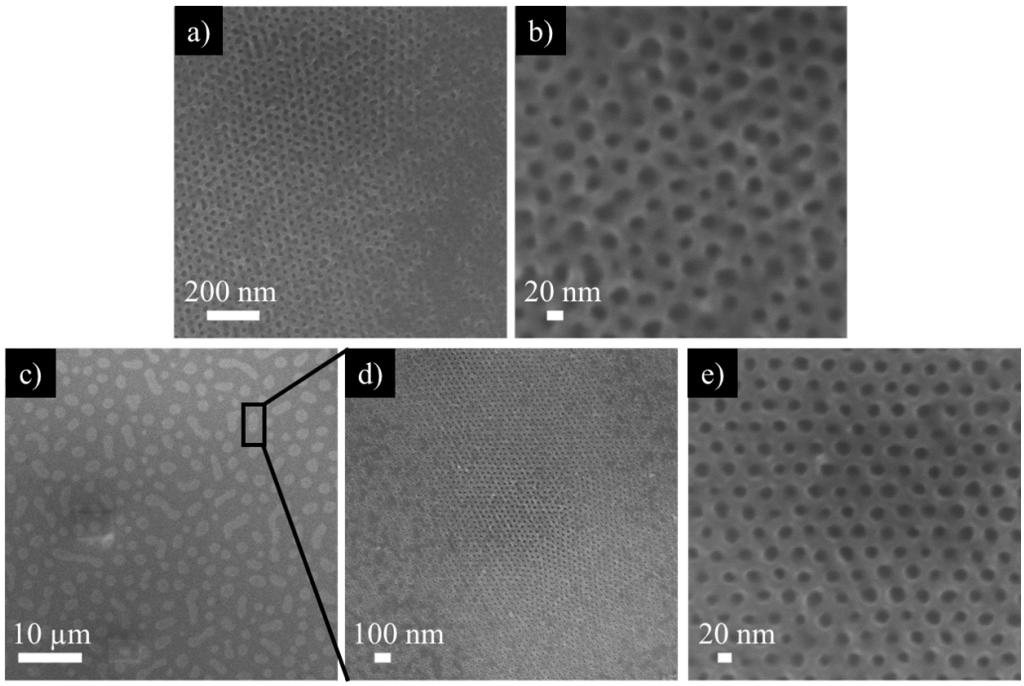


Figure 5.4: SEM images of two different PS-C35 homopolymer-BCP blends: a) PS(10%)-C35(90%) and b) PS(15%)-C35(85%). As the PS weight fraction increases so does the period of the pattern. This also introduces orientation defects in the sample.

C35. This indicates that the period grows at a higher rate. However, it is important to note that the measurement of the diameter had higher error, since the apparent diameter of a tilted cylinder appears larger than that of a vertical one when observed from the top view. Regarding the blend with 15% PS, a similar trend is observed. The sample is divided in two alternating regions that occupy $\sim$ 50% of the area each. Similarly to the 10% PS case, the dark gray regions show an absence of vertical alignment. In the well oriented areas the pattern has also some misalignment. As for the period and diameter size, the period is growing at a higher rate. In this sample, a period of $\sim$ 40 nm was measured, while the diameter is $\sim$ 16 nm. This means that the diameter only grows $\sim$ 2 nm, whereas the period increases by $\sim$ 6 nm compared to pristine C35. These two blends demonstrate that, by adding PS, the period of the mixture can be tailored while maintaining a relatively stable diameter. However, the expected miss-orientation and phase inconsistencies appear at the same time, making these kind of blends difficult to be applied for Si nanostructuration if done with a BCP that already has proper morphology (i.e. with pristine BCPs that form perfectly oriented cylinders).

The second type of blends were BCP-BCP mixtures combining C80 and C35, which have significantly different diameters ($\alpha_{BCP} > 2$). This is aggravated by the fact that the miscibility of two BCPs significantly depends on the volume fraction of the larger one, which in this case was always below 50 %, as we aimed to avoid periods bigger than 60 nm. Three blends with different BCP weight fractions were studied (10%-90%, 25%-75% and

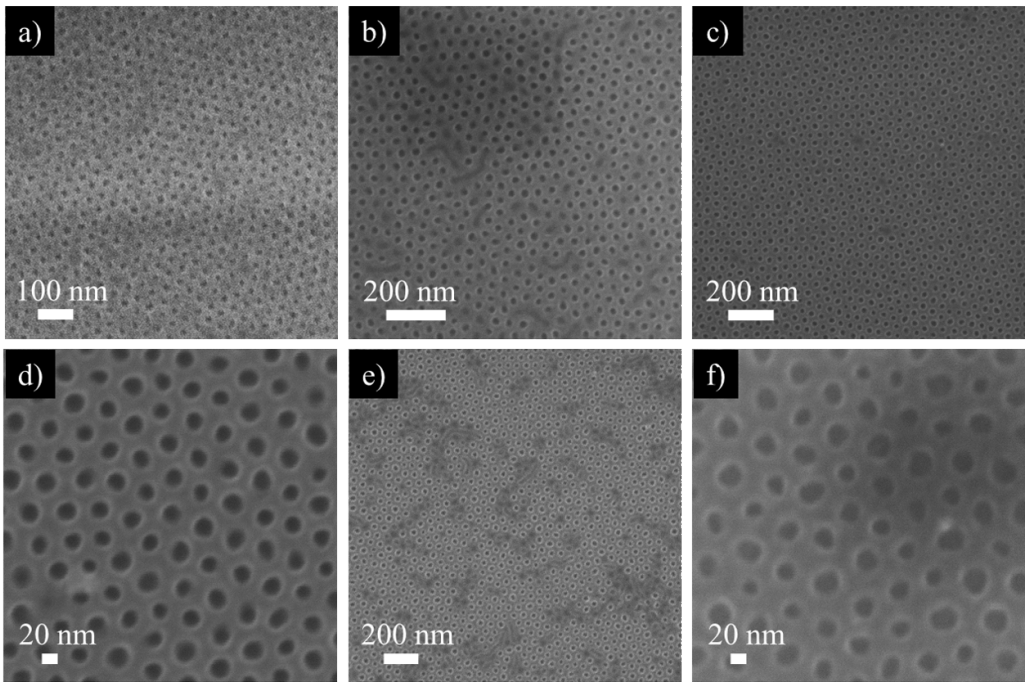


Figure 5.5: SEM images of three different C80-C35 BCP-BCP blends: a) NL1 and C80(10%)-C35(90%), b) NL1 and C80(25%)-C35(75%), c) and d) NL18 and C80(25%)-C35(75%), e) and f) NL18 and C80(50%)-C35(50%). As the C80 weight fraction increases so do the period and the diameter of the pattern. Also, higher variability of the diameter is observed as the C80 weight fraction increases.

50%-50% of C80 and C35, respectively), the results of which can be seen in Figure 5.5. Nonetheless, complete miscibility of both BCPs is observed even when only 10% of C80 is introduced in the mixture. Regarding pattern orientation, the 10-90 pattern is uniformly vertical across the sample using the same C35 brush layer (NL1). In the case of 25-75, some misalignment of the cylinders is observed, which was later corrected changing the brush layer to NL18. With this brush, the pattern orientation becomes perfect across the sample. In the 50-50 blend, even if NL18 is used, some miss-orientations can appear due to the higher proportion of C80. Therefore, it is more challenging to form a completely vertical pattern because the thermally driven diffusion of the C80 molecules is slower. Despite this, the vast majority of the sample is well aligned with this blend. Moreover, a clear trend is observed on the diameter size and uniformity. As the fraction of the C80 BCP increases, both the diameter and pattern irregularities increase. The 10-90 shows a hexagonal pattern with constant pore diameter. The 25-75 shows greater dispersion in the pore diameter and a slight distortion from the hexagonal arrangement, whereas the 50-50 blend further accentuates this distortion. In this last, pore shape ranges from circular to elliptical, as expected from the difference of the length of both BCPs (see Section 1.5.1). All three periods and diameters measured match perfectly the calculated ones, and higher standard deviations are observed for the 50-50 case (see Table 5.2). For the self-assembly of these blends, the furnace temperature was 230°C, the same as that used for the C35. These results demonstrate that blends offer a more energy-efficient way to obtain larger periods by having one low-weight BCP that can drive the pattern formation due to its high mobility under lower temperatures. Obviously, there is a disadvantage regarding the pattern and diameter inhomogeneities with these type of blends but, in the scope of this work, this variability might be beneficial for a more enhanced phonon scattering.

Among the presented BCPs, L28, L37, C35(25%)-C80(75%) and C35(50%)-C80(50%) were the most extensively used for thermoelectric study, with special attention to the C35(50%)-C80(50%) BCP. This last is the most appealing since it allows complete pattern transfer into Si while forecasting good thermal scattering enhancement and low electrical conductivity degradation (neck size between 20-30 nm). Nonetheless, optimization of the pattern transfer was also done for the rest of BCPs.

5.2 Pattern transfer on Silicon

The most critical step in the nanostructuring of the Si film is transferring the BCP pattern into it. Typically, PMMA is selectively removed to leave a PS mask that can later be used to etch the underlying Si layer. This is the procedure that was followed in this work.

5.2.1 PMMA etching

Two routes are available to selectively etch PMMA without completely removing PS: dry and wet etching. The first involves a RIE, but the combination of gases must be carefully optimized to obtain enough etching selectivity. Examples of these are: oxygen [162], Co-Ar [163], O_2/CHF_3 [164], Ar [165] and Ar/O_2 [166]. The availability of gases in our clean room offered oxygen, Ar and the combination of both as possible candidates. Since the etching selectivity towards pure oxygen is low in these polymers [167], Ar was selected as the main etchant for PMMA. However, enough oxygen presence in the samples is needed during the etching process to ensure a constant etching rate as the depth increases. Otherwise, the etching velocity of the Ar bombardment may diminish,

Table 5.3: Optimized parameters for the PMMA etching in an ICP type RIE machine (Alcatel AMS-110 DE).

T (C)	P (Pa)	Ar (sccm)	O2 (sccm)	RF chamber (W)	RF chuck (W)
20	1.3	200	10	200	5

losing some of the selectivity with PS. For this reason, a small fraction of oxygen gas was also introduced in the recipe, with the aim of obtaining a constant in-depth etching rate of PMMA. The selectivity of this etching arises from the fact that the primary parameter affecting the etch rate of an organic material under ion bombardment is the carbon content of its molecules [168]. Since PS has more carbon content, this justifies its higher resistance towards this etching. Also, the presence of an aromatic ring in the PS increases its hardness [169].

The optimal etching parameters for L37 are listed in Table 5.3. A 20:1 ratio between Ar and O_2 ensures a constant etching rate of PMMA. Given the high selectivity between the two blocks, the chuck power (i.e. the RF used to force the directionality of the ion bombardment towards the sample) can be kept low, as there is no need for a highly anisotropic etching during this step. The results of PMMA etching with this recipe can be seen in Figure 5.6. Accurate measurements of the remaining PMMA and PS thickness

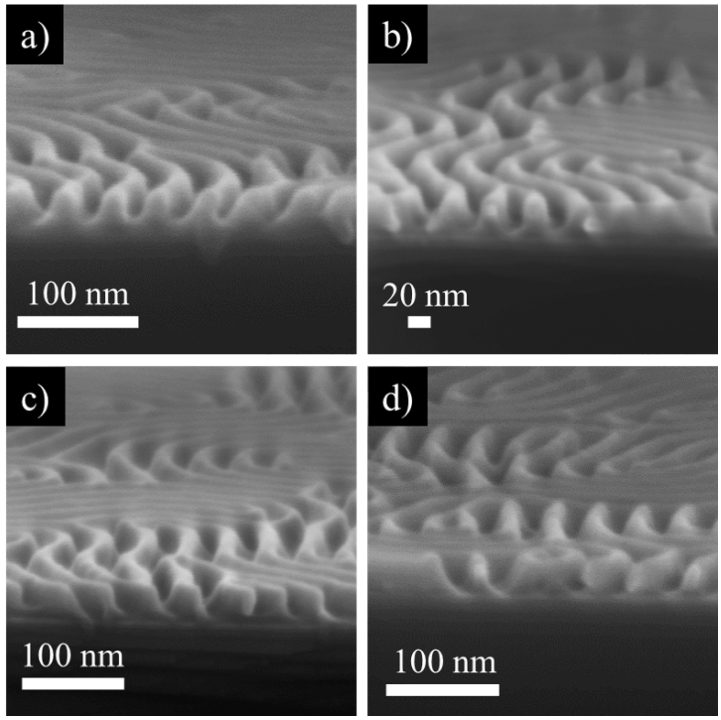


Figure 5.6: Tilted cross-section SEM images of the Ar/O_2 RIE of L37 BCP samples: a) 41s of RIE, b) 51s of RIE, c) 57s of RIE and d) 1min 11s of RIE. Above 51 s of attack the PMMA has completely been etched but the brush elimination is difficult to characterize. The initial thickness of the sample is 50 nm.

as a function of the etching time, conducted with cross-section SEM images, are plotted in Figure 5.7a and b. The etching of PMMA with this recipe is consistent over time and has an etching rate of ~ 0.95 nm/s. PS also shows a constant etching rate, with a value of ~ 0.42 nm/s. These lead to a selectivity of ~ 2.3. Since this value is high, PMMA can be completely etched with a RIE > 51 s while leaving > 25 nm of PS to be used later as the mask for the Si pattern transfer (if the initial BCP thickness is ~ 50 nm). However, the sidewall profile of the PS lamellas after etching is not perfectly vertical.

The etching of the brush layer, instead, is more difficult to characterize. Since its thickness is $\sim$ 8-9 nm, changes in the nanometer scale are difficult to measure using SEM images. An approximate etching rate was calculated by plotting the brush thickness against time once PMMA was completely removed (see Figure 5.7c). Taking into account the significant errors assumed in these measurements, an etching rate of $\sim 0.32 \pm 0.08$

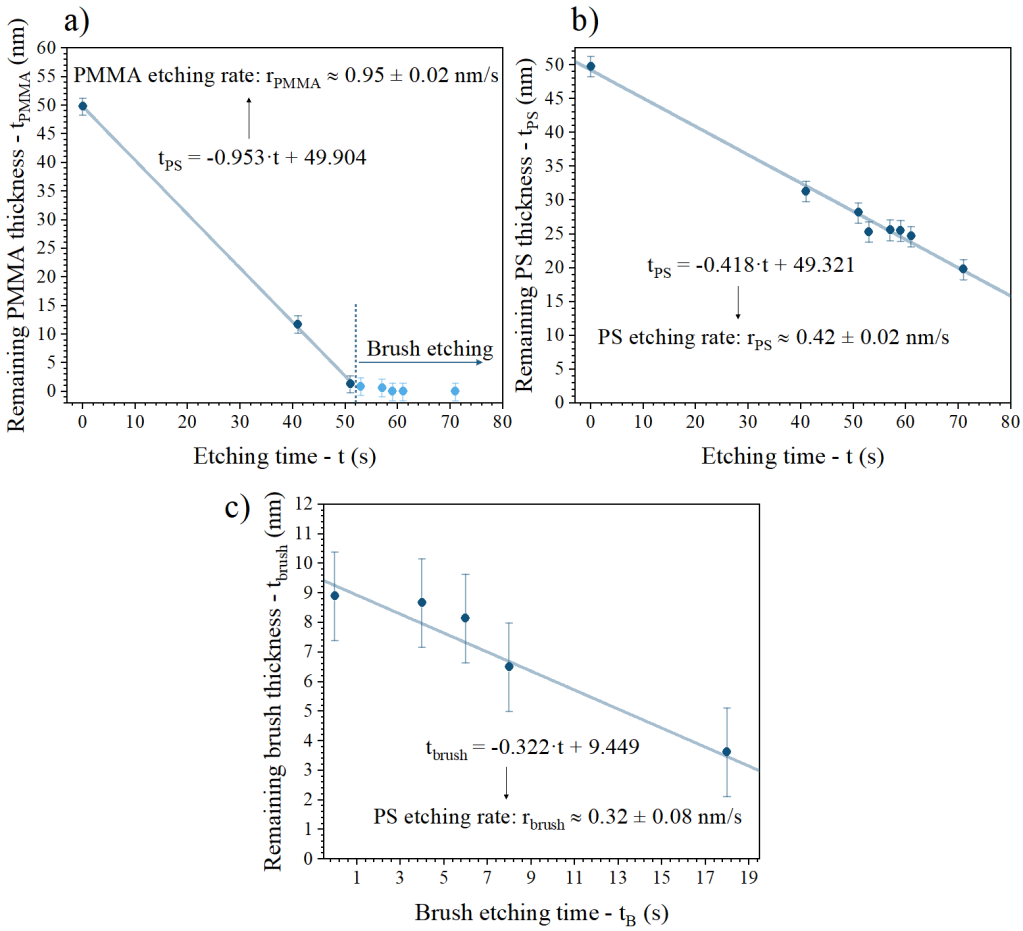


Figure 5.7: Plots of the measured remaining a) PMMA, b) PS and c) brush thickness as a function of the attack time with the Ar/O_2 RIE. The linear fits indicate a constant $\sim$ ~ 0.95 nm/s, 0.42 nm/s and ~ 0.32 nm/s etching rate, respectively. The measurement of the brush layer made with the SEM is complicated, meaning that this etching rate is only a broad approximation due to the high error in the characterized thicknesses.

nm/s was obtained. This is in good agreement with the ~ 0.42 nm/s etching rate found for the PS. During this step, the exposed PMMA should be rapidly removed, so the measured etch rate mainly reflects PS etching in the brush. In principle, complete elimination of the brush would be the desired outcome to ensure the pattern transfer onto the underlying Si. However, increasing etching times to fully eliminate the brush will lead to PS etching on the BCP, diminishing the PS mask thickness by $\sim$ 8-9 nm. This could complicate the Si etching step (PS would have t $\leq$ 20 nm). For these reasons, a 55 s attack was designated as the optimal time, leaving $\sim$ 80% of the brush. The higher Si-PS etching selectivity, that will be discussed in the next section, also justifies performing most of the brush removal during the Si etching step.

After optimizing the RIE parameters for L37, these were transferred to the rest of BCPs. However, when going towards BCPs with smaller periods, the etching velocity diminishes. This kind of behavior is expected and well known in etching processes, where the size and density of the features affect the etching rates (i.e. microloading effect [170]). The remaining BCPs were all compatible with this RIE recipe, although the process times were adjusted in each case according to the pattern size. In the case of C35, the results of the etching are shown in Figure 5.8. PMMA is completely eliminated, leaving $\sim$ 13 nm of PS mask. The challenge with this type of dry etching in cylindrical BCPs is that the BCP film is already thin prior to etching. Since the etching selectivity is ~ 2.3, PS is always reduced in the process, thinning even more the final mask. From the point of view of the thickness of the deposited BCP, there is no adjustment that can be done to increase this value while maintaining correct orientation of the cylinders, as shown in Section 5.1. Thus, the dry route was discarded for cylindrical BCPs and alternative wet etching routes were explored.

The main wet routes to etch PMMA in PS-b-PMMA involve dissolving PMMA in acetic acid or isopropanol (IPA). However, because PMMA is covalently bonded to PS, prior exposure of the BCP to ultraviolet (UV) light, e-beam, X-ray, or proton-beam irradiation is required to break these bonds and degrade the PMMA, thereby facilitating its solubility [137], [171], [172], [173]. UV exposure was selected in this work because it allows the simultaneous irradiation of the entire chip or wafer, thereby reducing processing time. This process is governed by PMMA degradation caused by chain scission of its

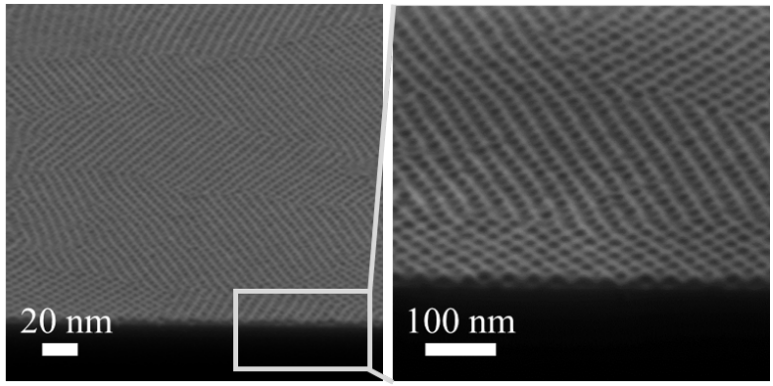


Figure 5.8: SEM images of the Ar/O_2 RIE of C35 BCP samples with 20 nm of film thickness. PMMA is completely removed with a 36 s RIE attack but a thin $\sim$ 13 nm PS mask is left after the process.

covalent bonds due to UV irradiation at a specific wavelength [174]. This, at the same time, hardens the PS chains by means of cross-linking, further reducing its solubility in organic solvents. However, STEM studies have shown that etching PMMA completely using a wet route is impossible, since some polymer remains in the walls of the PS [175], either embedded in the PS matrix or adding a small roughness to the wall profile. Since this effect is almost negligible due to the small amount of remaining PMMA, which will also be rapidly etched by the Si RIE, this route predicts good removal of PMMA while leaving the PS mask untouched.

Figure 5.9 shows the results of wet etching optimization. While the duration of the etching in acetic acid is not critical, the time of exposure to UV light is of utmost importance and requires a precise duration to avoid the degradation of the BCP. In our case, an EPROMs Spectroline-3300A with 18.5 mW/cm^2 irradiation intensity and λ = 254 nm was used. For the calculations of the dose needed to achieve PMMA degradation, the results reported by *A. Gharbi et al.* [137] were used, together with the PMMA light absorption data to adjust the dose to the employed λ [174]. Then, a range of exposure times was tested. From the trend observed in the SEM images of Figure 5.9, where the UV exposure time is reduced from 5 min 30 s to 3 min 50 s, it is evident that overexposure can damage the BCP. As the exposure time is reduced, the pattern becomes more defined, and at 3 min 50 s no damage is observed on the sample. Simultaneously, this exposure

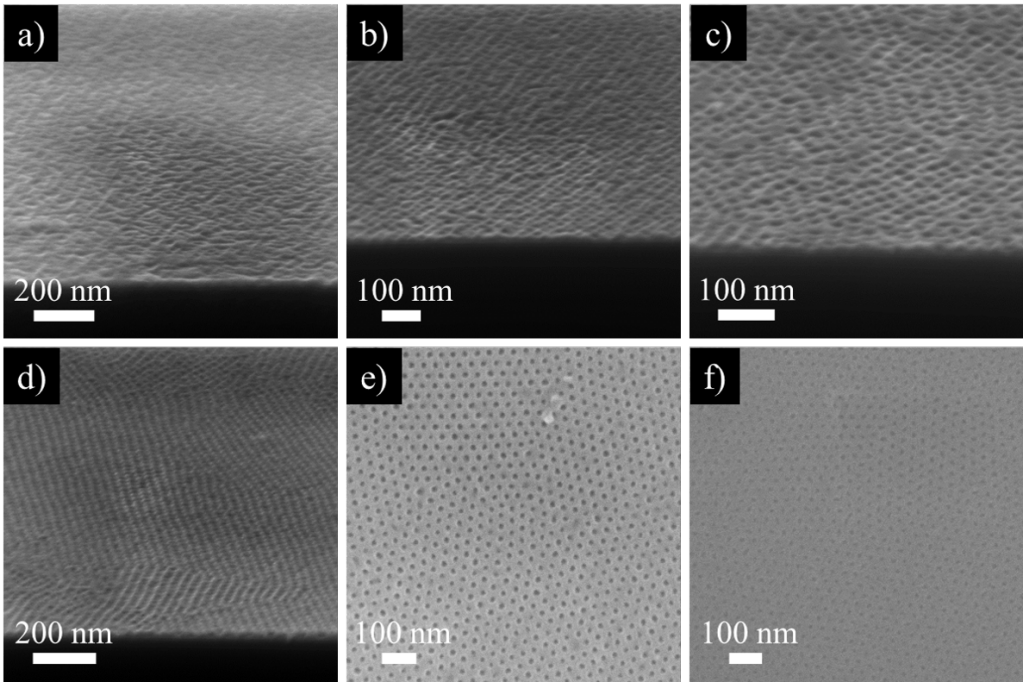


Figure 5.9: SEM images of the PMMA wet etching route of C35 BCPs: a) 5min 30s UV - 8min acetic acid (AA), b) 4min 15s UV - 8min acetic acid (AA), c) 4min 3s UV - 8min acetic acid (AA), d) and e) 3min 50s UV - 8min acetic acid (AA), f) 3min 50s UV - 8min IPA. The optimal exposure time is 3 min 50 s using a λ = 254 nm UV light with an irradiation intensity of 18.5 mW/cm^2. Acetic acid completely dissolves PMMA while IPA is not capable. After this process the PS remains untouched.

ensures complete degradation of the PMMA and its subsequent dissolution in acetic acid. If the exposure is further reduced, PMMA is not completely etched. As a second route, PMMA dissolution was tested in IPA under the same exposure conditions. In this case, PMMA is not etched (see Figure 5.9f, where the low contrast indicates that the PMMA has not been removed). These results demonstrate a wet etching procedure to eliminate PMMA without affecting the PS using $\lambda = 254$ nm UV light. At this stage, the PMMA is etched, but the brush layer remains beneath the pattern. For this purpose, a subsequent 7 s etching step using the Ar/O_2 RIE recipe was performed to partially etch the brush layer, which was later completely removed during the Si RIE process.

Regarding the application of the wet etching procedure to the lamellas, surface tension during the subsequent drying step caused their collapse, even when their aspect ratio was reduced to thicknesses of approximately 30 nm. Since this kind of PS mask thickness can be obtained with RIE using an initial BCP of 50 nm, dry etching remains the optimal procedure to obtain defect-free > 25 nm thick PS masks with lamellar BCPs.

5.2.2 Silicon etching

The final step of the pattern transfer process consists of using the PS mask to etch the underlying Si film. The possibilities in this topic are wide, as there are a lot of well known dry [176], [177] and wet [178] etching routes for Si in the micro-scale. On the side of dry routes, there are several possibilities, with the Bosch process being the most standard technique in the field of micro-machining [179]. However, this mechanism is well established for micro-scale etching but faces significant problems at the nanoscale due to the scalloping effect. For these reasons, the so-called mixed Bosch process is the most appealing, as it shows better compatibility with nano-structures [180], [181]. The etching chemistry is based on two different gases that act as passivating (C_4F_8) and etching (SF_6) species. In this process, instead of pulsing both gases in sequential steps, both are introduced simultaneously, resulting in simultaneous passivation and etching. For this process to be reliable, an optimal ratio between the two species, together with a precise chuck and plasma power, must be obtained to ensure that the passivating molecules do not block the Si etching. On the other hand, etching rates higher than passivation rates could lead to isotropic behavior. Finally, another limitation of the pattern transfer should be noted. Usually, intermediate fabrication steps are added to successfully transfer the pattern into Si films [80], [89]. In our case, the pattern transfer into Si is performed directly using the PS mask, without intermediate steps. This simplifies the overall procedure but narrows the window of optimal etching conditions, as the selectivity between Si and PS is limited.

The optimization of the pattern transfer onto Si films using the mixed Bosch process is shown in Figure 5.10. The initial conditions were: chamber power of 1200 W, same gas flow of both passivating and etching species, and chuck power of 10 W. The chamber power was selected to avoid the ionization of an excessive number of passivating species, since there is a power threshold beyond which their increase may hinder Si etching [182]. The chuck power was initially kept low to minimize PS etching rate during the bombardment. With these parameters the profile of the attack is highly isotropic and limited to depths < 30 nm. Beyond these depths, the PS layer peels off due to the underetching of the underlying Si. Increasing only the chuck power kept the isotropy nearly unchanged, whereas increasing the amount of passivating species resulted in a lower etch rate. Therefore, the optimization required simultaneous adjustment of both parameters by increasing the C_4F_8 flow and the chuck power. The results of Figure 5.10 show that a

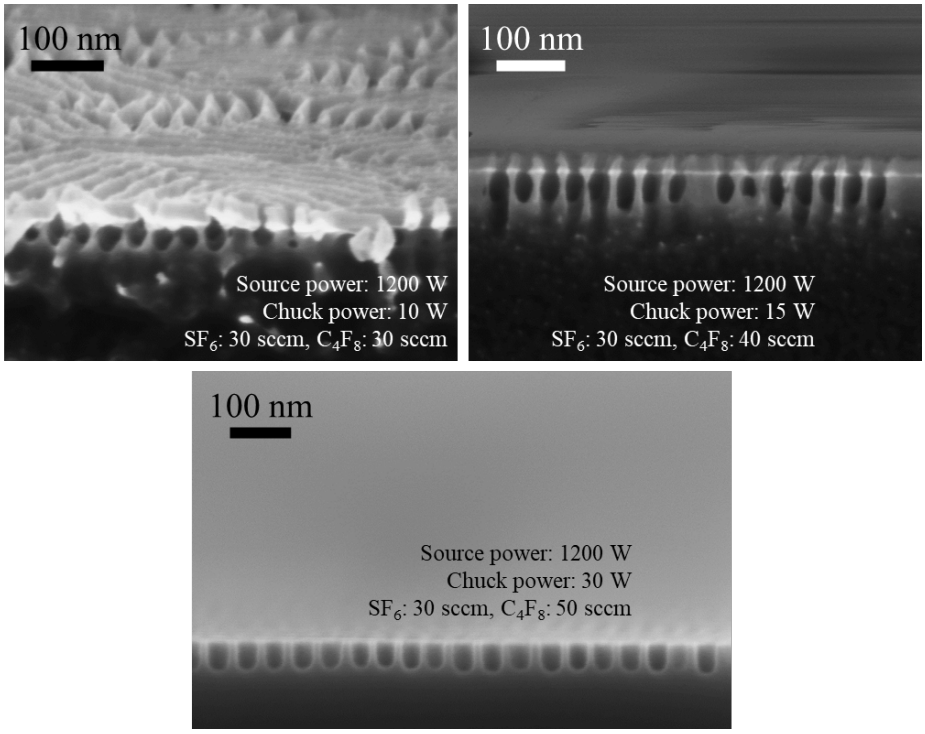


Figure 5.10: Optimization of the mixed Bosch process RIE to obtain a completely anisotropic attack. By increasing the amount of passivating gas (C_4F_8) in the chamber and, at the same time, elevating the chuck power to force higher directionality a perfect vertical wall can be obtained.

Table 5.4: Optimized parameters for Si etching in an ICP type RIE (Alcatel AMS-110 DE).

T (C)	P (Pa)	SF_6 (sccm)	C_4F_8 (sccm)	RF chamber (W)	RF chuck (W)
20	2	30	50	1200	30

perfectly vertical wall profile was obtained using a 3 to 5 ratio of the gas flows (SF_6 and C_4F_8, respectively) and a chuck power of 30 W. The remaining parameters are the same as those in the first recipe. The complete etching conditions can be seen in Table 5.4.

This optimization was performed using the L37 BCP. Then, the pattern transfer of SOI samples was studied with the same BCPs, the results of which are shown in Figure 5.11. As expected, longer RIE durations result in greater etched depths and larger hole diameters. Plots of the Si etched depth and remaining PS thickness as a function of the etching time are shown in Figure 5.12a and b. In the case of the Si depth, the fitting shows a first $\sim$ 7 s interval during which no etching occurs. This initial stage corresponds to both the first 2-3 s required for chamber power stabilization and to the time needed to remove the remaining $\sim$ 6 nm of brush layer still present in the sample ($\sim$ 2-3 nm of brush were previously etched during PMMA removal). After, the etching rate is constant with a value of $\sim$ 4.3 nm/s. Regarding the PS mask, the results show a constant etch

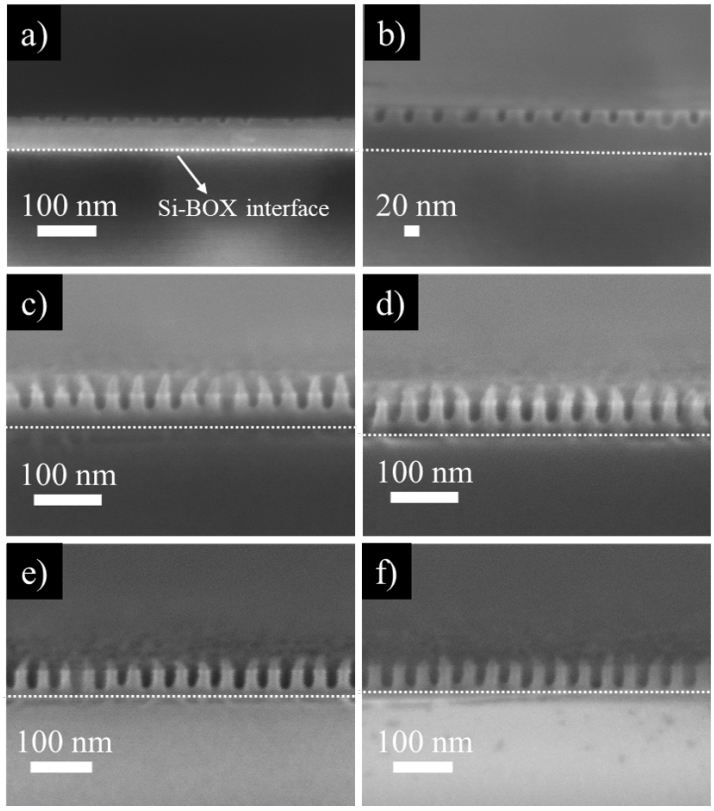


Figure 5.11: SEM images of SOI samples with lamellar BCPs etched with the mixed Bosch process as a function of the etching time: a) 10s of RIE, b) and c) 12s of RIE without and with the PS mask on top, d) 14s of RIE, e) 16s of RIE, f) 18s of RIE. The $\sim$ 25 nm thick PS masks withstand the Si RIE, enabling the complete etching of a 50 nm thick Si film.

rate of $\sim$ 0.82 nm/s. These values lead to a Si-to-PS selectivity of $\sim$ 5.3. It's because of this high selectivity that it's more efficient to end the brush etching in this step.

Besides this, a decrease in neck size is observed with increasing etching time. This can be attributed to the fact that the PS mask does not have a perfectly vertical profile, as shown in the previous section, leading to a gradual widening of the PS features as the thinner regions are etched by RIE. Minor lateral etching of Si could also account for this behavior. However, the widening of the holes eventually reaches a limit. The measurements of the Si neck size with time in L37 patterns are shown in Figure 5.12c. The minimal neck size is $\sim$ 18 nm, and this value is reached after $\sim$ 7 s of Si attack. As from this point on the neck reaches a saturation, this is the final neck size achievable with L37. Further etching will maintain the neck as long as PS is not completely eliminated.

Regarding cylindrical BCPs, the same optimized procedure was used for pattern transfer to study its compatibility. SEM images showing examples of the obtained etchings can be seen in Figure 5.13. Figure 5.13c, d, e and f are the optimal time conditions to achieve etching $>$ 50 nm while preserving the PS mask and maintaining a reasonable neck size in the two most relevant cylindrical blends (C35(75%)-C80(25%) and C35(50%)-

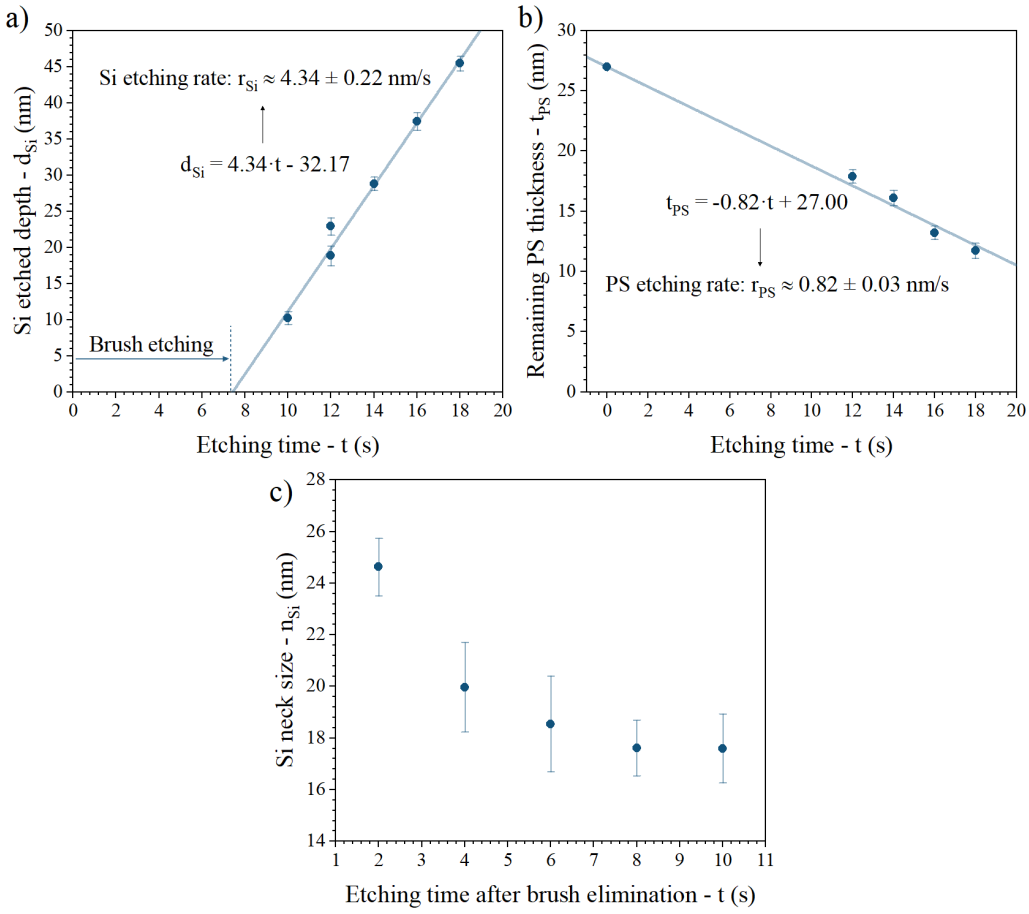


Figure 5.12: Plots of: a) Si etched depth, b) remaining PS and, c) Si neck size versus RIE time with the mixed Bosch RIE in L37 BCPs. The linear fits indicate $\sim$ 4.3 nm/s and $\sim$ 0.82 nm/s etching rates, respectively. The first $\sim$ 7 s of RIE correspond to the time needed to etch the remaining brush layer on the sample. As for the neck size, saturation is reached $>$ 7 s of Si attack, giving a final neck of $\sim$ 18 nm when complete pattern transfer is done.

C80(50%)). Similarly to what was observed in the PMMA elimination by dry etching, cylindrical patterns have a lower etch rate compared to lamellar ones due to the smaller size of the holes. Furthermore, as the period of the cylindrical BCP is smaller, the etching time should be increased to obtain the same depth results. The etched depths measured on the C35(50%)-C80(50%) BCP as a function of the RIE duration are shown in Figure 5.14a. Again, the fitting indicates an initial time range during which Si is not attacked, corresponding to the elimination of the remaining brush. However, this time is $\sim$ 2-3 s shorter than that of L37. The 7s Ar/O_2 RIE performed on the cylindrical samples after the PMMA wet removal with UV/AA is the reason behind this difference (i.e. the brush layer is further etched prior to the Si RIE). As for the Si etching rate, the velocity is $\sim$ 20 % slower compared to that of L37 ($\sim$ 3.4 nm/s). Taking into account that the PS mask is etched at the same velocity, the selectivity in these patterns is smaller ($\sim$ 4.3). The

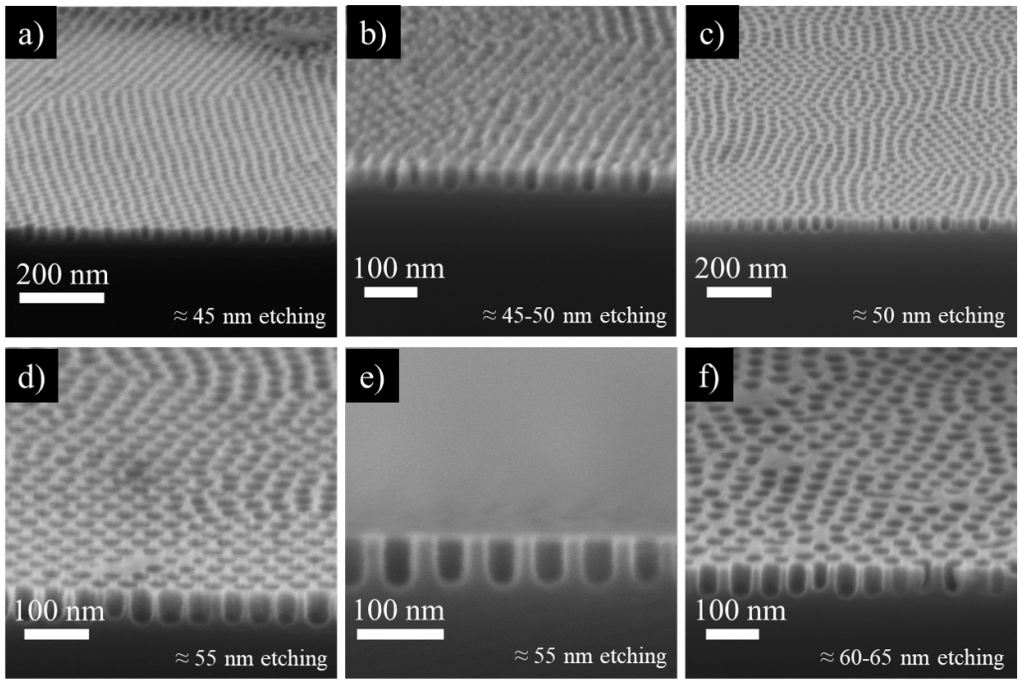


Figure 5.13: SEM images of the pattern transfer of cylindrical BCPs into Si: a) C35, 18s of RIE, b) C35(90%)-C80(10%), 19s of RIE, c) C35(75%)-C80(25%), 19s of RIE, d) C35(75%)-C80(25%), 21s of RIE, e) C35(50%)-C80(50%), 20s of RIE, f) C35(50%)-C80(50%), 22s of RIE. In C35(75%)-C80(25%) and C35(50%)-C80(50%) BCPs, the neck sizes are compatible with low electrical conductivity degradation. Due to neck size limitations, all BCPs with periods < 45 nm were discarded for the nanostructuring of Si films.

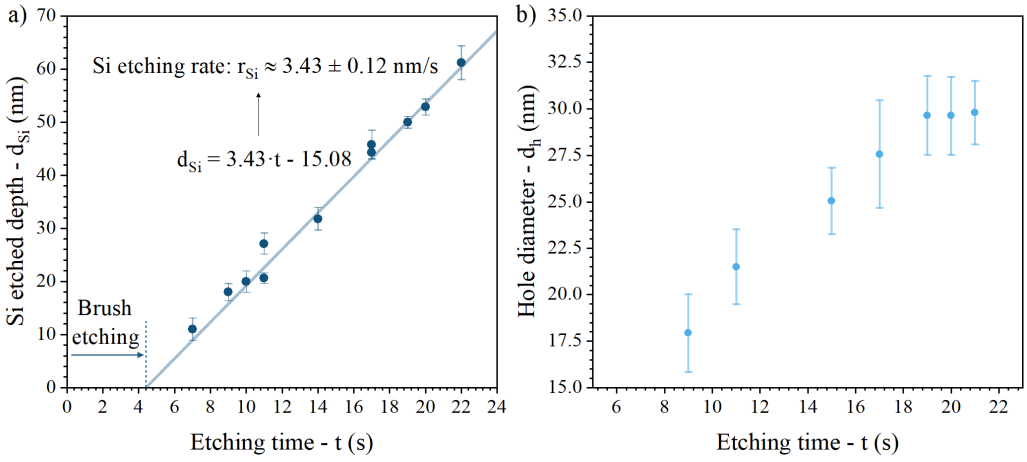


Figure 5.14: Plot of the: a) measured etched depth and, b) hole diameter, as a function of the attack time with the mixed Bosch RIE in cylindrical C35(50%)-C80(50%) BCPs. The linear fit indicates a ~ 3.4 nm/s etching rate. The first ~ 4 s that show no attack in the Si film correspond to the time needed to etch the brush layer remaining on the sample. Saturation in the hole size is obtained around 30 nm.

saturation of the hole diameter reaches a value of $\sim$ 30 nm in these C35(50%)-C80(50%) BCPs, which is obtained after etching Si for more than $\sim$ 16-18 s (see Figure 5.14b).

Figure 5.13a and b serve to illustrate the depth limitations of the pattern transfer observed on C35 and C35(90%)-C80(10%) BCPs. C35 is limited to $\sim$ 45 nm in depth because hole widening eventually disrupts the film continuity when RIE durations exceed 19 s. A 45 nm depth, however, is not compatible with thermoelectric applications due to its $<$ 10 nm Si neck size, which will highly degrade the electrical properties of the film. The blends with C80 allow $>$ 50 nm etching but only two of them have neck size parameters in the desired range. The C35(90%)-C80(10%) BCP shows the same neck size problems observed on C35. Thus, C35(75%)-C80(25%) and C35(50%)-C80(50%) BCPs were selected as the optimal geometries for the nanostructuring of 50 nm thick Si films. Neck size problems only appear on C35(75%)-C80(25%) after etching more than 55 nm of Si, while C35(50%)-C80(50%) shows good neck sizes even after $>$ 65 nm of etching.

Example SEM images of the pattern transfer for the optimal BCPs used in thermoelectric applications are shown in Figure 5.15 in 50-nm and 17-nm SOI thick films. Free-surface lamellar patterns are only partially transferred in the SOI layer to maintain electrical continuity across the film. Cylindrical patterns, on the other hand, allow both partial and complete etching of the Si film. Interestingly, the u-shaped etch profile observed during the RIE ends once the buried oxide layer is reached, achieving perfectly

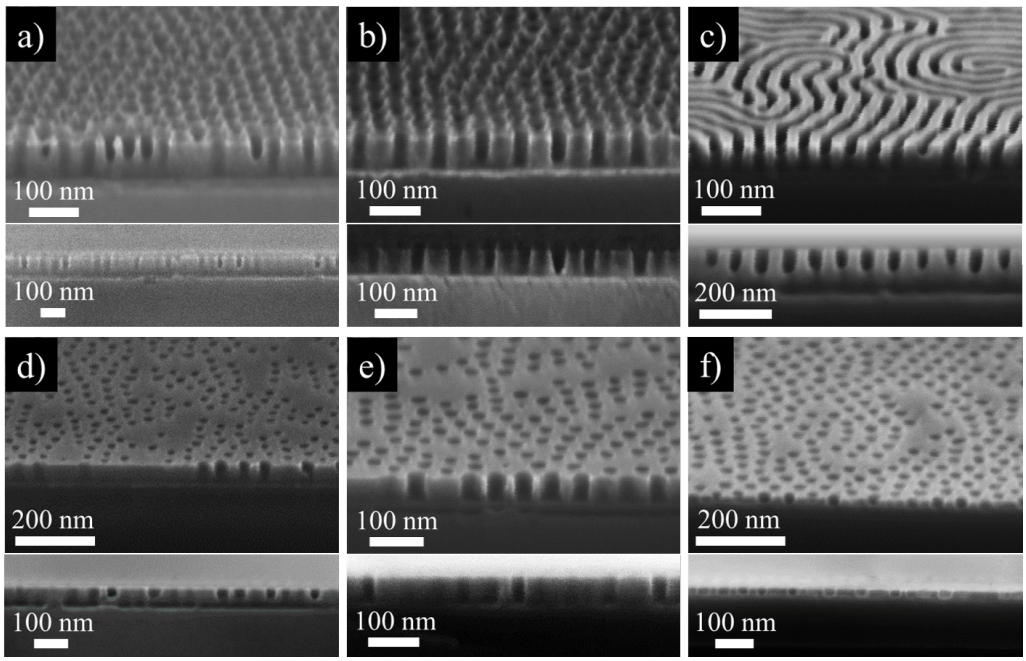


Figure 5.15: Tilted and cross-section SEM images of the pattern transfer of the optimal BCPs in the final 50 nm thick SOI samples: a) 50-nm SOI with partial etching using C35(75%)-C80(25%), b) 50-nm SOI with complete etching using C35(75%)-C80(25%), c) 50-nm SOI with partial etching using L37, d) 50-nm SOI with partial etching using C35(50%)-C80(50%), e) 50-nm SOI with complete etching using C35(50%)-C80(50%), f) 17-nm SOI with complete etching using C35(50%)-C80(50%). Perfectly vertical profile is obtained in the complete pattern transfer.

vertical walls in the holes. The SEM images of the C35(75%)-C80(25%) in Figure 5.15 show the appearance of the remaining PS mask on top of the Si film after the RIE. The mask withstands the full pattern transfer procedure, indicating that the thicknesses used during all the fabrication steps are adequate. The final step involves removing the PS mask, leaving only the nanostructured Si film. This was done by means of an oxygen plasma with the following parameters: 600 sccm of O_2 and 600 W of chamber power for 5 min.

5.3 Doping of silicon thin films with Spin on dopant

As explained in Section 2.1.6, SoD offers the possibility of performing a non-destructive and low-cost doping of ultra-thin films. Throughout this work, the boron-doping SoD by Honeywell was used (ACCUSPIN®B-40). This product consists of a Borosilicate-based organic polymer that forms a boron-doped SiO_2 layer on the sample surface after drying. This SoD is front-end CMOS compatible.

Before spinning the SoD, the samples were cleaned in a piranha solution bath (H_2SO_4 : H_2O_2 = 3:1) for 10 minutes to eliminate organic residues, followed by a 10 minute water rinse. After, a 10 second dip in 5% HF, followed by another 10 minute water rinse, was done to etch the SiO_2 native layer. The processing in a clean room environment ensured low humidity for good film quality. When the relative humidity exceeds 50%, the SoD layer shows haziness and leads to non-uniform doping profiles on the samples [183]. The samples were spin-coated at 4000 rpm for 30 seconds. Then, the SoD was cured on a hotplate at 200°C for 180 s to eliminate the volatile solvent. In this case, a single curing step was enough to evaporate the solvent without cracking the SoD, while other SoDs may require multi-step curing to avoid this [184]. The annealing of the SoD was carried out at temperatures between 850 and 950°C in an inert atmosphere. The samples were loaded into the oven at 600°C and subsequently heated to the target plateau temperature at a rate of 5°C/min. After annealing, the samples were cooled down from the process temperature. Typically, when doping such thin Si layers, short rapid thermal annealing (RTA) treatments are sufficient to ensure dopant diffusion to depths greater than 50 nm. However, the doping profile with these RTAs tends to be far from uniform in these nanometric depths [184], [185]. In our case, dopant diffusion should be confined to the Si layer of the SOI sample, as both the buried oxide and the SiO_2 layer formed by the SoD at the interface act as diffusion barriers. Thus, the plateau duration was extended

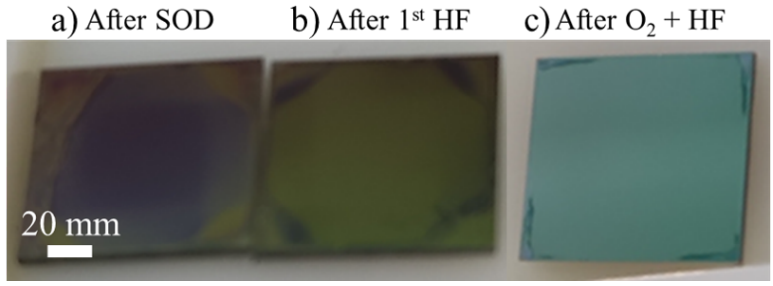


Figure 5.16: Pictures of 1x1 cm^2 chips throughout the SoD cleaning process to dope 50 nm thick Si films. a) After extracting the chip from the annealing furnace, b) after initial cleaning with HF, c) after O_2 plasma treatment and the later HF cleaning.

to ensure high uniformity of the doping in the thin Si film.

Theoretically, the residue remaining in the sample after the annealing step should only be composed of a SiO_2 thin film, which should be completely etched with 5% HF. However, repeated HF dips proved insufficient to completely clean the sample, as an insulating layer remained. Considering that the SoD is composed of borosilicate intertwined with a polymeric matrix, cleaning processes for organic materials were also explored. The optimal cleaning sequence was found to consist of a 1 minute 5% HF dip, followed by a 2 minute water rinse and a subsequent 20 minute exposure to an oxygen plasma. The optimal values of oxygen plasma were 600 sccm of O_2 and 1000 W of chamber power for 20 min. With this step, any polymer remaining on the sample after the diffusion step was completely removed. Finally, a 2 minute 5% HF dip followed by a 2 minute water rinse eliminated the remaining SiO_2 layer (see Figure 5.16). To confirm that the sample is clean, complete hydrophobicity was to be observed after the final water rinse. If hydrophobicity was not observed, further dips in 5% HF followed by water rinsing were performed until hydrophobicity was achieved.

The doping objective was set to achieve carrier concentrations between 10^{19} and 10^{20} cm^{-3}. Annealing was conducted at temperatures in the range of 850–950°C, and the samples were subsequently evaluated. Resistivity was determined from 4-probe characterization as described in Section 2.3. The resistivity and doping density are shown in Figure 5.17. The resistivity of the film shows a linear trend that is inversely proportional to the annealing temperature, and boron densities fall within the 10^{19} to 10^{20} cm^{-3} range. Based on these results, the 850°C and 900°C anneals were chosen for further optimization, and four new batches of nine chips each were processed: three of them were annealed at 900°C, and the fourth at 850°C (see Figure 5.18). The nine chips of each batch were spin coated on the same day and annealed simultaneously in the furnace. The plot demonstrates high reproducibility within batches and lower reproducibility between different batches. Nevertheless, the differentiation between the two annealing tempera-

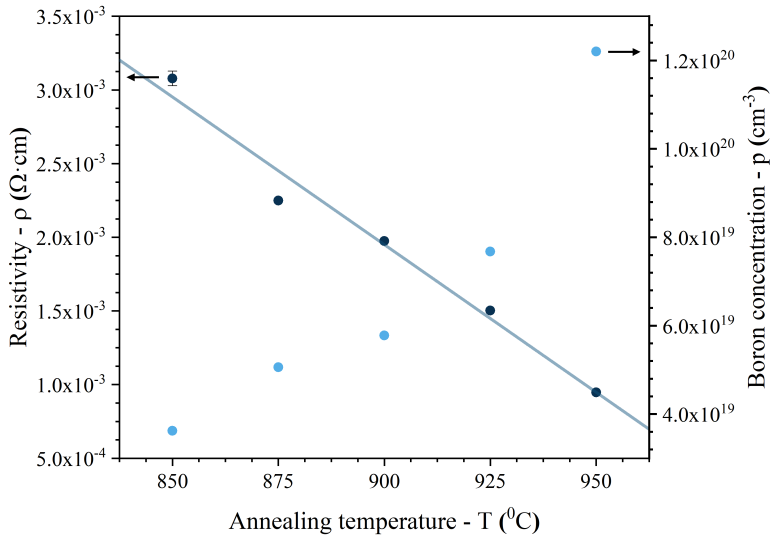


Figure 5.17: Resistivity and doping concentration obtained with SoD versus annealing temperatures. The doping values are calculated assuming no change in the carriers mobility.

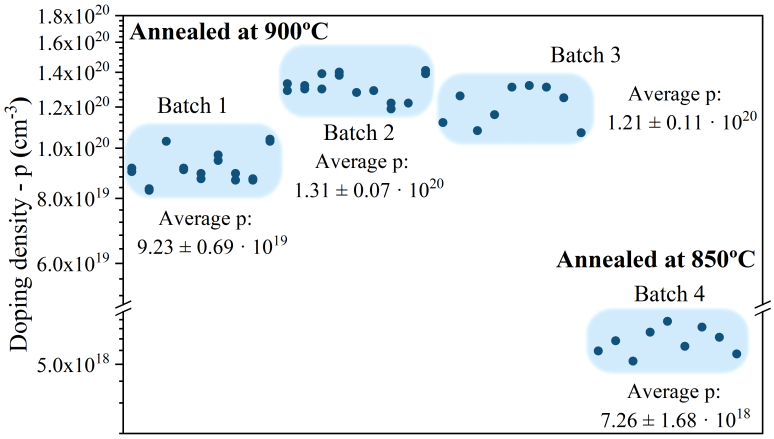


Figure 5.18: Comparison of doping densities of 50 nm thick Si films in different batches of chips doped with SoD at 900°C and 850°C.

tures is clear and, when annealing at 900°C, doping levels appropriate for thermoelectric applications are ensured (i.e. from $6{\cdot}10^{19}$ to $1.3{\cdot}10^{20}$ cm^{-3}).

The GDOES profile of boron and oxygen in 17 and 50 nm thick SOI chips doped with SoD at 900°C is shown in Figure 5.19. The presence of boron is clear in both Si and BOX, indicating that dopant atoms were able to diffuse deeply into the underlying oxide. Two possibilities could justify this behavior: GDOES eliminates the layers sequentially, but leftover atoms from the previously etched layers may remain on the surface, thus appearing in the spectra of the underlying layers. However, considering that long annealing times were used in these samples, and that the oxide only blocks boron diffusion when the boron concentration is higher than 10^{19} cm^{-3} within the oxide [186], some diffusion of dopants into the BOX is expected. Both observations agree with the fact that boron presence decreases in the BOX with depth, while bulk Si contains no boron. As for the homogeneity of the depth profile in the top Si, both samples show good uniformity, with a slightly higher quantity of boron near the interface with the BOX. This is expected for concentrations above 10^{19} cm^{-3} where the oxide acts as a stopping layer, accumulating dopants in its interface. These results demonstrate that longer annealing times help homogenize the in-depth profile of the doping and are compatible with thin Si SOI samples.

Further characterization was performed to study the homogeneity of the doping at the wafer scale. In this frame, 100 mm SOI wafers with 50 nm thick Si device layers were doped under the same spinning and annealing conditions, and 4-probe characterization was later performed at 50 points homogeneously distributed within the wafers. The mappings are reproduced in Figure 5.20. Average resistivities of $1.46{\cdot}10^{-3} \pm 1.67{\cdot}10^{-4}$ Ω·cm and $1.41{\cdot}10^{-3} \pm 7.14{\cdot}10^{-5}$ Ω·cm were obtained in two wafers, proving that the SoD procedure leads to reliable and homogeneous doping at a wafer scale. Furthermore, the doping values are well within the resistivity range obtained at a chip scale across different batches, demonstrating the reproducibility of the process when scaling to wafer-scale. All the results fall within the optimal range for thermoelectric applications.

Besides, the doping of N-type intrinsic wafers by SoD was evaluated to assess its value for other technologies. In this case, the annealing was set at 1100°C. The profile of Boron at the center of the wafer and at the outer ring is reproduced in Figure 5.21.

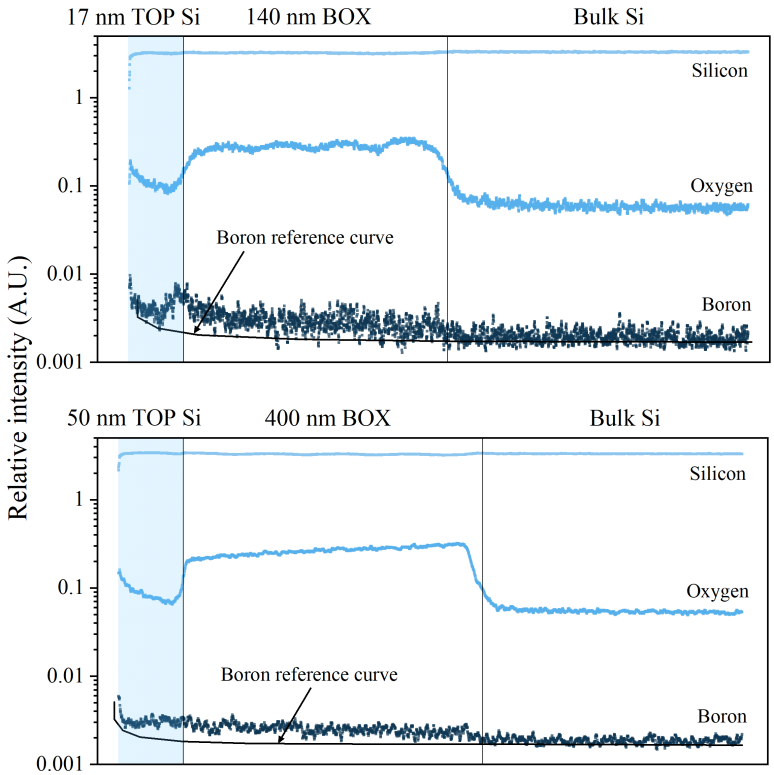


Figure 5.19: Plot of the relative intensity of silicon, oxygen and boron obtained by GDOES from 17 and 50 nm thick Si films doped by means of SoD at 900°C. Boron reference curve is plotted to better calibrate the boron presence in the samples.

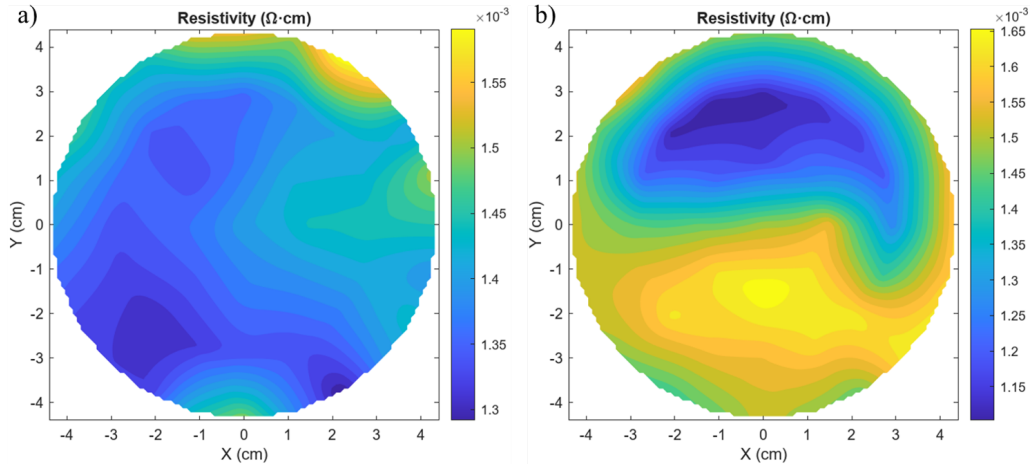


Figure 5.20: 4-probe maps of the resistivity of 50-nm thick SOI films doped with SoD at 900°C over a 4 inch wafer. Resistivities of $1.46{\cdot}10^{-3} \pm 1.67{\cdot}10^{-4}$ Ω·cm and $1.41{\cdot}10^{-3} \pm 7.14{\cdot}10^{-5}$ Ω·cm are obtained on the wafer in a) and b), respectively.

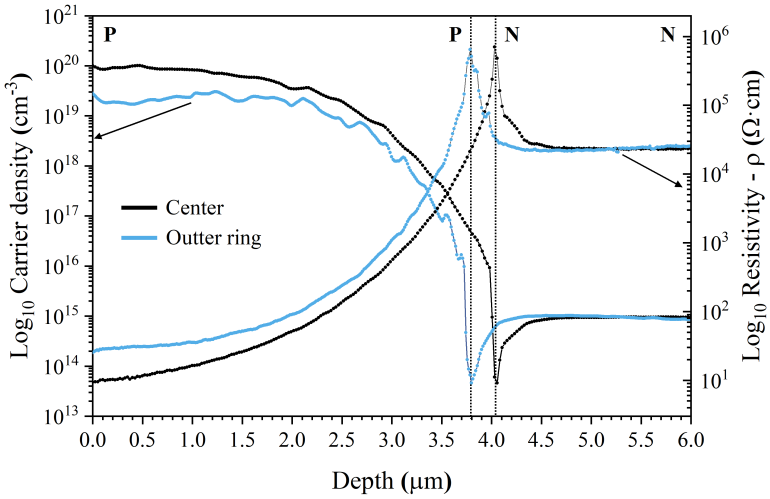


Figure 5.21: Carrier density and resistivity of an intrinsic N-type bulk Si wafer doped by SoD at 1100°C. 4 µm is the maximum depth where doping is above the intrinsic value.

A carrier density between $3{\cdot}10^{19}$ and 10^{20} cm^{-3} of boron atoms was obtained at the surface, depending on the spot, with the center of the wafer showing the highest doping. The profile of the doping shows a decrease with depth until it reaches 4 µm, where the intrinsic doping level is found. Interestingly, as there is no diffusion stopper near the surface (i.e. no BOX), the carrier density is similar to that obtained in the thin films at lower temperatures. These values and profiles demonstrate that SoD is also compatible with the doping of bulk Si.

5.3.1 Electrical characterization of nanostructured silicon thin films

After optimizing the doping of thin films, the approach to combine doping and nanopatterning was considered. The decision was made to complete the doping first and then the nanostructuration, because otherwise inhomogeneities in the doping could arise. The doping followed the procedure explained in Section 5.3. After, the BCP self-assembly and PMMA etching procedures were completed as in Section 5.2.1. The final etching of Si showed no significant variation with respect to the pattern transfer on the non-doped films, as it was only necessary to adjust the etching time by adding one second. Figure 5.22 shows two tilted cross-section SEM images of a doped and an un-doped Si film after the same nanostructuring process. The walls of the holes show the same verticality, and the diameters are similar in size. No difficulties were encountered in completely etching through the film.

Further 4-probe characterization of the film resistance was performed on the samples after BCP etching to compare these values with those from the bare films. The resistivity of the nanostructured films is expected to be higher for two reasons: the first is the decrease in the cross-sectional area after patterning the holes. The second is the possible increase in electron scattering that may occur because of the greater dimensional confinement of these structures. Thus, the resistance of the nanostructured film (R_{BCP}) can be related to the bare film (R) as follows:

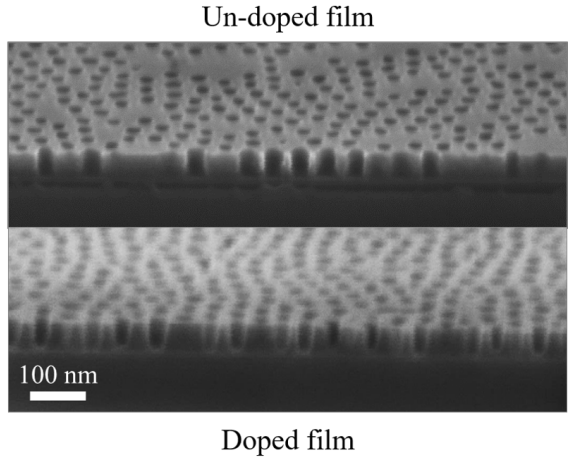


Figure 5.22: SEM images of a non-doped and a doped 50 nm thick Si film with the same cylindrical nanostructuration with a period of $\sim$ 57 nm.

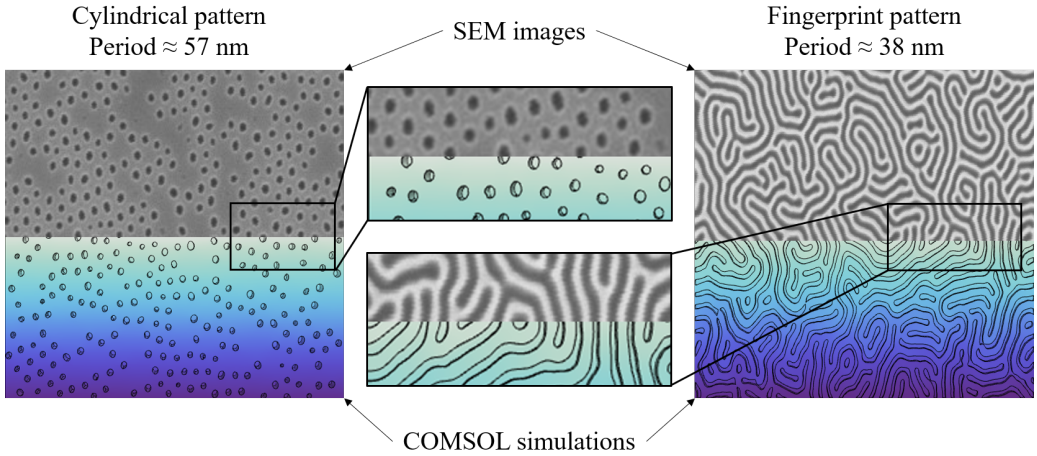


Figure 5.23: Examples of the transfer of the nanostructured patterns into a COMSOL model. The image-to-curve tool achieves a precise reconstruction of the pattern in COMSOL to later obtain accurate values of the geometrical factor of the thin films.

$$R_{BCP} = \rho_{BCP}\frac{L}{A}F_G = F_{BCP}\rho\frac{L}{A}F_G = F_{BCP}F_G R \tag{5.1}$$

being ρ_{BCP} the intrinsic resistivity of the nanostructured film, L and A the length and cross-sectional area of the film, and F_{BCP} and F_G the scattering and geometric factors, respectively. This last parameter, F_G, is only related to the volume of the final nanostructured film; therefore, it can be precisely obtained through COMSOL simulations. Top-view SEM images of the nanostructured samples were used to build the volumetric films in COMSOL using the image-to-curve tool, which allows for the conversion of changes in color in the images into curves by conveniently adjusting the parameters of a

Gaussian filter. Figure 5.23 shows the precision of this pattern transfer into COMSOL in two exemplary geometries. The geometric factor can be calculated by simulating the resistance of the film with and without the holes, while maintaining the resistivity value constant in both cases, and then calculating the ratio. The resistivity values are those measured from each bare film using the 4-probe method. An error of ± 4 nm in the etched depth was assumed when calculating the geometric factor of the nano-patterned films. This way, the resistivity of the nanostructured film is expressed as:

$$\rho_{BCP} = \rho F_{BCP} = \frac{R_{BCP}}{R}\frac{1}{F_G} \tag{5.2}$$

The results of these measurements and subsequent calculations for the cylindrical BCP with a period of 57 nm are shown in Figure 5.24. An increase in the intrinsic

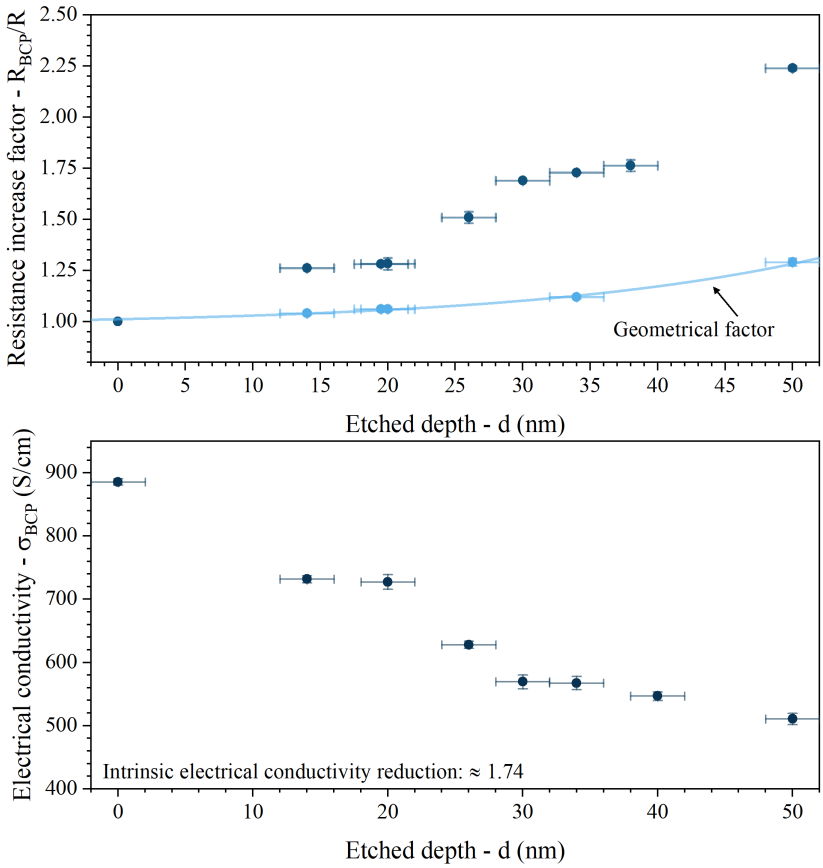


Figure 5.24: Resistance increase factors and intrinsic electrical conductivity of cylindrical C35(50%)-C80(50%) BCPs versus etched depth. For depths < 25 nm the underlying continuous film dominates the electrical flow and the increase on intrinsic resistivity of the film is low (< 1.2). Once this etching is surpassed, the holey pattern dominates and further increases it by ~ 1.7 in the completely etched film. The final values of intrinsic electrical conductivity versus etched depth calculated with the scattering factor (F_{BCP}) are shown in the lower plot.

resistivity of the film (i.e. ρ_{BCP}) of 10–20% is observed when the etching depth is below 25 nm. In this case, the enhancement of electron scattering is shallow because only decoration of the film is present, and boundary scattering does not dominate electrical conduction. On the other side, once the etching goes beyond this depth, boundary scattering of the holey pattern becomes more dominant, and the intrinsic resistivity increases by up to 74%. With these factors, and starting from the electrical conductivity achieved with the SoD on the bare Si films ($\sim$ 900 S/cm), a final intrinsic conductivity of $\sim$ 520 S/cm is obtained in the holey Si films with through holes. In this nanostructured pattern, the dimensions of the neck size increase with depth, reaching an average value of $\sim$ 27 nm when there is complete etching of the Si film. In Si thin films, an increase in resistivity can be observed once the thickness is under 30 nm, and it is especially noticeable for thicknesses below 20 nm [187]. Considering that the lateral size confinement of the holey films in this work is around 20-30 nm, an increase in resistivity is also expected. This behavior was also observed previously in similar holey patterns [101]. Nonetheless, this increase corresponds to the intrinsic resistivity, so it is only accurate from a material perspective. The increase in the overall resistance of the film is greater, as it also takes into account the geometric factor. For this type of nanostructuration and complete etching, the effective electrical conductivity of the film is $\sim$ 400 S/cm.

Table 5.5: Increment of resistance, geometric factor and scattering factor of Si thin film decorated with lamellar patterns.

Block copolymer	Etched depth (nm)	R_{BCP}/R	F_G	F_{BCP}
L37	10 ± 4	1.30	1.14	1.14
L37	21 ± 4	1.60	1.40	1.14

In the case of lamellar patterning, the etched depth is always lower than 25 nm, meaning that a continuous film with t > 25 nm is always present. In this configuration, the increase in intrinsic resistivity is around 1.1 in all the studied samples (Table 5.5. This is in agreement with the increase factor observed in the cylindrical patterns with equivalent etching depths, proving again that the underlying continuous film dominates the electrical transport if > 25 nm. Patterning to higher depths was discarded due to the significant degradation of conductivity expected.

5.4 Chapter conclusions

This chapter presented the work related to nanostructured Si thin films. The self-assembly of PS-b-PMMA BCPs was optimized using cylindrical and lamellar BCPs, either with their original morphology or through blending. Subsequently, these patterns were transferred into Si films using both wet and dry etching techniques, demonstrating that PS-b-PMMA nanometric patterns can be directly transferred (without any intermediate layer) into 50 nm thick Si films with complete anisotropy and reproducibility. A reliable procedure for doping thin Si films with SoD was developed at both chip and wafer scales. Moreover, the doped films were fully compatible with the previously optimized pattern transfer process. The doping resulted in an optimal dopant density in the 10^{19}-10^{20} cm^{-3} range, with good homogeneity across the wafers. Subsequent characterization of the nanostructured films showed that the intrinsic electrical resistivity of a film with a cylindrical holey pattern with a period of 57 nm suffers a 1.74-fold increase, reaching a

final σ_{BCP} of 520 S/cm. On the other hand, the lamellar patterning had a negligible effect on the intrinsic electrical resistivity when the etched depth was below 25 nm, which is the only patterning compatible with thermoelectric applications.

Chapter 6

Thermal characterization of nanostructured silicon thin films

This chapter presents the results of the thermal characterization of nanostructured silicon thin films with a 57-nm cylindrical pattern. This characterization was done using three different techniques: 3ω steady state, FDTR and bridge/laser. 3ω steady state was done in collaboration with UAB, while the other two were developed in the scope of an internship at the University of Basel in Switzerland. 3ω steady state and bridge/laser were used to measure the thermal conductivity of Si thin films with different etching depths, while FDTR characterization is still ongoing (see Section D.1 for the initial tests).

6.1 3ω steady state

6.1.1 3ω device design

As explained in Section 2.4.1, 3ω steady state characterization involves the use of a central metallic stripe on top of a suspended membrane to measure the in-plane thermal conductivity of the thin film. The device fabricated for these measurements features a 3 x 0.2 mm membrane, with two metallic stripes (each 5 µm in width) placed on top of it, one in the center (heater/sensor for the 3ω steady state) and another at the edge (sensor) to have the possibility of measuring the temperature of the bulk. The voltage probes of the central stripe are placed 500 µm from the membranes edge (see Figure 6.1) in order to measure the voltage with a homogeneous temperature profile. As shown in Figure 6.1 simulation plots, the lateral temperature profile is homogeneous in the central 2 mm of the membrane followed by a large thermal gradient in the close to the edges. This simulation result was used to place the probes 500 µm inside the membrane. Regarding the cross temperature profile, a linear decay is observed in the simulations in all the sections within the voltage probes. Therefore, with this membrane size and probe placement a rectangular area with homogeneous lateral temperature and linear cross profile is obtained.

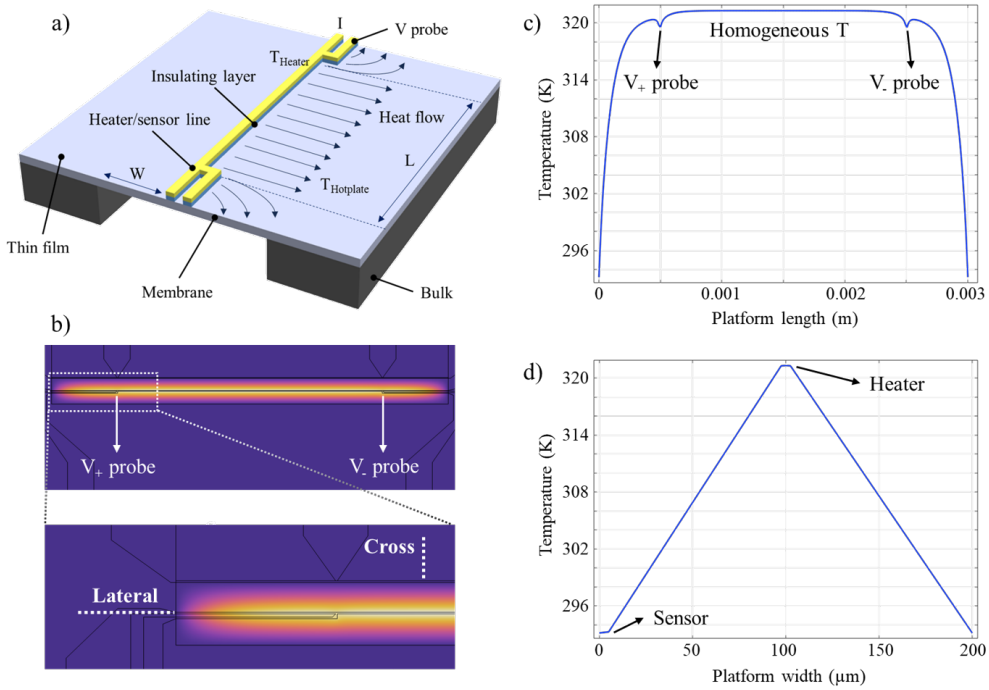


Figure 6.1: COMSOL simulations of the 3ω device design. a) Scheme of the typical 3ω chip, b) COMSOL simulations of the 3 mm x 200 µm membrane defined in the middle of the chip with two metallic stripes. The voltage probes of the central heater are placed 500 µm inside the membrane to measure a constant temperature profile. c) Lateral temperature profile. d) Cross temperature profile.

6.1.2 3ω device fabrication

The fabrication of the device started with a SOI wafer with the following thicknesses: 50 nm, 400 nm and 725 µm for the top Si, BOX and bulk Si, respectively. The latter value corresponds to the nominal thickness, as a more accurate measurement was not possible (nominal thickness is 725 µm ± 15 µm). A variation of approximately 15 µm was therefore considered (as reported in the manufacturer's certificate of analysis for the wafers). It is worth mentioning that the backside of the wafer was unpolished, a detail that proved to be relevant during the KOH etching step. A scheme of the fabrication steps is summarized in Figure 6.2. The process started with a cleaning in piranha (H_2SO_4:H_2O_2 = 3:1) for 10 minutes to eliminate organic residues followed by a 10 seconds dip in 5% HF to etch any native SiO_2 layer, with 10 min water rinses between each step. Then, SiO_2 films were deposited by PECVD on both sides of the wafer, 100 nm on the top and 200 nm on the bottom. Followed by a 300 nm thick low-stress Si_3N_4 layer deposited by LPCVD on both sides.

Bilayers were used on both sides for specific functional reasons. On the top side, Si_3N_4 serves as an electrical insulator between the subsequently deposited metal stripes and the Si film. Meanwhile, SiO_2 serves as a sacrificial layer to etch the Si_3N_4 without damaging the device Si. On the bottom side, it is used as a mask for the KOH etching. In this case, the addition of the SiO_2 layer helps compensating stress on the bottom

side. Otherwise, some peeling off of the nitride due to stress during the KOH could lead to undesired openings on the bulk Si. While optimizing each fabrication step, it was found that annealing the PECVD-deposited SiO_2 at 850°C for 30 min in N_2 was crucial to densify the layer and promote conformal coverage on the rough backside of the wafer, resolving previously observed pinholes and defects during membrane patterning. The membranes exhibited defect-free morphology after this annealing, with dimensions consistent with the mask designs.

After bilayer deposition, rectangles on the backside were patterned by photolithography and RIE of the Si_3N_4 and SiO_2 films to define the window for the subsequent

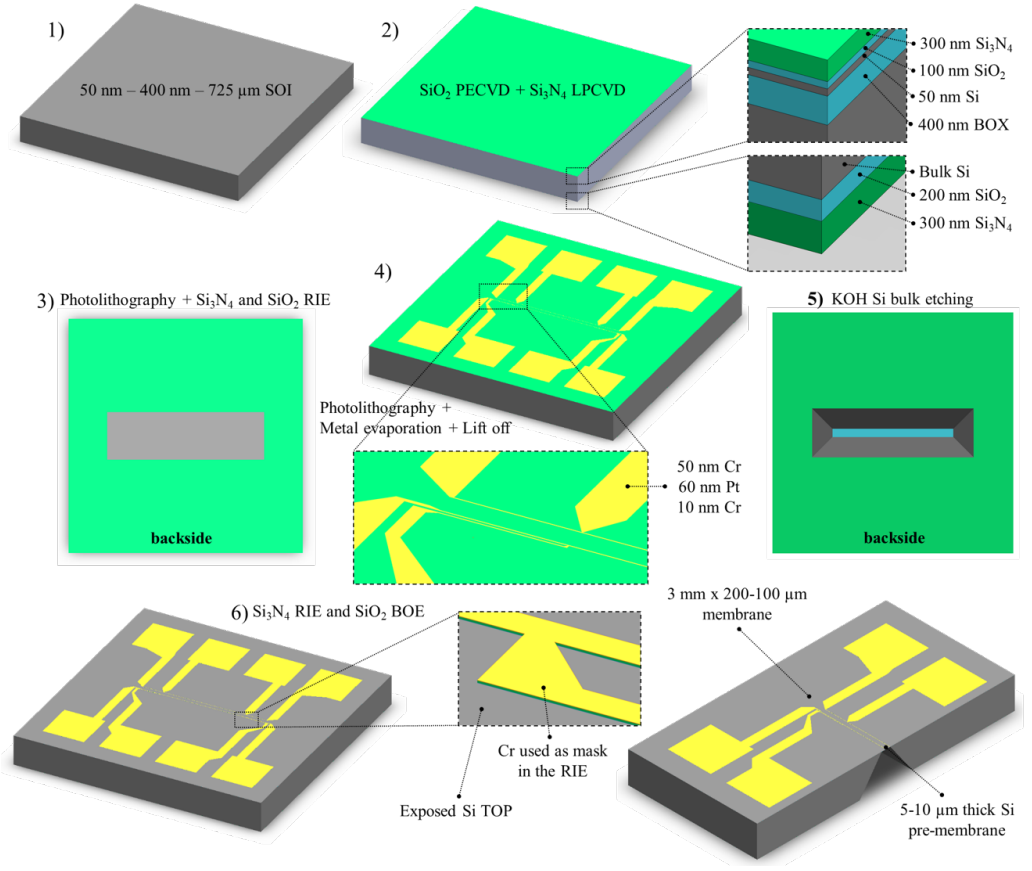


Figure 6.2: Scheme of the main fabrication steps of the 3ω chip. 1) SOI wafer with 50 nm, 400 nm and 725 µm thick layers of top Si, buried oxide and bulk Si, respectively. 2) PECVD deposition of SiO_2 on top (100 nm) and bottom (200 nm) of the wafer. In the optimized process, these depositions are followed by a 30 min annealing at 850°C. After that, a 300 nm thick low-stress Si_3N_4 is deposited by LPCVD on both sides. 3) Photolithography and RIE to define and open a window on the backside. 4) Photolithography, evaporation of a multilayer of Cr/Pt/Cr (10/60/30 nm) and lift-off. 5) KOH of the bulk Si, leaving 5-10 µm of bulk Si below the BOX as a pre-membrane. 6) Si_3N_4 elimination with a RIE using the Cr as a hard mask followed by a BOE attack to remove the exposed SiO_2 film.

KOH. Then, another photolithography process is used to define the metal layout, which is later evaporated on the sample. A trilayer of metal is deposited, composed of: 10 nm of chromium (Cr), 60 nm of platinum (Pt) and 30 nm of Cr. The first Cr layer is used for adhesion purposes of the Pt metal, which is the main metal of the heater. The top Cr film serves as a hard mask for the posterior RIE of the nitride. The subsequent lift-off eliminates the photoresist and the undesired metal. Next, the bulk Si is etched by means of KOH from the backside. Here, the Si_3N_4 serves as a mask for the KOH. The etch is stopped when 5–10 µm of bulk Si remains beneath the membrane, ensuring a sufficient mechanical robustness to withstand the subsequent processes required for BCP self-assembly and pattern transfer. Next, on the top side, a RIE removes the Si_3N_4 using the metal trilayer as a mask. Here, the 100 nm thick SiO_2 acts as a RIE stopper of the Si_3N_4 etching. Without the SiO_2 layer, any over-etching of the Si_3N_4 (which is necessary due to non-uniform RIE across the wafer) would risk etching and degrading the underlying thin Si layer. The RIE is followed by a wet etching of the remaining exposed SiO_2 in BOE to expose the thin Si layer, which is selective to Si. At this point, the wafer was diced into 6x6 mm^2 chips to maximize the effectiveness of the experimental efforts and the available resources. Representative images of the fabrications are shown in Figure 6.3. The optical image shows the final layout of the 3ω chip. The cross-section and tilted SEM images show regions around the metallic stripes where the thin Si was exposed. The images confirm the protective role of the SiO_2 film as a sacrificial layer for the underlying Si film.

The Si film nanostructuration was completed as described in Section 5.2, with some remarks. To address film inhomogeneities arising from the small chip size, the spin-coating speed was increased from 1500 rpm to 2000 rpm, and a reduced amount of the BCP-PGMEA solution was applied via drop-casting. This resulted in a reduction of the BCP thickness by $\sim$ 3 nm, without compromising a complete pattern transfer. Lastly,

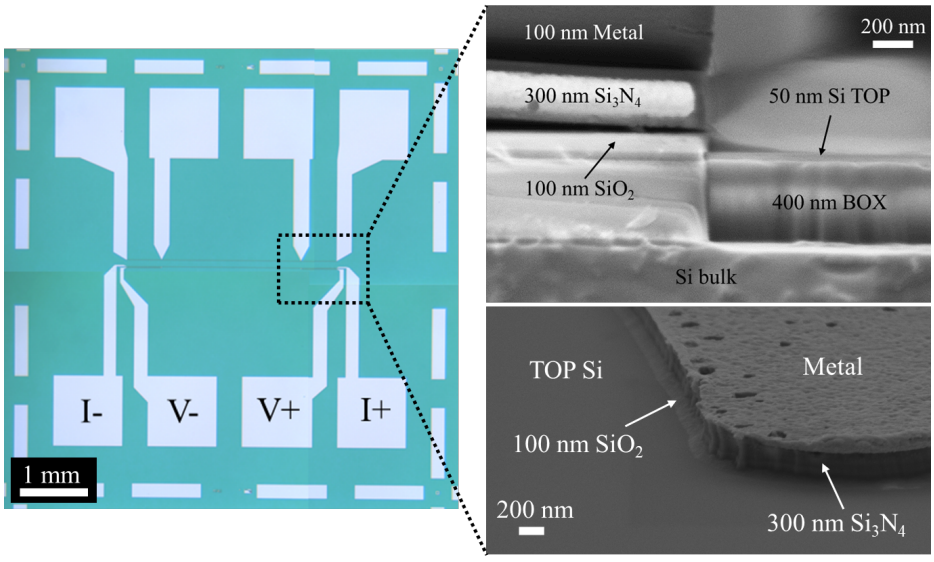


Figure 6.3: Optical and SEM images of the 3ω device after wafer-scale fabrication. The cross-section and tilted SEM images show details of the areas around the metallic stripes, where the layers present in the top side of the device are shown.

since the membrane thickness prevented the use of ultrasonic cleaning to remove the brush residues, a different procedure was developed. The process involved drop-casting a large volume of PGMEA onto the chips, followed by spinning at 2000 rpm for 30 s to remove the non-grafted residues. The rest of parameters were equivalent to those of the procedure on a free-surface.

Representative images of the pattern transfer on the 3ω devices can be seen in Figure 6.4. These images show how the brush is grafted onto the vertical walls of the device, and how the subsequent BCP deposition also forms cylindrical phases there. Away from the walls, the Si patterning is equivalent to that on free-surface and complete etching was achieved. Also, the hole profile and neck size were measured to be equivalent to those of the free-surface. A larger amount of BCP accumulated close to the vertical walls. This resulted in orientation discontinuities of the cylinders within the depth of the BCP film and hindered the pattern transfer to the underlying Si in regions extending up to ∼ 400-500 nm around the vertical walls of the metal stripe. The non-patterned area compared to the accurately nanostructured area was negligible in the 3ω membranes.

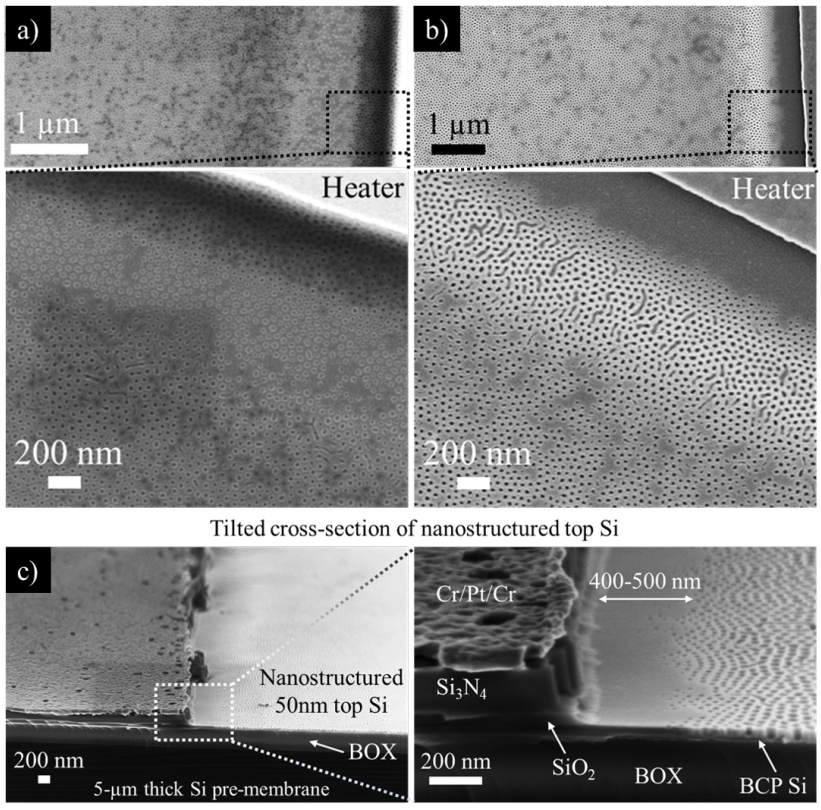


Figure 6.4: SEM images of the 3ω chip after wet etching of the PMMA cylinders and subsequent pattern transfer into Si using the PS mask; a) after wet etching of PMMA cylinders and, b) after the pattern transfer into Si using the PS mask. c) Tilted cross-sections of the same area showing the complete etching of the Si film integrated in this device. The magnification image highlights the ∼ 400-500 nm wide region close to the metal stripe where the pattern transfer is hindered.

The final and most critical step of the 3ω device fabrication was the membrane release. As it has been explained previously, at this point the chip had a 5-10 µm thick silicon pre-membrane for mechanical robustness. Since this bottom silicon can no longer be etched in a KOH bath without affecting the 50 nm-thick nanostructured Si on the top side, a new procedure was developed for backside KOH etching preserving the top side. Different experimental setups and procedures were explored to confine the KOH etching to a specific area on the backside. A first approach based on KOH at room temperature was discarded due to its slow etch rate, which was difficult to control and led to the formation of dry layers of potassium salts that hindered further etching of Si.

Another approach was based on mounting the 3ω chip between custom Teflon and PMMA pieces with an O-ring to confine the KOH droplet. Unfortunately, this was also discarded because the mechanical pressure required for proper sealing broke the device once the membrane was released (see Figure 6.5a). The next approach was successful and involved the use of hydrophobic adhesives to confine the KOH solution. The compatibility of vinyl and pressure sensitive adhesive (PSA) with KOH etching at 80°C for more than 1 h was validated for both materials. PSA was finally chosen for its better adherence to the backside of the chips. The procedure involved taping the backside of the chip with PSA and then placing the stack upside-down on a custom PMMA piece designed to prevent the membrane from contacting any other surface. This whole structure was placed on a hotplate at 90°C next to a beaker with 40% KOH in water. Finally, $\sim$ 50 ml of KOH were drop-casted with a micro-pipette inside the PSA hole. The average duration of the KOH etching in these conditions varied from 2 to 4 h depending on the remaining bulk Si thickness (5 to 10 µm). During this process, the chip was rinsed in water and IPA every 30-40 min. After each cleaning, the chip was placed back on the PMMA, and another $\sim$ 50 ml droplet of KOH was casted to continue the etching. The reason for performing this multi-step etching was that the potassium salts formed as byproducts of the KOH reaction impeded further etching. When complete membrane transparency was observed, the chip underwent a final cleaning step in water with $\sim$ 10-20% IPA. IPA was used to decrease surface tension and prevented mechanical damage to the membranes.

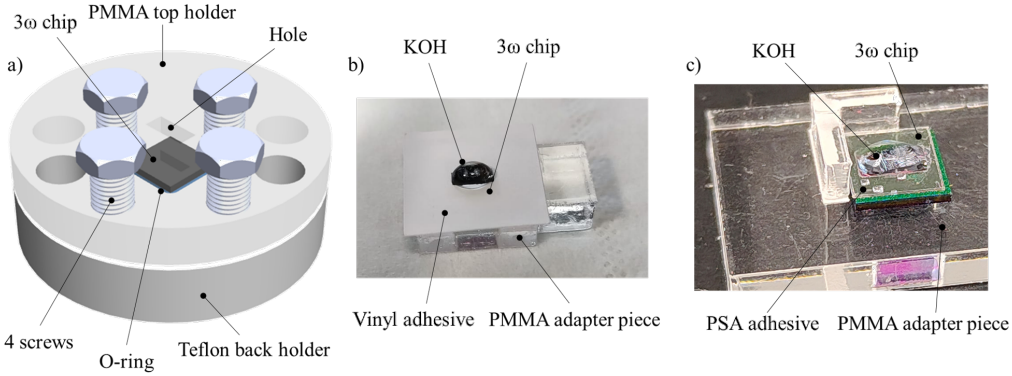


Figure 6.5: Schemes of the three main routes used to control the KOH droplet and perform the etching at temperatures > RT. a) Schematic of the PMMA and Teflon pieces to seal the chip with an o-ring and four screws. b) Assembly with hydrophobic vinyl adhesive to confine the droplet. c) Assembly with hydrophobic PSA adhesive to confine the droplet. The latter proved to be the most reliable to control the droplet.

After suspending several membranes with only Si and BOX, the compressive stress of the oxide caused extreme deformation on the membrane, normally leading to membrane rupture or cracks formation (see Figure 6.6). Therefore, the final optimization was focused on minimizing the suspended membranes stress by adding an additional Si_3N_4 thin film (the tensile stress of PECVD Si_3N_4 helps compensate for the compressive stress of SiO_2). Si_3N_4 layers of different thickness were deposited on top of different chips (see Figure 6.6). The thicknesses ranged from 180 to 300 nm. The results showed that increasing the thickness of the Si_3N_4 resulted in a smaller membrane deformation, up to the point (300 nm thick case) where a flat membrane was observed. However, 3ω steady state characterization of these devices measures the entire stack of layers (i.e. BOX, thin Si, and Si_3N_4). Therefore, a 180 nm thick Si_3N_4 film was selected to ensure that changes in κ of the Si thin film after nanostructuring could be detected. The addition of the Si_3N_4 layer required reordering some process steps and introducing new ones at chip level. In particular, after the nanostructuration of the Si film, a 180 nm thick Si_3N_4 film was deposited by PECVD on top of the chip. Since the Si_3N_4 coated the entire surface, it became necessary to add processing steps to remove it from the contact pads. Then, KOH was completed following the previously described PSA procedure. Once the membrane was fully released, the PSA adhesive was removed. Finally, the chip was wire-bonded onto a custom PCB to carry out the 3ω steady state measurements.

In summary, this section defines a process to fabricate functional devices integrating thin layers of nanostructured Si based on the transfer of BCP patterns. This required the optimization of several process steps, including BCP patterning, backside KOH etching and stress compensation (see Figure 6.7 for the final nanostructured 3ω membrane). Even though some chips could be fabricated and measured, as will be shown in the next section,

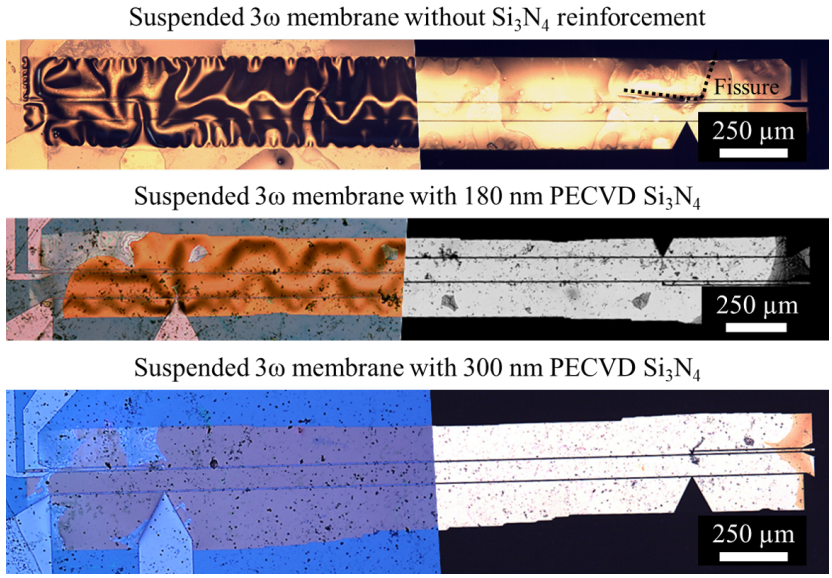


Figure 6.6: Optical images of three suspended membranes with different PECVD Si_3N_4 stress compensation. Left images were taken with top illumination, the right ones were taken with bottom illumination. The thicker the Si_3N_4, the better the stress compensation.

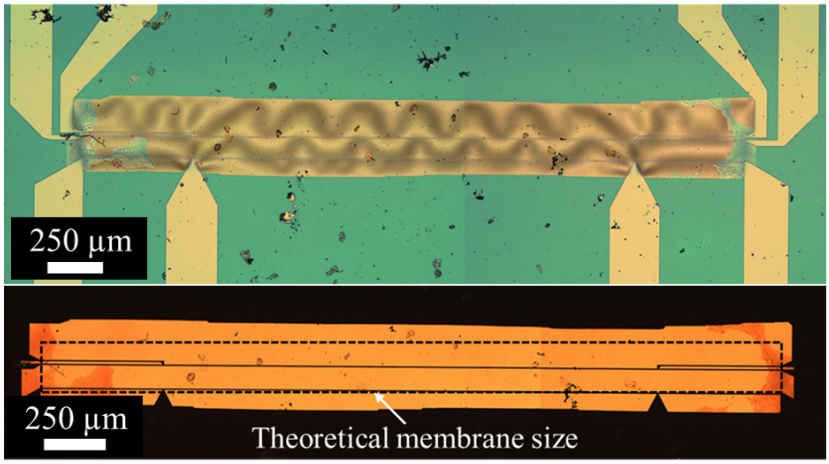


Figure 6.7: Optical images of a suspended membrane with Si_3N_4 support and nanostructured Si. The top images were taken with top illumination, while the bottom ones were taken with bottom illumination. The membranes are larger than the original design due to the appearance of pinholes in the bottom mask during the KOH etching process.

further improvements were explored. For example, it was found that an annealing after the PECVD deposition of SiO_2 was key to eliminate pinholes and defects in the backside mask to define the membranes. After this annealing, the membranes were defect-free and dimensions matching the mask designs. Despite that, these improved chips were not used in the 3ω steady state results shown below, but this improvement was later used in the µTEG fabrication.

6.1.3 3ω steady state characterization

To carry out the 3ω steady state measurements using the methodology in Section 2.4.1, the chips were mounted on custom PCBs using silver paste to ensure good thermal contact, which is key in these measurements. In brief, the chip was externally heated using a hotplate (280 - 305 K) while the central metallic stripe served as a heater inducing a heat flux via joule heating. All this was done in vacuum. The heater was also used as a sensor to measure the resistance change as a function of the applied current, which was converted to a temperature through the previously calibrated TCR. To obtain the TCR, R_0 (the resistance at zero current in the heater) at each hotplate temperature was determined by linear fitting of the resistance versus applied power and subsequent extrapolation to zero current. Then, the TCR of the metallic stripe can be obtained after a linear fitting to the R_0 vs temperature data (see Figure 6.8). As it can be seen, in the measured temperature range the linear fit has a good agreement. Equation 2.11 was used to calculate the thermal conductance of the film.

The results are shown in Figure 6.9a for all the C57 samples measured as a function of the hotplate temperatures. A clear trend is observed on the conductance versus etched depth curves. Deeper etching reduces the membrane's thermal conductance. Since Si_3N_4 and BOX layers are uniform across the chips, the observed change in thermal conductance is attributed solely to the nanostructuration of the Si layer. This is expected to be mainly a consequence of enhanced phonon scattering due to the nanostructuring of Si. As it turned

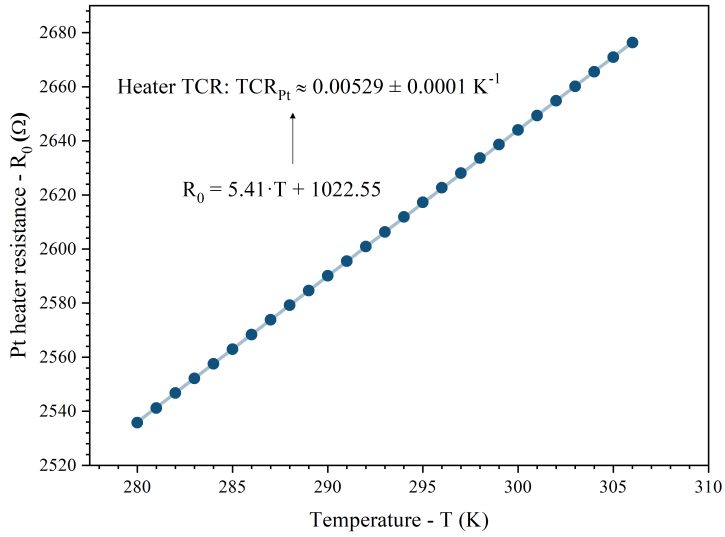


Figure 6.8: Pt heater resistance (R_0) versus hotplate temperature in the 3ω steady state measurements. A TCR of 0.00529 is obtained for the device shown.

not possible to suspend a membrane made of Si_3N_4 and BOX (i.e. without the thin Si film, due to membrane breakage caused by stress), the conductivity of a bare Si thin film obtained from the bridge method characterization, which is discussed in Section 6.3, was used here as a reference to obtain a value for $\kappa_{SiNx-BOX}$. To do so, the thickness of Si_3N_4 and BOX on each chip is needed, and using:

$$G_{Si}^{Bare} = 2 \cdot \kappa_{Si}^{Bare} \frac{L \cdot t_{Si}}{W_{mean}} \rightarrow G_{SiNx-BOX} = G_{TOT} - G_{Si}^{Bare} \rightarrow$$

$$\kappa_{SiNx-BOX} = G_{SiNx-BOX} \frac{W_{mean}}{2L \cdot t_{SiNx-BOX}} = (\frac{G_{TOT} \cdot W_{mean}}{2L} - \kappa_{Si}^{Bare} \cdot t_{Si}) \frac{1}{t_{SiNx-BOX}} \tag{6.1}$$

being L the distance between the voltage probes, and W_{mean} the average width of one membrane half (i.e. half the width of the overall membrane, see Figure 6.1). The factor two in the equation accounts for the fact that heat travels through both sides of the membrane in parallel. Using a similar procedure, the thermal conductivity of a nanostructured Si film can be written as:

$$\kappa_{Si}^{BCP} = (\frac{G_{TOT} \cdot W_{mean}}{2L} - \kappa_{SiNx-BOX} \cdot t_{SiNx-BOX}) \frac{1}{t_{Si}} \tag{6.2}$$

where L and t_{Si} are constant across the samples (2 mm and 50 nm, respectively) and W_{mean} was measured from the optical image on each membrane. $t_{SiNx-BOX}$ was measured using a reference chip during the Si_3N_4 deposition (t_{SiNx} was subsequently measured on the reference chip with spectroscopic reflectometry). Since divergences of less than 3 nm were found between the Si_3N_4 thickness in the reference chip and that of the paired 3ω devices, SiO_2 and Si_3N_4 layers were considered uniform across these samples. Therefore, $\kappa_{SiNx-BOX}$ from the reference sample was also used in the calculations of every κ_{Si}^{BCP}. Furthermore, thickness variations < 3 nm in the 180 nm thick

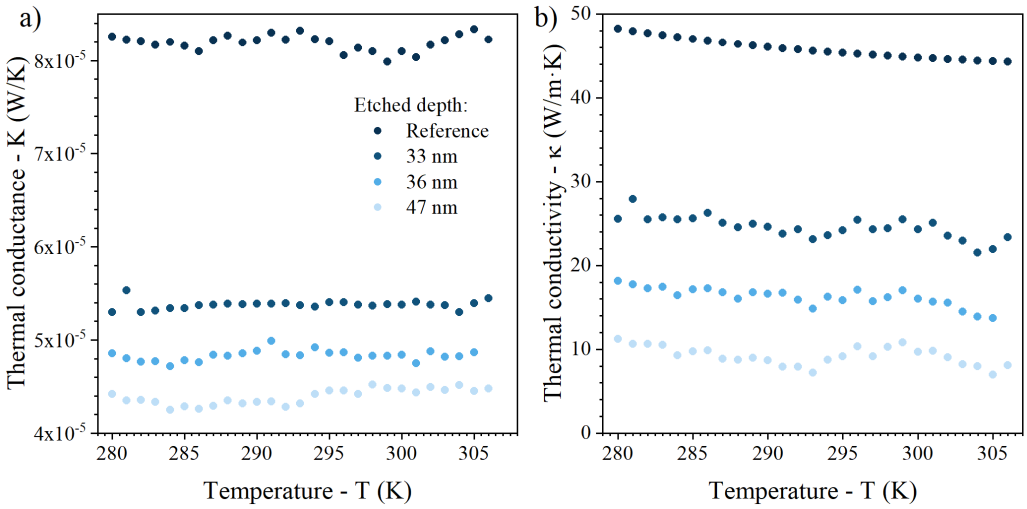


Figure 6.9: a) Thermal conductance of the differently etched C57 samples versus hotplate temperature. The conductance diminishes by increasing the depth of the pattern. b) Calculated thermal conductivity of the nanostructured Si films. The values used for the 50 nm thick bare film were measured with the bridge/laser method (see Section 6.3.3).

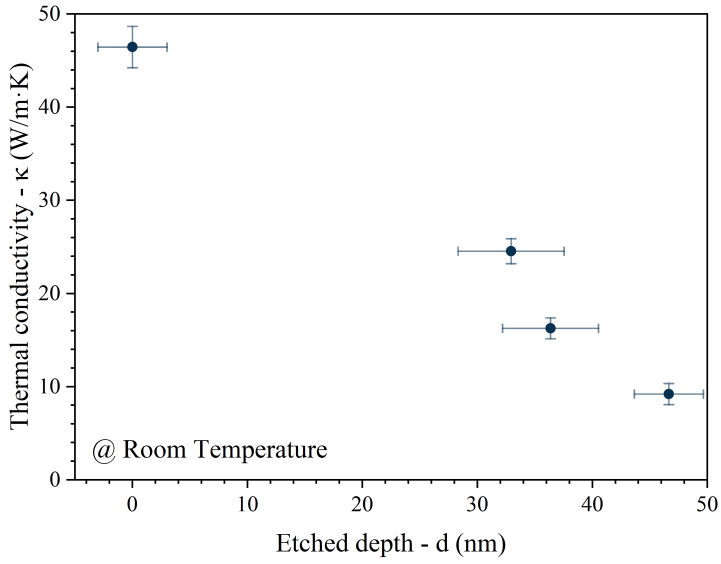


Figure 6.10: Silicon thermal conductivity at RT of the Si film as a function of the etched depth. A linear trend is observed, reaching a minimum value of $\sim$ 9.93 W/m·K ($\sim$ 46 nm etching).

Si_3N_4 film have a negligible impact on their thermal conductivity (such deviations are estimated to introduce an error of $\sim 1\%$ in the Si_3N_4 κ [188]). An uncertainty of 3 nm for $t_{SiNx-BOX}$, 2 µm for w_{mean} and 1 W/m·K for k_{Si}^{Bare} were considered. The κ of the partially etched silicon films obtained this way as a function of the hotplate temperature are shown in Figure 6.9. Figure 6.10 shows the thermal conductivity at RT as a function of the etched depth. Errors of κ of the nanostructured Si thin films were calculated by error propagation. The thermal conductivity decreases linearly with the etching depth, reaching a value of $\kappa = 9.93$ W/m·K for an etching depth of ~ 46 nm (one order of magnitude lower than the initial κ). For further details on κ as a function of the etched depth see Section 6.3.3, where 3ω steady state and bridge/laser results are discussed.

6.2 Thermoreflectance

As explained in Section 2.4.2, thermoreflectance characterization involves the use of a metallic transducer on top of the material of interest. To properly evaluate the in-plane thermal conductivity of the Si film, the device must have a suspended membrane. The design developed in this thesis consists of a rectangular suspended membrane featuring a circular Au transducer positioned at the center of this membrane. This section describes the fabrication of the thermoreflectance device, beginning with the development of the techniques to suspend 50 nm thick Si films. The second part of this section introduces the model developed to interpret the experimental results obtained from the fabricated devices. Last, Section D.1 describes the status of the membranes characterization.

6.2.1 Membrane release

The large uncertainty in the bulk silicon thickness of the SOI wafers used in this thesis (nominal thickness is 725 µm ± 15 µm) hindered the suspension of the membranes through backside KOH Si etching, as it would result in too large membranes or even no membranes at all (with KOH etching, the membrane size depends on the thickness of bulk Si). Therefore, alternative routes to suspend the membranes by etching the underlying BOX or the bulk Si from the topside were explored. Etching only the BOX is complex due to the thin BOX gap (400 nm). With such thin gaps, capillary forces may lead to membrane collapse (this effect is known as release stiction). Etching the underlying bulk silicon from the top, requires the protection of the top Si layer during the process. In this work, three different routes were explored to suspend the top Si through BOX etching: wet etching using BOE, BOE using a Si_3N_4 capping layer on the Si film, and HF vapors. In addition, two routes were investigated to etch the bulk Si beneath the membrane based on using Si_3N_4 and HfO_2 as protection layers. These latter ones are presented in Appendix B.

Membranes with widths and lengths ranging from 5 to 20 µm and 12.5 to 60 µm, respectively, were fabricated by laser photolithography followed by RIE of Si. Subsequent etchings of the BOX either in BOE or in 50% HF vapors were used for membrane suspension. The laser lithography processes were completed in a Kloe Dilase 650 Laser Writer and two different laser spots were used to ensure good membrane definition in the minimum working time: 1 µm for lengths < 15 µm, and 10 µm for > 17.5 µm.

In the first case, BOX etching must be followed by a critical point drying (done in a Tousimis CPD) to prevent membrane collapse caused by surface tension forces during the drying process. The sample transfer between both processes is critical to avoid membrane

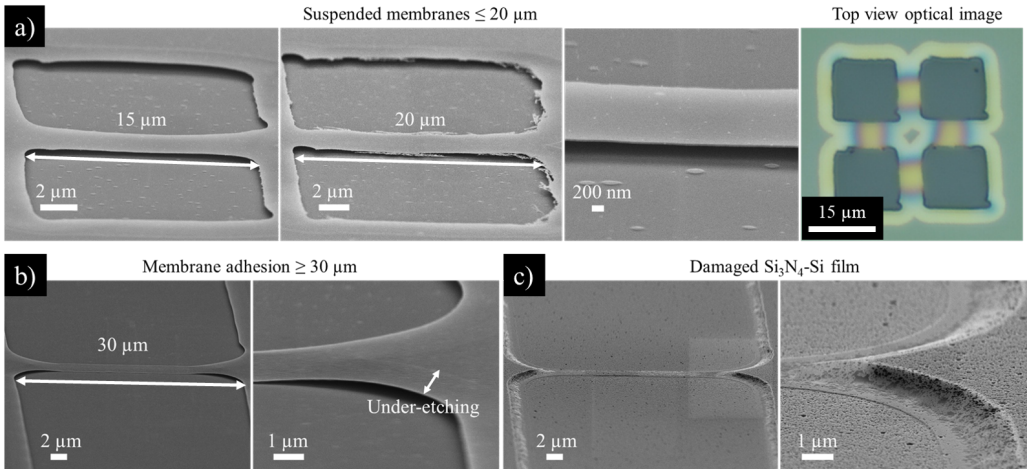


Figure 6.11: SEM and optical images of membrane release in SOI samples with the BOE approach. a) Suspended 50 nm thick Si films with lengths $\leq$ 20 µm by BOE. The membrane deflection increases with their length. The optical image shows the color change due to membrane deflection (the dark green areas are supported by the BOX). b) Collapsed membranes with lengths $>$ 20 µm done with BOE. c) Collapsed membranes with lengths $>$ 20 µm and a 100 nm thick Si_3N_4 as mechanical support. A 30 min etching in BOE damages the Si_3N_4 significantly.

collapse. To accomplish that, teflon holders were used to keep the sample wet during the transfer. Figure 6.11 shows the results obtained with this procedure. Membranes with lengths below 20 µm could be successfully suspended. However, membranes with lengths above 20 µm collapsed. From the images, it also evident that the membranes exhibit some deflection downwards indicating that their stress is not tensile enough the keep them straight once released. The addition of a Si_3N_4 layer on top of the membranes was expected to introduce tensile stress, helping to maintain the membrane flat and possibly enabling the release of longer than 20 µm membranes Figure 6.11c. The fabrication of these samples was similar to the process explained above but adding a 100 nm thick Si_3N_4 deposited on top of Si. However, the results showed that Si_3N_4 was significantly damaged after a 40 min exposure to BOE. Even though Si_3N_4-SiO_2 selectivity is high, Si_3N_4 is slowly attacked by HF [189], [190]. Thus, the long etching times needed to complete the process precluded the use of this solution.

The second approach to prevent membrane collapse involved the use of HF vapors. As no liquid is involved in the process, the CPD process can be avoided in this case. The chips were placed on a teflon basket with holes and placed above 50% HF solution at RT. All membranes released with this process collapsed. This could be justified by the fact that water is a byproduct of the SiO_2-HF etching reaction [191], which can condense under the membrane during release. Furthermore, some damage was observed in the membranes even though HF etching near RT is selective to silicon [192], [193].

The results using BOE and CPD validated a procedure to fabricate ultra-thin Si membranes by patterning the SOI chips from the topside. An alternative route based on topside KOH etching was also developed (see Appendix B).

6.2.2 Thermoreflectance device fabrication

The thermoreflectance device consists of a rectangular suspended membrane with a gold disk at its center (see Figure 6.12). On the sides, a gold frame marks the membrane limits. The gold disk serves as a transducer to absorb the heat from the pump laser and as a reflective material to ensure a large signal of the reflected probe laser. Some membranes were designed without the central gold disk to be later used for bridge measurements (see Section 6.3). Since the membrane is suspended, all the heat dissipated by the transducer flows through the Si film. The gold frame serves to thermalize the ends of the membrane.

The device fabrication was divided in 4 main steps: substrate cleaning, metal patterning, nanostructuration of Si and membrane release (see Figure 6.12). The metal was patterned before nanostructuring Si to ensure the flatness of the metal transducer and to simplify the thermal model (i.e. the underlying Si is not nanostructured and can be considered to behave as a capacitive element). The fabrication was carried out at the chip level to maximize the throughput of experimental resources. The chips cleaning was done with acetone followed by IPA and later with oxygen plasma. Then, the gold disk and frame were defined with laser lithography. Four different membrane lengths (frame gap

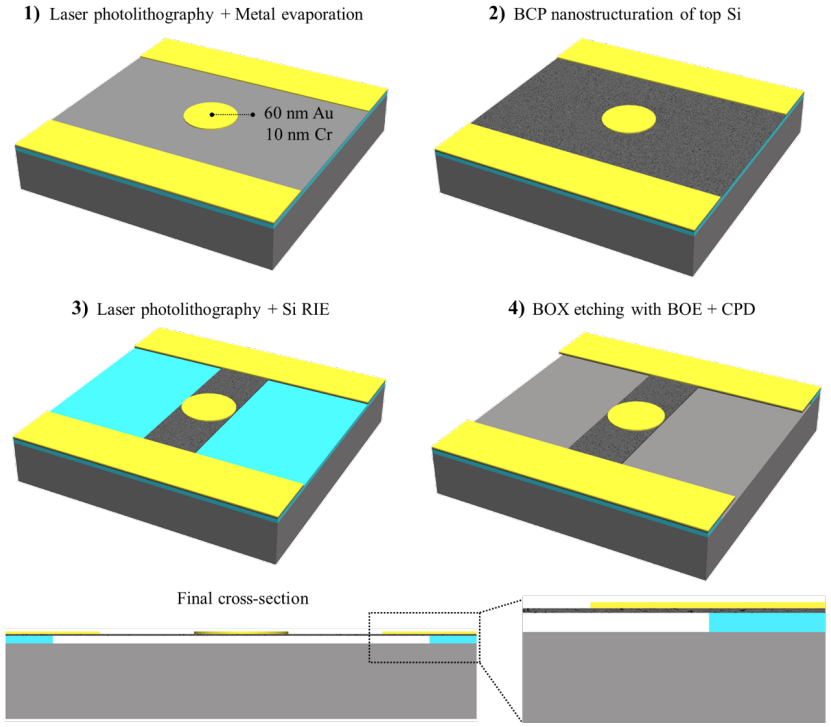


Figure 6.12: Scheme of the fabrication process of the thermoreflectance device. 1) Laser photolithography followed by metal evaporation and lift-off to the define the metallic layout (gold disk and frame for thermalization). 2) Nanostructuration of Si. 3) Laser photolithography and RIE to define the membranes (5 µm wide and 12.5, 15, 17.5 or 20 µm long). 4) Etching of the BOX by BOE followed by critical point drying to suspend the membranes. The final cross-section of the device shows the under-etching profile below the frames.

distance) were defined: 12.5, 15, 17.5 and 20 µm. The patterning of the central 5.5 µm in diameter disks had to be optimized to compensate for the laser overshoot and to achieve perfectly circular shapes. After optimization, accurate and circular disk with diameters of $\sim$ 5.5 µm were achieved. Next, a bilayer of 10 nm of Cr and 60 nm of Au was deposited by evaporation. The Cr layer is used as an adhesion layer and the gold film is used as a transducer in the thermoreflectance measurements. A final metal pattern was defined through a lift-off process. Later, the Si film was nanostructured following the procedures in Section 5.1 and Section 5.2. Since the structure is not yet suspended and the chip dimensions are 1x1 cm^2, no adjustments to the spin coating of the BCP were required. After that, a second laser lithography followed by a RIE was used to define the patterned Si membranes (see Figure 6.12 3). Lastly, they were released by removing the BOX in BOE. Rinsing in water with IPA and critical point drying (CPD) were crucial to prevent the membranes from collapsing. As seen in the cross-section scheme of the final device (Figure 6.12 bottom), some under-etching below the gold frame was present and later taken into account in the thermal model of the devices.

Representative SEM images of 15 µm long membranes with different etching depths are shown in Figure 6.13. This fabrication procedure successfully fabricated nanostructured Si with 57 nm cylindrical period for every membrane length. The fabrication using other BCP configurations (C46, C35 and L37) was not successful due to the low mechanical robustness of the membranes. In both cylindrical cases, the membranes became too

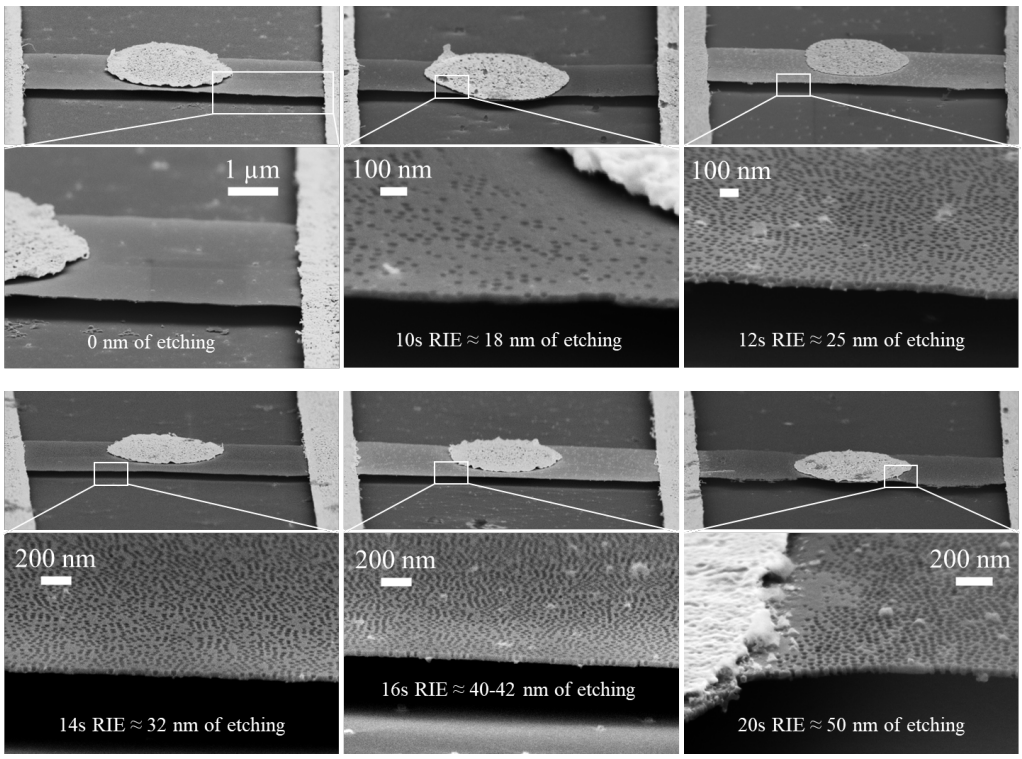


Figure 6.13: SEM images of the final 15 µm long membranes with gold transducer and frame and different etched depths. The through holes do not compromise the mechanical robustness on the C57 BCP.

porous and they would collapse. This also happened with L37 for etching depths beyond 10 nm (out of 50 nm). Therefore, characterization results were only possible on the C57 patterned set of membranes.

6.2.3 Simulations and thermal model

The thermoreflectance thermal model was defined in COMSOL and exposed to modulated heat with the laser pump. Exploiting the symmetry of the system, the model was simplified to a quarter of the membrane, as shown in Figure 6.14. Therefore, the boundary conditions for symmetry boundaries are set to zero heat flux. The model also includes a part of the bulk Si below the metal frame to evaluate its contribution on the overall response of the transducer. It also includes the $\sim$ 3 µm of the suspended thin Si/metal frame. The model discards convective effects because the measurements are to be in vacuum. The bulk side temperature is set to ambient temperature (T_{amb}), as are the initial conditions.

COMSOL simulations used the frequency domain package, as thermoreflectance is based on FDTR, whereas the time domain package was used specifically to study the time response of the system. The time response are more computationally demanding but have they allow to obtain its cut-off frequency, which can be calculated as the inverse of τ (the time at which the temperature reaches 2/3 of its thermalized value). Exciting the system at frequencies above the cut-off frequency results in lower amplitudes of the reflected signal. In terms of phase shift between pump and probe, the frequency region where the phase exhibits its steepest change is centered around this cut-off value (i.e. region with greatest phase sensitivity). Thus, obtaining a precise approximation to this value is key to learn the range of frequencies that are most suitable for the thermoreflectance measurement. The transient results on a 5 x 15 µm^2 membrane with a thermal conductivity of 3 W/m·K are shown in Figure 6.15. The right plot shows the device temperature map for different times. An exponential fitting gives a cut-off frequency of

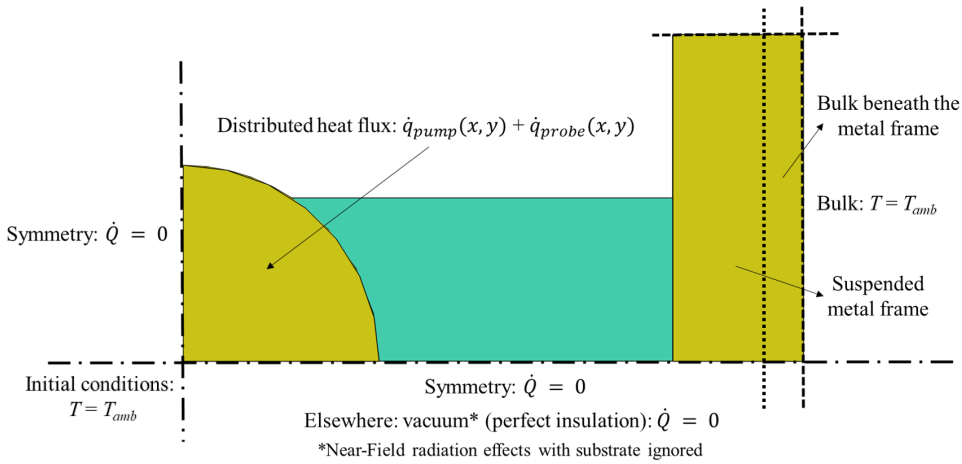


Figure 6.14: Scheme of the boundary conditions applied to the thermoreflectance system in COMSOL model. The geometry is limited to a quarter of the membrane for symmetry reasons.

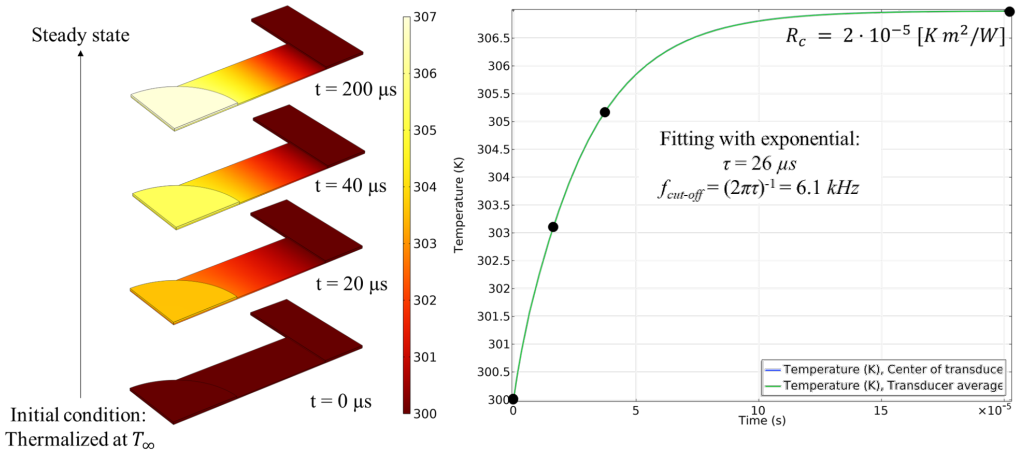


Figure 6.15: Mean transducer temperature versus time of a 5 x 15 µm^2 membrane with a thermal conductivity of 3 W/m·K. The exponential fitting gives a τ= 26 µs which results in a cut-off frequency of 6.1 kHz.

$\sim$ 6.1 kHz. This value corresponds to the specific geometry and κ used in the model. While different geometries and κ values will yield different cut-off frequencies, it serves to define the frequency range to carry out measurements. In this case, the 1 to 100 kHz range should cover the range where most of the phase shift will occur.

The frequency domain simulations, on the other hand, allow the evaluation of how various parameters influence the phase shift observed across different frequencies. Furthermore, they also serve to validate the thermal model used to fit the phase shift curves (i.e. to finally obtain the thermal conductivity of the film). As explained in Section 2.4.2, the quadrupole method was used to develop the system thermal model. Due to the difficulty parameterizing certain system components (such as the bulk substrate and the suspended part of the gold frame), the model was simplified to include only the contributions from the gold transducer, the underlying bare Si, the thermal contact resistance between them, and the Si membrane. This simplification is particularly justified for fully etched films, where time-domain simulations indicate that $\sim$ 96 % of the total temperature gradient across the membrane, implying that the model introduces an estimated fitting error of only $\sim$ 4 %. Also, both gold and the underlying Si are assumed to be thermalized at a uniform temperature and introduced in the thermal model as capacitors only, implying that heat storage dominates over heat conduction. Finally, the membrane is considered to be diffusive, with both resistive and capacitive components. All this leads to the following system matrix that relates the temperature, θ_0, and heat flux, ϕ_0, at the transducer with the temperature, θ_{out}, and heat flux, ϕ_{out}, at the bulk:

$$\begin{bmatrix}\theta_0\\ \phi_0\end{bmatrix} = \overbrace{\begin{bmatrix}1 & 0\\ C_1\cdot s & 1\end{bmatrix}}^{\text{Gold disk}} \cdot \overbrace{\begin{bmatrix}1 & R_C\\ 0 & 1\end{bmatrix}}^{\text{Disk-Si interface}} \cdot \overbrace{\begin{bmatrix}1 & 0\\ C_2\cdot s & 1\end{bmatrix}}^{\text{Underlying Si}} \cdot \overbrace{\begin{bmatrix}D_{11} & D_{12}\\ D_{21} & D_{22}\end{bmatrix}}^{\text{Membrane}} \cdot \begin{bmatrix}\theta_{out}\\ \phi_{out}\end{bmatrix} =$$

$$= \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \cdot \begin{bmatrix} \theta_{out} \\ \phi_{out} \end{bmatrix} \tag{6.3}$$

being the diffusive matrix:

$$\begin{bmatrix} D_{11} & D_{12} \\ D_{21} & D_{22} \end{bmatrix} = \begin{bmatrix} 1 & \dfrac{tanh\,(K(s)L)}{\kappa AK(s)} \\ \kappa AK(s) \cdot tanh\,(K(s)L) & 1 \end{bmatrix} \tag{6.4}$$

In these equations s corresponds to the Laplace variable, s = i · ω, C_1 and C_2 to the capacitance of gold and bare Si, R_C to the contact resistance and L and A are the length and cross-section area of the membrane.

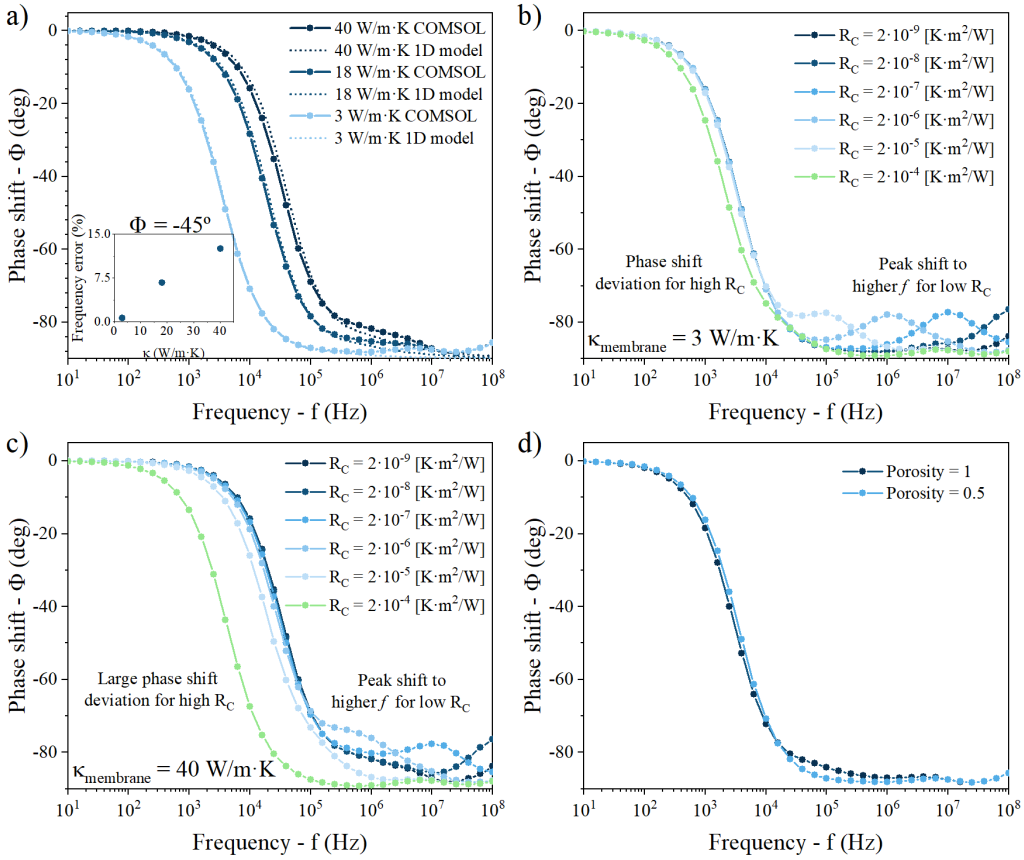


Figure 6.16: Phase shift versus frequency obtained with COMSOL simulations compared to the thermal model curve. Phase shift versus frequency plot: a) COMSOL simulations and the thermal model comparison for different κ values. As κ increases there is a larger divergence between both curves (inset: frequency error between simulation and model for Φ = -45º); b) comparison for different contact resistances and κ = 3 W/m·K; c) comparison for different values of contact resistance and κ = 40 W/m·K; and d) film porosity influence.

To solve these equations, some assumptions were made regarding the bulk side of the system. According to COMSOL simulation results, the bulk part of the chip attains less than 10% of the overall thermal gradient in samples with high thermal conductivity. Thus, a constant temperature is assumed ($\theta_{out} = 0$) on the bulk side of the membrane:

$$\frac{\theta_0}{\phi_0} = \frac{N_{12}}{N_{22}} = \frac{\frac{tanh\,(K(s)L)}{\kappa AK(s)}(1 + R_C C_2 s) + R_C}{\frac{tanh\,(K(s)L)}{\kappa AK(s)}(C_1 s + C_2 s + R_C C_1 C_2 s^2) + R_C C_1 s + 1} \tag{6.5}$$

The frequency domain simulations compared with the fitting model are shown in Figure 6.16. Figure 6.16a reflects the higher divergence between the simulated phase shift and the thermal model fitting as the thermal conductivity of the membrane increases. This is a consequence of neglecting the bulk contribution in the model, which introduces an error that becomes increasingly significant as the membrane thermal conductivity increases. When the thermal conductivity of the film is 3 W/m·K a perfect match is found between the thermal model and COMSOL simulated phase shift results. Thus, the simplified model yields larger κ errors for shallow surface decoration or bare samples (which have higher thermal conductivities). To address the limitations of the simplified model, a combined fitting approach can be employed: an initial estimate of the thermal conductivity (κ) can be obtained with the simplified model, which is then refined through COMSOL simulations incorporating the full geometry and bulk contributions.

Another important parameter for calculating κ is the contact resistance between the transducer and the film, R_C. Figure 6.16b and c) show the influence of contact resistance on the phase shift response as a function of frequency for different membrane thermal conductivities. For lower κ membranes, the phase shift changes occur for $R_C \geq 2{\cdot}10^{-4}$ K·m^2/W whereas, for higher κ membranes, significant changes already occur for $R_C \geq 2{\cdot}10^{-5}$ K·m^2/W. Beyond $1{\cdot}10^5$ Hz, the phase shift peak shifts towards higher frequencies as R_C decreases. Nonetheless, as long as $R_C < 2{\cdot}10^{-4}$ K·m^2/W (or $R_C < 2{\cdot}10^{-5}$ K·m^2/W for higher κ membranes), the frequency range to explore is not affected by R_C. Finally, plot d) evidences that the phase shift is slightly influenced by the film porosity. The membrane characterization results with thermoreflectance are detailed in Section D.1.

6.3 Bridge method

The third thermal characterization technique used in this thesis is the bridge method explained in Section 2.4.3. This work was carried out in the scope of an internship in the *Department Physik* of the University of Basel.

6.3.1 Bridge method devices and membrane transfer

The device used to characterize the nanostructured Si films is based on a device developed by the University of Basel, consisting of two suspended nitride membranes supported by elongated nitride beams, each incorporating an integrated platinum heater (Figure 6.17). The original gap between the platforms (< 3 µm) can be enlarged with FIB etching to define gaps in the 5 and 10 µm range. Devices with large gaps were used to measure membranes with high conductivity (i.e. with shallow nanostructuration) to ensure a higher contribution of the membrane conductance to the overall thermal system.

The membranes without the central gold transducers described in Section 6.2.2 were

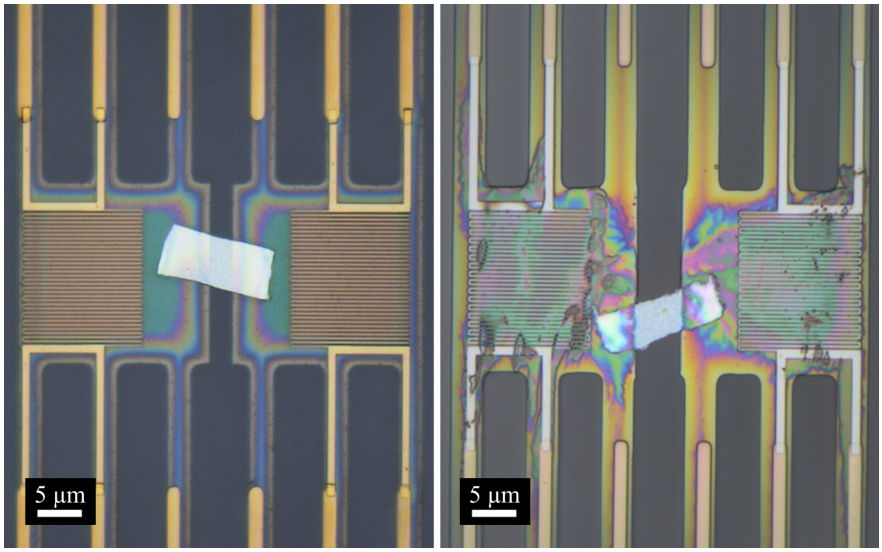


Figure 6.17: Optical images of two bridge devices with nanostructured Si membranes deposited on top. The narrow metal meander on the platforms are designed to exhibit higher resistance in these regions, thereby dissipating most of the heat there.

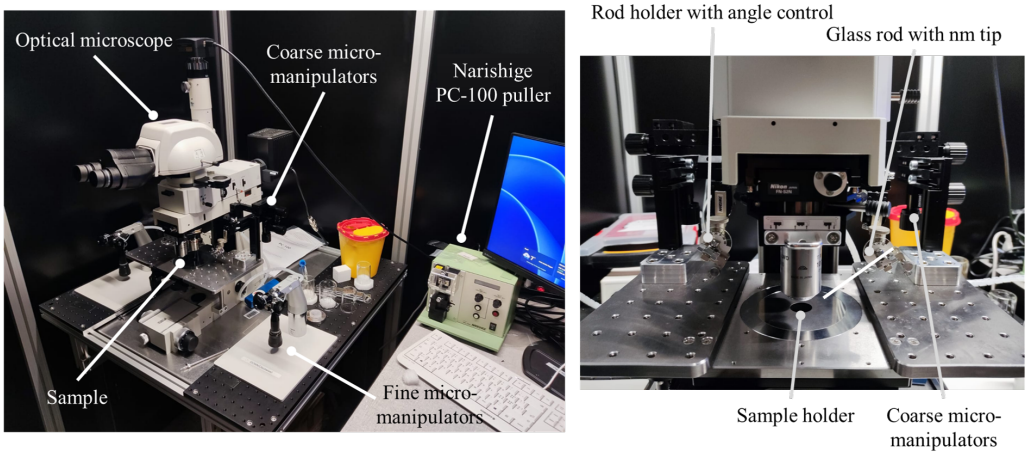


Figure 6.18: Images of the setup used for membrane transfer. The membranes are cut and deposited using two glass nanometric tips controlled with micro-manipulators. The process is monitored with an optical microscope at 100X amplification.

used in these devices. These membranes were transferred onto the bridge devices using an optical microscope and two Narishige micro-manipulators (see Figure 6.18). The process begins with the glass tips preparation. A glass rod was placed in a Narishige PC-100 puller, where it was heated by a coiled heater while being pulled downward by gravity, forming narrow nanoscale tips at the fracture point. These two fine tips are then introduced in the rod holder of the micro-manipulators, subsequently adjusting their angle. The first step in transferring the membranes consisted of detaching them from the chip

by pressing with the tips on both sides at the point where the membranes connect to the non-suspended regions. During this process, the second tip was placed beneath the center of the membrane to prevent it from adhering to the substrate after one side was cut. Interestingly, the mechanical properties of the membranes showed significant differences depending on the depth of the holey pattern. Non nanostructured samples exhibited high rigidity and tore immediately from the non-suspended part following the cut on one side. In contrast, the fully nanostructured membranes required tearing from both sides using the tips and demonstrated high flexibility withstanding 180^{o} bending (i.e. complete folding) without any fractures. Partially etched samples exhibited this same behavior, with higher flexibility for deeper etchings. The second step of the transfer was depositing the membranes on the platforms (Figure 6.17). The membranes were attached to the platforms via electrostatic forces. Perpendicular alignment was challenging due to electrostatic forces with the tips. However, this misalignment could be later taken into account in the simulations. To ensure a good thermal contact, membranes were pushed down with the tips against the platforms until fringe patterns of the nitride underneath were clearly visible on the membrane. Finally, the chips were glued and wire bonded to a custom PCB.

6.3.2 Bridge method characterization

The bridge method characterization, explained in Section 2.4.3, measures G_{Sample} and G_{Beam}^{Side} of both sides of the chip using Equation 2.24 and Equation 2.23. For this purpose, the PCB hosting the chip with the devices under test is introduced in a vacuum chamber with temperature control from 20 to 350 K, and connected to a Keithley Sourcemeter. Before starting the characterization, the PCB is stabilized at a given temperature. First, the left platform is used as a heater and powers between 0.1 and 3.5 µW are dissipated while the resistance of both platforms is monitored. With this data dR_{Heater}/dP and dR_{Sensor}/dP are obtained at each temperature. Then, a linear fit of the heater resistance vs temperature is done to calculate R_0 (the resistance at a specific temperature when no current is applied). Finally, dR_{Heater}/dP, dR_{Sensor}/dP and dR_0/dT are used to calculate G_{Sample} and G_{Beam}^{Side}. In this procedure, having an accurate dR_0/dT fit is of the utmost importance, as it is shown in Figure 6.19. If a linear relation between resistance and temperature is assumed, a constant dR_0/dT is found. However, platinum resistance is not linear for < 100 K and dR_0/dT was calculated to accurately define the relation.

To evaluate the importance of dR_0/dT calculation, Figure 6.20 shows the conductance values obtained with Equation 2.24 and Equation 2.23 using the linear R_0 vs T plot and the analytical derivative (polynomial fit). It is clear that errors in dR_0/dT lead to significant changes in the conductance values obtained. After the correction, the curve of this representative sample (50 nm thick Si film with complete etching) follows the expected trend for a Si structure with minimum features smaller than 25 nm ([86], in this case the minimum features correspond to the Si neck sizes). It is worth mentioning the significant difference between the left-to-right and right-to-left sample conductance observed in the uncorrected results. Again, using the corrected dR_0/dT for both platforms removes this discrepancy and both measurements (left-to-right and right-to-left) converge.

As it was mentioned before, membrane perpendicular alignment with respect to the platforms was not possible. To evaluate the angle influence on the measured sample thermal conductivity, a COMSOL model was used to calculate the specific conductance

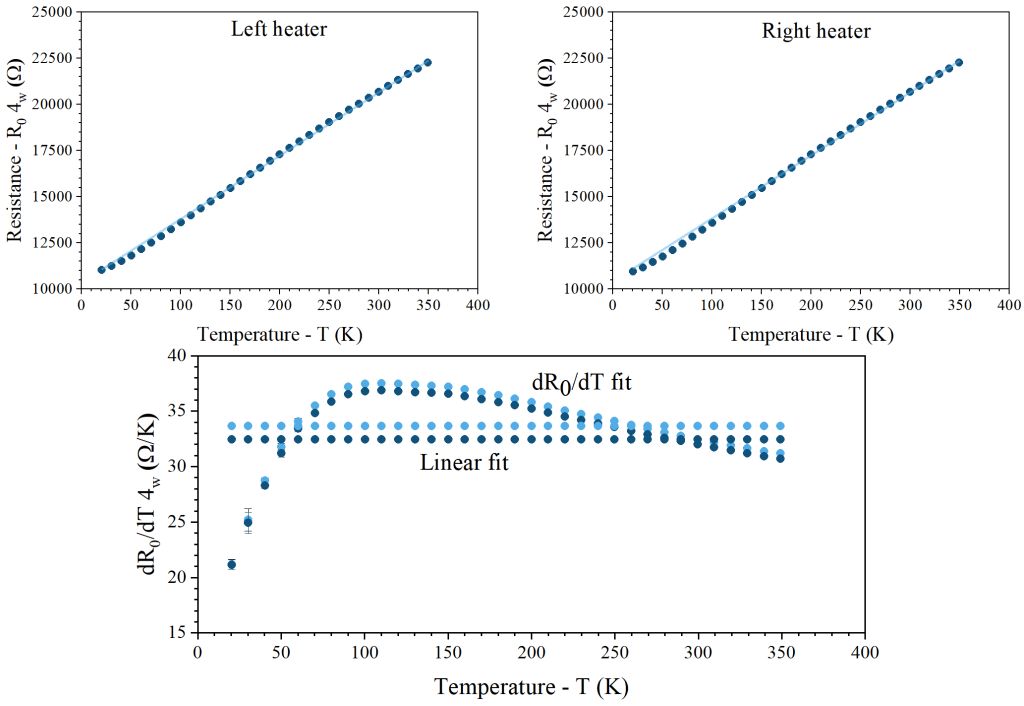


Figure 6.19: (Top) Representative plots of heater resistance as a function of temperature, showing minor nonlinearities. (Bottom) dR_0/dT calculations for data shown in top plots.

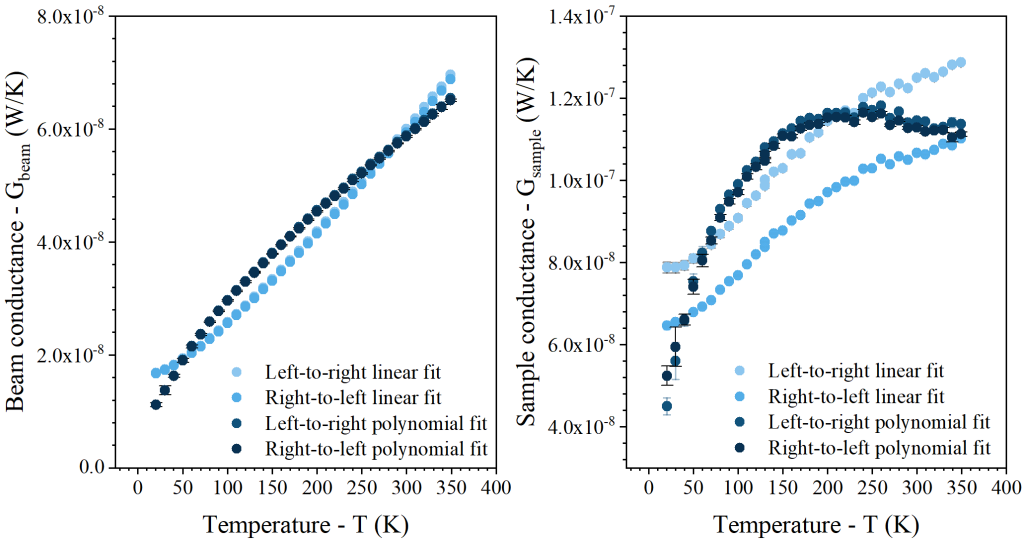


Figure 6.20: Plots of the calculated beam and sample conductance versus temperature on a 50 nm thick Si membrane with complete etching. Using a linear fit to calculate dR_0/dT results in significant deviations in the temperature dependence of the conductance.

corrections for each angle (see Figure 6.21). These simulations determined that the impact was strongly dependent on the dimensions of the membrane. As expected, the narrower and longer the membrane, the stronger the impact of the rotation in the conductance. On the other hand, the wider and shorter the membrane the smaller the variation of the conductance even for tiltings $> 45^{o}$. Therefore, the conductance of each sample was measured and subsequently corrected using simulation results.

Lastly, the sample conductivity is calculated from the measured conductance values and the membrane geometry. The thermal conductivities from the 50 nm thick Si samples with different degree of nanostructuration (i.e. different etched depths), from bare to completely etched Si, are shown in Figure 6.22. At this point, it needs to be highlighted

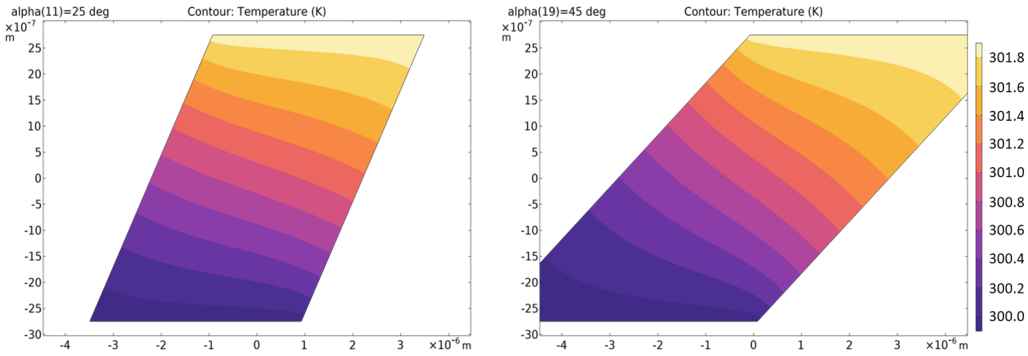


Figure 6.21: COMSOL simulation results of the temperature profile of a membrane with different rotations.

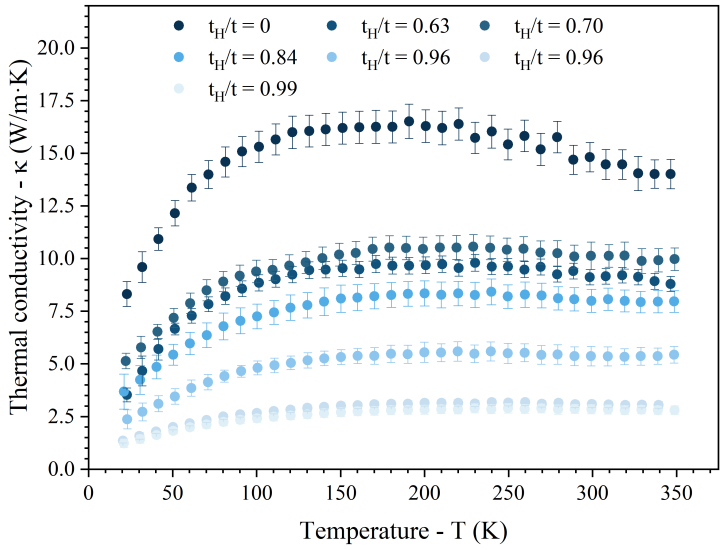


Figure 6.22: Thermal conductivity versus temperature for different etched samples from bare 50 nm thick films ($t_h/t = 0$) to fully etched ($t_h/t = 1$) with the 57 nm cylindrical pattern. Note that the $t_h/t = 0.70$ sample should have a lower κ than $t_h/t = 0.63$, but the trend is inverted in the plot. The different contact resistances in these samples are expected to be responsible for this behavior.

that these thermal conductivities also include thermal contact resistance contributions on both sides of the platforms. This implies that the film thermal conductivity is being underestimated. This is expected to be more significant in samples with higher thermal conductivity, where the relative contribution of the contact resistances is higher. However, the results of fully etched film also had a significant κ change across the thermal range. The first measurement at RT yielded a conductivity of $\kappa = 1.1$ W/m·K, while after exposing the device to the full temperature range (20 to 350 K) the measurement evolved until reaching and stabilizing to $\kappa = 2.5$ W/m·K at RT. This thermal conductivity evolution is attributed to a reduction of the thermal contact resistance induced by the exposition to the full temperature range. This also demonstrates that low κ films can also be highly underestimated. The laser heating method developed (see next section), allows eliminating the thermal contact resistance from the sample thermal conductivity.

6.3.3 Bridge method with laser heating characterization

As explained in Section 2.4.3.1, coupling laser heating of the sample at different positions along the length of the sample with the bridge device features the ability to measure the film's thermal conductivity without the thermal contact resistance. The setup used for these measurements was the same as in the previous section, as the vacuum chamber includes a small glass window that allows the laser beam to pass through. The characterization was done at RT and the laser movement across the membrane was automated with a python program. Figure 6.23 shows some example optical images of the laser beam on a measured sample. The measurement starts with manually positioning the laser beam over one of the membrane-platform contacts. After that, the program automatically moves the laser beam through the sample with a specified step until reaching the opposite membrane-platform contact. This procedure was used to set the focus positions at the beginning and end of the membrane to ensure that the laser beam was aligned with the center of the membrane. For each measurement, the laser heated up the sample with different powers while ΔTs were monitored on the right and left platforms through its integrated temperature sensors (heaters). Subsequently, it is possible to calculate the power flowing towards each heater. Therefore, in a next step, we can dissipate that exact

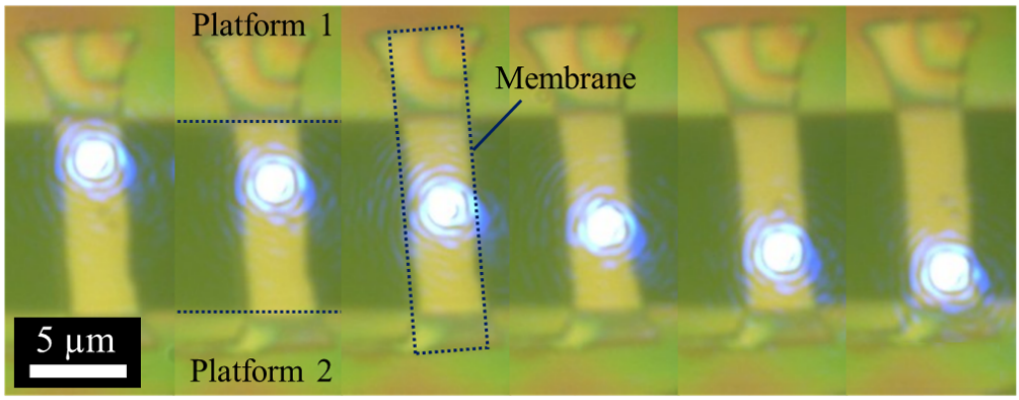


Figure 6.23: Sequence of optical images showing the laser heating at different positions along a 50 nm-thick Si membrane. In this particular case, the scan covered 10 µm with 0.5 µm steps. The different elements of the device are highlighted on the images.

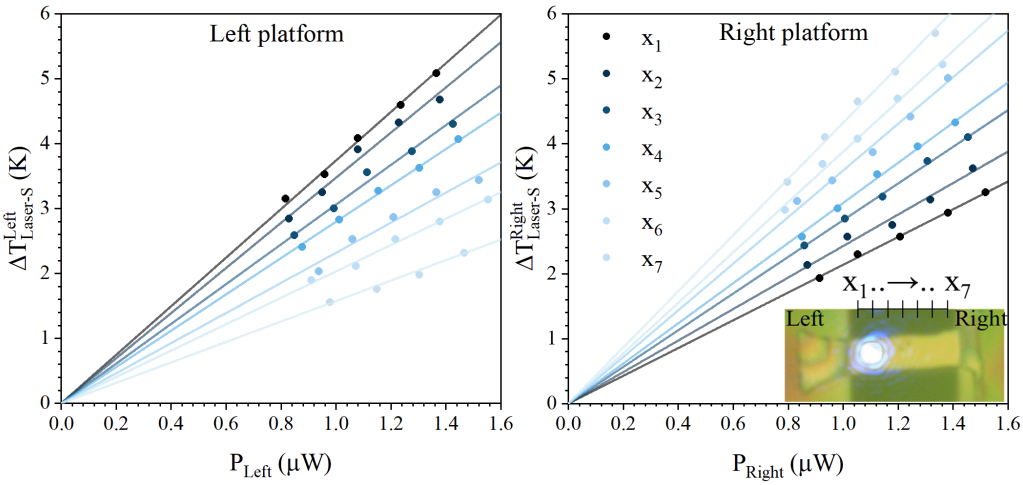


Figure 6.24: $\Delta T^{Side}_{Laser-S}$ versus laser power observed at each platform (left and right) as a function of the laser power on each side (P_{Side}). The inset shows the corresponding x positions on the membrane.

amount of heat on each heater, one after the other, to compensate the heat flow produced by the laser beam on each platform. After doing this independently on each heater, the system reached the second steady state (see Figure 2.14) where T^{*}_{Laser} was measured and T_{Laser} of the first thermal state was calculated. In the experiment, this compensation step was done on each side (i.e. compensating first P^{Left}_{Laser} and then P^{Right}_{Laser}), to check whether the same T_{Laser} was obtained regardless of the platform used for power compensation. Once this process was completed, the python control moved the laser spot to the next measurement position along the sample and restarted the characterization cycle.

$\Delta T^{Side}_{Laser-S}$ as a function of laser power (P_{Side}) on the different x positions are shown in Figure 6.24. The measurements were performed using different laser powers and for each laser beam position along the sample. Using this method, the value is obtained from the slope of a linear regression based on five points, rather than from the ratio $\Delta T^{Side}_{Laser-S}/P_{Side}$ calculated from single measurements. This reduces the error in the $\Delta T^{Side}_{Laser-S}/P_{Side}$ value. Next, the obtained values are plotted as a function of the x position along the membrane to find the slope of the curve (see Figure 6.25 for two samples which correspond to a half- and a completely-etched sample). When the laser heats the left side of the membrane, the left sensor measures a higher temperature increase, while the right sensor measures a smaller one. As the laser beam moves along x, this pattern changes until the right sensor measures higher temperatures than the left one, resulting in an X profile that intersects at a specific position. When the laser beam approaches the platform's edge, the sample's absorbance α changes (up to 10%) because part of the heat is dissipated on the platform itself, and not on the membrane. These outliers are not considered in the slope calculation because Equation 2.28 can not be applied. Both slopes are equivalent to R_{Film}/L (where L is the length of the membrane, see Equation 2.28) and, thus, these values were used to calculate the resistance of the film. Note that both slopes (left and right) are equivalent, with their difference consistently remaining below 0.5%. This is expected because the film is symmetric and isotropic. The point where both profiles cross indicates the position where thermal resistances towards each side are

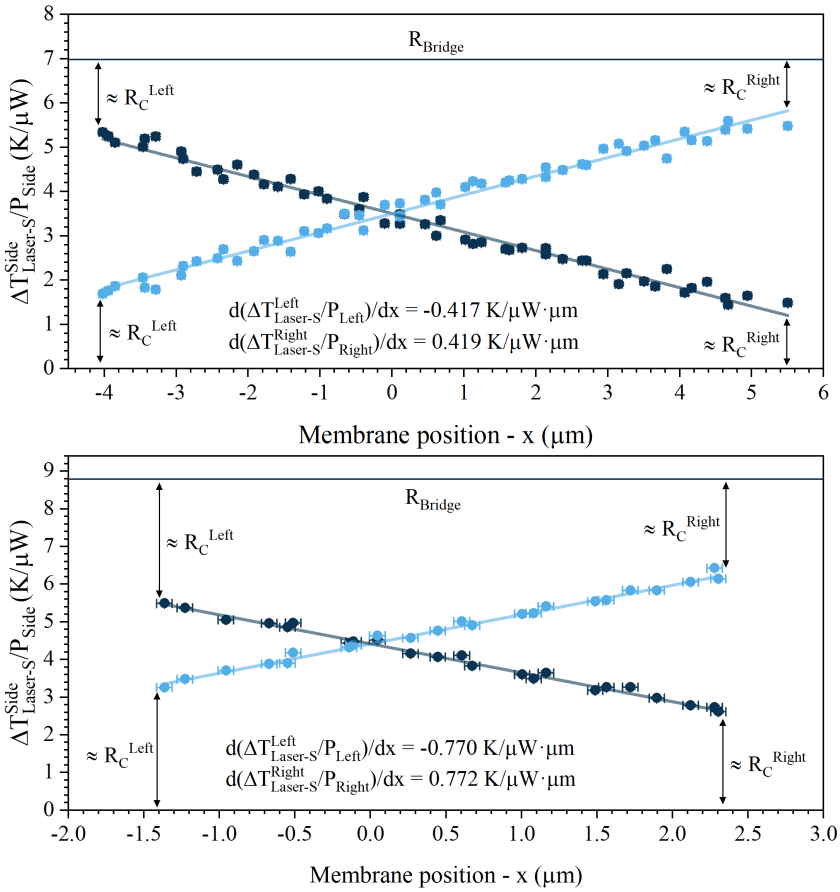


Figure 6.25: $\Delta T^{Side}_{Laser-S}/P_{Side}$ as a function of the laser beam position on the membrane for two different samples (half etched -top- and completely etched -bottom-). The X-like profile, showing equivalent slopes in both sides (left-to-right and right-to-left characterizations), demonstrates the isotropy of the film thermal conductivity.

equivalent. As this does not correspond to the membrane's center, it indicates that contact thermal resistances are different on each side. Actually, the thermal contact resistances for each side can be determined by extrapolating the total resistance measured with the bridge method (i.e. $R_{Bridge} = R_C^{Left} + R_{Film} + R_C^{Right}$), as shown in Figure 6.25. In this case, however, R_C values are slightly overestimated because the measurements were not carried out over the film–platform contact, since the strong absorbance variations would affect the results, as explained above.

After obtaining precise film thermal resistance values at 300 K, the thermal conductivity measured with the bridge method can be corrected across the entire temperature range, assuming that the contact resistances remain relatively constant with temperature once stabilized. This is done with the following calculation:

$$\frac{1}{G_{Contacts}} = \frac{1}{G^{Bridge-300K}_{Sample}} - \frac{1}{G^{Laser-300K}_{Film}} \rightarrow \frac{1}{G_{Film}} = \frac{1}{G^{Bridge}_{Sample}} - \frac{1}{G_{Contacts}} \tag{6.6}$$

where $G_{Sample}^{Bridge-300K}$ and $G_{Film}^{Laser-300K}$ are the thermal conductances measured with the bridge and laser methods at 300 K, respectively (i.e. *Sample* refers to a measurement of the entire system, including contact resistances, whereas *Film* refers to a result corresponding solely to the film itself). After obtaining $G_{Contacts}$, G_{Film} can be calculated for each temperature using the G_{Sample}^{Bridge} values (shown in Figure 6.22). The corrected results of films with different etching depths are shown in Figure 6.26. The corrections reached factors of up to 3 in some films, indicating the significant contribution of the contact resistances. Furthermore, no clear trend was observed between the correction factor and the etched depth of the film. Twin samples of each membrane (i.e. the membrane closest to the one transferred onto the bridge devices) were used to extract lamellas and imaged by Scanning Transmission Electron Microscopy (STEM) to precisely measure their average depths, thicknesses, diameters and hole densities (see Figure 6.27). As the average thickness of the films ranged between 40 and 45 nm, the hole depth vs Si thickness ratio (t_H/t) parameter was defined to compare the results throughout the different samples. Figure 6.26 reveals two clear trends in terms of the thermal conductivity versus t_H/t. First, the thermal conductivity diminishes as the t_H/t ratio increases, which is expected, as a higher t_H/t ratio indicates that the nanometric holey pattern has a greater influence in the overall heat conduction, resulting in a greater phonon transport suppression through boundary scattering. The second trend is associated with the temperature dependence of the thermal conductivity curve. In this case, a clear dome-like curve is observed for the reference film ($t_H/t = 0$), while this behavior is less pronounced as t_H/t increases. This behavior is in good agreement with previous observations found both in NWs and holey films with different periods [80], [86]. The different behaviors observed for varying t_H/t ratios in the films are due to the different contributions of

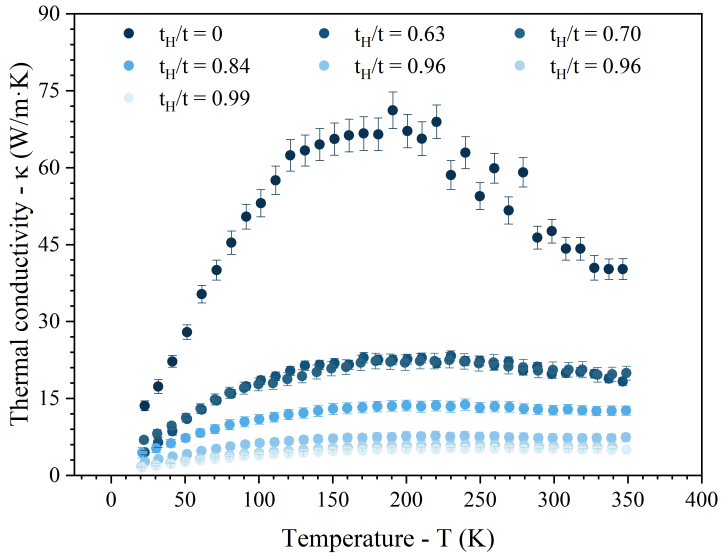


Figure 6.26: Thermal conductivity versus temperature for 50 nm thick films with different etching depths (from not etched t_h/t=0, to fully etched, t_h/t=1). All films are nanostructured with 57 nm pitch cylindrical patterns. Thermal conductivity measurements correspond to the corrected bridge method, removing the thermal contact resistance obtained with the laser heating method.

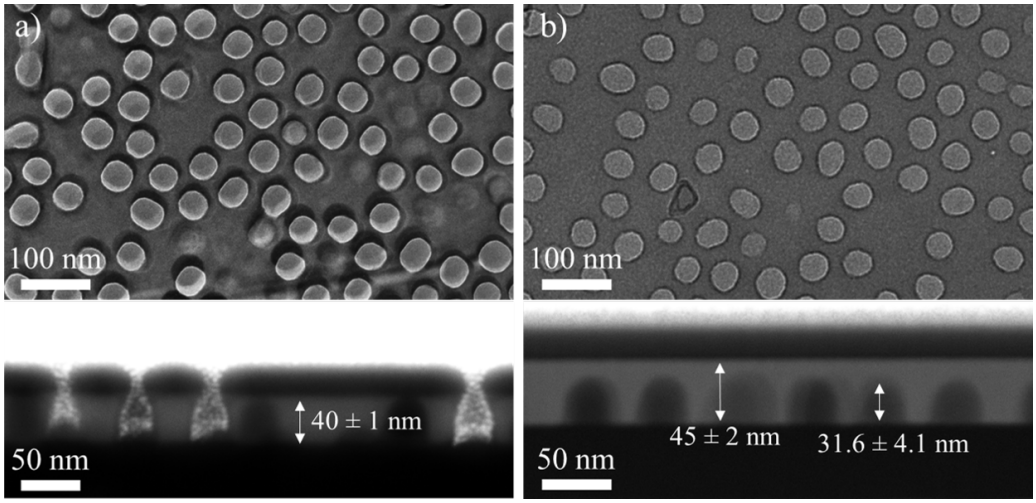


Figure 6.27: STEM images of two 50 nm thick Si films nanostructured with a 57 nm pitch cylindrical pattern. The left films (a) is completely etched ($t_H/t = 0.99$), whereas the film on the right (b) was partially patterned ($t_H/t = 0.70$). These STEM images were used to measure the average diameters, depths and hole densities of the different films for further calculations. The carbon protection layer clearly fills the through holes of the pattern on the film on the left (a).

phonon boundary scattering and phonon-phonon scattering for each case. For $t_H/t = 0$, boundary scattering is minimized and therefore, the initial increase of κ follows the temperature dependence of the specific heat ($\propto T^3$), while the decrease observed above 200 K is attributed to the greater contribution of phonon-phonon scattering at these temperatures. As for the initial increase of κ with temperature, it is also evident that the slope decreases when increasing t_H/t. This may be related to the fact that a smaller nanostructure reduces the phonon group velocities [86], or that at lower dimensionalities phonon boundary scattering becomes frequency-dependent [194]. However, the underlying mechanism of this effect is still not well understood. On the other hand, as t_H/t increases, boundary scattering increasingly dominates heat transport, eventually reaching a point where the phonon-phonon scattering becomes negligible, and almost no decrease with temperature is observed beyond 200 K.

Figure 6.28 summarizes the results of films thermal characterization at 300 K, which correspond to the measurements obtained with the laser method. The κ vs thickness without holes plot reveals a linear relationship. In the κ vs t_H/t ratio plot, we observe the same relationship but with an inverted slope. κ for the bare film and for the fully etched film were calculated to be 46.45 ± 2.20 and 5.14 ± 0.47 W/m·K, respectively. This demonstrates a 9-fold decrease in the thermal conductivity achieved through nanostructuration. The κ value for the bare film is in good agreement with previous simulations and measurements in the literature [195], with reported values around 40-45 W/m·K for films with similar Si thickness. For the holey film case, a κ value of 2.03 W/m·K was reported by *Tang et al.* [80] after nanostructuring a Si film with a 55 nm pitch hexagonal pattern with complete etching. However, the article lacks precise characterization of the contact resistance and κ could have been underestimated, as discussed in Section 6.3.2. Thermal conductivity may also be compared, in terms of film porosity, with the aforementioned

article, which reports a value of 35%. Assuming a hexagonal distribution of holes, the film porosity can be calculated using the following formula:

$$\Phi = \frac{\pi\sqrt{3}d^2}{6p^2} \tag{6.7}$$

where d and p are the diameter and period of holes (from center to center), respectively. As the films with through holes have a pitch of $\sim$ 58 nm and an average hole diameter of $\sim$ 30 nm (the BCP pattern originally has $\sim$ 25 nm - see Section 5.1.1 - but the pattern transfer process enlarges it by 5 nm), the calculated porosity for these films is $\sim$ 24%. The difference in porosity could partially explain the κ differences compared to those of *Tang et al.*. On the other hand, *Lim et al.* [89] reported values between 4

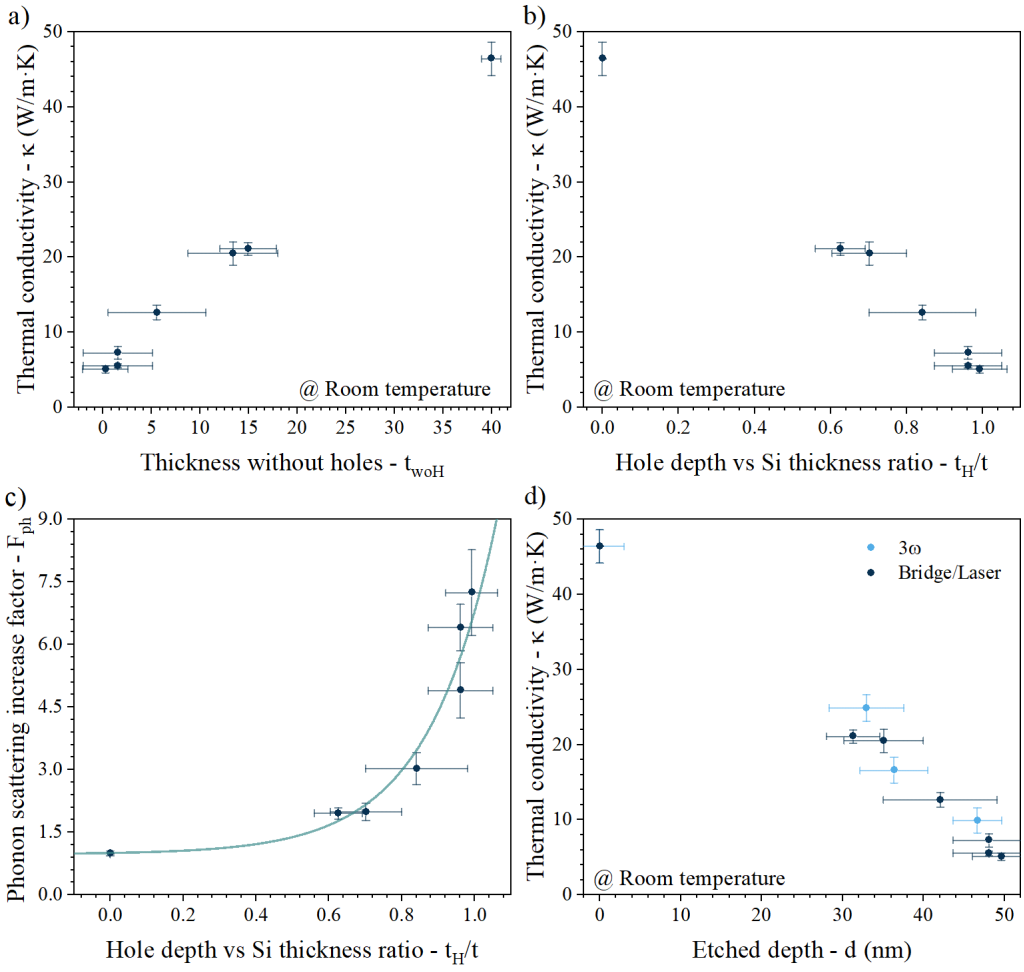


Figure 6.28: Plots of: a) κ vs thickness without holes, b) κ vs t_H/t ratio, c) Phonon scattering increase factor, F_{ph}, vs t_H/t ratio (the fitted curve is plotted to visualize the trend) and, d) comparison of the κ vs etched depth obtained with the 3ω and laser techniques. All the results were obtained at room temperature (300 K). A linear decrease of κ as t_H/t increases is observed, along with an increase of the F_{ph}.

and 7 W/m·K for holey Si films with hexagonal patterns and neck sizes between 24 and 30 nm, which are in good agreement with those obtained in this work (average neck sizes of $\sim$ 27 nm). Furthermore, Monte Carlo simulations by *Hao et al.* [196] reported that a 45-50 nm thick holey film with a square-like pattern and a porosity of 25% should have a $\kappa_{Holey}/\kappa_{Bare}$ ratio $\sim$ 0.11 - 0.12. The $\kappa_{Holey}/\kappa_{Bare}$ ratio of the films obtained in this work is 0.11, indicating good agreement, even though the hole pattern is not a square array but a hexagonal array.

Another important aspect to evaluate is the effect of nanostructuring on phonon scattering. Similarly to what was explained in Section 5.3.1, there are two contributions involved in the reduction of κ: the geometric factor, F_G, and the phonon scattering factor, F_{ph}. In this case, the geometric factor of the films was calculated based on the STEM characterization. A maximum $F_G \sim 1.297$ was calculated for the completely etched holey film, in good agreement with the maximum $F_G \sim 1.290$ that was obtained from the COMSOL simulations on the electrical conductivity (Section 5.3). Using the equivalent of Equation 5.1, the phonon scattering factor can be calculated as a function of the t_H/t ratio (see Figure 6.28c, where the fit serves as a guide to the eye). It becomes clear that increasing the t_H/t ratio further increases phonon scattering, reaching a maximum of F_{ph} at $\sim$ 7.5. Therefore, once the geometrical factor is excluded, this means that the intrinsic thermal conductivity of the fully etched holey Si film is $\sim$ 6.2 W/m·K. Lastly, the κ for a 50 nm thick film can be scaled using t_H/t ratios, allowing comparison with the values obtained from the 3ω steady state method. As shown in Figure 6.28d, good agreement is observed between both methods, demonstrating the reliability of both characterization techniques and the obtained results.

6.4 Chapter conclusions

Nanostructured films with 57 nm pitch cylindrical patterns were successfully integrated onto three different devices/structures, each requiring specific fabrication strategies. 3ω steady state and bridge/laser routes led to successful thermal conductivity measurements that demonstrated a 9-fold decrease of κ after patterning it with a 57 nm pitch cylindrical geometry. The measured κ of the fully etched film was 5.14 W/m·K at RT. Regarding the 50 nm thick bare Si film, the measured κ was 46.45 W/m·K at room temperature. A linear decrease in κ was observed with increasing etching depth. After excluding the geometrical factor and considering only the phononic contribution, this decrease becomes even more pronounced with the etched depth. Moreover, a thermal model capable of fitting the phase-shift measurements obtained with FDTR was also developed.

Chapter 7

Micro-thermoelectric generator based on nanostructured thin films

This chapter presents the fabrication of µTEGs based on 50 nm thick bare and nanostructured silicon thin films with a 57 nm pitch cylindrical pattern. Afterwards, thermoelectric characterization of the films (including open circuit voltage, Seebeck coefficient, and figure of merit) is presented and benchmarked against the µTEGs based on nanowires developed in this work, as well as other Si structures reported in the literature. Lastly, the optimization of the Ti-Si contact for thin films is presented.

7.1 Device design

The design of the thermoelectric generator with nanostructured Si films is based on the layout of the 4X type TEGs that integrate Si NWs or microbeams. The TE element of every design within this first generation of µTEGs is 15 µm long and 1 mm wide. The membranes of these devices include a metal serpentine that serves as a heater or thermometer, allowing operation in test and harvesting modes.

Different designs of the membrane supporting the platform, as well as ancillary elements for the TE material, were included to assess the robustness of the suspended areas (Figure 7.1). The membranes were designed in three configurations: a continuous Si_3N_4 membrane, a piano-like etched membrane, and no supporting membrane. The latter design relies solely on the inner platform itself to enhance mechanical robustness by reducing the suspended area, at the expense of decreased heat management efficiency. In terms of ancillary elements on the TE side of the platforms, different Si_3N_4 supports were included to evaluate robustness. The devices feature 0, 3, 9, or 17 ancillary supports with widths of 5 µm or 10 µm. Reducing the number or size of ancillary elements lowers the thermal conductance of the TE element but increases the fragility of the platform.

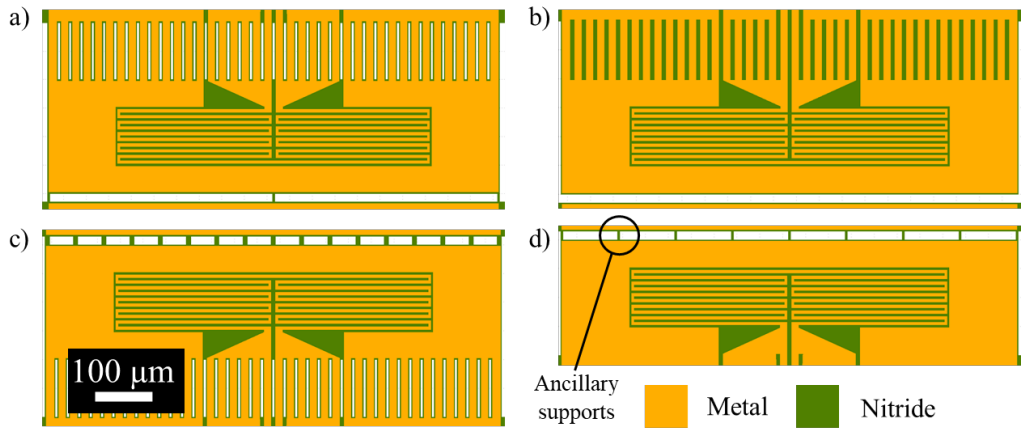


Figure 7.1: Example layouts of µTEGs to evaluate the mechanical robustness as a function of the supporting structures. a) Piano-like membrane with three 5 µm wide ancillary beams at the TE side. b) Continuous nitride membrane with no ancillary beams at the TE side. c) Piano-like membrane with seventeen 10 µm wide ancillary beams at the TE side. d) No supporting membrane and nine 5 µm wide ancillary beams at the TE area. From this point on, designs a) and d) are used to refer to the chip types (i.e. Type A and Type D, respectively).

7.1.1 Device fabrication

The fabrication started with SOI wafers from the same batch used in the previous cases. The thicknesses of the top Si, buried oxide and bulk Si were 50 nm, 400 nm and 725 µm, respectively. A scheme of the fabrication steps is shown in Figure 7.2. The process started with a piranha solution bath (H_2SO_4:H_2O_2 = 3:1) for 10 minutes to eliminate organic residues, followed by a 10 second dip in 5% HF to etch any SiO_2 native layer. Then, the wafers were doped following the procedure explained in Section 5.3. The SoD solution is deposited on the device side of the wafer with a velocity of 4000 rpm for 60 s and cured on a hotplate at 200°C for 180 s. Dopant diffusion was induced by thermal annealing at 900°C for 15 min, and the residues were removed after a sequence of HF etching, O_2 plasma and HF etching as shown in Section 5.3. Then, a photolithography and RIE of the Si layer defined the suspended platforms, the TE element and the collectors (Figure 7.2b). Next, a bilayer of SiO_2 and Si_3N_4 was deposited on both sides of the wafer (Figure 7.2c). SiO_2 was deposited by PECVD on the top (100 nm) and backside (200 nm). Si_3N_4 was deposited by LPCVD, with a thickness of 300 nm. Annealing at 850°C for 30 min after the SiO2 depositions was essential to remove any possible organic residues from the SiO_2 film. Moreover, this helped to ensure better coverage of the rough wafer backside and guaranteed proper patterning later in the process. After, the metal-Si inter-level contacts were patterned by photolithography and RIE of the 300 nm thick Si_3N_4 and BOE of the SiO_2 (Figure 7.2d). Here, SiO_2 acted as a sacrificial layer that protected the thin Si film during the Si_3N_4 RIE. Next, the metal layout was defined using a third photolithography step, followed by the sputtering of 30 nm of Ti and 200 nm of W and subsequent lift-off (Figure 7.2e). Ti acted as an adhesion layer, and W was selected as the main metal for its capability to withstand high current densities without melting. Following earlier work by the research group, an RTA at 700°C for 30 s in vacuum was

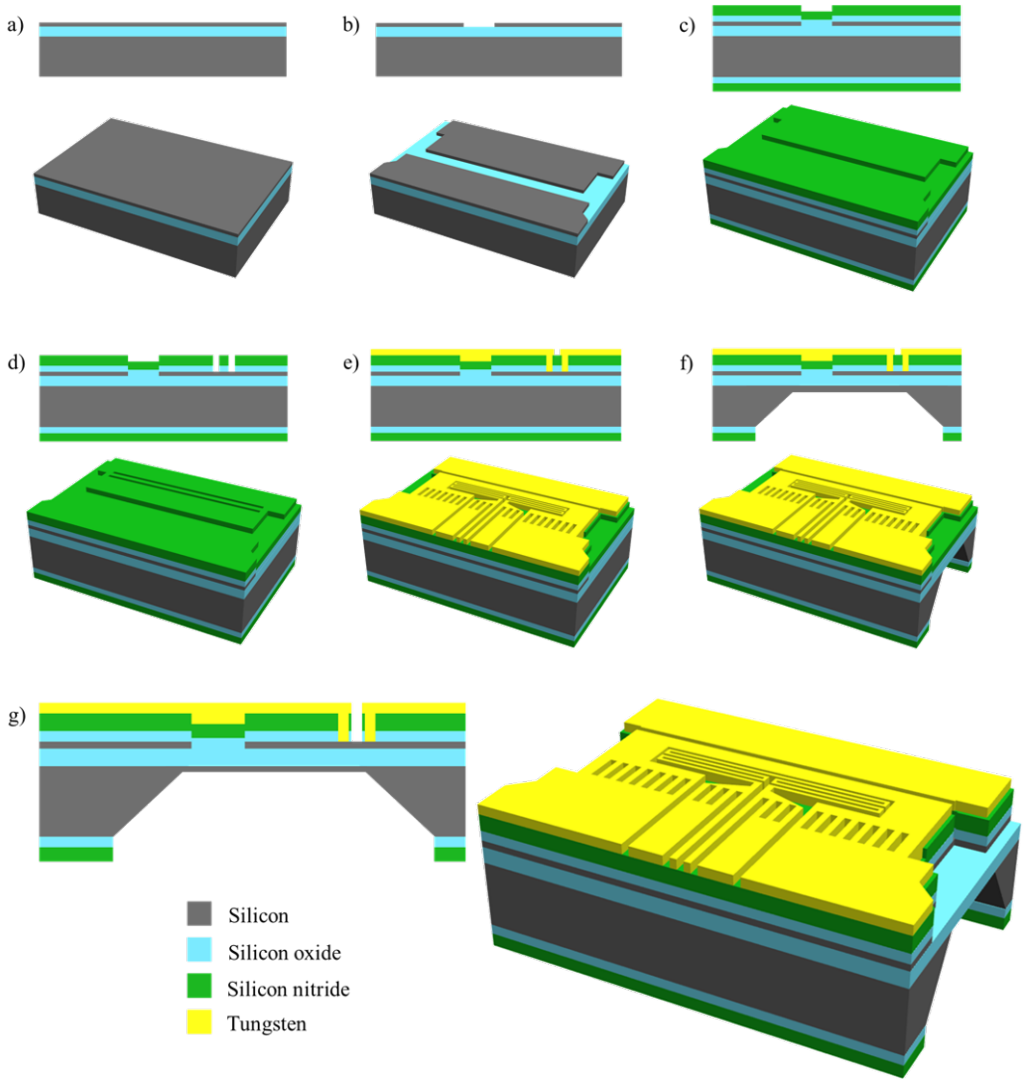


Figure 7.2: Scheme of the wafer-level fabrication steps for µTEGs based on nanostructured Si thin films. a) Doping of top Si by SoD. b) Photolithography and RIE to define the layout of the device Si. c) PECVD and LPCVD deposition of SiO_2 and Si_3N_4 layers. Annealing at 850°C for 30 min performed between the deposition of the oxides and the nitride. d) Photolithography and RIE of Si_3N_4 and BOE of SiO_2 to define the metal-Si inter-level contacts. e) Photolithography, sputtering of 30 nm of Ti and 200 nm of W followed by lift-off to define the metal layout. f) Backside window opening followed by KOH to etch bulk Si. A 5 µm thick Si pre-membrane is left. g) Photolithography and RIE of Si_3N_4 and BOE of SiO_2 to expose the top Si in the TE areas. This step also defines the ancillary elements.

completed to improve the doped Si contact with Ti [197]. However, these conditions were later proven to be suboptimal for 50 nm thick Si layers due to the presence of voids and cracks in the interface (see Section 7.5). The optimized annealing conditions were later found to be 450°C for 1 h in ultra-high vacuum. Wafer backside openings were patterned using a fourth photolithography step, followed by RIE of the Si_3N_4 and SiO_2 layers to define the membranes. The bulk Si was then etched in KOH until a thin ($\sim$ 5 µm) pre-membrane remained beneath the platforms (Figure 7.2f), which provided mechanical robustness during the following steps. The last wafer-level processing steps exposed the TE areas and defined the ancillary elements with a fifth photolithography, followed by RIE of Si_3N_4 and BOE of SiO_2, which were completed as described above (Figure 7.2g). At this stage, the wafer was diced into 7x7 mm^2 chips.

The two remaining process steps were completed at chip level. The first step involved the nanostructuration of the exposed 50 nm thick Si layer (i.e. the TE elements), which included the coating and annealing of the BCP, followed by pattern transfer via wet etching and RIE. These steps were analogous to those described for the 3ω chips (Section 6.1.2). SEM imaging after nanostructuration of the TE material (Figure 7.3) confirmed that the Si thin film patterning was equivalent to that of free-surface samples in earlier trials. SEM images also showed that, as in the case of the 3ω chips, there was a rim of approximately 400–500 nm around the oxide/nitride frame where no pattern was transferred. Overall, more than 80% of the total area of the trench was nanostructured. The pattern transfer procedure was considered successful in nanostructuring thin Si films within trenches as narrow as 15 µm.

The final step was the release of the platforms, which was equivalent to what was explained in Section 6.1.2. The etching of the 5 µm thick bulk Si pre-membrane was completed by micropipetting KOH solution onto the backside of the chip, which was protected with a PSA film. The chips were rinsed in DI water and IPA. In this case, the membranes withstood the water cleaning without adding IPA to reduce surface tension. The fabrication finished with the mechanical removal of the PSA adhesive. Optical images of four fully fabricated platforms are shown in Figure 7.4. The supporting membrane shown corresponds to a piano layout with a varying number of 5 µm wide ancillary supports for each membrane. The deformation observed in the top-illuminated images is a

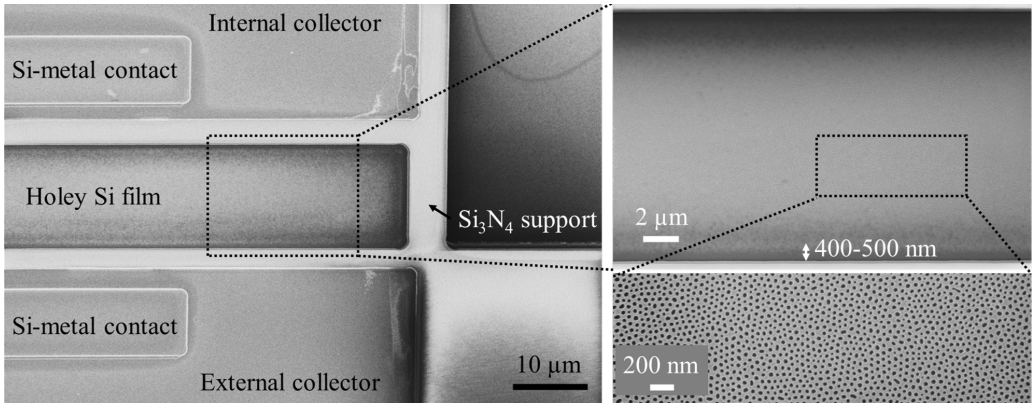


Figure 7.3: SEM images of the Si nanostructuring within the µTEGs. The 400-500 nm rim around the SiO_2/Si_3N_4 frame shows no nanostructuration due to the thicker BCP thickness in these areas.

consequence of the BOX compressive stress not being fully compensated by the Si_3N_4. The comparison of the different devices suggests a non-significant impact of adding additional ancillary elements to decrease the mechanical stress on the membranes. Therefore, the optimal layout in terms of thermoelectric performance (piano-like design and only 3 ancillary supports) is fully compatible with the overall fabrication process of the µTEGs.

With these results, a procedure to fabricate a µTEG integrating nanostructured Si thin films has been demonstrated. The methods developed for the 3ω devices (including BCP spin coating, pattern transfer, and KOH etching of the 5 µm thick Si membrane at chip level) were validated on the µTEGs. The resulting fabricated devices have mechanically robust membranes. However, subsequent characterization of the µTEGs revealed unexpected and disruptive alterations at the Ti–doped Si interface resulting from the RTA process intended to improve contact resistance. The experimental work carried out to optimize the annealing conditions and improve contact resistance is discussed in Section 7.5. The high contact resistance of the first batch of µTEGs hindered their use as power generators, but V_{OC} could be evaluated. A second batch of µTEGs with optimized Ti-Si contact resistance, which is currently under fabrication (see Section D.2), will enable the evaluation of the potential of µTEGs based on nanostructured Si.

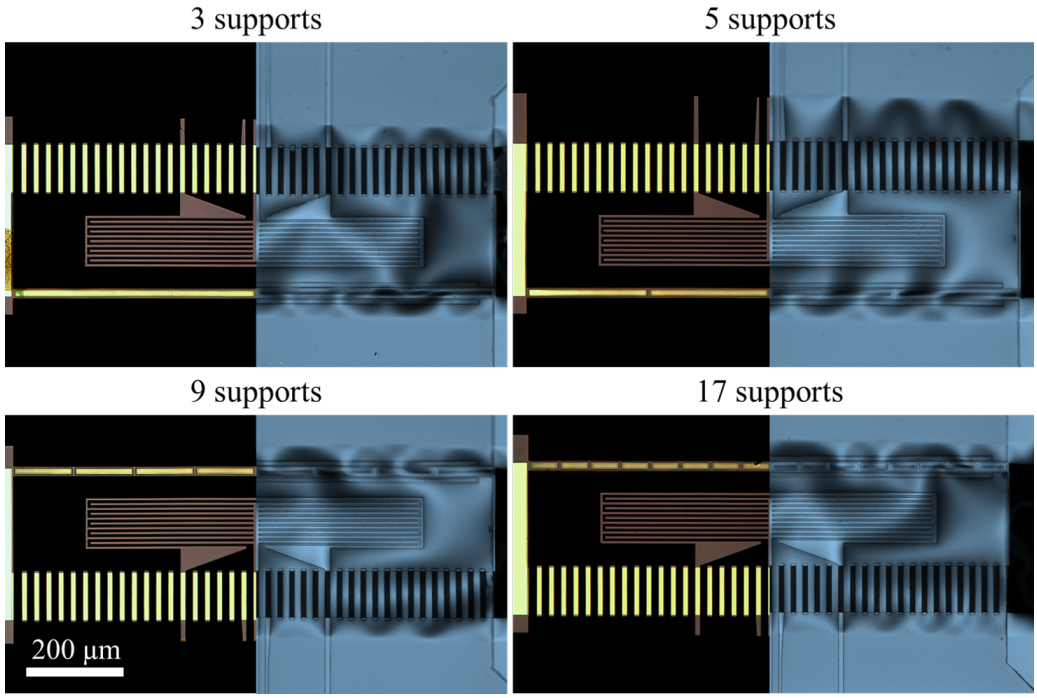


Figure 7.4: Optical images of a fully fabricated µTEG with nanostructured TE regions and suspended platforms. The devices shown correspond to those with piano-like supporting membranes and 5 µm wide ancillary Si_3N_4 supports (3, 5, 9 or 17). The left side of each membrane shows the optical image with bottom illumination. The optical images with top illumination (right side) reveal the mechanical stress in the membranes.

7.2 Open circuit voltage characterization

The µTEGs V_{OC} was evaluated under real operation conditions (i.e. in harvesting mode), as described in Section 3.2.1.2. The non-optimized contact resistance between the TE element and the metal in the first batch of devices has no impact on V_{OC} characteristics and, therefore, the evaluation of the µTEGs was meaningful. V_{OC} generation versus hotplate temperature of a µTEG with piano-like supporting membrane, 50 nm thick bare Si films as TE elements and three 5 µm wide ancillary supports is shown in Figure 7.5. It can be seen that as the heat exchange with the surrounding air increases (from closed cage to forced convection), the measured V_{OC} rises accordingly. The standard deviation of V_{OC} at each hotplate temperature also behaves in the same way (i.e. V_{OC} is noisier

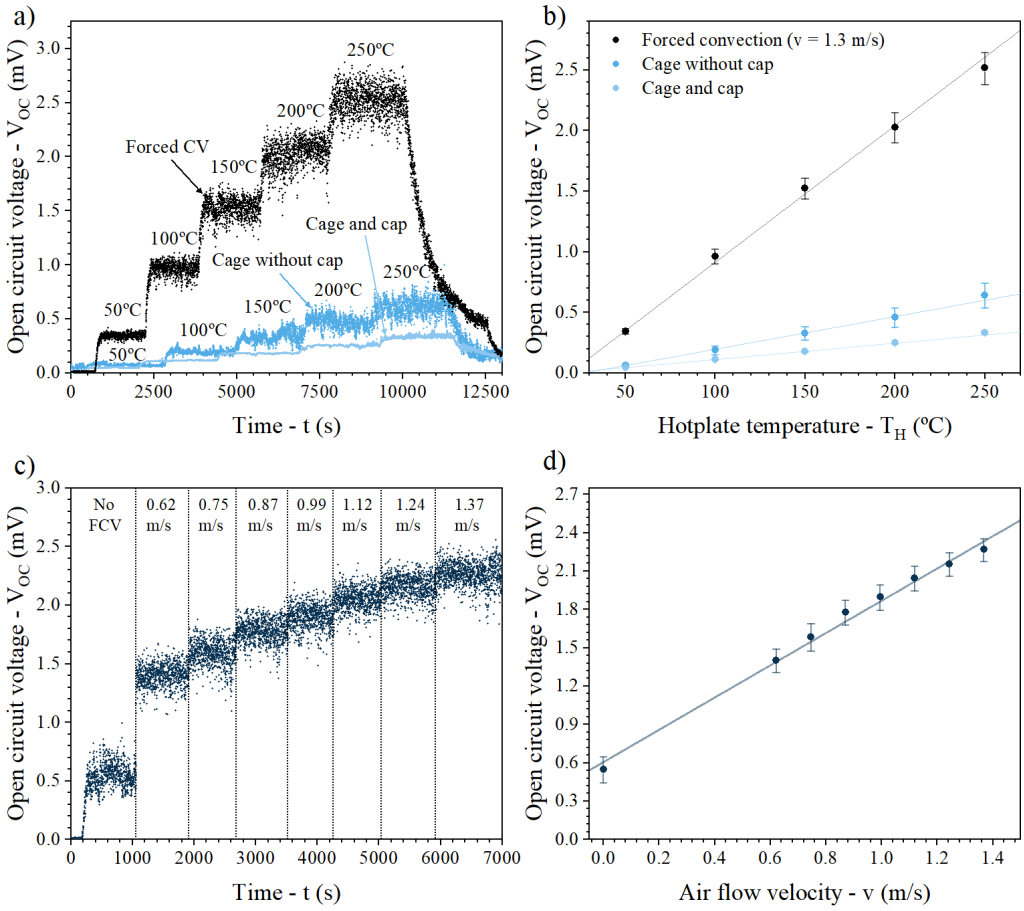


Figure 7.5: V_{OC} versus time and hotplate temperature on a µTEG with bare 50 nm thick Si under different convection regimes. a) evolution of V_{OC} with time at different hotplate temperatures and distinct convection regimes. b) Average V_{OC} versus applied hotplate temperature on distinct convection regimes. c) V_{OC} over time for a hotplate temperature of 250°C at increasing voltages on the fan (air flow velocity from 0 to 1.4 m/s). d) Average V_{OC} generation with time for a hotplate temperature of 250°C at increasing forced convection speeds.

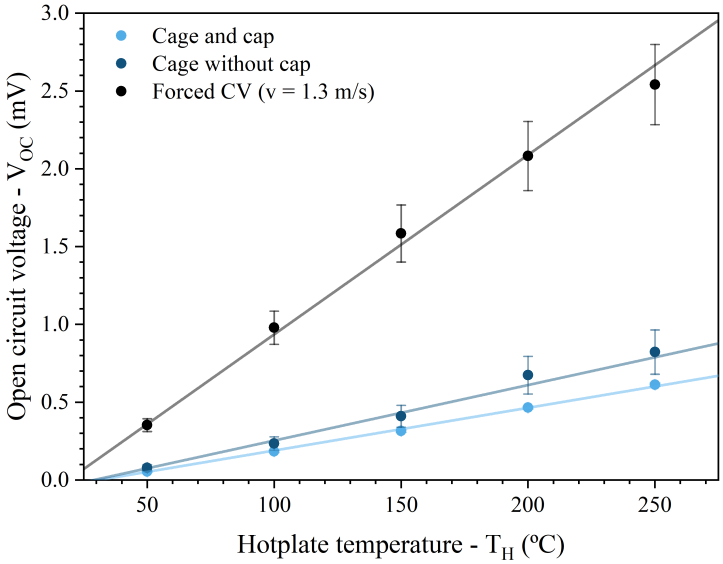


Figure 7.6: Average V_{OC} generation versus hotplate temperature of a µTEG with 57-nm pitch nanostructured Si film exposed to: still air with a walled cage, still air with a closed cage and forced convection (1.3 m/s).

as heat exchange with the surroundings increases). In this case, a maximum V_{OC} of 0.67 mV is obtained at 250°C when the µTEG is exposed to still air (i.e. real working conditions - cage without cap -), reaching a V_{OC} of 2.52 mV with a $\sim$ 1.3 m/s air flow. In this sense, Figure 7.5 c) and d) evidence how an increase in the air flow velocity leads to a linear increase of V_{OC} in the measured range, which is expected in this configuration (i.e. for the air flow velocities considered).

V_{OC} under analogous environmental conditions and hotplate temperatures of a µTEG where the 50 nm Si film had been nanostructured with a 57 nm pitch nano-pattern is shown in Figure 7.6. In this case, the µTEG generated a maximum V_{OC} of 0.82 mV when the hotplate was set to 250°C under natural convection. The V_{OC} raised to 2.6 mV when an air flow of $\sim$ 1.3 m/s was forced over the µTEG. These results demonstrate that µTEGs with nanostructured films generate higher V_{OC} (i.e. they achieve a larger temperature gradient across the TE element) compared to those based on bare Si films.

Figure 7.7a compares the V_{OC} generated by three different µTEGs at various hotplate temperatures, with the µTEGs enclosed in the cage to minimize thermal fluctuations and achieve the highest precision in the electrical measurements. The µTEGs are named according to the nomenclature of Table 7.1. The results show that nanostructuring significantly enhances the thermal performance of the µTEGs. Even with the less favorable layout (Type D, without the supporting membrane that helps establish the thermal gradient), the µTEG with patterned films outperforms the Type A device with bare Si films in V_{OC}. On average, over the entire temperature range, type A µTEG with nanostructured Si (chip 1) exhibited $\sim$ 1.99 times the V_{OC} of the type A µTEG with bare Si (chip 3).

The high R_C made it necessary to estimate the power performance of the first-generation devices. To do so, the measured V_{OC} ratio was considered (i.e. between chip 1 and 3), while the electrical resistivity for both films was based on the resistivities

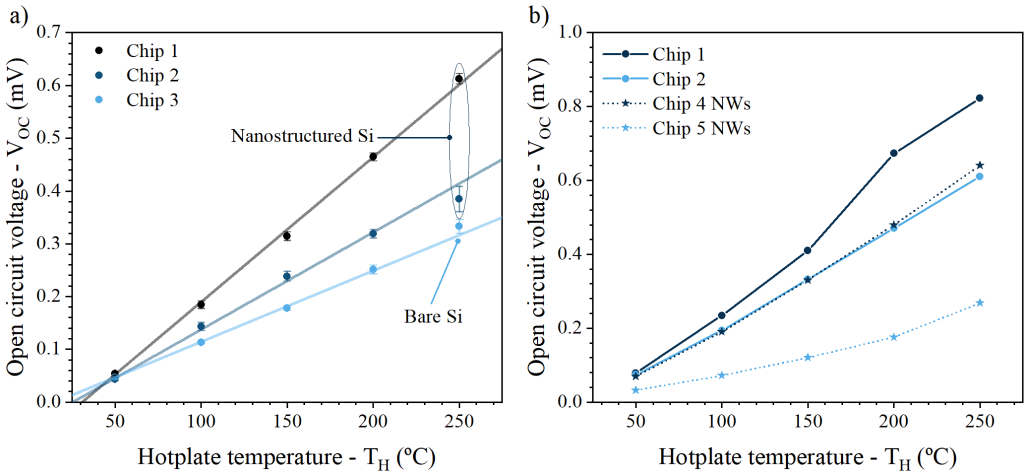


Figure 7.7: V_{OC} generation as a function of hotplate temperature and the nano-patterning of the thin Si film compared with the NW-based µTEGs presented in this thesis. a) Average V_{OC} as a function of hotplate temperature of three µTEGs (see Table 7.1) in the closed cage configuration. b) Average V_{OC} as a function of hotplate temperature of four µTEGs: two with TE thin films, two with Si NWs (with one -T1- and four -T4- trenches in series, and equivalent design to Type A of thin films) under natural convection.

Table 7.1: Different μTEG designs compared in Figure 7.7.

Chip	Layout design	Membrane	Ancillary supports	TE element
1	Type A	Piano-like Si_3N_4	Three 5 μm-wide	Holey Si
2	Type D	No membrane	Three 5 μm-wide	Holey Si
3	Type A	Piano-like Si_3N_4	Three 5 μm-wide	Bare Si
4	Type A T4	Piano-like Si_3N_4	No supports	Si NWs
5	Type A T1	Piano-like Si_3N_4	No supports	Si NWs

measured with SoD (Section 5.3). Since the nanostructured film resistivity is $\sim$ 2.25 times higher than that of the bare film, the average P_{max} over the entire temperature range is expected to be 1.76 times higher for nanostructured µTEGs with the same layout and without heat sink. In a bi-leg design (i.e. with n- and p-type nanostructured Si on both sides of the suspended platform), this increase is expected to be even more pronounced. Whether this trend persists after heat sink integration remains to be investigated.

The V_{OC} of the µTEGs based on Si thin films was compared to those of the NWs-based 4X-type devices in chapter 3. Figure 7.7b shows that both thin film-based µTEGs generate higher V_{OC} than the NW-based ones when the membrane design and trench length are equivalent (i.e. single-trench -T1- devices). This improvement cannot be attributed solely to the thermal conductivity of the films, because the thermal gradient depends on the overall conductance of the TE element. Since the NW array has a considerably larger cross-section than the Si thin films, and despite the higher thermal conductivity (κ) of the bare film compared to the Si NWs (46.45 W/m·K vs. $\sim$ 17.4

W/m·K, respectively), the thermal gradient is larger in the thin Si film-based µTEGs.

Even when comparing the V_{OC} of thin film–based µTEGs with that of NWs-based µTEGs containing four trenches in series (i.e. a four times longer TE element), the measurements remain higher or comparable for the nanostructured and bare cases, respectively. Considering that the Si thin films exhibit a lower Seebeck coefficient than the Si NWs (see Section 7.3), the thermal gradient of the films is consequently larger. When the Si thin film is nanostructured with a cylindrical pattern of period = 57 nm, the corresponding µTEG generates a $V_{OC} \sim 3.8$ and 1.4 times higher than those of the 1T-NWs and 4T-NWs µTEGs, respectively. Taking into account the corresponding Seebeck coefficients (see Section 3.2.1.1 and Section 7.3), the thermal gradient in the nanostructured film–based µTEG is ~ 4.4 and 1.6 times larger.

7.3 Seebeck coefficient characterization

Although the contact resistance between the TE element and the metal in the first batch of devices (non-optimized) limits the full device operation, it still permits V_{OC} characterization and Seebeck coefficient evaluation in these µTEGs. However, considering that the damaged Ti–Si interface could affect thermal contact resistance (making the evaluation of the actual thermal gradient on the TE element more difficult), the results obtained for the Seebeck coefficient are still preliminary. Further characterization of µTEGs will be performed after the second batch of fabrication is finished. The characterization procedure was equivalent to that in Section 3.2.1.1. First, the TCR of the heaters and thermometers of the different platforms was characterized inside a furnace. After that, the chips were assembled on the setup explained in Section 2.4.4. The hotplate temperature was set to 30°C, and the heater was used to increase the platform temperature, thereby creating a controlled thermal gradient. Figure 7.8 shows the results on a nanostructured µTEG. Examples of heating cycles to study the reproducibility of the Seebeck are shown in Figure 7.9. Good repeatability is observed after several cycles.

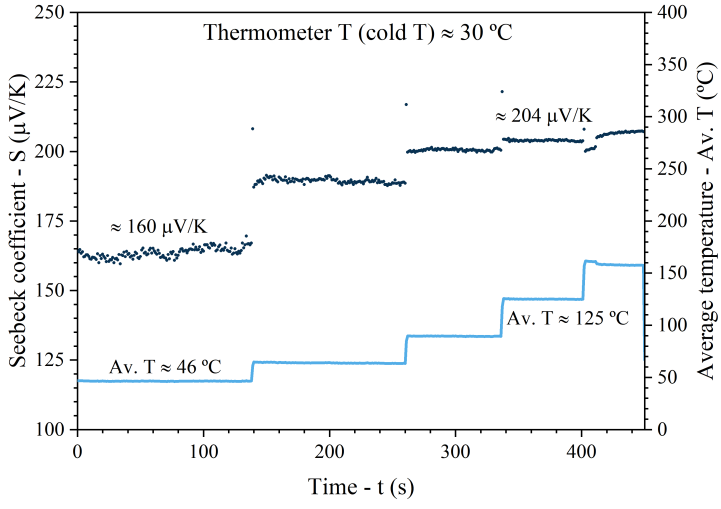


Figure 7.8: Seebeck characterization of the fully etched holey Si films with a period of 57 nm. The thermal gradient is measured with the heater and the thermometer at each platform.

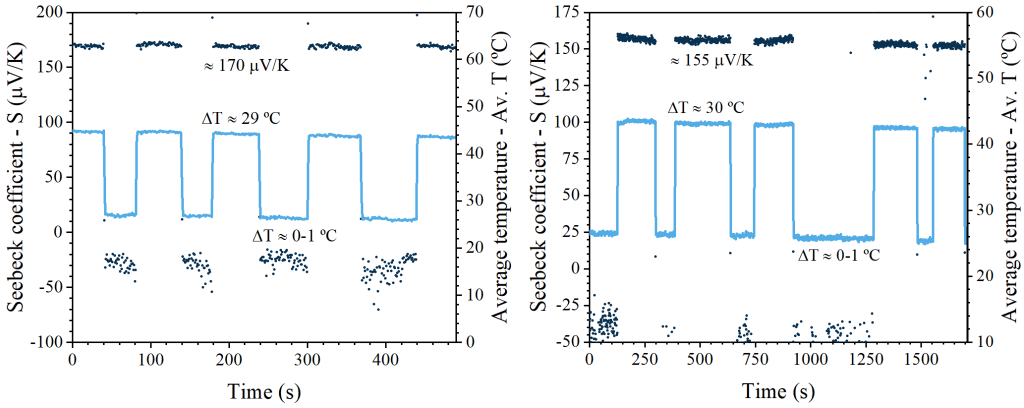


Figure 7.9: Seebeck coefficient measurement repeatability for fully etched holey Si films with a period of 57 nm on two different μTEGs.

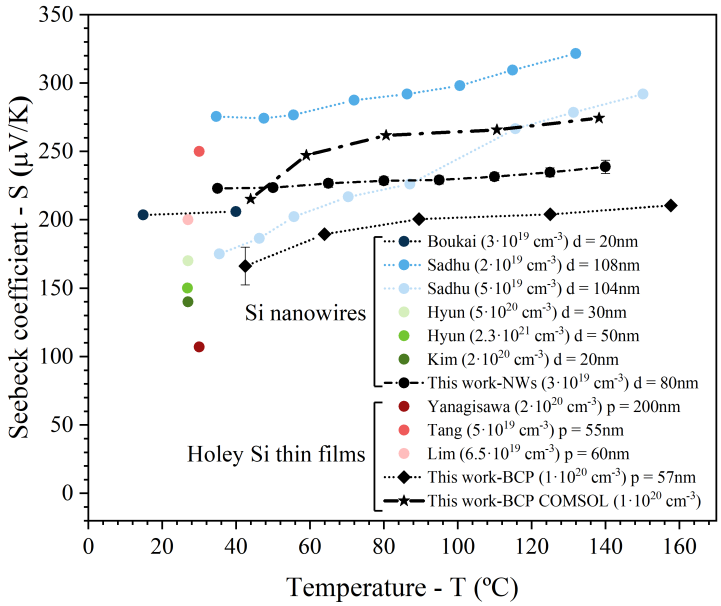


Figure 7.10: Comparison of Seebeck coefficient versus temperature obtained for the nanostructured TE films, measured and COMSOL-corrected, and from the Si NWs in this thesis against literature values. The plot includes Seebeck coefficient values measured on the μTEGs and those calculated after correcting the thermal gradient with COMSOL simulations. In NWs, d corresponds to the diameter, and in holey films, p corresponds to the period. Data extracted from [18], [80], [89], [101], [142], [143], [144]

After several measurements of the nanostructured films on different μTEGs, an average value of 166.14 ± 13.83 μV/K was obtained around RT.

However, this value was calculated under the assumption that the temperature gradient measured between the heater and the thermometer is the same as that experienced by the TE films. COMSOL simulations were conducted to verify the validity of this assump-

tion. To replicate the boundary conditions observed in the experiments, the temperature measured on the heater was applied to the central area of the suspended platforms in COMSOL. The temperature measured by the thermometer was applied to the top side of the bulk. The results of these simulations showed that the temperature gradient at the TE films was smaller than that measured with the thermometer and the heater. This is especially important on the heater side, as a significant portion of the temperature drop occurs across the platform before reaching the TE film (this effect becomes more pronounced when $G_{TE}/G_{Platform}$ is larger). Thus, Seebeck coefficient measurements were later corrected according to COMSOL simulations. For the RT case, the corrected value is 215.17 µV/K. The final Seebeck values at different temperatures (both directly measured and corrected) are shown in Figure 7.10 and compared with literature values for NWs and holey thin films. Since no COMSOL correction was applied in the NWs case [125], the comparison with the NWs from this work is done only with the uncorrected Seebeck values. Under these conditions, NWs exhibit higher Seebeck values across all temperatures, as expected due to their lower doping. On the other hand, Seebeck variations with temperature show a steeper increase in the case of holey films. Again, this can be explained by the fact that higher doping further suppresses the phonon-drag effect, resulting in a steeper increase in the Seebeck coefficient with temperature [145]. Regarding holey Si thin films, those reported by *Tang et al.* [80] and *Lim et al.* [89], which have similar patterning but lower doping, exhibit higher Seebeck values, even when compared to COMSOL-corrected results. In contrast, the films reported by *Yanagisawa et al.* [88] exhibit a lower Seebeck coefficient, which is expected due to their higher doping level. Thus, the Seebeck coefficient is in good agreement with the values and trends reported for other Si structures.

7.4 Figure of merit

To complete the thermal, electrical, and Seebeck results presented in the previous sections, the effect of nanostructuring on the figure of merit of 50 nm thick Si thin films can be quantified. Figure 7.11 presents the values of zT as a function of etched depth on the 57-nm pitch cylindrical patterning for the directly measured zT and the COMSOL-corrected values. The zT value is calculated using the Seebeck coefficient measured with the fully nanostructured samples for all cases, as no change is expected for patterned samples [89]. It's clear that the optimal case in terms of zT enhancement is the fully patterned sample. Furthermore, there is no linear relationship between zT and pattern depth. Depths below 30 nm show little to no increase in zT, whereas it is significantly enhanced for deeper etchings. The patterning effects on electrical and thermal transport explain this behavior. The zT values of the fully etched holey film in this work are 0.08 ± 0.01 and 0.14 ± 0.01 for the directly measured and COMSOL-corrected cases, respectively. These values are significantly higher than the zT of the NWs in this work (maximum zT of 0.04). Moreover, these values are lower than the state-of-the-art zT values reported in the literature for holey thin films or nanowires (0.4 for holey Si [80], 0.6 for rough Si nanowires [19], and 0.31 for porous Si nanowires [74]), primarily due to the higher thermal conductivity of the patterned films presented in this thesis compared to those reported. However, it is important to note that neither of these studies properly measured thermal contact resistance in their structures, as they only performed bridge-like measurements and assumed the contact resistances to be negligible. As explained in Section 6.3.2, even for films with very low thermal conductivity, significant corrections might be necessary to measure the film κ. Furthermore, other studies on holey Si films with similar neck sizes

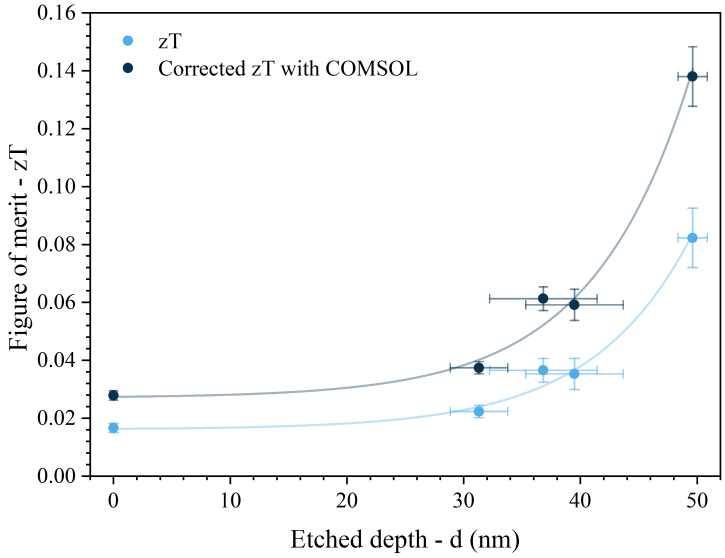


Figure 7.11: Figure of merit for the 57 nm pitch patterned Si thin films as a function of etched depth at room temperature. The plot shows the zT values calculated with the measured Seebeck values and zT calculated after the COMSOL-corrected thermal gradients. The lines are guides to the eye to illustrate the trend.

report more modest zT values (0.05 [89], 0.02 [64] and 0.09 [90]). In comparison with these studies, nano-patterned films developed in this thesis outperform most of them in terms of zT. Moreover, it should also be highlighted that the procedure to pattern the TE material can be performed at wafer-scale and is CMOS compatible. Compared to other BCP-based approaches [80], [89], the films developed in this work are the only ones that avoid intermediate fabrication steps and enable direct pattern transfer.

7.5 Ti-Si contact resistance

As explained in Section 7.1.1, the main limitation of the first batch of μTEGs was the poor Si–Ti contact resistance resulting from a 700°C RTA process, which had been used in earlier μTEGs on SOI wafers with a Si device layer of 15 μm thick [197]. Figure 7.12 shows three SEM images of the Si-Ti contact: before annealing, after RTA at 700°C and after the optimized annealing at 450°C. The increase in contact resistance after the RTA at 700°C is primarily attributed to Si acting as the dominant diffusion species in the Si–Ti reaction, which can lead to void formation in the film due to the rapid diffusion of Si into Ti [198]. This diffusion has a greater impact on thinner Si films, as it can completely degrade them and, thus, Si diffusion must be properly controlled to avoid film degradation. The Si–Ti reaction is a well known process that proceeds through different stages depending on the reaction temperature. More importantly, there exists a temperature range in which silicidation can be avoided while still allowing intermixing within the Si–Ti phase (between 300 and 450°C [199]). According to the literature, the contact resistivity reaches a minimum when annealing between 450 and 500°C [200]. However, the reported values are for either bulk or thick Si films. Therefore, this process was validated for 50 nm thick Si films.

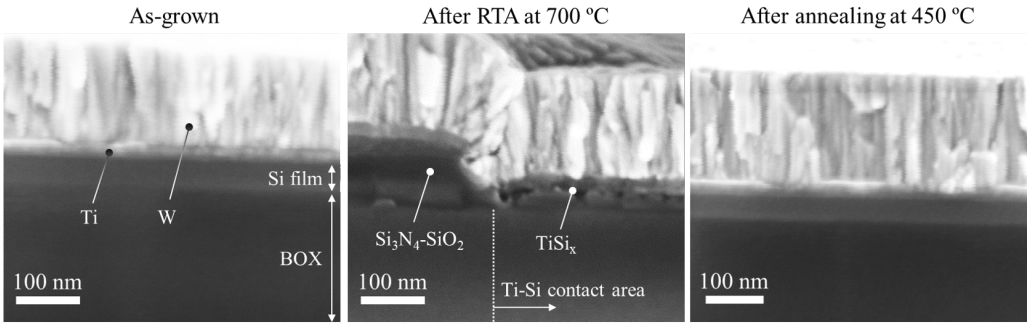


Figure 7.12: SEM images of the as-grown Si-Ti interface, after RTA at 700°C and after annealing at 450°C. It is evident that the RTA at such high temperature damages completely the film, while at 450°C the film remains intact.

In order to study whether this could be applied to ultra-thin Si films, TLM structures were fabricated at chip scale. First, the thin Si layer was patterned by laser photolithography followed by RIE. Second, the metal pads were defined by laser photolithography and sputtering of 30 nm of Ti and 200 nm of W, followed by lift-off (see Figure 7.13a).

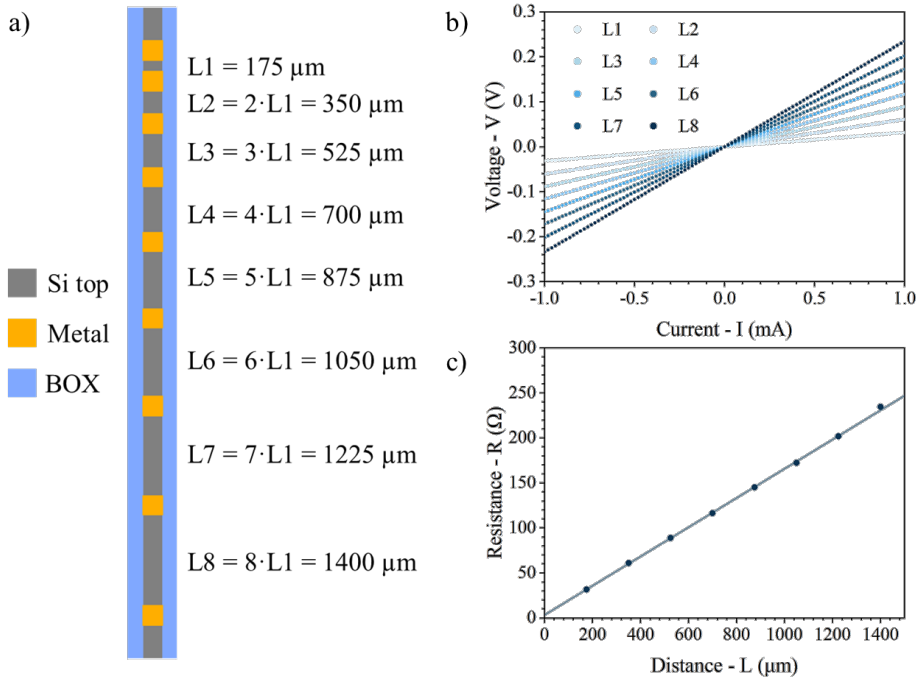


Figure 7.13: Scheme of the TLM chip and I-V and R vs distance curves. a) Scheme of the TLM chip. L indicates the distance between metal pads. The line is 300 µm wide. b) I-V curves obtained at different metal pad distances on 50 nm thick and 300 µm wide Si lines with 30 nm Ti and 200 nm W contacts. The results correspond to a non-annealed sample. c) Resistance versus metal pad length on the Si lines.

The samples were dipped in BOE immediately before the sputtering process to remove any native oxide. Figure 7.13b and c show the I-V and R vs distance curves obtained for non annealed samples. The linearity of the I–V curves demonstrates that the Si–Ti contact is ohmic, which can be attributed to the high doping level of the Si films.

The contact resistivity and sheet resistance before and after different thermal treatments are reflected in Figure 7.14. The annealing processes were conducted at temperatures up to 500°C under high vacuum. An average contact resistivity of $7.98{\cdot}10^{-5} \pm 1.96{\cdot}10^{-5}$ Ω·cm^2 was calculated from the characterization of the as-grown samples. Since the transfer length is ∼ 4% of the total contact width in the TLM measurements, L_T in a μTEG can be calculated (i.e. $L_T \sim 0.4$ μm). Therefore, a contact resistance of roughly 19.95 Ω is estimated on each side of the TE film, resulting in a total contact resistance of 40 Ω. The resistances of the TE films are ∼ 8.5 Ω and 4.9 Ω for the holey and bare films with the geometry of the μTEG, respectively. This implies that the total electrical resistance is dominated by the contacts.

After an hour of annealing at 450°C, the contact resistivity improved to $5.63{\cdot}10^{-6} \pm 1.87{\cdot}10^{-6}$ Ω·cm^2, which corresponds to an enhancement of one order of magnitude. Using the same transfer length, this would correspond to a contact resistance of ∼ 1.4 Ω on each side of the TE film. Therefore, the electrical contact contribution accounts for less than 33% of the total electrical resistance in the bare film case and less than 25% in the holey film device. Deviations lower than 3% in Si films R_S when comparing measurements before and after annealing indicate that there was no degradation following annealing at 450°C.

In summary, it has been demonstrated that the Si-Ti contacts can be optimized without damaging the interface or the thin Si film. It is also important to note that this contact exhibits fully ohmic behavior. The annealing conditions and the results obtained are in general agreement with the literature for Si samples with equivalent doping ($2{\cdot}10^{20}$

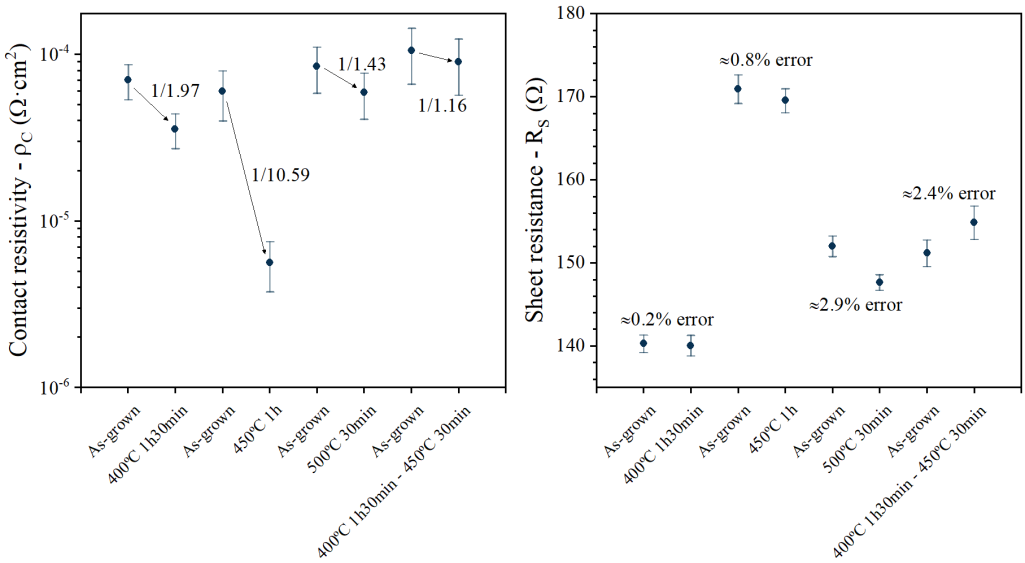


Figure 7.14: Si-Ti contact resistivity and Si sheet resistance for different thermal treatments. All thermal treatments were done under high vacuum conditions.

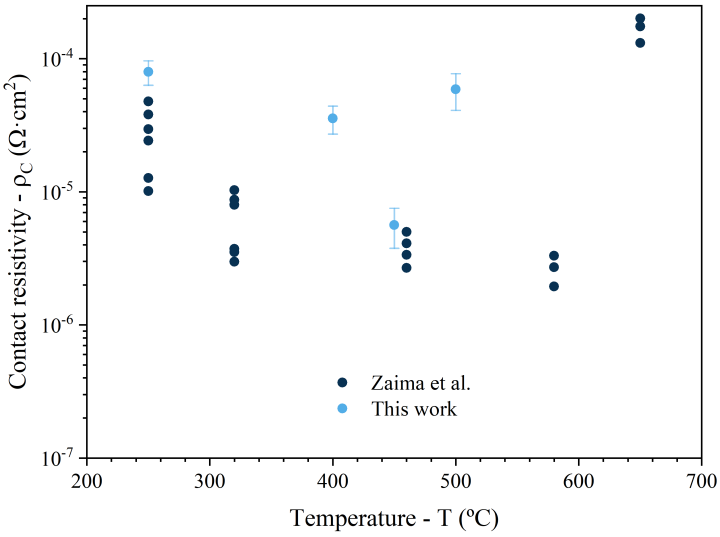


Figure 7.15: Comparison of Si-Ti contact resistivity of this work with those by *Zaima et al.* [201] (bulk Si with equivalent p-type doping of $2{\cdot}10^{20}$ cm^{-3}).

cm^{-3} p-type doping on bulk Si - see Figure 7.15) [201]. The second batch of µTEGs with optimized annealing conditions is currently under fabrication.

7.6 Chapter conclusions

µTEGs with bare and patterned films were fabricated with different designs, and the optimal design proved to be mechanically robust. To the best of the author's knowledge, this is the first thermoelectric generator based on holey silicon fabricated using block copolymer nano-patterning. V_{OC} and Seebeck coefficient characterization were evaluated with the first generation of µTEGs. The thermal management of the holey Si-based µTEGs resulted in a thermal gradient 1.99 times higher than that of the bare Si thin films-based µTEGs, and 4.4 times higher than that of the NWs-based µTEGs with equivalent design. Regarding the Seebeck coefficient, a value of 166 µV/K was found at RT, leading to a zT of 0.08 at RT. When the Seebeck coefficient was corrected using COMSOL simulations to evaluate the temperature gradient more accurately, zT increased to 0.14. These values are higher than those of most holey Si films reported in the literature. The main limitation of the first generation of µTEGs was the high contact resistance at the Si–Ti interface. This issue was experimentally addressed through a 450°C annealing process, which reduced the contact resistivity by approximately one order of magnitude, yielding a final value of $7.98{\cdot}10^{-5}$ Ω·cm^2. The second generation of µTEGs is currently under fabrication (see Section D.2).

Chapter 8

Conclusions

This thesis was devoted to the study of silicon as a thermoelectric material and investigated three silicon structures: microbeams, nanowires, and nano-patterned thin films. Building upon the group's previous work, the first two structures were examined from a thermoelectric generator perspective, focusing on their power generation capabilities. The last structure was entirely developed within the scope of this thesis, encompassing its optimization and characterization from both material and thermoelectric generation standpoints, along with ad hoc designs and fabrication of all devices in these studies. The following sections summarize the specific conclusions drawn from the results of each part.

Micro-thermoelectric generators based on silicon nanowires and microbeams

µTEGs integrating Si NWs and microbeams were investigated to determine the optimal thermoelectric configuration for each structure and to evaluate the Seebeck coefficient of the NWs. A reliable procedure for integrating a heat sink into these µTEGs was developed, followed by a detailed characterization of the resulting enhancement in power generation. In addition, long-term and transient measurements were performed to assess the autonomy and behavior of the µTEGs at different temperatures. Finally, a 2×2 TEG was fabricated and characterized, demonstrating the scalability of µTEG integration per device. The following paragraphs summarize the main achievements within each of these topics:

- **Bare µTEGs with Si NWs and microbeams.** In the case of the NW-based devices, the optimal thermoelectric length for power generation was found to be 75 µm, and a Seebeck coefficient of 205 µV/K was obtained at room temperature. This value is in good agreement with those reported in the literature for similar doping levels. In the case of the microbeam structures, the optimal geometry was determined to involve a limited number of microbeams due to their high thermal conductance. The high integration density achieved in the Parallel-type µTEG, along with the corresponding increase in output power, demonstrated the strong potential of silicon technology to maximize power generation per unit area. However, the power output of these µTEGs remained limited due to the low efficiency of their heat exchange with the environment.

- **Heat sink integration.** The integration of a heat sink in the µTEGs was achieved by using an intermediate Si adapter piece, which provided thermal contact exclusively at the platforms and corners, and distributed the weight of the heat sink. In order to achieve a proper placement of the adapter, a custom pick and place setup was used. The integration was optimized by exploring different procedures and thermal pastes, ultimately achieving a reliable and reproducible integration procedure.
- **µTEGs with heat sink.** The heat sink implementation led to 9- and 17-fold thermal gradient improvements on NWs and microbeams-based µTEGs, respectively. The characterization of the µTEGs demonstrated that the microbeams-based µTEGs had a higher increase in power generation due to the heat sink, ultimately surpassing the values of NWs-based devices. V_{OC} and P_{max} of these µTEGs at 250°C were 34 mV and 5.5 µW (NWs), and 20 mV and 8.2 µW (microbeams). Thus, it was proven that, as long as the heat management is properly optimized in the overall µTEG, the TE material with the lowest electrical resistance will result in the highest power generation. This implies that, given a proper µTEG design, the most convenient TE material is that with the highest power factor and not necessarily the one with the best zT. Lastly, power density values above 10 µW/cm^2 were achieved on the µTEGs with heat sink for hot temperatures above 175°C under natural convection and above 75°C when the equivalent of a natural breeze (i.e. 1.3 m/s) was present in the environment.
- **Long term and transient studies.** The long term studies demonstrated no degradation of the NWs up to 200°C. Beyond this temperature, enhanced native oxidation, which was observed by TEM, resulted in an increase in the internal resistance of µTEG. In contrast, the microbeam structures showed no signs of degradation within the investigated temperature range (50 to 250°C). The transient measurements of µTEGs revealed voltage peaks up to three times higher than the steady-state V_{OC} and, therefore, highlighted their potential for powering devices that require a cold-start voltage.
- **2x2 thermoelectric generator.** A thermoelectric generator integrating four µTEGs on a single PCB and sharing a common heat sink was successfully validated. This required a novel approach for the integration of the heat sink based on a multi-stack structure. The results demonstrate the feasibility of scaling up the number of µTEGs per device. Furthermore, this integration strategy enables improved efficiency of each individual µTEG by allowing the use of larger heat sinks for enhanced thermal management. With this configuration, the power density of each individual µTEG increased by up to 1.44 times compared to the microbeams-based µTEGs with individual heat sinks.

The results in this chapter demonstrate that individual 7×7 mm^2 µTEGs based on either Si microbeams or nanowires, when properly designed and integrated with a heat sink, can achieve power density values well within the range required for low-power IoT sensors. Moreover, these µTEGs exhibit compatibility with long-term operation across different temperatures (up to 200°C for NW-based µTEGs and beyond this limit for microbeams based ones). These results, therefore, meet the key requirements for IoT applications. Finally, the demonstrated scalability in the number of µTEGs per generator indicates that the final power and voltage output can be tailored to the specific needs of a given application by adjusting the number of integrated µTEGs.

Thermoelectric characterization of silicon thin films nanostructured with block copolymers

Self-assembly of PS-b-PMMA was optimized using cylindrical and lamellar BCPs either with their original morphology or through blending different BCPs. Afterwards, these patterns were transferred into Si films using wet and dry etching procedures. The doping level that is required for the films to be compatible with thermoelectric applications was achieved using the spin-on dopant technique. Ad hoc devices were fabricated to evaluate the thermal properties of the patterned films. Finally, μTEGs with nanostructured films were fabricated and characterized. The following paragraphs summarize the main achievements within each of these topics:

- **Self-assembly of PS-b-PMMA block copolymers.** Self-assembly of pristine BCPs on silicon substrates was successfully achieved using lamellar and cylindrical BCPs with controlled pattern orientation. In the case of cylindrical BCPs, blending was optimized to obtain periodicities with neck sizes above 20 nm. To this end, pairs of pristine BCPs combined with different brush layers were employed.
- **Pattern transfer onto silicon.** PMMA etching was optimized using both dry and wet routes: Ar/O_2 plasma for lamellar BCPs and brush layers, and UV light followed by acetic acid for cylindrical BCPs. Subsequently, pattern transfer onto silicon was performed using the PS block of the BCP as an etching mask. Etching depths exceeding 50 nm were achieved for both lamellar and cylindrical thermoelectric-compatible patterns, with complete anisotropy and high reproducibility using the mixed Bosch RIE process.
- **Doping of silicon thin films.** The spin-on dopant technique was used to successfully dope silicon thin films at both chip and wafer level with good homogeneity. The doped films were fully compatible with the previously optimized patterning procedure. Bulk doping at wafer-scale was also demonstrated. The intrinsic electrical resistivity of a 50 nm thick film had σ of $\sim$ 900 S/cm. When these films were fully nanostructured with a 57 nm pitch cylindrical holey pattern, a final σ of $\sim$ 520 S/cm (i.e. a 1.74-fold increase in resistivity) was measured. On the other hand, the lamellar pattern had a negligible effect on the intrinsic electrical resistivity when the etched depth was below 25 nm, which is the only patterning compatible with thermoelectric applications.
- **Thermal characterization of nanostructured thin films.** The nanostructured films were integrated into three different devices for the thermal characterization of the cylindrical films. Each device required a specific fabrication strategy. Thermal conductivity measurements using the 3ω and bridge/laser techniques demonstrated that κ of the starting 50 nm thick film at room temperature was 46.45 W/m·K. Regarding the fully nano-patterned film with a 57 nm pitch cylindrical geometry, κ was 46.45 W/m·K at room temperature. This corresponds to a 9-fold reduction in κ after nano-patterning. A linear decrease in the overall κ was observed with increasing etching depth. When only the contribution of the silicon film is considered (i.e. when excluding the geometric factor), this decrease becomes even more pronounced. In the case of the FDTR method, a thermal model to fit the phase-shift measurements was developed. The experimental characterization is still ongoing (see Section D.1).
- **Thermoelectric generator based on nanostructured thin films.** μTEGs

based on bare and patterned films were successfully fabricated. V_{OC} generation and Seebeck coefficient characterization were carried out with the first generation of µTEGs. The thermal management of the holey Si µTEGs was 1.99 times better than that of bare Si µTEGs, and 4.4 times better than that of the equivalent NWs-based µTEGs. A Seebeck coefficient of 166 µV/K was found at room temperature, and a zT of 0.08 was calculated. When the Seebeck coefficient was corrected by simulations in COMSOL to more accurately evaluate the temperature gradient, the Seebeck became 215 µV/K and zT increased to 0.14. These values are higher than those of the majority of holey Si films reported in the literature. Moreover, they achieve these zT values in a wafer-scale and, in-principle, CMOS-compatible patterning procedure with direct BCP pattern transfer (i.e. without intermediate fabrication steps). The main limitation of the first generation of µTEGs, namely the high Si–Ti contact resistance, was addressed, and an optimized value of 7.98 $\times 10^{-5}$ $\Omega{\cdot}cm^2$ was achieved after optimizing the annealing process at 450°C. The second generation of µTEGs is currently under fabrication (see Section D.2).

The results in this chapter demonstrate that the PS-b-PMMA pattern can be directly transferred onto 50 nm thick silicon films without intermediate layers or additional fabrication processes. Moreover, these patterned films can be integrated into a CMOS- and wafer-compatible device fabrication process to selectively nanostructure silicon films in specific regions. The figure of merit of these structures is higher than that of most of the holey Si films in the literature. As a consequence, the thermal management of the µTEGs is significantly improved. This results in a 3.8-fold increase in voltage generation compared to the equivalent nanowires-based µTEGs, potentially yielding a significant enhancement in power density due to the low electrical and contact resistances in these µTEGs. Therefore, these results demonstrate that patterned films offer a significant improvement both in terms of thermoelectric properties and thermoelectric generation compared to the first generation of silicon nanowire structures. To the best of the author's knowledge, this is the first thermoelectric generator based on holey silicon fabricated using block copolymer nano-patterning.

Scientific contribution

Journal Articles

- J. M. Sojo-Gordillo*, D. Estrada-Wiese*, A. Rodriguez-Iglesias*, C. Duque-Sierra, M. Fernandez-Regulez, I. Martin-Fernandez, M. Salleras, L. Fonseca, A. Morata, A. Tarancón. *Equal contribution as first author. **Durable Dense Packed All-Silicon Micro-Thermoelectric Generator for IoT Applications**, *Advanced Functional Materials*, 35(22), 2419639, 2025.
- R. Aragonés, R. Malet, J. Oliver, A. Prim, D. Mascarell, M. Salleras, L. Fonseca, A. Rodríguez-Iglesias, A. Tarancón, A. Morata, F. Baiutti, C. Ferrer, **Milliwatt μ-TEG-Powered Vibration Monitoring System for Industrial Predictive Maintenance Applications**, *Information*, 15(9), 545, 2024.
- A. Rodriguez-Iglesias*, J. M. Sojo-Gordillo*, M. Fernandez-Regulez, I. Martin-Fernandez, I. Zardo, L. Fonseca, M. Salleras, et al., *Equal contribution as first author. **3-probe thermal characterization of holey silicon thin films.**, *In preparation (from results of Chapter 6)*, 2025.
- A. Rodriguez-Iglesias, M. Fernandez-Regulez, I. Martin-Fernandez, L. Fonseca, M. Salleras, et al., **Micro-thermoelectric generator based on holey silicon thin films.**, *In preparation (from results of Chapter 7)*, 2026.

Conference proceedings

- A. Rodriguez-Iglesias, D. Estrada- Wiese, J. M. Sojo- Gordillo, M. Fernandez- Regulez, I. Martin-Fernandez, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca, **Power Enhanced All-Si based Micro-Thermoelectric Generators by Heat Sink Integration**, in: Smart Systems Integration (SSI), IEEE, 2023.

Conference contributions

- A. Rodriguez-Iglesias, D. Estrada- Wiese, J. M. Sojo- Gordillo, M. Fernandez- Regulez, I. Martin- Fernandez, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca, **Heat sink implementation on micro-thermoelectric generators (μTEGs) for power enhancement**, in: National Days on Energy Harvesting and Storage (JNRSE), 2022 (poster).
- A. Rodriguez-Iglesias, D. Estrada- Wiese, J. M. Sojo- Gordillo, M. Fernandez-Regulez, I. Martin- Fernandez, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca, **Power enhanced micro-thermoelectric generators (μTEGs) by heat sink integration**, in: Virtual Conference of Thermoelectrics (VCT), 2022 (oral).
- A. Rodriguez-Iglesias, M. Salleras, D. Estrada-Wiese, M. Fernandez-Regulez, I. Martin-Fernandez, L. Abad, J. Santander, L. Fonseca, J. M. Sojo-Gordillo, A. Morata, A. Tarancón, **Heat sink implementation on micro-thermoelectric generators (μTEGs) for power enhancement**, in: European Conference of Thermoelectrics (ECT), 2022 (oral).
- A. Rodriguez-Iglesias, D. Estrada- Wiese, J. M. Sojo- Gordillo, M. Fernandez- Regulez, I. Martin- Fernandez, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca, **All-Si based micro-thermoelectric generators enhanced by heat sink integration**, in: Spanish Conference on Electron Devices (CDE), 2023 (poster).
- A. Rodriguez-Iglesias, D. Estrada- Wiese, J. M. Sojo- Gordillo, M. Fernandez- Regulez, I. Martin- Fernandez, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca, **Power Enhanced All-Si based Micro-Thermoelectric Generators by Heat Sink Integration**, in: Smart Systems Integration (SSI), 2023 (oral).
- A. Rodriguez-Iglesias, D. Estrada- Wiese, J. M. Sojo- Gordillo, M. Fernandez- Regulez, I. Martin- Fernandez, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca, **Long-term performance stability of all-Si based micro-thermoelectric generators with integrated heat sink**, in: European Conference of Thermoelectrics (ECT), 2023 (oral).
- A. Rodriguez-Iglesias, I. Martín- Fernández, F. Pérez- Murano, J. Santander, F. X. Álvarez, A. F. Lopeandia, L. Fonseca, L. Abad, M. Salleras, M. Fernández-Regúlez, **Thermoelectric devices based on block copolymer nanostructured Si thin films**, in: European Conference of Thermoelectrics (ECT), 2023 (poster). **Awarded as Best application potential**.
- A. Rodriguez-Iglesias, I. Martín- Fernández, F. Pérez- Murano, J. Santander, F. X. Álvarez, A. F. Lopeandia, L. Fonseca, L. Abad, M. Salleras, M. Fernández-Regúlez, **Block copolymer nanostructured Si thin films for thermoelectric enhancement**, in: International Conference on Micro – and Nano Engineering (MNE), 2023 (oral).
- O. Muntada-Lopez, A. Rodriguez-Iglesias, F. Perez-Murano, M, Fernández-Regúlez, **Patterning of Ormostamp films at the nanometer scale for large scale surface functionalization**, in: International Conference on Micro – and Nano Engineering (MNE), 2023 (poster).

- A. Rodriguez-Iglesias, D. Estrada- Wiese, J. M. Sojo- Gordillo, M. Fernandez- Regulez, I. Martin- Fernandez, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca, **Micro-thermoelectric generators based on Si enhanced by heat sink integration**, in: Joint EuroSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS), 2023 (oral). **Awarded as Best paper of the conference**.
- A. Rodriguez-Iglesias, J. M. Sojo- Gordillo, M. Fernandez- Regulez, I. Martin- Fernandez, F. Pérez-Murano, F. X. Álvarez, A. F. Lopeandia, A. Morata, A. Tarancón, L. Abad, J. Santander, M. Salleras, L. Fonseca, **Recent developments on Thermoelectric devices based on Silicon**, in: Joint EuroSOI Workshop and International Conference on Ultimate Integration on Silicon (EuroSOI-ULIS), 2024 (poster).
- A. Rodriguez-Iglesias, M. Fernández- Regúlez, I. Martín- Fernández, F. Pérez- Murano, J. Santander, F. X. Álvarez, A. F. Lopeandia, L. Fonseca, L. Abad, M. Salleras, **Thermoelectric enhancement of thin Si films by means of block copolymer driven nanostructuration**, in: Materials Society Spring Meeting (MRS), 2024 (poster).
- J. M. Sojo- Gordillo, D. Estrada- Wiese, A. Rodriguez-Iglesias, M. Salleras, A. Morata, A. Tarancón, L. Fonseca, **All-Silicon Micro- Thermoelectric Generator for IoT Applications**, in: Materials Society Spring Meeting (MRS), 2024 (oral).
- A. Rodriguez-Iglesias, M. Fernández- Regúlez, I. Martín- Fernández, F. Pérez- Murano, J. Tur, F. X. Álvarez, A. F. Lopeandia, L. Fonseca, L. Abad, M. Salleras, **Boosting Thermoelectric Performance of Ultra-Thin Si Films Through Block Copolymer- Induced Nanostructuring**, in: Nanoscale and Microscale Heat Transfer (NMHT), 2024 (poster).
- A. Rodriguez-Iglesias, H. Gómez-Torres, J. Tur-Prats, M. Fernández-Regúlez, I. Martín-Fernández, F. Pérez-Murano, J. Santander, L. Fonseca, F. X. Álvarez, A. F. Lopeandia, M. Salleras, L. Abad, **Thermal conductance tunnabiliy by means of block copolymer driven nanostructuration of Si-ultrathin membranes**, in: European Thermal Sciences Conference (EUROTHERM), 2024 (oral).
- J. M. Sojo-Gordillo, D. Estrada-Wiese, A. Rodriguez-Iglesias, C. Duque-Sierra, M. Salleras, L. Fonseca, A. Morata, A. Tarancón, **Densely Packaged All-Silicon Micro-Thermoelectric Generator**, in: ASME Micro/Nanoscale Heat and Mass Transfer International Conference (MNHMT), 2024 (oral).
- A. Rodriguez-Iglesias, Iñigo Martín- Fernández, Francesc Pérez- Murano, Joaquín Santander, Ivan Molina- Jiménez, Hugo Gómez, F. Xavier Álvarez, Aitor F. Lopeandia, Luis Fonseca, Llibertat Abad, Marta Fernández-Regúlez, Marc Salleras, **Thermoelectric enhancement of ultra-thin Si films: a block copolymer driven nanostructuration approach**, in: Spanish Conference on Electron Devices (CDE), 2025 (oral).
- A. Rodriguez-Iglesias, Iñigo Martín- Fernández, Francesc Pérez- Murano, Joaquín Santander, Ivan Molina- Jiménez, Hugo Gómez, F. Xavier Álvarez, Aitor F. Lopeandia, Luis Fonseca, Marta Fernández-Regúlez, Llibertat Abad, Marc Salleras, **Thermoelectric Properties of Ultra-Thin Si Films via Block Copolymer Nanopatterning** in: Iberian Thermoelectric Workshop (ITW), 2025 (oral).

- A. Rodriguez-Iglesias, S. Rodriguez-Miguel, J. Santander, I. Martin-Fernández, C. Carbonell, M. Fernández-Regúlez, L. Abad, A. Chatterjee, L. Fonseca, N. Pryds, M. Salleras, **Planar Silicon-Based µTEG Test Platform for Evaluating Thermoelectric Materials and Optimizing Thermal Management**, in: European Conference of Thermoelectrics (ECT), 2025 (oral).
- M. Aceituno, J. Garcia- Masferrer, H. Gómez, A. Rodriguez-Iglesias, I. Molina-Jiménez, I. Martín- Fernández, M. Fernández- Regúlez, J. Santander, L. Fonseca, F. X. Àlvarez, M. Salleras, A. Lopeandia, L. Abad, **Integration of Thin Films and Nanostructuring Techniques to Enhance Thermoelectric Efficiency in Silicon Micro-Thermoelectric Generators**, in: European Conference of Thermoelectrics (ECT), 2025 (oral).

Appendix A

Directed self-assembly of block copolymers

Besides the free-surface self-assembly of BCPs, briefly explained in Section 2.1.9, the lithographic possibilities of BCPs have historically lead to the exploration of routes to precisely control the long range orientation and directionality of the blocks. Generally, the two main DSA routes in thin films are considered to be grapho- and chemo-epitaxy.

Grapho-epitaxy is the most widely used method and involves the fabrication of physical templates to force the BCP reorganization [202]. These templates are referred to as

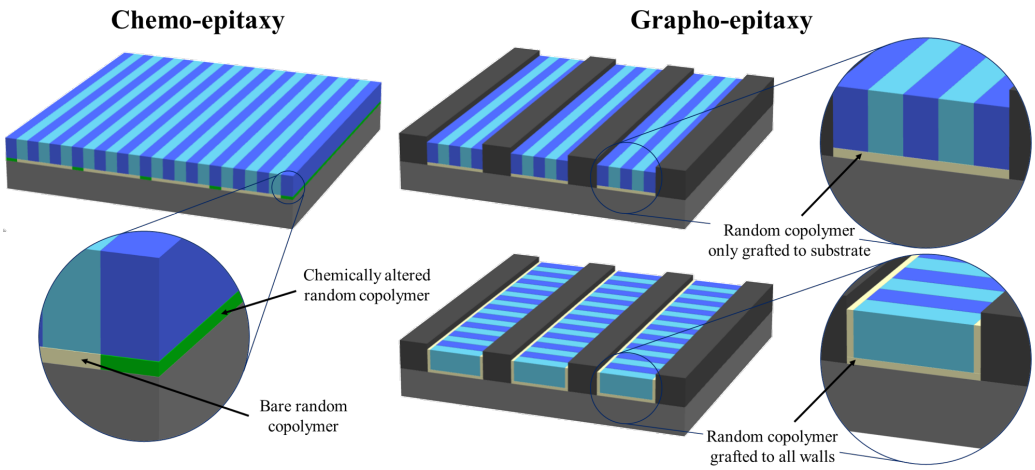


Figure A.1: Schemes of the typical DSA by chemo- and grapho-epitaxy. In the case of chemo-epitaxy the brush layer is chemically altered in different zones. Later, the BCP block with higher affinity to these parts will be forced to occupy them, directing the assembly. In grapho-epitaxy, a physical template is fabricated and the BCP is assembled inside it. If the brush layer is grafted in all walls, the BCP will align perpendicularly to them, while if the brush layer is only grafted in the bottom, the higher affinity of one of the blocks towards the walls causes parallel orientation.

guiding patterns (GPs), and are typically defined using top-down techniques. The brush layer is then grafted to the substrate or to the lateral and bottom walls. Depending on the case, the BCP will be forced to align either parallel or perpendicular to the template walls (see Figure A.1). To obtain well-ordered structures by grapho-epitaxy, an essential requirement is the commensurability of the template with the natural period of the BCP. For parallel alignment, the spacing between walls must be proportional to the period of the block copolymer. Otherwise, the polymer film may experience stretching or compression, introducing defects in the pattern. Large mismatches between the template spacing and the BCP period [203] typically result in clear disruptions of the order and a significant increase in defects. Also, any roughness on the walls can be transferred to the BCP pattern, leading to dislocations.

Chemo-epitaxy, on the other hand, consists of chemically patterning the substrates where the BCPs assemble. In this case, the higher affinity of one of the blocks for the chemically altered regions governs the directionality of the reorganization. The pattern should be as smooth as possible to avoid introducing stress into the BCPs. In order to obtain controlled patterns, the width of these regions is also of utmost importance. To obtain parallel lamellas perpendicularly oriented to the substrate, the width should be 0.5 or 1.5 times the period of the BCP [204], [205].

In both types of epitaxy, alignment is possible for cylindrical and lamellar PS-b-PMMA phases. However, it is more interesting for lamellar domains due to their potential advantages in thermoelectric applications. Lamellar BCPs show two main configurations when confined in parallel trenches, self-assembling either parallel or perpendicular to the template walls (see Figure A.1). Because the self-assembly of lamellar BCPs on a free surface leads to a fingerprint-like pattern, electrical continuity across the film is not maintained. On the contrary, DSA of lamellas with full nanostructuration preserves electrical continuity and improves phonon scattering.

A.1 Guiding pattern fabrication

In this thesis, the work related to the fabrication of guiding patterns (GPs) for lamellar alignment was centered on grapho-epitaxy, with the aim of fabricating physical templates compatible with wafer-scale standard photolithography techniques. The main limitations a GP can have in correctly aligning the BCP are related to the wall profile and the size of the trenches (the larger the template, the greater the difficulty in ensuring good alignment). The machine used to optimize this fabrication was a Stepper NSR 2205i12D i-line, which in principle has a maximum resolution of $\sim$ 400 nm and can expose wafers of 100 mm.

The templates used for this purpose were made with SiO_2. For the fabrication, the wafer is first cleaned in a piranha solution bath (H_2SO_4:H_2O_2 = 3:1) for 10 min, followed by a 10 s dip in 5% HF with 10 min water rinses. Then, the oxide layer is created by means of thermal oxidation in the bulk Si to form a 50 nm thick film. This thickness is chosen to obtain complete filling of the trench while maintaining the BCP thickness similar to that of free surface. The trenches are defined using Stepper photolithography and RIE. The layout design consists of parallel trenches with different periods. The first tests were conducted with 500 nm wide trenches, the results of which can be seen in Figure A.2a, b and c. As observed in Figure A.2a, the photoresist is not completely developed at the end of the photolithography step, leaving some residues at the bottom of the trenches. Figure A.2b shows the result of an etching with these residues still left before the RIE.

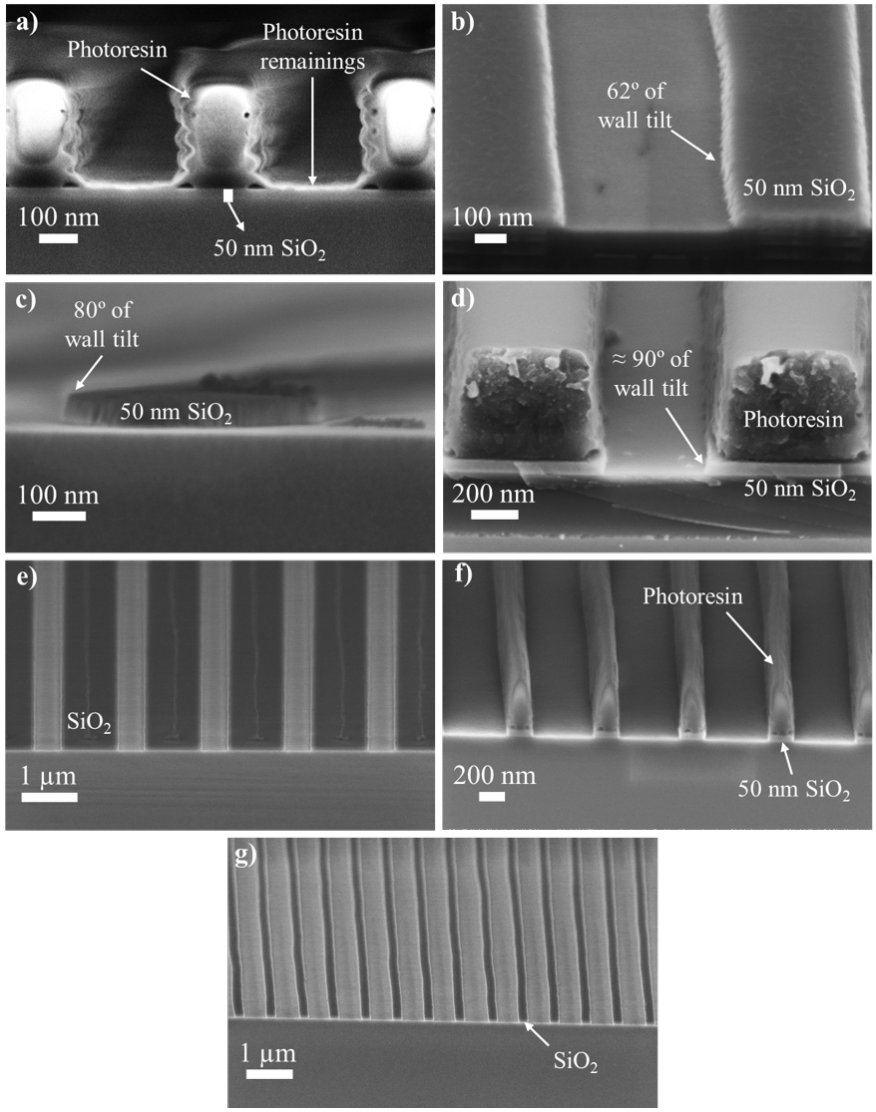


Figure A.2: SEM images of the optimization of the guiding pattern fabrication for BCP alignment. a) Cross-section of the developed photoresist with the presence of < 10 nm residues at the bottom. b) Wall profile of a trench if the photoresist residues are not eliminated. c) Wall profile of a trench if the photoresist residues are eliminated. d) Wall profile of a trench with a width of 400 nm etched in a CMOS-compatible RIE. e) 400 nm width trenches. The area covered by them is $\sim 33\%$. f) Double photolithography exposition using the same mask to increase the number of trenches per area. g) Final trenches layout. Trench width: ~ 400 nm, Period: ~ 600 nm.

This problem can be corrected by introducing an oxygen plasma etching step to eliminate these residues. The wafer is exposed to a rapid low-power process (chamber power: 300 W, oxygen flow: 300 sccm O_2, process time: 45s) to avoid etching all the photoresist. After completing this pre-etching step, the wall profile is improved to be almost vertical. Further optimization was done to reach the 400 nm resolution limit of the Stepper and to improve the wall profile. Two sequential hard baking steps were necessary to ensure that the photoresist could withstand the final RIE recipe. The photoresist is first exposed to UV light for 30 min to undergo pre-curing. This step is used to prevent the photoresist from flowing in the next hard baking processes. Then, it is baked on a hotplate at 230°C for 15 min, followed by a second baking for 30 min. In this last, the temperature is ramped up to 275°C. With this process, trenches with a width of $\sim$ 400 nm and a completely vertical profile were obtained (see Figure A.2d and e).

At this point, trenches near the resolution limit available in our clean room facilities were demonstrated. However, the efficiency of these structures in terms of trench versus chip area is low, as $\sim$ 66% of the chip is not available for BCP alignment. By decreasing the period between trenches to define denser patterns with new masks, resolution problems arise, and the width of the trenches is degraded ($>$ 500 nm). At the end, double exposition was found to be the most reliable procedure to maintain trench widths $\sim$ 400 nm. The final result can be seen in Figure A.2f and g. These results demonstrate a procedure to fabricate dense patterns of parallel trenches by means of standard photolithography, which are compatible with lamellar BCP alignment. Also, these samples were all fabricated at a wafer level.

A.1.1 DSA of lamellar block copolymers

The directed self-assembly of BCPs is similar to free surface self-assembly but requires further optimization of spinning and temperature conditions. Since the interesting alignment for thermoelectric applications is a pattern perpendicularly oriented to the walls of the trenches, lamellar BCPs need a neutral surface affinity towards both these sides and the bottom of the GP. In this way, the orientation of the BCP towards these three surfaces will force the film to be oriented perpendicularly to all the walls. The chips are cleaned in acetone and IPA and then exposed to an oxygen plasma to activate both Si and SiO_2 surfaces (bottom and side walls, respectively). Afterwards, the brush layer is spin-coated at 2000 rpm for 30s to cover all the walls with the random copolymer. The brush is grafted with a 230°C annealing during 5 min. The surplus brush is then eliminated by rinsing the chip in PGMEA using a ultrasound bath. The spinning of the BCP needed optimization of the velocity and weight fraction to deposit BCP only inside the trenches. This was achieved using a spinning velocity of 2500 rpm and a weight fraction of 1% of the BCP in PGMEA. Both annealing time and temperature differ from the optimal values for free surface self-assembly, as proper alignment requires higher diffusion of the BCP molecules. At higher temperatures and annealing times, the organization of the lamellas is enhanced. However, this reaches a threshold beyond which the degradation of the BCP occurs.

Figure A.3 shows a top view and a tilted cross-section of a DSA where the BCP has degraded. The limit at which this kind of BCP degradation appears is diffuse and depends on both the annealing time and temperature. Therefore, the relationship between these parameters can be adjusted to obtain ordered alignment without degradation. For example, BCPs were able to better withstand higher annealing temperatures for short periods of time than lower temperatures for longer durations. Moreover, the thickness

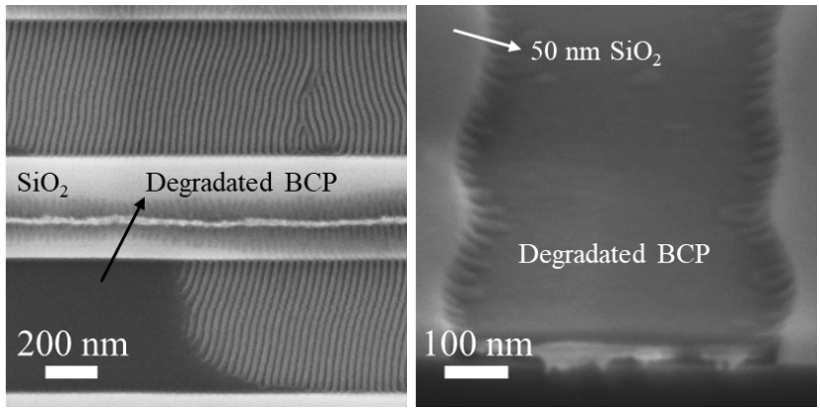


Figure A.3: Top view and tilted cross-section SEM images of a GP with degraded BCP. The degradation is not uniform in the samples, and some areas show degradation before others. After the degradation the BCP melts to form an individual phase where both polymers become indistinguishable.

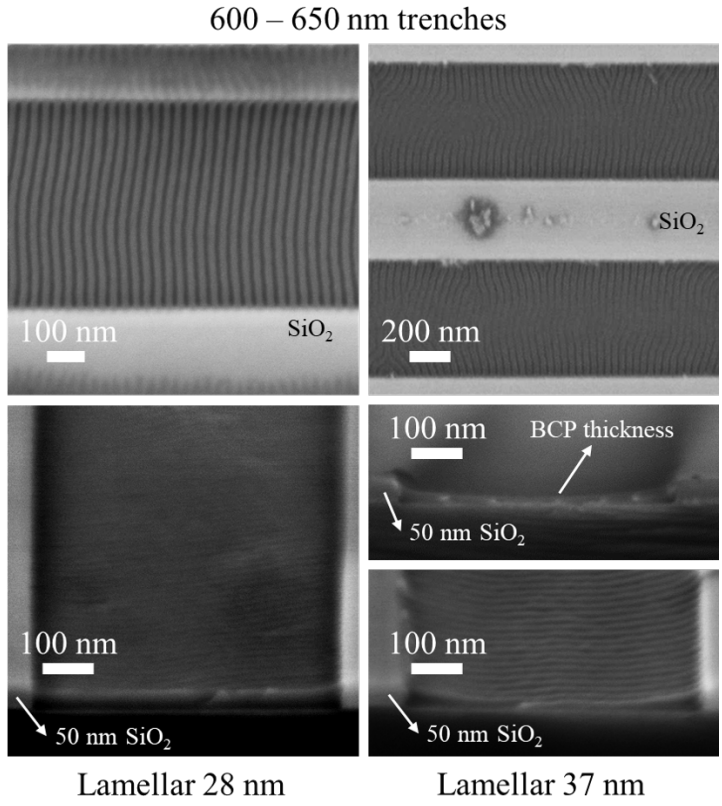


Figure A.4: Top view and tilted cross-section SEM images of a 600-650 nm wide GP with aligned BCPs (L28 and L37). The L28 is aligned with complete trench filling but the L37 can only be reasonably oriented if the thickness of the BCP is reduced to < 25 nm in the center of the trench.

influences the degradation rate of the film, with thicker BCP layers showing greater tolerance. During degradation, the BCP melts to form an individual phase where both polymers become indistinguishable (Figure A.3b).

The length of the trenches is the most critical parameter in the alignment, but the period of the BCP is also important. In the example SEM images shown in Figure 5.1, it is clear that the linearity of the pattern on free surface varies depending on the BCP period. Those with lower periods are more linear. Figure A.4 and Figure A.5 show top view and cross-section images of the alignment of L28 and L37 BCPs in two differently sized trenches (600-650 and 400-450 nm, respectively). The temperatures and annealing times that were found to be optimal ranged in both cases from 295°C for 10 min to 305°C for 7 min. However, these values are already at the limit, which means that in some cases slight degradation of small areas can be observed. The differences between using 600-650 and 400-450 nm trenches are especially noticeable when the BCP period is higher. For the case of L28, good alignment can be obtained in a > 600 nm trench with complete filling. Regarding the reliability of the alignment, proper long-order orientation is better in 400 nm trenches, as the presence of defects is higher in larger trenches. In the 400 nm trenches, the alignment is formed by strictly parallel lamellas in large areas of the

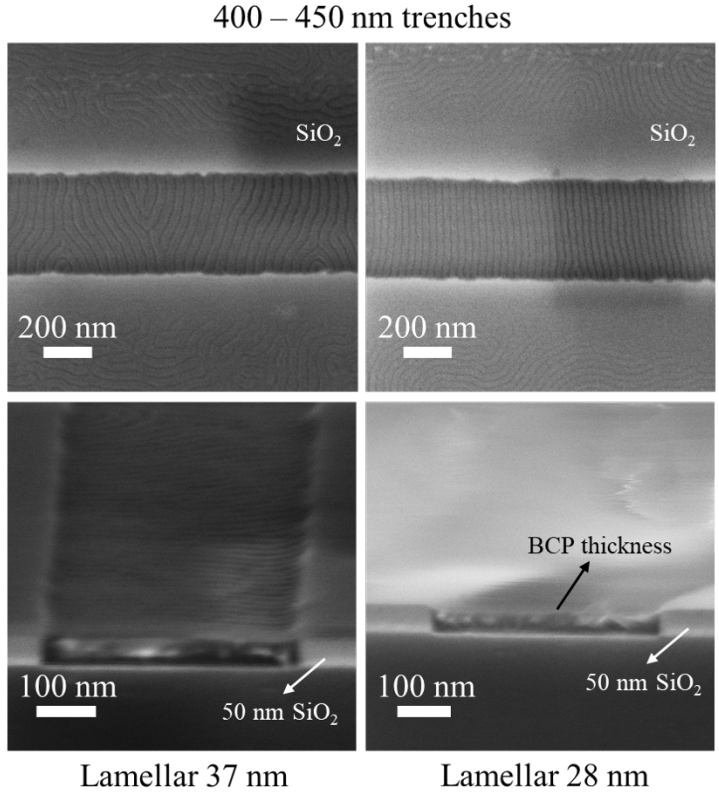


Figure A.5: Top view and tilted cross-section SEM images of a 400-450 nm wide GP with aligned BCPs (L28 and L37). The L28 can be aligned strictly with complete trench filling. The L37 can only be oriented to obtain lamella continuity between the walls, without a strict parallel alignment.

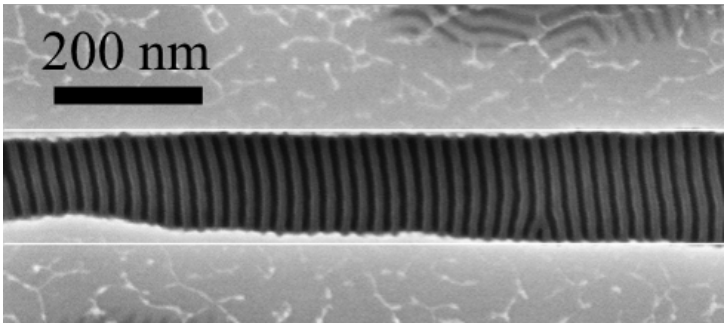


Figure A.6: SEM images of a $\sim$ 200 nm wide defective GP that was fabricated in the etch of a chip with aligned L37 BCP. In this case the orientation of the lamellas is strictly parallel even if the wall shows great roughness. However, no standard photolithography techniques are available in our clean room to fabricate such trenches.

chip, even if there is some wall roughness. The L37 is more sensitive to the length of the trench and its alignment is much more complicated due to its highly curved pattern in free surface. In the trenches of 600 nm, it is impossible to obtain enough alignment to ensure adequate continuity between the walls if complete filling of the trench is done. In this case, the only way to achieve complete continuity is by reducing the thickness inside the trench to $\sim$ 25 nm in the middle of the GP (see Figure A.4 L37). The weight fraction of the BCP in the PGMEA is reduced to 0.5 % during spinning to obtain this result. Taking into account that 8 nm of these are part of the brush, the final thickness of the BCP film itself is below 20 nm. This is not compatible with a pattern transfer because the PS mask cannot withstand the Si etching. By reducing the trenches to 400 nm, this same continuity can be obtained while achieving complete filling of the GP (see Figure A.5 L37). Again, the pattern cannot be forced to be strictly parallel, but the presence of discontinuity defects is minimal. In order to obtain parallel lamellas with the L37, the GPs should be further reduced to $<$ 300 nm. An example of this can be seen in Figure A.6, where parallel L37 lamellas are aligned in a defective trench that was fabricated with $\sim$ 200 nm in width. The filling here is complete. At this level of BCP confinement, the parallel alignment can even be achieved if there is high roughness in the lateral walls.

These results demonstrate the feasibility of aligning lamellar BCPs perpendicularly to the walls of the GPs using templates fabricated through standard photolithography techniques, which are compatible with wafer-scale and CMOS processes. Strictly parallel alignment of the lamellas is achievable only in BCPs with smaller periods; however, continuity between the walls was maintained for all BCPs studied in this thesis while ensuring complete filling of the trenches. This paves the way for the full transfer of the DSA lamellar BCP pattern into the Si film.

Appendix B

Release of membranes using topside KOH etching

The second approach that was explored to suspend ultra-thin Si membranes from the topside of the wafer involved the use of KOH etching and protective layers (see Section 6.2.1 for the BOE approach). These sets of experiments were conducted on diagonal membranes (see Figure B.1). The aim was to take advantage of the anisotropic etching of Si to eliminate it under a non-exposed area (i.e. below the membrane). In SOI samples with a (100) surface orientation, the (111) stopping planes form an inverted pyramid. In this way, defining two overlapping triangles on the sides of a diagonal membrane leads to the same pyramid profile. Lengths of up to 80 µm were fabricated. Two materials were explored as protective layers for KOH: 100 nm thick Si_3N_4 deposited by PECVD and 20 and 50 nm thick HfO_2 deposited by ALD. The results of this procedure are shown in Figure B.1. The chips with Si_3N_4 were suspended for lengths < 50 µm and widths of 10 and 20 µm. The inverted pyramid profile is clearly visible on those chips and demonstrates the reliability of the diagonal design approach. HfO_2 films, instead, could not withstand the KOH etching sufficiently to protect the top Si.

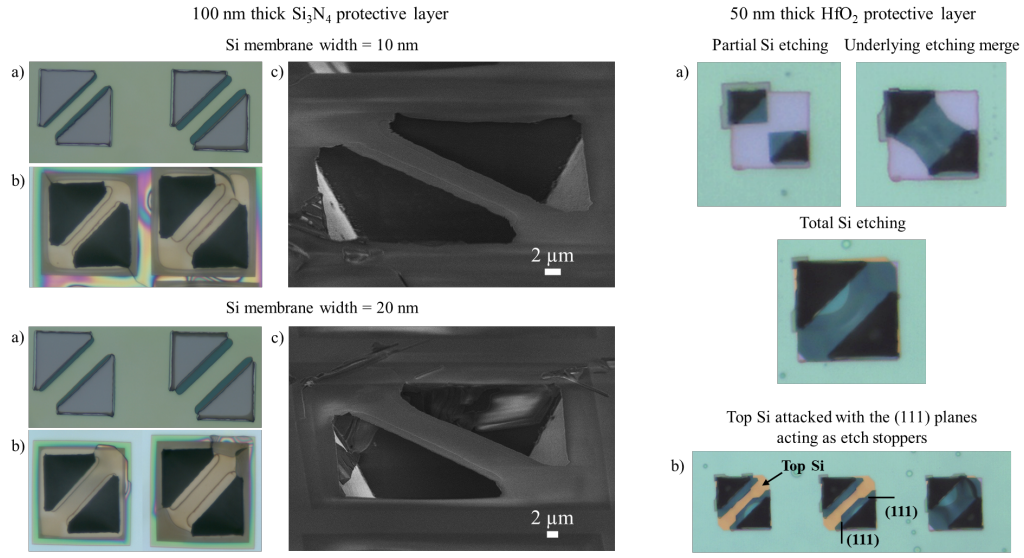


Figure B.1: SEM and optical images on membrane suspension in SOI samples with KOH using Si_3N_4 and HfO_2 as protection layers. On Si_3N_4: a) Optical image of the structure before KOH with two different Si_3N_4 side protection widths (2.5 and 5 µm). The light green regions are Si and Si_3N_4 over Bulk Si/BOX, and the darker areas are only Si_3N_4 over bulk Si/BOX. The gray triangles are the areas where the bulk Si is exposed. b) Optical image of the membranes after suspension. c) SEM images of suspended membranes with 2.5 µm side protection. On HfO_2: a) Optical images on the suspension process. The merging of the two squares is visible. b) Optical images of the structure after KOH. Top Si (golden stripe) is attacked laterally following the (111) planes, indicating that the HfO_2 masking is insufficient.

Appendix C

Adapter piece redesign

As shown in Section 4.2, the µTEGs with integrated heat sink exhibit V_{OC} saturation after enhancing heat exchange with the environment through higher forced convection rates. Since this behavior is caused by the design of the adapter piece, which features silicon corner pillars, some time was also devoted to fabricating a new adapter piece during this thesis.The goal was to minimize the parasitic heat path through the adapter pillars. This appendix presents the simulations and the first fabrication trials carried out.

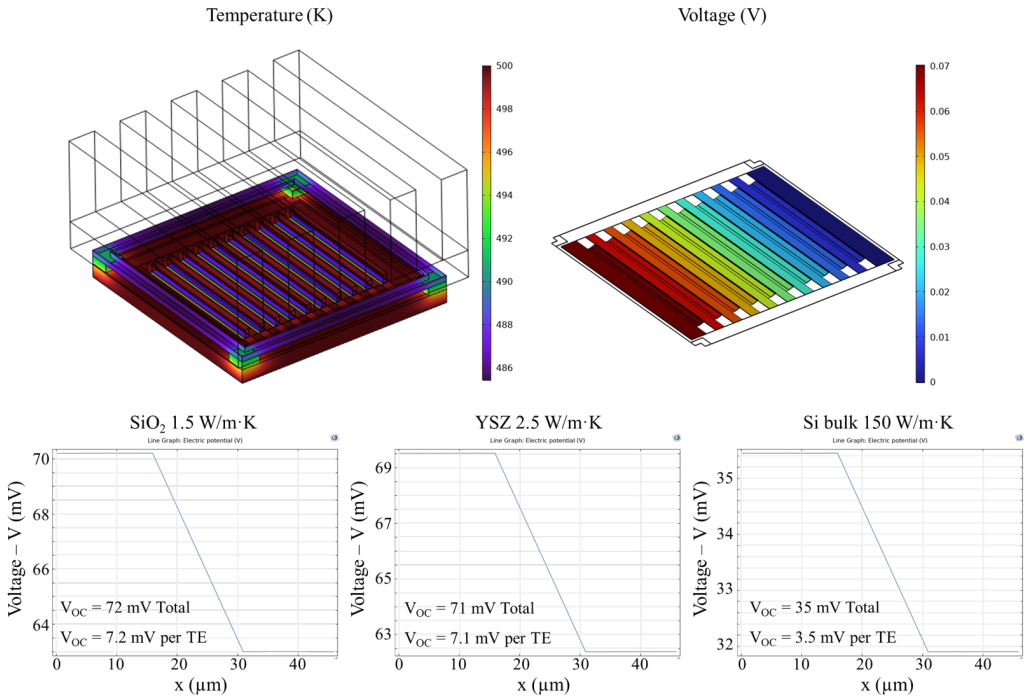


Figure C.1: Temperature and voltage COMSOL simulations with different adapter pillar materials. Three materials were considered for the pillar supports: SiO_2, Yttria-Stabilized Zirconia (YSZ) and bulk Si, each with its corresponding κ.

C.1 Simulations

COMSOL simulations were carried out to assess the V_{OC} enhancement that could be achieved using an adapter with insulating supports (see Figure C.1). The adapter is separated into two different parts: the corner pillars (either made of SiO_2, Yttria-Stabilized Zirconia (YSZ) or bulk Si) and the rest of the piece (i.e. the protuberances that contact the platforms and the upper flat surface). The area of the corner pillars is equivalent to that of the adapter fabricated for the NWs-based µTEGs. Moreover, a heat sink of equivalent size to the one used in this thesis is also incorporated. The cooling is simulated with natural convection heat exchange on the fins of the heat sink to mimic real working conditions. The hot surface is set at 200°C. The results of V_{OC} generation with the different pillar materials can be seen in Figure C.1. A 2.03- and 2.06-fold increase is observed when going from bulk Si to YSZ and SiO_2, respectively, resulting in a 4-fold increase in power generation in the µTEGs.

C.2 Fabrication trials

Adding insulating pillars to the corners of a Si adapter piece introduces several difficulties in assembling the different parts. On the contrary, a simpler approach involves fabricating a self-supporting insulating piece that can be integrated into the µTEG, into which the Si adapter can later be placed. Figure C.2 shows two initial design ideas for this piece. Design a) allows enough space to fit the wire-bonds after its integration, while design b) should be integrated after the wire-bonding. Both have a ring-type geometry and a square support in the center to integrate the Si adapter within it. In all the de-

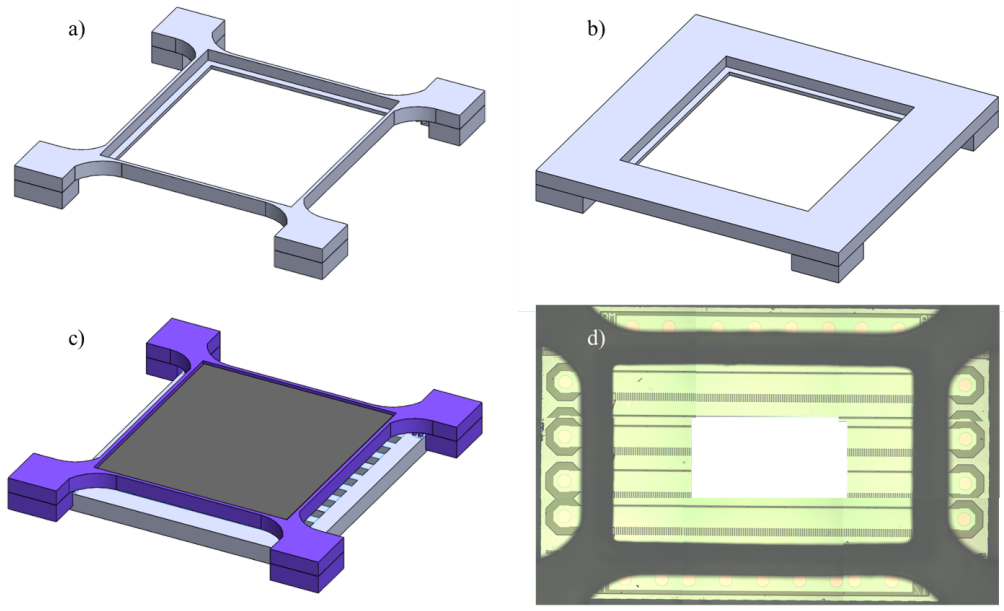


Figure C.2: Initial YSZ piece designs. a) Small ring design. b) Wide ring design. c) 3D model showing the integration of all components with the µTEG. d) Optical images of the a) adapter on top of a µTEG.

signed pieces, the total height of the adapter was calculated to be 350 µm: 150 µm for the supporting pillars and 200 µm for the square support. These should equal the 300 µm-high Si adapter protuberances plus 50 µm of thermal paste. The main limitation of this approach is the flatness of the insulating piece, since if the heights of its four corner pillars are not uniform, the Si adapter will not make uniform contact with the µTEG.

The fabrication of the first generation of insulating pieces was done in collaboration with IREC using 3D printing techniques. The material selected for these was YSZ. The results of the first designs showed good mechanical robustness (especially with design b) of Figure C.2), and good fitting within the µTEGs (see Figure C.2d). However, the Si adapter could not fit inside the square support of the YSZ ring. Furthermore, design a) resulted in significant bending of the piece.

These results led to the second generation of YSZ pieces, shown in Figure C.3. The ring shape of the support was substituted with individual corner supports, avoiding the quoins of the horizontal regions. Moreover, the corners of the four supports feature cylindrical incisions, and a more robust ring is added around the µTEG area. This design exhibited improved mechanical robustness and reduced bending, as well as good compatibility with both the µTEGs and the Si adapters (see Figure C.3h and i). However,

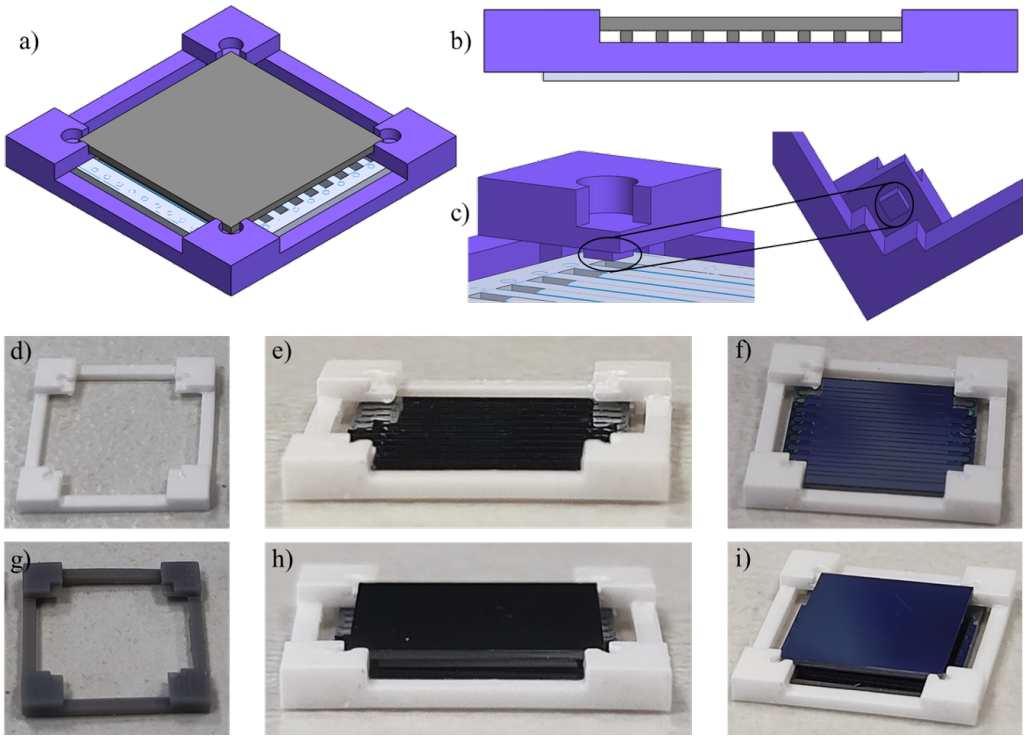


Figure C.3: Second YSZ piece design. a) 3D model showing the integration of all components with the µTEG. b) Lateral view of the integration. c) Closer view of the corner supports and the lower pillars that rest on the bulk of the device. d) Image of the final YSZ piece. e) and f) Different views of the YSZ piece integrated on the µTEG. g) Alternative piece fabricated with a photo-curable resin. h) and i) Different views of all components integrated with the µTEG.

it was impossible to obtain a uniform thermal paste footprint in a dummy µTEG. Confocal microscopy characterization later revealed that the heights of the four corner supports of the ring were unequal. Therefore, this 3D printing method proved incompatible with the height uniformity required to achieve homogeneous contact with the Si adapter.

Alternative micro-machining possibilities were explored. For this purpose, Pyrex wafers were used to investigate the fabrication of SiO_2 pieces. In this case, the design of the piece was simplified to make it compatible with HF etching. Since HF etching is isotropic, four photomask levels were designed to achieve the geometry shown in Figure C.4a. The fabrication consisted of the deposition of two Cr/Au masks on both sides of the wafer. Subsequent photolithographies, followed by metal etching between each metal deposition, defined the layout of each mask. Then, the first 150 µm-deep HF etching pre-defined the inner cross-hole. A subsequent etching step removed the first metal mask. A second HF etching was intended to define the 100 µm-deep corner supports on each side and to remove the remaining 200 µm of the inner cross-hole. However, completing the second HF etching step was impossible due to the peeling of the Au mask.

A new fabrication approach using Pyrex wafers is currently being explored via micro-

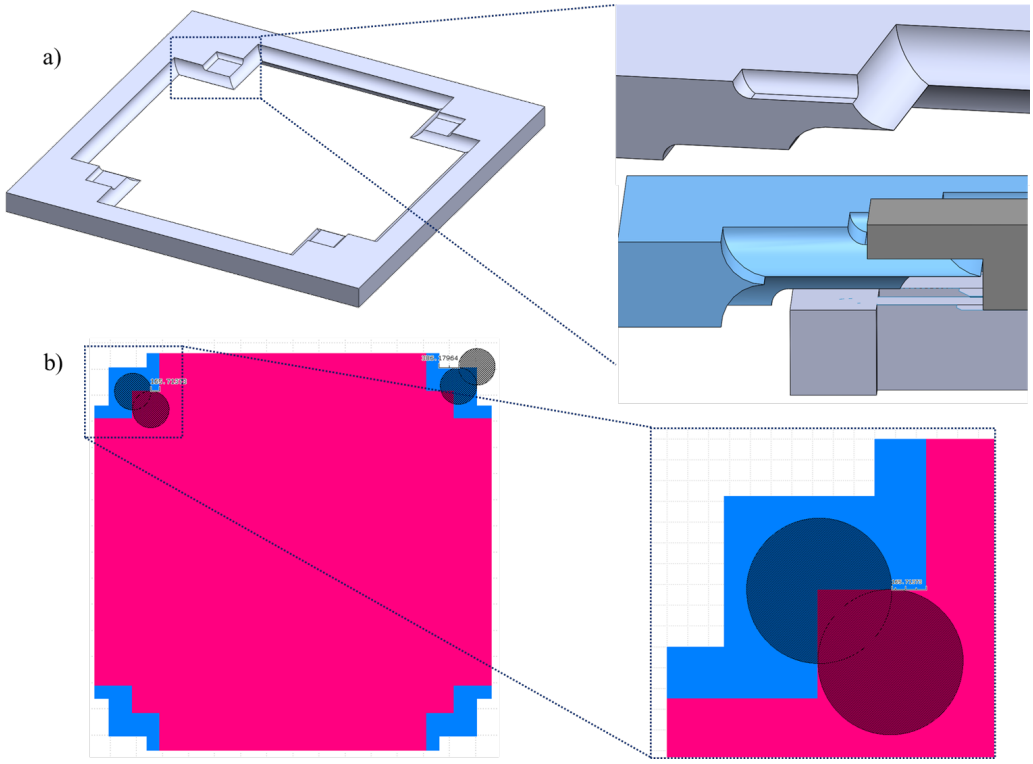


Figure C.4: a) 3D model of the SiO_2 insulating piece. Closer views of the supports and the integration of these with the Si adapter and µTEG are shown on the right. b) Proposal of a two step milling process to fabricate the SiO_2 insulating piece. In pink the milling to the define the upper side supports and pre-define the inner cross-hole. In blue the milling to the define the lower side supports. Additional cylindrical incisions (black circle) are planned to avoid corners. A final milling step would carve out the inner cross-hole of the piece.

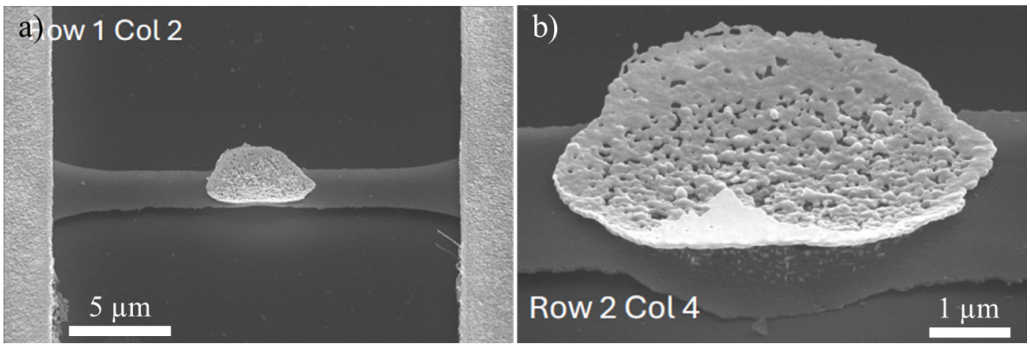
milling, with a design equivalent to that used in the HF process (see Figure C.4b). A first milling (pink area) will define the upper side supports and pre-define the inner cross-hole. Afterwards, a second milling (blue area) will do the same operation on the opposite face of the wafer. Finally, the last milling will carve out the inner cross-hole of the piece. Other possibilities, such as outsourcing the fabrication to private companies, may be considered in the future. Up to now, the fabrication of an insulating piece compatible with full integration has been unsuccessful. Nevertheless, a full assembly should be feasible if sufficient height uniformity is achieved in the piece supports.

Appendix D

Ongoing work on nanostructured films

D.1 FDTR characterization

The fabrication and modeling of the FDTR devices were presented in Section 6.2. To date, initial results were obtained for the reference sample, as shown in Figure D.1. Phase shift curves of different membranes of the same chip were measured using the parameters of Figure D.1c, leading to the expected -90º shift at high frequencies. However, significant variability is observed between the curves of different membranes, whereas the phase shift curves are reproducible over multiple measurements on the same membrane. Two factors may explain this behavior: different transducer roughness on each membrane or variations in membrane geometry. The cause of this variability is currently under study, and several strategies are being planned to identify the primary contributing factor. Bulk samples with the same transducer layer will be measured in different parts of the sample to evaluate whether the specific roughness in each region is the cause. If the transducer roughness itself is not the cause, but rather its effect on the thermal contact resistance (i.e. due to the different contact areas of each transducer), this will be investigated by performing the same measurements on several holey membranes. As previously shown in Section 6.2, the effect of the contact resistance is more dominant in samples with higher κ. Thus, if the variability is lower in holey samples, this could be ascribed to the differences in contact resistance on each membrane. If none of these is the cause, the specific geometry of each membrane should be taken into account when fitting the data. However, since the iterative fitting model is still under development, it is not yet possible to know how significant this variability is for κ calculation. Lastly, it is worth mentioning that, after the characterization of some membranes, detachment of the transducer was observed (see Figure D.1b). Nevertheless, this demonstrates that it is possible to extract a significant signal to measure ultra-thin Si membranes under vacuum using FDTR.



c)

Pump power (µW)	70
Probe power (µW)	60
Pump λ (nm)	400
Probe λ (nm)	532
Vacuum (mbar)	$3 \cdot 10^{-4}$
Laser objective	50x

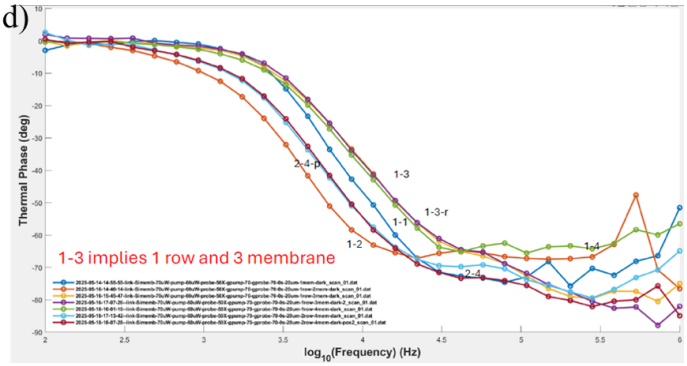


Figure D.1: Initial FDTR results on a bare Si film membrane. a) and b) SEM images of two membranes after FDTR characterization. c) Parameters used for the characterization of the membranes. d) First phase shift plots obtained with the reference membranes.

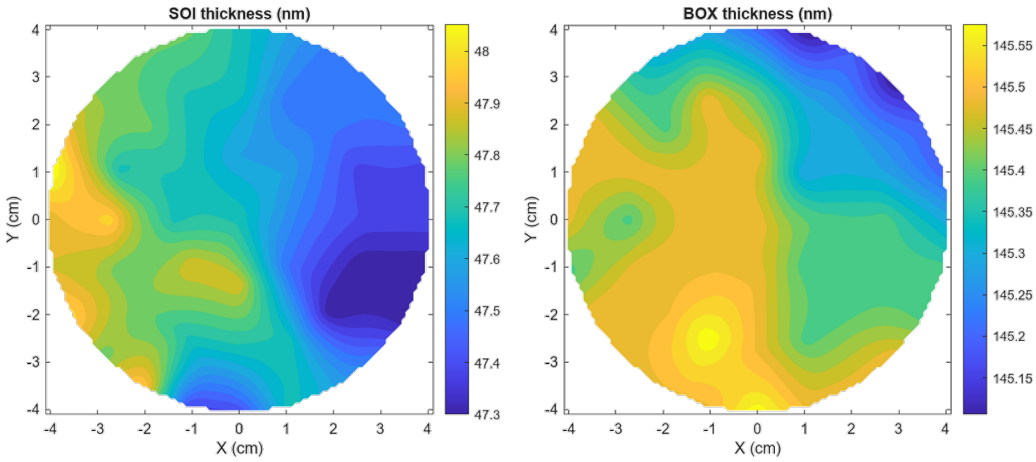


Figure D.2: Thinning of 88nm-thick SOI wafers. Device layer was thinned to 50 nm.

D.2 Thermoelectric generator with optimized Ti-Si contact

A route to successfully fabricate µTEGs with nano-patterned Si films was demonstrated in chapter 7. However, the high contact resistance obtained in these devices, caused by the 700°C RTA, limited their characterization to V_{OC} and Seebeck coefficient. Thanks to the subsequent studies on the contact resistivity of Si–Ti films presented in Section 7.5, this issue was properly assessed. Therefore, a second batch of µTEGs is currently under fabrication. Due to the shortage of the previous SOI wafers with the 50 nm thick top Si layer, different wafers are being used for the new batch. These have a buried oxide of 145 nm and a top Si layer of 88 nm. To achieve an equivalent Si layer thickness of 50 nm, a thinning procedure was developed. This involved an initial oxidation of the top Si to reduce its thickness, followed by HF etching of the grown SiO_2. Example color-maps of the wafer thicknesses after the thinning process can be seen in Figure D.2. With these top Si, µTEGs equivalent to those shown in chapter 7 can be fabricated. Once these µTEGs are completed, the characterization of the power generation will be carried out.

Bibliography

[1] Transforma Insights. "IoT Forecast Highlights". [Online]. Available: https://transformainsights.com/research/forecast/highlights.

[2] Statista. "Number of Internet of Things (IoT) connections worldwide from 2022 to 2023, with forecasts from 2024 to 2033 (in billions)". [Online]. Available: https://www.statista.com/statistics/1183457/iot-connected-devices-worldwide/.

[3] G. Bedi, G. K. Venayagamoorthy, R. Singh, R. Brooks, and K.-C. Wang, "Review of Internet of Things (IoT) in Electric Power and Energy Systems", *IEEE Internet of Things Journal*, vol. 5(2), pp. 847–870, 2018. DOI: 10.1109/jiot.2018.2802704.

[4] M. Haras and T. Skotnicki, "Thermoelectricity for IoT – a review", *Nano Energy*, vol. 10, 2018. DOI: 10.1016/j.nanoen.2018.10.013.

[5] A. Raj and D. Steingart, "Review—Power Sources for the Internet of Things", *Journal of The Electrochemical Society*, vol. 165(8), 2018. DOI: 10.1149/2.0181808jes.

[6] R. Vullers, R. van Schaijk, I. Doms, C. V. Hoof, and R. Mertens, "Micropower energy harvesting", *Solid-State Electronics*, vol. 53(7), pp. 684–693, 2009. DOI: 10.1016/j.sse.2008.12.011.

[7] J. A. Paradiso and T. Starner, "Energy Scavenging for Mobile and Wireless Electronics", *IEEE Pervasive Computing*, vol. 4(1), pp. 18–27, 2005. DOI: 10.1109/mprv.2005.9.

[8] Z. Wan, Y. Tan, and C. Yuen, "Review on energy harvesting and energy management for sustainable wireless sensor networks", *IEEE 13th International Conference on Communication Technology*, 2011. DOI: 10.1109/icct.2011.6157897.

[9] A. Firth, B. Zhang, and A. Yang, "Quantification of global waste heat and its environmental effects", *Applied Energy*, vol. 235, pp. 1314–1334, 2019. DOI: 10.1016/j.apenergy.2018.10.102.

[10] C. Forman, I. K. Muritala, R. Pardemann, and B. Meyer, "Estimating the global waste heat potential", *Renewable and Sustainable Energy Reviews*, vol. 57, pp. 1568–1579, 2016. DOI: 10.1016/j.rser.2015.12.192.

[11] O. Farhat, J. Faraj, F. Hachem, C. Castelain, and M. Khaled, "A recent review on waste heat recovery methodologies and applications: Comprehensive review, critical analysis and potential recommendations", *Cleaner Engineering and Technology*, vol. 6, 2022. DOI: 10.1016/j.clet.2021.100387.

[12] C. Haddad, C. Périlhon, A. Danlos, M.-X. François, and G. Descombes, "Some Efficient Solutions to Recover Low and Medium Waste Heat: Competitiveness of the Thermoacoustic Technology", *Energy Procedia*, vol. 50, pp. 1056–1069, 2014. DOI: 10.1016/j.egypro.2014.06.125.

[13] H. Jouhara, N. Khordehgah, S. Almahmoud, B. Delpech, A. Chauhan, and S. A. Tassou, "Waste heat recovery technologies and applications", *Thermal Science and Engineering Progress*, vol. 6, pp. 268–289, 2014. DOI: 10.1016/j.tsep.2018.04.017.

[14] A. O. Ochieng, T. F. Megahed, S. Ookawara, and H. Hassan, "Comprehensive review in waste heat recovery in different thermal energy-consuming processes using thermoelectric generators for electrical power generation", *Process Safety and Environmental Protection*, vol. 162, pp. 134–154, 2022. DOI: 10.1016/j.psep.2022.03.070.

[15] L. E. Bell, "Cooling, Heating, Generating Power, and Recovering Waste Heat with Thermoelectric Systems", *Science*, vol. 321(5895), pp. 1457–1461, 2008. DOI: 10.1126/science.1158899.

[16] H. Mamur, M. Bhuiyan, F. Korkmaz, and M. Nil, "A review on bismuth telluride (Bi2Te3) nanostructure for thermoelectric applications", *Renewable and Sustainable Energy Reviews*, vol. 82(3), pp. 4159–4169, 2018. DOI: 10.1016/j.rser.2017.10.112.

[17] A. Tarancón, "Powering the IoT revolution with heat", *Nature Electronics*, 2019. DOI: 10.1038/s41928-019-0276-4.

[18] A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W. A. G. III, and J. R. Heath, "Silicon nanowires as efficient thermoelectric materials", *Nature*, vol. 451, pp. 168–171, 2008. DOI: 10.1038/nature06458.

[19] A. I. Hochbaum et al., "Enhanced thermoelectric performance of rough silicon nanowires", *Nature*, vol. 451, pp. 163–167, 2008. DOI: 10.1038/nature06381.

[20] E. J. Sandoz-Rosado, S. J. Weinstein, and R. J. Stevens, "On the Thomson effect in thermoelectric power devices", *International Journal of Thermal Sciences*, vol. 66, pp. 1–7, 2013. DOI: 10.1016/j.ijthermalsci.2012.10.018.

[21] H. Liang, "Electrical and Thermal Load Matching of Thermoelectric Power Generation Systems", *Journal of Electronic Materials*, vol. 51, pp. 3950–3957, 2022. DOI: 10.1007/s11664-022-09645-0.

[22] A. Attar, H. Lee, and G. J. Snyder, "Optimum load resistance for a thermoelectric generator system", *Energy Conversion and Management*, vol. 226, 2020. DOI: 10.1016/j.enconman.2020.113490.

[23] Z. Wu, S. Zhang, Z. Liu, E. Mu, and Z. Hu, "Thermoelectric converter: Strategies from materials to device application", *Nano Energy*, vol. 91, 2022. DOI: 10.1016/j.nanoen.2021.106692.

[24] L. D. Hicks and M. S. Dresselhaus, "Effect of quantum-well structures on the thermoelectric figure of merit", *Physical Review B*, vol. 47(19), pp. 12 727–12 731, 1993. DOI: 10.1103/physrevb.47.12727.

[25] X. Gu, S. Li, and H. Bao, "Thermal conductivity of silicon at elevated temperature: Role of four-phonon scattering and electronic heat conduction", *International Journal of Heat and Mass Transfer*, vol. 160, 2020. DOI: 10.1016/j.ijheatmasstransfer.2020.120165.

[26] C. J. Glassbrenner and G. A. Slack, "Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point", *Physical Reviews*, vol. 134, 1964. DOI: 10.1103/PhysRev.134.A1058.

[27] M. W. Wu, N. J. M. Horing, and H. L. Cui, "Phonon-drag effects on thermoelectric power", *Physical Review B*, vol. 54(8), pp. 5438–5443, 1996. DOI: 10.1103/physrevb.54.5438.

[28] M. Cutler, J. F. Leavy, and R. L. Fitzpatrick, "Electronic Transport in Semimetallic Cerium Sulfide", *Physical Review*, vol. 133(4A), A1143–A1152, 1964. DOI: 10.1103/physrev.133.a1143.

[29] G. J. Snyder and E. S. Toberer, "Complex thermoelectric materials", *Nature Materials*, vol. 7(2), pp. 105–114, 2008. DOI: 10.1038/nmat2090.

[30] Z. Dughaish, "Lead telluride as a thermoelectric material for thermoelectric power generation", *Physica B: Condensed Matter*, vol. 322(1-2), pp. 205–223, 2002. DOI: 10.1016/s0921-4526(02)01187-0.

[31] M. Telkes, "The Efficiency of Thermoelectric Generators. I.", *Journal of Applied Physics*, vol. 18, pp. 1116–1127, 1947. DOI: 10.1063/1.1697593.

[32] H. J. Goldsmid and R. W. Douglas, "The use of semiconductors in thermoelectric refrigeration", *British Journal of Applied Physics*, vol. 5, p. 386, 1947. DOI: 10.1088/0508-3443/5/11/303.

[33] D. Beretta et al., "Thermoelectrics: From history, a window to the future", *Materials Science and Engineering: R: Reports*, 2018. DOI: 10.1016/j.mser.2018.09.001.

[34] M.Rull-Bravo, A. Moure, J. Fernández, and M. Martín-González, "Skutterudites as thermoelectric materials: revisited", *RSC Advances*, vol. 5(52), pp. 41 653–41 667, 2015. DOI: 10.1039/c5ra03942h.

[35] H. Goldsmid, *Introduction to Thermoelectricity*. Springer, Berlin Heidelberg, 2016.

[36] Y. I. Ravich, B. A. Efimova, and I. A. Smirnov, *Semiconducting Lead Chalcogenides*. Springer US, 1970.

[37] K. F. Hsu et al., "Cubic AgPbmSbTe2+m: Bulk Thermoelectric Materials with High Figure of Merit", *Science*, vol. 303(5659), pp. 818–821, 2004. DOI: 10.1126/science.1092963.

[38] G. Tan et al., "Non-equilibrium processing leads to record high thermoelectric figure of merit in PbTe–SrTe", *Nature Communications*, vol. 7, 2016. DOI: 10.1038/ncomms12167.

[39] J. He et al., "Role of Sodium Doping in Lead Chalcogenide Thermoelectrics", *Journal of the American Chemical Society*, vol. 135(12), pp. 4624–4627, 2013. DOI: 10.1021/ja312562d.

[40] C. C et al., "3D charge and 2D phonon transports leading to high out-of-plane ZT in n-type SnSe crystals", *Science*, vol. 360(6390), pp. 778–783, 2018. DOI: 10.1126/science.aaq1479.

[41] Z. LD et al., "Ultrahigh power factor and thermoelectric performance in hole-doped single-crystal SnSe", *Science*, vol. 351(6269), pp. 141–444, 2016. DOI: 10.1126/science.aad3749.

[42] G. Rogl et al., "In-doped multifilled n-type skutterudites with ZT=1.8", *Acta Materialia*, vol. 95, pp. 201–211, 2015. DOI: 10.1016/j.actamat.2015.05.024.

[43] J. F. T. Caillat and A. Borshchevsky, "Preparation and thermoelectric properties of semiconducting Zn4Sb3", *Journal of Physics and Chemistry of Solids*, vol. 58(7), pp. 1119–1125, 1997. DOI: 10.1016/s0022-3697(96)00228-4.

[44] J. Yu et al., "Unique Role of Refractory Ta Alloying in Enhancing the Figure of Merit of NbFeSb Thermoelectric Materials", *Advanced Energy Materials*, vol. 8(1), 2018. DOI: 10.1002/aenm.201701313.

[45] J. Zhang, L. Song, S. H. Pedersen, H. Yin, L. T. Hung, and B. B. Iversen, "Discovery of high-performance low-cost n-type Mg3Sb2-based thermoelectric materials with multi-valley conduction bands", *Nature communications*, vol. 8, 2017. DOI: 10.1038/ncomms13901.

[46] S. R. Brown, S. M. Kauzlarich, F. Gascoin, and G. J. Snyder, "New High Efficiency Thermoelectric Material for Power Generation", *American Chemical Society*, vol. 18(7), pp. 1873–1877, 2006. DOI: 10.1021/cm060261t.

[47] *Life Testing of Yb14MnSb11 for High Performance Thermoelectric Couples*, 2011.

[48] V. L. Kuznetsov, L. A. Kuznetsova, A. E. Kaliazin, and D. M. Rowe, "Preparation and thermoelectric properties of A8IIB16IIIB30IV clathrate compounds", *Journal of Applied Physics*, vol. 87(11), pp. 7871–7875, 2000. DOI: 10.1063/1.373469.

[49] Y. Saiga, B. Du, S. Deng, K. Kajisa, and T. Takabatake, "Thermoelectric properties of type-VIII clathrate Ba8Ga16Sn30 doped with Cu", *Journal of Alloys and Compounds*, vol. 537, pp. 303–307, 2012. DOI: 10.1016/j.jallcom.2012.05.049.

[50] M. Schwall and B. Balke, "Phase separation as a key to a thermoelectric high efficiency", *Phys. Chem. Chem. Phys.*, vol. 15(6), pp. 1868–1872, 2013. DOI: 10.1039/c2cp43946h.

[51] X. Yan et al., "Stronger phonon scattering by larger differences in atomic mass and size in p-type half-Heuslers Hf1xTixCoSb0.8Sn0.2", *Energy Environmental Science*, vol. 5(6), 2012. DOI: 10.1039/c2ee21554c.

[52] M. Ohtaki, K. Araki, and K. Yamamoto, "High Thermoelectric Performance of Dually Doped ZnO Ceramics", *Journal of Electronic Materials*, vol. 38(7), pp. 1234–1238, 2006. DOI: 10.1007/s11664-009-0816-1.

[53] G. Cerretti, B. Balke, G. Kieslich, and W. Tremel, "Towards higher zT in early transition metal oxides: optimizing the charge carrier concentration of the WO 3-x compounds", *Materials Today: Proceedings*, vol. 5(4), pp. 10 240–10 248, 2018. DOI: 10.1016/j.matpr.2017.12.271.

[54] Y.-L. Pei, H. Wu, D. Wu, F. Zheng, and J. He, "High Thermoelectric Performance Realized in a BiCuSeO System by Improving Carrier Mobility through 3D Modulation Doping", *Journal of the American Chemical Society*, vol. 136(39), pp. 13 902–13 908, 2014. DOI: 10.1021/ja507945h.

[55] S. Saini, H. S. Yaddanapudi, K. Tian, Y. Yin, D. Magginetti, and A. Tiwari, "Terbium Ion Doping in Ca3Co4O9: A Step towards High-Performance Thermoelectric Materials", *Scientific Reports*, vol. 7(1), 2017. DOI: 10.1038/srep44621.

[56] B. Russ, A. Glaudell, J. J. Urban, M. L. Chabinyc, and R. A. Segalman, "Organic thermoelectric materials for energy harvesting and temperature control", *Nature Reviews Materials*, vol. 1(10), 2016. DOI: 10.1038/natrevmats.2016.50.

[57] K. C. See, J. P. Feser, C. E. Chen, A. Majumdar, J. J. Urban, and R. A. Segalman, "Water-Processable PolymerNanocrystal Hybrids for Thermoelectrics", *Nano Letters*, vol. 10(11), pp. 4664–4667, 2010. DOI: 10.1021/nl102880k.

[58] K. Zhang, Y. Zhang, and S. Wang, "Enhancing thermoelectric properties of organic composites through hierarchical nanostructures", *Scientific Reports*, vol. 3(1), 2013. DOI: 10.1038/srep03448.

[59] B. A. MacLeod et al., "Large n- and p-type thermoelectric power factors from doped semiconducting single-walled carbon nanotube thin films", *Energy Environmental Science*, vol. 10(10), pp. 2168–2179, 2017. DOI: 10.1039/c7ee01130j.

[60] V. Kessler et al., "Thermoelectric Properties of Nanocrystalline Silicon from a Scaled-Up Synthesis Plant", *Advanced Engineering Materials*, vol. 15(5), pp. 379–385, 2012. DOI: 10.1002/adem.201200233.

[61] K. Valalaki, P. Benech, and A. G. Nassiopoulou, "High Seebeck Coefficient of Porous Silicon: Study of the Porosity Dependence", *Nanoscale Research Letters*, vol. 11(1), 2016. DOI: 10.1186/s11671-016-1411-z.

[62] P. Ferrando-Villalba et al., "In-plane thermal conductivity of sub-20 nm thick suspended mono-crystalline Si layers", *Nanotechnology*, vol. 25(18), 2014. DOI: 10.1088/0957-4484/25/18/185402.

[63] G. Pennelli, E. Dimaggio, and M. Macucci, "Thermal Conductivity Reduction in Rough Silicon Nanomembranes", *IEEE Transactions on Nanotechnology*, vol. 17(3), pp. 500–505, 2018. DOI: 10.1002/adem.201200233.

[64] R. Yanagisawa, N. Tsujii, T. Mori, P. Ruther, O. Paul, and M. Nomura, "Nanostructured planar-type uni-leg Si thermoelectric generators", *Applied Physics Express*, vol. 13, 2020. DOI: 10.35848/1882-0786/aba5c4.

[65] L. Yang et al., "High thermoelectric figure of merit of porous Si nanowires from 300 to 700K", *Nature Communications*, vol. 12(1), 2021. DOI: 10.1038/s41467-021-24208-3.

[66] Y. Zhao et al., "Engineering the thermal conductivity along an individual silicon nanowire by selective helium ion irradiation", *Nature Communications*, vol. 8, 2017. DOI: 10.1038/ncomms15919.

[67] M. C. Wingert et al., "Thermal Conductivity of Ge and Ge–Si Core–Shell Nanowires in the Phonon Confinement Regime", *Nano Letters*, vol. 11(12), pp. 5507–5513, 2011. DOI: 10.1021/nl203356h.

[68] G. Gesele, J. Linsmeier, V. Drach, J. Fricke, and R. Arens-Fischer, "Temperature-dependent thermal conductivity of porous silicon", *Journal of Physics D: Applied Physics*, vol. 30(21), pp. 2911–2916, 1997. DOI: 10.1088/0022-3727/30/21/001.

[69] N. S. Bennett, D. Byrne, A. Cowley, and N. Neophytou, "Dislocation loops as a mechanism for thermoelectric power factor enhancement in silicon nano-layers", *Applied Physics Letters*, vol. 109(17), 2016. DOI: 10.1063/1.4966686.

[70] J. de Boor et al., "Thermoelectric properties of porous silicon", *Applied Physics A*, vol. 107, pp. 789–794, 2012. DOI: 10.1007/s00339-012-6879-5.

[71] N. K. Upadhyay et al., "Enhancement in thermoelectric performance of bulk CrSi 2 dispersed with nanostructured SiGe nanoinclusions", *Journal of Alloys and Compounds*, vol. 765, pp. 412–417, 2018. DOI: 10.1016/j.jallcom.2018.06.175.

[72] S. L. Tonquesse et al., "Influence of Stoichiometry and Aging at Operating Temperature on Thermoelectric Higher Manganese Silicides", *Chemistry of Materials*, vol. 32(24), pp. 10 601–10 609, 2020. DOI: 10.1021/acs.chemmater.0c03714.

[73] T. Zhang, S. Wu, J. Xu, R. Zheng, and G. Cheng, "High thermoelectric figure-of-merits from large-area porous silicon nanowire arrays", *Nano Energy*, vol. 13, pp. 433–441, 2015. DOI: 10.1016/j.nanoen.2015.03.011.

[74] L. Yang et al., "High thermoelectric figure of merit of porous Si nanowires from 300 to 700K", *Nature Communications*, vol. 12, 2021. DOI: 10.1038/s41467-021-24208-3.

[75] L. Yang et al., "Scalable Multi-nanostructured Silicon for Room-Temperature Thermoelectrics", *ACS Applied Energy Materials*, vol. 2(10), pp. 7083–7091, 2019. DOI: 10.1021/acsaem.9b00893.

[76] E. K. Lee et al., "Large Thermoelectric Figure-of-Merits from SiGe Nanowires by Simultaneously Measuring Electrical and Thermal Transport Properties", *Nano Letters*, vol. 12(6), pp. 2918–2923, 2012. DOI: 10.1021/nl300587u.

[77] K.-M. Lee, S.-K. Lee, and T.-Y. Choi, "Highly enhanced thermoelectric figure of merit of a -SiC nanowire with a nanoelectromechanical measurement approach", *Applied Physics A*, vol. 106, pp. 955–960, 2012. DOI: 10.1007/s00339-011-6718-0.

[78] F. Zhou, J. Szczech, M. T. Pettes, A. L. Moore, S. Jin, and L. Shi, "Determination of Transport Properties in Chromium Disilicide Nanowires via Combined Thermoelectric and Structural Characterizations", *Nano Letters*, vol. 7(6), pp. 1649–1654, 2007. DOI: 10.1021/nl0706143.

[79] D. Banerjee et al., "Elevated thermoelectric figure of merit of n-type amorphous silicon by efficient electrical doping process", *Nano Energy*, vol. 44, pp. 89–94, 2018. DOI: 10.1016/j.nanoen.2017.11.060.

[80] J. Tang et al., "Holey Silicon as an Efficient Thermoelectric Material", *Nano Letters*, vol. 10(10), pp. 4279–4283, 2010. DOI: 10.1021/nl102931z.

[81] Y. Nakamura et al., "Anomalous reduction of thermal conductivity in coherent nanocrystal architecture for silicon thermoelectric material", *Nano Energy*, vol. 12, pp. 845–851, 2015. DOI: 10.1016/j.nanoen.2014.11.029.

[82] K. Ziouche, I. Bel-Hadj, and Z. Bougrioua, "Thermoelectric properties of nanostructured porous-polysilicon thin films", *Nano Energy*, vol. 80, 2021. DOI: 10.1016/j.nanoen.2020.105553.

[83] T. Taniguchi et al., "Thermoelectric Si1xGex and Ge epitaxial films on Si(001) with controlled composition and strain for group IV element-based thermoelectric generators", *Applied Physics Letters*, vol. 117(14), 2020. DOI: 10.1063/5.0023820.

[84] M. M. Timm et al., "Enhancing Thermoelectric Efficiency in CrSi2 Films through Al Ion Implantation-Induced Energy Filtering", *ACS Applied Electronic Materials*, vol. 7(1), pp. 246–252, 2025. DOI: 10.1021/acsaelm.4c01660.

[85] Y. Kurokawa et al., "Thermoelectric properties of Mg2Si thin films prepared by thermal evaporation of Mg and face-to-face annealing", *Materials Science in Semiconductor Processing*, vol. 163, 2023. DOI: 10.1016/j.mssp.2023.107552.

[86] D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, and A. Majumdar, "Thermal conductivity of individual silicon nanowires", *Applied Physics Letters*, vol. 83(14), pp. 2934–2936, 2003. DOI: 10.1063/1.1616981.

[87] W. Liu and M. Asheghi, "Thermal Conductivity Measurements of Ultra-Thin Single Crystal Silicon Layers", *Journal of Heat Transfer*, vol. 128(1), 2006. DOI: 10.1115/1.2130403.

[88] R. Yanagisawa, N. Tsujii, T. Mori, P. Ruther, O. Paul, and M. Nomura, "Nanostructured planar-type uni-leg Si thermoelectric generators", *Applied Physics Express*, vol. 13(9), 2020. DOI: 10.35848/1882-0786/aba5c4.

[89] J. Lim et al., "Simultaneous Thermoelectric Property Measurement and Incoherent Phonon Transport in Holey Silicon", *ACS Applied Electronic Materials*, vol. 10(1), pp. 124–132, 2016. DOI: 10.1021/acsnano.5b05385.

[90] N. Liu, T. Zhu, M. Rosul, J. Peters, J. Bowers, and M. Zebarjadi, "Thermoelectric properties of holey silicon at elevated temperatures", *Materials Today Physics*, vol. 14, 2020. DOI: 10.1016/j.mtphys.2020.100224.

[91] T. M. Tritt and M. A. Subramanian, "Thermoelectric Materials, Phenomena, and Applications: A Bird's Eye View", *MRS Bulletin*, vol. 31, pp. 188–198, 2006. DOI: 10.1557/mrs2006.44.

[92] J. Yan, X. Liao, D. Yan, and Y. Chen, "Review of Micro Thermoelectric Generator", *Journal of Microelectromechanical Systems*, vol. 1, pp. 1–18, 2018. DOI: 10.1109/JMEMS.2017.2782748.

[93] R. L. Cataldo and G. L. Bennett, "U.S. Space Radioisotope Power Systems and Applications: Past, Present and Future", *Radioisotopes - Applications in Physical Sciences*, 2011. DOI: 10.5772/23914.

[94] D. Champier, "Thermoelectric generators: A review of applications", *Energy Conversion and Management*, vol. 140, pp. 167–181, 2018. DOI: 10.1016/j.enconman.2017.02.070.

[95] Q. Luo et al., "A Thermoelectric Waste-Heat-Recovery System for Portland Cement Rotary Kilns", *Journal of Electronic Materials*, vol. 44, pp. 1750–1762, 2015. DOI: 10.1007/s11664-014-3543-1.

[96] S. Kotanagi and A. Matoge and Y. Yoshida and U. Fumiyasu and M. Kishi. "Timepiece and portable electronic device having thermoelectric generator unit, U.S. Patent US6 359 841". [Online]. Available: patents.google.com/patent/US6359841/%2030.

[97] C. B. Vining, "An inconvenient truth about thermoelectrics", *Nature Materials*, vol. 8, pp. 83–85, 2009, ISSN: 1476-4660. DOI: 10.1038/nmat2361.

[98] I. D. Noyan et al., "SiGe nanowire arrays based thermoelectric microgenerator", *Nano Energy*, vol. 57, pp. 492–499, 2019. DOI: 10.1016/j.nanoen.2018.12.050.

[99] S. E. Oualid et al., "Innovative design of bismuth-telluride-based thermoelectric micro-generators with high output power", *Energy Environmental Science*, vol. 13, pp. 3579–3591, 2020. DOI: 10.1039/D0EE02579H.

[100] G. Hu, H. Edwards, and M. Lee, "ilicon integrated circuit thermoelectric generators with a high specific power generation capacity", *Nature Electronics*, 2019. DOI: 10.1038/s41928-019-0271-9.

[101] R. Yanagisawa, N. Tsujii, T. Mori, P. Ruther, O. Paul, and M. Nomura, "Nanostructured planar-type uni-leg Si thermoelectric generators", *Applied Physics Express*, 2020. DOI: 10.35848/1882-0786/aba5c4.

[102] S. Lal, D. Gautam, and K. M. Razeeb, "Fabrication of micro-thermoelectric devices for power generation and the thermal management of photonic devices", *Journal of Micromechanics and Microengineering*, vol. 29(6), 2019. DOI: 10.1088/1361-6439/ab18f1.

[103] S. Koike, R. Yanagisawa, M. Kurosawa, and M. Nomura, "Design of a planar-type uni-leg SiGe thermoelectric generator", *Japanese Journal of Applied Physics*, vol. 59, 2020. DOI: 10.35848/1347-4065/ab9d5e.

[104] H. Matsuo, K. Yoshitoku, M. Saito, H. Takahashi, I. Terasaki, and T. Homma, "Fabrication of ZnO-Based Thermoelectric Micro-Devices by Electrodeposition", *Journal of The Electrochemical Society*, vol. 165, 2018. DOI: 10.1149/2.0021810jes.

[105] S. Asadikouhanjani, A. Zolfagharian, and M. Bodaghi, "Design and Fabrication of Microarchitected Thermoelectric Generators: Prospects and Challenges", *Advanced Enineering Materials*, vol. 26(6), pp. 3579–3591, 2024. DOI: 10.1002/adem.202301609.

[106] R. Yanagisawa et al., "High-power-density hybrid planar-type silicon thermoelectric generator with phononic nanostructures", *Materials Today Physics*, vol. 45, 2024. DOI: 10.1016/j.mtphys.2024.101452.

[107] H. Hu, M. Gopinadhan, and C. O. Osuji, "Directed self-assembly of block copolymers: a tutorial review of strategies for enabling nanotechnology with soft matter", *Soft Matter*, vol. 10(22), 2014. DOI: 10.1039/c3sm52607k.

[108] R. A. Farrell, T. G. Fitzgerald, D. Borah, J. D. Holmes, and M. A. Morris, "Chemical Interactions and Their Role in the Microphase Separation of Block Copolymer Thin Films", *International Journal of Molecular Sciences*, vol. 10(9), pp. 3671–3712, 2009. DOI: 10.3390/ijms10093671.

[109] L. Leibler, "Theory of Microphase Separation in Block Copolymers", *Macromolecules*, vol. 13(6), pp. 1602–1617, 2009. DOI: 10.1021/ma60078a047.

[110] X. Gu, I. Gunkel, and T. P. Russell, "Pattern transfer using block copolymers", *Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 371(2000), pp. 1602–1617, 2013. DOI: 10.1098/rsta.2012.0306.

[111] P. Maji and K. Naskar, "Styrenic block copolymer-based thermoplastic elastomers in smart applications: Advances in synthesis, microstructure, and structure–property relationships—A review", *Journal of Applied Polymer Science*, vol. 139(39), 2022. DOI: 10.1002/app.52942.

[112] A. N. Singh, R. D. Thakre, J. C. More, P. K. Sharma, and Y. K. Agrawal, "Block Copolymer Nanostructures and Their Applications: A Review", *Polymer-Plastics Technology and Engineering*, vol. 54(10), pp. 1077–1095, 2015. DOI: 10.1080/03602559.2014.986811.

[113] H. Feng, X. Lu, W. Wang, N.-G. Kang, and J. W. Mays, "Block Copolymers: Synthesis, Self-Assembly, and Applications", *Polymers*, vol. 9(10), 2017. DOI: 10.3390/polym9100494.

[114] H.-C. Kim, S.-M. Park, and W. D. Hinsberg, "Block Copolymer Based Nanostructures: Materials, Processes, and Applications to Electronics", *Chemical Reviews*, vol. 110(1), pp. 146–177, 2010. DOI: 10.1021/cr900159v.

[115] A. Nunns, J. Gwyther, and I. Manners, "Inorganic block copolymer lithography", *Polymer*, vol. 54(4), pp. 1269–1284, 2013. DOI: 10.1016/j.polymer.2012.11.057.

[116] S. Koizumij, H. Hasegawa, and T. Hashimoto, "Ordered Structure in Blends of Block Copolymers. 3. Self-Assembly in Blends of Sphere- or Cylinder-Forming Copolymers", *Macromolecules*, vol. 27(15), pp. 4371–4381, 2001. DOI: 10.1021/ma00093a044.

[117] T. Hashimoto, K. Yamasaki, S. Koizumi, and H. Hasegawa, "Ordered structure in blends of block copolymers. 1. Miscibility criterion for lamellar block copolymers", *Macromolecules*, vol. 26(11), pp. 2895–2904, 2001. DOI: 10.1021/ma00063a039.

[118] J. Xie and A.-C. Shi, "Phase Behavior of Binary Blends of Diblock Copolymers: Progress and Opportunities", *Langmuir*, vol. 39(33), pp. 11 491–11 509, 2023. DOI: 10.1021/acs.langmuir.3c01175.

[119] D. Yamaguchi and T. Hashimoto, "A Phase Diagram for the Binary Blends of Nearly Symmetric Diblock Copolymers. 1. Parameter Space of Molecular Weight Ratio and Blend Composition", *Macromolecules*, vol. 34(18), pp. 6495–6505, 2001. DOI: 10.1021/ma0021489.

[120] X. Chevalier et al., "Blending approaches to enhance structural order in block-copolymer's self-assemblies", *Advances in Patterning Materials and Processes XXXII*, 2015. DOI: 10.1117/12.2085821.

[121] H. Ahn et al., "Microdomain expansion and transition behavior of PS-b-PMMA/PS homopolymers by SAXS analysis", *Advances in Patterning Materials and Processes XXXII*, vol. 53(22), pp. 5163–5169, 2012. DOI: 10.1016/j.polymer.2012.08.055.

[122] X. Chevalier et al., "Improvements of self-assembly properties via homopolymer addition or block-copolymer blends", *Alternative Lithographic Technologies VI*, 2014. DOI: 10.1117/12.2046329.

[123] J. M. Sojo-Gordillo et al., "Tuning the Thermoelectric Properties of Boron-Doped Silicon Nanowires Integrated into a Micro-Harvester", *Advanced Materials Technologies*, vol. 7(10), 2022. DOI: 10.1002/admt.202101715.

[124] J. M. S. Gordillo, "Semiconductor nanostructures for thermal and thermoelectric applications", Ph.D. dissertation, Physics Department, Universitat Autonoma de Barcelona, 2022.

[125] G. G. Díez et al., "Enhanced thermoelectric figure of merit of individual Si nanowires with ultralow contact resistances", *Nano Energy*, vol. 67, 2020. DOI: 10.1016/j.nanoen.2019.104191.

[126] A. Nunns, J. Gwyther, and I. Manners, "Inorganic block copolymer lithography", *Polymer*, vol. 54(4), pp. 1269–1284, 2013. DOI: 10.1016/j.polymer.2012.11.057.

[127] C. J. Hawker and T. P. Russell, "Block Copolymer Lithography: Merging "Bottom-Up" with "Top-Down" Processes", *MRS Bulletin*, vol. 30(12), pp. 952–966, 2005. DOI: 10.1557/mrs2005.249.

[128] K. H. Kim, Y. Huh, I. Song, D. Y. Ryu, J. G. Son, and J. Bang, "Recent advances in block copolymer self-assembly: From the lowest to the highest", *Journal of Polymer Science*, vol. 62(4), 2024. DOI: 10.1002/pol.20230491.

[129] P. Mansky, Y. Liu, E. Huang, T. P. Russell, and C. Hawker, "Controlling Polymer-Surface Interactions with Random Copolymer Brushes", *Science*, vol. 275(5305), pp. 1458–1460, 1997. DOI: 10.1126/science.275.5305.1458.

[130] Y. Zhao, E. Sivaniah, and T. Hashimoto, "AXS Analysis of the OrderDisorder Transition and the Interaction Parameter of Polystyrene-block-poly(methyl methacrylate)", *Macromolecules*, vol. 41(24), pp. 9948–9951, 2008. DOI: 10.1021/ma8013004.

[131] R. P. H. Jr and P. A. Seeger, "Temperature dependence of the interaction parameter of polystyrene and poly(methyl methacrylate)", *Science*, vol. 23(3), pp. 890–893, 1990. DOI: 10.1021/ma00205a033.

[132] T. Thurn-Albrecht et al., "Nanoscopic Templates from Oriented Block Copolymer Films", *Advanced Materials*, vol. 12, pp. 787–791, 2000. DOI: 10.1002/(SICI)1521-4095(200006)12:11<787::AID-ADMA787>3.0.CO;2-1.

[133] U. Jeong, D. Ryu, J. Kim, D. Kim, T. Russell, and C. Hawker, "Volume Contractions Induced by Crosslinking: A Novel Route to Nanoporous Polymer Films", *Advanced Materials*, vol. 15(15), pp. 1247–1250, 2003. DOI: 10.1002/adma.200304401.

[134] C.-C. Liu, P. F. Nealey, Y.-H. Ting, and A. E. Wendt, "Pattern transfer using poly(styrene-block-methyl methacrylate) copolymer films and reactive ion etching", *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures*, vol. 25(6), 2007. DOI: 10.1116/1.2801884.

[135] Y.-H. Ting et al., "Plasma etch removal of poly(methyl methacrylate) in block copolymer lithography", *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures*, vol. 25(6), 2008. DOI: 10.1116/1.2966433.

[136] R. A. Farrell, N. Petkov, M. T. Shaw, V. Djara, J. D. Holmes, and M. A. Morris, "Monitoring PMMA Elimination by Reactive Ion Etching from a Lamellar PS-b-PMMA Thin Film byex SituTEM Methods", *Advanced Materials*, vol. 43(20), pp. 8651–8655, 2010. DOI: 10.1021/ma101827u.

[137] A. Gharbi et al., "PMMA removal options by wet development in PS-b-PMMA block copolymer for nanolithographic mask fabrication", *Journal of Vacuum Science Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena*, vol. 33(5), 2015. DOI: 10.1116/1.4929548.

[138] R. K. Marcus and J. A. C. Broekaert, *Glow Discharge Plasmas in Analytical Spectroscopy*. Wiley, 2002. DOI: 10.1002/0470857854.

[139] L. B. Valdes, "Resistivity Measurements on Germanium for Transistors", *Proceedings of the IRE*, vol. 42(2), pp. 420–427, 1954. DOI: 10.1109/jrproc.1954.274680.

[140] D. Maillet, S. André, J. C. Batsale, A. Degiovanni, and C. Moyne, *Thermal Quadrupoles: Solving the Heat Equation through Integral Transforms*. Wiley, 2000, ISBN: 978-0-471-98320-0.

[141] P. Y. Huang et al., "A three-probe method for accurate nanoscale thermal transport measurements", *Applied Physics Letters*, vol. 124(18), 2024. DOI: 10.1063/5.0201873.

[142] J. Kim et al., "Seebeck coefficient characterization of highly doped n- and p-type silicon nanowires for thermoelectric device applications fabricated with top-down approach", *Journal of Nanoscience and Nanotechnology*, vol. 13(9), pp. 6416–6419, 2013. DOI: 10.1166/jnn.2013.7612.

[143] J. Sadhu et al., "Quenched Phonon Drag in Silicon Nanowires Reveals Significant Effect in the Bulk at Room Temperature", *Nano Letters*, vol. 15(5), pp. 3091–3096, 2015. DOI: 10.1021/acs.nanolett.5b00267.

[144] Y. Hyun, Y. Park, W. Choi, J. Kim, T. Zyung, and M. Jang, "Evaluation of Seebeck coefficients in n- and p-type silicon nanowires fabricated by complementary metal–oxide–semiconductor technology", *Nanotechnology*, vol. 23(40), p. 405 707, 2012. DOI: 10.1088/0957-4484/23/40/405707.

[145] E. Krali and Z. A. K. Durrani, "Seebeck coefficient in silicon nanowire arrays", *Applied Physics Letters*, vol. 102(14), 2013. DOI: 10.1063/1.4800778.

[146] G. Nellis and S. Klein, *Heat transfer*. Cambridge University Press, 2009. DOI: 10.1017/CBO9780511841606.

[147] Z. M. Zhang, *Nano/Microscale Heat Transfer*. Springer International Publishing, 2020. DOI: 10.1007/978-3-030-45039-7.

[148] T. Zhan et al., "Miniaturized planar Si-nanowire micro-thermoelectric generator using exuded thermal field for power generation", *Science and Technology of Advanced Materials*, vol. 19(1), pp. 443–453, 2018. DOI: 10.1080/14686996.2018.1460177.

[149] M. Tomita et al., "Modeling, Simulation, Fabrication, and Characterization of a 10-W/cm^2 Class Si-Nanowire Thermoelectric Generator for IoT Applications", *IEEE Transactions on Electron Devices*, vol. 1(9), 2018. DOI: 10.1109/ted.2018.2867845.

[150] D. B. Williams and C. B. Carter, *Transmission Electron Microscopy*. Springer, 2009. DOI: 10.1007/978-0-387-76501-3.

[151] A. E. Pap, K. Kordás, T. F. George, and S. Leppavuori, "Thermal Oxidation of Porous Silicon: Study on Reaction Kinetics", *The Journal of Physical Chemistry B*, vol. 108(34), pp. 12 744–12 747, 2004. DOI: 10.1021/jp049323y.

[152] B. E. Deal and A. S. Grove, "General Relationship for the Thermal Oxidation of Silicon", *Journal of Applied Physics*, vol. 36, 1965. DOI: 10.1063/1.1713945.

[153] S. Bose, T. Anand, and M. L. Johnston, "Integrated Cold Start of a Boost Converter at 57 mV Using Cross-Coupled Complementary Charge Pumps and Ultra-Low-Voltage Ring Oscillator", *IEEE Journal of Solid-State Circuits*, vol. 54(10), pp. 2867–2878, 2019. DOI: 10.1109/JSSC.2019.2930911.

[154] Y. K. Ramadass and A. P. Chandrakasan, "A Battery-Less Thermoelectric Energy Harvesting Interface Circuit With 35 mV Startup Voltage", *IEEE Journal of Solid-State Circuits*, vol. 46(1), pp. 333–341, 2011. DOI: 10.1109/JSSC.2010.2074090.

[155] B.-M. Lim, J.-I. Seo, and S.-G. Lee, "A Colpitts Oscillator-Based Self-Starting Boost Converter for Thermoelectric Energy Harvesting With 40-mV Startup Voltage and 75 Maximum Efficiency", *IEEE Journal of Solid-State Circuits*, vol. 53(11), pp. 3293–3302, 2018. DOI: 10.1109/JSSC.2018.2863951.

[156] C. E. Porter and F. D. Blum, "Thermal Characterization of PMMA Thin Films Using Modulated Differential Scanning Calorimetry", *Macromolecules*, vol. 33(19), pp. 7016–7020, 2000. DOI: 10.1021/ma0003021.

[157] B. Zhang, R. Yan, and N. Zhao, "Dynamics and glass transition temperature of polystyrene films supported on hydroxyl terminated substrates", *AIP Advances*, vol. 10, 2020. DOI: 10.1063/1.5145220.

[158] J. Danglad-Flores, S. Eickelmann, and H. Riegler, "Deposition of polymer films by spin casting: A quantitative analysis", *Chemical Engineering Science*, vol. 179, pp. 257–264, 2018. DOI: 10.1016/j.ces.2018.01.012.

[159] D. Meyerhofer, "Characteristics of resist films produced by spinning", *Journal of Applied Physics*, vol. 49, 1978. DOI: 10.1063/1.325357.

[160] A. Andreozzi, E. Poliani, G. Seguini, and M. Perego, "The effect of random copolymer on the characteristic dimensions of cylinder-forming PS-b-PMMA thin films", *Nanotechnology*, vol. 22(18), 2011. DOI: 10.1088/0957-4484/22/18/185304.

[161] J. F. Verwey, R. P. Kramer, and B. J. de Maagt, "Mean free path of hot electrons at the surface of boron-doped silicon", *Journal of Applied Physics*, vol. 46(6), pp. 2612–2619, 1975. DOI: 10.1063/1.321938.

[162] C.-C. Liu, P. F. Nealey, Y.-H. Ting, and A. E. Wendt, "Pattern transfer using poly(styrene-block-methyl methacrylate) copolymer films and reactive ion etching", *Journal of Vacuum Science Technology B*, vol. 25, pp. 1963–1968, 2007. DOI: 10.1116/1.2801884.

[163] R. A. Farrell, N. Petkov, M. T. Shaw, V. Djara, J. D. Holmes, and M. A. Morris, "Monitoring PMMA Elimination by Reactive Ion Etching from a Lamellar PS-b-PMMA Thin Film by ex Situ TEM Methods", *Macromolecules*, vol. 43(20), pp. 8651–8655, 2010. DOI: 10.1021/ma101827u.

[164] H. Yamamoto, T. Imamura, M. Omura, I. Sakai, and H. Hayashi, "Selective etch of poly(methyl methacrylate) in block copolymer based on control of ion energy and design of gas chemistry for directed self assembly lithography", *Japanese Journal of Applied Physics*, vol. 53, 2010. DOI: 10.7567/JJAP.53.03DD03.

[165] M. Satake, T. Iwase, M. Kurihara, N. Negishi, Y. Tada, and H. Yoshida, "Characteristics of selective PMMA etching for forming a PS mask", *Proceedings of Advanced Etch Technology for Nanopatterning II*, vol. 8685, 2013. DOI: 10.1117/12.2011071.

[166] B. T. Chan et al., "28 nm pitch of line/space pattern transfer into silicon substrates with chemo-epitaxy Directed Self-Assembly (DSA) process flow", *Macromolecules*, vol. 123, pp. 180–186, 2014. DOI: 10.1016/j.mee.2014.07.028.

[167] M. Satake, T. Iwasea, M. Kuriharaa, N. Negishia, Y. Tadab, and H. Yoshida, "Characteristics of selective PMMA etching for forming a PS mask", *Advanced Etch Technology for Nanopatterning II*, 2013. DOI: 10.1117/12.2011071.

[168] H. Gokan, S. Esho, and Y. Ohnishi, "Dry Etch Resistance of Organic Materials", *Journal of The Electrochemical Society*, vol. 130(1), 1983. DOI: 10.1149/1.2119642.

[169] H. Kawata, H. Fukuda, T. Matsunaga, M. Yasuda, and K. Murata, "Enhancement of Dry-Etching Durabilities by Energy or Etchant Quenching", *Japanese Journal of Applied Physics*, vol. 38(Part 1, No. 7B), pp. 4483–4487, 1999. DOI: 10.1143/jjap.38.4483.

[170] C. Hedlund, H.-O. Blom, and S. Berg, "Microloading effect in reactive ion etching", *Journal of Vacuum Science Technology A*, vol. 12(4), pp. 1962–1965, 1994. DOI: 10.1116/1.578990.

[171] J. O. Choi, J. A. Moorea, J. C. Corelli, J. P. Silverman, and H. Bakhru, "Degradation of poly(methylmethacrylate) by deep ultraviolet, x-ray, electron beam, and proton beam irradiations", *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures*, vol. 6(6), 1988. DOI: 10.1116/1.584071.

[172] T. Thurn-Albrecht et al., "Nanoscopic Templates from Oriented Block Copolymer Films", *Advanced Materials*, vol. 12(11), pp. 787–791, 2000. DOI: 0.1002/(sici)1521-4095(200006)12:11<787::aid-adma787>3.0.co;2-1.

[173] J. Bürger et al., "High-Resolution Study of Changes in Morphology and Chemistry of Cylindrical PS-b-PMMA Block Copolymer Nanomasks during Mask Development", *Advanced Materials Interfaces*, vol. 9(26), pp. 787–791, 2022. DOI: 10.1002/admi.202200962.

[174] AllResist. "UV-structuring of PMMA resists". [Online]. Available: https://www.statista.com/statistics/1183457/iot-connected-devices-worldwide/.

[175] J. Bürger, V. S. Kunnathully, D. Kool, J. K. N. Lindner, and K. Brassat, "Characterisation of the PS-PMMA Interfaces in Microphase Separated Block Copolymer Thin Films by Analytical (S)TEM", *Nanomaterials*, vol. 10(1), 2020. DOI: 10.3390/nano10010141.

[176] H. Jansen, H. Gardeniersa, M. de Boer, M. Elwenspoek, and J. Fluitman, "A survey on the reactive ion etching of silicon in microtechnology", *Journal of Micromechanics and Microengineering*, vol. 6(1), pp. 14–28, 1996. DOI: 10.1088/0960-1317/6/1/002.

[177] H. Rhee, H. Kwon, C.-K. Kim, H. Kim, J. Yoo, and Y. W. Kim, "Comparison of deep silicon etching using SF6/C4F8 and SF6/C4F6 plasmas in the Bosch process", *Journal of Vacuum Science Technology B: Microelectronics and Nanometer Structures*, vol. 26(2), 2008. DOI: 10.1116/1.2884763.

[178] P. Pal, V. Swarnalatha, A. V. N. Rao, A. K. Pandey, H. Tanaka, and K. Sato, "High speed silicon wet anisotropic etching for applications in bulk micromachining: a review", *Micro and Nano Systems Letters*, vol. 9(1), 2021. DOI: 10.1186/s40486-021-00129-0.

[179] F. Laermer, S. Franssila, L. Sainiemi, and K. Kolari, "Deep reactive ion etching", *Handbook of Silicon Based MEMS Materials and Technologies*, pp. 417–446, 2020. DOI: 10.1016/b978-0-12-817786-0.00016-5.

[180] S. S. Walavalkar, A. P. Homyk, D. Henryb, and A. Scherer, "Three-dimensional etching of silicon for the fabrication of low-dimensional and suspended devices", *Nanoscale*, vol. 5(3), 2013. DOI: 10.1039/c2nr32981f.

[181] M. D. Henry, S. Walavalkar, A. Homyk, and A. Scherer, "Alumina etch masks for fabrication of high-aspect-ratio silicon micropillars and nanopillars", *Nanotechnology*, vol. 20(25), 2009. DOI: 10.1088/0957-4484/20/25/255305.

[182] M. D. Henry, "ICP Etching of Silicon for Micro and Nanoscale Devices", Ph.D. dissertation, California Institute of Technology, 2010. DOI: 10.7907/Z9MW2FBC.

[183] S. Teh and D. Chuah, "Diffusion profile of spin-on dopant in silicon substrate", *Solar Energy Materials*, vol. 19(3-5), pp. 237–247, 1989. DOI: 10.1016/0165-1633(89)90009-9.

[184] C. Barri et al., "Engineering of the spin on dopant process on silicon on insulator substrate", *Nanotechnology*, vol. 32(2), 2021. DOI: 10.1088/1361-6528/abbdda.

[185] B. D. Choudhury and S. Anand, "Rapid thermal annealing treated spin–on doped antireflective radial junction Si nanopillar solar cell", *Optics Express*, vol. 25(8), 2017. DOI: 10.1364/oe.25.00a200.

[186] P. R. Wilson, "The diffusion of boron in the Si-SiO2 system", *Solid-State Electronics*, vol. 15(9), 1972. DOI: 10.1016/0038-1101(72)90137-2.

[187] J. MacHale et al., "Exploring conductivity in ex-situ doped Si thin films as thickness approaches 5 nm", *Journal of Applied Physics*, vol. 125(22), 2019. DOI: 10.1063/1.5098307.

[188] S.-M. Lee and D. G. Cahill, "Heat transport in thin dielectric films", *Journal of Applied Physics*, vol. 81, pp. 2590–2595, 1997. DOI: 10.1063/1.363923.

[189] D. M. Knotter and T. J. J. (Denteneer, "Etching Mechanism of Silicon Nitride in HF-Based Solutions", *Journal of The Electrochemical Society*, vol. 148(3), 2001. DOI: 10.1149/1.1348262.

[190] M. H. anb J Schilm, G. Michael, J. Meinhardt, and R. Flegler, "Corrosion of silicon nitride materials in acidic and basic solutions and under hydrothermal conditions", *Journal of the European Ceramic Society*, vol. 23(4), pp. 585–594, 2013. DOI: 10.1016/s0955-2219(02)00303-5.

[191] P. Hammond, "Vapor-phase etch processes for silicon MEMS", *Handbook of Silicon Based MEMS Materials and Technologies*, 2020. DOI: 10.1016/b978-0-12-817786-0.00020-7.

[192] L. Liu, F. Lin, M. Heinrich, A. G. Aberle, and B. Hoex, "Unexpectedly High Etching Rate of Highly Doped n-Type Crystalline Silicon in Hydrofluoric Acid", *ECS Journal of Solid State Science and Technology*, vol. 2(9), pp. 380–383, 2013. DOI: 10.1149/2.026309jss.

[193] R. Hidayat et al., "Selective etching mechanism of silicon oxide against silicon by hydrogen fluoride: a density functional theory study", *Physical Chemistry Chemical Physics*, vol. 25(5), pp. 3890–3899, 2023. DOI: 10.1039/D2CP05456F.

[194] R. Chen, A. I. Hochbaum, P. Murphy, J. Moore, P. Yang, and A. Majumdar, "Thermal Conductance of Thin Silicon Nanowires", *Physical Review Letters*, vol. 101(10), 2008. DOI: 10.1103/PhysRevLett.101.105501.

[195] A. Vega-Flick et al., "Thermal transport in suspended silicon membranes measured by laser-induced transient gratings", *AIP Advances*, vol. 6(12), 2016. DOI: 10.1063/1.4968610.

[196] Q. Hao, G. Chen, and M.-S. Jeng, "Frequency-dependent Monte Carlo simulations of phonon transport in two-dimensional porous silicon with aligned pores", *Journal of Applied Physics*, vol. 106(11), 2009. DOI: 10.1063/1.3266169.

[197] I. Donmez, "Improving the performance of an all-Si based thermoelectric micro/nanogenerator", Ph.D. dissertation, Physics Department, Universitat Autonoma de Barcelona, 2018.

[198] W. Lur and L. J. Chen, "Growth kinetics of amorphous interlayer formed by interdiffusion of polycrystalline Ti thin-film and single-crystal silicon", *Applied Physics Letters*, vol. 54, pp. 1217–1219, 1989. DOI: 10.1063/1.100720.

[199] R. Butz, G. W. Rubloff, T. Y. Tan, and P. S. Ho, "Chemical and structural aspects of reaction at the Ti/Si interface", *Journal of Applied Physics*, vol. 30, 1984. DOI: 10.1103/PhysRevB.30.5421.

[200] S. Mao and J. Luo, "Titanium-based ohmic contacts in advanced CMOS technology", *Journal of Physics D: Applied Physics*, vol. 52, 2019. DOI: 10.1088/1361-6463/ab3dc9.

[201] S. Zaima, T. Yamauchi, Y. Koide, and Y. Yasuda, "Further experiments on the minimum in the resistance-temperature curve of gold", *Applied Surface Science*, vol. 70-71(2), pp. 624–628, 1993. DOI: 10.1016/0169-4332(93)90591-X.

[202] S.-J. Jeong, J. Y. Kim, B. H. Kim, H.-S. Moon, and S. O. Kim, "Directed self-assembly of block copolymers for next generation nanolithography", *Materials Today*, vol. 16(12), pp. 468–476, 2013. DOI: 10.1016/j.mattod.2013.11.002.

[203] Z.-G. Wang, "Response and instabilities of the lamellar phase of diblock copolymers under uniaxial stress", *The Journal of Chemical Physics*, vol. 100(3), pp. 2298–2309, 1994. DOI: 10.1063/1.466528.

[204] L. Evangelio, M. Fernández-Regúlez, X. Borrisé, M. Lorenzoni, J. Fraxedas, and F. Pérez-Murano, "Creation of guiding patterns for directed self-assembly of block copolymers by resistless direct e-beam exposure", *Journal of Micro/Nanolithography, MEMS, and MOEMS*, vol. 14(3), 2015. DOI: 10.1117/1.jmm.14.3.033511.

[205] L. Evangelio, M. Fernández-Regúlez, J. Fraxedas, M. Müller, and F. Pérez-Murano, "Role of Penetrability into a Brush-Coated Surface in Directed Self-Assembly of Block Copolymers", *ACS Applied Materials Interfaces*, vol. 11(3), pp. 3571–3581, 2019. DOI: 10.1021/acsami.8b19062.