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Grau d'Enginyeria Electrònica de Telecomunicació

Study of dependencies on the operating conditions of RTN signals in nanoelectronic CMOS devices

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Agraïments

M’agradaria expressar el meu agraïment sincer a totes les persones que han contribuit d’alguna manera a la realització d'aquest treball final. En primer lloc, vull agrair a la meva tutora, Montserrat Nafría Maqueda, per la seva indestructible paciència, dedicació i apassionat compromís amb el camp de l’enginyeria electrònica. L'orientació experta i la motivació constant van ser fonamentals per assolir els objectius d'aquest projecte.

Agraeixo també a la meva família, en especial als meus pares i germans/es pel suport incondicional i per ser la meva font constant d'inspiració. La seva confiança en mi i el seu constant alè van ser motors que van impulsar la meva perseverança. No tinc prou paraules per expressar la meva gratitud cap a vosaltres. El seu suport incondicional i la seva comprensió han estat un far lluminós en els moments desafiadors d'aquest viatge acadèmic

Als meus amics, els agraeixo per la seva amistat, comprensió i confiança. Les seves paraules d'alè i moments compartits van afegir un valor incalculable a la meva experiència tant durant aquest treball com durant la meva estada a la Universitat Autònoma.

Aquest èxit no hagués estat possible sense el suport i l'afecte de totes aquestes persones. A cadascun/a de vosaltres, us estic profundament agraïda.

Presentation

Over the past years, Complementary Metal Oxide Silicon (CMOS) technology has played an increasingly important role in the world's integrated circuit industry, and for the present and foreseeable future, CMOS will remain the dominant technology used to fabricate integrated circuits (ICs). The key factors contributing to its success are its low power consumption at extremely high working speeds and manufacturability. The intrinsic speed of MOS transistors has increased three main orders of magnitude during the last thirty years due to the scaling down of integrated circuits feature sizes in accordance with Moore's law, which stipulates that the number of transistors on a single chip doubles every 18 months. One of the key benefits of CMOS technology is that it keeps the fundamental characteristics of low power consumption, high noise tolerance, wide operating voltage, and wide operating temperature range. Furthermore, it continuously and quickly raises the intrinsic speed and integration degree. Consequently, one of the main technologies in Very Large-Scale Integration (VLSI) is now without a doubt CMOS technology [1]

As the demand for more complex hardware circuitry and a higher number of transistors grew, MOSFET's downsizing emerged as the prominent solution. In 1974, Dennard et al. proposed that scaling a product's dimensions and voltages by a factor of "s" requires a simultaneous scaling of doping concentrations by a factor of (1/s) to maintain electric fields inside the device [2]. The ability to scale MOSFETs down in size allowed for the creation of increasingly compact and powerful integrated circuits. As transistors shrank, more could be packed onto a single chip, leading to the evolution of semiconductor devices to higher processing speeds, reduced power consumption, and overall improved performance in electronic systems. In this context, the CMOS semiconductor industry pioneered advancements to progressively shrink the minimum gate length from micrometres when Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) were first described, to today's gate lengths of 5-nm, reaching nanoscale dimensions [3].

Furthermore, the scaling of the transistor's gate thickness has led to a notable increase in gate leakage current among other short channel effects. To enhance the performance of fabricated devices, the industry has introduced new and more complex gate dielectric stack materials like Silicon oxynitride (SiON), High-K Metal gate insulators (HKMG), and novel device geometries such as FinFETs, FDSOI, or MuGFETs in ultra-scaled technology nodes. These innovations aim to continue the scaling trend and provide better control over short channel effects [4].

While scaling transistor size has brought about numerous benefits, it has also introduced some drawbacks and challenges regarding its reliability. The discrete nature of matter and charge leads to heightened variations in the intrinsic performance of transistors, posing a critical threat to the fundamental reliability of fabricated devices and circuits. Variations in transistor parameters, such as threshold voltage and mobility, and their degradation during circuit operation, have become growing concerns in nanometre integrated circuit design. Several degradation mechanisms, which depend on operating conditions and time, can cause a significant change of the transistor parameters. Variability sources are categorized into Time Zero Variability (process variability occurring during fabrication) and Time Dependent Variability (emerging during circuit operation). Circuit design techniques addressing these variabilities in advanced technology nodes rely on accurate MOSFET compact models based on statistical characterization of individual MOSFET devices.

Among the aging and transient effects that are included in the category of Time Dependent Variability are Bias Temperature Instability (BTI) and Random Telegraph Noise (RTN). Both phenomena have a common physical origin, i.e. trapping/detrapping of charges in/from MOSFET defects, thus modelling them together will increase the accuracy of assessing circuit reliability. However, the stochastic nature of defects behaviour requires that many devices at the same conditions must be measured to perform complete statistical studies.

On top of that, since both RTN and BTI are highly dependent on the biasing conditions of the devices, a thorough characterization of both phenomena necessitates the measurement of numerous devices under various biasing conditions, requiring sophisticated characterization techniques for extensive device characterization within reasonable measurement times. Using specially designed array-based ICs, such as the ENDURANCE chip, and measurement methodologies, to parallelize the measurements and shorten the effective time needed for statistical characterization in several devices, is the most comprehensive solution for this issue.

Therefore, in order to comprehend its impacts and move one step forward to the development of more reliable electronic circuits, the following work examines the dependencies of these degradation mechanisms on a different number of biasing situations through a statistical analysis of data samples and measurements.

Contents

Objectives

Within the current landscape of CMOS electronic device research, the understanding and mitigation of reliability issues play a pivotal role in enhancing their long-term reliability and performance. This research project embarks on a comprehensive investigation of Time-Dependent Variability (TDV) in CMOS devices, with a specific focus on Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI). The principal objectives of this study encompass the exploration of TDV phenomena, the development of a MATLAB program for automated compact model parameter extraction, and the subsequent statistical analysis and characterization of these degradation mechanisms.

The primary aim of this work is to examine TDV dependencies on biasing conditions, notably the RTN and BTI phenomena, which have emerged as critical challenges in modern semiconductor technology. By studying these degradation mechanisms, we aspire to unravel their main principles and gain insights into their implications for nanometre CMOS technologies. To achieve this, a statistical analysis of an extensive set of variability measurements over hundreds of transistors under different operating conditions will be conducted.

The fundamental part of this research involves the creation of a MATLAB program capable of automating the analysis and extraction of relevant information for characterizing electronic devices. This program will facilitate the extraction of accurate parameters of the most significant stochastic sources of variability from a statistical point of view, such as the average number of defects per device. The automation of this process not only will accelerate the analysis but will also ensure consistency and accuracy in data extraction, laying the groundwork for a robust statistical assessment.

Finally, once the data is obtained through the automated program, the subsequent phase of this work will concentrate on the detailed analysis of the extracted information. Advanced statistical techniques will be applied to assess the dependence of degradation mechanisms on various operating conditions. Factors such as applied gate voltage (V_G) and time, will be analysed to understand their impact on TDV mechanisms.

The extraction of model parameters, combined with detailed statistical analysis, will enable the identification of trends, patterns, and correlations among these variables, providing valuable insights into the impact of external stimuli on these degradation mechanisms.

In essence, this work not only aims to study the impact of Time Dependent Variability phenomena through the analysis of laboratory data samples but also strives to advance the automation of CMOS device characterization and statistical data extraction. By combining these elements, we aim to unravel the complexities inherent in these electronic components. The outcomes of this study have the potential to enlighten future advancements in semiconductor technology, fostering the development of more robust and reliable electronic devices by foreseeing the negative impacts of these degradation mechanisms on circuit functionality and mitigate them in the design and operational phases.

CHAPTER I

1. The MOSFET at the base of CMOS technology

The need for smaller, faster, more cost-effective, and energy-efficient devices in the 1930s led to the rise of Field Effect Transistors (FET) as an alternative to vacuum tube technology. Initially it became difficult to explain their structure, as the surface states availability at the interface of the semiconductor and oxide marked the prevention of the electric field from absorbing the semiconducting element. However, researchers Singha and Attala successfully overcame this issue by introducing the insulated gate field effect transistors which were made of three layers, namely Metal (M), Oxide (O) and Semiconductor (S) known as Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Since then, MOSFETs have proven to be one of the best switching devices, consisting of the following terminals: Gate, Drain, Source and Substrate [5].

A MOS transistor, usually named a majority-carrier device because the current in a conducting channel between the source and drain is modulated by a voltage applied to the gate (V_G), can be classified into two types, namely pMOS (Fig.1) and nMOS (Fig. 2), which widely hold a major role in the field of integrated circuit design [6]. In an n-type MOS transistor (i.e., nMOS), most carriers are electrons (Fig. 2). When a positive voltage is applied on the gate with respect to the substrate, the number of electrons in the channel (the region immediately under the gate) is enhanced and consequently the conductivity of the channel increases. The operation of a p-type transistor (i.e., pMOS) is analogous to the MOS transistor (Fig. 1), with the exception that most carriers are holes, and the voltages are negative with respect to the substrate [7].

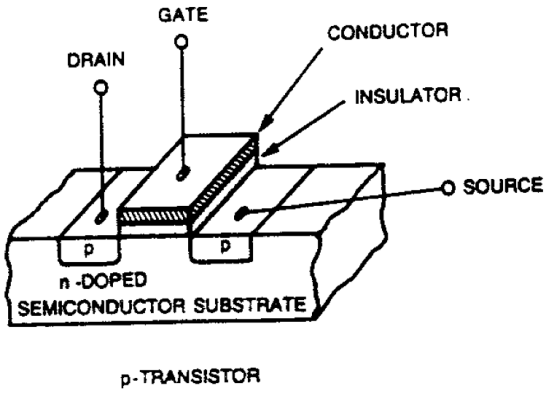

Fig. 1 pMOS transistor physical structure [6].

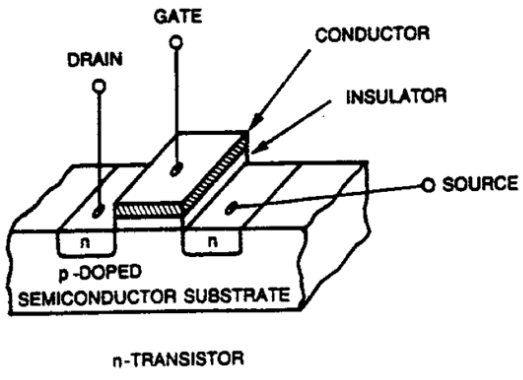

Fig. 2 nMOS transistor physical structure [6].

One of the problems encountered with pMOS and nMOS MOSFETs was high static power consumption. However, in the early 1970s, Frank Wanlass presented a novel design that incorporated both a p-type and an n-type MOSFET in the same logic, resulting in excellent noise immunity and minimal static power consumption. That is how the Complementary Metal-Oxide-Semiconductor (CMOS) technology arrived to mark the pace of "Very Large-Scaled Integration" (VLSI) [5].

1.1. I/V Characteristics of MOS transistors

The first parameter of interest that characterizes the switching behaviour of a CMOS device is the threshold voltage V_T. It is defined as the required value of the gate-to-source voltage (V_{GS}) necessary to cause surface inversion (to create the conducting channel)[6].

For gate voltages less than a threshold value denoted by V_T, the channel is cut-off, thus causing a very low drain-to-source current, I_D, which is not strictly zero for $V_{GS} < V_T$ due to the diffusion current, and which decreases exponentially with $V_{GS}-V_T$. In general, the threshold voltage is a function that depends on various device and process parameters, such as the work function difference between the gate and the substrate, the intrinsic substrate (surface) Fermi potential, the depletion region charge concentration, the interface charge concentration, the gate oxide thickness and oxide (dielectric) permittivity, as well as the concentration of the channel implantation that is used to adjust the threshold voltage level. In addition, the absolute value of the threshold voltage decreases with an increase in temperature [7].

When in a nMOS the gate-to-source voltage exceeds the threshold voltage, an n-type conducting channel is formed between the source and the drain, which can carry the drain (channel) current. If a small, positive voltage is applied to the drain, a current proportional to this voltage will start to flow from the drain to the source through the conducting channel. The effective resistivity of the continuous inversion layer between the source and the drain depends on the gate voltage. This operating mode is called the linear mode, where the channel region acts as a voltage-controlled resistor. During this operating mode, the electron velocity in the channel is usually much lower than the drift velocity limit.
As the applied drain voltage is increased, the inversion layer charge and the channel depth at the drain end start to decrease. Eventually, when the drain voltage reaches a limit value called the saturation voltage (V_{Dsat}), the inversion charge at the drain is reduced to zero (ideally), and the velocity of electrons reaches very high values. This event is named as the "pinch-off" of the channel. Beyond the pinch-off point, i.e., for drain voltage values larger than the saturation voltage, electrons travel in a very shallow

pinched-off channel with a very high velocity, which is called the “saturation velocity.” This operating regime is known as the saturation mode [7].

In a pMOS transistor, the fundamental mechanisms of surface inversion and channel conduction are the same as in nMOS transistors, although the majority carriers consist of holes, not electrons. Thus, the gate-to-source voltage applied to the gate electrode to achieve surface inversion must be negative. Also, it should be considered that the hole mobility is considerably smaller than the electron mobility at room temperature, which leads to a smaller effective channel conductance for the pMOS transistor with the same channel dimensions. Nevertheless, the complementary nature of nMOS / pMOS biasing and operating conditions offers very useful circuit implementation possibilities, which underlines the importance and the wide-spread use of Complementary MOS (CMOS) circuits in a very large range of applications [7].

An interesting representation of MOSFET’s performance is the I_D-V_G characteristic (Fig. 3) which provides valuable information on the variation of the source-to-drain current (l_{DS}) with respect to the gate-to-source voltage (V_{GS}), and defines the gate voltage at which the transistor begins to conduct, i.e., the threshold voltage V_T.

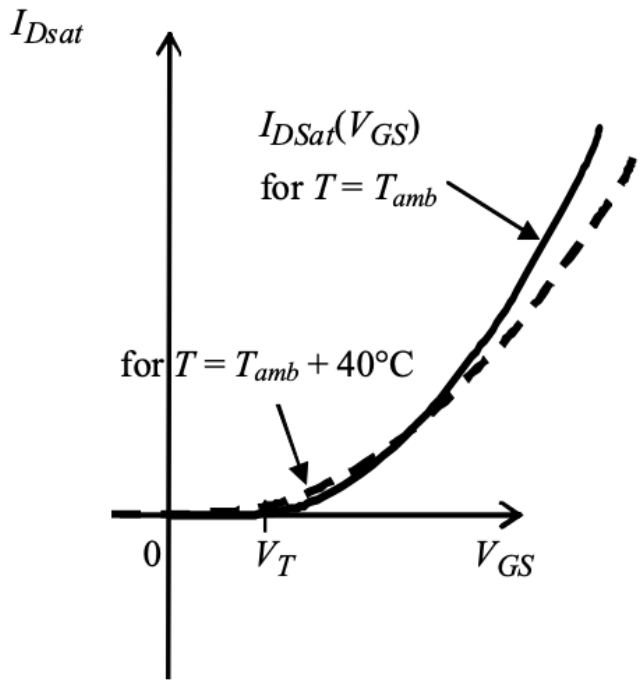

Fig. 3. I_D/V_{GS} characteristic of a typical nMOS transistor [8].

The output characteristic curves of an nMOS transistor can be seen in Figure 4 covering the three phases, the onset of the pinch-off, the linear (or resistive) region, and the saturation region, where the border between the resistive region and the saturation region corresponds to $V_{DS} = (V_{GS} - V_T)$ plotted as a dashed line.

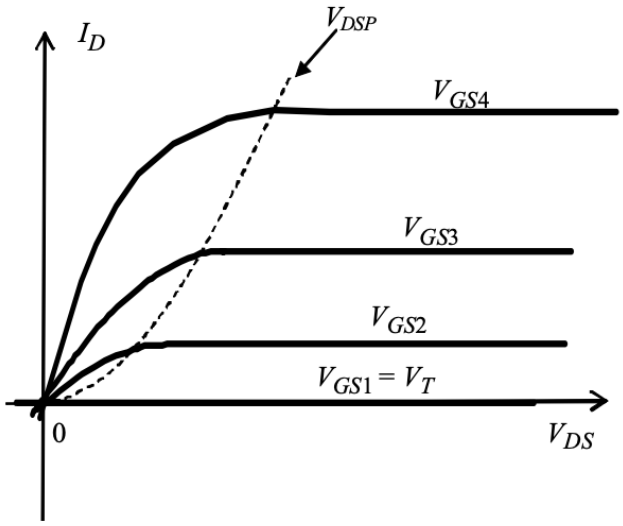

Fig. 4. I_D/V_{DS} characteristic of a typical nMOS transistor [8].

For pMOS transistors, the characteristic curves have a similar shape. But since in pMOS transistors the gate-source voltage must be negative to induce p-type inversion layer, and consequently, the polarities of the drain-source voltage and the drain current are negative, all voltages and currents on the characteristics must be marked as negative [7].

1.2. Scaling effects on MOS transistors

The most common description of the evolution of CMOS technology is known as Moore's law. According to this law proposed by Gordon Moore in 1965, every two years the transistor quantity contained in a dense integrated circuit had to be doubled [9]. By scaling down technologies, a larger quantity of transistors could be produced from a single silicon wafer. This not only resulted in a more cost-effective and compact circuit, but it also enhanced performance and speed. Subsequently, in 1974, Robert Dennard and his colleagues outlined a scaling approach for metal-oxide-semiconductor field-effect transistors (MOSFETs) that would consistently enhance transistor area, performance, and power reduction. This methodology consisted of scaling the transistor's gate length, gate width, gate oxide thickness, and supply voltage all by the same scale factor, and increasing channel doping by the inverse of the same scale factor [10]. Since then, transistors resulted in a decrease of their area, higher drive current (higher performance), and lower parasitic capacitance (lower active power). The scaling evolution of MOS integrated circuits over the last decades is presented in Table 1.

S. No.	MOSFET Technology (Gate length)	Year of production
1	10 µm, 10000 nm (2D Technology)	1971
2	6 µm, 6000 nm	1974
3	3 µm, 3000 nm	1977
4	1.5 µm, 1500 nm	1981
5	800 nm	1987
6	600 nm	1990
7	350 nm	1993
8	250 nm	1996
9	180 nm	1999
10	130 nm	2001
11	90 nm	2003
12	65 nm	2005
13	45 nm	2007
14	32 nm	2009
15	22 nm (3D Technology)	2012
16	14 nm	2014
17	10 nm	2016
18	7 nm	2018
19	5 nm	~2020
	Future trend	
20	3 nm	~2021
21	2 nm	~2024

Table 1. Scaling evolution of MOS technologies [5].

However, making a chip with many transistors is not an easy task since major issues such as short channel effects (SCE) appear when reducing the dimensions of the transistor since it causes the dependence of device characteristics, such as threshold voltage, upon channel length. SCE degrades the controllability of the gate voltage to drain current, which leads to the degradation of the subthreshold slope and the increase in drain off-current [11].

The evolution of ultra-scaled CMOS technologies, marked by the reduction in transistor dimensions, has introduced challenges associated with variability. As semiconductor components approach smaller scales, issues such as process variations and device parameter fluctuations become more pronounced. These challenges in variability can significantly impact the performance and reliability of integrated circuits, raising substantial concerns for the design and manufacturing processes. Addressing and mitigating these variability issues in ultra-scaled CMOS technologies are vital aspects to ensure the continued progress and efficiency of advanced semiconductor devices. In the realm of modern CMOS processes, one approach to classifying sources of random variability involves distinguishing between Time-Zero Variability (TZV) and Time-Dependent Variability (TDV), both of which may coexist [12].

Time-Zero Variability (TZV), typically known as spatial or process variability, is a well-known variability source that consists of a constant, either random or systematic, permanent shift of some device parameters (and, thus, a permanent deviation of the nominal circuit performance). This is due to the imperfect fabrication process and the granular nature of the used materials causing effects that worsen with technology scaling, such as random dopant fluctuations, line edge roughness, gradient effects or metal gate granularity in those technologies using metal gates. Time-Dependent Variability (TDV), on the other hand, includes transient effects, like random telegraph noise (RTN), and aging effects, like hot-carrier injection (HCI) and both types of bias temperature instability (BTI); negative BTI (NBTI) and positive BTI (PBTI) [12], [13].

As we have seen, integrated circuit performance has increased dramatically over the past few decades because of the downscaling of CMOS technology. Nonetheless, this downscaling poses major challenges with respect to the device lifetime and reliability, as with CMOS scaling, the effects of both time-dependent and time-zero variability become more severe [14].

2. Time Dependent Variability

As mentioned above, Time-Dependent Variability (TDV) has become an important concern for both analog and digital circuit designers due to its growing impact on circuit reliability. TDV consists of electrically neutral defects, that do not manifest themselves as any degradation immediately after manufacturing as TZV. Instead, these defects become apparent only when a stimulus, such as voltage, is applied. Nevertheless, it is crucial not to overlook these defects as they have the ability to capture carriers during circuit operation, weaken the formation of a channel in a MOSFET, and consequently lead to a shift in the threshold voltage (V_T) of the transistor [15].

TDV comprises both transient effects, such as Random Telegraph Noise (RTN), and aging phenomena, such as Bias Temperature Instability (BTI) or Hot-Carrier Injection (HCI) [16].
RTN, BTI and HCI have been associated to the stochastic trapping/detrapping of charge carriers in/from defects present in the oxide or silicon-oxide interface of the devices. These defects can be originated during the manufacturing process or generated during the device operation. All these phenomena cause shifts in the transistor parameters. During circuit operation, the variability effects related to the trapping/detrapping in/from oxide defects could result in circuit malfunction due to the shift of some transistor parameters, such as the threshold voltage (V_T) as mentioned. These shifts display a discrete and stochastic nature in deeply scaled CMOS technologies and originate variations in the circuit performances over time. For this reason, an accurate extraction method of the defect parameters requires a massive statistical characterization of transistors [17].

2.1. Random Telegraph Noise

Random telegraph noise (RTN) in MOSFETs recently has attracted much more attention due to its increasing amplitude with device size scaling, which can hurt circuit performance and reliability [18]. Therefore, it is becoming an important issue that concerns circuit designers, especially for advanced logic technologies with smaller headroom ($V_{DD}-V_T$) and less design margin [19].

In nanoscale MOSFETs, the stochastic trapping/detrapping behaviour of charges in/from defects in the gate dielectric and/or its interfaces causes random fluctuations between two or more drain current levels (Fig. 5) [12]. Because of its similarity to a telegraph signal this switching is called random Telegraph Signal (RTS) or Random Telegraph Noise [20]. In large devices, it is this superposition of many hundreds of RTSs events what actually generates the low-frequency (1/f) noise [21]. Therefore, the physical origin of both RTN and low-frequency 1/f noise is most likely to be the same [22].

These random fluctuations of the drain current between two or more levels are determined by the trap state (neutral or charged), when a constant voltage is applied. For instance, Figure 5 illustrates a RTN trace in the simplest scenario, a two-level signal when only one defect is present in the device. The drain current alternates between two levels: I_H (when charges are released from traps) and I_L (when charges are trapped), with a separation distance of ΔI. The times t_e and t_c represent the time durations for a charge to be emitted or trapped, respectively, and they are statistically distributed following an exponential distribution with average values of τ_e and τ_c.

To fully characterize a two-level RTN signal, three parameters are necessary: the average emission time (τ_e), average capture time (τ_c), and the magnitude of the current shift (ΔI) which can be directly obtained from the RTN trace. The physical characteristics of the defect, such as energy level and location in the oxide and along the channel, strongly influence these three parameters. Thus, depending on the position of the trap along the channel, a different ΔI_D will be introduced in the device drain current [23].

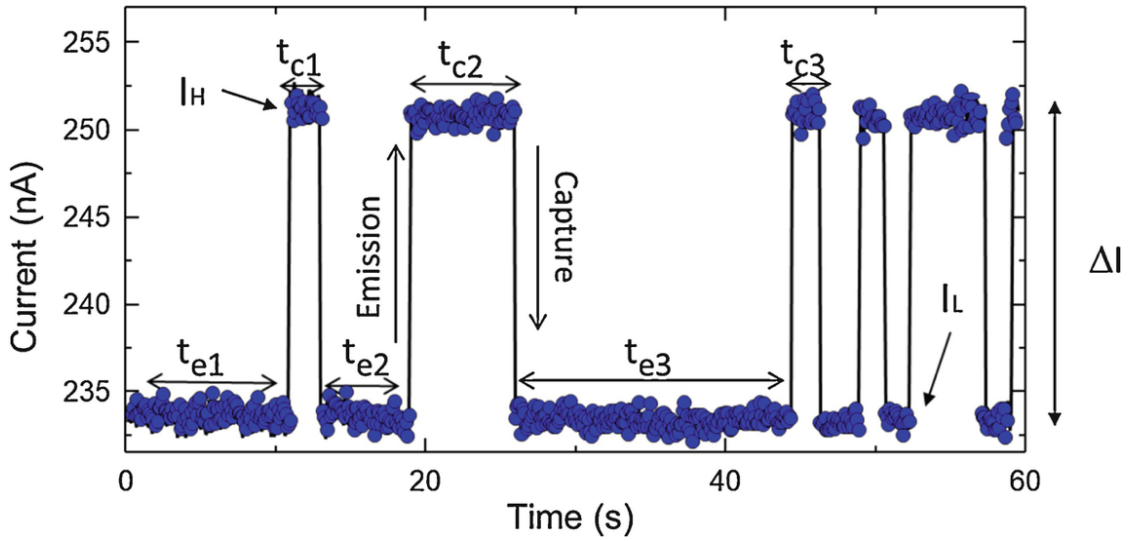

Fig. 5. Two-level RTN trace in time domain [23].

The standard procedure for the analysis of random telegraph fluctuations in time domain consists of directly finding in the time record of the trace the time instances at which the system undergoes transitions between the distinct states. This is the most crucial and delicate stage of the analysis. Having annotated the record with switching instances one can directly determine individual pulse lengths and switch amplitudes, build their histograms, and determine the statistical average values. The method mentioned above is straightforward in the case of clean RTS signals, but in the experimental reality (as we can appreciate in Fig. 5), fluctuations on the current level can be observed associated to other background noise components. This additional noise is commonly contributed by the investigated system and the measuring chain, having to deal with RTS signals that are strongly perturbed by

background noise. As a result, it can be really challenging to determine the exact moments at which the switches occur and therefore, the corresponding current/threshold voltage levels. The procedure of direct determination in that case is not an easy task and fails completely when facing signals with a small ratio of the RTS amplitude to the background noise variance [24].

These trapping occurrences cause variations in the MOSFET's threshold voltage (V_T). It is evident that the charges cause modifications to the device's potential profile (Fig. 6.a), which result in a shift in its I_D–V_G transfer characteristics, moving the transfer curve to the right (Fig. 6.b). This shift implies a current decrease for the same bias (a fixed V_G), which is equivalent to an increase of the threshold voltage (V_T). Once the charges get detrapped again, the initial characteristics will be recovered, i.e., the initial threshold voltage V_T [23].

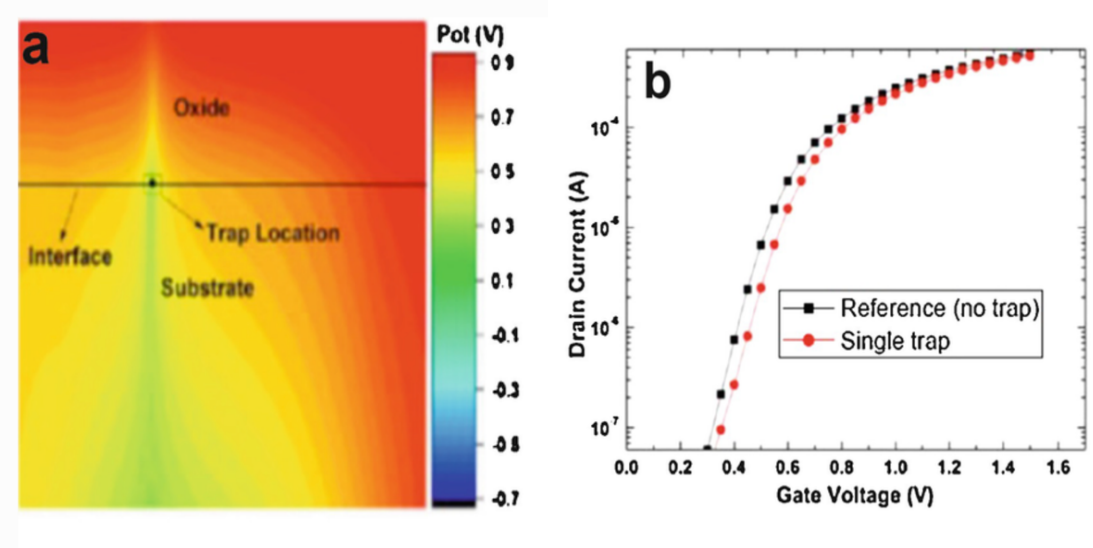

Fig. 6. (a) Potential profile (b) I_D–V_G of the device when the trap is neutral (black squares) or charged (red dots) [23].

Multiple active defects can be present in a device, situated at different locations along the interface and/or oxide depth (Fig. 7a). The current density in a device with three defects is displayed in Figure 7b. Given that these defects are placed at different points at the interface, each of these defects will lead to a different ΔV_T (or, equivalently ΔI_D) and could also be characterized by different time constants (τ_e, τ_c). In an ideal scenario where there is no noise or interaction among traps, the number of levels in a device can be determined by the number of defects present. For N defects, it is possible to distinguish 2^N levels. For instance, Figure 7c illustrates an RTN trace with four levels, which is a result of two defects in the device. However, the number of defects in a device is inversely proportional to the device area, so that in advanced nodes this number will be typically small [23].

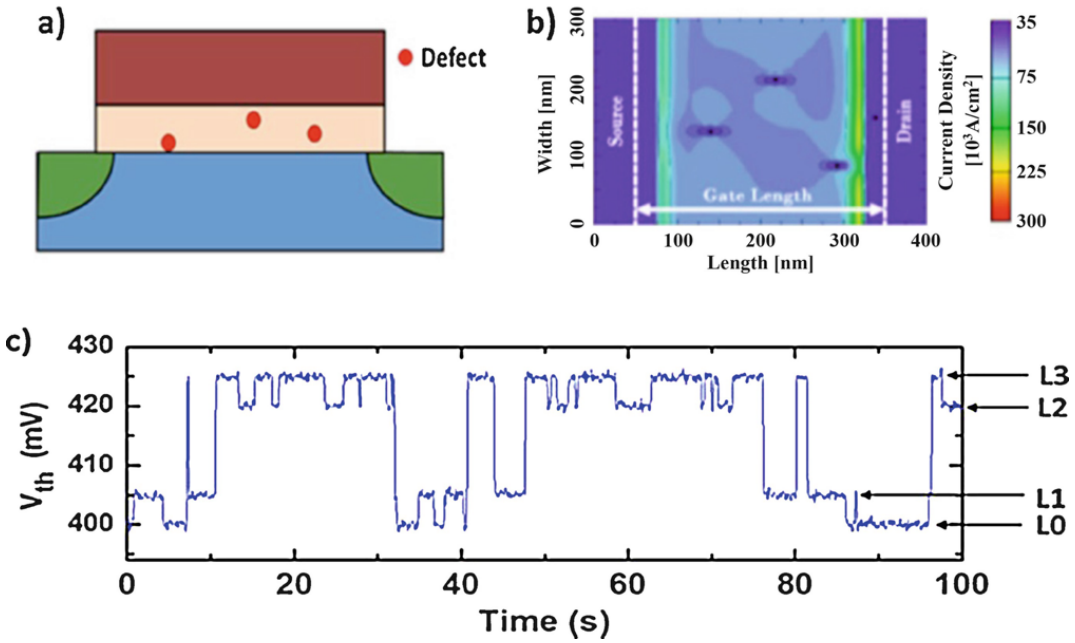

Fig. 7. (a) Schematic front view of a MOSFET with 3 defects (b) TCAD simulation of the current density in a device with three defects. (c) RTN trace of a device with two defects leading to multiple levels in the RTN (L0–3) [23].

Due to the random and transient V_T changes in the device that RTN introduces, we can affirm that it is an intrinsically stochastic process. Additionally, it must be taken to account that this behaviour changes from device to device for several reasons. First, the number of defects per device in a set of devices is statistically distributed following a Poisson distribution. Secondly, the drain current change (ΔI_D) or, equivalently, the V_T shift (ΔV_T) associated with each defect is exponentially distributed and lastly, the time constants τ_e and τ_c are widely distributed, expanding over several time decades, from μs to seconds (typical in experimental situations) [23].

From the above and given the characteristics of this mechanism, it can be concluded that it is crucial that a massive statistical characterization (with many devices and long-lasting traces) of the phenomena is carried out, and that advanced automated analysis methodologies are developed to manage the extensive amount of data that will result from this characterization. This process will be essential to understand the Time-Dependent Variability introduced by RTN and guarantee the future implementation of more reliable circuits and systems.

2.2. Bias Temperature Instability

Bias temperature instability (BTI) is one of the most critical degradation mechanisms that limits the circuit reliability in modern semiconductor devices. Negative BTI (NBTI), observed since the late 1990's, remains a critical issue in present-day Si-based p-channel MOSFETs. With the introduction of high-k gate dielectrics, Positive BTI (PBTI) emerged as a concern for n-channel MOSFETs, later on minimized by high-k material quality improvement; nevertheless, PBTI and NBTI still represent a concern for technologies beyond Silicon [25]. The degradation due to BTI is transient and, as the name suggests, is greatly influenced by bias voltages and temperature, making it very difficult to detect possible BTI-related failures during manufacturing test. Therefore, characterization and modeling of BTI is extremely important to protect a chip from BTI-related failures [26].

The most effective, earliest reported and thus most prominent ageing effect is the negative Bias Temperature Instability effect (NBTI). NBTI occurs predominantly in pMOS transistors and causes an increase in the transistor's absolute threshold voltage [27]. Specifically, during a BTI test, the absolute threshold voltage of the MOSFET increases, while the device is biased in inversion mode. The threshold voltage shift leads to a decrease in drain current in the on-state of the transistor and ultimately to a degradation of the switching speed of CMOS circuits, which does not directly lead to their failure but accumulates each time the system is under stress. For p-channel MOSFETs the term negative bias temperature instability (NBTI) is used, whereas for n-channel MOSFETs the degradation is called positive bias temperature instability (PBTI) since the corresponding gate bias conditions (V_G) are negative and positive, respectively (Fig. 8) [28].

Fig. 8. Bias configuration for pMOS and nMOS devices in CMOS circuits [28].

The assessment of BTI induced MOSFET parametric degradation is usually done by stressing the device at an accelerated aging condition, using a gate bias (V_G) that is higher ($V_G = V_{G\text{-}STR}$) than that used during normal operation. MOSFET transfer I–V characteristics are measured before and after BTI stress, and the difference between pre- and post-stress values is used to assess degradation in device parameters

[29]. Figure 9 shows the I_D-V_G characteristics measured before and after NBTI and PBTI stress respectively in (a) p-channel and (b) n-channel MOSFETs. Reduction in I_D is observed for both NBTI and PBTI stress. NBTI results in negative shift after stress, while PBTI results in positive shift of the I–V characteristics. Shift in I–V characteristics after stress is a measure of ΔV_T due to gate insulator charges; positive charges for NBTI causing negative ΔV_T, while negative charges for PBTI causing positive ΔV_T [30].

After the stress bias is removed from the FET gate, BTI degradation starts to recover immediately. ΔV_T recovery (also known as relaxation) is typical for the BTI measurement (Fig. 10a bottom). It has been the source of most of the controversy surrounding the BTI phenomenon since it complicates comparison of results if not appropriately measured and specified [25].

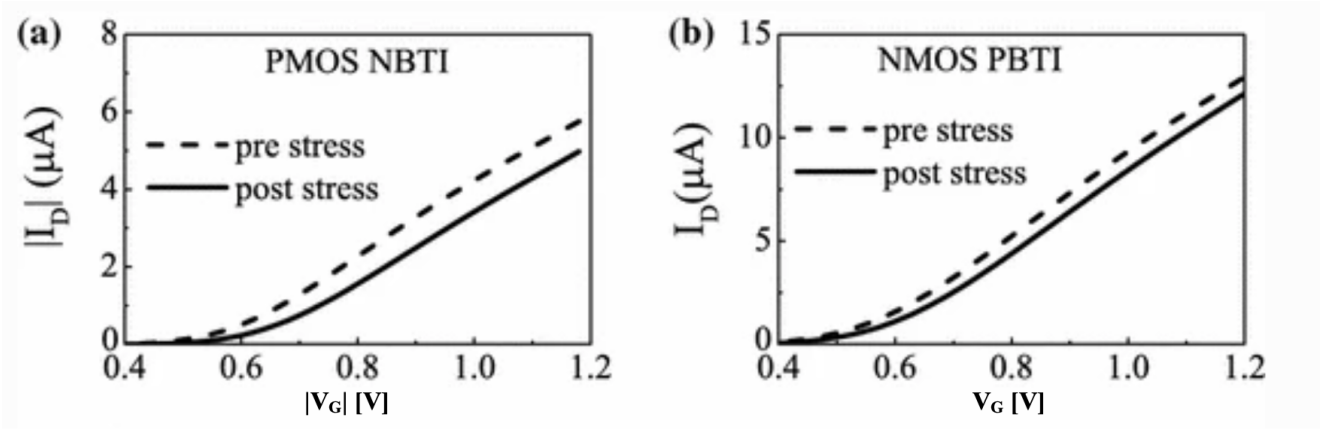

Fig. 9. I_D–V_G transfer characteristics before and after stress. Voltage and currents for pMOS are given in absolute value [30]

It has been proven that RTN and BTI are two manifestations of the same phenomenon, which is the trapping/detrapping of charges in/from defects in the device, being the main difference, the time constants of the defects involved, faster in the case of RTN. Another difference is that BTI is expected to occur at larger voltages and consists of a permanent and a recovery component [23].

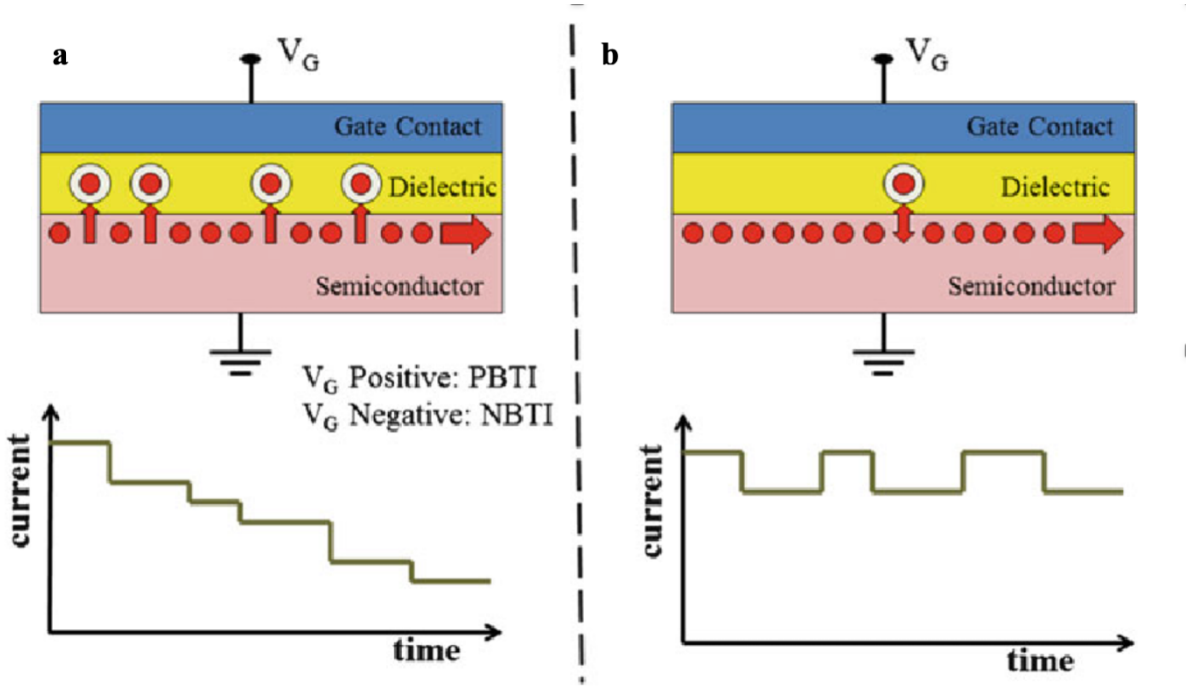

Fig. 10. (a) Traps that contribute to BTI (b) Traps that contribute to RTN
Traps are represented as white circles and carriers as red circles. Current traces during recovery are shown in the bottom figures [31].

On the one hand, traps that contribute to BTI are the ones that stay occupied after a capture event occurs, as seen in Figure 10a. These are the traps with occupation probability close to 100%, which means that their capture time is much shorter than the emission time. For these traps, charge capture is by far the most likely event. For instance, if a transistor is turned on by applying a voltage at its gate terminal, the surface potential changes in such a way that trap occupation probability increases. The rate at which charge carriers are captured abruptly becomes larger than the rate at which carriers are emitted, and the number of trapped charges increases over time. Traps change their occupation state according to their characteristic time constant, the faster traps (the ones with shorter capture time constants) become filled first, while the slowest traps take longer to become filled. Each trap that becomes occupied degrades the channel conductivity, decreasing the device current. In largely scaled devices (i.e., with a very small area) this current decrease is seen to occur in discrete steps, each step being related to the capture of a single channel carrier (Fig. 10a bottom). Since the dynamics of this occupation depends on the bias point and temperature, it may lead to bias temperature instability (BTI).

On the other hand, traps that contribute to Random Telegraph Noise (RTN) are the ones that keep switching their state between occupied and empty. These are the traps with occupation probability close

to 50%, which means that their capture and emission times are similar. These traps show significant activity, by capture and subsequent emission of charge carriers from the channel region (Fig. 10b) [31].

Nowadays it is believed that RTN is an important factor in the understanding of BTI reliability issues in advanced CMOS technologies. In this regard, it has been proposed that RTN and the recoverable component of BTI are very likely related to the same kind of defects. There are several reasons that prove it; in the first place all defects that contribute to the BTI recovery can also become spontaneously charged, leading to an RTN signal, and most RTN defects would contribute to BTI recovery as well. Secondly, the distributions of RTN and BTI characteristic parameters are similar for the two phenomena and lastly, both RTN and BTI defects are volatile, meaning that they can disappear and reappear [23].

The similarities between RTN and BTI mentioned above make it of utmost importance to analyse and characterize both phenomena together. In this direction, a model that is able to describe both mechanisms simultaneously will be described in the next section.

3. The Probabilistic Defect Occupancy Model (PDO)

During circuit operation, the variability effects related to the trapping/detrapping in/from oxide defects could result in circuit malfunction due to the shift of some transistor parameters, such as the threshold voltage (V_T). Thus, it is critical for IC designers to consider TDV effects to implement reliability-aware circuits. To this end, appropriate TDV compact models, like the Probabilistic Defect Occupancy (PDO) model [18], are essential. These models need to account for and clearly distinguish the 'slow' defects, responsible for aging-induced degradation, from the 'fast' defects causing the RTN transient variations [17]. This model can describe the observed ΔI_D or its equivalent ΔV_T.

As already mentioned in previous sections, RTN behaviour described by the charge/ discharge events produces drain current shifts. However, those events may be hidden by the background noise at lower currents. The drain current shift at two different time instants is given by $\Delta I_D = I_D(t_2) - I_D(t_1)$ where t_2 is large enough to activate the trapping of defects. The time window or time sweep of these two times, corresponds to the stress time $\boldsymbol{t_s = t_2 - t_1}$ as can be seen in Figure 11.

Note that ΔI_D can be $\Delta I_D = 0$, $\Delta I_D > 0$ or $\Delta I_D < 0$.

- If $\Delta I_D = 0$, then there are no defects in the device or, if there are any, they do not effectively change their occupancy state during the stress/measurement time.
- If $\Delta I_D > 0$, then the defects have changed its occupancy state during the measurement by detrapping a carrier in t_2 in regard to t_1.
- $\Delta I_D < 0$, then the defects have changed their occupancy state during the measurement by trapping a carrier in t_2 in regard to t_1.

To model these ΔI_D shifts produced by RTN and BTI aging phenomena under biasing conditions in the presence of background noise, the following equation, where the three effects are modelled together, is proposed [18].

$$\boldsymbol{\Delta I_D = \sum_{i=1}^{i=N_{RTN}} \eta_{RTN,i}[oc_i(t_2) - oc_i(t_1)] + \sum_{i=1}^{i=N_{BTI}} \eta_{BTI,i} + randn(\sigma)} \qquad \textbf{(1)}$$

This model permits to obtain V_T (or equivalently I_D) variability under arbitrary V_{GS} biasing conditions and is based on the stochastic properties of the trapping/detrapping of charges in/from defects. It assumes that each individual device has a finite number of active defects (N) that can be charged or discharged. This behaviour will produce different V_T variations in the device due to the contribution of each defect. In this scenario, an active defect can capture a charge producing a decrease of the I_D device current or an increase of the I_D current if a defect releases a charge. In this model, the ΔI_D can be described by Eq.

(1) being N_{RTN} and N_{BTI} the number of active defects linked to RTN and BTI, respectively; $\eta_{RTN,i}$ and $\eta_{BTI,i}$ the current shifts associated to the RTN and BTI caused by the trapping/detrapping in the i-th defect; $oc_i(t)$ the probability of occupation of the i-th defect at time t, which is 1 if occupied or 0 if empty, and the $randn(\sigma)$ term represents the background noise which follows a Gaussian distribution with mean value 0 and standard deviation σ. When it comes to the number of active defects, N_{RTN} and N_{BTI} can be different for each device, while η_{RTN} and η_{BTI} can be different for each defect. This indicates that nominally identical devices undergo different variations, which requires considering the statistical distributions of these parameters for an accurate phenomenological modelling. To model the statistical distribution of currents, we assume that N_{RTN} and N_{BTI} follow a Poisson distribution, with mean values $< N_{RTN} >$ and $< N_{BTI} >$, respectively, while η_{RTN} and η_{BTI} follow an exponential distribution with mean values $< \eta_{RTN} >$ and $< \eta_{BTI} >$, respectively. Notably, these distributions depend on only one parameter, i.e., their average value. Then, by correctly introducing these four parameters into Eq. (1), it is possible to model the statistical behaviour of RTN and BTI together. Furthermore, including sigma in the model allows considering background noise effects into the current shifts [18].

3.1. The Cumulative Distribution Function (CDF)

Since the equation described (Eq. 1) models the current distributions in summative terms, we can plot the experimental ΔI_D shown in Figure 11 statistical distributions using the Cumulative Distribution Function (CDF) of ΔI (Fig. 12). The CDF serves as a powerful tool for extracting detailed information as it captures the probability that a random variable is less than or equal to a certain value, in our case, the probability of a current shift value being less or equal to a certain value.

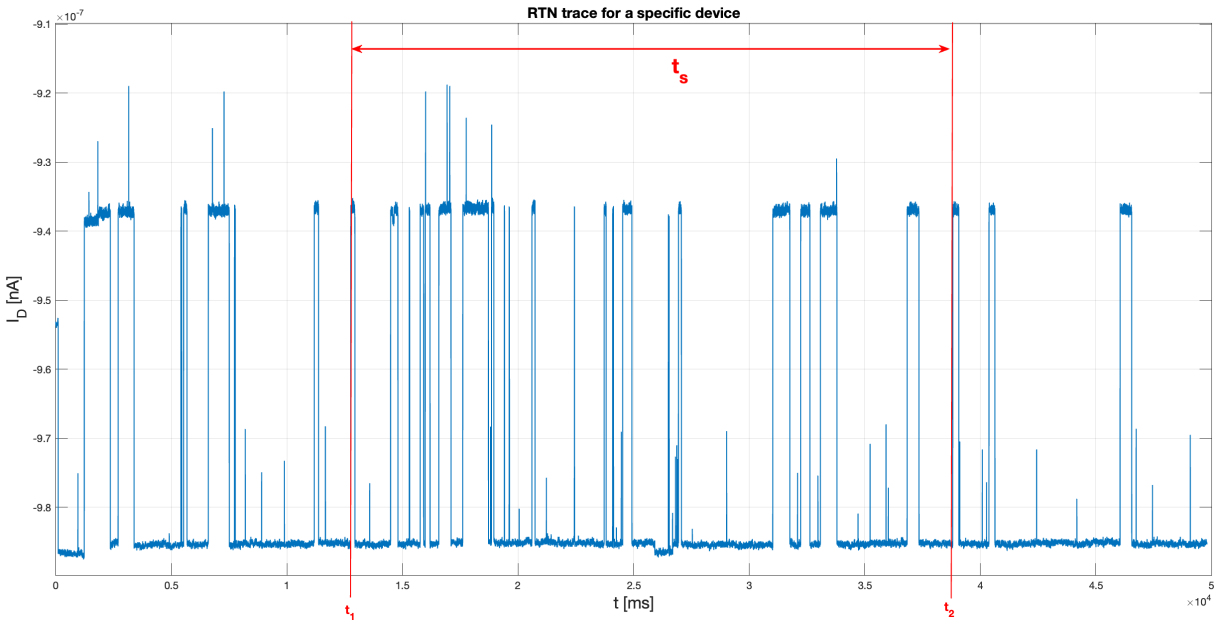

Fig. 11. Example of RTN trace for a single device

In our study, this tool is going to be key to extract detailed information about both the statistical nature of current shifts and the underlying parameters. This will contribute to a comprehensive understanding of Random Telegraph Noise and Bias Temperature Instability phenomena in electronic devices. This type of representation offers insights into the statistical behaviour of RTN and BTI, capturing the probability distribution of current shifts over time.

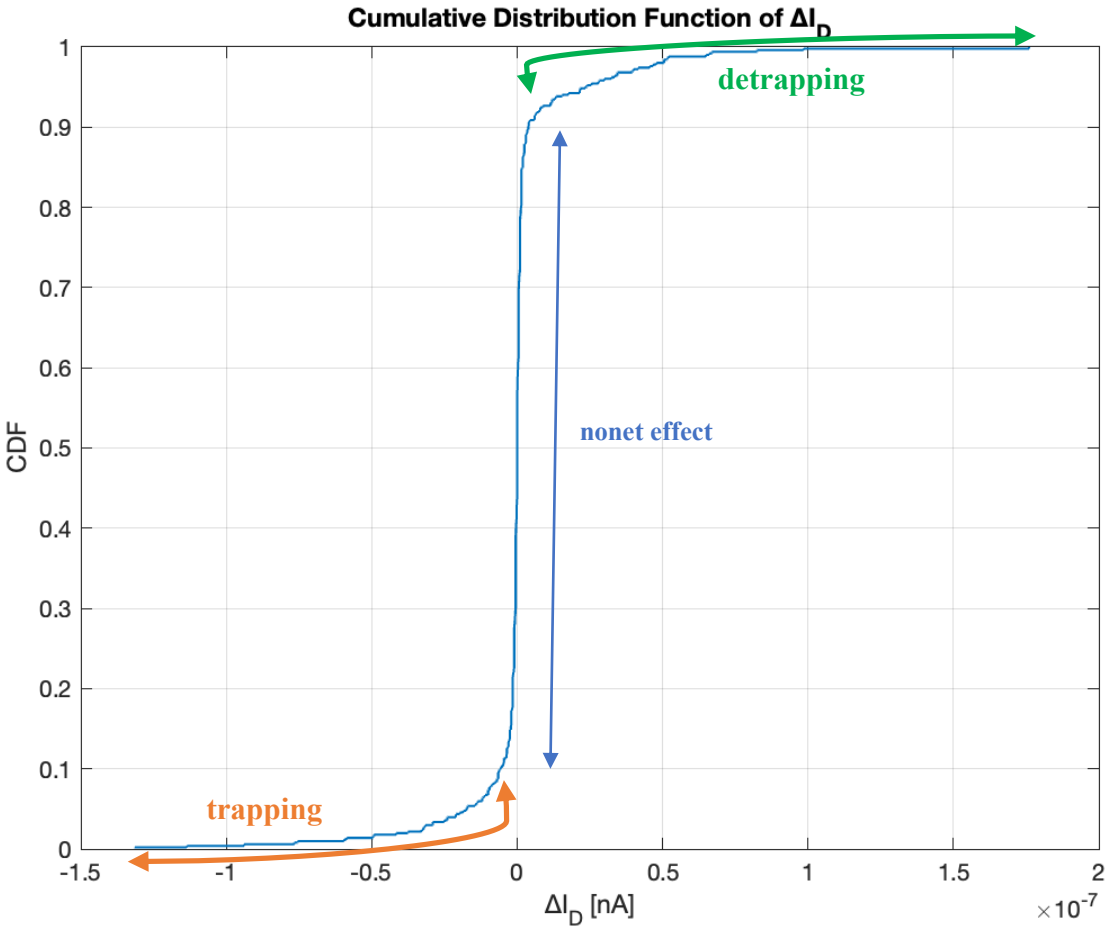

Fig. 12. Cumulative Distribution of ΔI_D for 504 devices

Some of the useful information we can obtain is the discrete charge trapping and detrapping events characteristic of RTN or trapping events characteristic of BTI phenomena by observing the CDF tails. If we consider that negative tails of the CDFs can be attributed to trapping events (Fig. 12) since when a charge is trapped the drain current decreases, and positive tails to detrapping events (Fig. 12) since drain current increases, we can describe the behaviour of defects when it comes to the stress time applied and other operating conditions. Also, the region of the CDF where the current shifts equal 0 ($\Delta I_D = 0$) (Fig. 12) suggests either the absence of defects in the device or, if present, that their occupancy states remain relatively stable throughout the stress period.

CDFs can be compared across different technologies, time stresses, temperatures, or bias conditions to understand the impact and dependencies of biasing conditions on both phenomena. In this line, observing how BTI-induced degradation evolves over time, provides insights into the aging effects on transistor performance helping in the characterization of stress-induced effects. Finally, comparing the CDF with theoretical or simulated distributions validates models by finding discrepancies between observed and modelled CDFs and permits model improvement.

In summary, CDF statistical analysis of RTN and BTI traces provide a complete view about statistical aspects, defect characteristics, and their temporal variations, facilitating informed decision-making for device design, reliability assessment, and optimization of electronic systems.

4. The ENDURANCE array-based Integrated Circuit chip

4.1. ENDURANCE description

In order to achieve truly reliable integrated circuits (ICs), accurately characterizing the effects of Time-Dependent Variability (TDV) in modern CMOS technologies has become a crucial step. However, it is impractical to characterize transistors over a long period of time. Instead, a typical aging characterization procedure involves conducting accelerated aging tests. These tests involve raising the temperature and/or the drain voltage and/or the gate voltage above their nominal values for a shorter period of time to induce the device degradation faster, known as the stress time (t_s). These elevated voltages and temperatures are referred to as stress conditions. During the stress-measurement (SM) cycle, the devices are subjected to multiple periods of stress, with the duration of each period increasing exponentially from seconds to hours. After each stress period, the device performances are evaluated by measuring the current at low voltages, to assess the impact of the stress. By comparing the extracted main parameters of the transistors with their pre-stress values, the shifts in their performance can be computed [12].

Due to the stochastic nature of these phenomena, a large number of devices must be characterized to obtain trustworthy characterization results. Typically, device characterization techniques are conducted using probe stations for on-wafer device measurements. This characterization procedure, which implies physical contact on usually one Device Under Test (DUT) at a time, results in long serial aging test times when thousands of transistors are involved. In this work, to overcome these limitations, a unique ICs has been utilized in order to effectively analyse the variability phenomena and conduct precise statistical characterization of RTN, BTI, and other TZV effects in a single IC chip. Array structures have two advantages for the statistical characterization of TZV and TDV in CMOS transistors: on the one hand, a larger number of DUTs can be characterized for a given silicon area, on the other hand, proper parallelization techniques can be used to significantly speed up the statistical characterization. To achieve rapid and reliable statistical characterization of TDV effects, it is necessary to employ array structures consisting of numerous transistors. These array structures enable the automated characterization of thousands of DUTs by incorporating digital circuitry to regulate access to each DUT terminal via the IC pads. This access capability also offers the added benefit of parallelizing the aging tests, allowing multiple DUTs to be stressed simultaneously. As a result, the overall characterization time is significantly reduced [12].

This ICs uses a stress parallelization capability of the array-based approach to carry out the measurements. The design of the ENDURANCE chip (Fig. 13) guarantees the capability to perform reliable characterization of all significant reliability effects, including TZV, RTN, BTI, and also, HCI aging [12].

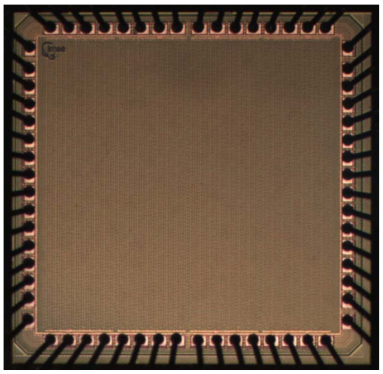

Fig. 13. ENDURANCE chip [12]

This DUT array chip, named ENDURANCE has been fabricated in a 65-nm CMOS technology and encapsulated in a JLCC68 package for testing. It contains 3136 CMOS transistors, which allow performing a trustworthy TZV and TDV characterization, and both serial and parallel stresses of DUTs. The chip includes 3136 regular-threshold-voltage MOS transistors (nominally operating at maximum 1.2 V) or DUTs distributed over two matrices, one of nMOS transistors and another of pMOS transistors. Each DUT matrix is subdivided into two submatrices of 56 rows and 14 columns, named "left/right DUT block," and containing 784 DUTs each. Figure 14 shows the main building blocks of the ENDURANCE IC chip [12].

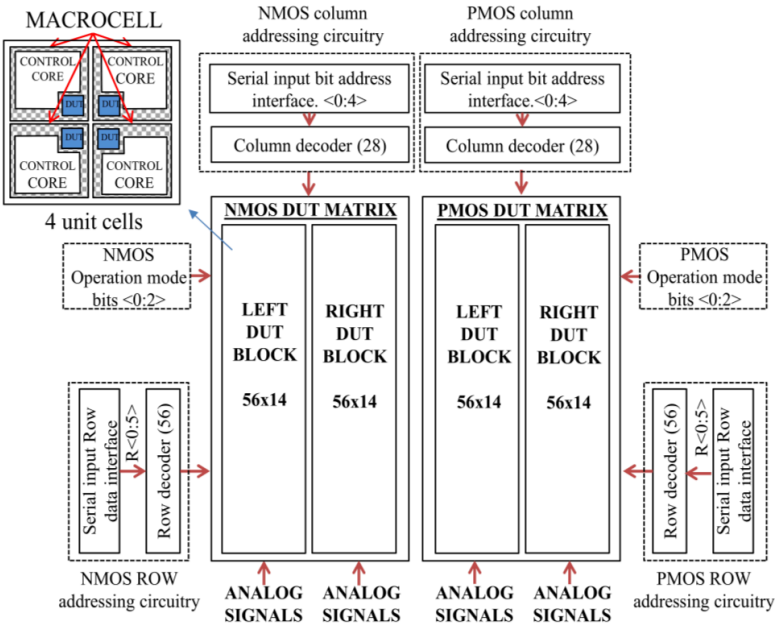

Fig. 14. ENDURANCE architecture [12]

4.2. Measurements

The ENDURANCE chip is equipped with the capability to execute three distinct operation modes by interfacing each Device Under Test (DUT) with the internal signal paths for stress, measurement, or standby [12]. However, in the context of this specific work, the data was obtained by subjecting the devices under nominal and lower operating conditions and recording the full current trace during a pre-determined time. The primary focus of this investigation was to analyse the impact of two Time Dependent Variability (TDV) agents: Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI) under normal operational parameters.

As mentioned above, given the stochastic behaviour of defects from device-to-device, to achieve a meaningful statistical characterization and fully understand or describe RTN and BTI phenomena, a substantial number of devices were essential, and enough data points were expected from measurements. For that reason, these measurements were performed under nominally identical bias conditions in different devices. In this specific study, 504 different devices or pMOS transistors were subjected to measurements under the several biasing conditions getting a total of 25000 data points or time instants in order to get a complete statistical characterization and modelling of the phenomenology. Each transition between these 25000-time instants occurred at 2-millisecond intervals, accumulating a total measurement duration of 50 seconds, enough to grant the trapping/detrapping events since it is sufficiently a larger time than some of the defects' time constants.

The prescribed operating conditions involved applying gate voltages in proximity to the nominal operation voltage (i.e., V_G = 1.2V) and below. Specifically, the operating conditions consisted of gate voltages around the threshold voltage (V_T) and above, i.e., absolute values of $\mathbf{V_G = 0.6V}$, $\mathbf{V_G = 0.7V}$, $\mathbf{V_G = 0.8V}$, $\mathbf{V_G = 1.0V}$ and $\mathbf{V_G = 1.2V}$ for a drain voltage of $\mathbf{V_D = 0.1V}$, while the source voltage was kept at $\mathbf{V_S = 0V}$ (grounded). Note that the mentioned voltage values are inherently negative, as they pertain to pMOS (p-type Metal-Oxide-Semiconductor) transistors, as well as the measured currents.

Finally, for this specific investigation, measurements were conducted without stress phases, constituting a one-time measurement approach. Thus, to study the influence of various test durations (t_s) on RTN and BTI and considering the absence of parallelizing or stress phases during the measurement stage, the statistical study phase utilized the two-point method ($t_s = t_2 - t_1$) described before instead. Although parallelization has not being used in this work, this approach allows reducing the time required for measuring RTN traces for the statistical analysis of the samples.

CHAPTER II

1. Development

The electrical characterization of the MOSFET's in the ENDURANCE chip was conducted using the experimental setup depicted in Figure 15 at the *Instituto de Microelectrónica de Sevilla* (IMSE-CNM).

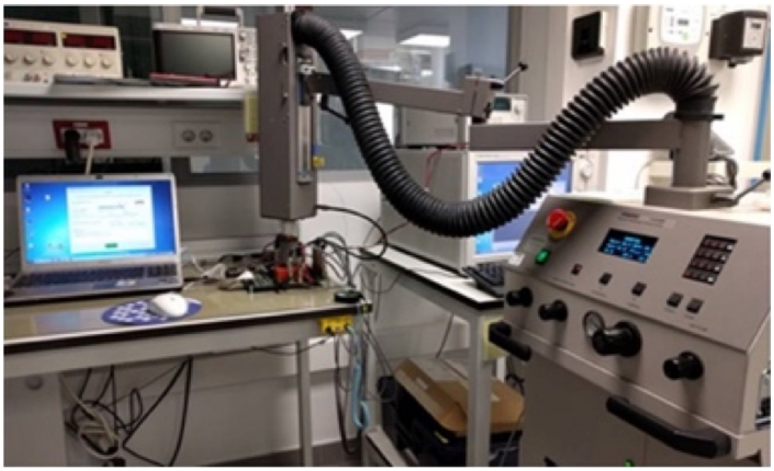

Fig. 15. Laboratory set-up for measurements

This setup included a custom-designed Printed Circuit Board (PCB) shown in Figure 16 that connects the instrument to the chip. The Keysight B1500 Semiconductor Parameter Analyzer (SPA) was utilized for voltage biasing of the Devices Under Test (DUTs) through the provided Force-and-Sense connections of its source measurement units (SMU). Simultaneously, the Agilent E3631A power supply was employed for chip biasing [12].

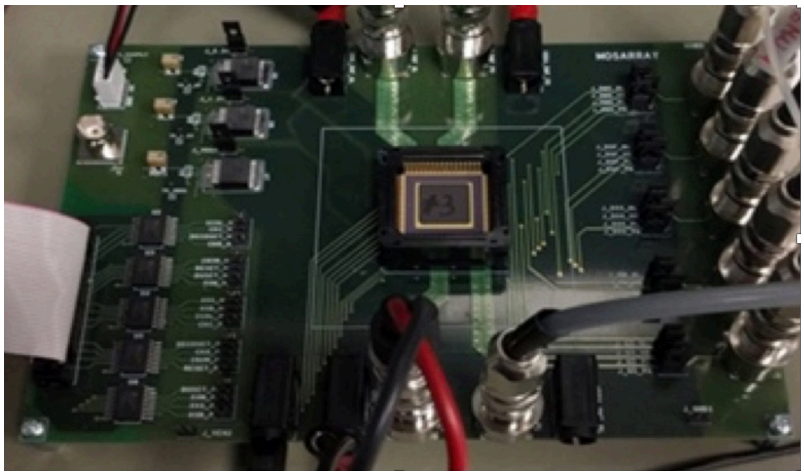

Fig. 16. ENDURANCE chip in PCB

1.1. RTN traces extraction

As mentioned in the previous section, for this specific setup and specific biasing conditions, a total of 25000 data points or time instants with 2-millisecond intervals between points were obtained, accumulating a total measurement duration of 50 seconds in 504 different PMOS devices for each voltage condition, i.e., $\mathbf{V_G = 0.6V}$, $\mathbf{V_G = 0.7V}$, $\mathbf{V_G = 0.8V}$, $\mathbf{V_G = 1.0V}$ and $\mathbf{V_G = 1.2V}$ for a drain voltage of $\mathbf{V_D = 0.1V}$ and source voltage $\mathbf{V_S = 0V}$ (grounded). Therefore, a total of 63-million data points from 504 current traces of 50 seconds each (25000 data points) for 5 different voltages are the result of the measurements. Once this massive number of samples is obtained, the next step is to analyse and plot in MATLAB the drain current I_D and find signs of RTN. As examples, different RTN traces for the $\mathbf{V_G = 0.6V}$ condition are represented in Figures 17-19 for different devices, where RTN behaviour, i.e., current shifts caused by trapping and detrapping events, can be easily identified in Figures 17 and 18.

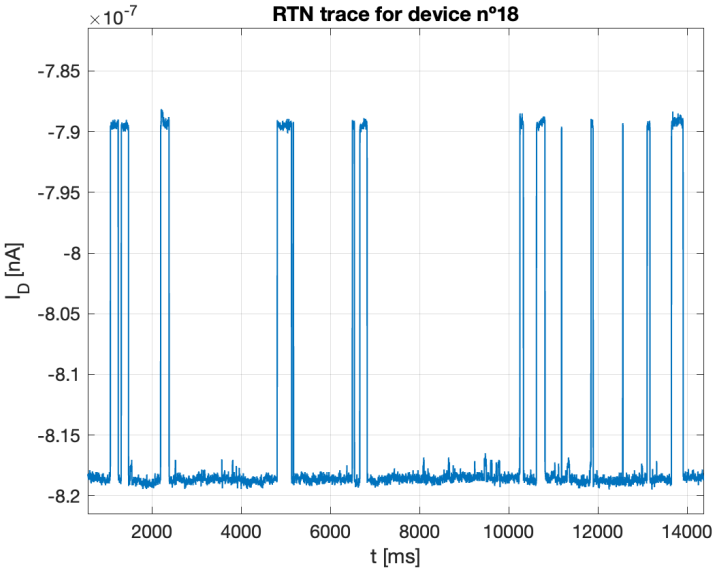

Fig. 17. RTN trace for device nº18

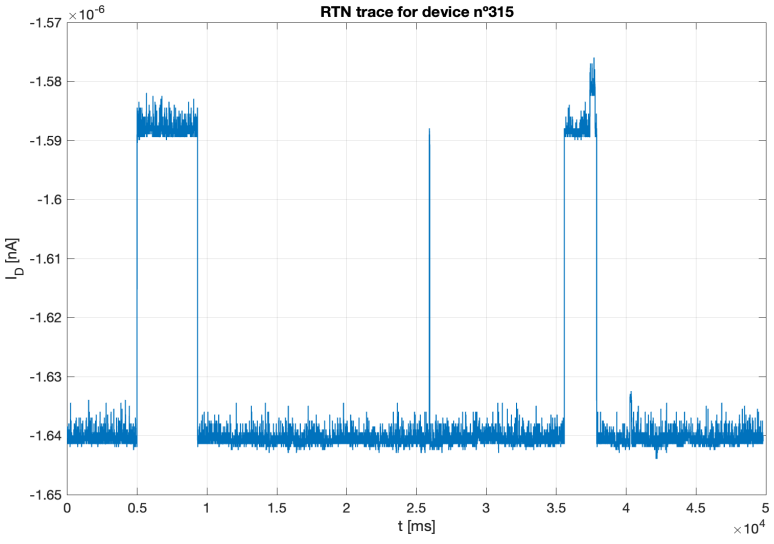

Fig. 18. RTN trace for device nº315

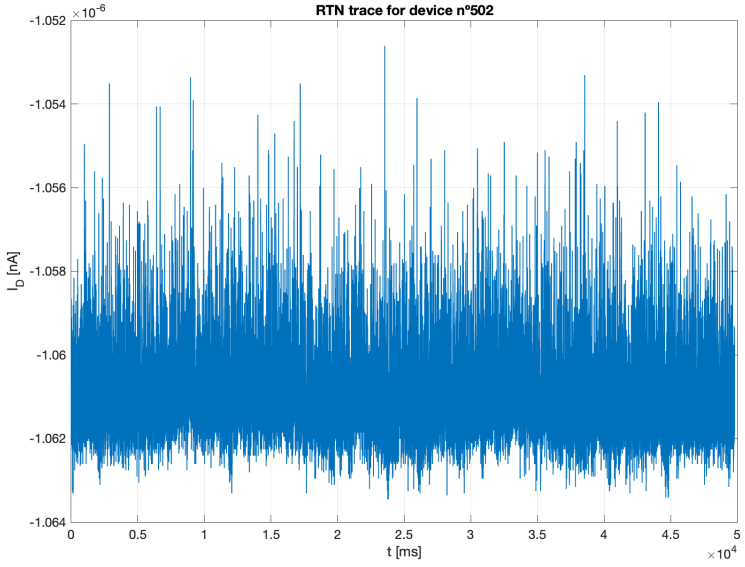

Fig. 19. RTN trace for device nº502

After plotting these traces for 3 different devices under the same biasing condition (V_G = 0.6V) we realize that RTN traces differ one from another between devices (Fig. 17, Fig. 18), changing its behaviour considerably from device to device. There are also devices that show no RTN traces at all (Fig. 19).

This insight clearly stresses the importance of conducting a thorough statistical characterization in a substantial number of devices, given the inherently stochastic nature of the RTN signal due to the random behaviour of defects from device-to-device. For this reason, the large dispersion of the RTN between devices makes it necessary to investigate a sufficiently large number of cells, to allow statistical evaluation of the real impact of RTN at circuit level and gain a deeper understanding of RTN and BTI time dependent variability phenomena.

1.2. Cumulative Distribution of current shifts ΔI_D

As we already emphasized, from these measurements many gigabytes of data have been obtained ready to be analysed. This creates the necessity to automatize the process of data analysis and parameter extraction by developing a software program able to reduce the time required to analyse such amount of data. In this particular case, MATLAB has been used to implement a program able to make the functions described. Some of the most useful data analysis that has been implemented is the statistical study of current shifts (ΔI_D) through their Cumulative Distribution Function for different stress times (t_s) and gate voltages (V_G) as will be described next. The CDF is used to estimate the cumulative probability that a random variable is less than or equal to a certain value as can be seen in the following code lines from MATLAB (Fig. 20).

```
1.  […]
2.  Id = m_current(5000,:) - m_current(1,:); % calculates the current shift
3.  Id_orden = sort(Id); % sorts the values of current shifts
4.  n = length(Id_orden);
5.  prob_acumulativa = (1:n)/n; % calculates the vector of cumulative probabilities
6.  x = Id_orden;
7.  y = prob_acumulativa;
8.  […]
```

Fig. 20. Code extracted from 'codiCDF.m', see more in Annex.

In the first line of code (Fig. 20) we observe how the calculation of the current increase (ΔI_D) is carried out by taking two specific times t_1 and t_2 that will make up the stress time by means of the already described method of the two points $t_s = t_2 - t_1$ (Fig. 11 from CHAPTER I), the line `prob_acumulativa = (1:n)/n;` is calculating the Cumulative Distribution Function (CDF) of the current shifts.

In this case, `Id_orden` contains the ordered values of the Id variable, and `prob_acumulativa` or the cumulative probability is calculated by dividing the integers from 1 to the total number of elements in `Id_orden` (which is n) by n, creating a vector that represents the cumulative probability of the drain current shift. Each element of this vector indicates the cumulative probability that a current shift (ΔI_D) value is less than or equal to the corresponding value in `Id_orden`.

To determine the time dependence of this CDFs, we carry out a time sweep for 5-, 50-, 500- and 5000-time instants getting the CDF for **10 ms, 100 ms, 1000 ms (or the equivalent, 1 s), and 10000 ms (or the equivalent, 10 s) stress times** respectively as can be seen in the figure below (Fig. 21).

```
1.  […]
2.  for i = [5 50 500 5000] % time instants
3.      Id = m_current(i,:) - m_current(1,:); % calculates current shifts for each t_stress
4.      Id_orden = sort(Id); % sorts the values of current shifts
5.      n = length(Id_orden);
6.      prob_acumulativa = (1:n)/n;
7.      x = Id_orden;
8.      y = prob_acumulativa;
9.      ts = i*2; % stress time in milliseconds (interval between time instants is 2ms)
```

```
10. […]
11. end
12. […]
```

Fig. 21. Code extracted from 'SaveCDFs.m', see more in Annex.

This process has been repeated for each of the biasing conditions described, **V_G = 0.6V, V_G = 0.7V, V_G = 0.8V, V_G = 1.0V** and **V_G = 1.2V**, to study the time dependence and voltage dependence of RTN signals.

1.3. Parameter extraction from the CDF: the model

The full modelling of the ΔI_D distributions requires the evaluation of their dependencies on time and the biasing conditions, so that the voltage dependencies of parameters like the average number of active defects behind each RTN trace set <N> have been studied.

According to the compact model that the *Reliability of Electron Devices and Circuits* (REDEC) group at the *Universitat Autònoma de Barcelona* (UAB) is developing, Eq. 2 describes the average number of active defects in a set of devices, i.e., average number of defects per device that have been activated by trapping or detrapping events and produce a current shift.

$$< N > = \sqrt{2(2 + aL^b)} \cdot \ln(p_0) \qquad (2)$$

Where a = 0.878 and b = 1.92 are two fitting parameters; $L = log_{10}(t_s) - log_{10}(2ms)$, being the number of time decades in which the defects can be detected (where 2ms is the minimum time measured). Finally, p_0 is the probability of current shift's value being 0, i.e., $\Delta I_D = 0$ as can be seen in Figure 22.

From a statistical perspective, this last parameter (p_0) can be observed from the CDF graph directly by calculating the difference between the point where the positive values of the positive tail of the CDF start (y2) and the point where the negative values of the negative tail end (y1). These points can be seen in Figure 22 as red dots.

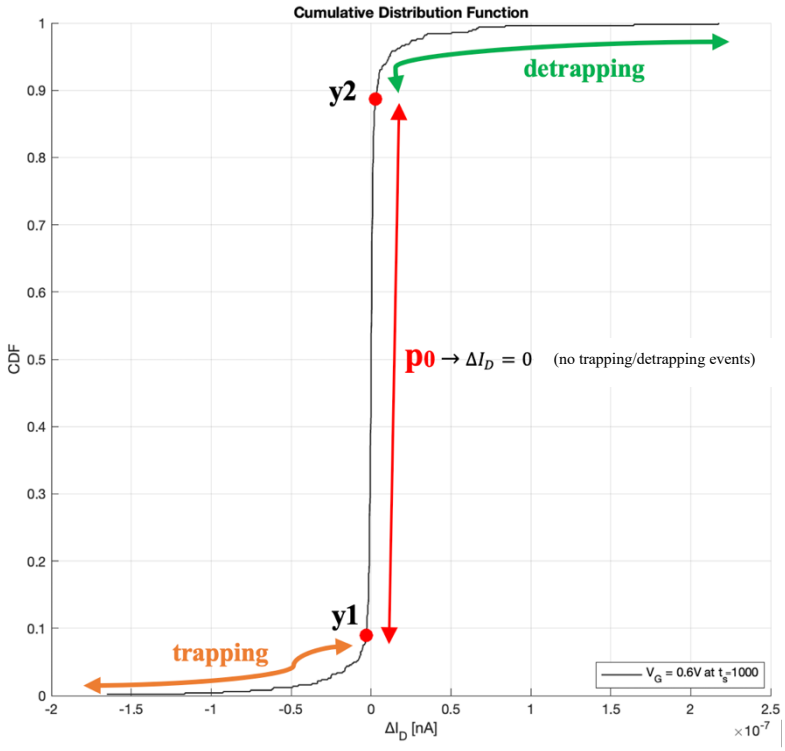

Fig. 22. Example of CDF for a particular condition where parameter p_0 is shown. Red dots represent points y_2 and y_1 respectively.

This simple calculation can be seen in Figure 23 line 21, `p0 = y2 - y1;`. However, in order to attain a more accurate measurement of this parameter, we need to consider the impact of experimental background noise. Therefore, we will assume that the background noise follows a Gaussian distribution with mean value 0 and standard deviation σ = 3 nA as we can see in the first code lines.

Once we have obtained the parameters needed to calculate the average number of active defects, L and p_0, we will proceed to calculate <*N*> with the equation developed by the REDEC group (Eq. 2) as we can see in the following code lines (Fig. 23).

```
1.      % calculation of minimum positive value and maximum negative value
2.      min_x_positiu = min(x(x > 3e-9)); % 3nA as standard deviation of Gaussian noise
3.      [min_y_positiu, index_positiu] = min(y(x == min_x_positiu));
4.
5.      max_x_negatiu = max(x(x < -3e-9)); % 3nA as standard deviation of Gaussian noise
6.      [min_y_negatiu, index_negatiu] = min(y(x == max_x_negatiu));
7.
8.      x2 = min_x_positiu;
9.      y2 = min_y_positiu;
10.     x1 = max_x_negatiu;
11.     y1 = min_y_negatiu;
12.
13.     %% calculation of average number of defects (N)
14.
15.     % Parameters
16.     a = 0.878;
17.     b = 1.92;
18.
19.     % L and p0 calculation
20.     L = log10(Ts) - log10(2e-3);
21.     p0 = y2 - y1;
22.
23.     % <N> equation
24.     N = abs(sqrt(2 * (2 + a * L^b)) * log(p0));
25.
26.     %%
```

Fig. 23. Code extracted from 'PlotCDFs.m', see more in Annex.

Now that we have calculated the average number of active defects <N> for each specific operating condition, we are ready to study its dependencies on stress times and gate voltage.

In the upcoming chapter, the study of the mentioned conditions and parameters will encompass the use of diverse representations to examine both the time and voltage dependencies, as well as the dependence of the <N> parameter with these operating conditions. This investigation aims to provide valuable insights into the effects and behaviours of Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI) within the circuit's operating conditions.

CHAPTER III

Results

In this section, the outcomes of the procedures outlined in the preceding chapter will be presented and analysed from a statistical standpoint. Furthermore, we will investigate the dependence of RTN and BTI effects on device performance including temporal dependence and applied voltage dependence, as well as other parameters in relation to these magnitudes. This comprehensive examination aims to provide a deeper understanding of the dependencies involved, shedding light on the intricate relationships between time, applied voltage, and various parameters in the context of the study.

1. Dependence on operating conditions

1.1. Time dependence

The Cumulative Distribution Function of current shifts for specific gate voltages at different stress times have been analysed to study the time dependence on RTN and BTI phenomena.

Among the five gate voltages we have studied, V_G = 0.6V, V_G = 0.7V, V_G = 0.8V, V_G = 1.0V and V_G = 1.2V, the most significant data can be found at the operating voltage value V_G = 1.2V and at the lowest voltage value V_G = 0.6V. Thus, these two values will be described in more detail in this section.

For the lowest gate voltage, V_G = 0.6V, the Cumulative Distribution Function for different stress times has been plotted. In Figure 24 we can find represented the CDFs for shorter to larger stress times; 10ms, 100ms, 1s and 10s. Also, in Figure 25 the results for the largest voltage value (V_G = 1.2V) have been represented to have a clear vision of the behaviour of the variability phenomena at such operating conditions.

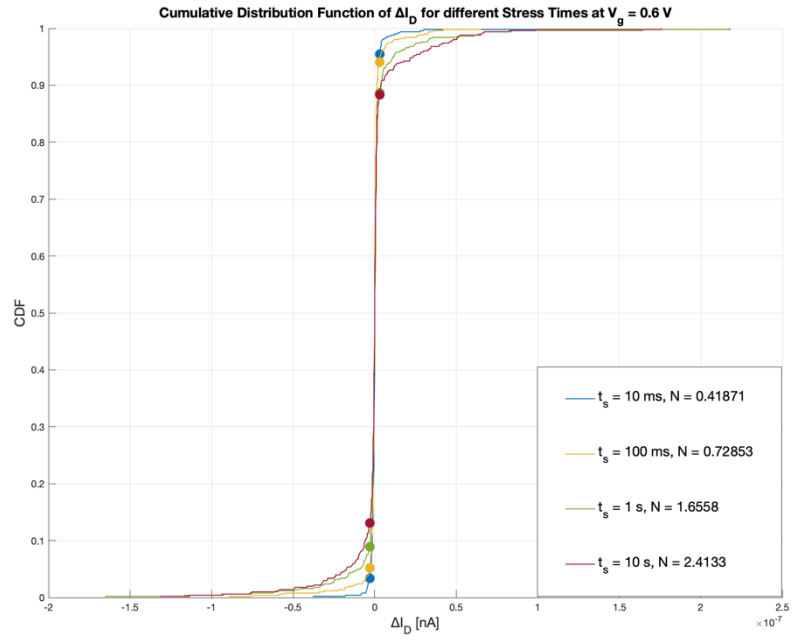

Fig. 24. CDF of ΔI_D at V_G = 0.6V (lowest voltage)

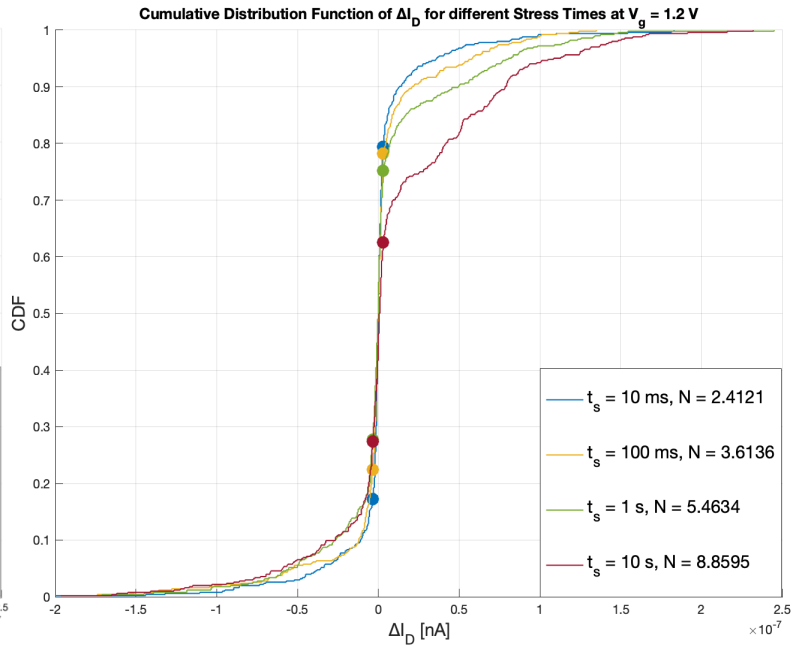

Fig. 25. CDF of ΔI_D at V_G = 1.2V (operating voltage)

First of all, in Figure 24, for the lowest voltage V_G = 0.6V, we can observe how the distribution of current shifts goes from -1.7nA to 2.2nA, with a large probability of current shifts being 0 ($\Delta I_D = 0$). As we already mentioned in section 3.1 of this work, $\Delta I_D = 0$ indicates that either there are no defects in the device or, if there are any, they do not effectively change their occupancy state during the measurement. We also observe a notable symmetry between negative tails and positive tails of the CDF that hints at a similar number of trapping and detrapping events. This clearly indicates that the number of trapping and detrapping events is similar with the probability of both events being approximately the same. Thus, as we mentioned before, this indicates a dominance of RTN at low voltage values, as it is the typical behaviour of this phenomena.

In contrast, in Figure 25 we can see how, for the largest voltage/operating voltage of V_G = 1.2V, ΔI_D rapidly increases with t_{stress} because of the larger trapping probability for larger stress times. We can note the disruption in symmetry with the prolonged stress duration, consistently presenting a higher likelihood of trapping events. This increased probability stems from the activation of more defects surpassing their capture time constants. Conversely, the probability of detrapping events diminishes at longer times. This observation, in absolute terms, points towards the manifestation of BTI, highlighting a greater tendency to trap charges than to detrap them. As stress time increases, the probability of devices having current shifts $\Delta I_D = 0$ decreases from above indicating less probability of having positive current shifts. Consequently, there is a decrease in detrapping events and an increase in trapping events relative to detrapping. This distinctive behaviour aligns with the characteristic pattern associated with Bias Temperature Instability (BTI) in which trapping events are more likely than detrapping events.

1.2. Voltage dependence

Another crucial operating condition is the voltage applied. The Cumulative Distribution Function of current shifts for specific stress times have been analysed at different voltages to study the voltage dependence on Time Dependent Variability phenomena. Among the many stress times we have represented, the most significant ones are the lowest stress time of 10 milliseconds and the largest stress time of 10 seconds. Thus, the CDFs of these two values at different gate voltages will be described in this section.

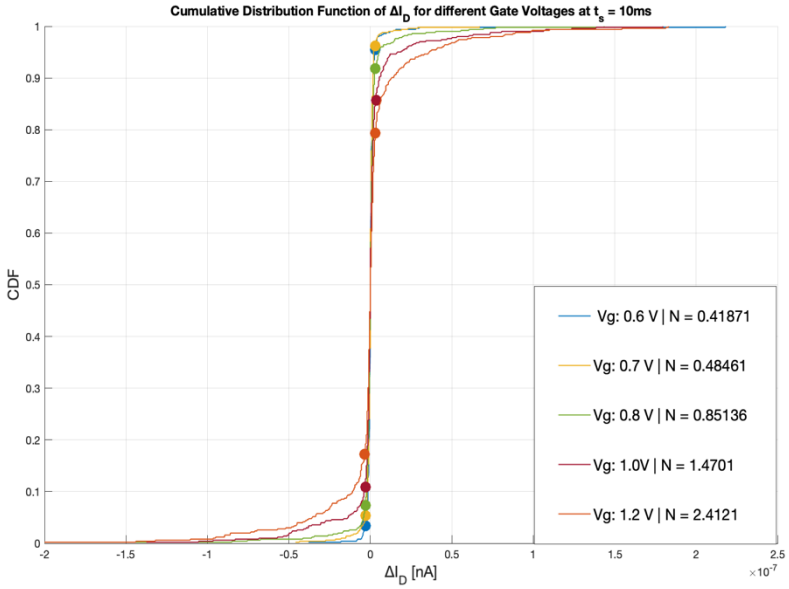

Fig. 26. CDF of ΔI_D at t_S = 10 ms (lowest stress time)

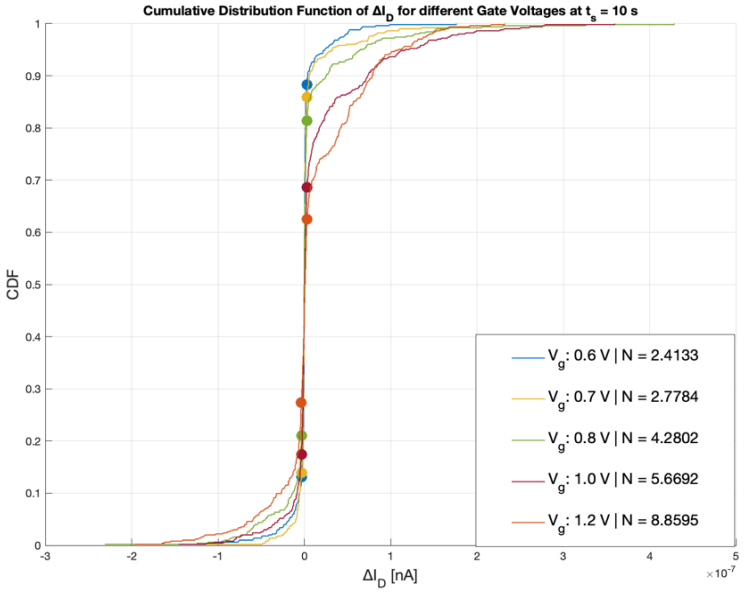

Fig. 27. CDF of ΔI_D at t_S = 10 s (largest stress time)

As we can observe the behaviour is similar to the time dependency in Figure 24. For low stress times, and in particular the lowest stress time of t_S = 10 ms, CDFs are symmetrical indicating equal probabilities of trapping and detrapping events, thus a RTN component can be seen in Figure 26. For the largest stress time (t_S = 10 s) and largest voltage values (V_G = 1.0V and V_G = 1.2V), ΔI_D rapidly increases with applied voltage because of the larger trapping probability for larger applied voltage. In this point, no symmetry is shown indicating less detrapping events in regard of trapping events, and hence a BTI component appears at voltages near to the operating voltage as can be seen in Figure 27.

The full modelling of the ΔI_D distributions requires the evaluation of their dependencies on the biasing conditions, so that the voltage dependencies of <N> have been studied in the upcoming section.
This study seeks to offer valuable insights into the main factor influencing the behaviour of Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI) in drain current, i.e., the number of active defects N, within the circuit's operational conditions.

2. Dependence of <*N*> on VG and t_S

In this section, the number of average active defects <N> is represented to study its dependence on operating conditions.

2.1. Dependence of N on V_G, as a function of the Stress Time

The dependence of the average number of active defects per device <*N*> on Gate voltage at stress times 10ms, 100ms, 1s and 10s has been represented, as shown in Figure 28.

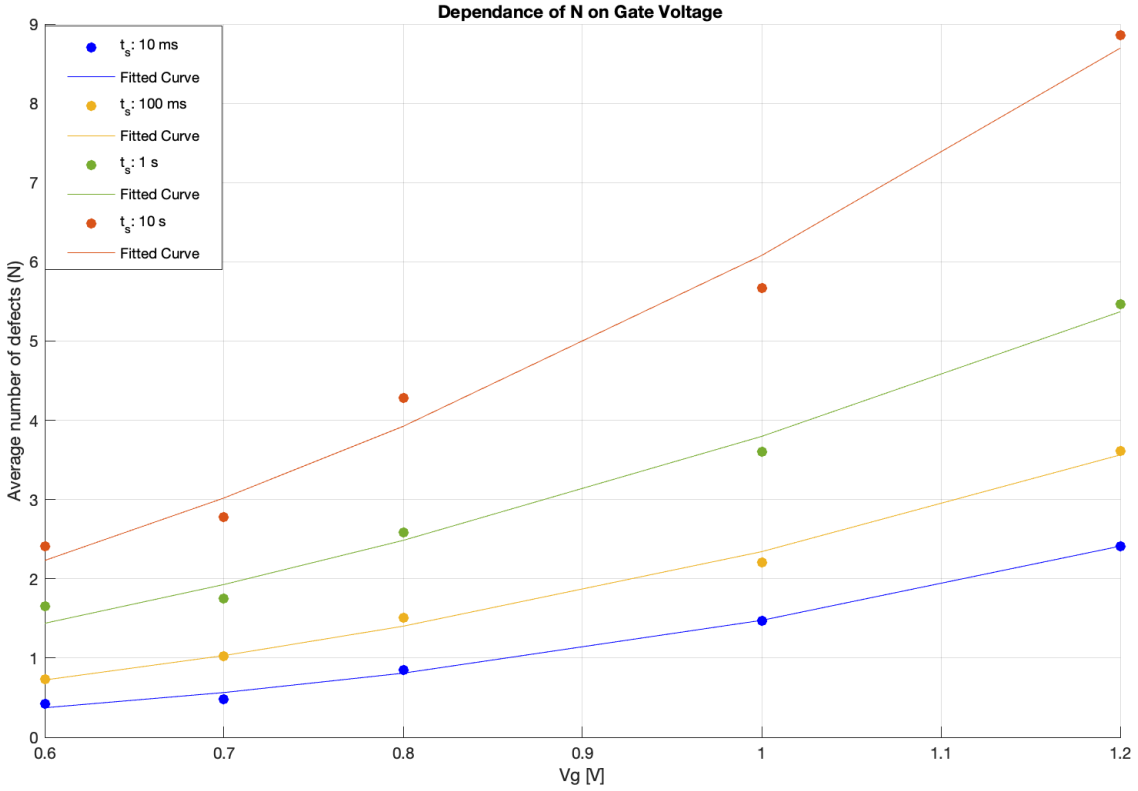

Fig. 28. Dependence of N on Gate Voltage (data points are represented by dots and fitted curves by lines)

In Figure 28, we can observe how as applied voltage increases, the number of active defects grows as well since the trapping probability increases with the applied voltage. For the largest stress time of 10 seconds at low voltages we already have more than 2 active defects, reaching rapidly almost 9 active defects per device at the operating voltage, i.e., V_G = 1.2 V. This increase in active defects is translated into RTN and BTI components.

The dependence of the average number of active defects <*N*> on Gate Voltage, is described in the studied voltage range by a potential equation of type $< N > = a \cdot Vg^b$, where a and b are fitting parameters with values a = 4.2092 and b = 2.0231.

2.2. Dependence of N on t_S, for different Gate Voltages

Another useful representation is the dependence of the average number of active defects <*N*> on the stress time plotted in Figure 29.

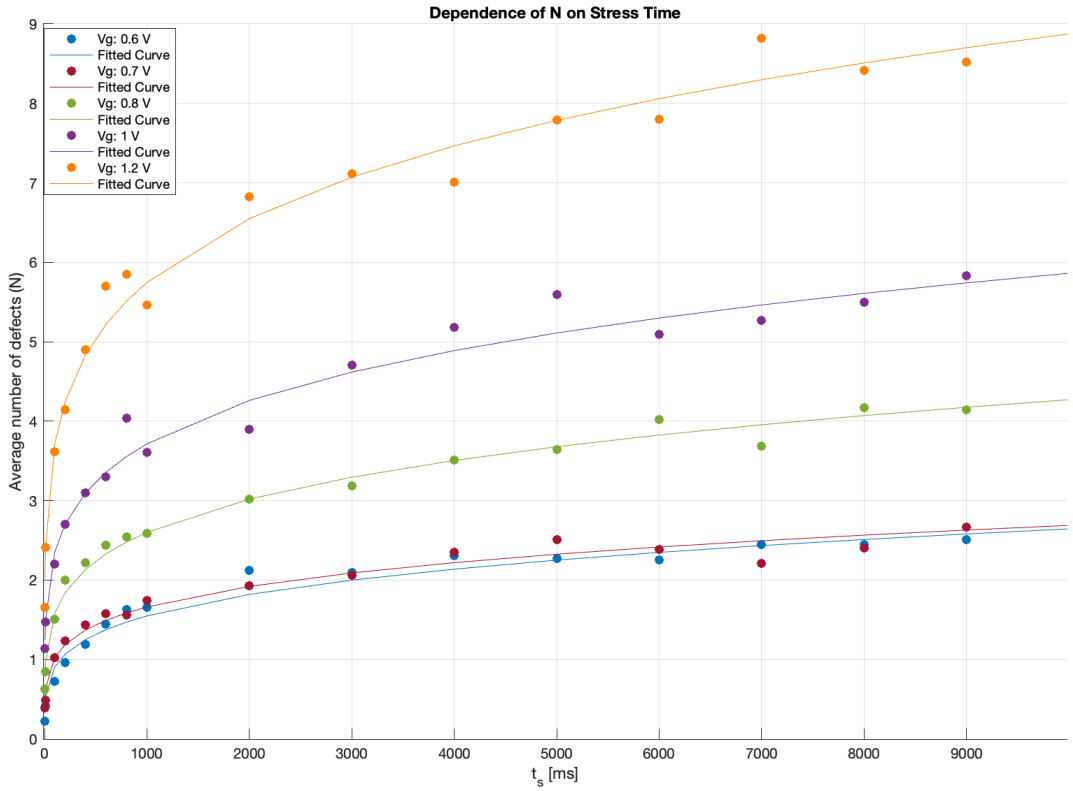

Fig. 29. Dependence of N on Stress Time (data points are represented by dots and fitted curves by lines)

As stress time increases, the number of active defects <*N*> increases as well, as shown in Figure 29. This behaviour is given by the fact that at larger stress times, defects with larger time constants (τ_e/τ_c) have been activated; reaching the maximum value of almost 9 defects at the highest voltage (operating voltage of 1.2V) and stress time of 10 seconds. This increase in active defects is translated into RTN and BTI components as well.

The dependence of the average number of active defects <*N*> on stress times is described by a potential equation of type $< N > = a \cdot ts^b$, where a and b are fitting parameters with values a = 0.755 and b = 0.2024.

3. Color Map

Finally, we can represent all the dependencies separately described above together in a color map. This will provide a comprehensive and overall picture of the dependencies between the average number of active defects <*N*> and the biasing conditions and its temporal evolution (Fig. 30a).

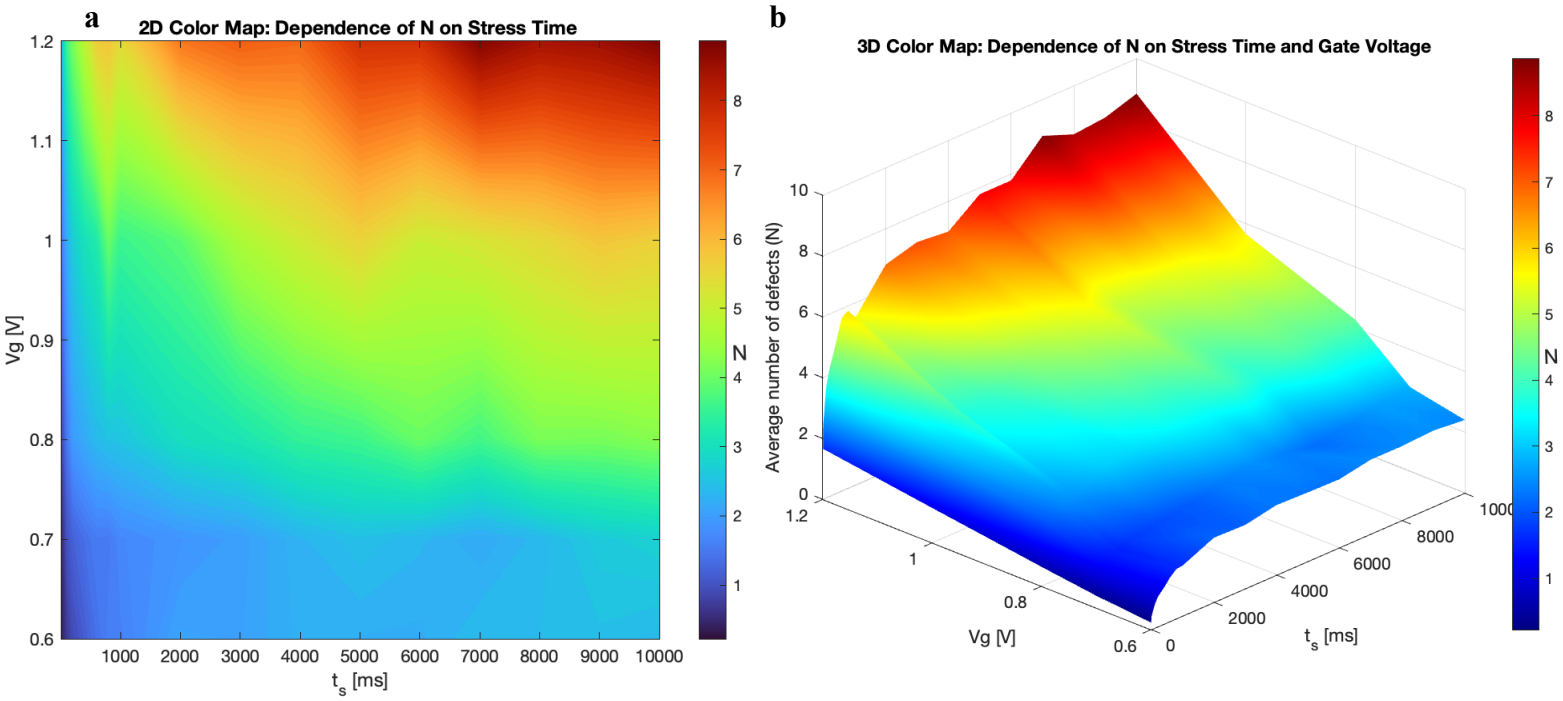

Fig. 30. (a) 2D Color Map that shows dependence of N on Stress Time and Gate Voltage
(b) 3D Color Map that shows dependence of N on Stress Time and Gate Voltage

A three-dimension graph is represented in Figure 30b where the mean number of defects as a function of the stress time and the gate voltage is plotted to identify the correlation between these three magnitudes.

As concluded from the previous graphs, this graph shows in a compact way that, as time and voltage grow, more and more defects are activated.

Conclusions

In today's ultra-scaled CMOS technologies, Time Dependent Variability (TDV) effects (such as RTN and BTI) have become significant concerns for both analog and digital circuit design, presenting challenges in reliability and performance. Given the stochastic nature of Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI), a statistical characterization approach is necessary, where multiple devices must be analysed. RTN is intricately linked to the trapping and detrapping of charges in/from defects, while in Bias Temperature Instability (BTI) gains relevance with trapping of charges in defects, adding complexity to understanding these phenomena. The development of compact models becomes crucial to address the complexities posed by RTN and BTI, and the Probabilistic Defect Occupancy (PDO) model emerges as a valuable tool, requiring parameters derived from experimental observations during statistical characterization.

This project aimed to streamline the characterization process by automating the extraction of crucial parameters from the study of Cumulative Distributions (CDF) of previously calculated current shifts ΔI_D as dictated by the PDO model. The study focused on processing vast amounts of data, involving thousands of traces generated by gigabytes of laboratory samples.

The CDFs of ΔI_D of hundreds of MOSFET devices under various biases between near-threshold and nominal operating conditions was presented in this study, interpreted within a defect-centric model (i.e., the PDO). Thanks to the methodology developed by the REDEC group of *Universitat Autònoma de Barcelona* (UAB), the extraction of an indispensable parameter for the compact model, i.e., the average number of active defects (N), was made possible. This parameter, essential for understanding the behaviour of RTN and BTI, was evaluated over a range of voltages and stress times. The exploration encompassed nominal to lowest voltages, providing insights into the effects of these phenomena on the nominal modes of operation within a circuit and their time evolution.

The analysis of the Cumulative Distribution Function (CDF) of ΔI_D for each biasing condition, confirm that the impact of RTN and BTI is strongly dependent on the operating conditions (i.e., bias and time) of the devices. By observing the variations of ΔI_D in the CDF during stress times and for applied voltages, it was demonstrated that RTN and BTI coexist, with one dominating over the other depending on the biasing conditions. The statistical analysis of measurements and extracted model parameters indicate that, for smaller applied voltages, RTN is the dominant TDV mechanism. However, BTI can also be observed at larger voltage values, and especially when the operating voltage is applied, raising concerns as these are the normal conditions under which a circuit operates. From the analysis of the

average number of active defects <N> extracted from experimental data, dependencies on the biasing conditions have also been studied. In this line, it has been determined that at larger voltage values and stress times, N grows potentially due to the increase in trapping probability.

In essence, this project not only addresses the challenges posed by RTN and BTI but also introduces a practical methodology for automating parameter extraction, reducing characterization time. The overarching goal is to advance the comprehension of the influence of these phenomena on circuit operation, paving the way for the development of more dependable and resilient ultra-scaled devices in the future.

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Table of figures

Annex

The following annex includes full code of the software developed for this specific project in MATLAB capable of automatising data extraction and statistically characterise RTN and BTI phenomena.

RTN_PlotTrace.m

```
% Plots RTN traces - Nouhaila El Bouinany

% Neteja l'espai de treball i la pantalla de la figura
clear;
clf;
clc;
close all;

load('RTN_Vg0p6.mat') % Carrega fitxer de dades
m_current(1:100,:)=[]; % Elimina les primeres 100 mostres
dispositiu = 18;
x = 1:size(m_current, 1);
y = m_current(:,dispositiu); % Carrega totes files del dispositiu


% Grafica la CDF
figure;
plot(x*2, y, 'LineWidth', 1); % (instants temps)* 2ms per obtenir el temps
title(['RTN trace for device nº', num2str(dispositiu)], 'FontSize', 14);
xlabel('t [ms]', 'FontSize', 14);
ylabel('I_D [nA]', 'FontSize', 14);
grid on;

% Tamany eixos x y
set(gca, 'FontSize', 13);
```

simpleCDF.m

```
% CDF simple function - Nouhaila El Bouinany

load('RTN_Vg0p6.mat') % Carrega fitxer de dades
m_current(1:100,:)=[]; % Elimina les primeres 100 mostres
Id = m_current(5000,:) - m_current(1,:); % Calcula l'increment de corrent
Id_orden = sort(Id); % Ordena els valors
n = length(Id_orden);
prob_acumulativa = (1:n)/n; % Calcula valors de probabilitat acumulativa
x = Id_orden;
y = prob_acumulativa;


% Grafica la CDF
figure;
stairs(x, y, 'LineWidth', 1);
title('Cumulative Distribution Function of ΔId');
xlabel('ΔI_D [nA]');
ylabel('CDF');
grid on;
```

SaveCDFs.m

```
% Calculates CDF and saves it - Nouhaila El Bouinany

% Neteja l'espai de treball i la pantalla de la figura
clear;
clf;
clc;
close all;
```

```
% fitxers: 'RTN_Vg0p6.mat','RTN_Vg0p7.mat','RTN_Vg0p7.mat','RTN_Vg1p0.mat','RTN_Vg1p2.mat'

fitxer = 'RTN_Vg1p2.mat'; % MODIFICAR. Nom del fitxer a carregar
load(fitxer) % Carreguem fitxer de dades
[~, nomSenseExt, ~] = fileparts(fitxer);% Treu extensio del fitxer
m_current(1:100,:) = []; % Elimina primeres 100 mostres

for i = [2 5 50 100 200 300 400 500 1000 1500 2000 2500 3000 3500 4000 4500 5000] % Instants t
    Id = m_current(i,:) - m_current(1,:); % Calcula l'increment de corrent
    Id_orden = sort(Id); % Ordena els valors
    n = length(Id_orden);
    prob_acumulativa = (1:n)/n;
    x = Id_orden;
    y = prob_acumulativa;
    Ts = i*2; % Cada interval son 2ms

    %% EXTRAURE Vg. Agafa el valor numeric X.X de la estructura '_VgXpX'
    % Troba el valor numèric
    valor_numeric = regexp(nomSenseExt, '_Vg([\dp.d]+)', 'tokens', 'once');
    % Substitueix la "p" pel punt decimal
    valor_numeric = strrep(valor_numeric{1}, 'p', '.');
    % Converteix la cadena al valor numeric de tensió Vg
    Vg = str2double(valor_numeric);
    %%

    dades = [x',y', repmat(Ts, length(x), 1), repmat(Vg, length(x), 1) ]; % Guarda els valors
de x, y, Ts, Vg a la matriu dades

    nom_fitxerCDF = sprintf('CDF_%s_Ts_%d.mat', nomSenseExt, Ts); % Grava el nom de fitxer amb
fitxer carregat i el Ts actual
    save(nom_fitxerCDF, "dades" ); % Grava la matriu de valors de la CDF en un fitxer .mat

end
```

PlotCDFs.m

```
% Program to graph comparisons of CDFs and <N> - Nouhaila El Bouinany
% Figure 1: CDF vs Id, Figure 2: p0 vs Ts, Figure 3: p0 vs N, Figure 4: N vs Vg, Figure 5: N vs Ts

% Neteja l'espai de treball i la pantalla de la figura
clear;
clf;
clc;
close all;

%% MODIFICAR. Llista de fitxers desitjats .mat a carregar i comparar.

% 1. Selecciona el fitxer 'CDF_RTN_Vg0p6_Ts_10' (sol fitxer especific)
prefix = 'CDF_RTN_Vg0p6_Ts_1000';
fitxers = dir([prefix, '.mat']);

% 2. Selecciona tots els fitxers començats en 'CDF_RTN_' (diversos fitxers)
% prefix = 'CDF_RTN_';
% fitxers = dir([prefix, '*.mat']);

% 3. Selecciona tots els fitxers acabats x.mat
%fitxers = dir('*10000.mat');

% Ordena els fitxers
fileNames = {fitxers.name};
numbers = cellfun(@(x) sscanf(x, '%*[^0-9]%d'), fileNames, 'UniformOutput', false);
numero = cellfun(@(x) x(end), numbers);
[~, order] = sort(numero);
sortedFiles = fitxers(order);
%%

% Inicialitza una nova figura
figure;
```

```
% Inicialitza matrius per guardar dades
num_files = length(fitxers);
vector_Ts = zeros(1, num_files);
vector_p0 = zeros(1, num_files);
vector_N = zeros(1, num_files);
vector_Vg = zeros(1, num_files);

% Itera a través de cada fitxer i en grafica les seves dades
for i = 1:length(sortedFiles)

    hold on;
    fitxer_actual = sortedFiles(i).name;
    [~, nomSenseExt, ~] = fileparts(fitxer_actual); % Treu extensio del fitxer

    % Carrega el fitxer .mat i extreu la matriu 'dades' amb els valors x, y de la CDF
    carrega = load(fitxer_actual);
    dades_actuals = carrega.dades;

    % Obté les variables x i y de la matriu 'dades' creada a 'SaveCDFs.m'
    x = dades_actuals(:, 1);
    y = dades_actuals(:, 2);
    Ts = dades_actuals(1, 3);
    Vg = dades_actuals(1, 4);

    % Trobem el mínim valor positiu i el màxim valor negatiu en el eix x
    min_x_positiu = min(x(x > 3e-9)); % 3n per tenir en compte l'efecte del soroll
    [min_y_positiu, index_positiu] = min(y(x == min_x_positiu));

    max_x_negatiu = max(x(x < -3e-9)); % 3n per tenir en compte l'efecte del soroll
    [min_y_negatiu, index_negatiu] = min(y(x == max_x_negatiu));

    x2 = min_x_positiu;
    y2 = min_y_positiu;
    x1 = max_x_negatiu;
    y1 = min_y_negatiu;

    %% Càlcul del número mitjà de defectes per dispositiu <N>

    % Paràmetres
    a = 0.878;
    b = 1.92;

    % Càlcul de L i p0
    L = log10(Ts) - log10(2e-3);
    p0 = y2 - y1;

    % Fórmula de N
    N = abs(sqrt(2 * (2 + a * L^b)) * log(p0));

    %%

    % Guarda valors de Ts, N, p0 en vectors per graficar les Fig2, Fig3, Fig4, Fig5
    vector_Ts(i) = Ts;
    vector_p0(i) = p0;
    vector_N(i) = N;
    vector_Vg(i) = Vg;

    % Figura 1: Grafica les CDFs i el valor de N a la llegenda
    nomSenseExtLeg = strrep(nomSenseExt, '_', ' '); % Per evitar que MATLAB interpreti '_' del
nom de fitxer com a subíndex a la llegenda
    h = stairs(x, y, 'LineWidth', 1, 'DisplayName', [nomSenseExtLeg ' | N = ' num2str(N)]);

    % Representa punts de p0 a la gràfica amb el mateix color que la seva CDF
    color_linea_actual = get(h, 'Color');
    scatter([x2, x1], [y2, y1], 100, color_linea_actual, 'filled','HandleVisibility', 'off');

    % % Mostrem els resultats a la consola
    % disp(['----' nomSenseExt '----']);
    % disp(['Mínim valor positiu eix x: ', num2str(x2), ', Punt mínim de y corresponent: ',
sprintf('%.10f', y2)]);
    % disp(['Màxim valor negatiu eix x: ', num2str(x1), ', Punt mínim de y corresponent: ',
sprintf('%.10f', y1)]);
```

```
    % disp(['p0 = ', sprintf('%.10f', p0)]);
    % disp(['N = ', sprintf('%.2f', N)]);

    % Guardem els valors dels parametres Ts, L, p0 i N en un fitxer MATLAB
    % parametres = struct('ts', Ts, 'L', L,'p0', p0, 'N', N);
    % save('parametres.mat', '-struct', 'parametres','-v7.3'); % MODIFICAR NOM. Grava els
valors dels parametres en un fitxer .mat

end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% FIGURES %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% FIGURA 1: CDFs en funció de ΔId

% Etiquetes i llegenda de la Figura 1
xlabel('ΔI_D [nA]');
ylabel('CDF');
title('Cumulative Distribution Function');
legend('show');

grid on;
hold off;

% MODIFICAR NOM. Gravar la Figura 1 (.fig) amb nom desitjat
% savefig('CDF_comparativaTs_Vg.fig');
% %%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% FIGURA 2: Dependència de p0 amb Ts. Unica Vg diferents Ts.

% Grafica la dependència de p0 amb Ts
figure;
plot(vector_Ts, vector_p0, '-x', 'LineWidth', 1.5);
xlabel('t_s [ms]');
ylabel('p0');
title('Dependència de p0 amb t_s');
grid on;

% Etiquetes amb el valor dels punts
text(vector_Ts, vector_p0, num2str(vector_Ts'), 'HorizontalAlignment', 'left',
'VerticalAlignment', 'bottom');

% % MODIFICAR NOM. Gravar la Figura 2 (.fig) amb el nom desitjat
% savefig('Dependencia_p0_ts.fig');


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% FIGURA 3: Dependència de p0 amb N. Única Vg diferents Ts.

% Grafica la dependència de p0 amb N
figure;
plot(vector_N, vector_p0, '-o', 'LineWidth', 1.5);
xlabel('Número mitjà de defectes (N)');
ylabel('p0');
title('Dependència de p0 amb N');
grid on;

% Etiquetes amb el valor dels punts
text(vector_N, vector_p0, num2str(vector_p0'), 'HorizontalAlignment', 'left',
'VerticalAlignment', 'bottom');

% % MODIFICAR NOM. Gravar la Figura 3 (.fig) amb el nom desitjat
% savefig('Dependencia_p0_N.fig');


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% converteix els vectors en matrius

% disp(['Warning: i=', num2str(i)]);
numVoltatges = 5; % MODIFICAR: num. de voltatges que comparem
```

```
numeroTempsTs = i/numVoltatges; % retorna la quantitat de ts que tenim de cada Vg

% reshape converteix els vectors en matriu al tallar els vectors cada
% 'numeroTempsTs' i transposar-los
matriz_Ts = (reshape(vector_Ts,numVoltatges, numeroTempsTs))';
matriz_N = (reshape(vector_N, numVoltatges, numeroTempsTs))';
matriz_p0 = (reshape(vector_p0, numVoltatges, numeroTempsTs))';
matriz_Vg = (reshape(vector_Vg, numVoltatges, numeroTempsTs))';

%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% FIGURA 4: Dependència de N amb Vg per a diferents Ts

ValoresTs = matriz_Ts(:,1); % guardem els valors de ts utilitzats

% Grafica la dependència de N amb Vg
figure;

% Paleta colors per les linies de fitting
colores = jet(numeroTempsTs);

for j = 1:(numeroTempsTs) % recorre la matriu fila per fila


    [XData, YData] = prepareCurveData(matriz_Vg(j, :), matriz_N(j, :));

    % Set up fittype and options.
    ft = fittype( 'power1' );
    opts = fitoptions( 'Method', 'NonlinearLeastSquares' );
    opts.Display = 'Off';
    opts.StartPoint = [4.2092 2.0231]; %  fitting_param (a = 4.2092 , b = 2.0231)
    % Fit model to data.
    [fitresult, gof] = fit(XData, YData, ft, opts);
    % Llegenda dades x  y
    legend_ts = ['t_s: ' num2str(ValoresTs(j,1)) ' ms'];
    % Plot data.
    scatter(XData, YData, 'o', 'filled', 'MarkerEdgeColor', colores(j, :), 'MarkerFaceColor',
colores(j, :), 'DisplayName', legend_ts);
    hold on;
    % Plot fit result
    plot(XData, fitresult(XData), 'DisplayName', 'Fitted Curve', 'Color', colores(j, :));

end

xlabel('Vg [V]');
ylabel('Número mitjà de defectes (N)');
title('Dependència de N amb Vg');
legend('show');
grid on;
hold off;

% % MODIFICAR NOM. Gravar la Figura 4 (.fig) amb el nom desitjat
% savefig('Dependencia_N_Vg.fig');


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% FIGURA 5: Dependència de N amb Ts per a diferents Vg

ValoresVg = matriz_Vg(1,:); % guardem els valors de Vg utilitzats

% Grafica la dependència de N amb Ts
figure;

% Paleta colors per les linies de fitting
colors = jet(numVoltatges);
for k = 1:(numVoltatges) % recorre la matriu fila per fila

[xData, yData] = prepareCurveData(matriz_Ts(:, k), matriz_N(:, k));

% Set up fittype and options.
```

```
ft = fittype( 'power1' );
opts = fitoptions( 'Method', 'NonlinearLeastSquares' );
opts.Display = 'Off';
opts.StartPoint = [0.755 0.2024]; %  fitting_param (a = 0.755 , b = 0.2024 )
% Fit model to data.
[fitresult, gof] = fit(xData, yData, ft, opts);
% Llegenda dades x  y
legend_vg = ['V_g: ' num2str(ValoresVg(k)) ' V'];
% Plot data
scatter(xData, yData, 'o', 'filled', 'MarkerEdgeColor', colors(k, :), 'MarkerFaceColor',
colors(k, :), 'DisplayName', legend_vg);
hold on;
% Plot fit result.
plot(xData, fitresult(xData), 'DisplayName', 'Fitted Curve', 'Color', colors(k, :));


end

% Llegenda fitting
legend('Location', 'NorthEast', 'Interpreter', 'none');
xlabel('t_s [ms]');
ylabel('Número medio de defectos (N)');
title('Dependencia de N con t_s');
grid on;
hold off;

% % MODIFICAR NOM. Gravar la Figura 5 (.fig) amb el nom desitjat
% % savefig('Dependencia_N_ts.fig');
```

ColorMap2D.m

```
% COLOR MAP 2D - Nouhaila El Bouinany

% Neteja espai
clear;
clf;
clc;
close all;

% MODIFICAR. Llista de fitxers desitjats .mat a carregar i comparar
prefix = 'CDF_RTN'; %prefix = 'CDF_RTN_Vg0p6';
fitxers = dir([prefix, '*.mat']);


fileNames = {fitxers.name};

numbers = cellfun(@(x) sscanf(x, '%*[^0-9]%d'), fileNames, 'UniformOutput', false);
numero = cellfun(@(x) x(end), numbers);
[~, order] = sort(numero);
sortedFiles = fitxers(order);


% Inicialitza una nova figura
figure;

% Inicialitza matrius per guardar dades
num_files = length(fitxers);
vector_Ts = zeros(1, num_files);
vector_p0 = zeros(1, num_files);
vector_N = zeros(1, num_files);
vector_Vg = zeros(1, num_files);

for  i = 1:length(sortedFiles)

    fitxer_actual = sortedFiles(i).name;
    [~, nomSenseExt, ~] = fileparts(fitxer_actual); % Treu extensio del fitxer

    % Carrega el fitxer .mat i extreu la matriu 'dades' amb els valors x, y de la CDF
    carrega = load(fitxer_actual);
```

```
    dades_actuals = carrega.dades;

    % Obté les variables creades a 'SaveCDFs.m'
    x = dades_actuals(:, 1);
    y = dades_actuals(:, 2);
    Ts = dades_actuals(1, 3);
    Vg = dades_actuals(1, 4);

    % valor mínim positiu i màxim negatiu
    min_x_positivo = min(x(x > 3e-9)); % 3n
    [min_y_positivo, index_positivo] = min(y(x == min_x_positivo));

    max_x_negativo = max(x(x < -3e-9));
    [min_y_negativo, index_negativo] = min(y(x == max_x_negativo));

    x2 = min_x_positivo;
    y2 = min_y_positivo;
    x1 = max_x_negativo;
    y1 = min_y_negativo;

    %% Càlcul de <N>

    % Parametres
    a = 0.878;
    b = 1.92;

    % Càlcul de L, p0
    L = log10(Ts) - log10(2e-3);
    p0 = y2 - y1;

    % Fórmula de N
    N = abs(sqrt(2 * (2 + a * L^b)) * log(p0));
%%
    % Guarda valors de Ts, N, p0 en vectors
    vector_Ts(i) = Ts;
    vector_p0(i) = p0;
    vector_N(i) = N;
    vector_Vg(i) = Vg;
end

% crea matriu dels vectors
[X, Y] = meshgrid(unique(vector_Ts), unique(vector_Vg));
Z = griddata(vector_Ts, vector_Vg, vector_N, X, Y);

% Degradat de blau a vermell
colormap(jet);

% Mapa de color amb degradat
numLevels = 100;
contourf(X, Y, Z, numLevels, 'LineStyle', 'none');
colormap(turbo);

xlabel('t_s [ms]');
ylabel('Vg [V]');
title('Mapa de color 2D: Evolució de N en funció de Ts i Vg');

% Ordena colorbar
c = colorbar;
clim([min(vector_N), max(vector_N)]); % Ajusta el rang de colors

% Etiqueta colorbar
ylabel(c, 'N', 'Rotation', 2, 'HorizontalAlignment', 'right', 'FontSize',12);


axis tight;
axis square;
```

ColorMap3D.m

```
% COLOR MAP 3D - Nouhaila El Bouinany

% Neteja espai
clear;
clf;
clc;
close all;

% MODIFICAR. Llista de fitxers desitjats .mat a carregar i comparar
prefix = 'CDF_RTN'; %prefix = 'CDF_RTN_Vg0p6';
fitxers = dir([prefix, '*.mat']);

fileNames = {fitxers.name};

numbers = cellfun(@(x) sscanf(x, '%*[^0-9]%d'), fileNames, 'UniformOutput', false);
numero = cellfun(@(x) x(end), numbers);
[~, order] = sort(numero);
sortedFiles = fitxers(order);

% Inicialitza una nova figura en 3D
figure;

% Inicialitza matrius per guardar dades
num_files = length(fitxers);
vector_Ts = zeros(1, num_files);
vector_p0 = zeros(1, num_files);
vector_N = zeros(1, num_files);
vector_Vg = zeros(1, num_files);

for i = 1:length(sortedFiles)
    fitxer_actual = sortedFiles(i).name;
    [~, nomSenseExt, ~] = fileparts(fitxer_actual); % Treu extensio del fitxer

    % Carrega el fitxer .mat i extreu la matriu 'dades' amb els valors x, y de la CDF
    carrega = load(fitxer_actual);
    dades_actuals = carrega.dades;

    % Obté les variables creades a 'SaveCDFs.m'
    x = dades_actuals(:, 1);
    y = dades_actuals(:, 2);
    Ts = dades_actuals(1, 3);
    Vg = dades_actuals(1, 4);

    % valor mínim positiu i màxim negatiu
    min_x_positivo = min(x(x > 3e-9)); % 3n
    [min_y_positivo, index_positivo] = min(y(x == min_x_positivo));

    max_x_negativo = max(x(x < -3e-9));
    [min_y_negativo, index_negativo] = min(y(x == max_x_negativo));

    x2 = min_x_positivo;
    y2 = min_y_positivo;
    x1 = max_x_negativo;
    y1 = min_y_negativo;

    %% Càlcul de <N>

    % Parametres
    a = 0.878;
    b = 1.92;

    % Càlcul de L, p0
    L = log10(Ts) - log10(2e-3);
    p0 = y2 - y1;

    % Fórmula de N
    N = abs(sqrt(2 * (2 + a * L^b)) * log(p0));
```

```
    % Guarda valors de Ts, N, p0 en vectors
    vector_Ts(i) = Ts;
    vector_p0(i) = p0;
    vector_N(i) = N;
    vector_Vg(i) = Vg;
end

% Crea matriu dels vectors
[X, Y] = meshgrid(unique(vector_Ts), unique(vector_Vg));
Z = griddata(vector_Ts, vector_Vg, vector_N, X, Y);

% Degradat de blau a vermell
colormap(jet);

% Gràfica 3D
surf(X, Y, Z, 'EdgeColor', 'none', 'FaceColor', 'interp');

xlabel('t_s [ms]');
ylabel('Vg [V]');
zlabel('Número mitjà de defectes (N)');
title('Mapa de color 3D: Evolució de N en funció de Ts i Vg');

% Ordena colorbar
c = colorbar;
clim([min(vector_N), max(vector_N)]); % Ajusta el rang de colors

% Etiqueta colorbar
ylabel(c, 'N', 'Rotation', 2, 'HorizontalAlignment', 'right', 'FontSize', 12);

view(3);  % Vista en 3D
```