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TREBALL DE FI DE GRAU

GRAU EN ENGINYERIA ELECTRÒNICA DE TELECOMUNICACIÓ

SER-DES HIGH SPEED COMMUNICATION DRIVER FOR GF22NM

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Abstract

This Bachelor's Thesis presents the design and circuit-level verification of a high-speed SerDes transmitter driver implemented in GF22nm FD-SOI technology. The proposed architecture is based on a differential Push-Pull Current-Mode Logic (PPCML) output stage combined with a configurable three-tap feed-forward equalizer. The transmitter also includes the required biasing circuits, 0.8 V to 1.8 V level shifters, common-mode feedback, modified TSPC flip-flops, and power-down control.

The circuit was designed and simulated using the Cadence environment and GF22nm device models. Transient simulations verified the correct operation and synchronization of the control logic, voltage-domain interfaces, and differential output stage. Eye diagrams were evaluated at data rates between 1 Gb/s and 10 Gb/s, showing the expected reduction in signal amplitude and eye opening as the data rate increased. The configurable de-emphasis function was also verified directly at the transmitter output, confirming the correct combination of the main cursor and post-cursor branches.

The results demonstrate the functional feasibility of the proposed architecture under nominal pre-layout conditions. Further work should include layout implementation, post-layout verification, variability analysis, and optimization of the equalization coefficients for representative transmission channels.

Resum

Aquest Treball de Fi de Grau presenta el disseny i la verificació a nivell de circuit d'un driver de transmissió d'alta velocitat per a un sistema SerDes, implementat amb tecnologia GF22nm FD-SOI. L'arquitectura proposada es basa en una etapa de sortida diferencial Push-Pull Current-Mode Logic (PPCML) combinada amb un equalitzador feed-forward configurable de tres taps. El transmissor també incorpora els circuits de polarització necessaris, convertidors de nivell de 0.8 V a 1.8 V, realimentació de mode comú, biestables TSPC modificats i control d'apagada.

El circuit s'ha dissenyat i simulat mitjançant l'entorn Cadence i els models de dispositiu GF22nm. Les simulacions transitòries han permès verificar el funcionament i la sincronització de la lògica de control, les interfícies entre dominis de tensió i l'etapa de sortida diferencial. També s'han analitzat diagrames d'ull per a velocitats compreses entre 1 Gb/s i 10 Gb/s, observant-se la reducció esperada de l'amplitud i de l'obertura de l'ull en augmentar la velocitat. La funció de de-emphasis configurable també s'ha verificat directament a la sortida del transmissor.

Els resultats demostren la viabilitat funcional de l'arquitectura en condicions nominals pre-layout. Com a treball futur, caldria realitzar el layout, les simulacions post-layout, l'anàlisi de variabilitat i l'optimització dels coeficients d'equalització per a canals representatius.

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Chapter 1

Introduction

The continuous growth in data throughput requirements in modern electronic systems has increased the demand for high-speed and efficient communication interfaces. In this context, serial communication links have become a key solution, since they allow the transmission of large amounts of data while reducing the number of physical interconnections, routing complexity, and area requirements.

Among these interfaces, Serializer/Deserializer (SerDes) architectures are widely used in integrated circuits and high-performance electronic systems. A SerDes system converts parallel data into a high-speed serial stream for transmission and reconstructs the original information at the receiver side. This approach is especially useful in applications where bandwidth, compact integration, and signal integrity are critical design constraints.

Within a SerDes transmitter, the output driver is one of the most important building blocks. Its function is to deliver the electrical signal to the communication channel with the required voltage and current levels while maintaining proper timing performance. As a result, the driver has a direct impact on key parameters such as signal integrity, power consumption, switching speed, and overall link reliability. Designing a high-speed driver therefore represents an important challenge in modern microelectronic design.

This Bachelor's Thesis focuses on the design of a high-speed communication driver for a SerDes application in GF22nm FD-SOI technology, using the Cadence design environment. The work includes the study of the circuit requirements, the design and implementation of the driver, and its validation through simulation. Special attention is given to the behavior of the circuit under high-speed operating conditions and to the trade-offs between performance, robustness, and power consumption.

1.1 Motivation

The relevance of high-speed serial links can also be understood from the strong increase in data rates achieved by modern communication standards over the last decades. Interfaces such as USB, PCIe, and Ethernet have continuously evolved towards higher throughput in order to meet the demands of data-intensive electronic systems. This trend highlights the need for efficient circuit techniques capable of supporting high-speed operation.

As data rates continue to increase, the design of the transmitter becomes more challenging, since the output stage must deliver the signal with sufficient speed and amplitude while preserving signal integrity and limiting power consumption. In this context, the transmission driver plays a key role, as its performance directly affects timing behavior, output waveform quality, and overall link reliability. Therefore, the design of high-speed driver circuits has become an important topic in modern microelectronic systems.

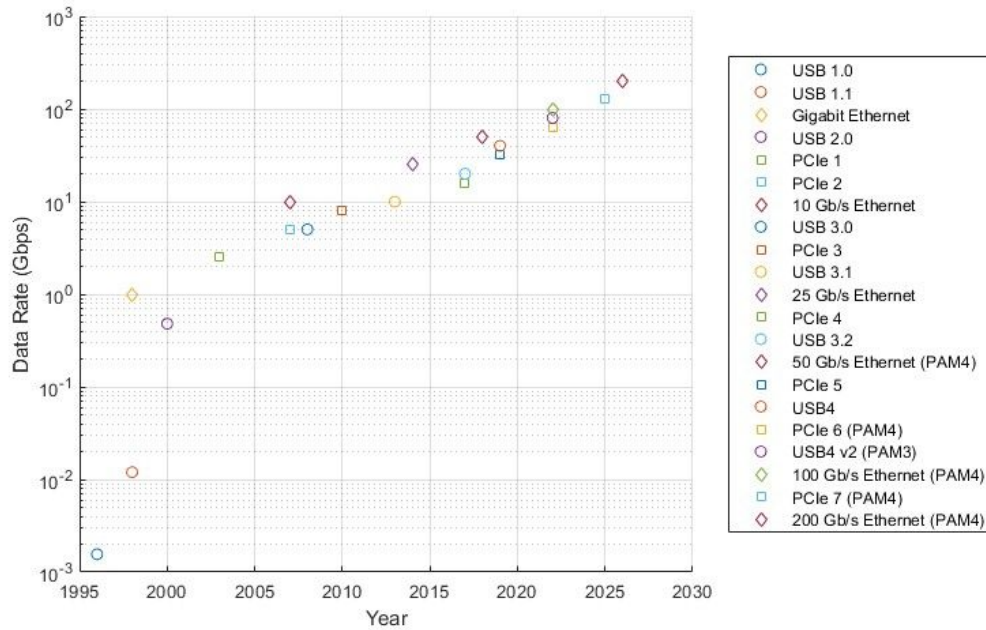


Figure 1.1: Evolution of data rates in representative communication standards over time [1].

1.2 Problem Statement

In high-speed SerDes links, the output driver is a critical block, since it is responsible for delivering the transmitted signal to the communication channel with the required amplitude, timing accuracy, and robustness. As operating speeds increase, the design of this stage becomes more challenging, because the driver must preserve signal integrity while meeting strict constraints in terms of power consumption, switching speed, and voltage headroom.

In addition, the implementation of the driver in GF22nm FD-SOI technology introduces further design considerations related to device operation, biasing conditions, and the coexistence of different voltage domains. As a result, the development of a suitable high-speed transmission driver requires careful circuit design in order to achieve reliable operation under demanding performance conditions.

1.3 Objectives

The main objective of this Bachelor's Thesis is to design and validate a high-speed communication driver for a SerDes application in GF22nm FD-SOI technology using the Cadence design environment.

To achieve this goal, the following specific objectives are defined:

- To review the fundamentals of high-speed serial communication and the role of transmitter drivers in SerDes systems.
- To identify the main design requirements and constraints of a high-speed transmission driver.
- To design the main circuit blocks required for the proposed implementation, including the output driver and its supporting stages.
- To verify the correct operation of the designed circuits through simulation in Cadence.
- To evaluate the behavior of the proposed implementation under representative high-speed operating conditions.
- To analyze the obtained results and discuss possible improvements or future extensions of the design.

1.4 Thesis Organization

The remainder of this thesis is structured as follows:

- Chapter 2 presents the theoretical background related to high-speed serial links, including an overview of SerDes architectures, the role of the transmitter, the main signal integrity metrics, and a brief introduction to FD-SOI technology.
- Chapter 3 describes the design of the proposed transmission driver, including the main circuit blocks and the design considerations taken into account during its development.
- Chapter 4 discusses the verification methodology and presents the simulation results obtained for the proposed implementation.
- Chapter 5 summarizes the main conclusions of this work and outlines possible directions for future improvement.

Finally, the bibliography is included at the end of the document.

Chapter 2

Fundamentals of High-Speed Ser-Des and Technology Background

This chapter presents the theoretical background required to understand the design of the proposed high-speed transmission driver. First, an overview of SerDes architecture is provided, with special attention to the role of the transmitter and the output driver in high-speed serial links. Then, the main performance metrics used to characterize SerDes systems are introduced, including inter-symbol interference (ISI), jitter and eye diagram analysis. In addition, a brief overview of FD-SOI technology is presented, since the proposed circuit has been implemented in this technology node. These concepts are essential for evaluating signal integrity and link reliability, and they provide the basis for understanding the design choices discussed in the following chapter.

2.1 Overview of Ser-Des Architecture

A typical SerDes link consists of two main subsystems: the transmitter (TX) and the receiver (RX), connected through a physical channel. Figure 2.1 shows a simplified block diagram of a full-duplex SerDes architecture.

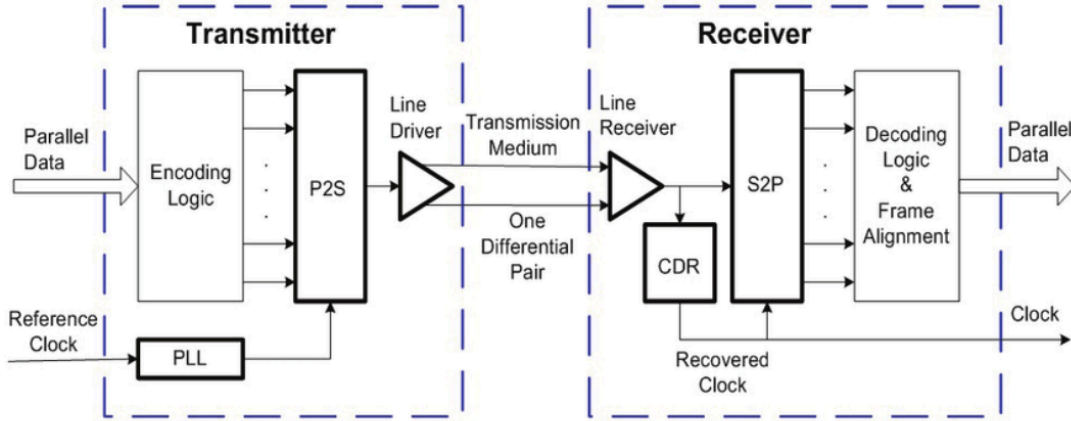


Figure 2.1: Simplified block diagram of a SerDes link, showing the transmitter side (encoding logic, PLL, P2S converter, and line driver) and the receiver side (line receiver, CDR, S2P converter, and decoding logic), connected through a differential transmission medium [2].

On the transmitter side, the parallel input data is serialized by a Parallel-to-Serial (P2S) converter, which combines multiple low-speed data lanes into a single high-speed stream. A Phase-Locked Loop (PLL) generates the high-frequency clock required for serialization and ensures proper timing alignment. Optionally, a feed-forward equalizer (FFE) may be applied at the transmitter side to compensate for the high-frequency losses introduced by the channel [3, pp. 12–14]. Finally, the output driver delivers the signal to the channel with the required voltage swing, output impedance, and timing accuracy.

The physical channel introduces frequency-dependent attenuation, dispersion, and reflections that degrade the transmitted signal. Its behavior is typically characterized through its insertion loss and return loss profiles, which determine the effective channel bandwidth and the degree of inter-symbol interference at the receiver input.

On the receiver side, a continuous-time linear equalizer (CTLE) or a decision-feedback equalizer (DFE) compensates for the distortion introduced by the channel. A Clock and Data Recovery (CDR) circuit extracts the embedded clock from the incoming data stream and uses it to sample the received bits at the optimal time instant. Finally, a Serial-to-Parallel (S2P) converter reconstructs the original parallel data.

In high-speed SerDes links, differential signaling is commonly adopted throughout the signal path. By transmitting complementary signals over a pair of conductors, differential links provide inherent rejection of common-mode noise and supply-induced disturbances, which is essential for maintaining signal integrity at multi-gigabit data rates. The output driver designed in this work follows this approach, generating a differential output signal as described in Chapter 3.

2.2 Signal Integrity and Performance Metrics in SerDes Links

2.2.1 Jitter

Jitter refers to the deviation of signal transitions from their ideal time positions. In a high-speed communication link, excessive jitter reduces the available timing margin at the receiver and may lead to incorrect data sampling. In general, jitter can be classified into random jitter, which is caused by noise-related stochastic effects, and deterministic jitter [2], which is associated with bounded and often repeatable sources such as duty-cycle distortion, inter-symbol interference, or supply-related disturbances. As data rates increase, jitter becomes one of the main limiting factors in reliable serial communication.

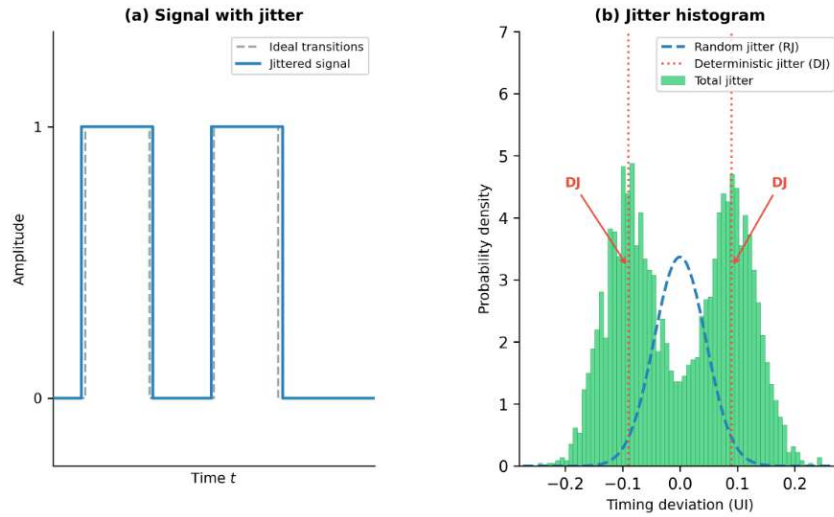


Figure 2.2: Illustration of jitter in a high-speed serial link. (a) Time-domain signal showing the deviation of the actual transitions with respect to their ideal positions. (b) Jitter histogram showing the contributions of random jitter (RJ) and deterministic jitter (DJ).

2.2.2 Inter-Symbol Interference

Inter-symbol interference (ISI) is a form of signal distortion in which the energy associated with a transmitted symbol spreads into adjacent symbol periods, causing them to interfere with one another at the sampling instant. In high-speed serial links, ISI is one of the most significant impairments limiting reliable data transmission.

The primary cause of ISI in SerDes channels is the frequency-dependent attenuation of the transmission medium. Copper-based channels, such as PCB traces or cables, exhibit losses that

increase with frequency due to the skin effect [4, pp. 58–63]. As a result, the channel behaves as a low-pass filter, attenuating the high-frequency components of the transmitted signal more than the low-frequency ones. In the time domain, this frequency selectivity causes each transmitted pulse to spread beyond its nominal bit period, overlapping with neighboring symbols.

The impact of ISI becomes more severe as the data rate increases, since higher signaling speeds require wider channel bandwidth, which in turn implies greater high-frequency attenuation. At multi-gigabit data rates, ISI can significantly reduce both the voltage margin and the timing margin of the received signal, leading to a partially or fully closed eye diagram.

To mitigate the effects of ISI, equalization techniques are commonly employed at both ends of the link. On the transmitter side, pre-emphasis or feed-forward equalization (FFE) boosts the high-frequency content of the signal before transmission [3, pp. 15–17], partially compensating for the expected channel losses. Although receiver-side equalization techniques such as CTLE and DFE also exist, they are outside the scope of this work.

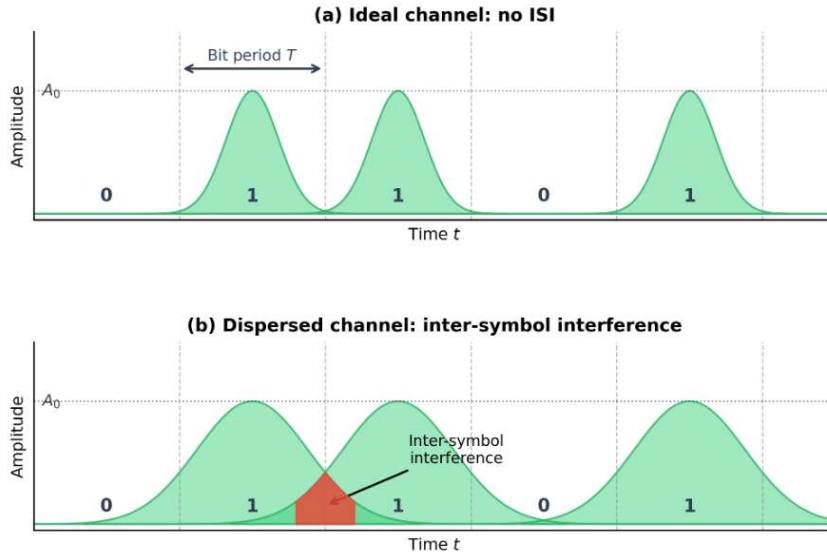


Figure 2.3: Illustration of inter-symbol interference in a high-speed serial link. (a) Ideal channel: pulses remain confined within their bit period. (b) Dispersed channel: pulse spreading causes energy overlap between adjacent symbols.

2.2.3 Eye Diagram

Another widely used tool for Ser-Des characterization is the eye diagram. An eye diagram is obtained by superimposing multiple unit intervals of the transmitted signal, allowing a visual evaluation of signal integrity. The resulting eye opening provides information about the quality of the link in both voltage and time domains. In particular, the eye height is related to the

voltage margin and noise tolerance, while the eye width is associated with the available timing margin and the effects of jitter. A well-opened eye generally indicates a robust signal with good transmission quality, whereas a closed eye suggests increased distortion, noise, or timing uncertainty.

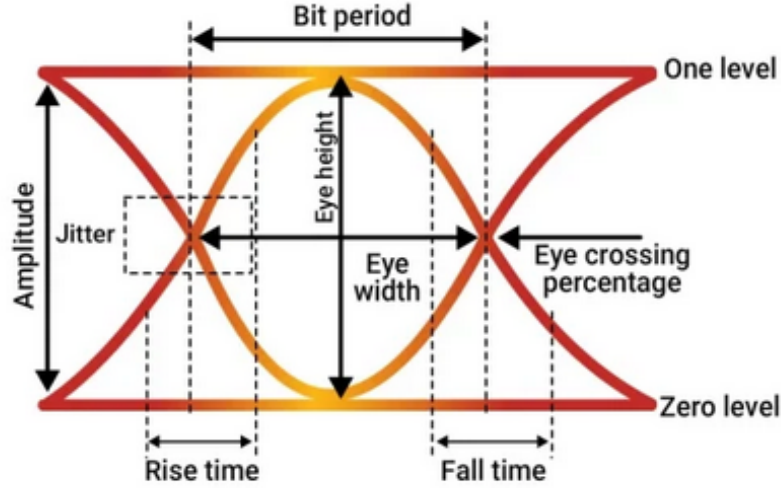


Figure 2.4: Eye diagram illustrating the main signal integrity metrics: eye height, eye width, jitter, rise time, fall time, and eye crossing percentage [5].

2.3 Overview of FD-SOI Technology

FD-SOI (Fully Depleted Silicon-on-Insulator) is a planar CMOS technology in which a very thin silicon film is placed on top of a buried oxide (BOX) layer, so that the transistor channel is fully depleted [6]. Unlike conventional bulk CMOS, this structure improves electrostatic control, reduces leakage, and helps reduce short-channel effects [7]. These features make FD-SOI attractive for high-speed and low-power integrated circuits.

A distinctive feature of FD-SOI is its body-biasing capability, which allows the threshold voltage to be modulated through a back-gate voltage [6]. This provides extra flexibility to optimize the trade-off between speed and power consumption. In the context of this work, GF22nm FD-SOI provides the transistor speed required for multi-gigabit serial communication, as well as the availability of both 0.8 V and 1.8 V devices within the same process, which is a key aspect of the proposed transmitter architecture as discussed in Chapter 3.

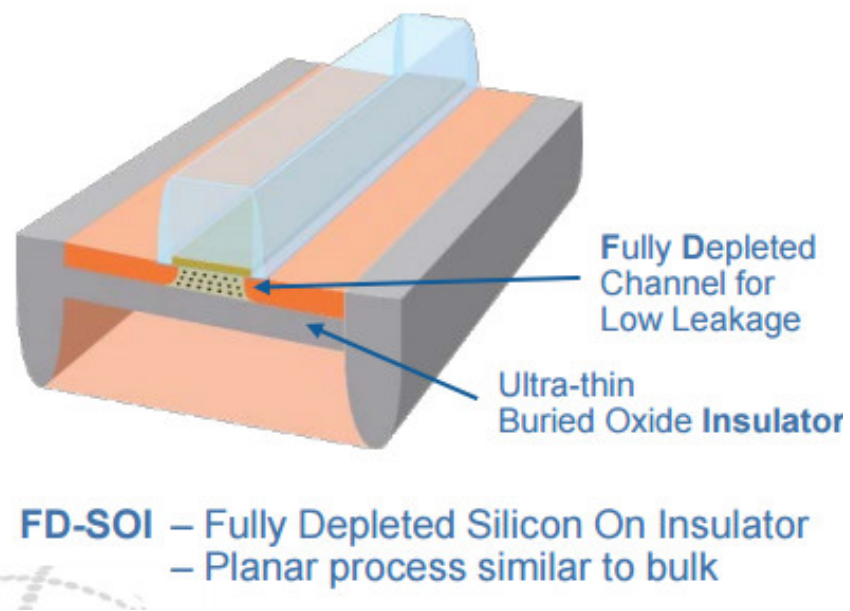


Figure 2.5: Cross-sectional view of an FD-SOI transistor structure, showing the fully depleted channel and the buried oxide layer. Adapted from [8].

Chapter 3

Circuit Design

This chapter presents the circuit design of the proposed high-speed transmitter and describes the function of its main building blocks. First, the global architecture and the interaction between the different voltage domains are introduced. The biasing network, PPCML output driver, level shifters, common-mode feedback circuit, and control logic are then analyzed individually. Finally, the configurable feed-forward equalization and power-down strategies implemented in the transmitter are discussed.

3.1 Overview of the architecture

The global block diagram of the proposed transmitter is depicted in Figure 3.1. The architecture is composed of five main functional blocks:

1. A **biasing circuit**, which generates the current references required by the different functional blocks, as described in Section 3.2.
2. Three parallel **Push-Pull Current Mode Logic (PPCML) drivers**, each biased with a different current level (6 mA, 1.2 mA, and 0.5 mA), implementing a three-tap feed-forward equalizer at the transmitter side to compensate for the high-frequency losses introduced by the channel, as explained in Section 3.3.
3. A **level shifter (LS)**, which translates the control signals from the 0.8 V domain to the 1.8 V domain required by the output stage, ensuring correct signal levels at the driver inputs, as described in Section 3.4.
4. A **common-mode feedback (CMFB) circuit**, which regulates the output common-mode voltage and helps keep the current-source transistors in the intended operating region, as presented in Section 3.5.

5. The **de-emphasis control logic**, which generates the control signals required to implement the de-emphasis function. It operates in the 0.8 V domain and consists of a multiplexer and a set of flip-flops that produce the appropriate combinations of the present and delayed versions of the input data, as explained in Section 3.6.

The output of the three parallel drivers is combined and delivered to the transmission line, producing a differential output signal at V_{out}^+ and V_{out}^- .

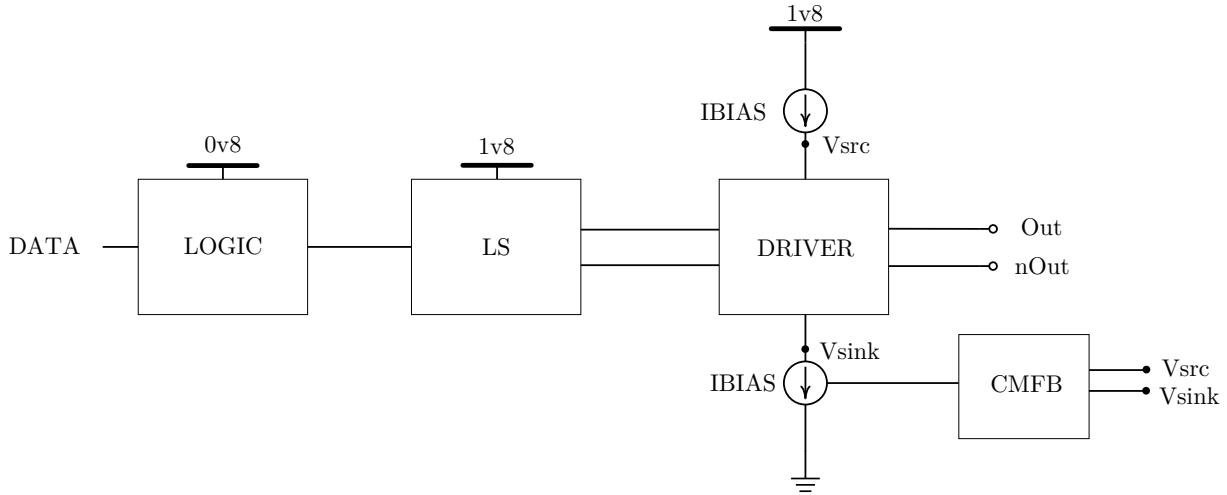


Figure 3.1: Block diagram of the proposed transmitter architecture. The blocks correspond to the de-emphasis control logic, level shifter, PPCML driver, biasing circuit, and CMFB circuit. Note that in the actual implementation, the level shifter, the PPCML driver and the CMFB circuit are replicated three times, one instance per driver tap (6 mA, 1.2 mA, and 0.5 mA).

3.2 Biasing Circuit

The biasing circuit is responsible for generating the current references required by the PPCML stages. In the proposed design, three different current levels are provided, namely 6 mA, 1.2 mA, and 0.5 mA, in order to supply the appropriate bias conditions to the different output stages. Therefore, this block plays a key role in defining the operating point and overall behavior of the driver circuitry.

The current generation is based on 0.8 V transistors, while the output branches of the current sources are implemented with 1.8 V devices. This choice is motivated by the fact that the generated currents must be delivered to the PPCML drivers, which operate in a higher-voltage domain. As a result, the use of 1.8 V transistors at the output ensures proper voltage compliance and reliable interaction with the driver stage.

The transistors of the main PPCML stage are implemented as 1.8 V devices and sized with a width-to-length ratio of $W/L = 40 \mu\text{m} / 150 \text{ nm}$. This sizing is determined by the requirement to support a bias current of 6 mA. The large transistor width is necessary to distribute the current density across a sufficiently wide channel, preventing excessive voltage drop and maintaining reliable operation at the required bias conditions.

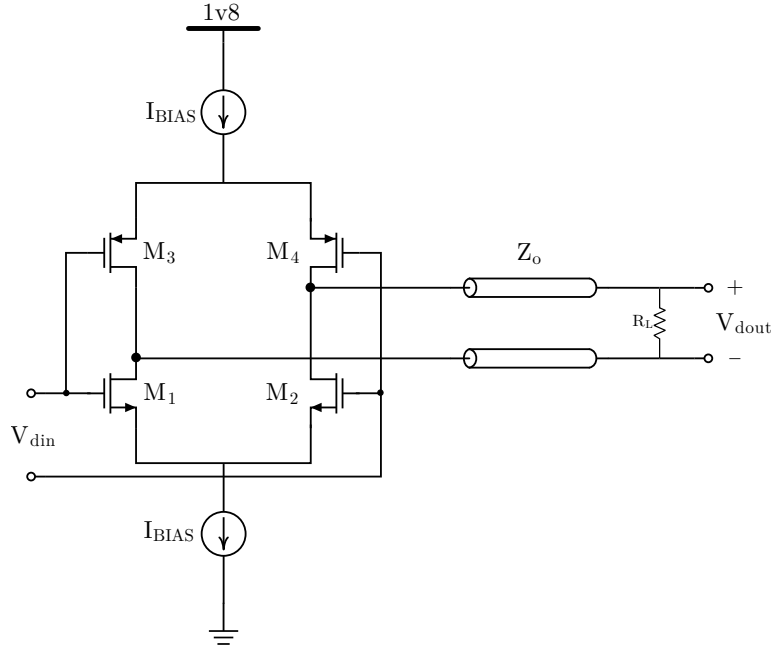


Figure 3.3: Schematic of the PPCML driver used as the differential output stage. The driver steers the bias current through the load to generate the high-speed differential output signal.

3.4 Level Shifter

The level-shifter design incorporates a cross-coupled regenerative structure. This structure is first introduced separately, followed by a description of the level-shifter architecture and operation.

3.4.1 Cross-Coupled Buffer

Cross-coupled structures are used in several parts of the proposed transmitter because they provide a regenerative effect through positive feedback. When one differential node starts to rise and the other starts to fall, the cross-coupled devices reinforce this voltage difference, accelerating the transition and improving the definition of the differential logic levels.

This regenerative behavior is especially useful in high-speed signal paths. At high operating

frequencies, the available time for each transition is limited, so slow edges can reduce timing margin and degrade signal integrity. By reinforcing the differential transition, the cross-coupled buffer helps sharpen the signal edges, improve switching speed, and provide more robust complementary outputs.

In the proposed transmitter, this principle is used in the level shifter to strengthen the voltage conversion between the 0.8 V and 1.8 V domains. The same cross-coupled structure is also employed in the differential control paths, as described later in Section 3.6.

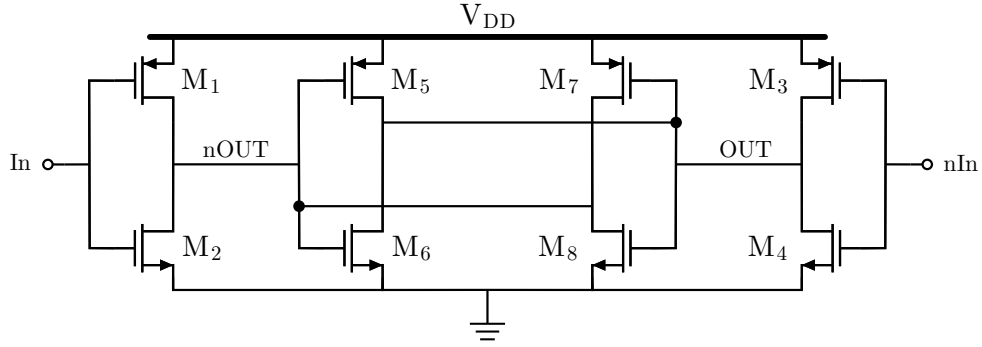


Figure 3.4: Schematic of the cross-coupled regenerative buffer.

3.4.2 Level-Shifter Architecture and Operation

The level shifter is used to translate the input control signal from the 0.8 V domain to the 1.8 V domain required by the PPCML stage. This block is necessary because the low-voltage logic signal is not sufficient to properly drive the following stage. Therefore, the level shifter acts as an interface between two voltage domains, ensuring correct logic conversion and adequate signal amplitude at the PPCML input. Its design must provide fast transitions, limited propagation delay, and reliable operation, since its performance directly affects the switching behavior of the output stage.

Figure 3.5 shows a simplified schematic of the level shifter. The core of the circuit consists of a cross-coupled PMOS pair (M3, M4), which performs the voltage translation between domains [10]. The transistors M1 and M2 act as pull-down devices driven by the input signal and its complementary version, controlling the switching of the internal nodes. The positive feedback introduced by the cross-coupled structure reinforces the transition between logic states, resulting in faster and more robust output switching.

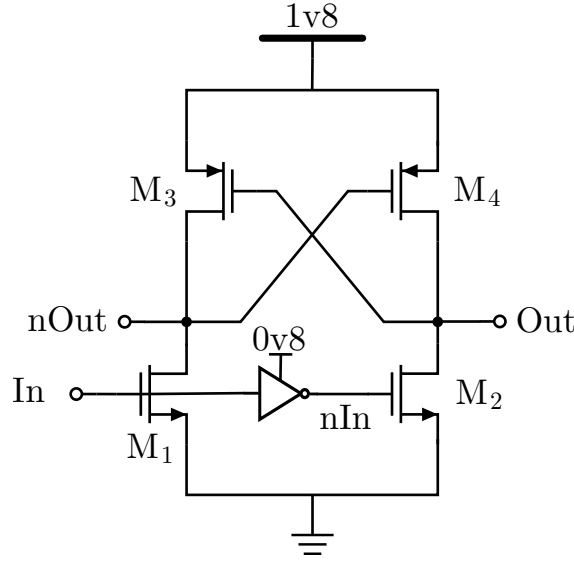


Figure 3.5: Simplified schematic of the level shifter used to translate the control signals from the 0.8 V logic domain to the 1.8 V PPCML input domain. The cross-coupled PMOS pair provides regenerative feedback to accelerate the voltage conversion.

The complete implementation is shown in Figure 3.6. Compared with the simplified schematic, the full circuit can be understood as four functional blocks: a low-voltage input stage, a regenerative cross-coupled core, a high-voltage output stage, and a dedicated bias-generation network. These additions are consistent with low-voltage level-shifter design techniques, where auxiliary devices are commonly introduced to improve transition speed and energy efficiency [11].

The low-voltage input stage, formed by M13–M16, receives the complementary input signals In and nIn in the 0.8 V domain and creates the initial imbalance between the two internal branches. This imbalance is then amplified by the regenerative core, which comprises the cross-coupled networks M9–M12 and M5–M8. These stages provide positive feedback, reinforcing the switching decision and improving the speed and robustness of the level conversion.

Finally, M1–M4 form the high-voltage output stage, generating the translated Out and $nOut$ signals in the 1.8 V domain. These full-swing outputs provide the voltage levels required to properly drive the following PPCML stage under high-speed operating conditions.

A dedicated bias-generation network is also included to define the gate voltages of M_2 and M_4 . A 10 μA current source forces current through the diode-connected transistor M_{17} , generating the common bias voltage V_{bias} . This voltage is applied to the gates of both M_2 and M_4 , since the two devices require the same bias condition. The internally generated bias voltage establishes their operating point and helps the level-shifter branches switch reliably.

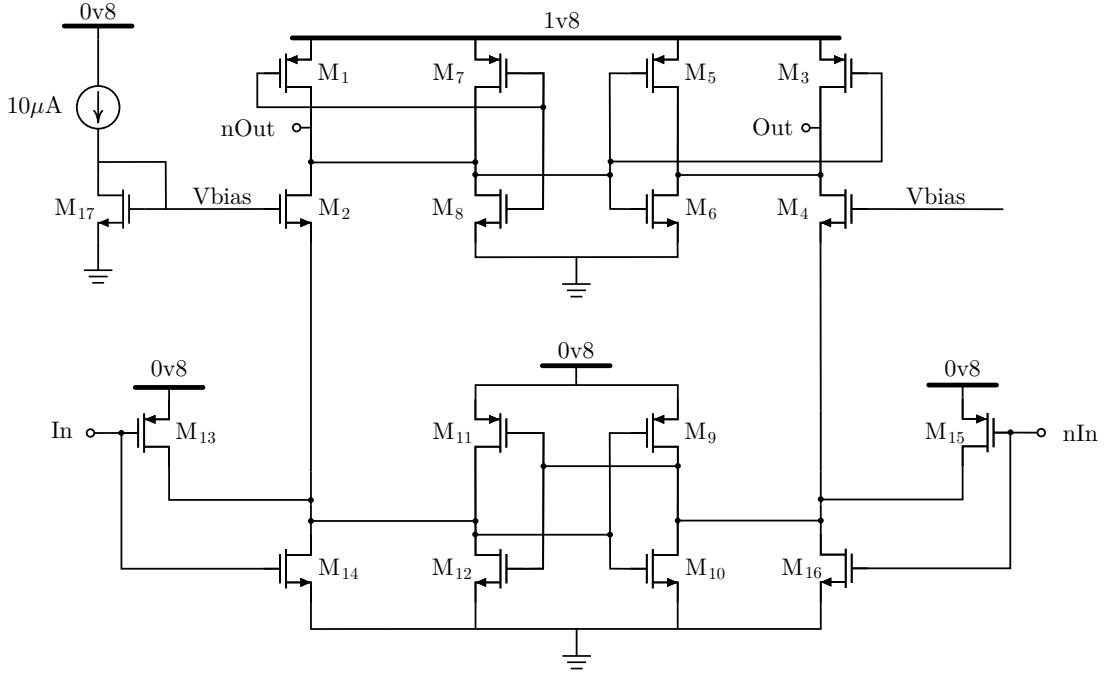


Figure 3.6: Complete schematic of the level shifter used in the proposed design, comprising 17 transistors. The circuit operates between the 0.8 V and 1.8 V voltage domains.

In addition to the high-speed level shifters used in the main data path, simpler level-shifting cells are also used for the power-down control signals. The enable signals are generated in the 0.8 V logic domain, but some of the controlled blocks operate partially or entirely in the 1.8 V domain. Therefore, these enable signals must also be translated to 1.8 V before being applied to the corresponding control transistors.

This auxiliary level-shifting function is required in the PPCML driver branches, in the level-shifter power-down circuitry, and in the CMFB operational amplifier, where the enable signal must correctly turn on or turn off devices connected to the high-voltage domain. In this way, both the high-speed data/control paths and the low-speed configuration signals are made compatible with the voltage domain of the blocks they drive.

Figure 3.5 shows the simplified level-shifter topology used to translate 0.8 V logic signals into the 1.8 V domain.

3.5 Common Mode Feedback

The common-mode feedback circuit is used to regulate the average voltage of the differential nodes and keep it close to a desired reference level. In fully differential circuits, a common-mode feedback loop is required to define and stabilize the output common-mode voltage [12]. Its main

purpose is to ensure that the current-source transistor operates in saturation, thus preserving the intended bias conditions. By controlling the common-mode level, the CMFB prevents loss of voltage headroom and helps maintain a stable current for the PPCML stage.

The common-mode voltage is sensed by averaging the two differential output nodes, Out and nOut, and comparing the result with a reference voltage. The error signal is then processed by an operational amplifier, whose output controls the gate voltage of the current-source transistors of the PPCML stage. In this way, if the common-mode voltage deviates from the desired reference level, the CMFB circuit adjusts the bias current accordingly to restore the correct operating point.

The operational amplifier used in the CMFB circuit is shown in Figure 3.7. It operates between the 0.8 V and 1.8 V domains and is biased with a current of $10\ \mu\text{A}$. The amplifier provides sufficient gain to ensure accurate common-mode regulation while maintaining stability under the high-speed operating conditions of the PPCML stage.

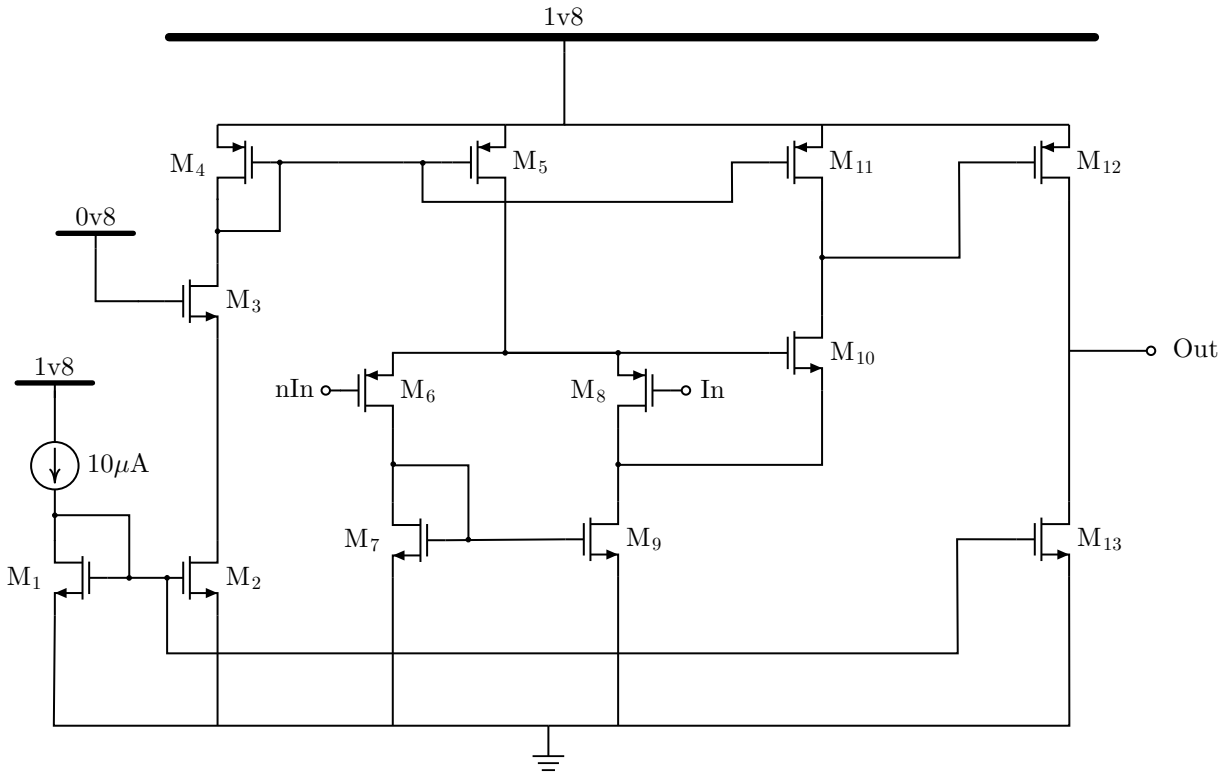


Figure 3.7: Schematic of the operational amplifier used in the common-mode feedback circuit, comprising 13 transistors. The circuit operates between the 0.8 V and 1.8 V voltage domains, with a bias current of $10\ \mu\text{A}$.

The node between M8 and M9 acts as an intermediate high-impedance node of the first gain

stage. Variations in the input signal modify the current flowing through M8, while M9 provides the corresponding active-load/current-mirror action. As a result, the current imbalance at this node is converted into a voltage variation. In small-signal terms, the voltage gain at this node is limited by the finite output conductance of M8 and M9, g_{ds8} and g_{ds9} , which define the effective output resistance of the node.

This voltage variation is applied to the source of M_{10} , which operates approximately as a common-gate stage. The resulting variation in drain current is transferred to the node shared by M_{10} and M_{11} .

Transistor M_{11} provides the DC bias current for this branch and, in small-signal operation, contributes through its finite output resistance. Therefore, the current variation generated by M_{10} produces a voltage variation at the intermediate node. Its equivalent small-signal resistance can be approximated as

$$R_{o2} \simeq r_{o10} \parallel r_{o11} = \frac{1}{g_{ds10} + g_{ds11}}.$$

The M_{10} – M_{11} branch can therefore be interpreted as an intermediate gain stage that transfers the signal generated by the differential input pair towards the output stage.

Following the small-signal analysis methodology presented in [13, pp. 270–273], the low-frequency open-loop gain of the operational amplifier can be approximated by considering the circuit as a cascade of individual gain stages. For each stage, the voltage gain is estimated as the product of its effective transconductance and the equivalent small-signal resistance at the corresponding output node.

The first stage is formed by the differential input pair M_6 – M_8 and the active load M_7 – M_9 . Assuming matched input transistors, $g_{m6} \simeq g_{m8}$, their transconductance is denoted by $g_{m6,8}$. The second stage is formed by the common-gate transistor M_{10} and the PMOS bias transistor M_{11} , whose finite output resistance contributes to the equivalent small-signal resistance of the intermediate node. The output stage is formed by M_{12} and M_{13} . Therefore, the low-frequency open-loop gain can be approximated as

$$A_0 \simeq \frac{-g_{m6,8}}{g_{ds8} + g_{ds9}} \cdot \frac{g_{m10}}{g_{ds10} + g_{ds11}} \cdot \frac{-g_{m12}}{g_{ds12} + g_{ds13} + g_L},$$

where g_L represents the small-signal conductance of the load connected to the output. Equivalently,

$$A_0 \simeq \frac{g_{m6,8} g_{m10} g_{m12}}{(g_{ds8} + g_{ds9})(g_{ds10} + g_{ds11})(g_{ds12} + g_{ds13} + g_L)}.$$

This expression represents a first-order approximation that neglects body effect, parasitic capacitances, and the loading interaction between consecutive stages. Consequently, it provides an analytical estimate of the low-frequency open-loop gain of the amplifier.

The dominant small-signal poles of the amplifier are determined by the resistance and capacitance associated with its high-impedance nodes. In particular, the pole at the output node can be approximated as

$$\omega_{p,\text{out}} \simeq \frac{1}{(R_{o,\text{out}} \parallel R_L) C_{\text{out}}},$$

where

$$R_{o,\text{out}} \simeq r_{o12} \parallel r_{o13} = \frac{1}{g_{ds12} + g_{ds13}}.$$

Since the load resistance is significantly smaller than the intrinsic output resistance of the amplifier, the equivalent resistance at the output node can be approximated as

$$R_{o,\text{out}} \parallel R_L \simeq R_L.$$

Consequently,

$$\omega_{p,\text{out}} \simeq \frac{1}{R_L C_{\text{out}}}.$$

The relatively small value of R_L results in a small output-node time constant and therefore places the output pole at a high frequency. As a result, this pole introduces limited additional phase shift around the unity-gain frequency. Under these loading conditions, explicit Miller compensation is not required.

3.6 Control Logic

The control logic block generates the control signals required to drive the three parallel PPCML driver instances, each corresponding to one tap of the transmitter-side feed-forward equalizer. In order to produce the required present and delayed data versions, the logic uses modified TSPC D flip-flops with input selectors. These cells provide both synchronization and configurability, allowing the de-emphasis function to be enabled or disabled depending on the selected operating mode.

3.6.1 Modified TSPC D Flip-Flop with Input Selector

In order to generate the control signals required by the three-tap de-emphasis scheme, the control logic must provide both the present data sample and delayed versions of it. These delayed signals are used to drive the post-cursor taps of the transmitter-side feed-forward equalizer. For this purpose, the logic employs a modified D flip-flop based on true single-phase clocking (TSPC).

TSPC flip-flops are dynamic sequential circuits that operate with a single clock phase, avoiding the need for complementary clock signals [14]. This feature simplifies the clock distribution network and makes the topology attractive for high-speed timing paths. In the proposed cell, a 2:1 input-selection network is integrated with the first dynamic stage of the flip-flop, allowing one of two candidate input signals to be selected before the clocked sampling operation. During the following clock period, the selected value is available at the output as a synchronized data version.

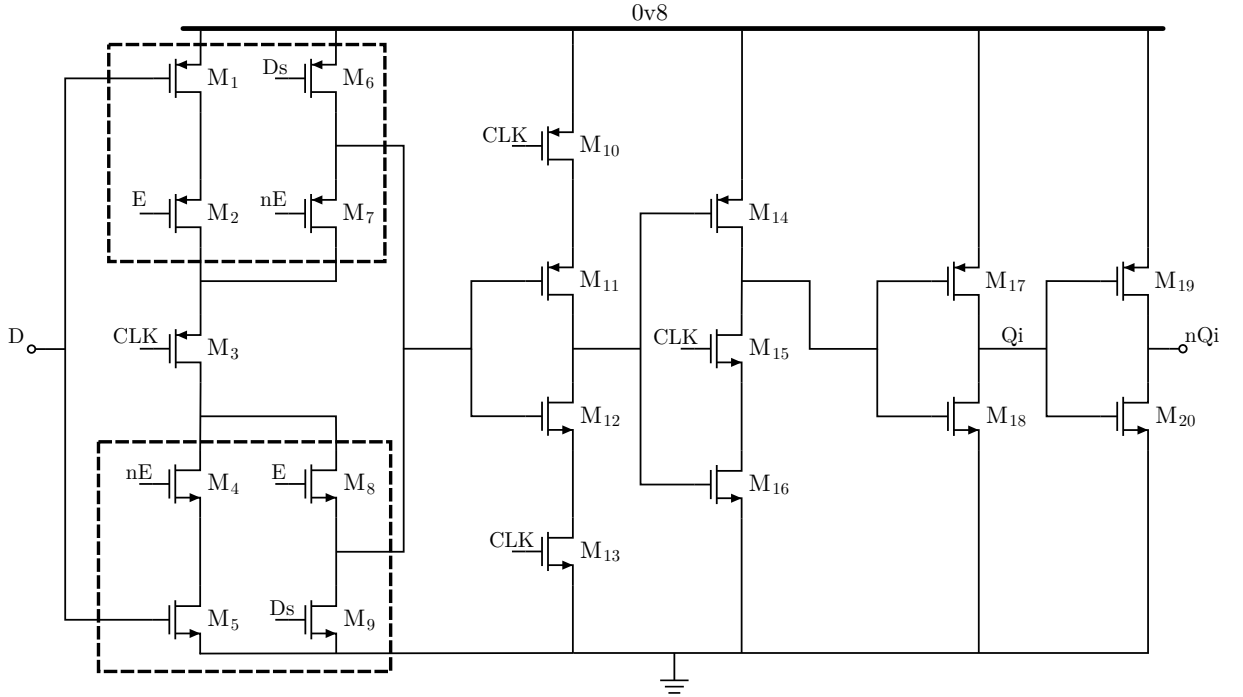


Figure 3.8: Rising-edge modified TSPC D flip-flop with integrated 2:1 input selector used in the de-emphasis control logic. The dashed boxes indicate the input-selection network, while the internal outputs Q_i and nQ_i are later applied to a cross-coupled buffer to generate the final Q and nQ signals.

In the schematic, the dashed boxes highlight the input-selection network controlled by E and nE , while D_s denotes the selected data signal applied to the TSPC sampling core. It should

be noted that the selector is not implemented as an isolated purely combinational multiplexer, but is integrated with the first dynamic stage of the flip-flop. The clock-controlled transistor M3 belongs to the sequential sampling path and determines when the selected input data is captured.

The signals Q_i and nQ_i correspond to the internal complementary outputs of the flip-flop cell. These signals are subsequently applied to a cross-coupled buffer, which strengthens the differential levels and generates the final Q and nQ control signals. For clarity and due to space limitations, the cross-coupled buffer is not included in the flip-flop schematic and is instead described separately in Section 3.4.1.

To support high-speed operation, the control logic uses a chain of flip-flops triggered alternately on the rising and falling edges of the clock. This interleaved structure allows consecutive data samples to be processed using opposite clock transitions, reducing the timing burden of each individual stage and enabling the delayed versions required by the de-emphasis logic.

Let f_c denote the clock frequency used to define the target bit period. The corresponding unit interval is $T_{UI} = 1/f_c$. Therefore, a data stream operating at this bit rate presents one bit every T_{UI} . However, when an alternating 10101010 sequence is used for verification, the voltage waveform repeats every two bit periods. As a result, its waveform period is $T_{DATA} = 2/f_c$, corresponding to a periodic frequency of $f_c/2$. This does not mean that the data rate is reduced; it only reflects the fact that the 10101010 pattern requires two bits to repeat.

By combining rising-edge and falling-edge triggered flip-flops, the control logic can generate the required delayed and time-aligned data versions for the de-emphasis taps while preserving the target unit interval defined by f_c .

Figure 3.8 corresponds to the rising-edge version of the modified TSPC D flip-flop. The falling-edge version keeps the same general architecture, but the sampling path is modified so that the cell reacts to the opposite clock transition. In this version, M15 is implemented as a PMOS device, and the internal node between M15 and M16 drives the inverter formed by M17 and M18.

3.6.2 Feed-Forward Equalization and De-emphasis

The transmitter implements a three-tap FFE, which can be described as a finite impulse response (FIR) filter applied at the symbol level [3]. The transmitted signal $y[k]$ at time instant k is given by:

$$y[k] = c_0 \cdot x[k] + c_1 \cdot x[k - 1] + c_2 \cdot x[k - 2] \quad (3.1)$$

where $x[k]$ is the input data symbol at time k and c_n are the tap coefficients. In the proposed implementation, the magnitude of each coefficient is determined by the bias current of the corresponding PPCML driver instance, as summarized in Table 3.1. The post-cursor taps c_1 and c_2 are applied with opposite polarity with respect to the cursor tap c_0 , implementing a de-emphasis scheme in which the energy of consecutive equal symbols is reduced, thereby attenuating the low-frequency content of the transmitted signal.

Table 3.1: FFE tap assignment and corresponding driver current.

Tap	Symbol	Role	Driver current
c_0	$x[k]$	Cursor (main)	6.0 mA
c_1	$x[k - 1]$	Post-cursor 1	1.2 mA
c_2	$x[k - 2]$	Post-cursor 2	0.5 mA

It should be noted that Table 3.1 reports the magnitude of each tap contribution. The sign inversion required for de-emphasis is implemented at circuit level by applying the post-cursor taps with opposite differential polarity with respect to the main cursor tap.

The direct correspondence between the FIR formulation of Equation 3.1 and the circuit implementation is illustrated in Figure 3.9, where each tap coefficient is realized by an independent PPCML driver instance biased at the corresponding current level.

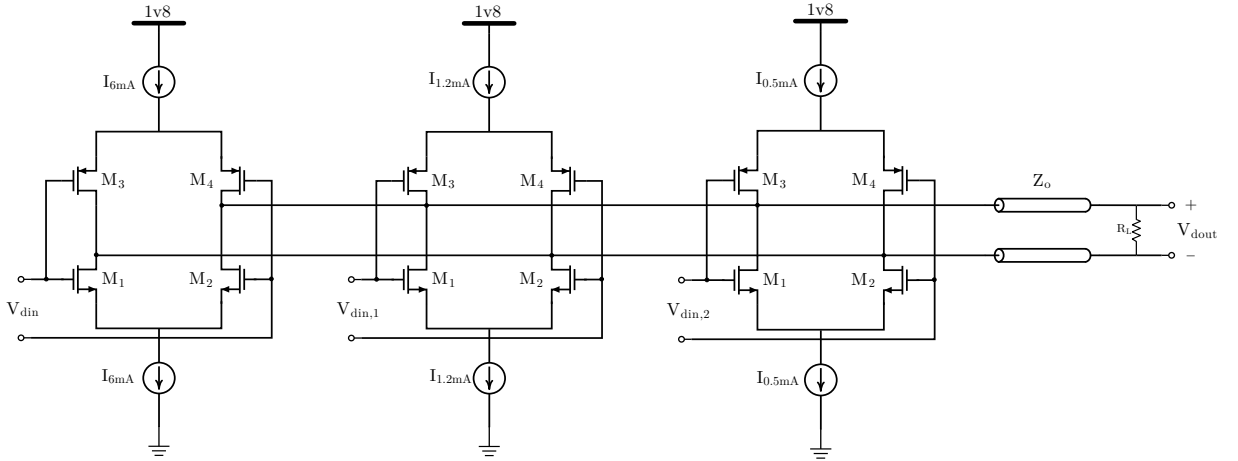


Figure 3.9: Circuit implementation of the three-tap FFE filter. Each tap is realized by an independent PPCML driver instance biased at a different current level: 6 mA for the main cursor tap c_0 , 1.2 mA for post-cursor tap c_1 , and 0.5 mA for post-cursor tap c_2 . The weighted summation of the FIR filter is implemented through the parallel combination of the three driver outputs connected to a common differential load.

3.6.3 Configurable De-emphasis

The amount of de-emphasis applied by the transmitter is not fixed, but can be configured depending on the characteristics of the transmission channel. This flexibility is motivated by the fact that the degree of signal degradation introduced by the channel depends strongly on its length and physical properties.

In the case of a short transmission line, the channel attenuation is small and the received eye diagram remains sufficiently open without equalization. Under these conditions, activating the post-cursor taps would introduce unnecessary distortion and increase power consumption. The multiplexer within the control logic therefore allows the post-cursor tap signals to be disabled, so that only the main cursor driver is active and the transmitter operates without de-emphasis.

Conversely, for a long transmission line, the frequency-dependent losses of the channel are more severe and inter-symbol interference significantly degrades signal integrity at the receiver. In this case, the post-cursor taps are enabled and the de-emphasis function is activated, allowing the transmitter to pre-compensate for the expected channel losses before transmission.

This configurable architecture makes the proposed transmitter suitable for deployment in different link environments without requiring circuit modifications, providing a practical trade-off between equalization performance and power consumption that can be adapted to the target application.

This architecture achieves a direct correspondence between the FIR filter formulation of Equation 3.1 and the physical circuit implementation: the weighted summation of tap contributions is realized through the parallel combination of three independent current-steering drivers whose outputs are connected to a common differential load.

Power-Down Strategy

The proposed transmitter includes a distributed power-down network that allows the main circuit blocks to be disabled when they are not required. This control is applied to the biasing circuit, the PPCML drivers, the level shifters, and the operational amplifier used in the common-mode feedback loop. The objective of this strategy is to reduce power consumption and avoid unnecessary switching activity in inactive operating modes.

The level shifters include power-down control in order to avoid current consumption when the associated driver branch is inactive. Similarly, the CMFB operational amplifier can be disabled by turning off its bias current when the corresponding PPCML stage is not operating. Therefore, the power-down network provides an additional degree of configurability and improves the energy efficiency of the transmitter.

In the biasing circuit, the power-down control disables the corresponding current source branches, preventing the generation of unused bias currents. In the PPCML drivers, the same principle is used to turn off the current paths associated with inactive driver taps. This is especially useful in the configurable de-emphasis architecture, where the post-cursor branches can be disabled when equalization is not required.

In addition to disabling the bias current branches, logic gating is used in the driver branches and in the level-shifter control paths. The enable signals are combined with the data/control signals by means of simple logic gates, such as AND and OR gates, so that when a branch is disabled its internal control nodes are forced to a defined inactive logic state. This prevents unnecessary transitions from propagating through inactive blocks, avoids undesired switching at the level-shifter and PPCML inputs, and further reduces the dynamic power consumption of the transmitter.

Therefore, the power-down strategy acts at two different levels. On the one hand, it suppresses the current consumption by disabling the corresponding bias branches. On the other hand, it reduces dynamic switching activity by holding the control nodes of inactive paths in a non-switching state.

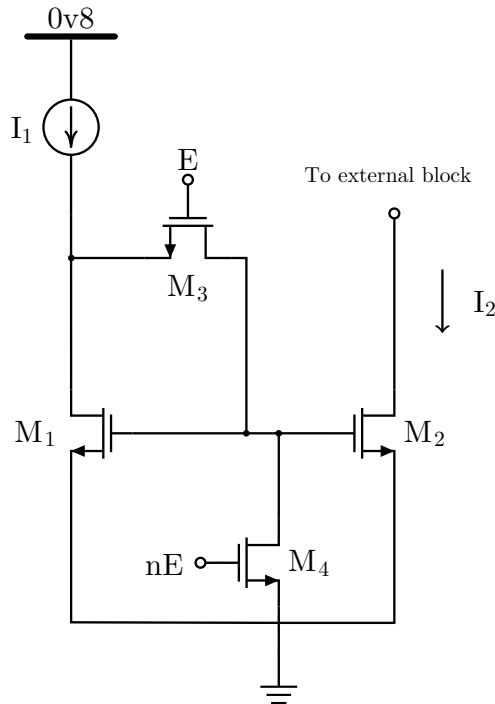


Figure 3.10: Conceptual power-down mechanism used in the bias current sources. When $E = 1$, M_3 connects the mirror bias voltage to the gate of M_2 , generating the output current I_2 . When $E = 0$, M_4 pulls the gate of M_2 to ground, preventing a floating node and disabling the output branch.

The power-down operation is controlled by the complementary signals E and nE . When the current source is enabled, $E = 1$ and $nE = 0$. In this condition, transistor M_3 connects the bias voltage generated by the reference branch to the gate of M_2 , allowing the reference current I_1 to be mirrored into the output branch and generating the bias current I_2 .

When the branch is disabled, $E = 0$ and $nE = 1$. Transistor M_3 disconnects the mirror bias node from the gate of M_2 , while M_4 pulls this gate node to ground. This prevents the gate of M_2 from remaining floating and ensures that the output transistor is fully turned off. As a result, the current I_2 delivered to the external biased block is suppressed, reducing the power consumption of the inactive branch.

Chapter 4

Verification

This chapter presents the simulation results used to verify the operation of the proposed SerDes transmitter. The objective of the verification process is to confirm the correct operation of the main circuit blocks, evaluate the high-speed behavior of the output driver, and demonstrate the effect of the configurable de-emphasis technique.

4.1 Simulation Setup

The proposed transmitter was verified in the Cadence environment with the GF22nm FD-SOI technology models. The output stage was connected to a differential load and to a transmission-line model used to evaluate the high-speed output behavior.

Different input data patterns were used depending on the objective of each simulation. First, a repetitive (10101010) sequence was applied in order to evaluate the high-frequency switching capability of the transmitter. This pattern forces a transition at every bit period and is therefore useful to observe the eye diagram degradation as the data rate increases. Second, a (111000111000) sequence was used to evaluate the effect of de-emphasis, since it contains groups of consecutive equal bits and allows the difference between the cursor and post-cursor contributions to be observed more clearly.

In order to obtain more realistic simulation conditions, the input data and clock signals are not applied directly to the transmitter as ideal voltage sources. Instead, both signals are first passed through buffer stages implemented with transistors from the same technology. This avoids applying unrealistically ideal transitions to the circuit and introduces finite rise and fall times, as well as a more representative driving capability.

The use of input buffers also isolates the ideal stimulus sources from the circuit under test and provides signal waveforms that are closer to those generated by a real digital block. Therefore,

the transient and eye-diagram simulations include the effect of non-ideal input edges at the data and clock inputs, making the verification setup more representative of practical operating conditions.

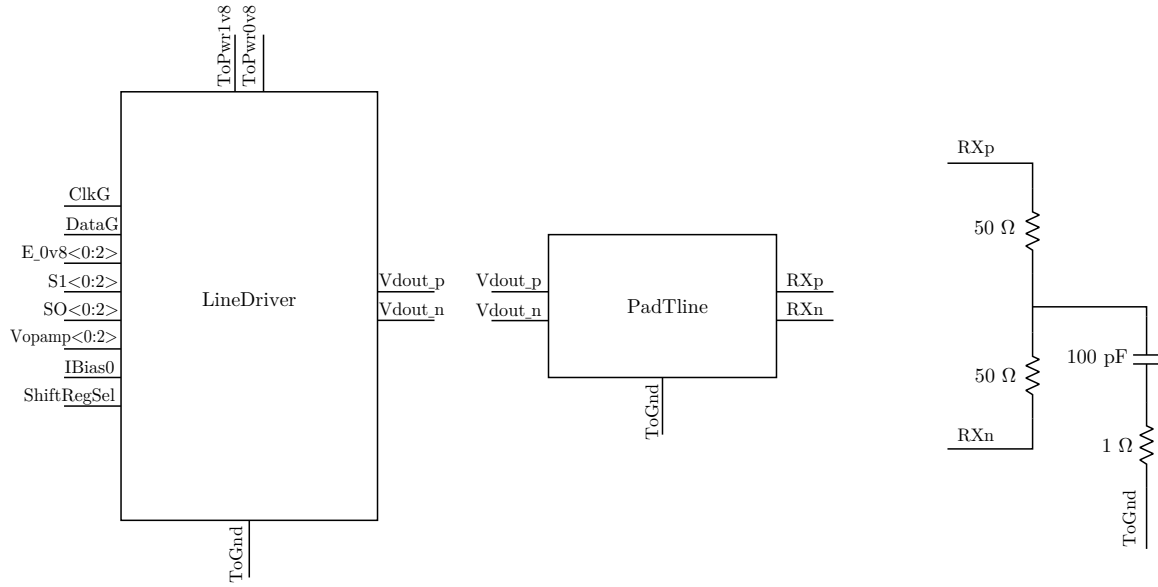


Figure 4.1: Simplified view of the top-level Cadence testbench used for transient and eye-diagram simulations. The figure shows the main signal path, including the transmitter block, channel model, and differential load; the DC supply and bias sources are defined in the simulation setup but omitted here for clarity.

4.2 Functional Verification

The first verification step consists of checking the correct propagation of the data through the different circuit blocks. The control logic generates the required present and delayed data versions, which are then translated from the 0.8 V domain to the 1.8 V domain by the level shifters. These signals drive the PPCML stages, producing a differential output voltage at the load.

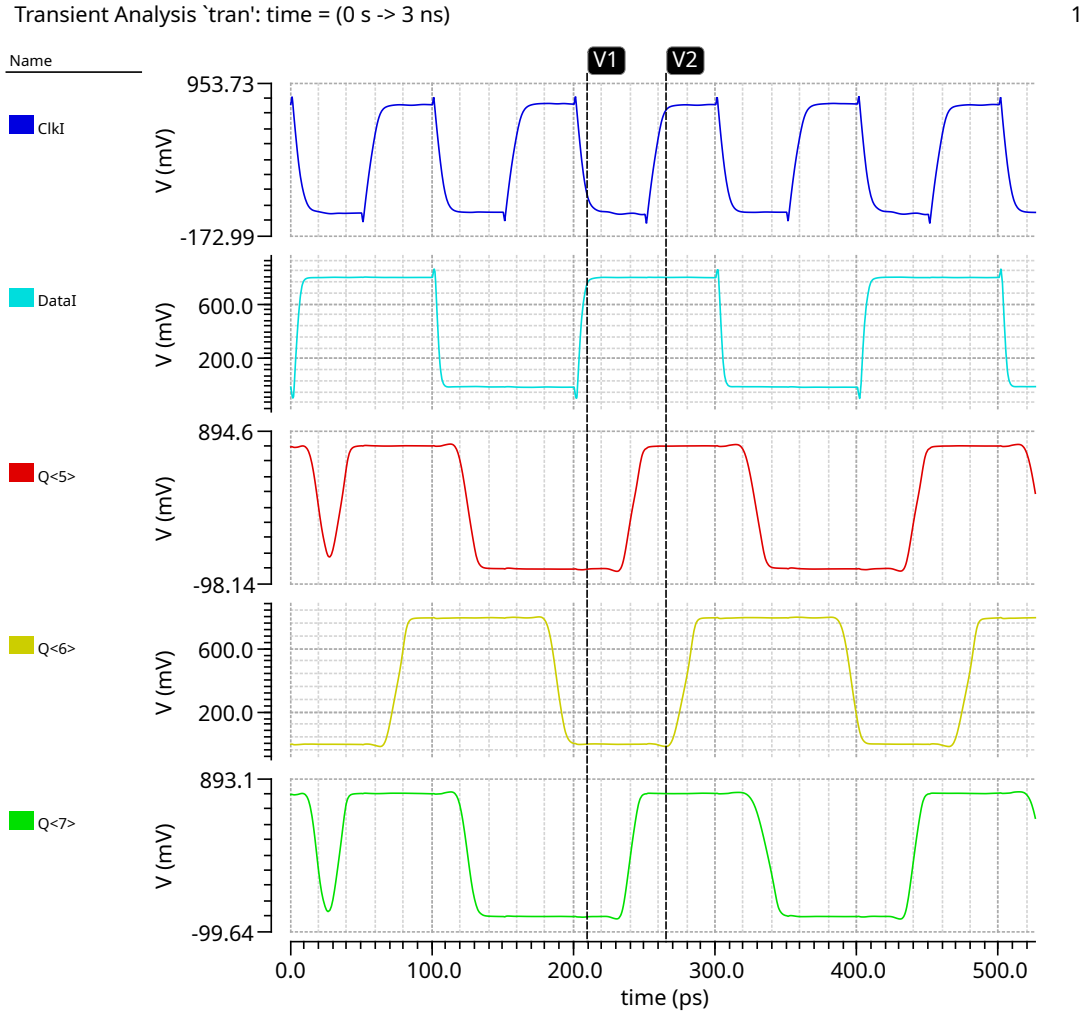


Figure 4.2: Transient response of the control-logic flip-flop chain for a 10101010 input sequence at 10 Gb/s. The signals Q_5 , Q_6 , and Q_7 correspond to consecutive delayed data versions, generated by alternating falling-edge and rising-edge triggered flip-flops. In this case, Q_5 and Q_7 are generated by falling-edge cells, while Q_6 is generated by a rising-edge cell.

The simulated waveforms confirm the correct operation of the interleaved flip-flop chain. The alternating rising-edge and falling-edge cells generate consecutive delayed versions of the input data, allowing the control logic to provide the time-aligned signals required by the three-tap de-emphasis scheme.

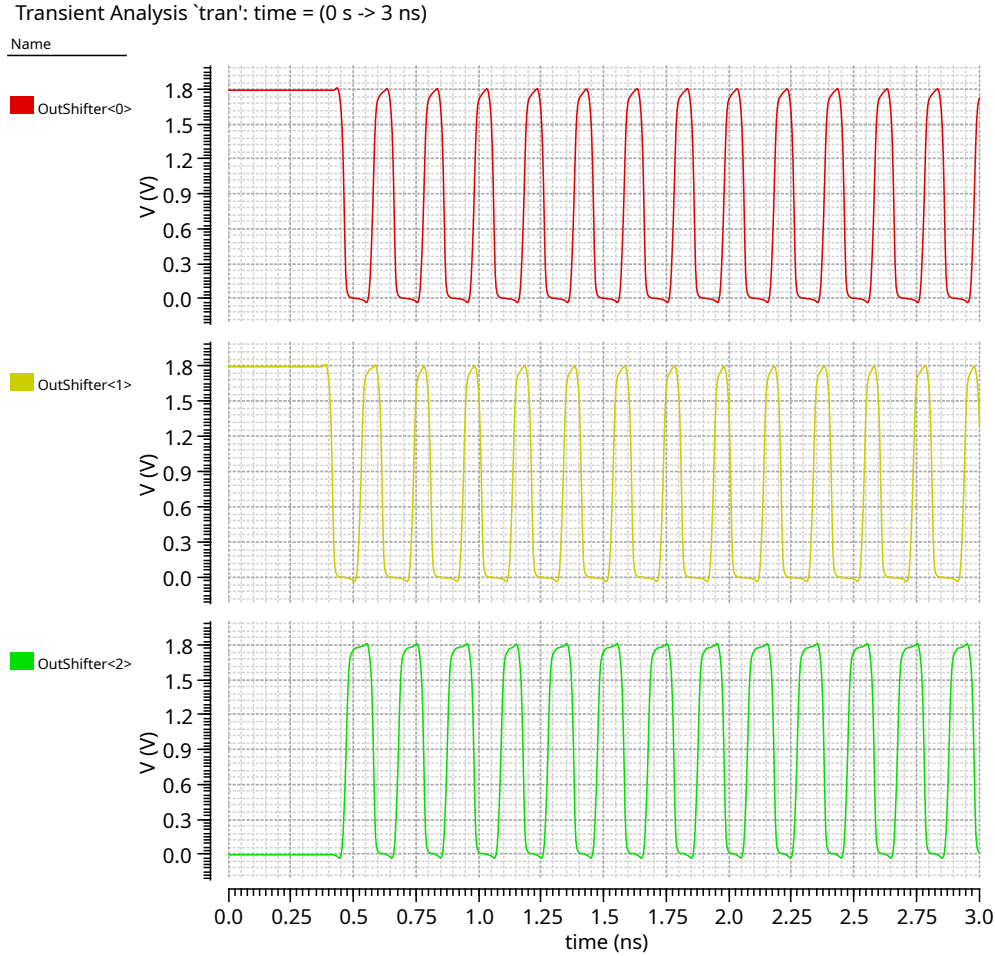


Figure 4.3: Transient response of the level-shifter outputs for a 10101010 input sequence at 10 Gb/s. The output signals are translated from the 0.8 V logic domain to the 1.8 V domain required by the PPCML driver inputs.

The simulated waveforms show that the three level shifters correctly generate full-swing 1.8 V output signals. However, the first level-shifter output exhibits a slightly larger propagation delay than the other two outputs. This difference is mainly caused by the larger capacitive load associated with the high-current PPCML branch that it drives. Since this branch is scaled to handle a higher bias current, its input devices present a larger gate capacitance. As a result, the corresponding level shifter requires more time to charge and discharge the load, increasing its delay with respect to the lower-current branches.

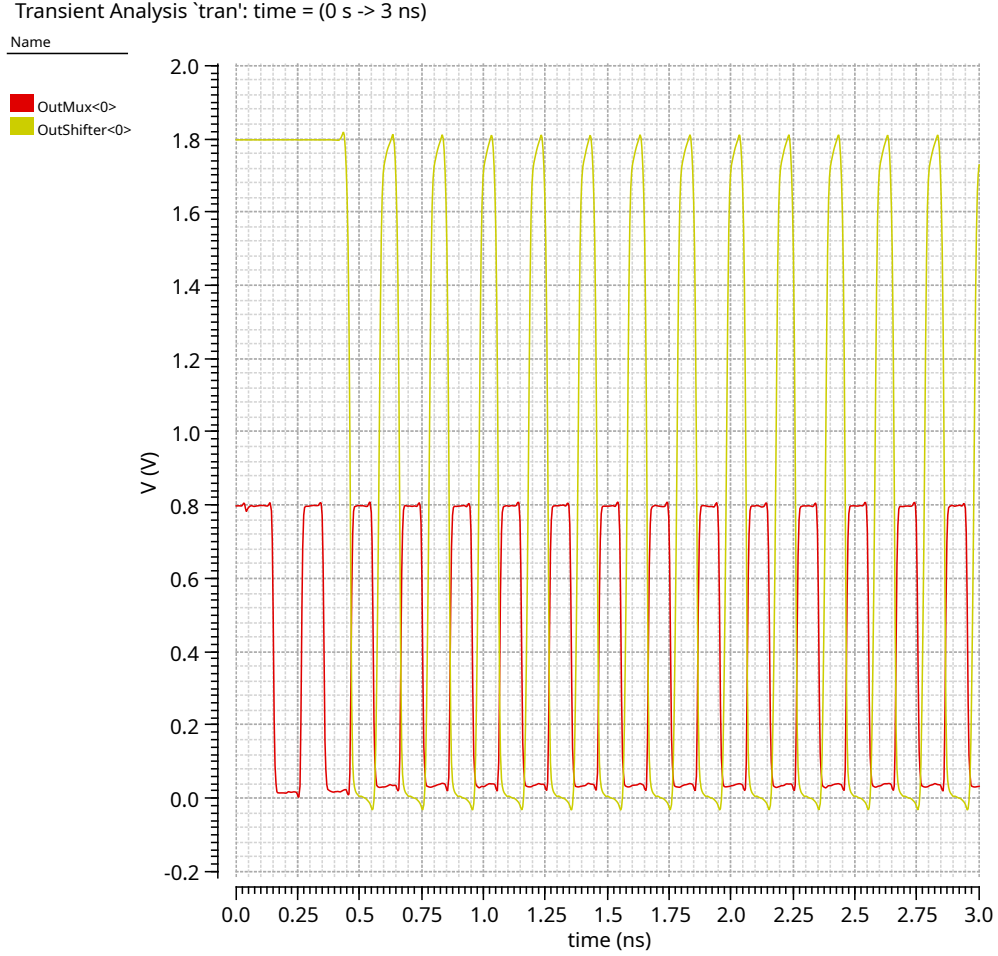


Figure 4.4: Comparison between the mux output and the corresponding level-shifter output. The observed delay is mainly introduced by the output stage of the level shifter, which uses scaled regenerative buffers to provide enough driving capability for the PPCML input load.

The comparison between the mux output and the level-shifter output shows the propagation delay introduced by the level-shifting stage. This delay is mainly associated with the final buffered output stage, which is intentionally scaled to drive the capacitive input load of the PPCML driver. Although this increases the propagation delay, it provides the required output swing and driving strength for reliable high-speed operation.

4.3 Eye Diagram Analysis at Different Data Rates

The eye diagrams were measured at the far end of the transmission line, after the channel model and before the differential load. These were obtained for different data rates using the (10101010) input sequence and for a channel length of 0.3 M. This test evaluates the ability of

the transmitter to generate clean transitions under increasingly demanding timing conditions. At lower data rates, the output eye remains clearly open, indicating sufficient voltage and timing margins. As the data rate increases, the available unit interval is reduced and the eye opening decreases due to the finite rise and fall times of the circuit and the bandwidth limitations of the signal path.

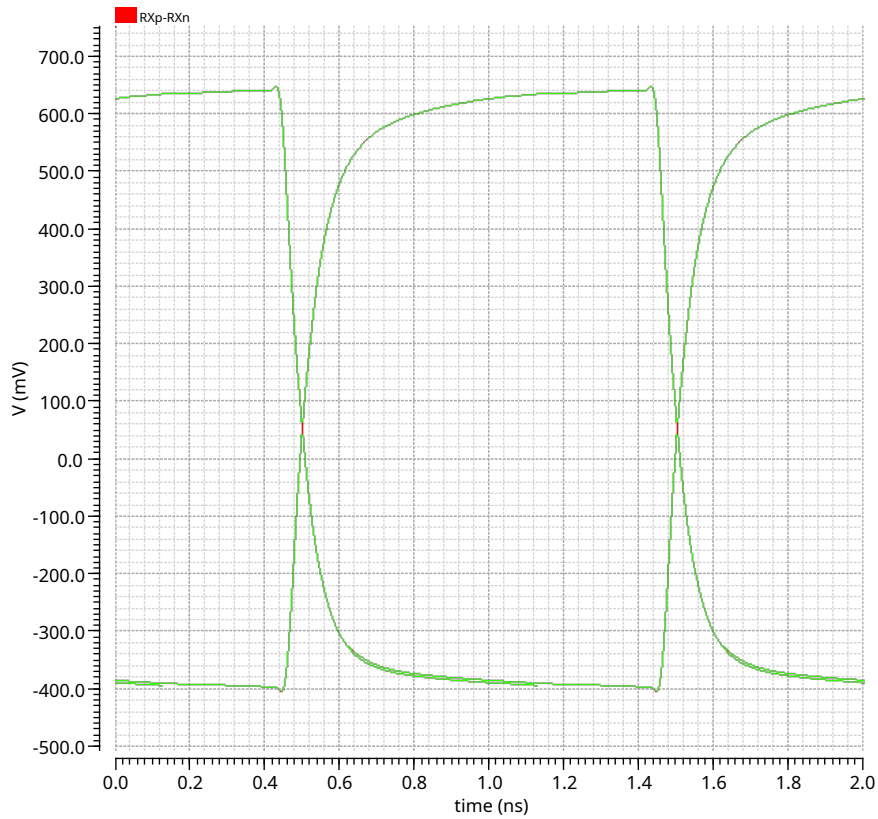


Figure 4.5: Eye diagram at 1 Gb/s using the 10101010 input sequence

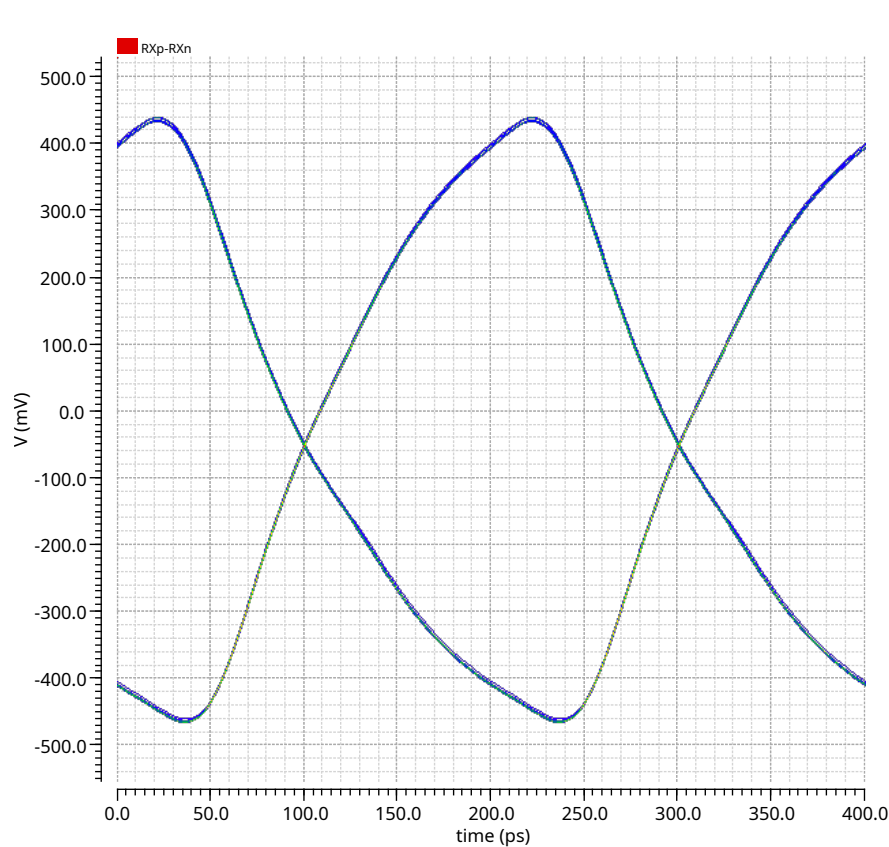


Figure 4.6: Eye diagram at 5 Gb/s using the 10101010 input sequence.

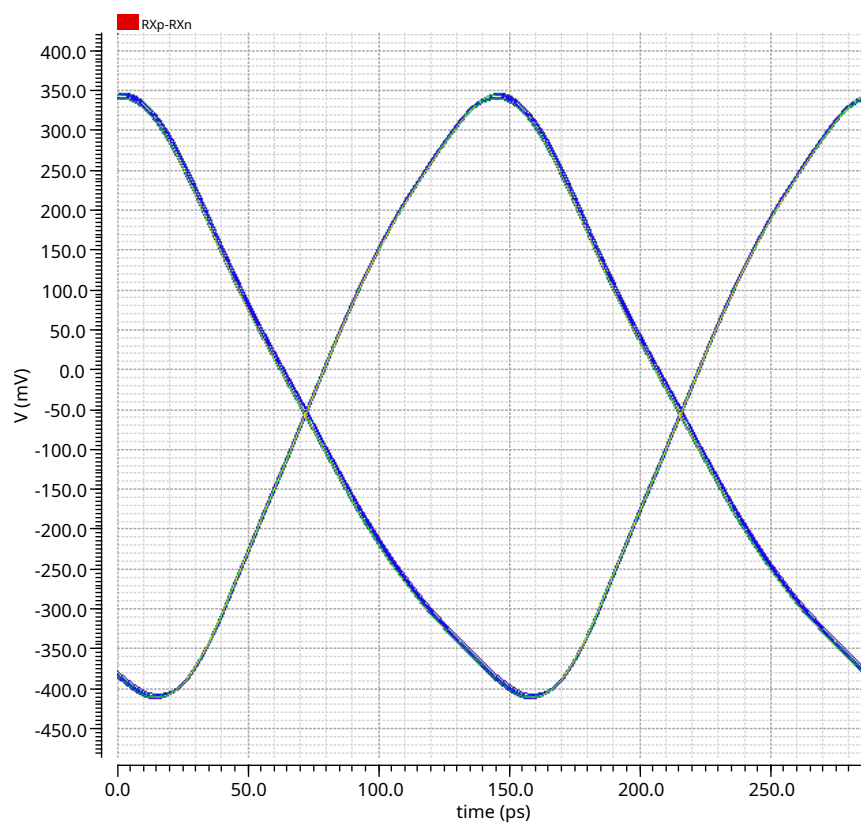


Figure 4.7: Eye diagram at 7 Gb/s using the 10101010 input sequence.

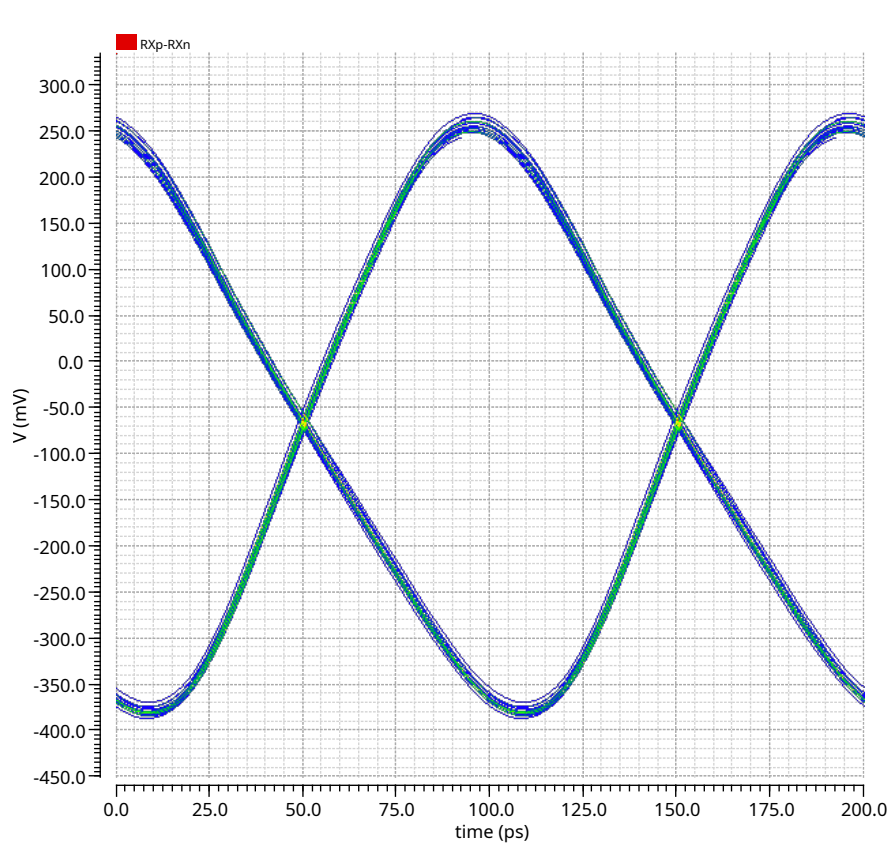


Figure 4.8: Eye diagram at 10 Gb/s using the 10101010 input sequence.

As the data rate increases, the unit interval becomes shorter and the circuit has less time to complete each transition. Due to the finite bandwidth of the transmitter signal path, including the driver, parasitic capacitances, and the load, the output waveform does not fully settle to its final voltage level before the next transition occurs. As a result, the effective output amplitude and the eye height are reduced at higher data rates.

This effect is further reinforced by the frequency-dependent attenuation of the transmission channel, which behaves as a low-pass network and attenuates the high-frequency components required for fast transitions.

4.4 Functional Verification of Configurable De-emphasis

The de-emphasis operation was also verified directly at the differential output of the transmitter. In this simulation, the output was observed before the transmission-line model in order to isolate the behavior of the driver and its control logic from the frequency-dependent losses introduced by the channel. Figure 4.9 shows the differential output voltage, defined as $V_{\text{dout}+} - V_{\text{dout}-}$,

with the de-emphasis function enabled. The waveform exhibits different output-amplitude levels depending on the relationship between the present data sample and its delayed versions. A larger differential amplitude is generated around selected data transitions, whereas a lower amplitude is maintained during consecutive symbols with the same contribution. This behavior confirms the functional operation of the main cursor and post-cursor driver branches.

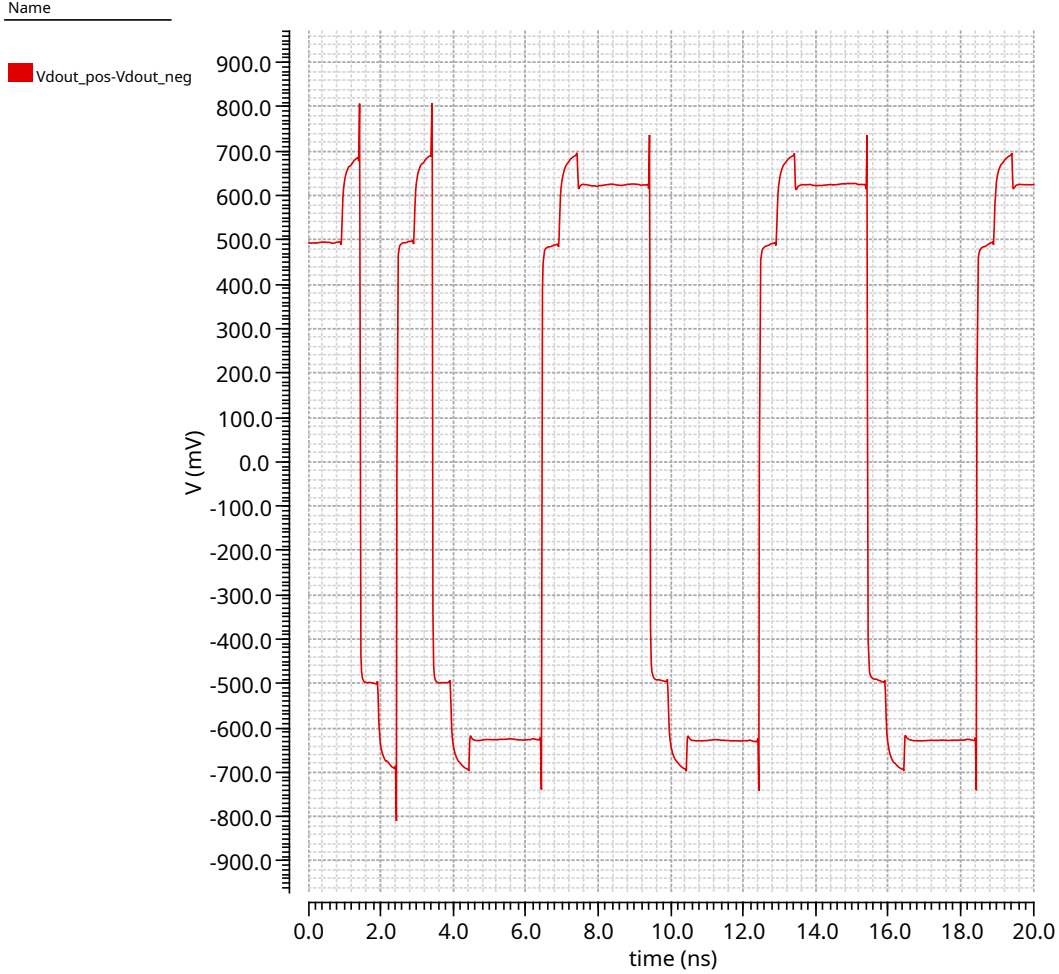


Figure 4.9: Differential transmitter output with the configurable de-emphasis function enabled.

The amount of de-emphasis can be configured by enabling or disabling the post-cursor driver branches. In the proposed implementation, the main cursor is generated by the 6 mA PPCML driver, while the additional 1.2 mA and 0.5 mA branches provide the delayed tap contributions. Consequently, several operating configurations can be selected depending on the required equalization strength. However, the control signals must be adapted to the selected configuration and operating data rate. In particular, the delayed data samples must remain correctly aligned with their corresponding unit intervals, and the polarity of each post-cursor contribution must

be selected according to the desired de-emphasis response. Therefore, changing the data rate or the enabled tap configuration may require adapting the timing and selection signals generated by the control logic. Since this verification does not include a transmission channel, it only demonstrates the correct functional generation and configurability of the de-emphasized waveform. The improvement in eye opening and the optimum tap weights for a particular channel would require additional simulations using representative channel models.

4.5 Discussion of Results

The simulation results confirm the correct functional operation of the main blocks of the proposed transmitter. The control logic generates the present and delayed data versions required by the feed-forward equalizer, while the level shifters translate these signals from the 0.8 V logic domain to the 1.8 V domain used by the PPCML output stages. The transient simulations also show that the different blocks remain correctly synchronized under the evaluated high-speed operating conditions.

The eye-diagram results show a progressive degradation of the transmitted signal as the data rate increases from 1 Gb/s to 10 Gb/s. At lower data rates, the longer unit interval allows the output waveform to approach its final voltage level before the next transition. At higher data rates, the reduced unit interval and the finite bandwidth of the transmitter path limit the settling of the signal, reducing the output amplitude and the vertical eye opening. The parasitic capacitances, the output load, and the frequency-dependent attenuation of the channel also contribute to this behavior. Nevertheless, an open eye is still obtained under the nominal simulation conditions evaluated in this work.

The configurable de-emphasis architecture was verified directly at the differential output of the transmitter. The different voltage levels observed in the transient waveform confirm that the main cursor and post-cursor branches are combined according to the generated control signals. The 1.2 mA and 0.5 mA post-cursor branches can be independently enabled or disabled, allowing the equalization strength to be modified.

However, this test was performed before the transmission-line model and therefore demonstrates the functional generation of the de-emphasized waveform rather than its improvement for a specific channel. The optimum tap configuration depends on the losses and impulse response of the channel. Furthermore, the timing and selection signals of the control logic must be adapted to the selected data rate and tap configuration in order to maintain the correct alignment of the delayed data samples.

The presented results correspond to nominal, pre-layout circuit simulations. Consequently, the effects of extracted interconnect parasitics, process and temperature variations, device mis-

match, and manufacturing variability have not yet been included. These aspects must be evaluated before considering the design ready for physical implementation.

Chapter 5

Conclusions

This Bachelor's Thesis has presented the design and circuit-level verification of a high-speed SerDes transmitter driver implemented in GF22nm FD-SOI technology. The main conclusions of the work can be summarized as follows:

- The proposed architecture combines a differential PPCML output stage with a configurable three-tap feed-forward equalizer. The complete transmitter also includes the required bias-generation circuits, 0.8 V to 1.8 V level shifters, common-mode feedback circuitry, modified TSPC flip-flops, and a distributed power-down strategy.
- The functional simulations confirmed the correct operation of the main transmitter blocks. The control logic generates the present and delayed data samples required by the equalization scheme, while the level shifters provide the voltage translation required to drive the 1.8 V PPCML stages. The differential output behavior was evaluated at data rates from 1 Gb/s to 10 Gb/s under nominal simulation conditions.
- The eye-diagram simulations showed the expected reduction in signal amplitude and eye opening as the data rate increased. This behavior is mainly associated with the shorter unit interval and the finite bandwidth of the transmitter, load, parasitic elements, and transmission channel. The 10 Gb/s simulation represented the most demanding operating condition considered in this work and demonstrated the high-speed operation of the proposed architecture under the evaluated conditions.
- The configurable de-emphasis function was also verified at the transmitter output. The resulting waveform confirmed the contribution of the main cursor and the two independently configurable post-cursor branches, biased at 6 mA, 1.2 mA, and 0.5 mA, respectively. This architecture provides flexibility to adapt the transmitted waveform by enabling or disabling the post-cursor taps. However, the optimum configuration and its quantitative benefit for

a particular communication channel were not determined in this work, since this would require adapting the control timing and optimizing the tap weights using representative channel models.

5.1 Future Work

The next stage of the project would consist of completing the physical implementation and extending the verification of the proposed transmitter. The main future developments are summarized as follows:

- **Physical layout implementation:** the complete transmitter should be implemented at layout level, taking into account device matching, symmetry, interconnection lengths, current density, and the routing of the high-speed differential signals.
- **Design-rule checking:** a Design Rule Check (DRC) should be performed to verify that the physical implementation satisfies the manufacturing constraints of the GF22nm technology.
- **Layout-versus-schematic verification:** an LVS verification should be carried out to confirm that the extracted layout connectivity and device parameters correspond to the original schematic design.
- **Parasitic extraction:** the resistive and capacitive parasitic elements introduced by the devices and interconnections should be extracted from the completed layout.
- **Post-layout simulation:** the extracted circuit should be simulated to evaluate the impact of the layout parasitics on the propagation delay, output amplitude, eye opening, and maximum operating data rate.
- **Variability analysis:** additional verification should include process, voltage, and temperature corners, as well as Monte Carlo simulations to evaluate the effect of device mismatch and manufacturing variability.
- **Extended circuit characterization:** a complete small-signal AC characterization of the operational amplifier and the common-mode feedback loop could be performed, including open-loop gain, bandwidth, pole locations, and stability.
- **De-emphasis optimization:** the tap weights and control timing should be adapted and optimized for representative transmission channels. Their effectiveness could then be evaluated using quantitative eye-diagram measurements or bit-error-rate simulations.

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