Universitat Autònoma de Barcelona

Masther's Thesis

Master in Telecommunication Engineering

Characterization of FD-SOI transistor

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AGRAÏMENTS:

En primer lloc vull donar les gracies als directors del projecte Albert Crespo i Montse Nafría , també al Javier Martín, que m'han donat l'oportunitat de treballar en aquest camp tant interessant de l'enginyeria electrònica, així com el seu suport, dedicació, disponibilitat i paciència per resoldre tots els dubtes i guiar-me durant la realització d'aquest treball.

També al professors i col·laboradors del Departament d'Enginyeria Electrònica de la UAB, per proporcionar-me l'espai i les eines necessàries per a la realització d'aquest projecte de fi de màster.

Resum:

En aquest projecte s'han realitzat mesures en transistors FD-SOI, fabricats per CEA-LETI, per tal de dur a terme una caracterització d'aquests dispositius , ja que són molt nous i necessiten de ser estudiats. Aquest treball s'ha centrat en caracteritzar l'envelliment dels dispositius i el RTN observat . Per a caracteritzar l'envelliment i la variabilitat de les mostres en funció dels cicles aplicats, les mesures s'han realitzat aplicant tensions d'estrés constant (CVS) directament al dispositiu amb una taula de puntes i un analitzador de paràmetres de semiconductors (SPA). Per tal d'observar RTN s'han estudiat diferents procediments elèctrics, controlant els diferents paràmetres durant les mesures.

Resumen:

En este proyecto se han realizado medidas en transistores FD-SOI, fabricados por CEA-LETI, para llevar a cabo una caracterización de estos dispositivos , puesto que son muy nuevos y necesitan de ser estudiados. Este trabajo se ha centrado en caracterizar los mecanismes de envejecimiento de los dispositivos y el RTN observado- Para caracterizar el envejecimiento y la variabilidad de las muestras en función de los ciclos aplicados, las medidas se han realizado aplicando tensiones de estrés constante (CVS) directamente al dispositivo con una tabla de puntas y un analizador de parámetros de semiconductores (SPA). Para observar RTN se han estudiado diferentes procedimientos eléctricos, controlando los diferentes parámetros durante las medidas.

Summary:

In this project, measurements have been made on FD-SOI transistors, fabricated by CEA-LETI, to carry out a characterization of these devices, since they are very new and need to be studied. This work has focused on characterizing the aging mechanism of the devices and the observed RTN. To characterize the aging mecnhainsm and variability of the samples based on the applied cycles, the measurements have been made by applying constant stress voltages (CVS) directly to the device with a wafer prove station and a semiconductor parameter analyzer (SPA). To observe RTN, different electrical procedures have been studied, controlling the different parameters during the measurements.

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Presentation

Nowadays, the rapid technological advances of recent years have induced a massive spread of electronic devices surrounding our environment (from tablets to smartwatches and even health monitoring gadgets), their architecture is designed with integrated circuits. This is related with the new generation of devices known as IoT devices (Internet of Things) where ubiquitous electronic devices exchange information between them and with the cloud.

This massive expansion of connected "things" has been rapidly increasing the demand for energy. Thus, “the law of how much performance corresponds to a better device”, the predominant design theory in past years, is no longer acceptable. Instead, now the systems designed for IoT applications need to take account the energy efficiency. The result is not only an increased devices autonomy, also the preservation of natural resources in order to respect our world.

Scaling the technology node of a microprocessor resulted in reducing the power consumption while maintaining a similar performance, this implies a higher energy efficiency was achieved with technology scale down.

This energy gain with transistors scale down has been possible until the 90 nm node. Beyond this node, several fundamental physics limitation previously neglected, for example Short Channel Effects and the Drain-Induced Barrier Lowering (DIBL).
To overcome the 90 nm manufacturing barrier, alternative technologies, based on thin film, have been proposed. The two main alternatives proposed by the industry were: the Fully depleted Silicon on Insulator (FD-SOI) and the Fin Field Effect Transistor (FinFET) technologies in which the electrostatic control in the channel has been improved to enable the pursuit of power consumption and performance improvements with downscale [7].
Concreting, in this work it has studied the Fully Depleted Silicon on Insulator (FD-SOI) transistor.

This master's thesis is organized as follows:

- Chapter 1: Introduces the evolution from the MOS capacitors to the newest FD-SOI transistor, comparing it to the conventional MOSFET technologies. Also are introduces the aging mechanism and the source variability of these devices.
- Chapter 2: Explains the experimental procedure that has been implemented to perform the measurements of the different studies carried out in this master's thesis, having very importance the RTN and the aging characterization.
- Chapter 3 : Here is studied the fresh characteristics curves of the fresh UTBB FD-SOI devices, including the extraction of their threshold voltage and mobility. Moreover, their dependence on the channel dimensions was also analyzed.
- Chapter 4: Are showed and interpreted the results obtained of the Random Telegraph Noise (RTN), for different device dimensions.
- Chapter 5: Are analyzed the aging results obtained when activate a Positive BTI in these N-type UTBB FD-SOI transistors
- Finally, chapter 6 concludes this thesis, summarizing the main contributions and presenting the conclusions and future perspectives of this work-

Chapter 1

Introduction

In this section is explained the MOS capacitor, which is the structure on which the MOSFET transistor is based, and its FD-SOI evolution characterized in this master's thesis.

The main problems derived from transistor scaling are also introduced, such as short channel effects (SCE), in particular the drain-induced barrier lowering (DIBL), or with emphasis on those related to reducing the thickness of the gate dielectric for the vertical scaling, such as tunnel leakage current. Moreover, the time-dependent variability related to aging mechanisms and source variability will be studied as relevant sources of circuit degradation performances.

1.1 MOS Capacitor

The MOS capacitor is a two-terminal structure made up of two electrodes with a layer of insulating material between them. Figure 1-1 shows the structure of a MOS capacitor with P-type substrate.

The first one, the gate terminal (Gate, G), can be of metal or very doped polysilicon. The other electrode is the substrate terminal (Bulk, B), and is made of semiconductor material, usually silicon (Si), which is doped with impurities in order to change the electrical properties of the semiconductor. Depending on the nature of the impurities charge, net negative/positive charge it will became an N-type or P-type substrate.

Just in the middle, between the two electrodes the dielectric is located, traditionally it was SiO_2, and was later improved with the introduction of nitrogen (SiON), in order to improve the insulating properties, and thus decreasing the leakage currents without modifying the MOS capacitor value [1]. Currently, the use of materials with high dielectric permittivity (high-k materials) has become widespread, since they seem to offer a better implementation benefits offering a solution to the problems derived from the

scaling, since the combination of the metal gate and high-k dielectric are very attractive to maintain low gate leakage and control SCEs [2].

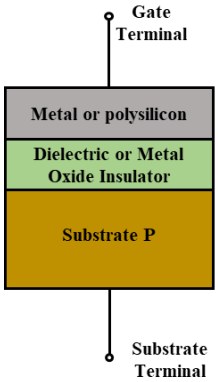


Figure 1-1: Structure of the MOS p-type capacitor, with the gate (Gate, G) and substrate (Bulk, B) terminals.

1.1.1 Operation Regimes of the MOS Capacitor

When no potential is applied through the capacitance terminals of the MOS structure, it is said to be in equilibrium [3]. Since voltage is applied, the structure of bands of the MOS capacitance is modified, giving rise to different electrical behaviors of the semiconductor in the region near the oxide. Figure 1-2 shows the charge concentrations at the metal-oxide and oxide-semiconductor interfaces for the different situations that can occur, summarizing the three following operating regions of the MOS capacitor, for the case of a p-type substrate.

Accumulation Regime

When a positive potential drop is applied between the gate and the substrate, part of this potential falls on the oxide interface, creating an electric field in the MOS structure capable of attracting holes in the semiconductor towards the dielectric (Figure 1-2a). The carriers are accumulated close to the oxide-substrate interface (these carriers are electrons in n-type substrate and holes in p-type substrate).

Depletion Regime

When a positive voltage is applied on a PMOS structure, the resulting electric field causes electrons to be attracted to the oxide-semiconductor interface, recombining with holes in the semiconductor region near the oxide. The voltage applied is negative voltage for a NMOS structure. This forms a zone of depletion at the oxide-semiconductor interface with zero net charge, the electrons are repelled from the channel to the substrate (Figure 1-2b). MOS capacitor is said to be in depletion mode.

Inversion Regime

If the voltage between the gate and the substrate is positive and sufficiently high, the potential drop in the oxide becomes bigger, and therefore the electric field in the structure is greater. This causes a greater number of electrons to be attracted to the oxide-semiconductor interface, which does not find holes to recombine. This accumulation of electrons causes an inversion of carriers in the semiconductor region near the oxide (Figure 1-2c). In this situation, it is said that the MOS capacitor is in the regime of inversion of carriers. That is, although the fact that the substrate is doped with a positive charge, in other words the oxide-substrate interface has become p-type, in this operating regime the total free charge at the oxide-semiconductor interface is negative. The voltage for which this situation is reached is called the threshold voltage (V_{th}).

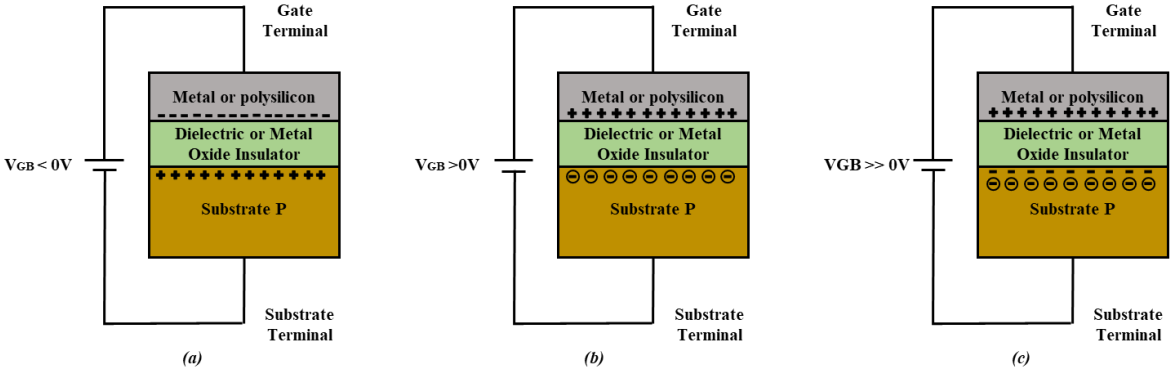


Figure 1-2: Charges in a Metal-Oxide-Semiconductor structure (p-type substrate) under accumulation, depletion and inversion conditions. (a) Accumulation regime of majority carriers, (b) Depletion regime of carriers and (c) In the inversion regime of carriers.

1.2 MOSFET Transistor

The MOSFET transistor (Metal-Oxide-Semiconductor Field-Effect Transistor) is a device based in the MOS Capacitor structure, Figure 1-3 shows the structure of a MOSFET transistor with a P-type substrate. Then, of the same way it has one metal plate and a second one doped semiconductor substrate. But in the MOSFET, at both sides of the capacitive structure (MOS), two regions have been added with a high concentration of doping substances of opposite charges to the substrate. These regions are known as the drain and source terminals. The region of the substrate located between the source and drain and just below the oxide insulator is called channel. Since carriers in the channel are electrons, the MOSFET is named nMOSFET or nMOS and when these carriers are holes the MOSFET is called pMOSFET OR pMOS

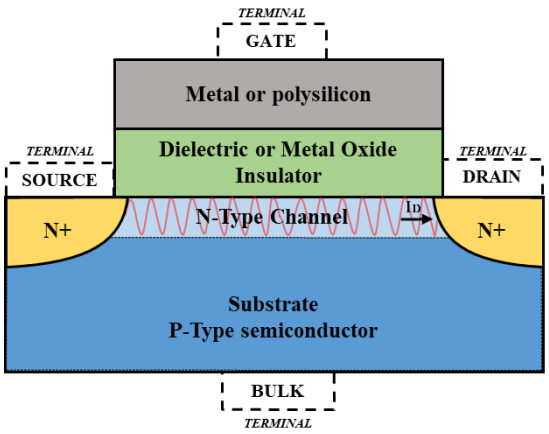


Figure 1-3: Structure of the nMOSFET transistor, with the gate (Gate, G), the terminals of the doped regions (Drain, D and Source, D) and the substrate (Bulk, B) terminals.

Then, the functionality of the transistor is based on the current flow between the drain and the source terminal (when in inversion mode a layer of minority carriers is created in the channel area). The gate voltage controls the current flow through the channel when a voltage to the drain is applied (V_D).

1.2.1 Regions of Operation of MOS Transistors

The voltages differences between the gate, drain and source terminals (assuming bulk or substrate to be at same voltage as source) determine the magnitude of current flowing in MOSFET. In each of these regions, we can represent the current as a function of gate-to-source voltage (V_{GS}) and drain-to-source voltage (V_{DS}).

In a MOS device, the voltage at gate terminal needs to be such that it attracts carriers of appropriate type towards itself, in this way, when sufficient carriers are attracted towards gate, channel is said to be formed. A current, then, flows between source and drain terminals depending upon the voltages at gate and drain terminals. The voltage of substrate also impacts the magnitude of current as it also determines the amount of carriers in the channel.

For an nMOS device, the channel is formed by electrons. So, to attract electrons, gate voltage must be positive greater than source voltage. For the formation of channel, the difference between V_G and V_S ($V_G - V_S$) must be greater than V_{th} (threshold voltage of the MOSFET).

Threshold voltage is defined as the minimum difference in gate-to-source voltage needed for the formation of channel in a MOS device. For nMOS, V_{th} is positive, as for channel formation gate needs to be at higher voltage as explained above. Similarly, for pMOS, V_{th} is negative as gate needs to be at lower voltage than source for channel to be formed.

On increasing gate voltage beyond threshold voltage, current through MOS increases with increasing gate voltage. Also, if we increase drain voltage keeping gate voltage constant, current increases till a particular drain voltage. After that, increasing drain voltage does not affect the current. Depending upon the relative voltages of its terminals, MOS is said to operate in either of the cut-off, linear or saturation region.

In the next Figure 1-4 is shown the different operation regions, the V_{DS} in function of the drain current (I_D).

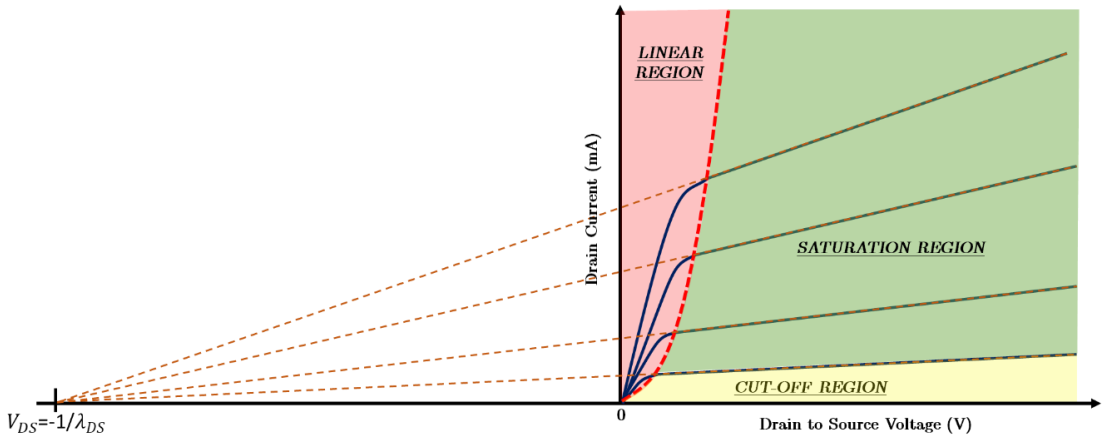


Figure 1-4: MOSFET Operation Regions as a function of V_{DS} and I_D

Cut-off regime

When the gate voltage is small (less than V_{th}), the number of carriers in the channel region it will be small, and then no current can flow between Source and Drain ($I_D = 0$). It is then said that the transistor is in cut-off.

Cut-off region is also known as sub-threshold region. In this region, the dependence of current on gate voltage is exponential. The magnitude of current flowing through MOSFET transistor in cut-off region is negligible as the channel is not present.

Linear or ohmic regime

As gate voltage increases enough, beyond the threshold voltage (V_{th}), induces a layer of inversion of carriers, known as MOSFET channel, and the current I_D flows can flow throw it, if $V_{DS}>0$. Then, the current is represented as a linear function of V_{GS} and V_{DS} voltages. The MOSFET transistor is said to be operating in linear region.

Saturation Regime

When the channel is formed ($V_{GS} \geq V_{th}$) and the voltage V_{DS} continues to increase, there comes the situation ($V_{DS} \geq V_{GS} - V_{th}$) where the voltage between drain and gate decreases, causing the constriction of the channel in the area near the drain.

In this situation, the drain current becomes saturated, in other words, increasing drain voltage seems to have no effect on current. The transistor is said to work in the saturation zone.

The Figure 1-5 shows the structure of a MOSFET transistor with a p-type substrate and the Equation Table 1-1 shows the condition and the drain current value (I_D), both for each operation region [4].

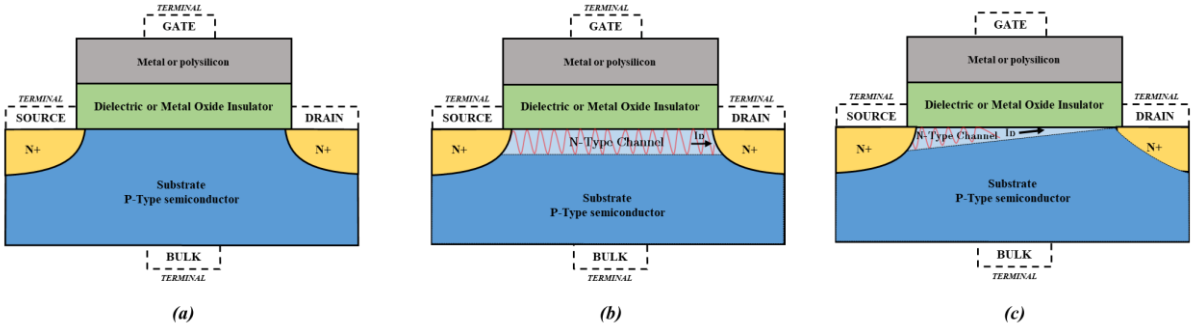
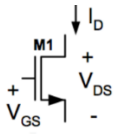
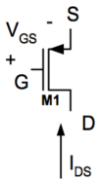


Figure 1-5: Cross section of the MOSFET transistor (a) When V_{GS} < V_{th} doesn't form a channel, the transistor is cutoff, (b) When $V_{GS} \geq V_{th}$ the carrier inversion channel is created between drain and source, the transistor operates in the linear zone, and (c) When $V_{DS} \geq V_{GS} - V_{th}$ the constriction zone is created, the transistor is operating in the saturation zone

N-type MOSFET			
Cut-off region	$V_{GS} \leq V_{th}$	$I_D = 0$	
Linear Region	$V_{GS} > V_{th}$ $V_{DS} < V_{GS} - V_{th}$	$I_D = \frac{\mu_n W C_{ox}}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right)(1 + \lambda_{DS})$	
Saturation Region	$V_{GS} \geq V_{th}$ $V_{DS} \geq V_{GS} - V_{th}$	$I_D = \frac{\mu_n W C_{ox}}{2L}(V_{GS} - V_{th})^2(1 + \lambda_{DS})$	
P-type MOSFET			
Cut-off region	$V_{SG} \leq \lvert V_{th} \rvert$	$I_{SD} = 0$	
Linear Region	$V_{SG} > \lvert V_{th} \rvert$ $V_{SD} < V_{SG} - \lvert V_{th} \rvert$	$I_{SD} = \frac{\mu_P W C_{ox}}{L}\left((V_{SG} - \lvert V_{th} \rvert)V_{SD} - \frac{V_{SD}^2}{2}\right)(1 + \lambda_{SD})$	
Saturation Region	$V_{SG} \geq \lvert V_{th} \rvert$ $V_{SD} \geq V_{SG} - \lvert V_{th} \rvert$	$I_{SD} = \frac{\mu_P W C_{ox}}{2L}(V_{SG} - \lvert V_{th} \rvert)^2(1 + \lambda_{SD})$	

Equation Table 1-1: Equation for I_D in a transistor MOSFET in Cutoff, linear and saturation regions for both N-Type and P-Type Substrate

1.3 Scaling MOS Devices

Over the past three decades, CMOS technology scaling has been a primary driver of the electronics industry, and has provided a path toward both denser and faster integration, since the scaling is the primary factor in achieving high-performance microprocessors and memories. The importance and persistence of this activity is rooted in the confluence of two of the strongest drives governing the business; the push for greater device performance, measured in terms of switching speed, and the desire for greater manufacturing profitability, dependent upon reduced cost per good device built.

The need for this better performance and integration has accelerated the scaling trends in almost every device parameter, such as effective channel length, gate dielectric thickness, supply voltage, device leakage, etc.

Some of these parameters are approaching fundamental limits, and alternatives to the existing material and structures may need to be identified in order to continue scaling.

The continued physical feature size scaling of complementary Metal Oxide Semiconductor (CMOS) transistors is experiencing asperities due to the following several factors, and maybe it is expected to reach its boundary at size of 22 nm technology.

Next, these are the most important challenges that could hinder CMOS technology from being utilized in future.

Physical challenges

Many parasitic effects have appeared when scaling-down the horizontal dimensions of the conventional MOS transistors below 100 nm. In fact, the so called short channel effects (SCE) arise when the distance between the source and the drain reaches the order of magnitude of the depletion region, it produces an effect over saturation current.

Also, there are effects due to the scaling in vertical dimension, the gate oxide tunneling produce leakage currents from the gate to the channel.

Material challenges

These basically come from the inability of the dielectric and wiring materials to provide reliable insulation and conduction, respectively with continued scaling.

Power-thermal challenges

These are because of the ever increasing number of transistors integrated per unit-area, which demands larger power consumption and higher thermal dissipation.

Technological challenges

These are the results from the incompetency of lithography-based techniques to provide the resolution below the wavelength of the light to manufacture to CMOS devices.

Economic challenges

These are mainly due to the rising in cost of production, fab, and testing that may reach a point where it will be not affordable from economic point of view.

1.3.1 Horizontal Scaling

For the long-channel devices (non-scaled transistors), the source and drain are separated far enough that their depletion regions have no effect on the potential or field pattern in most part of the device, these effects are masked. Hence, for such devices, the threshold voltage is virtually independent of the channel length and drain bias.

However, due to the aggressive horizontal scaling of MOSFET, these devices behave differently to the long-channel devices described in Section 1.2. First, the threshold voltage becomes a function of the channel length and width. Secondly, the subthreshold properties are degraded, being variable depending on the $V_{DS,}$ as a consequence of DIBL (Drain-Induced Barrier Lowering). Third, the effective length channel (L_{eff}) becomes a function of the V_{DS} bias because of the channel length modulation. These present effects have practical importance in the design of high-performance CMOS circuits today.

1.3.1.1 Short Channel Effect (SCE)

As a consequence of the SCE, the absolute value of the threshold voltage decreases with decreasing channel length, this is caused for the lowering voltage barrier in the channel, as depicted in the Figure 1-7b. This may be understood on the basis of a charge sharing model is illustrated in the next Figure 1-6.

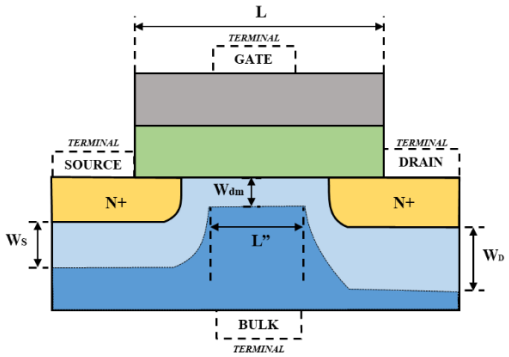


Figure 1-6: Charge sharing and the SCE in a short-channel MOSEET.

In the short-channel MOSFFET some of the field lines in the source and drain depletion regions terminate on charges under the gate. In other words, some of the depletion layer charge under the gate is shared with the source and drain. Therefore, the threshold voltage should be estimated based on the trapezoidal region of charge under the gate. Then the threshold voltage is reduced, compared with long-channel value, by approximately [5]:

$$\Delta V_{th} \approx \frac{W_{dm}\,(L\prime - L)\varepsilon_{ox}}{2WLt_{ox}} \approx \frac{\varepsilon_{ox}(W_S + W_D)W_{dm}}{2WLt_{ox}} \qquad \textit{Equation 1-1}$$

Where:

W = Width of MOSFET channel

L = Length of MOSFET channel

W_{dm} = Depletion width in semiconductor under inversion

W_S = Source junction depletion width

W_D = Drain junction depletion width

ε_{ox} = Permittivity of the oxide

t_{ox} = Oxide thickness

The threshold voltage also becomes dependent on the device width. This requires that the implementation adjustment be designed so that the narrowest devices on the wafer have acceptable threshold voltages.

1.3.1.2 Drain-Induced Barrier Lowering

In addition, biasing the drain-to-source terminal also influences the depth of the depletion region in a short channel transistor, as in Figure 1-7c. Therefore, the short channel effect is intensified by the polarization of the drain, an effect known as Drain Induced Barrier Lowering (DIBL).

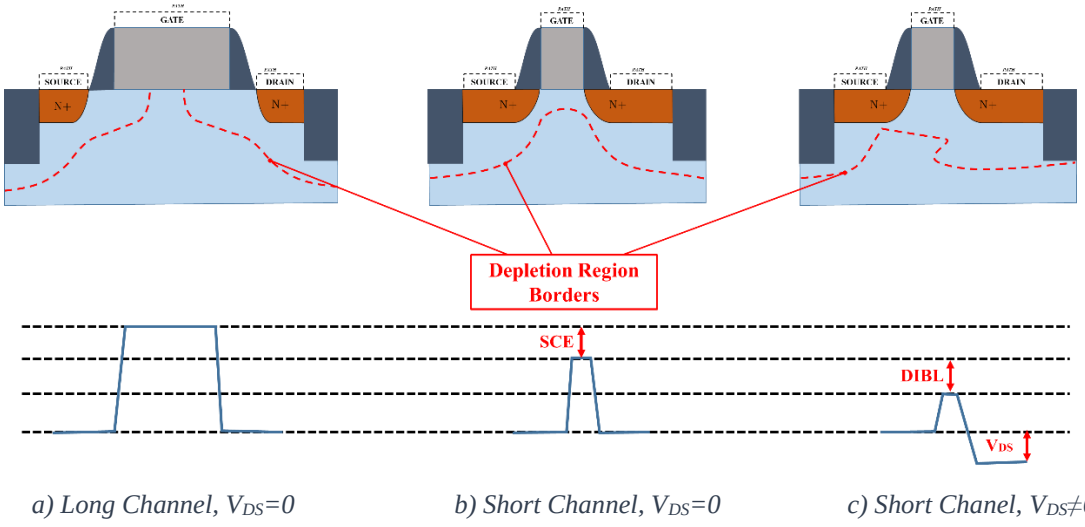


Figure 1-7: Lowering of the voltage barrier caused by the reduction of transistor's gate length

In the Figure 1-8 [6] is shown the DIBL effect in terms of the voltage threshold degradation.

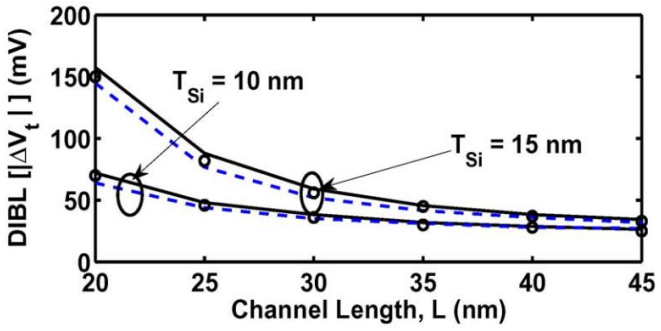


Figure 1-8: DIBL plotted as a function of channel length

Therefore, an increase in the drain-to-source bias causes a reduction in the threshold voltage and an increase in the subthreshold current. This contrasts with the case of a long-channel device, for which the subthreshold current is essentially independent of the V_{DS}.

DIBL is enhanced at high drain voltages and shorter channel lengths. The surface DIBL typically occurs before the deep bulk punch-through. It might cause permanent damage to transistors by localized melting of material.

1.3.1.3 Channel Modulation Effect

The drain current in a MOSFET saturates at the value of V_{DS}, which causes the channel to pinch off at the drain end. It occurs when the channel length is lower than 150nm. Further increase in V_{DS} causes the pinch-off point to move into the channel, toward the source, as shown in Figure 1-7c. This effect results in that the I_D-V_{DS} characteristic of the transistor has a positive slope in the saturation zone, it can be seen in the Figure 1-4.
Mathematically, the channel length modulation is modeled by multiplying the drain current expressions by a factor that increases linearly with the drain-to-source bias. For linear operation, the expression for the drain current including the channel length modulation is:

$$I_D = \frac{\mu_n W C_{ox}}{2L} (V_{GS} - V_{th})^2 (1 + \lambda_{DS}) \qquad \textit{Equation 1-2}$$

Where λ_{DS} is the empirical channel length modulation parameter. The channel length modulation effect is important in short-channel MOSFETs.

1.3.2 Vertical Scaling

While scaling down the channel length, oxide thickness has to be reduced nearly in proportion to the channel length. Decrease in oxide thickness results in increase in the electric field across the gate oxide. The high electric field and low oxide thickness result in considerable current flowing through the gate of the transistor. This current destroys the classical infinite input impedance assumption of MOS transistors and thus affects the circuit performance severely, causing electrical shorts between the gate and substrate and increasing the power consumption of the devices. This is known as gate oxide tunneling.

The dielectric strength of the thin oxide may permit oxide breakdown due to application of an electric field in excess of breakdown field. It may cause permanent damage due to current flow through the oxide.

1.4 The FD-SOI Transistor

In the previous Section 1.3 it has been described the challenges of the continuous scale down of semiconductor nodes, making possible the integration density and significant performance gains for each new technology node, as foreseen by Moore's law [7].

Although the improvements with scaling have been consistent for technology nodes until 90 nm, a number of fundamental physics limitation, previously neglected, have decreased the attractiveness of conventional bulk technology scaling beyond the referred node. The main physics limitations are Short Channel Effects (SCE), reduced carrier mobility, increased gate tunneling current and increased p-n junction leakage [8].

When the dimensions of the MOSFET transistor are reduced, the length of the gate is smaller, and consequently the working control over the channel region is also reduced, lowering the transistor performance. Consequently, some unwanted leakage current flows even when the transistor is switched off, this leakage current has been increasing with every new generation of transistor and represents a growing proportion of power consumption.

Moreover, according to the study published in [9], for nodes below 28nm, using conventional bulk transistor techniques will increase the cost per wafer by approximately 3%, and a 13% for 20nm node, mainly due to additional levels of process of manufacturing complexity at an ever-increasing rate. In technologies smaller than 28 nanometers new solutions need to be found to reduce complexity while bringing the benefits of reduced silicon geometries that the industry expects.

The Fully depleted silicon on insulator (FD-SOI) is a new approach that delivers these benefits while enabling a simplification of the manufacturing complexity process.

The FD-SOI technology use an undoped thin silicon film between source and drain, (see Figure 1-9) which enables a much better electrostatic control of the channel by the gate [10]. As a result, the so called short channel effect and the subthreshold leakage are greatly reduced.

Furthermore, the undoped silicon also substantially reduces the variation of transistor's threshold voltage (Vth) induced by the fabrication process, thus enabling circuit's operation at lower supply voltages (V_{dd}).

It's important to mention the evolution of the FD-SOI devices. Once the thickness of the silicon layer (t_{si}) is reduced to the point of generating a fully depleted channel, two different technologies are achievable by adjusting the thickness of the buried oxide layer (t_{BOX}): The FD-SOI with thick BOX, depicted in Figure 1-9a and the Ultra-Thin Body and BOX FD-SOI (UTBB FD-SOI), shown in Figure 1-9b.

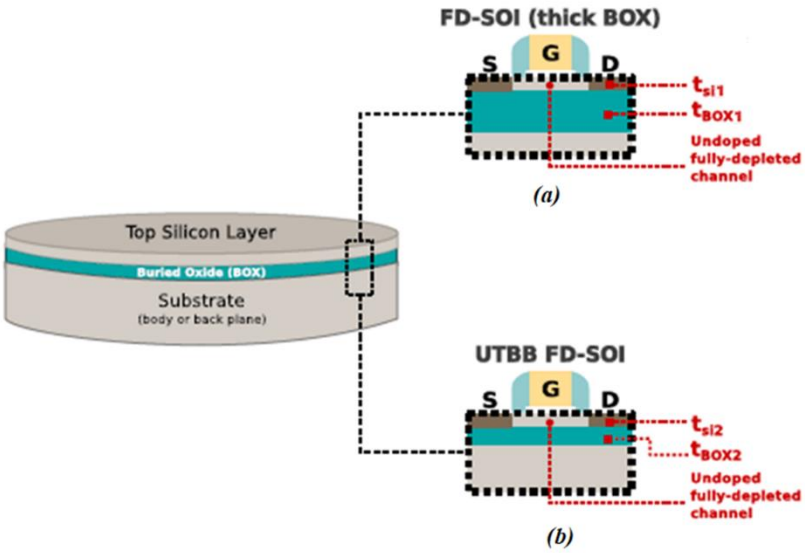


Figure 1-9 (a) FD-SOI (Thick BOX) and (b) UTBB FD-SOI. Both have the same thickness: tsi1= tsi2; However, the BOX of the UTBB FD-SOI is thinner: $t_{BOX2} < t_{BOX1}$ [10]

Not only the UTBB FD-SOI has been proven to have considerably reduced SCE but also a thin BOX allows calibrating transistors V_{th} by gate biasing.

Thanks to these advantages and the advances the technique for manufacturing SOI wafers, the UTBB FD-SOI technology prevails as the SOI alternatives to replace conventional bulk. Further details on UTBB FD-SOI will be given in the next section.

1.4.1 The UTBB FD-SOI Structure

A typical cross section of an UTBB FD-SOI (**U**ltra-**T**hin **B**ody and **B**ox **F**ully **D**epleted **S**ilicon **O**n **I**nsulator) transistor is shown in Fig. 1-9b and compared to a cross section of a conventional bulk transistor, in Fig. 1-9a. As explained in the previous section, the main difference between these technologies is the insertion of the ultra-thin BOX in the UTBB FD-SOI, separating the thin silicon film that forms source, drain and the channel from the substrate of the transistor.

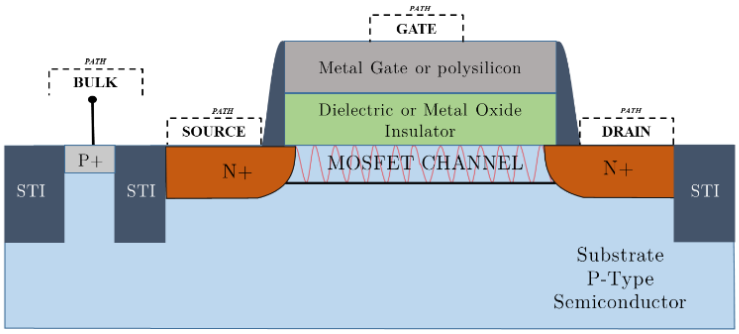


Figure 1-9a: Conventional nMOSFET transistor

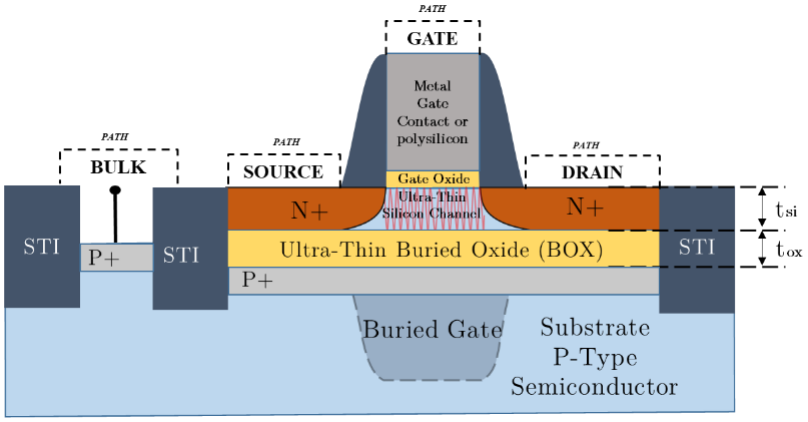


Figure 1-9b: FD-SOI nMOSFET transistor

Figure. 1-9: NMOS transistor cross sections. In the UTBB FD-SOI technology, the path for junction leakage is eliminated, and the gate and subthreshold leakages are considerably reduced.

1.4.1.1 Advantages of Thin Silicon Films

The extremely thin top silicon layer of UTBB FD-SOI transistors provides a much better electrostatic control than conventional MOSFET transistor. For achieving optimal electrostatic behavior, t_{si} is kept in the order of one third of the gate length value.

For instance, $t_{si} \cong$12nm to 15nm in UTBB FD-SOI 28 nm technology [11]. As a result, two major advantages: the first one is a reduced subthreshold slope. This parameter

reflects the capability of the gate to effectively control the current flow through the channel. The second major advantages of a better electrostatic control is the reduction of short-channel effects, especially DIBL. According to its theoretical Equation 1-3, the value of the DIBL is directly proportional to the depth of the source and drain junctions. Since in UTBB FD-SOI the depth of the junctions is t_{si}, which is considerably smaller than the corresponding depth in conventional bulk, the value of DIBL is considerably reduced in UTBB FD-SOI [10].

$$DIBL = \frac{\varepsilon_{SI}}{\varepsilon_{OX}}\left(1 + \frac{{X_j}^2}{L^2{}_{el}}\right)\frac{T_{ox}\cdot T_{dep}}{L^2{}_{el}}V_{DS} \qquad \textit{Equation 1-3}$$

1.4.1.2 Advantages of an Undoped Channel

In contrast to the conventional MOSFET technology, the isolation provided by the BOX (Ultra-thin Body and Box) make free the UTBB FD-SOI transistor from the obligation of doping the channel. Therefore, in the UTBB FD-SOI the different quantities of dopants injected into the channel during the manufacturing process is greatly reduced there by limiting the variability of the process.

As result the characteristic of each transistor is closer to the doped average, making that a circuit designed in UTBB FD-SOI technology operate in a faster frequency than an equivalent circuit designed in the same technology node in conventional MOSFET technology.

An undoped channel brings two major improvement: removing the random dopants fluctuation (RDF) of the channel and reducing the V_{th} variability, which are considered as two of the most critical challenges for scaling down in CMOS technology.

1.4.1.3 Advantages of the Isolation with an BOX and its upgrade Ultra-Thin Box

The presence of the BOX (Buried Oxide Layer), which completely isolates the source and drain from the substrate imposes certain advantages. The most straightforward one is the complete elimination of the current leakage from source-to-drain to the substrate.

Eliminating one of the sources of leakage that exists in conventional MOSFET technology allows reducing the static power consumption in UTBB FD-SOI technology.

Furthermore, the insertion of the BOX limits the depth of source and drain, which allows reducing the diffusion surface. As a consequence, a reduced parasitic junction capacitance is achieved.

Considering that the source and drain terminals are connected to each other to form logic gates, and considering that the output capacitance seen by a certain logic gate is the equivalent of all junction capacitances of all source/drain terminals connected to the output of that logic gate, reducing the junction capacitance directly reduces the energy required to switch a logic gate state. Therefore, the dynamic power consumption in an UTBB FD-SOI circuit is considerably lower while delivering the same level of performance of the conventional MOSFET transistor at the same operation frequency [12].

Another positive effect of the BOX addition is the elimination of the latch-up [13]. This phenomenon occurs in conventional MOSFET technology, under some specific situations. In the UTBB FD-SOI, thanks to the BOX and the Shallow Trench Isolation (STI in Figure. 1-9b), the adjacent transistors are electrically isolated from each other. The latch-up effect is thus eliminated in the FD-SOI technology.

Designing the FD-SOI 28nm node with a UTBB layer (Ultra-Thin Body and Box) for instance, $t_{box} \cong$ 15nm to 25nm [10], makes the transistor strengthens the electrostatic control over the channel by reducing the DIBL [14]. The short channel effects (SCE) are also decreased with a Ultra-Thin BOX due to the suppression of the lateral electrostatic coupling that exists between source, drain and channel of transistors with a thick BOX [15]. As a result, the reduction of t_{box} enhances the scalability of UTBB FD-SOI transistors down to the 11 nm node with an almost constant t_{si}.

1.4.2 Modulating the V_{th} of UTBB FD-SOI Transistors

In order to meet the tight power and performance constraints of nowadays complex design systems, the use of transistors with different V_{th} is mandatory.

In high performance designs, for instance, low V_{th} transistors are commonly used in critical paths to increase the performance of the overall system, whereas high V_{th} transistors are preferred for non-critical paths, so that the static power consumption is reduced. Availability of a variety of transistors with a large range of threshold voltage (V_{th}) is essential for designing high performance/low power chips.

1.4.2.1 Modulating the V_{th} through Manufacturing Techniques

The conventional MOSFET technology proposes three levels of V_{th}, high; regular; and low. In order to create these variants, the V_{th} is modified either by controlling the doping of the channel, or by changing the gate length used. These two options were not kept in the UTBB FD-SOI. Indeed, as described in previous sections, the channel in UTBB FD-SOI is undoped to reduced variability. Thus, doping the channel would increase the variability of the transistors. Moreover, the second method considerably raises the manufacturing cost and complexity.

Thus, to provide Multi-V_{th} devices and dynamic V_{th} modulation with an undoped channel in order to satisfy the low power circuit design requirements, a third method for creating a multi V_{th} platform have been used [15].

The substrate underneath the BOX is doped to a high level concentration [16], illustrated by the p+ layer in Figure 1-9b, also known as back plane.

Furthermore, since the back doping layer is isolated from the source/drain by BOX layer in the UTBB FD-SOI structure, it's possible to choose the well polarity. Thus, two V_{th} level possibilities are used in UTBB FD-SOI: a low Vth option (LVT), and a higher V_{th} option, which is known as regular V_{th} (RVT).

In the RVT configuration, the back plane dopant type is the opposite of source and drain dopants, which causes an increase in transistors V_{th}. A cross section schematic of a NMOS and a PMOS RVT transistors is depicted in Figure 1-10.

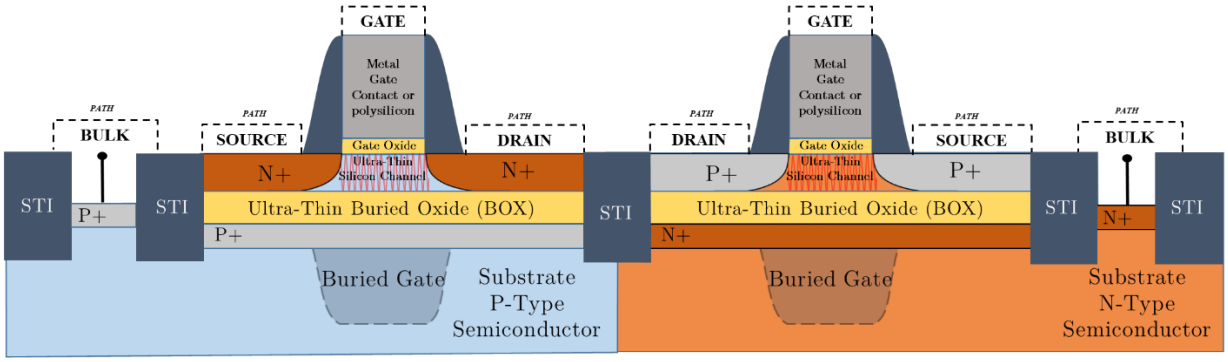


Figure 1-10 NMOS and a PMOS RVT transversal sections

In this case, the p-well and n-well disposition is equal to the conventional MOSFET technology: the NMOS lies over a p-well and the PMOS lies over an-well. Due to the similarity with the conventional bulk, this architecture is known as conventional well.

Conversely, in the LVT configuration, the back plane dopant type is the same of source and drain dopants, which causes a decrease in transistors V_{th}. A cross section schematic of a NMOS and a PMOS LVT transistors is depicted in Figure 1-11. Thus, the p-well and n-well dispositions are flipped if compared to the conventional bulk technology: the NMOS lies over an n-well and the PMOS lies over a p-well.

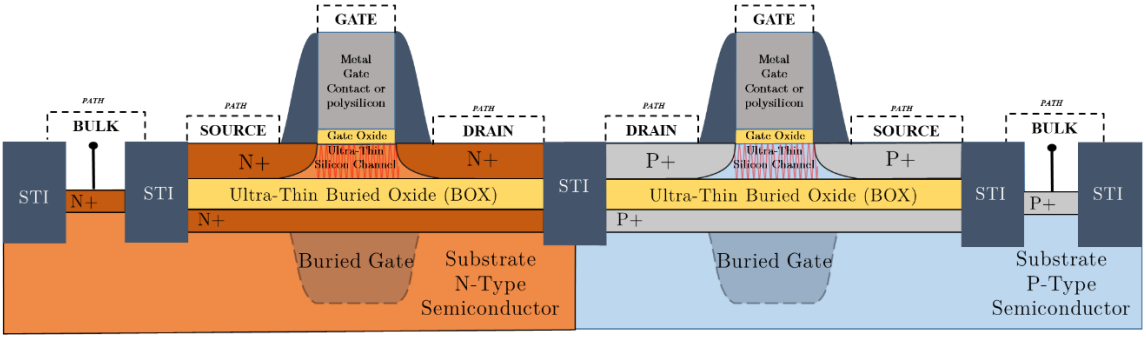


Figure 1-11 NMOS and a PMOS LVT transversal sections

This disposition of n-wells and p-wells are only possible since the BOX provides electrical isolation between source/drain and the back plane. It is commonly referred to as flip-well.

1.4.2.2 Modulating V_{th} post manufacturing: Body Biasing

The UTBB FD-SOI technology provides another method for modulating the V_{th} post manufacturing. Thanks to the ultra-thin BOX, applying a voltage to the back gate and using it as a fourth terminal, modifies the V_{th} of the transistors, a technique known as body biasing.

The back gate allows controlling the threshold voltage by about 85mV/V(depending on the design), when changing the back gate voltage, this is what is called as body biasing and it can be adjusted even during circuit operation, thus increasing the frequency of the circuit or reducing its static power consumption. Biasing is more efficient in FD-SOI, thanks to the dielectric isolation by the buried oxide layer.

Body biasing has been also used to compensate process variation, since the biasing voltage is applied post manufacturing,

For Forward Body Biasing (FBB), the transistor requires less voltage at the gate to switch, when the voltage applied reduces the V_{SD}, and then V_{th} is reduced as well. This results in faster transistor switching, increasing the overall performance and reducing the power system's static consumption

Similarly, Reverse Body-Biasing (RBB) can be applied to the transistors to increase the threshold voltage of the transistor, when voltage is applied to the body in order to increase the V_{SB} and consequently the V_{th}, this lowers the off-stage leakage and minimizes the static power consumption when the transistors are off.

Body biasing capabilities in FD-SOI opens a variety of opportunities such as achieving lower threshold voltages for the devices and lower power, and it can also be used for compensating process variations in a cell.

In addition, it has to be mentioned that the body biasing presents a better operation range when it is applied in the UTBB FD-SOI than when applied in an equivalent conventional MOSFET technology node. This opens new perspectives for performance boosting, static power consumption and post silicon variability control [17].

1.4.3 Power efficiency and performance on UTBB FD-SOI

FD-SOI includes excellent mismatch properties, a simplified planar manufacturing and capitalization of existing design techniques. Thanks to the possibility of biasing offers

unique "smart" solutions for dynamic power optimization [18]. Further, it has been experimentally demonstrated that FBB dramatically extends the power efficiency of this technology, making it a highly competitive technology for low voltage and energy efficient CMOS applications.

1.4.4 Manufacturing Cost

Fully Depleted Silicon-On-Insulator (FD-SOI) technology has been shown to be cost and performance competitive, being an alternative to the state of the art MOSFET technologies. Mobile and IoT applications demand both very high performance in RF and low manufacturing cost. This makes FD-SOI technologies a powerful option when weighted against conventional MOSFET.

As it was explained in the previous section 1.3, the chip processing cost per wafer keeps increasing from one technology node to the next one in function of the process complexity and number of masks. This processing cost evolution is shown in the next Figure 1-12a.

The process cost is more than doubled from the 90 nm node to the 22 nm node [19]. It's a fact that process cost becomes increasingly the dominant factor in the total cost.
In contrast, the substrate cost remains flat or even decreases significantly when the technology node advances.

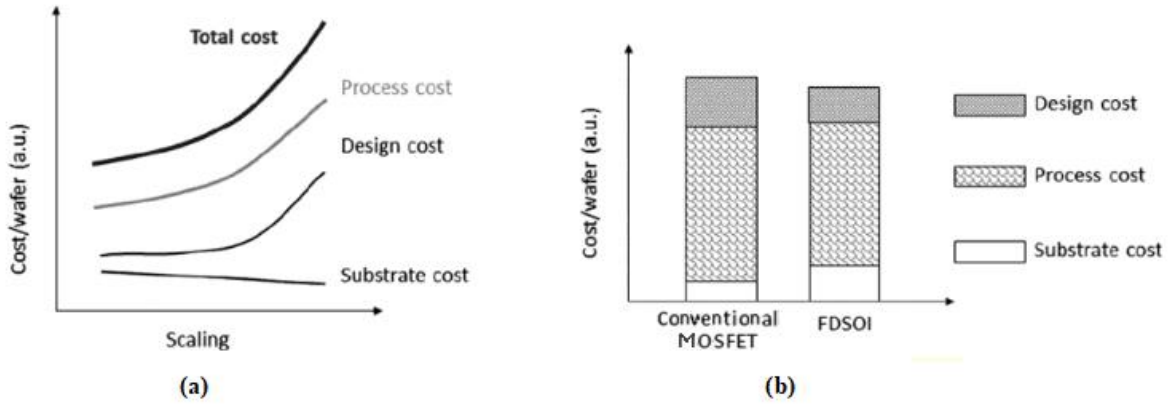


Figure 1-12 (a) Process and design costs per wafer increase while substrate cost decreases as technology advances. Substrate cost becomes a small fraction of the total cost of the state-of-the-art technology nodes. (b) Cost comparison of a conventional MOSFET transistor and FD-SOI. FD-SOI has higher substrate cost which is offset by the lower process [19].

Furthermore, the FD-SOI substrate cost may be offset by process simplifications enabled by FD-SOI, as for example the device isolation is straightforward applying a simple STI (Shallow Trench Isolation). Another cost-saving advantage of FD-SOI is the elimination of block masks, which are used for forming extensions and halos (punch-through suppression) in conventional MOSFET technology but are not needed for FD-SOI. Then, for an advanced technology as the FD-SOI, reduction of processing cost becomes even the most important and effective when reducing the total manufacturing cost.

Process simplification by FD-SOI results in the improvement of chip yield. The impact of the cost of raw FD-SOI wafers is further diluted when taking into account the design cost. The cost of raw wafers is becoming a small fraction of the total cost.

Therefore, it is possible for FD-SOI technology to achieve comparable or even lower manufacturing costs in comparison to bulk technology. Note that even though the cost per processed wafer increases, the cost per transistor decreases due to device scaling. A cost comparison between the state of the art conventional MOSFET and planar FD-SOI is schematically shown in Figure 1-12b. The higher substrate cost of FD-SOI is completely offset by the reductions in processing and design costs, rendering a lower total cost of planar FD-SOI than conventional MOSFET.

In conclusion, the UTBB FD-SOI technology exhibits good performance in all the evaluated parameters, manufacturing cost, short channel effects containment, power efficiency. Compared to the conventional MOSFET, it seems to be superior in many aspects, however several studies are required before FD-SOI becomes a mature technology. But many advantages and the manufacturing cost, in which both conventional MOS technology and UTBB FD-SOI are similar, make it a promising technology.

1.4.5 State-of-the-art FD-SOI Technology

There is a researcher article which has studied the influence of the back gate bias on the devices characterized in this work [20]. The devices studied in this paper are transistors SOI Ω-gate nanowire for the widths W=10μm (widest device) and W=10 nm (narrowest device). It concludes that the narrowest channel provides a better electrostatic control

between gate and channel, and its dependence on V_B is much lower when compared to a wider channel. This is shown in the Figure 1-13. (In this paper the V_B is the back gate voltage).

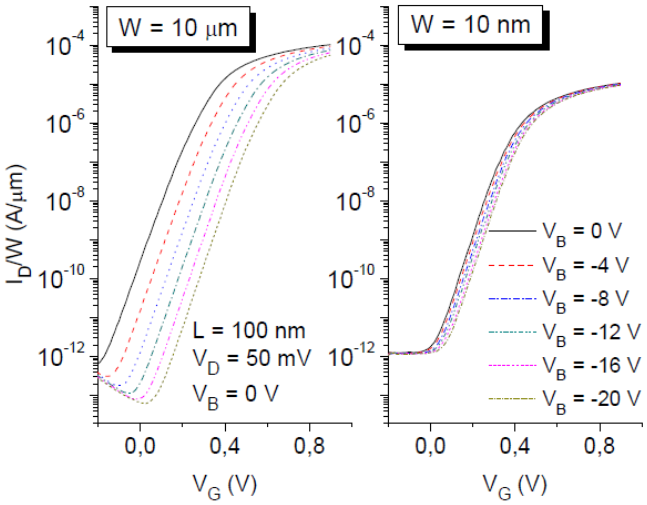


Figure 1-13: Normalized drain current of Ω-Gate NW for channel width of 10µm (A) and 10nm (B) and different back gate bias (V_B) [20].

It can be seen that the V_{th} dependence on V_B for the narrowest channel is smaller due to the strong coupling provided by the gate. As the channel becomes wider, V_{th} turns into more dependent on V_B and starts to be steeper reaching -15.5 mV/V for W = 10 µm and L = 100 nm due to the transversal electric field only. The V_{th} value as a function of V_B are illustrated in Figure 1-14.

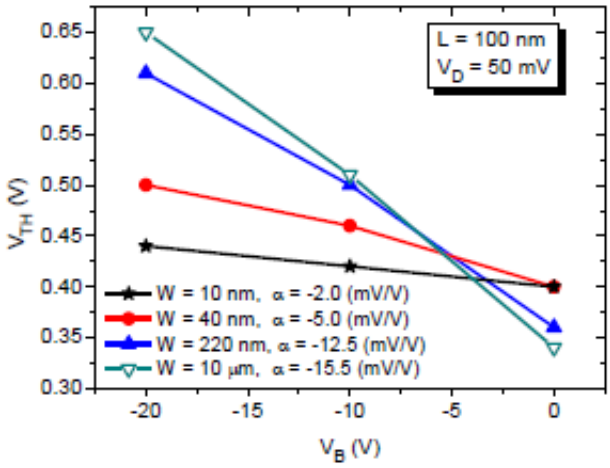


Figure 1-14. Threshold voltage as a function of back gate bias for different channels widths [20].

The electrostatic immunity was observed for the narrowest devices, DIBL does not show any dependence on V_B. However, wider channel devices achieve, in the worst case, a DIBL of around 110mV/V (W = 10 µm at VB = 0 V). The DIBL decreases for high negative V_B values thanks to the inversion channel confinement at gate oxide-channel interface. The DIBL as a function of V_B are illustrated in Figure 1-14.

When the back interface operates near the accumulation, the electrons are expelled to the vicinity of the first interface, which induces a better control over them providing an improvement in some parameters like DIBL.

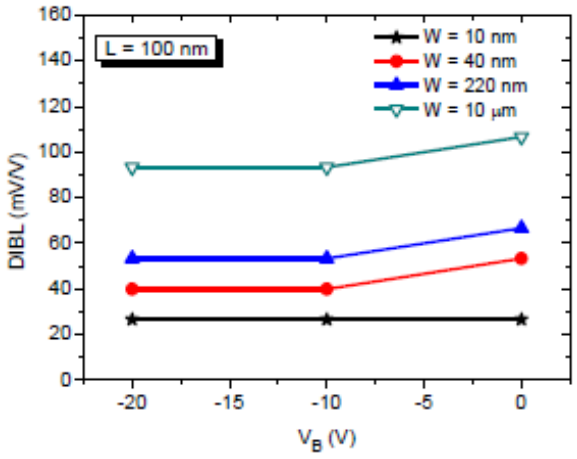


Figure 1-14. Drain Induced Barrier Lowering (DIBL) as a function of back gate bias for FD-SOI transistors with different widths [20].

1.5 Aging Mechanisms and Source Varaibility

Unreliability effects in nano-metric CMOS technologies have become a major concern to analog and digital circuit designers. Both, variability and time-dependent variability related to Random Telegraph Noise (RTN) and Bias Temperature Instability (BTI), will be studied as relevant sources of circuit degradation performances.

In nano-metric technologies, aging phenomena, as for example the BTI, reveal a stochastic behavior that has been linked to charge/discharge of physical defects . Other phenomena, like RTN, are intrinsically stochastic and considered to be caused by similar charge/discharge mechanisms.

1.5.1 Bias Temperature Instability (BTI)

From a practical point of view, it is very important to estimate BTI degradation at the end of expected usage lifetime of devices (and hence circuits and products like microprocessors). The estimation of BTI induced MOSFET parametric degradation is usually done by stressing the device at an accelerated aging condition, using a gate bias (V_G) higher than that used during normal operation while keeping the other contacts grounded, this is called constant voltage stress (CVS). MOSFET transfer I–V characteristics are measured before and after BTI stress, and the difference between pre- and post-stress values is used in order to have a prior knowledge of the degradation in device parameters, such as the threshold voltage V_{th}, the channel mobility, the trans-conductance or subthreshold slope [21].

However, rather than a single value, it is of interest to estimate the time evolution of BTI degradation. In a typical BTI test scenario, transfer I–V measurements are performed by interrupting the stress at certain pre-defined times, the interruptions are usually spaced in logarithmic intervals of time, and the time evolution of BTI induced shift in MOSFET parameters is estimate. The accelerated stress test is performed up to several 1000's of seconds or hours, or sometimes up to days, in wafer-level setup, although sometimes the test can go on for months in package-level setup. The measured time evolution of parametric degradation at accelerated stress condition is then extrapolated to expected end-of-life (e.g., 10 years) and to normal operating V_G by using suitable models.

The most prominent form of BTI when dealing with modern CMOS technologies occurs when the gate of a pMOSFET is biased negatively (in the strong inversion regime), this is called Negative Bias Temperature Instability (NBTI) while the gate is biased positively the phenomenon is called Positive Bias Temperature Instability (PBTI).

1.5.1.1 Negative Bias Temperature Instability (NBTI)

NBTI is a key reliability issue in MOSFETs. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage. However, the very same mechanism affects also n-MOS transistors when biased in the accumulation regime. For example, with a negative bias applied to the gate the NBTI manifests as an increase in the threshold voltage, a degradation of the mobility, drain current and trans-conductance. (See Figure 1-15)

1.5.1.2 Positive Bias Temperature Instability (PBTI)

One disadvantage of the new high-k gate oxide materials is an upcoming effect similar to NBTI. Positive Bias Temperature Instability (PBTI) only works on nMOS transistors, and according to that the stress condition is contrary to NBTI, is applied a positive potential on the gate and a zero potential on source and drain. This lets the threshold voltage drift to higher values [22].

So both NBTI and PBTI weaken the devices over time as is clearly represented in the next Figure 1-15.

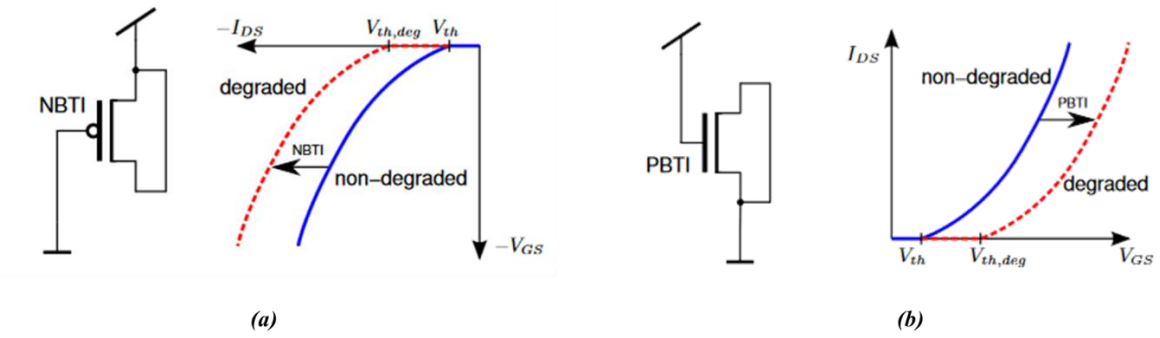


Figure 1-15: (a) Stress conditions and impact of NBTI to pMOS transistors (b) Stress conditions and impact of PBTI to nMOS transistors [21].

1.5.2 Random Telegraph Noise (RTN)

As it was previously explained in the Section 1.2.1, for an ideal MOSFET transistor working in inversion mode with fixed gate ($|V_G| > Vth$) and drain ($|V_{DS}| > 0$) voltages, the current intensity of the I_D channel should be kept constant. However, in the case of MOSFET transistors in nanoscale technologies such as devices implemented with UTBB FD-SOI technology, we observed that some devices show fluctuations in the value of the drain current over time.

Defects at the semiconductor-insulator interface as well as inside the insulator result in non-ideal behavior of metal-oxide semiconductor field-effect transistors MOSFETs, causing variations in the threshold voltage (V_{th}). Since the detailed microscopic nature of these defects is still controversial, a phenomenological classification into inter-face traps

(fast states), border states (slow states, anomalous positive charge), and oxide traps (fixed oxide charge, etc.) is often employed [23].

The fluctuations are due to defects randomly exchanging charge with the substrate. In fact, for modern MOSFET transistors any defect within the oxide is considered a potential edge state, particularly if the interaction with the gate is also taken into account.

As the number of defects in a transistor follow a Poisson distribution, with the mean scaling with the device area, discrete levels can be observed in small-area devices. This form of noise has become known as Random Telegraph Noise (RTN). It is for this reason that the Border States are considered the cause of the RTN [24].

Although conceptually simple, RTN signals can be catalogued according to the number of discrete levels that the signal exhibits. In its simplest form, an RTN signal appears as the random switching of an observable quantity (e.g., voltage, current, impedance), between two discrete levels, as the signal shown in next Figure 1-15 [25].

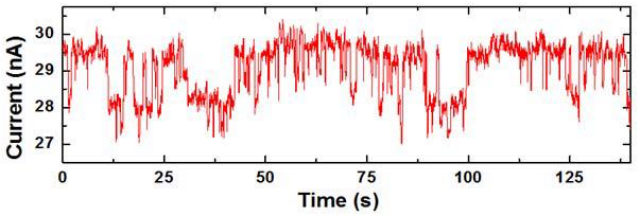


Figure 1-16: RTN signal with two distinct levels of current [25]

Also , there are RTN signals characterized by more than two discrete levels and are labeled as multilevel RTN, this case, the observed multilevel RTN signal results from the superposition of many two-level RTN signals (components), each related to an individual defect.

Chapter 2

Experimental Procedures

This chapter explains the experimental procedure that has been implemented to perform the measurements of the different studies carried out in this master's thesis on the RTN in UTBB FD-SOI devices and their aging. For this, the stress techniques used for the aging and characterization of the fresh samples in order to analyze the RTN which will be explained.

Finally, the instrumentation equipment with which the stresses and characterization have been performed and the programs implemented to perform the processing and analysis of the data obtained, which have given great support to the research performed will be described.

2.1 Characterization Techniques

I_G-V_G

The I_G-V_G characteristic is obtained by measuring the I_G gate current through the oxide when a sweep of the applied gate voltage V_G is carried out, with the rest of the terminals connected to ground plane. Figure 2-1 shows this characteristic for a UTBB FD-SOI without stress. As can be seen, at tensions very low the current through the oxide is practically null, while around 1V it can be seen that the current increases with the applied voltage due to the current through the Direct Tunnel mechanism. The I_G-V_G feature is used to assess the conductive state of the gate dielectric that have the UTBB FD-SOI transistors. This characteristic allows observing the degradation of the oxide, either from the fresh device or after applying an electrical stress that activates the different mechanisms of oxide degradation. The more current through the oxide is observed, the more degradation will have occurred in the oxide. It must be taken into account that the current value is very small, it has a current's magnitude below nano-amperes.

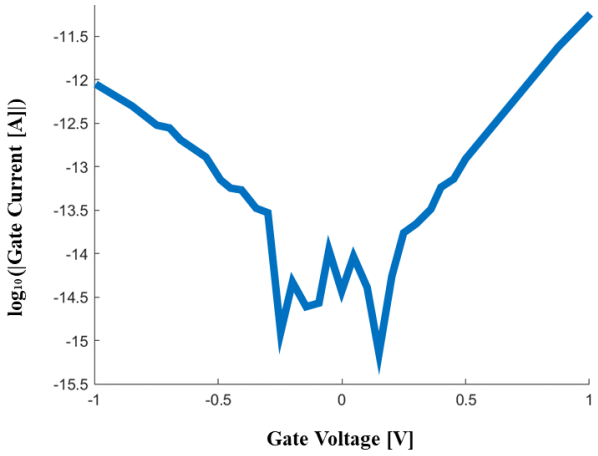


Figure 2-1: I_G-V_G characteristic of a UTBB FD-SOI transistor with dimensions W = 300nm and L = 20nm. At very low voltages the current is null, while at voltages of the order of 1V a certain tunneling current is observed due to the tunneling effect.

The following two I-V features (I_D-V_{DS} and I_D-V_{GS}) describe the MOSFET electrical functionality. These characteristics are obtained through the measured channel current in the drain, depending on the applied gate and drain voltages. Figure 2-2a shows the I_D-V_{GS} feature and Figure 2-2b shows the I_D-V_{DS} feature.

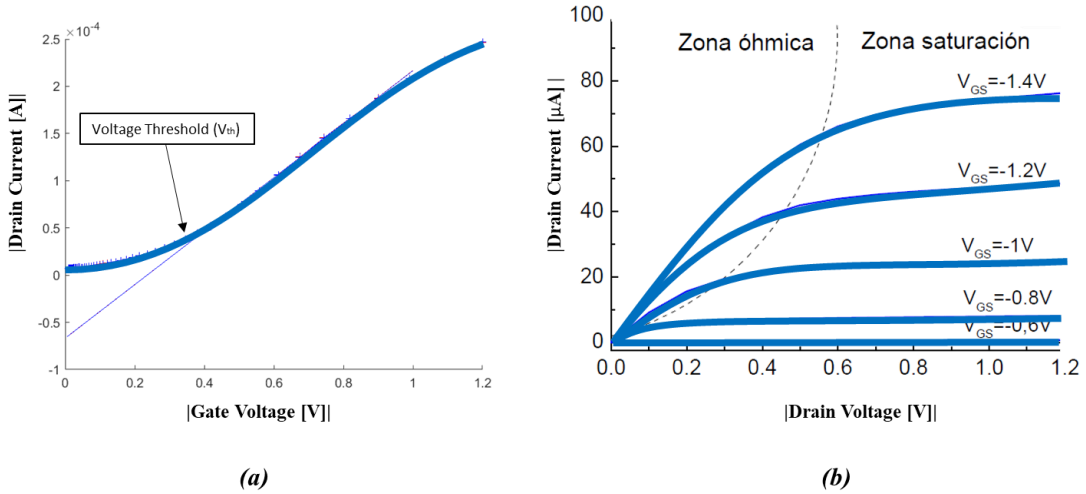
ID-VGS

The I_D-VGS characteristic is obtained by recording the I_D drain current when is carried out a gate voltage sweep (V_G), applying a constant voltage to the drain, with the rest of the terminals connected to ground plane. If the voltage applied to the drain is low (V_{DS} ~ 0.1V), this characteristic is known as the linear zone input characteristic, and allows obtaining the voltage at which there are sufficient electrons in the inversion layer to make a low resistance conducting path between the source and drain, this voltage is known as threshold voltage (V_{th}).

When V_{GS} is less than the threshold voltage V_{th}, the channel is not formed, and consequently, almost no current flows between the drain and the source, indicating that the transistor is in cut-off.

ID-VDS

The I_D-V_D characteristic is obtained by measuring the drain current by sweeping the applied voltage on the V_D drain, when different constant voltages are selected at the gate terminal (V_G), and the rest of terminals are connected to the ground plane. As explained in Section 1.2, this feature shows the three operating regions of the transistor.



(a) *(b)*

Figure 2-2: (a) I_D-V_{GS} characteristic of a UTBB FD-SOI n transistor. The threshold voltage Vth is the voltage V_{GS} at which the transistor begins to drive current. (b) I_D-V_{DS} feature for different V_{GS}. For V_{GS} <V_{th} the transistor is in cut-off, while for V_{GS}> V_{th} the transistor can operate in a linear zone if V_{DS} is low, or can enter saturation if V_{DS} continues to grow.

2.1.1 Stress Techniques

Under the low electric field operating conditions at which UTBB FD-SOI devices currently operate, in a circuit it takes a very long time (months or even years) to observe the impact of degradation mechanisms on the device.

To deal with this, the device is subjected to stress conditions, during various periods of stress (whose duration normally increases exponentially in a range that goes from seconds to hours). These stress conditions consist in subjecting the device to an increased in temperature and /or drain bias and/or gate bias, above their nominal value, during a shorter period of time than operating in normal conditions, called stress time.

This increase in the working conditions reduces the observation times of the effects of degradation and dielectric breakdown to more reasonable periods of time. Furthermore, these results obtained with accelerated tests can also be used later to study the reliability of the devices in real conditions by using laws of extrapolation of results [26].

There are different stress techniques that accelerate the degradation process. However, for this thesis, since we want to evaluate the aging of the UTBB FD-SOI transistor, we have only applied a Constant Voltage Stress (CVS) [27] in order to activate the Positive Bias Temperature Instability (PBTI, explained in the previous Section 1.5.1).

2.2 Measurement Equipment

2.2.1 Wafer Probe Station (WPS)

The experimental measurements realized in this thesis have been carried out by applying stresses directly on wafers, which contain the studied UTBB FD-SOI devices. It has used a wafer probe station (for: CASCADE) to connect the instrumentation transistor.

The wafer prove station is formed by a microscope of high resolution, four tip positioners, the wafer support named chuck and a base station with and X-Y stage to allow moving the chuck, consequently the wafer. The station is shown in (Figure 2-3a).

The four tip precision positioners are micromanipulators located on the base station of the measurement table that support conductive platinum tips, that allow direct access to the terminal contacts of each device inside the wafer.

The chuck significantly reduces measurement-settling, moreover according to the wafer design, it can be used as a contact for the substrate terminal.

With the X-Y stage we can move the wafer in all directions, in this way it allows to place the wafer inside the microscope vision

The wafer prove station is protected from electromagnetic interference by a Faraday box that isolates it from the outside, every time a measurement has been made it has been completely closed.

In the Faraday box there is a connection panel matrix that provides convenient triaxial connection cables to the to the external test equipment's guard, called SMUs (Source Monitor Unit) these are included to the semiconductor parameter analyzer, which allow to apply and record the voltages and currents at each tip.

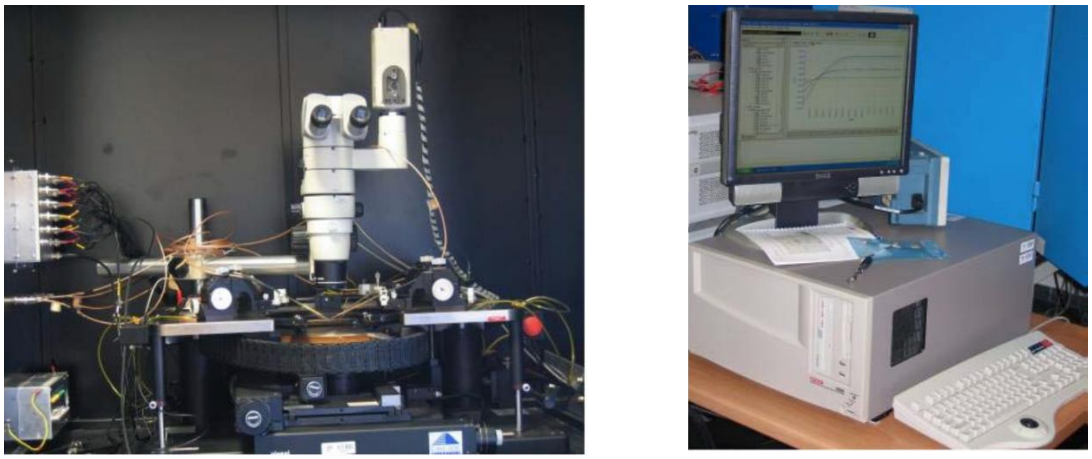
2.2.2 Semiconductor Parameter Analyzer (SPA)

The wafer probe station is monetarized for the semiconductor parameter analyzer Keithley 4200-SCS (Figure 2-3b), and it's used as the measurement equipment in this work.

This semiconductor analyzer allows applying the voltages to the tips, and, at the same time, measure the current. This connection between the SPA and the probe station is implemented by four triaxials cables.

The main software used in the SPA is Keithley Interactive Test Environment (KITE running on S.O Windows XP). It provides a simple user interface where only the configuration parameters of the electrical sequence of values of voltage and current to inject in the device terminals are required.

By properly configuring this instrument, stresses can be automatically performed and the electrical characteristics of the devices studied can be extracted. Finally, it allows to generate a .kdf file with the obtained results. These results include all the characteristic curves of the device and the parameters which define the device perfomance.



(a) (b)

Figure 2-3: Equipment that allows measurements at the level of the wafer, used to perform the stress and characterization of the devices. (a) Tip table that allows measurements to be made at the wafer level. (b) Keithley 4200-SCS semiconductor analyzer with which stresses are applied and voltages and current are recorded

2.3 Analysis and Measurement

The Random Telegraph Noise (RTN) is a random stochastic phenomenon, but the different parameters that characterize it follow certain statistical distributions. In order to find this distributions, for the study of the RTN in the UTBB FD-SOI, it has been carried out a considerable number of measures, which has generated a very large volume of data to process and analyze.

Furthermore, 26 devices have been measured of different scale dimensions under various working conditions and with different measurement procedures. This has been done with the aim of studying the variability and evolution of the phenomenon and the parameters that characterize it.

In order to automate the analysis work, different applications and methodologies have been used to improve the fluency and timing of the analysis tasks. Figure 2-4 shows the outline of the workflow followed after data capture at the end of a measurement with the semiconductor analyzer.

When the measurement data is saved, the Keithley 4200 instrumentation kit software allows you to export the data in a ‘txt’ file called ley Keithley Data File, KDF ’, which contains all the measurement data. The ‘KDF’ format provides all the measurement data

captured during its execution, mixed with the information of the implemented project to carry out the measurements with the semiconductor analyzer. It must be noted that this .KDF format requires prior treatment to adapt the data before analysis.

For the treatment of the '.KDF' file obtained after making the measurement with the semiconductor analyzer, the C ++ programming environment has been used .This treatment consists of collecting and reordering the data from the del KDF 'file in a folder tree, in which the data is stored in various '.txt' files, one for each measured parameter (voltage, current or time). Once the data had been ordered, the MATLAB software was used to analyze them. This part of the process is structured in different functions, which can be activated or omitted depending on what you want to analyze.

Finally, the resulting data from the .txt files have been plotted by a plotting software.

Next Figure 2-4 represents the work flow of the measuring process of the device.

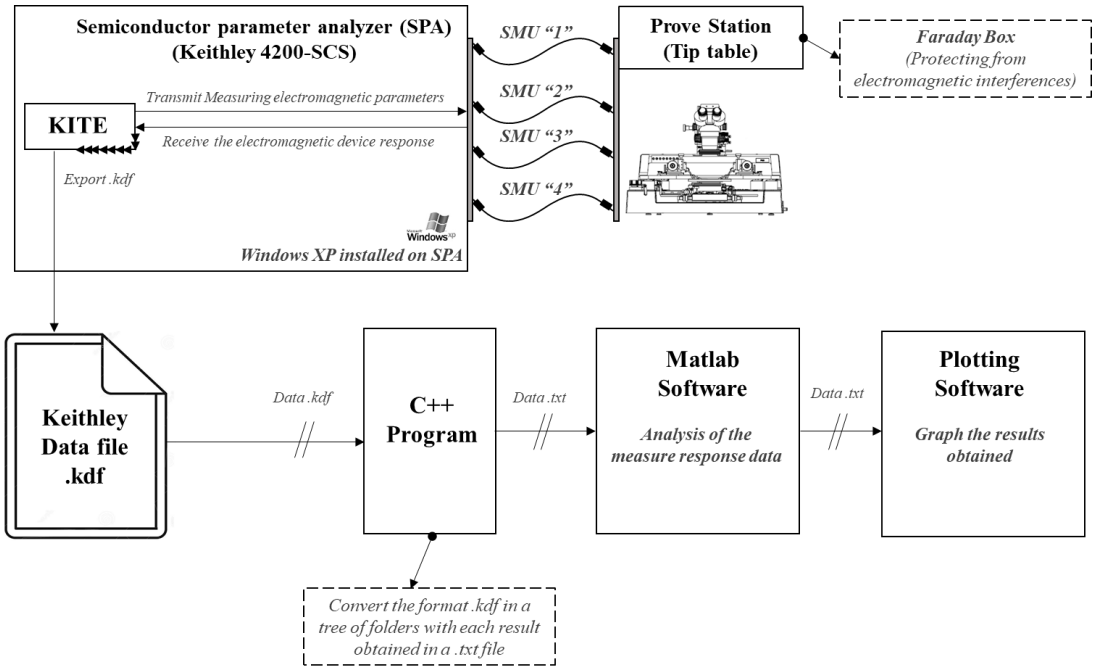


Figure 2-4: Work Flow of the measurement process realized.

2.4 Random Telegraph Noise (RTN) Characterization Tools

Since in recent times RTN has gained much attention as a reliability issue, some research groups focused on RTN data analysis techniques allowing the extraction of the RTN parameters from the measured data, and both qualitative and quantitative methods have been developed. The Weighted Time-Lag Plot method used in this work to analyze the RTN is explained here below.

2.4.1 Weighted Time-Lag Plot

In theory, even with a first glance, we can be more confident on the current fluctuations that have been measured and the existence (or not) of a defect. However, when the background noise is large, defects detection and their parameters extraction can be difficult.

For the RTN signal where background noise is low enough, shown in Figure 2-3, a method is still needed to identify the Random Telegraph Noise (RTN). To overcome this, was proposed the Time Lag Plot (TLP) is proposed. TLP can be drawn by simply plotting points in an x-y plane, where x is set to i-th sampled data, and y to the next (i+1)-th sampled data. With the TLP method is easily count the number of multiple traps, the result is shown at Figure 2-2 [28].

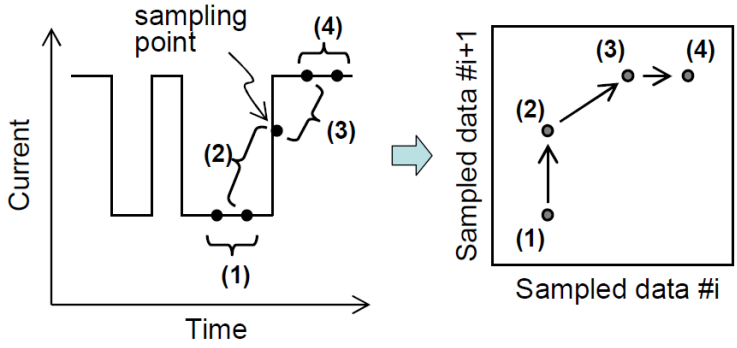
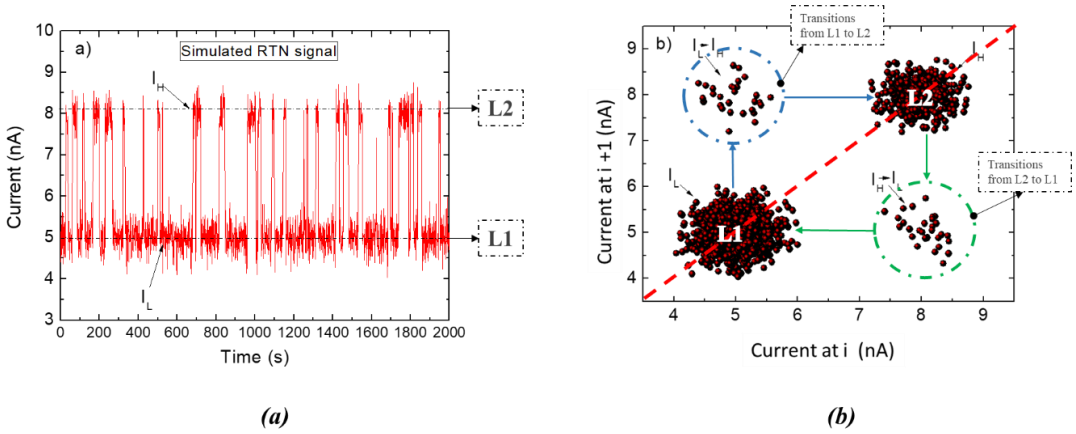


Figure 2-2: Explanation of Time Lag Plot (TLP). TLP visualizes autocorrelation of waveforms [28].



(a) *(b)*

Figure 2-3: a) waveform of a simulated simple two states RTN signal without background noise and b) Time Lag Plot (TLP) for simple two state RTN [29].

However, if the background noise (i.e., noise that comes from measurement equipment or other sources inside the device under study) is relevant when compared with the current/voltage measurements of the Random Telegraph Signals, the precise defects detection and their parameters extraction can be difficult.

In the next Figure 2-4 [29], is shown a simulated RTN signal with background noise added.

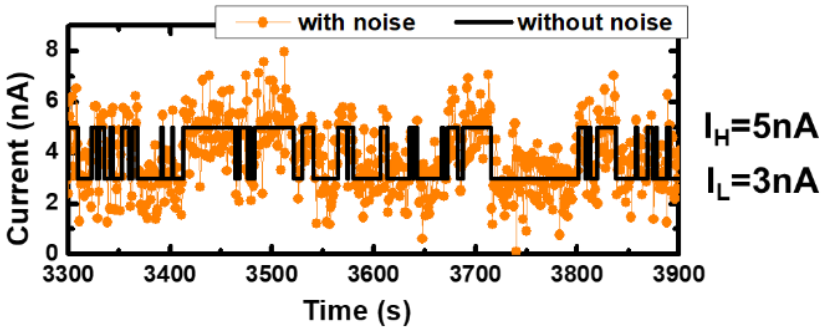


Fig 2-4: A two-level simulated signal RTN generated by one defect with and without background noise. The sample rate considered was 1 s and the number of points in the RTS 10.000 [29].

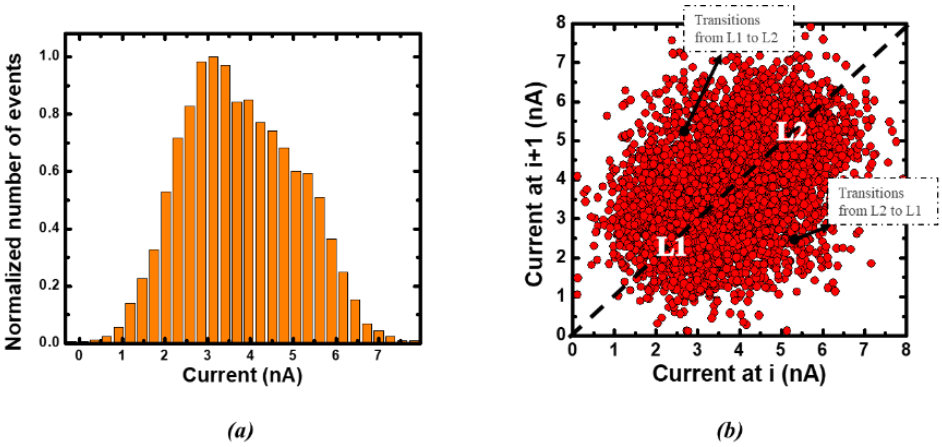


Figure 2-5: (a) Histogram graph representing the current probability distribution obtained directly from the RTS; (b) TLP of the RTN; the background noise hides the current levels and transition regions (L1, L2 and the transition regions) [29]

The RTN signal histogram graph (Figure 2-5a, [29]) cannot help, because the two peaks associated with I_L (corresponding to current level 1) and I_H (corresponding to current level 2) are hidden by the background noise. In the same way, in the Figure 2-5b is shown the TLP constructed from the RTN signal trace. It is impossible to distinct any regions because, these are again overlapped because of the background noise.

For this, a better new method called Weighted Time Lag Method (w-TLP) was developed easily implementable and robust even when this background noise is large [25].

The weighted time lag method presented here tries to extend the TLP by minimizing the effect of the noise in the RTS and allows more accurate defect parameters extraction. We depart considering a point of the plotted TLP with coordinates (I_i, I_{i+1}). For this point we define the ϕi function as Equation 2-1:

$$\varphi_i(x,y) = \frac{1}{2\pi\alpha^2}\exp\left(\frac{-[(I_i-x)^2+((I_{i+1}-y)^2)]}{2\alpha^2}\right) \qquad \textit{Equation 2-1}$$

Where 'x' and 'y' are the coordinates of the space where the TLP is considered. Note that 'ϕ_i' is a normal bivariate distribution with standard deviation 'α' and correlation coefficient '0'. Then, 'ϕi' (x, y) represents the probability that the point with coordinates (I_i, I_{i+1}) corresponds to a level or to a transition in the location (x,y) of the TLP space.

After the ‘ϕi’ definition, we define the weighted time lag function ‘Ψ’ as Equation 2-2 large [25]:

$$\Psi(x,y) = K\sum_{i=1}^{N-1}\varphi_i \qquad \textit{Equation 2-2}$$

being ‘K’ a normalization constant chosen to get the maximum value of ‘Ψ’ equal to ‘1’ and ‘N’ the number of points in the RTS. If ‘Ψ’ is plotted for few points (Figure 2-6) two local maximums are roughly defined whose values are closer to I_L and I_H.

To understand why these peaks are revealed, we have to note that the contribution of each point of the TLP, which results in ‘Ψ’, is weighted by the distance between the position of this point and (x,y). Therefore, the function ‘Ψ’ takes higher values in the most populated regions of the TLP. In the diagonal of the w-TLP of Figure 2-6 two well defined local maximums can be detected (Ψ_L and Ψ_H) in the positions 3.05nA and 4.89nA. These values correspond to the two levels of the RTS.

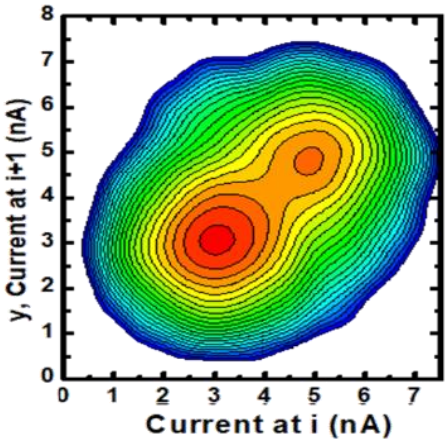


Figure 2-6: Representation of Log(Ψ) using the full RTN trace [25].

Then, the construction of the function ‘Ψ’ is valid to detect levels of the RTS that cannot be determined from conventional methods, such as the RTS histogram or the TLP, when the background noise is relevant.

2.5 Samples Description

The experiments of this work have been performed on Ω-gate Nano Wire (NW) SOI transistors (P and N type) fabricated at CEA-LETI (Grenoble, France) in a 22nm process. The gate stack is composed by HfSiON/TiN (Hf-based high-k/metal gate stack) with an EOT (layer equivalent oxide thickness) = 1.3 nm in order to suppress detrimental SCE and gate leakage and the height (H_{NW}) is 11 nm.

The devices are featuring buried oxide thickness of t_{ox} = 145nm (ultra-thin body, UTB) have been considered. All the devices studied have wides comprising from 300nm to 10 µm with channel lengths ranging from 10nm to 10µm. The cross section of these devices is shown in Figure 2-7 [20].

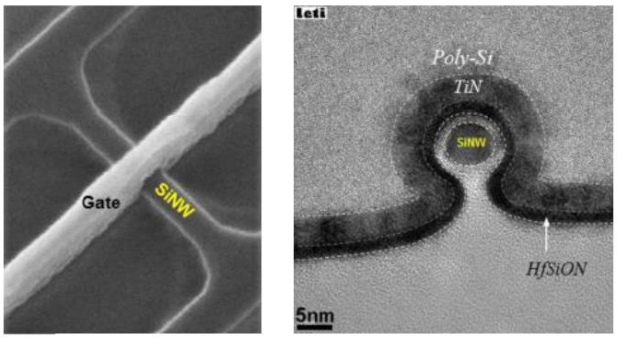


Figure 2-7: (Left) SEM and (right) cross-sectional TEM images of SOI Omega-Gate Nanowire [20]

Chapter 3

Characterization of Fresh MOSFETS

In this chapter are studied the fresh characteristics of the fresh UTBB FD-SOI devices, including the extraction of their threshold voltage and mobility. Moreover, their dependence on the channel dimensions was also analyzed.

3.1 Fresh characteristics of FD-SOI Devices.

The fresh characterization of the presented UTBB FD-SOI devices consists in the measurements of I_G-V_G, I_D-V_{GS} and I_D-V_{DS} curves.

3.1.1 Short Channel N-type Transistors (L=10nm)

Figure 3-1 show the fresh characteristics of a UTBB FD-SOI N-type transistor with a channel length of 10nm and a channel width of 300nm split in 10 channel of 30nm. As can be seen in the I_G-V_G (Figure 3-1a), the current across the thin oxide layer at 1V is around 10pA. Regarding to the I_D-V_G characteristic (Figure 3-1b), it can be observed that subthreshold region presents certain slope and drive current value at 0V is 30µA approximately. This indicates that the V_{DS} applied during this characteristic (100mV) is large enough to produce current even below the threshold voltage due to the short channel length (10nm). For the I_D-V_{DS} curves (Figure 3-1c), the short channel effect on the drive current in the saturation region is also clearly appreciated.

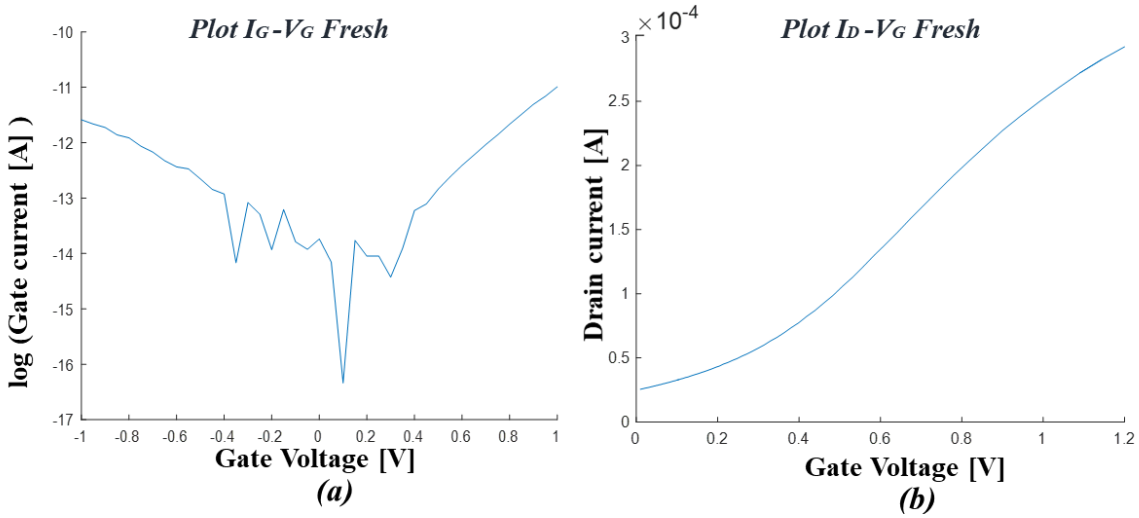


Figure 3-1: (a) I_G-V_G and (b) I_D-V_G, characteristics of a fresh UTBB FD-SOI N-type transistor with channel Length 10nm and channel width of 300nm split in 10channel of W=30nm.

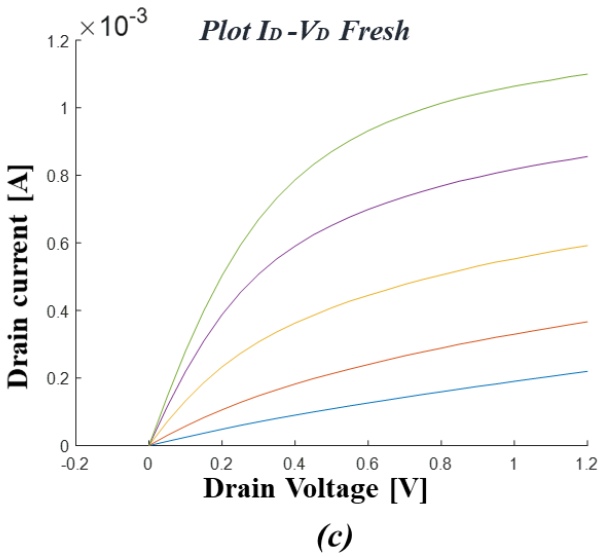


Figure 3-1: (c) I_D-V_{DS} characteristics of a fresh UTBB FD-SOI N-type transistor with channel Length 10nm and channel width of 300nm split in 10channel of W=30nm.

3.1.2 Long channel N-type transistors (L=10.000nm)

To compare the previous characteristics of a short channel transistor with the characteristics of a largest one, Figure 3-2 shows the characteristics of a UTBB FD-SOI N-type transistor with the same channel width of 300nm, but with a channel length of 10µm, which is 1000 times longer than before. As observed, for the I_G-V_G current at 1V is 10nA, which is 3 orders of magnitude higher than before, according to the channel area dependence of the tunnel current across the gate oxide. For the I_D-V_G, subthreshold region presents lower current values and remains almost flat from 0V to V_{th} ~ 0.4V, indicating no short channel effects. Furthermore, the drive current in the saturation region in the I_D-V_{DS} curves do not exhibit channel modulation effects.

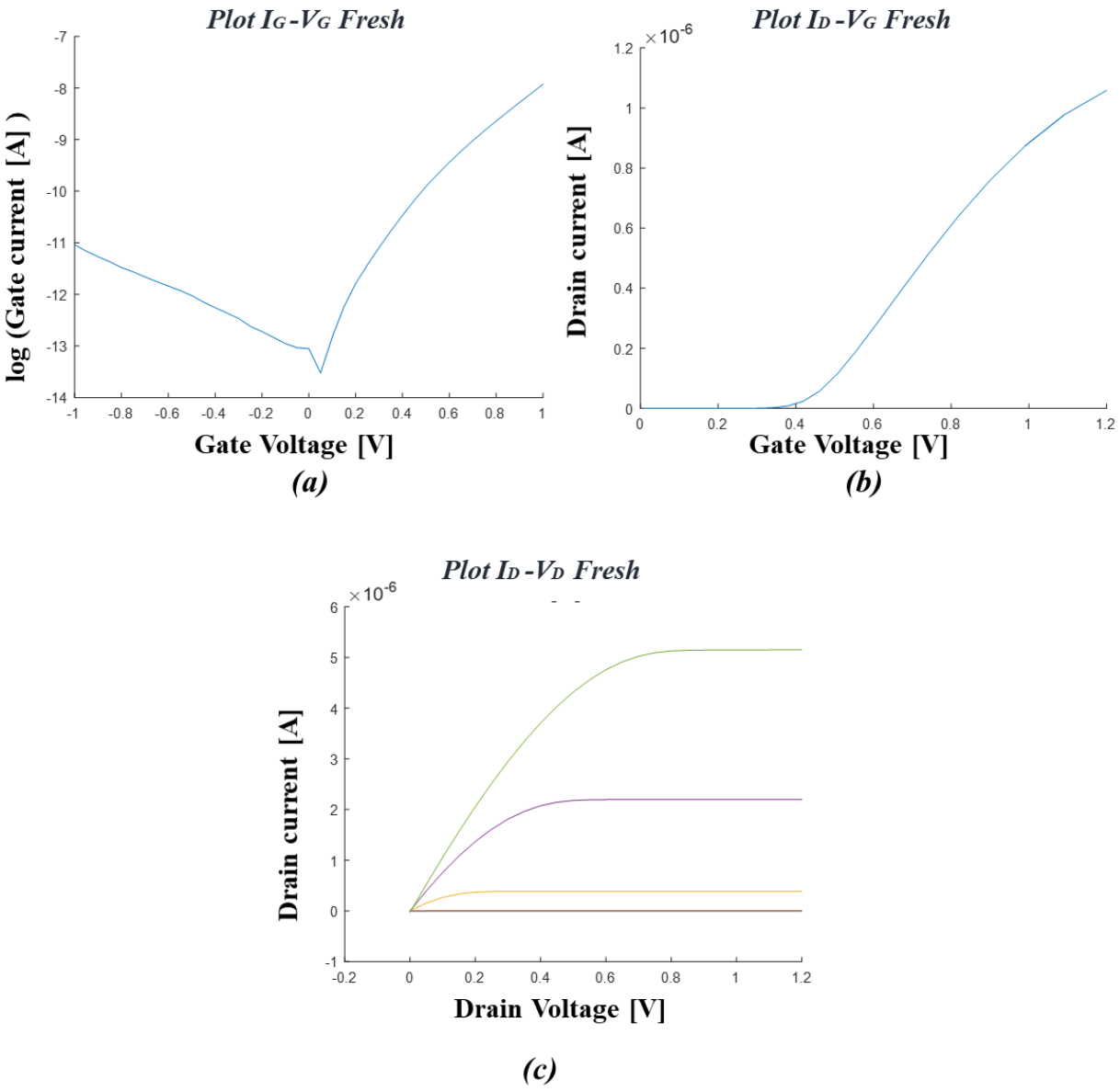


Figure 3-2: (a) I_G-V_G, (b) I_D-V_G, and (c) I_D-V_{DS} characteristics of a fresh UTBB FD-SOI N-type transistor with a channel width of 300nm split in 10 channels, and a channel length of 10µm.

3.2 Threshold Voltage and Mobility Extraction.

In order to extract the threshold voltage (V_{th}) and mobility device parameters, an automatic process was implemented using Matlab. The method used was based on the maximum slope of the I_D-V_{GS} characteristic over the subthreshold region. The tangent line in the maximum slope point is extrapolated and the projected point to the x-axis corresponds to the threshold voltage (V_{th}). Device mobility is related with this maximum slope. Other simpler methods can be used, as a level current. However, as can be seen in

Figure 3-1 and 3-2, it could be quite difficult define a common level for all I_D-V_{GS} due to the large difference between the curves of the 10nm and 10µm devices. Figure 3-3 shows the graphical representation of the method used. The blue line corresponds to the fresh I_D-V_G of a 40nm device (width of 300nm split in 10 channels, and a channel length of 40nm), and the green line is the tangent line to the maximum slope point of the curve over the subthreshold region. In this case, the threshold voltage value obtained is 0.385V.

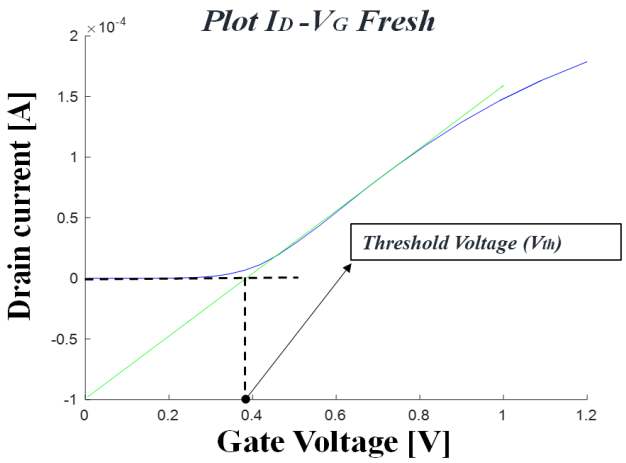


Figure 3-3: I_D-V_G characteristics of a fresh UTBB FD-SOSI N-type transistor with a channel width of 300nm split in 10 channels, and a channel length of 40nm.

The Threshold Voltage (V_{th}) is the intersection voltage point between the green tangent line and the zero drain current (I_D=0A), and the maximum slope of this green line is the mobility. Both parameters were extracted with Matlab.

3.3 Channel Dimensions Dependence

In order to analyze the transistor characteristics dependence on the device channel dimensions, in this section different fresh transistors with different width and length are studied. As can be seen in the next Figure 3-4, the tunnel current through the dielectric stack increases proportional with the device area.

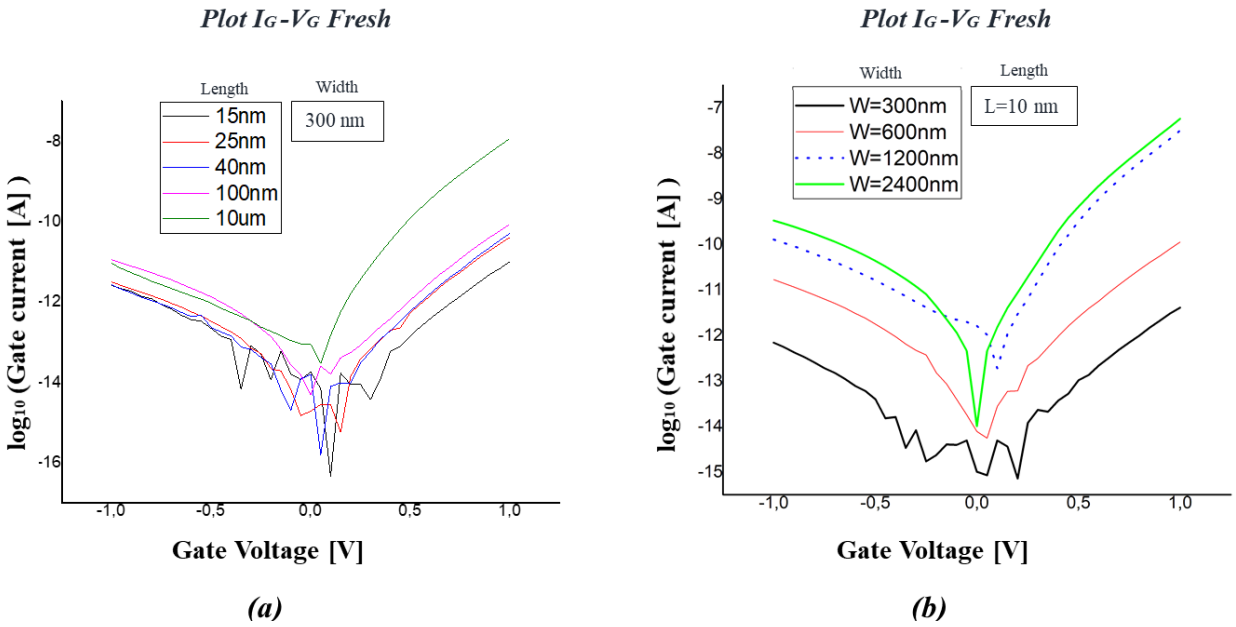


*Figure 3-4: Fresh I_G-V_G characteristics of UTBB FD-SOI N-type transistors. (a) The width is 30nm*10channels for all devices, while the length ranged from 15nm to 10µm. (b) The length was 10nm for all devices, while the width ranged from 300nm to 2400nm.*

In the Figure 3-5 it can be seen how the drive current increases as length is reduced. For L=25nm drive current reaches 230µA. On the other hand, the threshold voltage decreases with the channel length as can be appreciated in the Figure 3-5 around 0.3V.

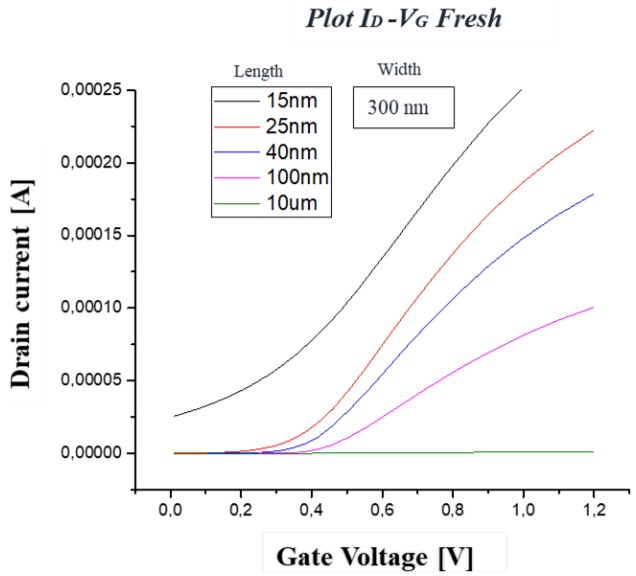


*Figure 3-5: Fresh ID-VG characteristics of the UTBB FD-SOI N-type transistors of Figure 3-4. The width is 30nm*10channels for all devices, while the length is ranged from 15nm to 10µm.*

As observed, differences due the channel length are also observed in the subthreshold region where the off state current increases as the length is reduced. It is more significant in the case of L=15nm where the current around 0V is larger than 20µA.

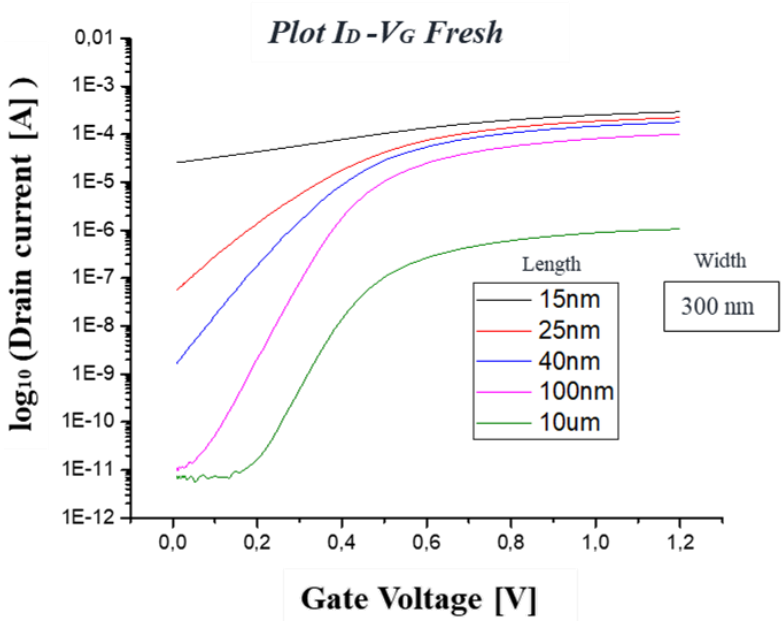


Figure 3-6: Fresh I_D-V_G characteristics from the Figure 3-5 represented with Y-axis in log scale.

Next Figure 3-7 shows the threshold voltage value of the previous samples as a function of the channel length. For intermediate values of L (from 25 to 100nm), threshold voltage linearly depends on the channel length. However, for the cases of L=15nm and L=10µm, this dependence is not followed. It is because the maximum slope method must be treated with care.

In the case of the short channel (L=15nm), the shape of the curve produces a V_{th} of 0.13V with this method, but observing the Figure 3-5 it could also be located around 0.3V. Something similar happens in the case of L=10µm, but in the opposite direction. In this case, the low slope of the curve in a combination with the extraction method used results in a lower value (0.44V) than the one you can extract from Figure 3-5 (0.6V).

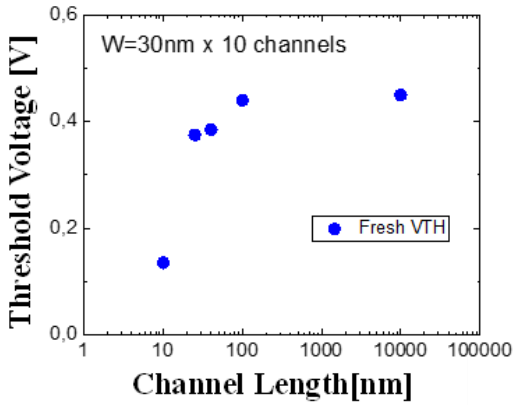


*Figure 3-7: Threshold voltage of the measured devices as a function of the channel length. The results are obtained with the maximum slope method. The devices are the same from the previous Figures 3-4, 3-5 and 3-6. UTBB FD-SOI N-type transistors, the width is 30nm*10channels for all devices, while the length is ranged from 10nm to 10µm.*

3.3.1 Study of the Back Gate Biasing

In the next Figure 3-8 it can be seen how the back gate voltage doesn't seems to affect to the drain current. It doesn't affect independently of the area of the device measured.

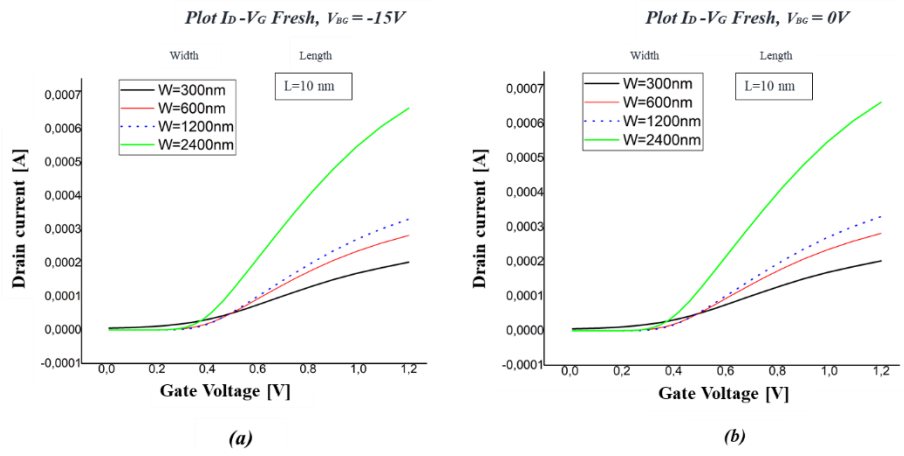


Figure 3-8: Fresh I_D-V_G characteristics of UTBB FD-SOI N-type transistors. The selected devices have all the same length L= 10nm, while the width is ranged from 300nm to 2400nm. (a) Fresh I_D-V_G characteristics with a V_{BG}=-15V (b) Fresh I_D-V_G characteristics with a V_{BG} =0V

In order to study the effect of back gate on the transistor characteristic, the curves shown in figure 3-8 for the narrowest and the widest devices are analyzed in more detail. Figure 3-9 shows the same than the previous characteristics but focusing in the widest (Figure 3-9a) and narrowest (Figure 3-9b) devices measured. Here, in these following graphs it

can be clearly seen how the drain current curve is the same when is applied a back gate voltage V_{GB}=-15V.

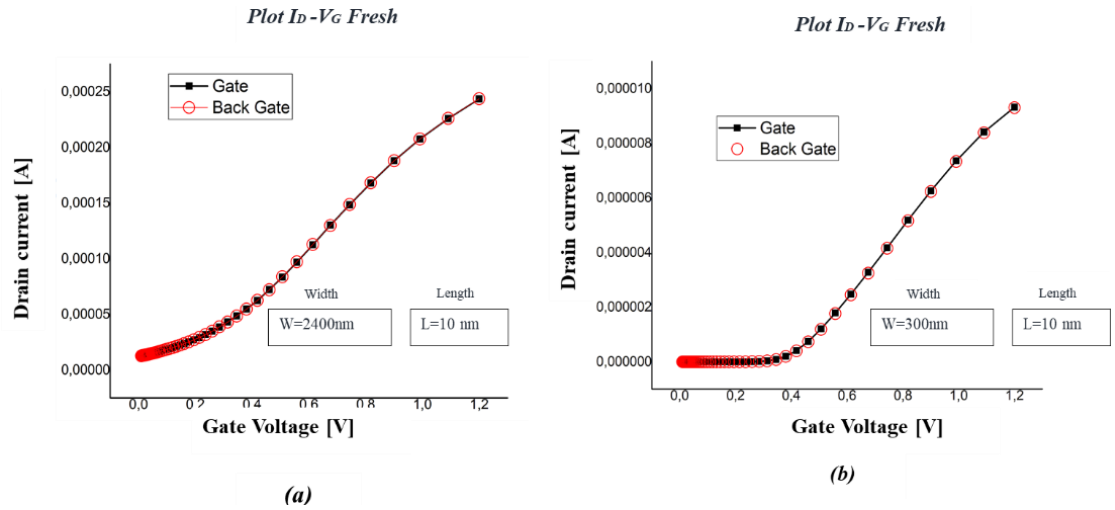


Figure 3-9: Fresh I_D-V_G characteristics of UTBB FD-SOI N-type transistors, with and without Back Gate Voltage applied, V_{BG}=-15V. The selected devices have all the same channel length L= 10nm and a width of (a) W=2400nm and (b) W=3000nm

Chapter 4

Experimental RTN Results

In this chapter the Random Telegraph Noise (RTN) has been studied in the UTBB FFD-SOI transistors. In order to carry out with this study, the w-TLP method has been used.

This sample-weighted approach of the conventional TLP method allows to identify the RTN levels clearly as populated regions in the diagonal of the TLP space, while populated regions outside the diagonal are related to the transitions between states.

When the device is not affected by traps, a single cloud appears in the TLP space; the appearance of a constellation with two lobes indicates the presence of a single-trap a three-lobe constellation, reveals the existence of three predominant current levels (two traps, and when multiple current levels appear, a spread lobe indicates a multi-trap situation.

For a complete analysis of the RTN in the studied devices, different experiments were done. Then, the next set of characterizations with three different gate and back gate biases were defined:

i. [V_{G1}=0.5V; V_{BG1}=0V**]** **ii. [**V_{G2}= 1V; V_{BG2}=0V**]** **iii. [**V_{G3}= 1V; V_{BG3} = -15V**]**

To study the RTN as a function of the device channel dimensions, the previous three characterization biases were applied to different devices with different channel lengths (ranged from 10nm to 10µm) and widths (ranged from 300nm to 10µm).

4.1 RTN on Short Channel Devices (W=300nm, L=10nm)

Figure 4-1 shows the three mentioned characterizations of the RTN (at different biases) for the smallest channel device (W=300nm and L=10nm).

For the RTN characterization (V_{G1}=0.5V and V_{BG1}=0V), at Figure 4-1a two different levels are detected. However, when analyzing Figure 4-1b, the signal does not exhibit a clear RTN due the progressive variation trend. Nonetheless during the second bias RTN characterization (V_{G2}=1V and V_{BG2}=0V) fluctuations between two levels clearly appear despite de large noise of the signal (Figure 4-1d). It is clearly observed in Figure 4-1c, where two peaks appear in the diagonal of the w-TLP.

Therefore, trapping and detrapping of a single defect has been detected during this experiment. Moreover, transitions between levels are also observed in Figure 4-1c out of the diagonal that means many transitions between these two levels are registered during the stress time.

Finally, for the third RTN characterization (V_{G3}=1V and V_{BG3}= -15V), in the Figure 4-1e, the same defect than before is captured because the same levels of current are registered (levels are located in the same value of current). However, peaks look less clear than during the second characterization (V_{G2}=1V and V_{BG2}=0V).

Compering the case with / without a V_{BG} = -15V, it seems that RTN registered is very similar, suggesting that in this small channel fresh device the back gate doesn't affect too much.

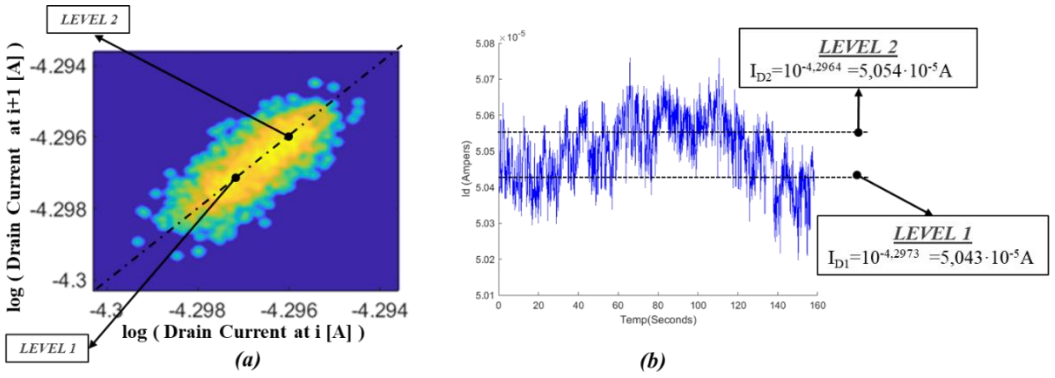


Figure 4-1: (a) Device N3W with two lobes (levels) in the w-TLP constellation, as result from the single active trap, and (b) its drain current trace, when the voltages applied in (a) and (b) are V_{G1}= 0,5V and $V_{BG\,1}$= 0V. W =300nm, L=10nm.

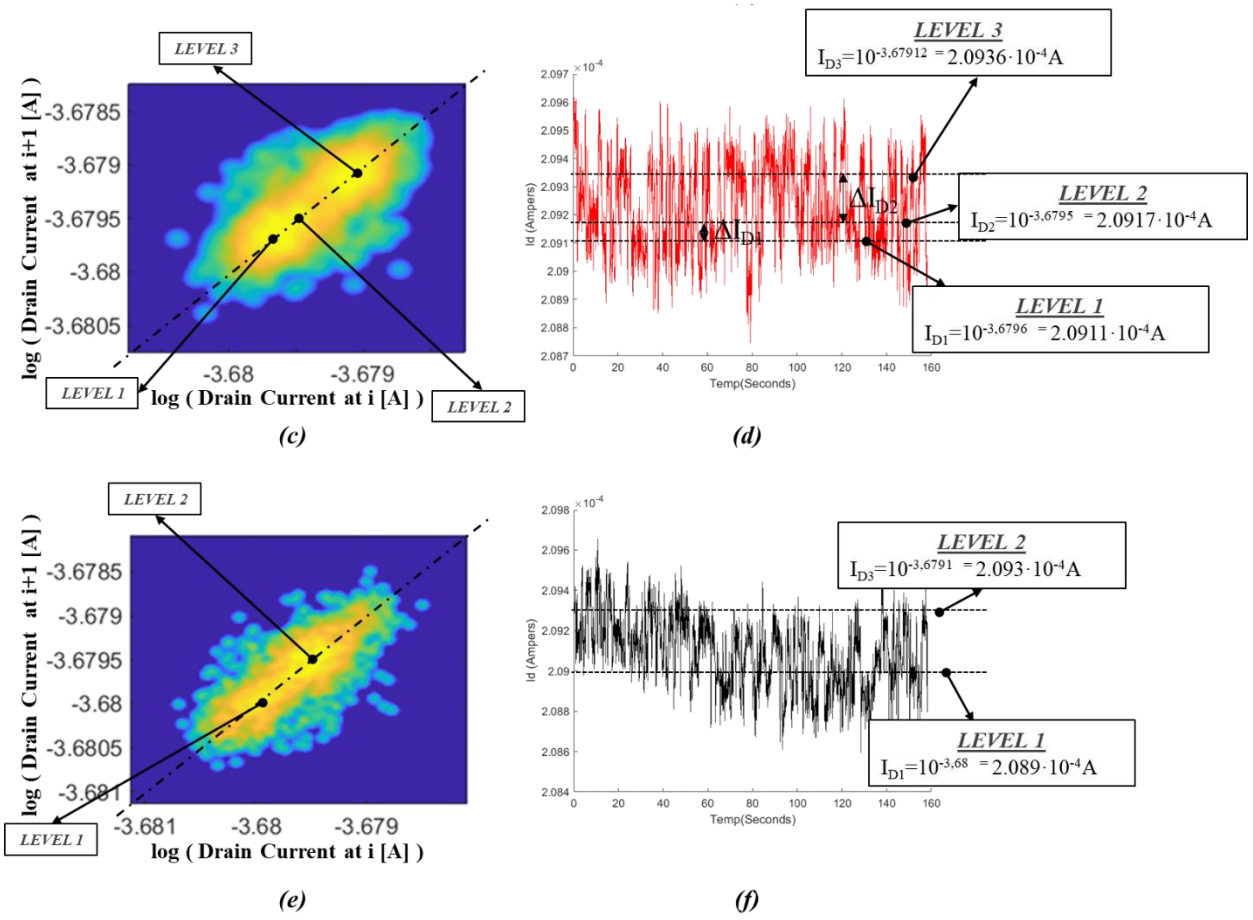


Figure 4-1: (c) Device N1W with a three-lobes (levels) in the w-TLP constellation, identifying the characteristic signature of two traps, and (d) its drain current trace, when the voltages applied in (c) and (d) are V_{G2} =1V and V_{BG2} = 0 V. (e) Device N1W with two lobes (states) in the w-TLP constellation, as result from the single active trap, and (f) its drain current trace of the device. Voltages applied in (e) and (f) are V_{G3} =1V and V_{BG3} = -15 V. All the devices measured have these dimensions: W =300nm, L=10nm.

4.2 RTN on Long Channel Devices (W=300nm, L=10µm)

Figure 4-2 shows the three characterizations obtained in a fresh device with W=300nm and L=10µm, which is much larger than the previous sample. As it has observed in Figures 4-2a (applied V_{G1}=0.5V and V_{BG1}=0V), 4-2c (applied V_{G2}=1V and V_{BG2}=0V), and 4-2e (applied V_{G3}=1V and V_{BG3}=-15V), just one peak in the diagonal is observed. Moreover, the time domain traces (Figures 4-1b, 4-2d and 4-2f) are too noisy and do not show fluctuations between discrete levels.

When comparing this experiment with the previous in a smart channel device, RTN seems to be less detrimental in large devices. However, experiment are not enough to conclude this result. All the w-TLP is lacking of RTN signature, only thermal noise is reflected.

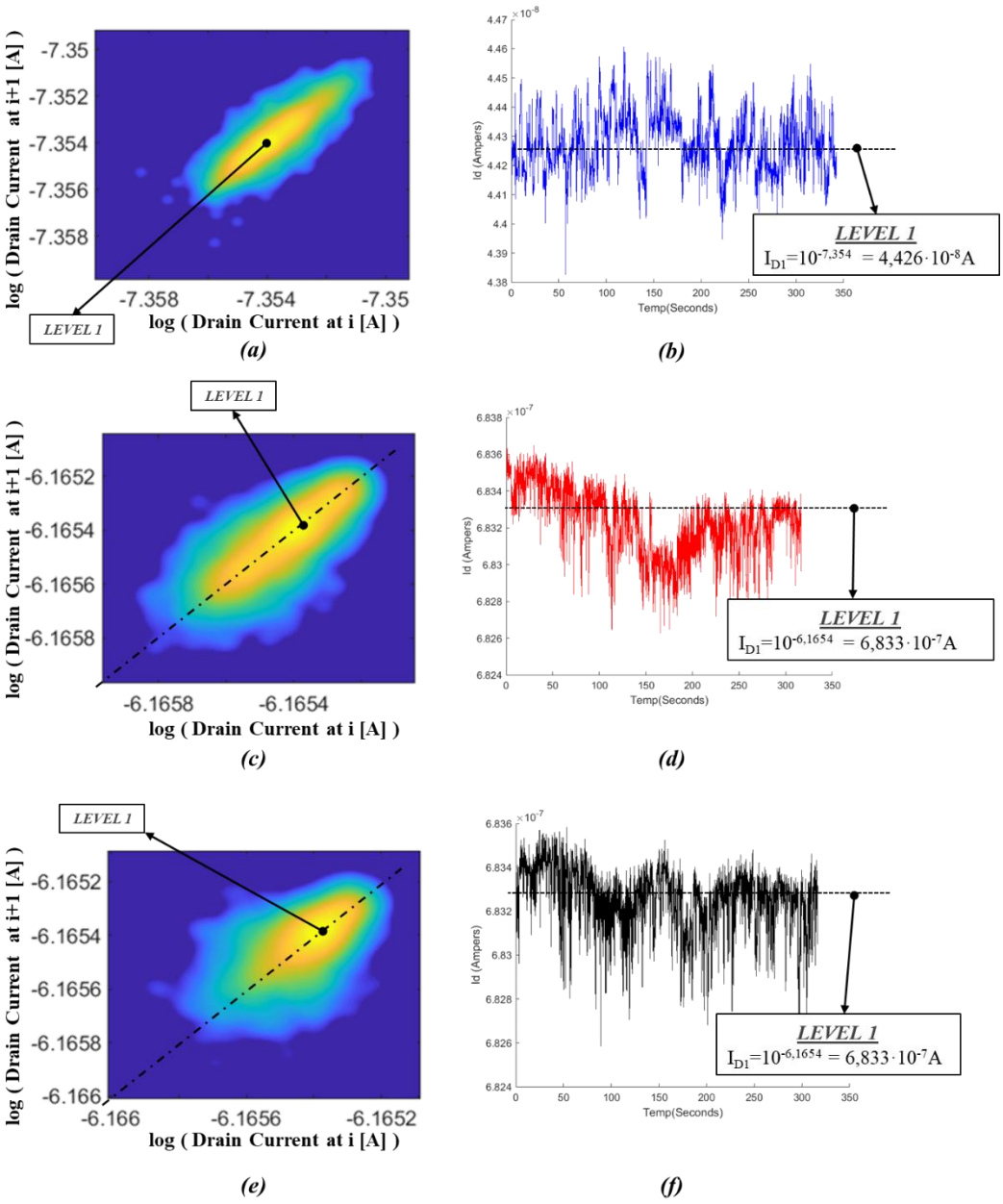


Figure 4-2: (a) W-TLP of the device N14 and (b) its drain current trace, when the voltages applied in (a) and (b) are V_{G1}= 0,5V and V_{BG1} =0V. (c) W-TLP of the device N14 and (d) its drain current trace, when the voltages applied in (c) and (d) are V_{G2} =1V and V_{BG2}= 0 V. (e) W-TLP of the device N14 and (f) its drain current trace, when the voltages applied in (e) and (f) are V_{G3} =1V and V_{BG3}= -15 V. The device measured here is N14 and have the next dimensions: W=300nm, L=10µm.

4.3 RTN on Wide Devices (W=10 µm, L=10nm)

Figure 4-3a (applied V_{G1}=0.5V and V_{BG1}=0V), 4-3c (applied V_{G2}=1V and V_{BG2}=0V) and 4-3e (applied V_{G3}=1V and V_{BG3}= -15V) show the w-TLP of a fresh device with W=10µm and L=10nm, being the largest W/L ratio studied in this part. Therefore, is in this case of channel dimensions where the largest drive current is registered during the RTN characterization. As observed, only one peaks is observed.

When observing the drive current registered during the characterizations, Figures 4-3b (V_{G1}=0.5V and V_{BG1}=0V), 4-3d (V_{G2}=1V and V_{BG2}=0V) and 4-3f (applied V_{G3}=1V and V_{BG3}= -15V) no fluctuations are registered between discrete levels. On the contrary, progressive and noisy trend is observed, especially when V_G=1V, suggests that some degradation is happening due the set of voltages applied for the characterization.

On the other hand, a resolution problem is detected during the third characterization where V_{G3}=1V and V_{BG3}= -15V, see the Figures 4-3e and 4-3f. It is caused by the current values (~5mA) which are much larger than the variations caused by the noise (~50nA). It causes this discrete mesh of points in the w-TLP. In order to control the resolution for the characterization of the RTN, this parameter was fixed (auto is the default option). However, it didn't solve this problem completely, and it occurred in few measurement as observed in section 4.5.

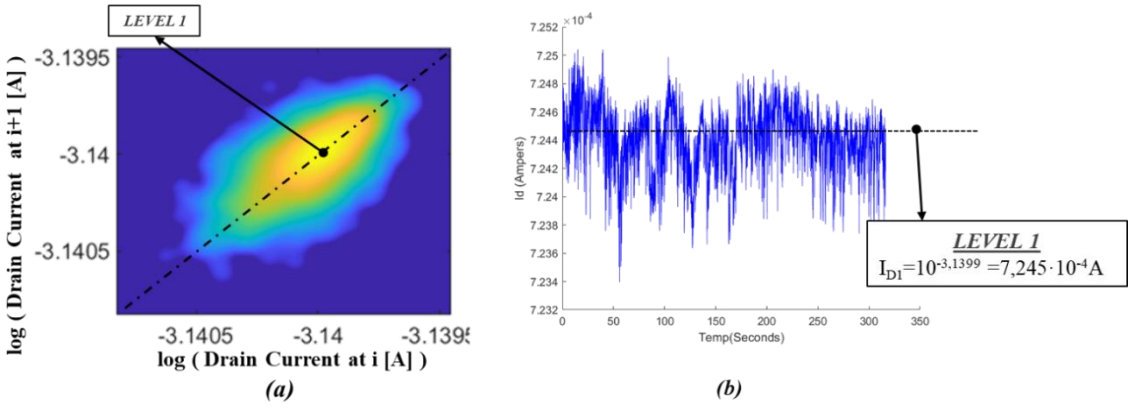


Figure 4-3: (a) W-TLP of the device N2 and (b) its drain current trace, when the voltages applied in (a) and (b) are V_{G1} = 0,5V and V_{BG1}=0V. W =10µm, L=10nm.

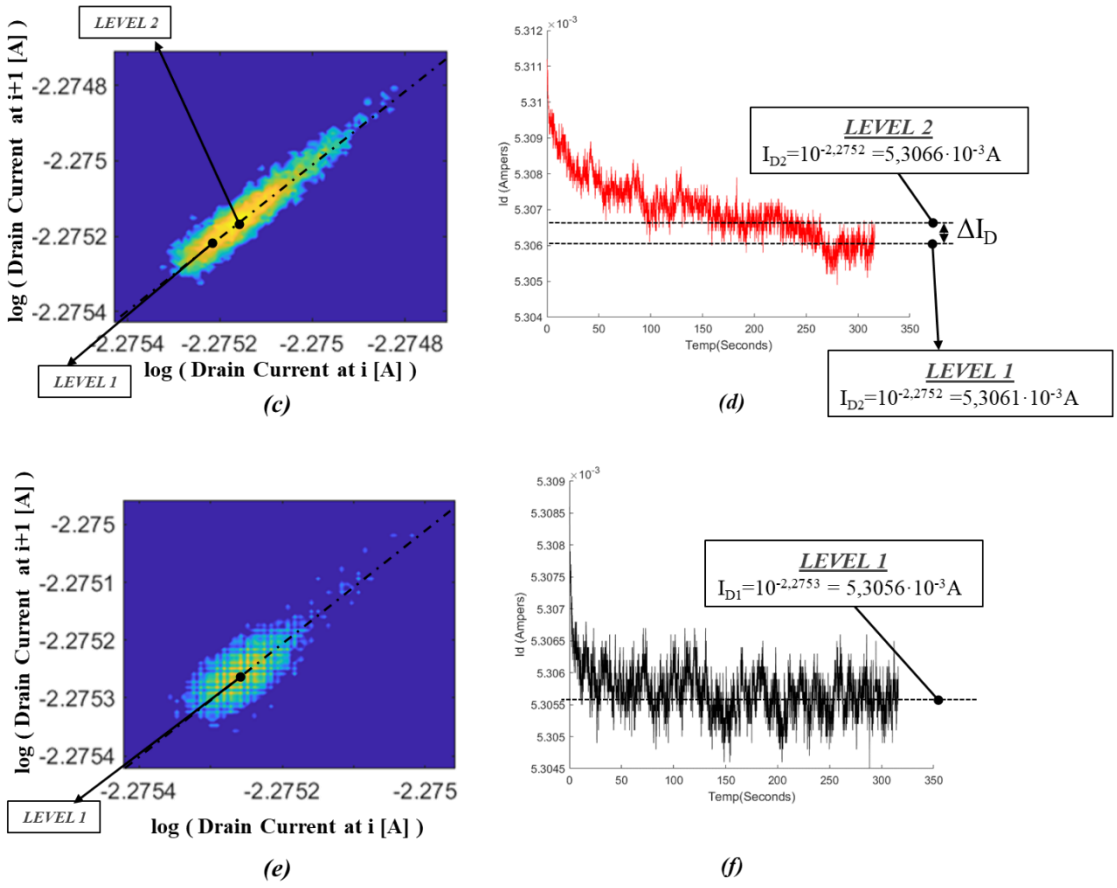


Figure 4-3: (c) W-TLP of the device N1 and (d) its drain current trace, when the voltages applied in (c) and (d) are V_{G2} =1V and V_{BG2}= 0 V. (e) W-TLP of the device N1 and (f) its drain current trace, when the voltages applied in (e) and (f) are V_{G3} =1V and V_{BG3}= -15 V. All the devices measured have these dimensions: W=10µm, L=10nm.

Figure 4-4 show the RTN analysis of the experiment done in a fresh device with W=10µm and L=50nm. As observed in Figure 4-4a (V_{G1}=0.5V and V_{BG1}=0V), two peaks are clearly observed in the w-TLP, and when looking Figure 4-4b, multiple transitions between two clear and stable levels are observed. Even more, transitions are clearly characterized out of the diagonal.

However, when doing the second RTN characterization (V_{G2}=1V and V_{BG2}=0V), these peaks are not too clear. And this gets worst in the third characterization (V_{G3}=1V and V_{BG3}= -15V), were the trace is just noise.

Again, some progressive reduction is observed when we apply a V_{BG}= -15V (Figure 4-4f). So that, for small channel devices (W=10nm) the voltages applied seem to not produce degradations, but in the case of large channel (L=10µm) length the V_G=1V and V_{DS}=100mV, it suggest the idea that the soft degradation in the channel current, supposedly by the Hot carrier injection (HCI) aging mechanism activated during the RTN characterization, is produced.

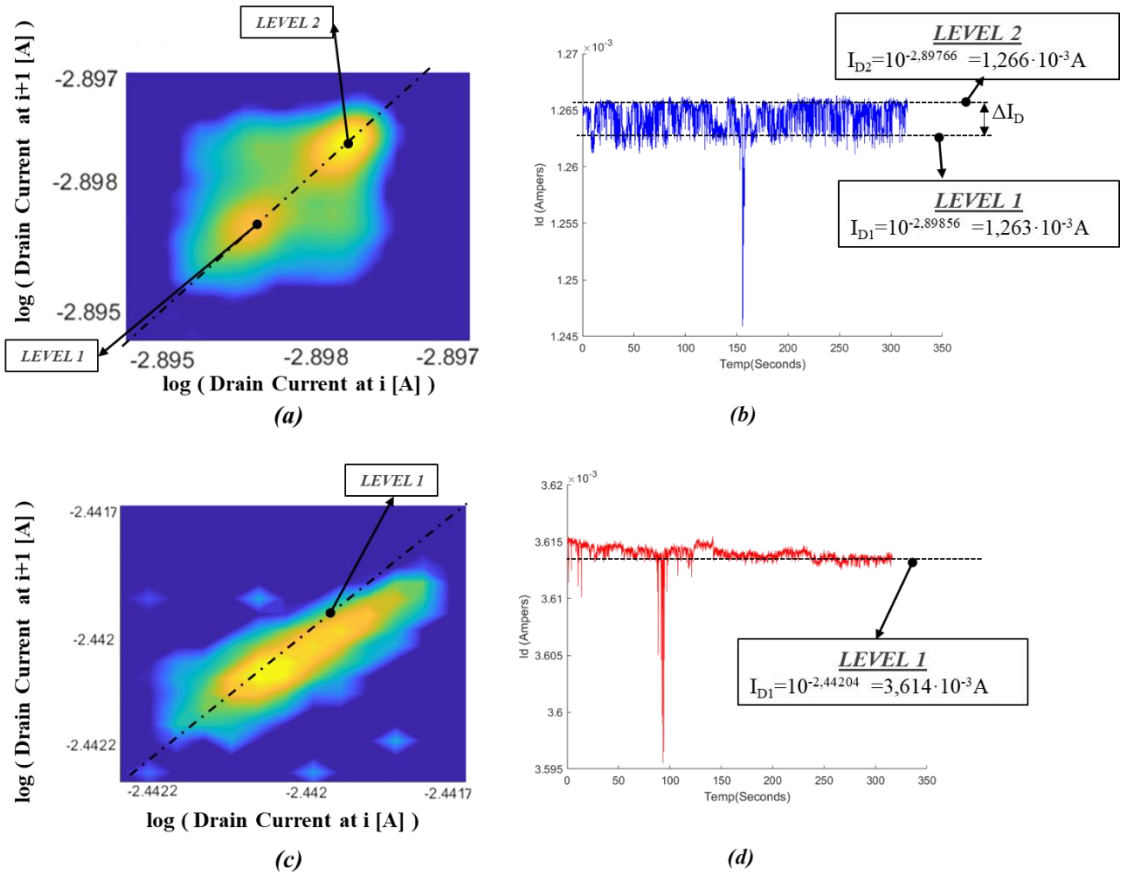


Figure 4-4: (a) W-TLP of the device N1 and (b) its drain current trace, when the voltages applied in (a) and (b) are V_{G1}= 0,5V and V_{BG1}=0V. (c) W-TLP of the device N1 and (d) its drain current trace, when the voltages applied in (c) and (d) are V_{G2} =1V and V_{BG2} = 0 V. W=10µm, L=50nm.

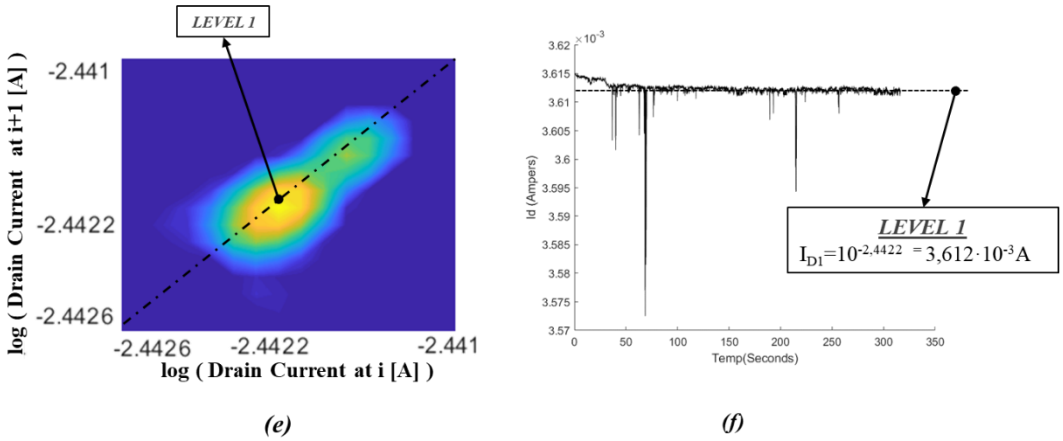


Figure 4-3: (e) W-TLP of the device N1 and (f) its drain current trace, when the voltages applied in (e) and (f) are V_{G3}=1V and V_{BG3}= -15 V. The device measured here is the N1 and have the next dimensions: W=10µm, L=50nm.

4.4 Batch of RTN Measurements

Tables 4-1 resume the first characterization (applied V_{G1}=0.5V and V_{BG1}=0V). The yellow colored graphs are the ones that are equal in both tables (only was used one device for these channel dimensions, in the others plots we have used two different devices of same dimensions). As observed, RTN is no much present in these devices. Only in the case of the smallest dimensions (W=300nm and L=10nm) two peaks are detected, in both experiments. However, in the unique experiment done for the largest dimensions (W=10µm and L=50nm) analyzed in Section 4.3, a clear presence of a single defect that produce fluctuation between two discrete levels when is trapped and detrapped.

When comparing the traces obtained with V_G=0.5V and V_G=1V (with V_{GB}=0V) (Tables 4-1 and 4-2 respectively), RTN signals seem to be more appreciable. But again (V_G=1V in tables 4-2), no much defects are detected despite the larger bias applied.

The effect of the back gate (V_{BG}) is summarized in Tables 4-3 were the V_G = 1V and V_{BG} = -15V. As observed, the few RTN events detected for a V_{BG} = 0V are reduced, suggesting that back gate contributes to stabilize the RTN. However, more experiments are required in this direction. Finally, to summarize it, and making an overview, RTN seems to be more significant in the case of the smallest width (W=300nm). This result is agreement with the literature because the effect of a single trap in the middle of the channel will affect as much as smaller is the channel width. However, once again, this

observation must be corroborated by doing more experiments in more samples. In that sense, future experiments must also account for different time's resolutions in order to capture other defects that are captured and emitted faster than the few ones observed with the presented experiments. So that, different time resolutions and time windows should studied to investigate if there are defects that appear in a lower time scale.

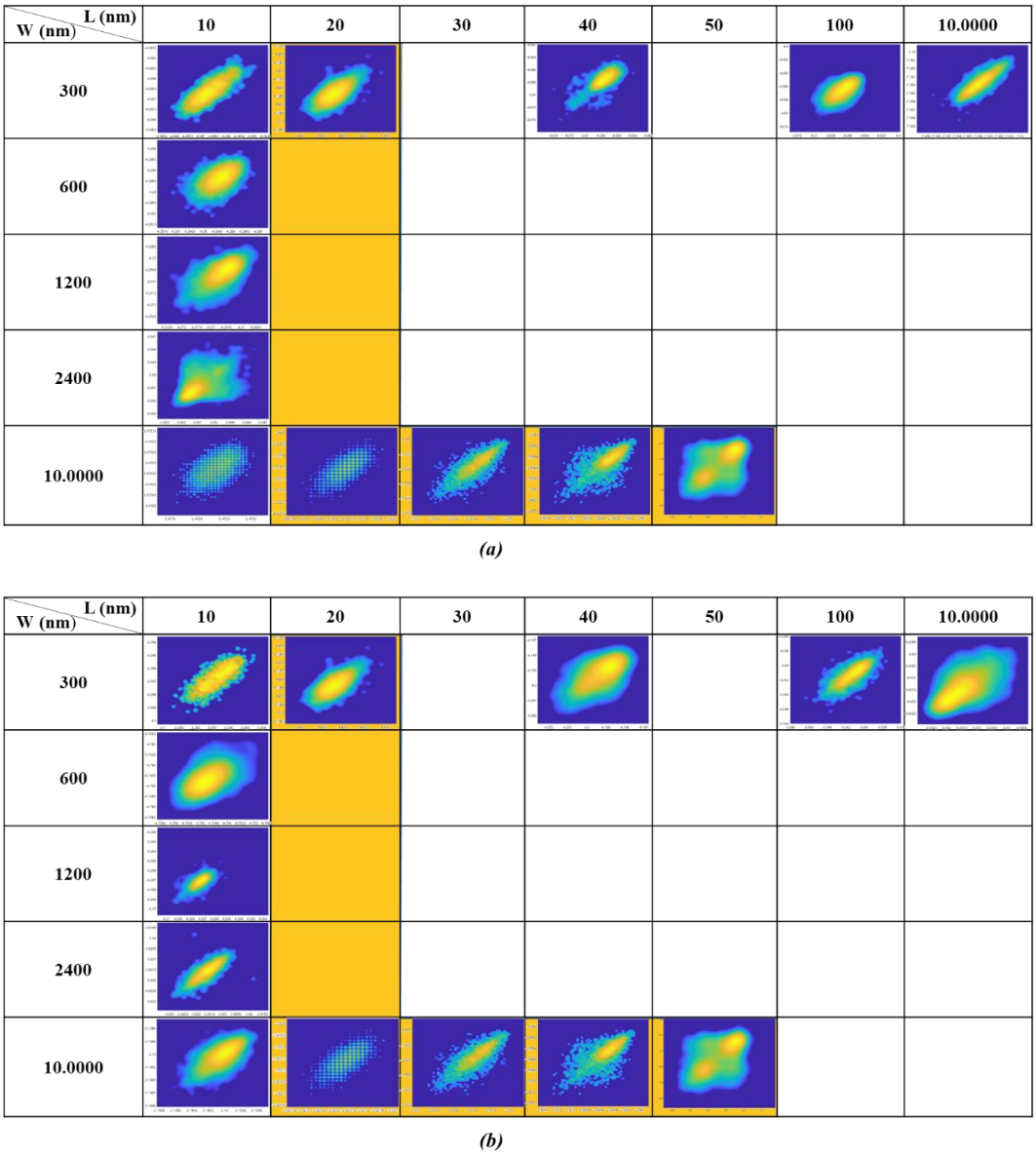
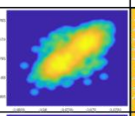
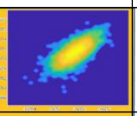
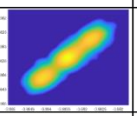
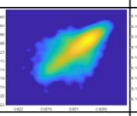
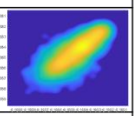
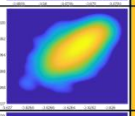
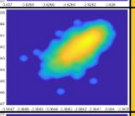
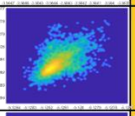
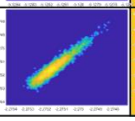
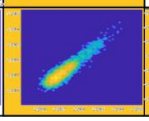
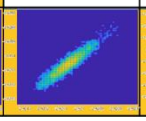
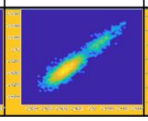
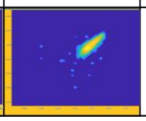
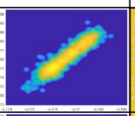
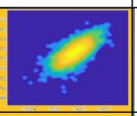
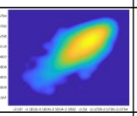
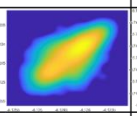
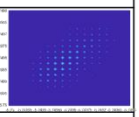
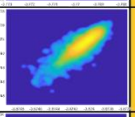
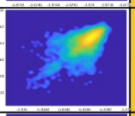
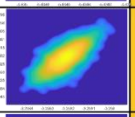
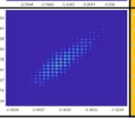
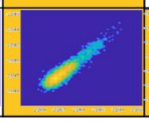
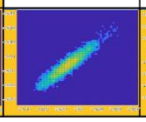
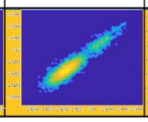
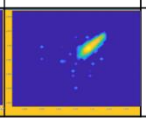


Table 4-1: W-TLP results for a V_{G1} = 0.5V and V_{BG1} = 0V, for the different devices dimension, where yellow colored plots correspond to the devices which are equal in both tables (only one device was analyzed for these channel dimensions).

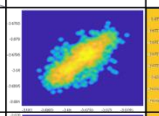
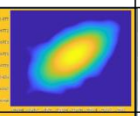
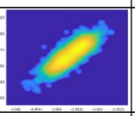
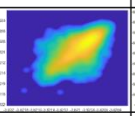
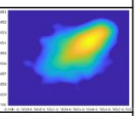
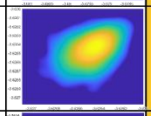
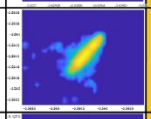
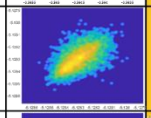
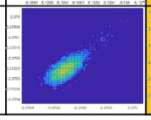
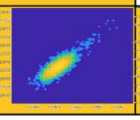
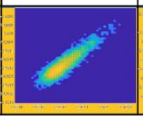
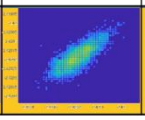
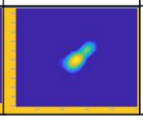
W (nm) \ L (nm)	10	20	30	40	50	100	10.0000
300							
600							
1200							
2400							
10.0000							

(a)

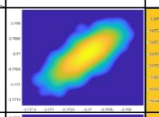
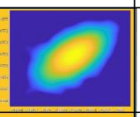
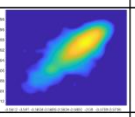
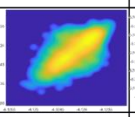
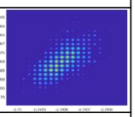
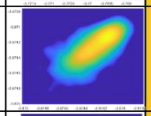
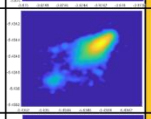
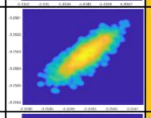
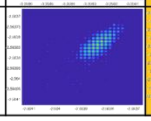
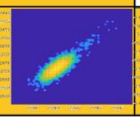
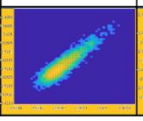
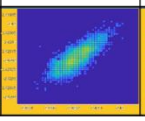
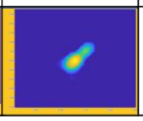
W (nm) \ L (nm)	10	20	30	40	50	100	10.0000
300							
600							
1200							
2400							
10.0000							

(b)

Table 4-2: W-TLP results for a V_{G2} = 1V and V_{BG2} = 0V, for the different devices dimension, where yellow colored plots correspond to the devices which are equal in both tables (only one device was analyzed for these channel dimensions).

W (nm) \ L (nm)	10	20	30	40	50	100	10.0000
300							
600							
1200							
2400							
10.0000							

(a)

W (nm) \ L (nm)	10	20	30	40	50	100	10.0000
300							
600							
1200							
2400							
10.0000							

(b)

Table 4-3: W-TLP results for a V_{G3} = 1V and V_{BG3} = -15V, for the different devices dimension, where yellow colored plots correspond to the devices which are equal in both tables (only one device was analyzed for these channel dimensions).

Chapter 5

Positive Bias Temperature Instability characterization (PBTI)

In this chapter, the Positive BTI in these N-type UTBB FD-SOI transistors is studied by using the few measurements made in the laboratory. So that, the results obtained in this chapter will not be enough for a wide analysis of this aging mechanism, and much more experiments are required for its characterization. However, initial results can be analyzed and used to plan the next measurements.

In order to activate the PBTI in the studied devices, constant voltage stresses (CVS) with positives bias at the gate terminal were applied during certain time. The back gate was kept to 0V in all the experiments, so that, the effects of the back gate to the activations of this aging mechanism was not studied. In order to obtain the device performance during the stress time, the stresses were interrupted periodically to register the device characteristics in between.

To analyze the PBTI effects in different devices with different channel dimensions, four devices with different channel length were used (10, 25, 40, 100nm). Moreover, to analyze the effects of the stress voltage on the device performance, different gate voltages during the stresses were applied (1.5V, 2.2V and 2.4V). However, it must be highlighted that device channel length and stress voltage were changed from sample to sample at the same time, which difficulties direct comparisons.

5.1 PBTI Effect on the device characteristics.

The Figure 5-1 shows the gate current through the gate oxide during the stress time. The stress voltage was interrupted every 210 seconds to register the device characteristics. Despite the noise observed in the gate current, and some random changes, it can be observed that current increases a little (in absolute value) during a certain stress cycle. Moreover, the trend with the pass of the stress time is that gate current increases as a result of the PBTI stress.

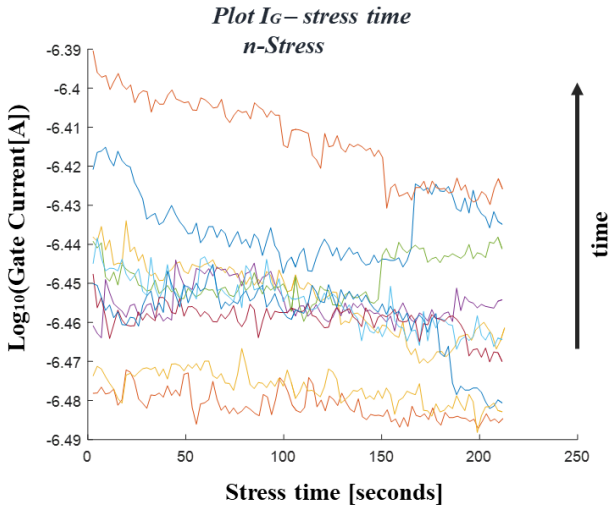


Figure 5-1: Evolution of the characteristic I_G during a constant stress (10 cycles) experiment in a UTBB FD-SOI N-type transistor with a channel of length 40nm and channel width of 300nm split in 10channel of W=30nm.

When observing the I_G-V_G, characteristics (Figure 5-2) of the fresh device (red symbols) and ones obtained after each stress, the tunnel current increase is confirmed (colored lines). Note that this effect is much significant at positives voltages.

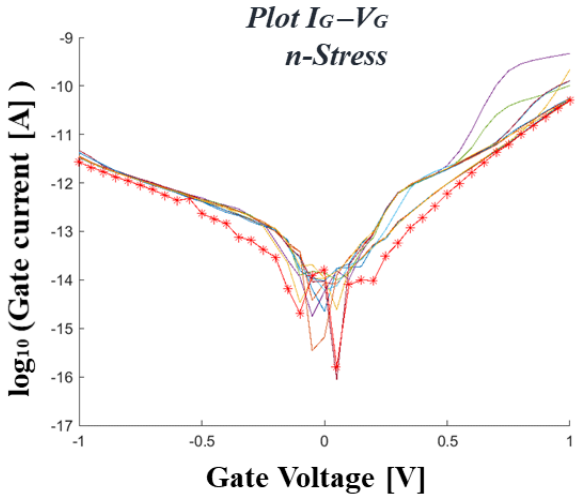


Figure 5-2: Evolution of the characteristic I_G - V_G during a constant stress (10 cycles) experiment in a UTBB FD-SOI N-type transistor with a channel of length 40nm and channel width of 300nm split in 10channel of W=30nm.

In the case of the I_D-V_G characteristic (stress time is 210 seconds), the degradation of the gate oxide produces a reduction of the drive current. As shown in Figure 5-3, drive current

after the stresses (lines without dots) is a little bit lower than the fresh one (line marked with red symbols), which means an increase of V_{th}. Moreover, the threshold voltage is larger after the first stress cycle. After the first interruption of the stress, no significant changes are observed (colored lines seem to be quite similar). It suggests that the changes due to the stress are occurring faster during the first stress time.

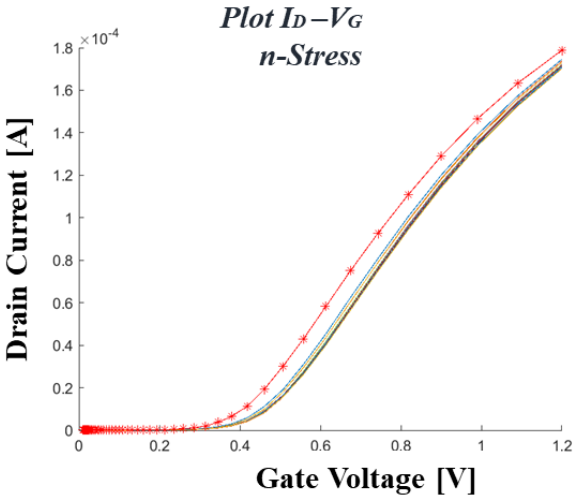


Figure 5-3: Evolution of the characteristic I_D - V_G during a constant stress (10 cycles) experiment in a UTBB FD-SOI N-type transistor with a channel of length 40nm and channel width of 300nm split in 10channel of W=30nm.

Regarding the I_D-V_D, characteristic (Figure 5-4) according with the observations in Figure 5-3, the drive current of the stressed device (colored lines) is lower than the fresh (red symbols), especially in the saturation region.

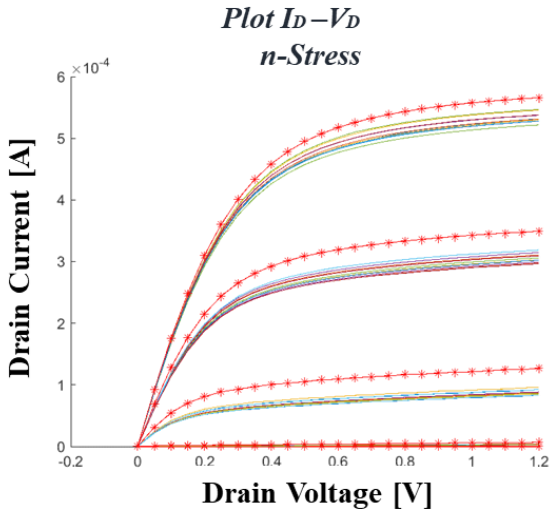


Figure 5-4: Evolution of the characteristic I_D - V_D during a constant stress (10 cycles) experiment in a UTBB FD-SOI N-type transistor with a channel of length 40nm and channel width of 300nm split in 10channel of W=30nm.

5.2 PBTI: Device channel length and stress voltage analysis.

To analyze the degradation as a function of the channel length and the stress voltage, different devices with different channel lengths (but equal channel width, W=300nm) were stressed under different stress conditions/voltages. As mentioned before, not enough measurements were done for complete study of these parameters. Anyway, the four measurements done were compared as an initial analysis. However, more experiments a required to complete the study.

Figure 5-5 shows the threshold voltage evolution registered after each interruption of the stress together with the fresh value for all measurements mentioned above. Note that the first experiment was the one applied to the 10nm-length device, which was programmed with a larger time step. In the next measurements, it was reduced to capture initial stages of the PBTI degradation. Time x-axis was represented in log scale.

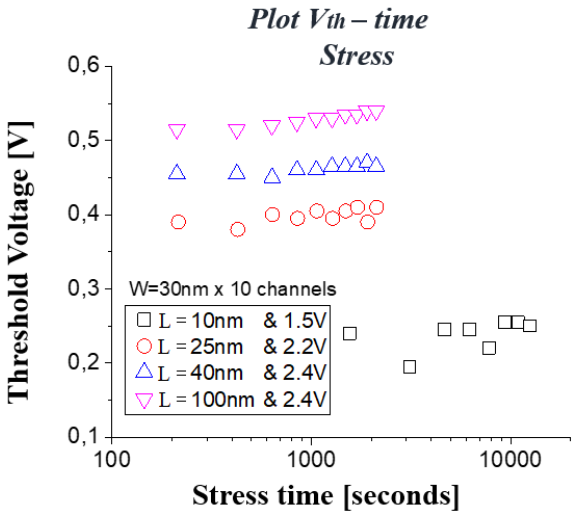


Figure 5-5: Evolution of the threshold voltage during a constant stress (10 cycles) experiment in a UTBB FD-SOI N-type transistor with a different channel length and the same channel width of 300nm split in 10channel of W=30nm.

In order to do a better analysis of the threshold evolution shown at Figure 5-5, there were expressed the values obtained from V_{th} in terms of relative variation respect to the fresh value. Here, the 10nm was discarded because it presents very small values of V_{th}, in Figure 5-6 it can be seen that the relative variation is greater for a high values of stress tension. Furthermore, it is observed that for the same stress voltage (2.4V) the relative variation of V_{th} is very similar.

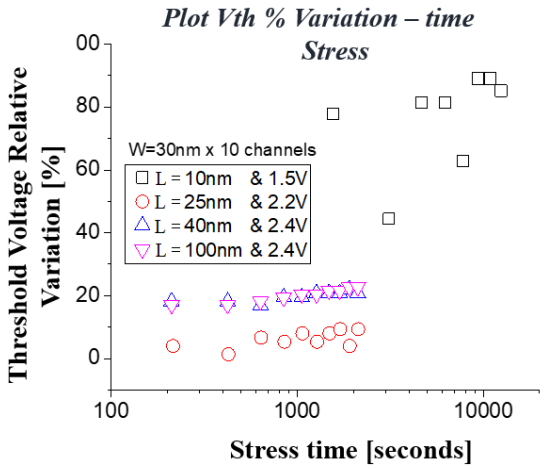


Figure 5-6: Evolution of the relative variation respect to the fresh value during a constant stress (10 cycles) experiment in a UTBB FD-SOI N-type transistor with some different channel lengths and the same channel width of 300nm split in 10channel of W=30nm.

As it is mentioned before, for the device with a channel length of 10nm, the fresh value of the threshold voltage is very small. However, it has a higher relative variation of the threshold voltage, when it was applied a stress voltage of V_G=1.5V. This can be clearly seen in the next Figure 5-7, showing the I_D-V_G characteristic stress evolution of this device.

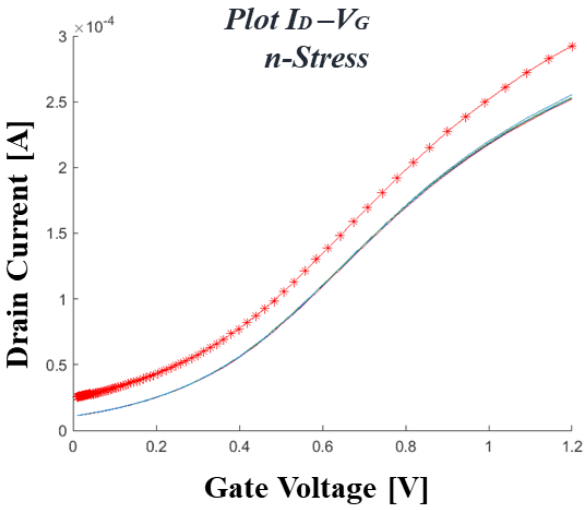


Figure 5-7: Evolution of the characteristic I_D - V_G during a n-constant stress (10 cycles) experiment in a UTBB FD-SOI N-type transistor with a channel of length 10 nm and channel width of 300nm split in 10channel of W=30nm.

Figure 5-8 shows the relative variation in mobility obtained by periodically interrupting stress. How it was explained previously in the Section 3.2, from the I_D-V_G the device mobility is related with this maximum slope in this curve. As can be seen, there was no clear trend between stress voltages, nor between channel lengths, not even between the values obtained in the same measurement/experiment, these being very noisy around 0%. This is an expected result, since PBTI in N-type transistors produces a reduction in threshold voltage, but does not produce changes in carrier mobility. This clearly indicates that PBTI is a degradation mechanism that affects gate oxide, and not channel, so it has an impact on threshold voltage but not on carriers transport.

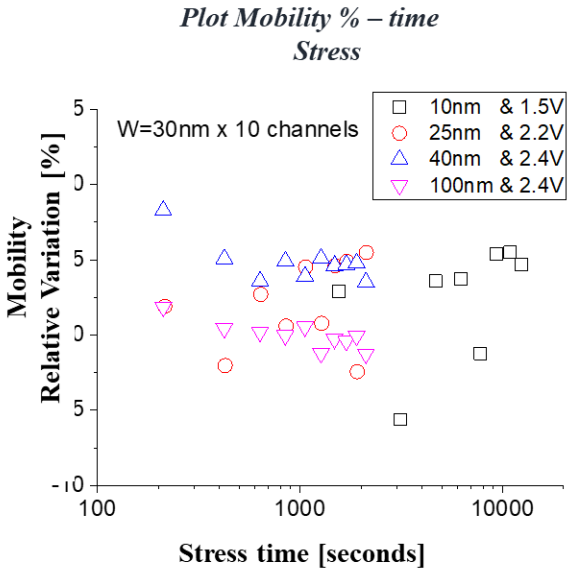


Figure 5-8: Evolution of the relative variation of the mobility during a constant stress (10 cycles) experiment in the UTBB FD-SOI N-type transistor with some different channel lengths and the same channel width of 300nm split in 10channel of W=30nm.

In this chapter it has been studied the PBTI aging in different N-type MOS transistors of various dimensions applying different stresses to the gate voltage, after this it can be concluded that has been observed some dependence of the threshold voltage degradation with the voltage value applied during the stress (CVS).

In terms of mobility, this dependence has not been observed, nor practically degradation in general terms, regardless of the channel length and the voltage applied to the gate during the stress. This is coherent with the prior knowledge about PBTI, which especially degrade the threshold and not the carrier mobility.

About the variation of the threshold voltage mentioned (V_{th}) it reaches the value of approximately of 20% respect to the fresh value, which indicates that it is a rather significant degradation.

Chapter 6

Conclusions

In this work some transistors with the UTBB FD-SOI technology have been studied. This technology is very new and has emerged as a result of the need for the continuous scaling of devices. Therefore, as a new technology it must be studied and characterized, as subjected to the mechanisms of RTN variability and BTI aging. The studied devices have been n-type MOS transistors with a channel length ranged from 10nm to 10µm and a channel width of 300nm up to 10µm.

Regarding the fresh measurements of the device, it has been observed that the characteristic of the gate oxide, tunneling current, depends on the device area. It has also been clearly observed the dependence of the channel current with its width and length. Moreover, the effect of the back gate (V_{BG}) has been analyzed in order to determine how much it influences on the fresh characteristics it has, noting that its effect is negligible since the device characteristics are when applying 0V or -15V to the back gate.

In respect of the fresh RTN measurements, it has been observed (in the most of these experiments) that, when these devices show low variability of the channel current (drain current) due to RTN is registered. However, in some cases the trapping and detrapping of defects has been observed, showing some fluctuations between two levels. The RTN has been studied for three different combinations of gate and back gate voltages. It has been observed that as the gate voltage increases from 0.5V to 1V, the levels due to RTN were slightly clearer, and in addition, more levels appeared in some cases. Finally, when comparing the RTN when a gate voltage of 1V is applied, it seems to decrease for a back gate of V_{BG} = -15V respect to having a back gate of V_{BG} = 0V.

As for PBTI measurements, it's observed a certain degradation of the threshold voltage (V_{th}). It reaches the 20% of variation respect the fresh values, when applying a constant voltage stress of ~ 2.4V at the gate terminal during approximately 2000 seconds.
In addition, the measurements were interrupted every 210 seconds periodically to register this degradation of the threshold voltage as a function of time. It has been observed that the greatest degradation occur during the first stress period, therefore for future measurements it would be interesting to record the variation of the threshold voltage with

shorter time intervals. Regarding the mobility of the carriers, it has not been observed that they have been affected by the applied stresses, according with the PBTI effects reported in the literature for large scaled MOS technologies.

For future measurements, regarding the analysis of the RTN it would be necessary to focus on the dimensions where it is observed more RTN (short channel devices) and deepen the study by different time windows and temporal resolutions, since the measurements made in this work had a very low resolution (very large temporal step), this will probably increase the probability of observing more defects.

Regarding the aging measurements, it would be necessary to continue studying the dependence with the voltage applied during the stress and also to see the effect of the back gate in terms of the activation of the aging mechanisms.

In relation to what has been mentioned before, it would be interesting to study the RTN after degrading the devices, since during the stress defects are generated causing more traps in the channel. Therefore more RTN could be observed, being this a more realistic characterization of the RTN, because over time the devices are degraded. Then it would be very interesting to make a study about how the observed RTN is affected when a degradation is forced to the device.

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